TPS74901
JAJS247K – JUNE 2007 – REVISED JUNE 2024

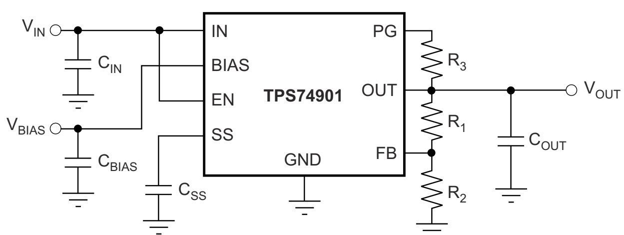
TPS74901 プログラマブル ソフトスタート機能付き、3A 低ドロップアウト リニア レギュレータ

1 特長

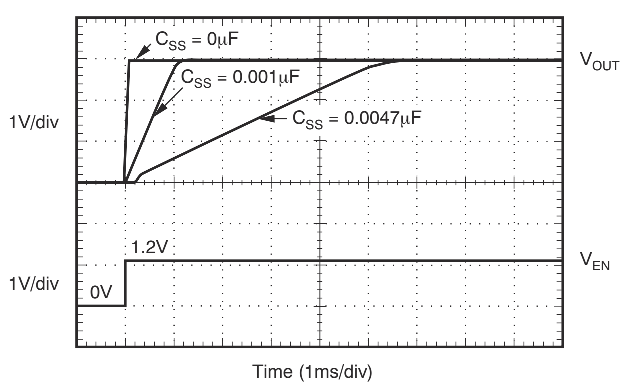
- V_{OUT} 範囲：0.8V～3.6V
- 非常に低い V_{IN} 範囲：0.8V～5.5V
- V_{BIAS} 範囲：2.7V～5.5V
- 低いドロップアウト：3A で 120mV (標準値)
- パワー グッド (PG) 出力により、電源電圧の監視や、他の電源のためのシーケンシング信号の供給が可能
- 入力、負荷、温度に関する精度：1% (新チップ)
- 入力、負荷、温度に関する精度：2% (レガシー チップ)
- 可変スタートアップ突入電流
- V_{BIAS} により、過渡応答性に優れた低 V_{IN} 動作を実現
- 2.2µF 以上の出力コンデンサで安定動作
- パッケージ：
  - 小型の 3mm × 3mm × 1mm VSON
  - 5mm × 5mm × 1mm VQFN および DDPAK-7
- アクティブ High イネーブル

2 アプリケーション

- ネットワーク接続ストレージ (NAS) - エンタープライズ
- ラック サーバー
- ネットワーク インターフェイス カード (NIC)
- 商用ネットワークとサーバーの電源



代表的なアプリケーション回路 (可変)



ターンオン応答

3 概要

TPS74901 低ドロップアウト (LDO) リニア レギュレータは、広範なアプリケーション向けの使いやすく堅牢な電力管理ソリューションです。ソフトスタートをユーザーがプログラムできるので、スタートアップ中の容量性突入電流を低減して、入力電源のストレスを最小限に抑えることができます。ソフトスタートは単調性で、多くの種類のプロセッサおよび特定用途向け IC (ASIC) の電源供給向けに設計されています。イネーブル入力とパワー グッド出力により、外部レギュレータとの間でシーケンシングを簡単に行えます。この優れた柔軟性により、フィールド プログラマブル ゲート アレイ (FPGA)、デジタル信号プロセッサ (DSP)、および特殊なスタートアップ要件を持つ他のアプリケーションのシーケンス要件を満たすソリューションを構成できます。

高精度の基準電圧およびエラー アンプは、負荷、ライン、温度、プロセスの全体にわたって 2% の精度を維持します。本デバイスは 2.2µF 以上の任意のタイプのコンデンサで安定して動作し、-40℃～+125℃で仕様が規定されています。TPS74901 は、小型 (3mm × 3mm) の VSON パッケージおよび小型 (5mm × 5mm) の VQFN パッケージで供給されるため、非常に小さいトータル ソリューション サイズを実現できます。このデバイスは、DDPAK-7 パッケージでも供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS74901	RGW (VQFN、20)	5mm × 5mm
	KTW (DDPAK/TO-263、7)	8.89mm × 10.1mm
	DRC (VSON、10)	3mm × 3mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

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4 Pin Configuration and Functions

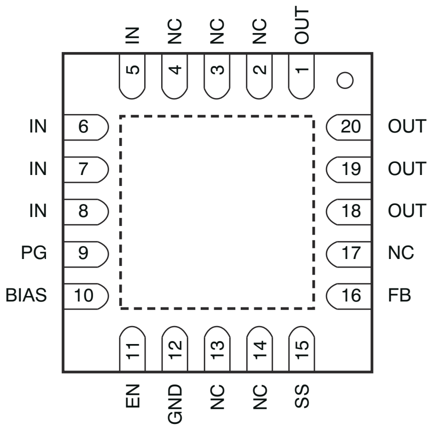


図 4-1. RGW Package, 20-Pin VQFN (Top View)

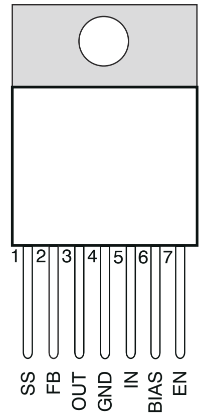


図 4-2. KTW Package (Legacy Chip), 7-Pin DDPAK/ TO-263 (Top View)

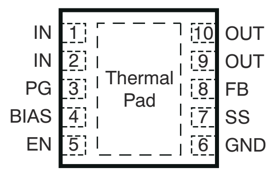


図 4-3. DRC Package, 10-Pin VSON With Thermal Pad (Top View)

表 4-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DDPAK/TO-263	VQFN	VSON		
BIAS	6	10	4	I	Bias input voltage for error amplifier, reference, and internal control circuits.
EN	7	11	5	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
FB	2	16	8	I	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
GND	4	12	6	—	Ground
IN	5	5, 6, 7, 8	1, 2	I	Unregulated input to the device.
NC	—	2, 3, 4, 13, 14, 17	—	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	3	1, 18, 19, 20	9, 10	O	Regulated output voltage. A small capacitor (total typical capacitance ≥ 2.2µF, ceramic) is needed from this pin to ground to assure stability.
PG	—	9	3	O	Power-good (PG) is an open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pullup resistor from 10kΩ to 1MΩ must be connected from this pin to a supply up to 5.5V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
SS	1	15	7	—	Soft-start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 100µs.
Thermal Pad				—	Solder to the ground plane for increased thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{PG}	Power-good voltage	–0.3	6	V
I_{PG}	PG sink current	0	1.5	mA
V_{SS}	Soft-start voltage	–0.3	6	V
V_{FB}	Feedback voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See Thermal Information		
T_J	Junction Temperature	–40	150	°C
T_{stg}	Storage Temperature	–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (V_{IN})		5.5	V
V_{EN}	Enable supply voltage			5.5	V
V_{BIAS} [1]	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})[2]		5.5	V
V_{OUT}	Output voltage	0.8		3.6	V
I_{OUT}	Output current	0		3	A
C_{OUT}	Output capacitor	2.2			µF
C_{IN}	Input capacitor[3]	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(3) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

5.4 Thermal Information

THERMAL METRIC[1]		TPS749					UNIT
		RGW (VQFN)	RGW (VQFN) [2]	KTW (TO-263)	DRC (VSON)	DRC (VSON) [2]	
		20 PINS	20 PINS	7 PINS	10 PINS	10 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	38.1	34.7	33.8	48.1	47.2	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	36.3	31	35.9	60.3	63.7	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	17.5	13.5	25	22.4	19.5	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	0.7	1.4	6	1.0	4.2	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	17.6	13.5	23.6	22.6	19.4	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	6.2	3.6	N/A	4.3	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.
(2) New Chip.

5.5 Electrical Characteristics

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference (Adj.)	T_A = +25°C	0.798	0.802	0.806	V
V_{OUT}	Output voltage range	V_{IN} = 5V, I_{OUT} = 3A	V_{REF}		3.6	V
V_{OUT}	Accuracy (RGW and SON packages)[1]	V_{OUT} + 2.2V ≤ V_{BIAS} ≤ 5.5 V, 50mA ≤ I_{OUT} ≤ 3A (Legacy Chip)	–2	±0.5	2	%
		V_{OUT} + 2.2V ≤ V_{BIAS} ≤ 5.5V, 50mA ≤ I_{OUT} ≤ 3A (New Chip)	–1	±0.3	1	
	Accuracy (KTW package)[1]	V_{OUT} + 2.4V ≤ V_{BIAS} ≤ 5.5V, 50mA ≤ I_{OUT} ≤ 3A (Legacy Chip Only)	–2	±0.5	2	
$ΔV_{OUT(ΔVIN)}$	Line regulation	$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5V (Legacy Chip)		0.03		%/V
		$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5V (New Chip)		0.001		
$ΔV_{OUT(ΔIOUT)}$	Load regulation	50mA ≤ I_{OUT} ≤ 3A		0.09		%/A
V_{DO}	V_{IN} dropout voltage[2]	I_{OUT} = 3A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 3.25V[3] (Legacy Chip)		120	280	mV
		I_{OUT} = 3A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 3.25V[3] (New Chip)		120	200	
	V_{BIAS} dropout voltage[2]	I_{OUT} = 3A, V_{IN} = V_{BIAS} (Legacy Chip)		1.31	1.75	V
		I_{OUT} = 3A, V_{IN} = V_{BIAS} (New Chip)		1.45	1.6	
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT(nom)}$, RGW Package	3.9	4.6	5.5	A
		V_{OUT} = 80% × $V_{OUT(nom)}$, KTW Package	3.8	4.6	5.5	
I_{BIAS}	BIAS pin current	Legacy Chip		1	2	mA
		New Chip		1	1.2	
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4V (Legacy Chip)		1	50	µA
I_{SHDN} (smart enable)		V_{EN} ≤ 0.4V, V_{IN} = V_{BIAS} = 5.5V (New Chip)		0.85	2.75	

5.5 Electrical Characteristics (続き)

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{FB}	Feedback pin current	Legacy Chip	–1	0.15	1	µA
		New Chip	–30	0.15	30	nA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5A, V_{IN} = 1.8 V, V_{OUT} = 1.5V		60		dB
		300 kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		30		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (Legacy Chip)		50		dB
		1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (New Chip)		57		
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (Legacy Chip)		30		
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (New Chip)		49		
V_n	Output noise voltage	BW = 100Hz to 100kHz, I_{OUT} = 3A, C_{SS} = 1nF (Legacy Chip)		25		µVrms x Vout
		BW = 100 Hz to 100 kHz, I_{OUT} = 3A, C_{SS} = 1nF (New Chip)		20		
t_{STR}	Minimum start-up time	R_{LOAD} for I_{OUT} = 1A, C_{SS} = open (Legacy Chip)		200		µs
		R_{LOAD} for I_{OUT} = 1A, C_{SS} = open (New Chip)		250		
I_{SS}	Soft-start charging current	V_{SS} = 0.4V (Legacy Chip)		440		nA
		V_{SS} = 0.4V (New Chip)		530		
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			50		mV
$V_{EN(dg)}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5V (Legacy Chip)		0.1	1	µA
		V_{EN} = 5V (New Chip)		0.1	0.25	
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1mA (sinking), V_{OUT} < V_{IT} (Legacy Chip)			0.3	V
		I_{PG} = 1mA (sinking), V_{OUT} < V_{IT} (New Chip)			0.12	
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25V, V_{OUT} > V_{IT} (Legacy Chip)		0.1	1	µA
		V_{PG} = 5.25V, V_{OUT} > V_{IT} (New Chip)		0.001	0.05	
T_J	Operating junction temperature		–40		125	℃
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		℃
		Reset, temperature decreasing		140		

5.5 Electrical Characteristics (続き)

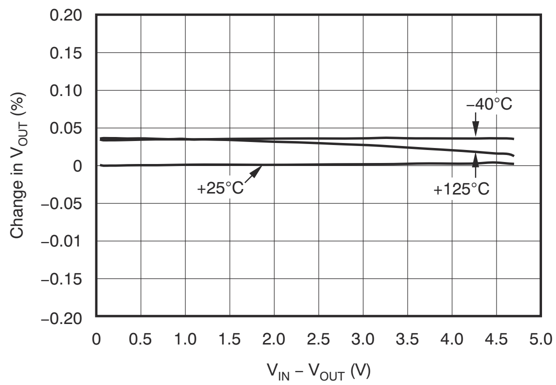
at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 μF, C_{IN} = C_{OUT} = 10 μF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PULLDOWN}$		V_{BIAS} = 5V, V_{EN} = 0 V		0.83		kΩ

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 5-11.

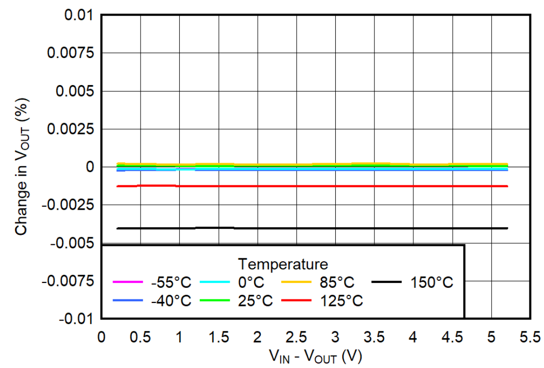
5.6 Typical Characteristics: I_{OUT} = 50mA

at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF (unless otherwise noted)



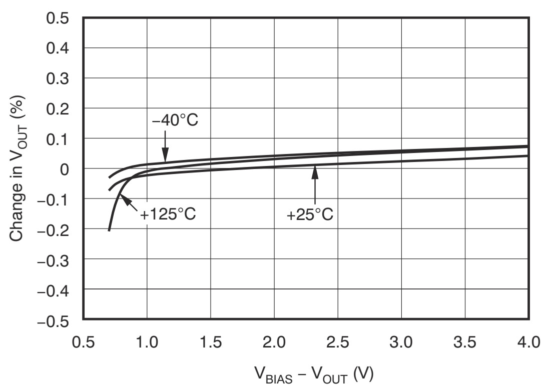
Legacy chip

図 5-1. V_{IN} Line Regulation



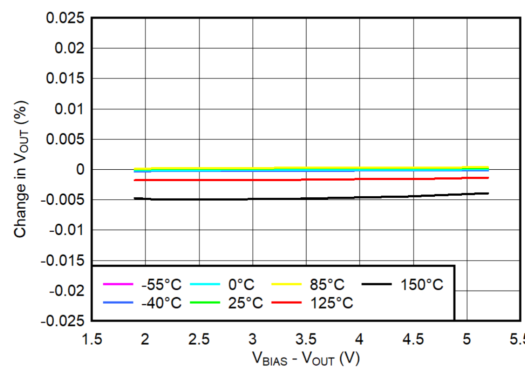
New chip

図 5-2. V_{IN} Line Regulation



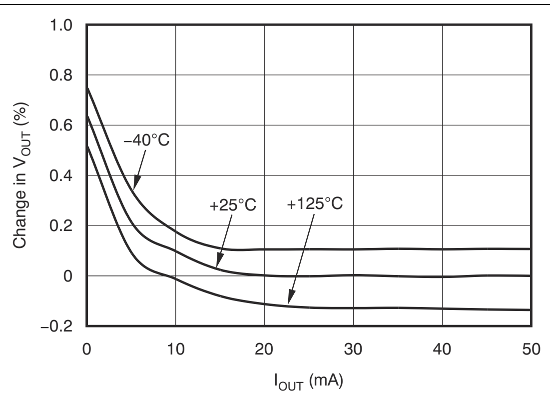
Legacy chip

図 5-3. V_{BIAS} Line Regulation



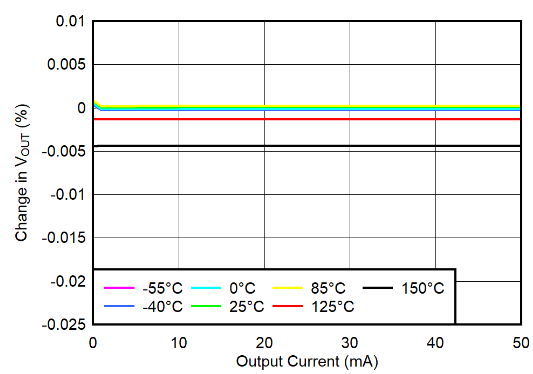
New chip

図 5-4. V_{BIAS} Line Regulation



Legacy chip

図 5-5. Load Regulation at Light Load

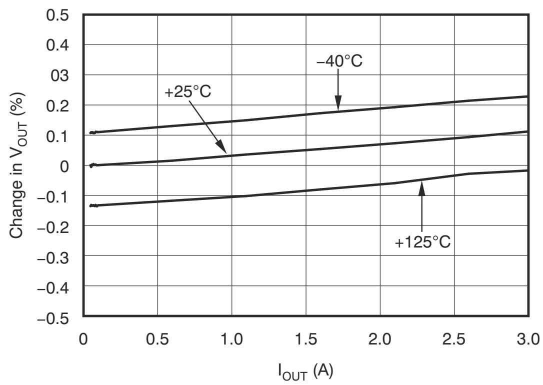


New chip

図 5-6. Load Regulation at Light Load

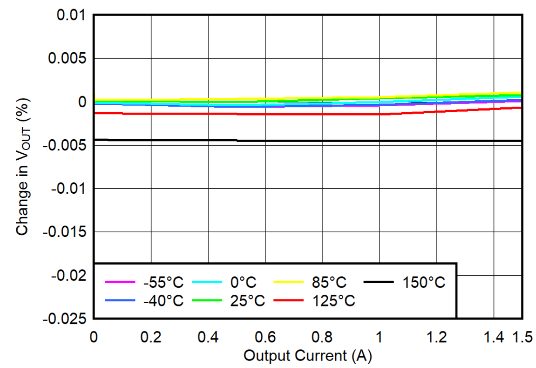
5.6 Typical Characteristics: I_{OUT} = 50mA (continued)

at T_J = 25°C, $V_{IN} = V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, $V_{EN} = V_{IN}$, C_{IN} = 1μF, C_{BIAS} = 4.7μF, and C_{OUT} = 10μF (unless otherwise noted)



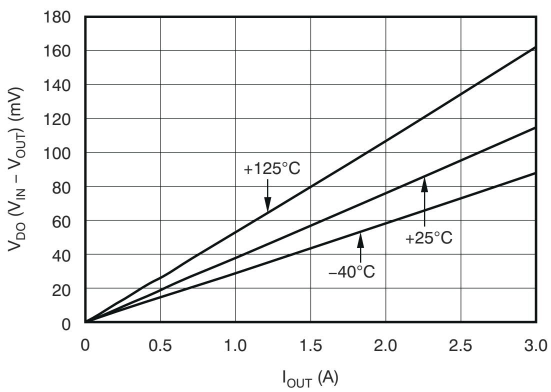
Legacy chip

図 5-7. Load Regulation



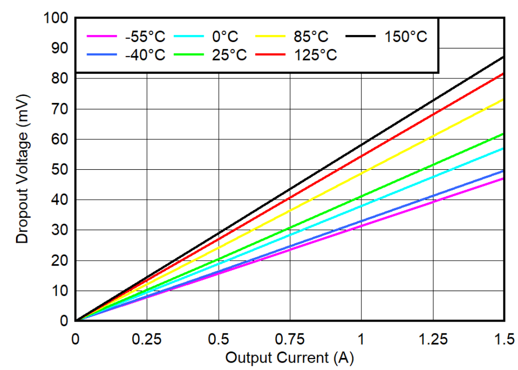
New chip

図 5-8. Load Regulation



Legacy chip

図 5-9. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)



New chip

図 5-10. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

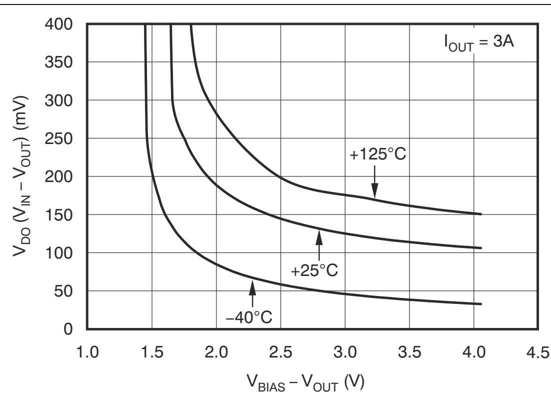
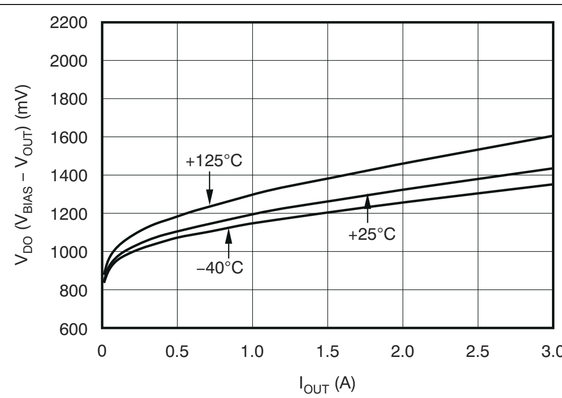


図 5-11. V_{IN} Dropout Voltage vs V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

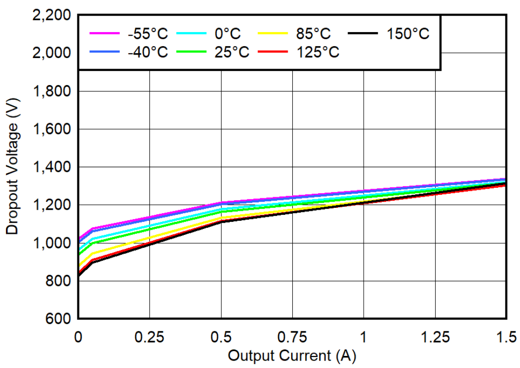


Legacy chip

図 5-12. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

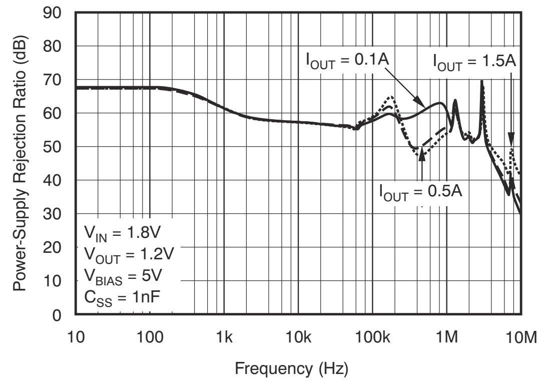
5.6 Typical Characteristics: I_{OUT} = 50mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF (unless otherwise noted)



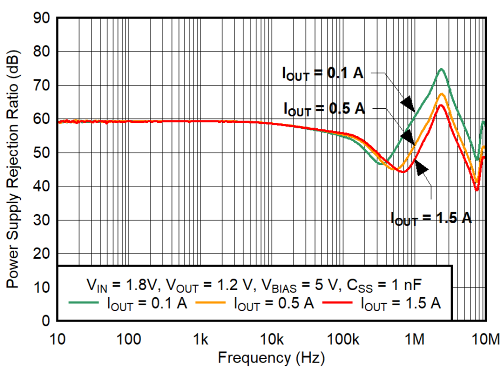
New chip

図 5-13. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)



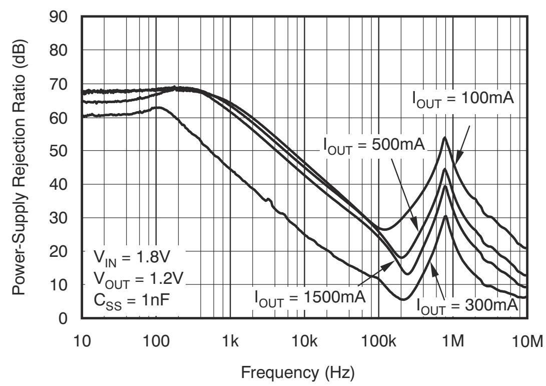
Legacy chip

図 5-14. V_{BIAS} PSRR vs Frequency



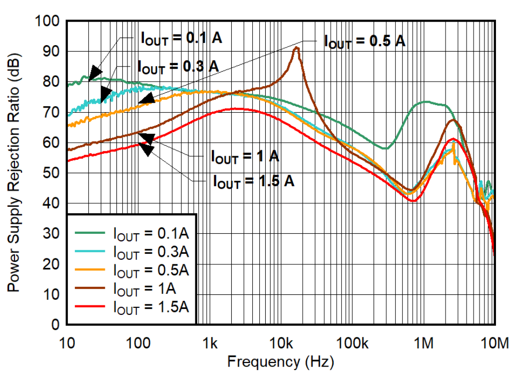
New chip

図 5-15. V_{BIAS} PSRR vs Frequency



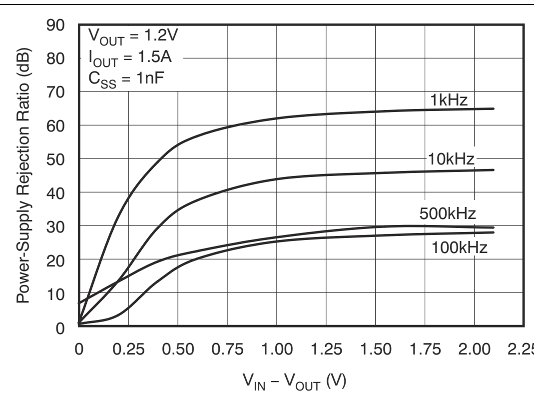
Legacy chip

図 5-16. V_{IN} PSRR vs Frequency



New chip

図 5-17. V_{IN} PSRR vs Frequency

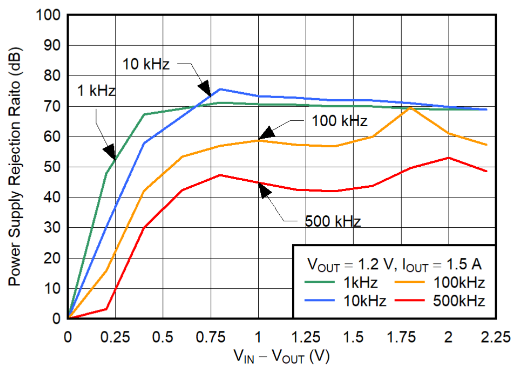


Legacy chip

図 5-18. V_{IN} PSRR vs (V_{IN} – V_{OUT})

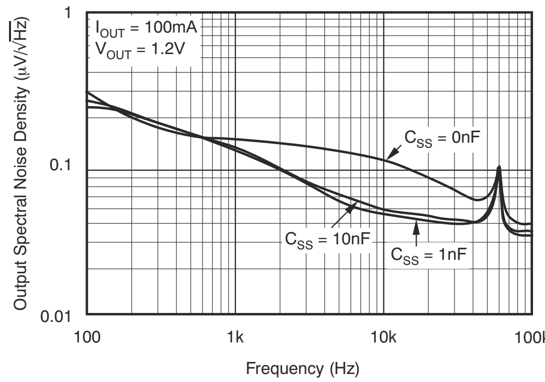
5.6 Typical Characteristics: I_{OUT} = 50mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF (unless otherwise noted)



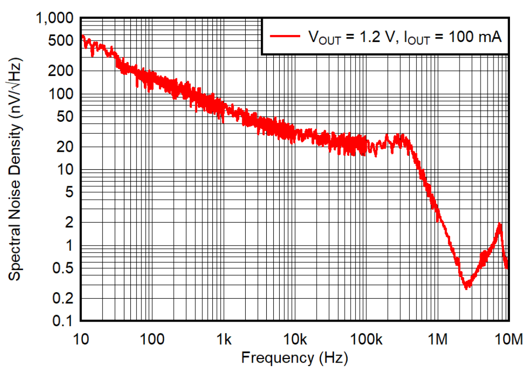
New chip

図 5-19. V_{IN} PSRR vs (V_{IN} – V_{OUT})



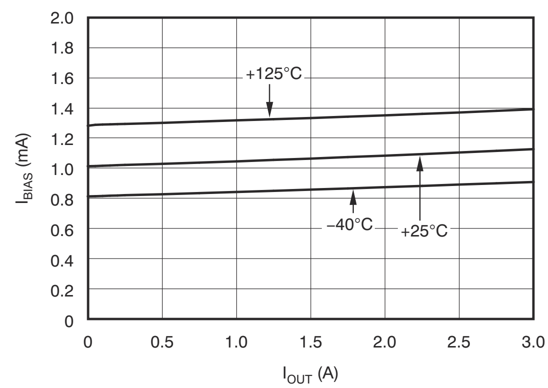
Legacy chip

図 5-20. Noise Spectral Density



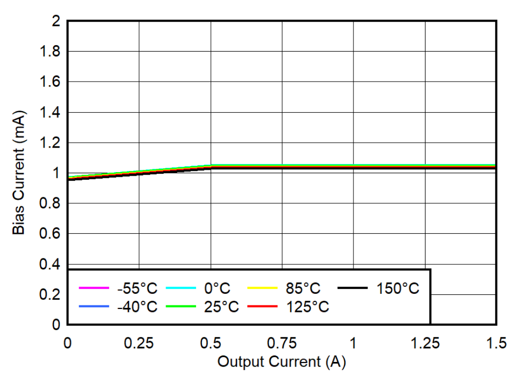
New chip

図 5-21. Noise Spectral Density



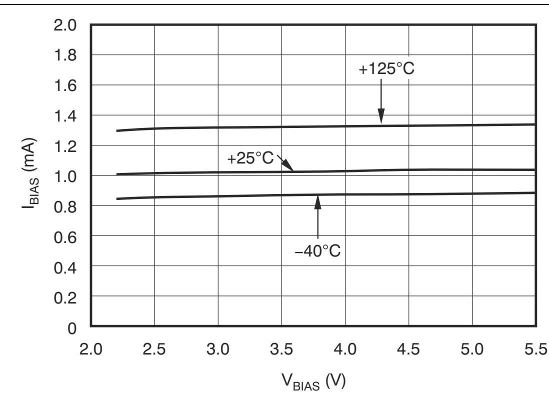
Legacy chip

図 5-22. BIAS Pin Current vs I_{OUT} and Temperature (T_J)



New chip

図 5-23. BIAS Pin Current vs Output Current and Temperature (T_J)

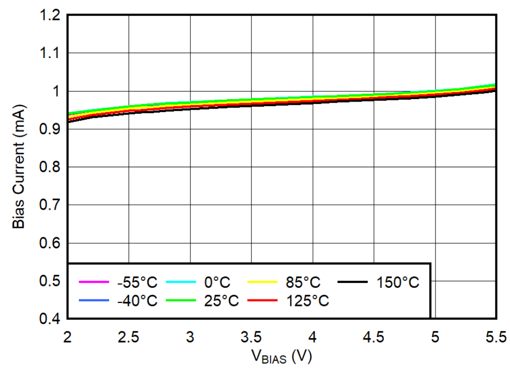


Legacy chip

図 5-24. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)

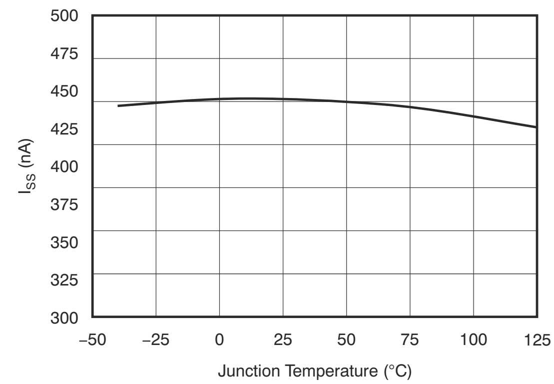
5.6 Typical Characteristics: I_{OUT} = 50mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1μF, C_{BIAS} = 4.7μF, and C_{OUT} = 10μF (unless otherwise noted)



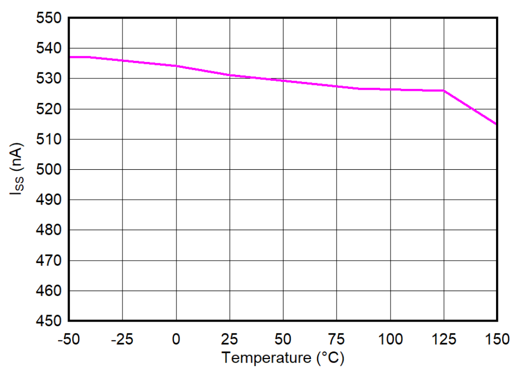
New chip

図 5-25. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)



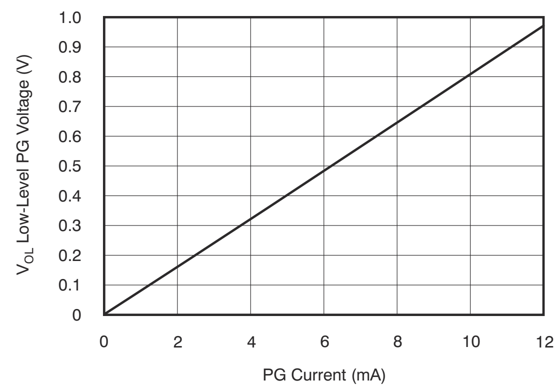
Legacy chip

図 5-26. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)



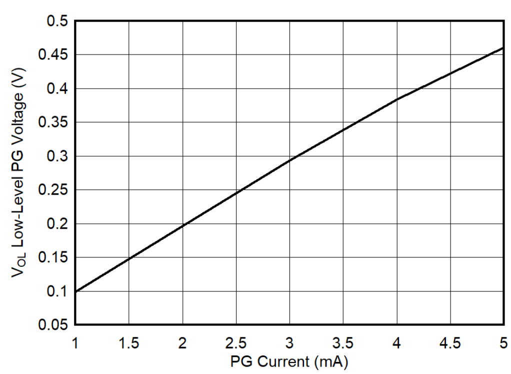
New chip

図 5-27. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)



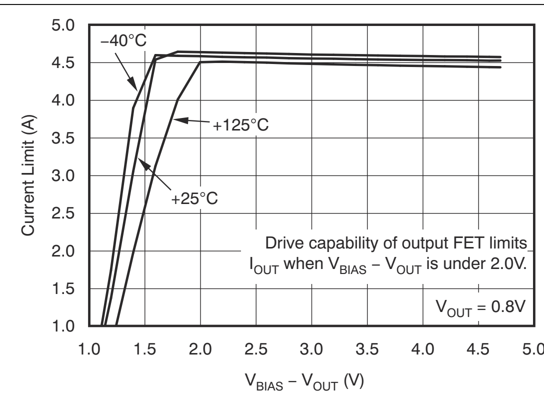
Legacy chip

図 5-28. Low-Level PG Voltage vs Current



New chip

図 5-29. Low-Level PG Voltage vs Current

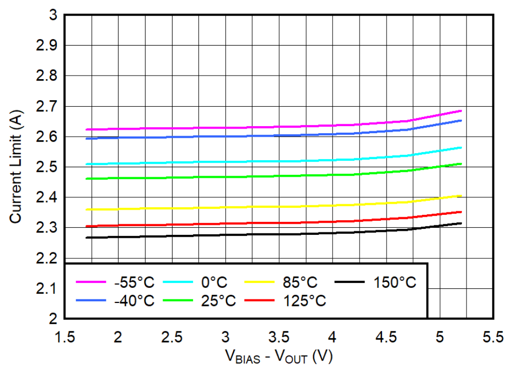


Legacy chip

図 5-30. Current Limit vs (V_{BIAS} – V_{OUT})

5.6 Typical Characteristics: I_{OUT} = 50mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF (unless otherwise noted)

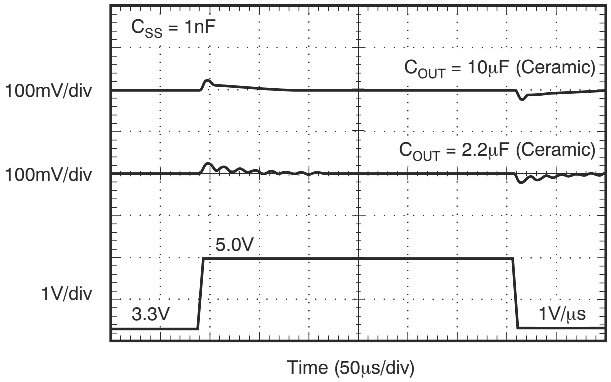


New chip

図 5-31. Current Limit vs (V_{BIAS} – V_{OUT})

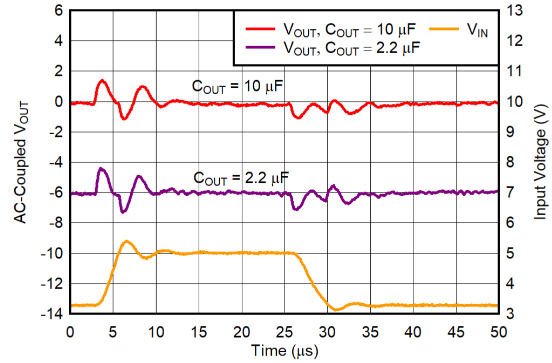
5.7 Typical Characteristics: I_{OUT} = 1 A

at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 1A, V_{EN} = V_{IN} = 1.8V, V_{OUT} = 1.5V, C_{IN} = 1μF, C_{BIAS} = 4.7μF, and C_{OUT} = 10μF (unless otherwise noted)



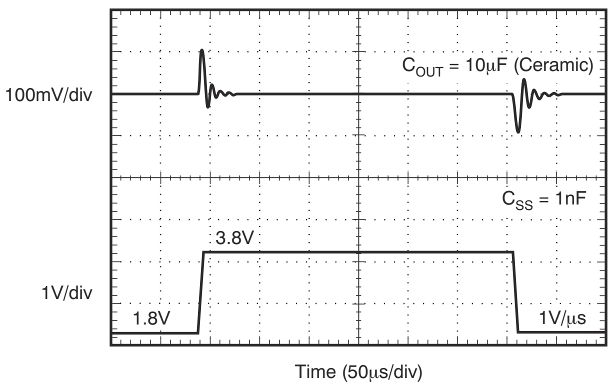
Legacy chip

図 5-32. V_{BIAS} Line Transient



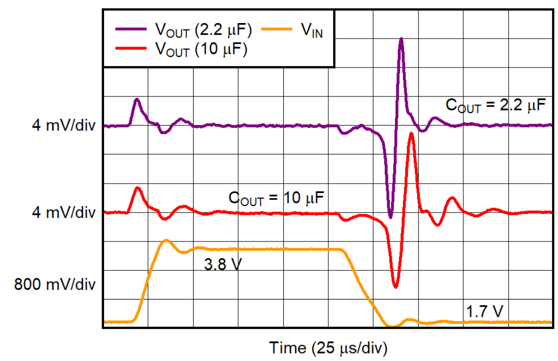
New chip

図 5-33. V_{BIAS} Line Transient



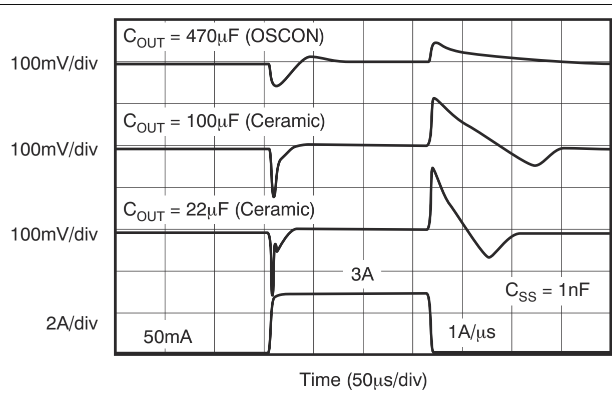
Legacy chip

図 5-34. V_{IN} Line Transient



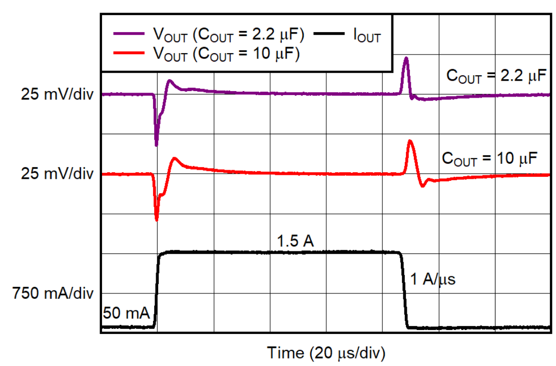
New chip

図 5-35. V_{IN} Line Transient



Legacy chip

図 5-36. Output Load Transient Response

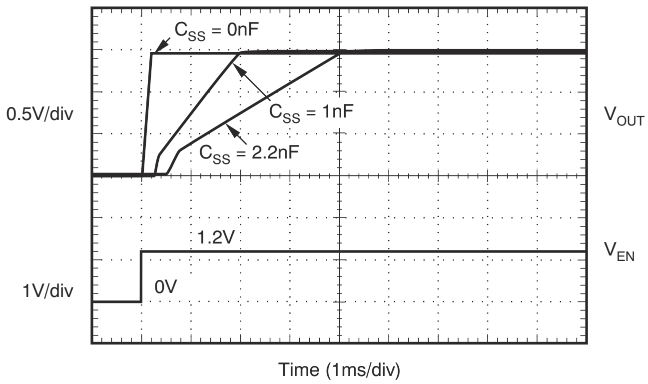


New chip

図 5-37. Output Load Transient Response

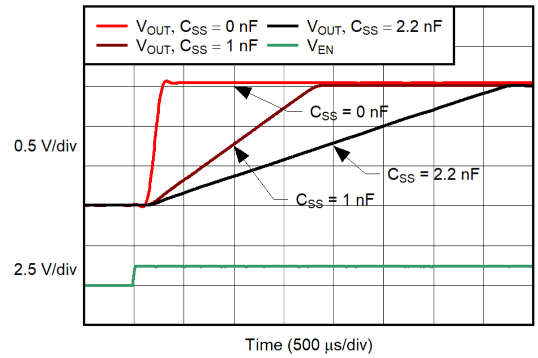
5.7 Typical Characteristics: I_{OUT} = 1 A (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 1A, V_{EN} = V_{IN} = 1.8V, V_{OUT} = 1.5V, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF (unless otherwise noted)



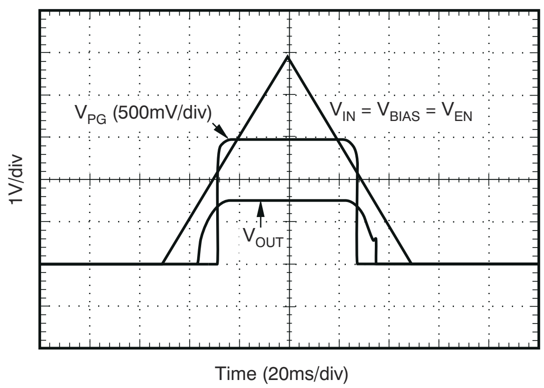
Legacy chip

図 5-38. Turn-On Response



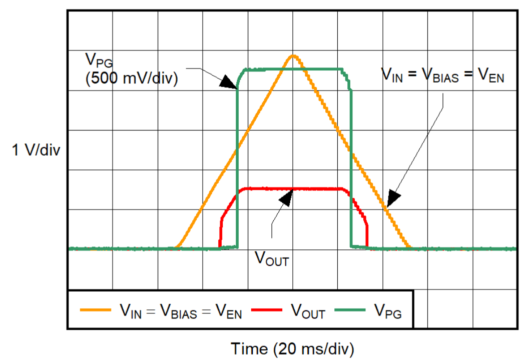
New chip

図 5-39. Turn-On Response



Legacy chip

図 5-40. Power-Up and Power-Down



New chip

図 5-41. Power-Up, Power-Down

6 Detailed Description

6.1 Overview

The TPS74901 is a low-dropout (LDO) regulator that features soft-start capabilities. This regulator uses a low-current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very-low input and output voltages.

Using an NMOS pass transistor offers several critical advantages for many applications. Unlike a p-channel metal-oxide-semiconductor field effect transistor (PMOS) topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74901 to be stable with any capacitor with a value of 2.2µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS74901 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor-intensive systems.

6.2 Functional Block Diagrams

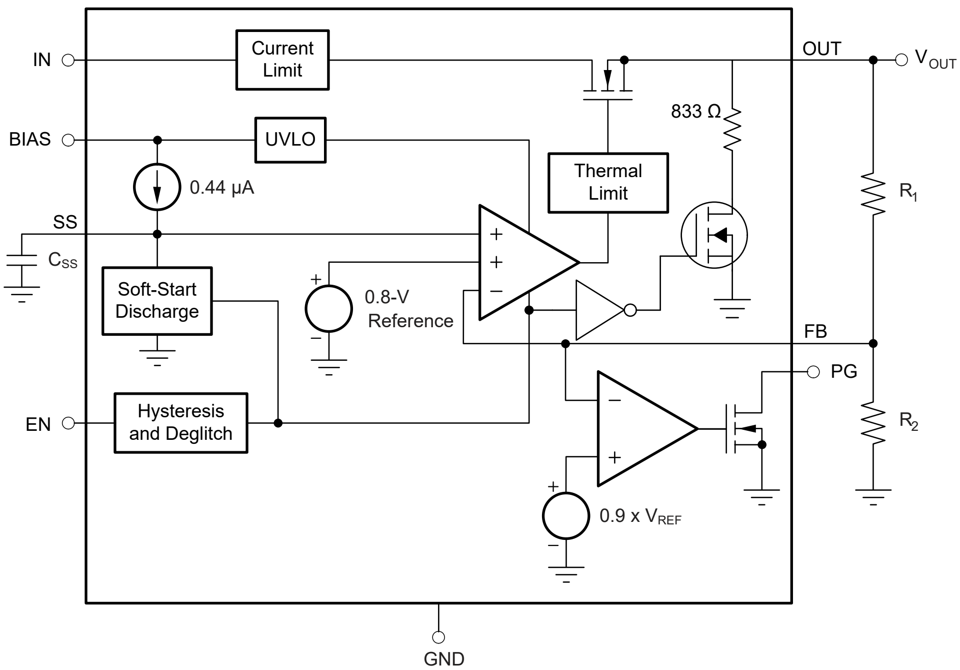


図 6-1. Legacy Chip Functional Block Diagram

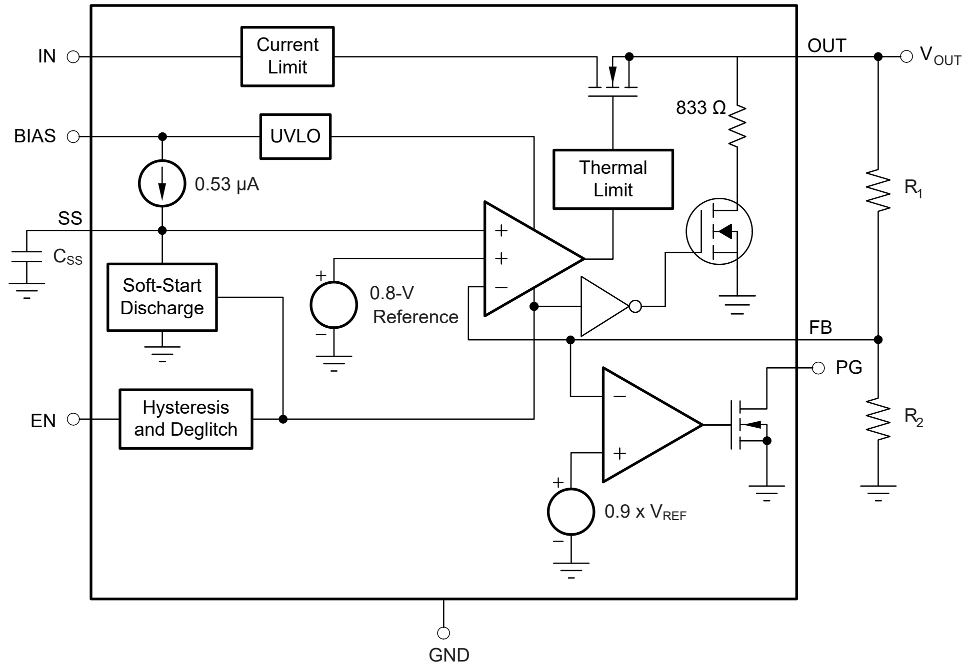


図 6-2. New Chip Functional Block Diagram

6.3 Feature Description

6.3.1 Enable and Shutdown

The enable (EN) pin is active high and is compatible with standard digital-signaling levels. V_{EN} below 0.4V turns the regulator off and V_{EN} above 1.1V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS74901 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50mV of hysteresis and a deglitch circuit to help avoid ON-OFF cycling because of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8V and varies with temperature and process variations. Temperature variation is approximately –1mV/°C; process variation accounts for most of the rest of the variation to the 0.4V and 1.1V limits. If precise turn-on timing is required, a fast rise-time signal must be used to enable the TPS74901.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, then connect EN as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

The TPS749 has an internal active pulldown circuit that connects the output to GND through an 833Ω resistor when the device is disabled. This resistor discharges the output with a time constant of:

$$\tau = \left(\frac{833 \times R_L}{833 + R_L}\right) \times C_{OUT}$$

6.3.2 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5V or lower rail through an external pullup resistor. This pin requires at least 1.1V on V_{BIAS} to have a valid output. The PG output is high-impedance when V_{OUT} is greater than V_{IT} + V_{HYS}. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1mA, so the pullup resistor for PG must be in the range of 10kΩ to 1MΩ. PG is only provided on the VQFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

6.3.3 Internal Current Limit

The TPS74901 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 4A and maintain regulation. The current limit responds in approximately 10µs to reduce the current during a short-circuit fault.

The internal current-limit protection circuitry of the TPS74901 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS74901 above the rated current degrades device reliability.

6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heat sinking. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74901 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS74901 into thermal shutdown degrades device reliability.

6.4 Device Functional Modes

表 6-1 lists the conditions that lead to the different modes of operation.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	V_{BIAS}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}(V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} \geq V_{OUT} + V_{DO}(V_{BIAS})$	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO}(V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} < V_{OUT} + V_{DO}(V_{BIAS})$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)		$V_{EN} < V_{EN(low)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	—	$T_J > 165°C$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass transistor is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Input, Output, and BIAS Capacitor Requirements

The device is designed to be stable for all available types of and values of output capacitors ≥ 2.2µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pin strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7µF. Good quality, low-ESR capacitors must be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors must be placed as close as possible to the pins for optimum performance.

7.1.2 Transient Response

The TPS74901 is designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance otherwise does. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see 図 5-36 in the *Typical Characteristics* section. Because the TPS74901 is stable with output capacitors as low as 2.2µF, many applications can need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device can be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive high-value capacitors at the LDO output.

7.1.3 Dropout Voltage

The TPS74901 offers very low dropout performance, making the device designed for high-current low V_{IN} and low V_{OUT} applications. The low dropout of the TPS74901 allows the device to be used in place of a DC/DC converter and still achieve good efficiencies. This capability provides designers with the power architecture for applications to achieve the smallest, simplest, and lowest-cost solution.

There are two different specifications for dropout voltage with the TPS74901. The first specification (see 図 7-1) is referred to as *V_{IN} dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 3.25V above V_{OUT}, which is the case for V_{BIAS} when powered by a 5V rail with 5% tolerance and with V_{OUT} = 1.5V (*3.25V* is a test condition of this device and can be adjusted by referring to 図 5-11). If V_{BIAS} is higher than V_{OUT} + 3.25V, V_{IN} dropout is less than specified.

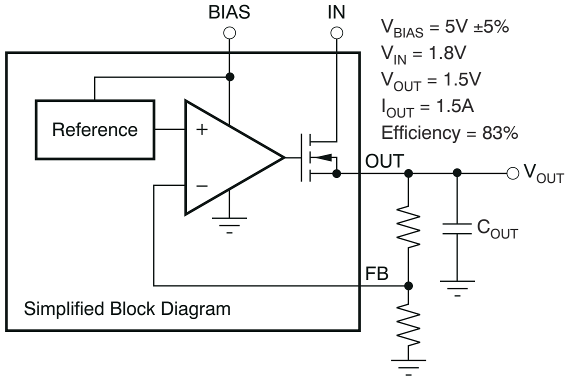


図 7-1. Typical Application of the TPS74901 Using an Auxiliary Bias Rail

The second specification (shown in 図 7-2) is referred to as V_{BIAS} *dropout* and is applied to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor; therefore, V_{BIAS} must be 1.75V above V_{OUT}. Because of this usage, IN and BIAS tied together easily consume a huge amount of power. Pay attention not to exceed the power rating of the device package.

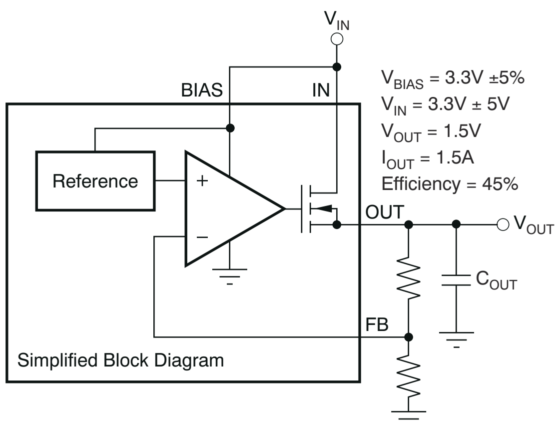


図 7-2. Typical Application of the TPS74901 Without an Auxiliary Bias

7.1.4 Output Noise

The TPS74901 provides low-output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001μF soft-start capacitor, the output noise is reduced by half and is typically $30\mu V_{RMS}$ for a 1.2V output (10Hz to 100kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001μF soft-start capacitor is given in 式 1.

$$V_N(\mu V_{RMS}) = 25 \left(\frac{\mu V_{RMS}}{V}\right) \text{ x } V_{OUT}(V) \tag{1}$$

The low-output noise of the TPS74901 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

7.1.5 Programmable Soft-Start

The TPS74901 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because power-up initialization problems are eliminated when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74901 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time is dependent on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using 式 2.

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (2)$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor can set the start-up time. In this case, the start-up time is given by 式 3:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \quad (3)$$

where:

- $V_{OUT(NOM)}$ is the nominal set output voltage
- C_{OUT} is the output capacitance
- $I_{CL(MIN)}$ is the minimum current limit for the device

In applications where monotonic start-up is required, the soft-start time given by 式 2 must be set to be greater than 式 3.

The maximum recommended soft-start capacitor is 0.015µF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit can possibly be unable to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 0.015µF can be a problem in applications where the enable pin must be rapidly pulsed while still requiring the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See 表 7-1 for suggested soft-start capacitor values.

表 7-1. Standard Capacitor Values for Programming the Soft-Start Time

C_{SS} (1)	SOFT-START TIME (Legacy Chip)	SOFT-START TIME (New Chip)
Open	0.1ms	0.25ms
270pF	0.5ms	0.4ms
560pF	1ms	0.8ms
2.7nF	5ms	4.1ms
5.6nF	10ms	8.5ms
0.01µF	18ms	15ms

(1) $t_{SS}(s) = 0.8 \times C_{SS}(F) / I_{SS}$, where $t_{SS}(s)$ = soft-start time in seconds.

Another option for setting the start-up rate is to use a feedforward capacitor. See the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note for more information.

7.1.6 Sequencing Requirements

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications as long as V_{IN} is greater than 1.1V, and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until the set output voltage is reached. If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}. If the soft-start time has not expired, the output tracks V_{IN} until V_{OUT} reaches the value set by the charging soft-start capacitor. 図 7-3 shows the use of an RC delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive EN from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

注

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50μA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10kΩ.

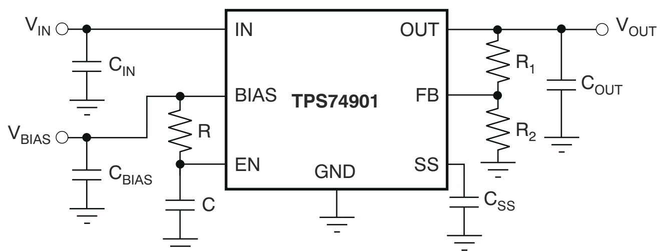
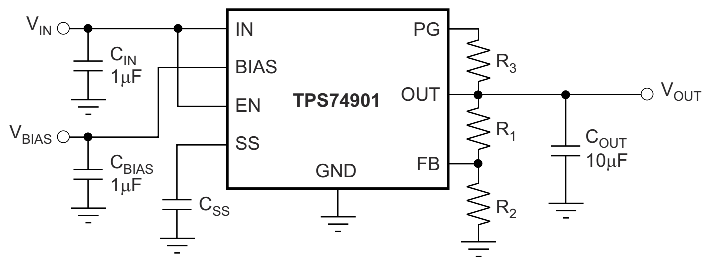


図 7-3. Soft-Start Delay Using an RC Circuit on Enable

7.2 Typical Application

図 7-4 shows the typical application circuit for the TPS74901 adjustable output device.

R_1 and R_2 can be calculated for any output voltage using the formula shown in 図 7-4. 表 7-2 lists sample resistor values of common output voltages. To achieve the maximum accuracy specifications, R_2 must be ≤ 4.99kΩ.



$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

図 7-4. Typical Application Circuit for the TPS74901 (Adjustable)

表 7-2. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R_1 / R_2)$.

7.2.1 Design Requirements

The goal of this design is to create a 1.2V rail at 3A with minimal external components from a 1.5V rail.

7.2.2 Detailed Design Procedure

First choose the bias, which must be at least 1.75V above the output voltage. A 3.3V rail is used to achieve this minimum voltage. For a minimal external component count and size, select the minimum capacitor sizes. C_{IN} = 1µF, C_{BIAS} = 1µF, and a C_{OUT} = 10µF. The C_{OUT} value was chosen to improve transient response. Using 表 7-2, R_1 is set to 2.49kΩ and R_2 is set to 4.99kΩ to create a 1.2V rail. The pullup resistor for PG is set to 10kΩ.

7.2.3 Application Curves

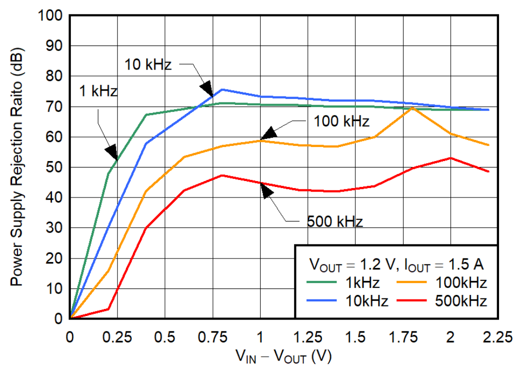


図 7-5. V_{IN} PSRR vs (V_{IN} – V_{OUT})

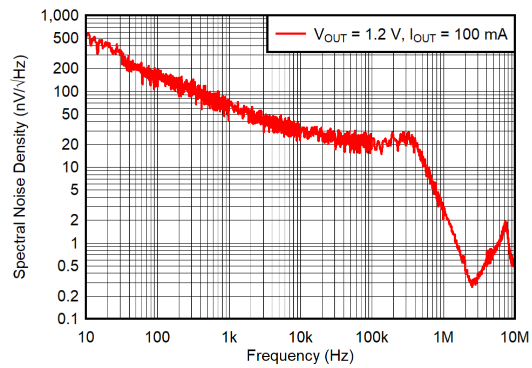


図 7-6. Noise Spectral Density

7.3 Power Supply Recommendations

The TPS74901 is designed to operate from an input voltage from 1.1V to 5.5V, provided the bias rail is at least 1.75V higher than the input supply. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally.

Connect a low-output impedance power supply directly to the IN pin of the TPS74901. This supply must have at least 1µF of capacitance near the IN pin for stability. A supply with similar requirements must also be connected directly to the bias rail with a separate 1µF or larger capacitor.

If the IN pin is tied to the bias pin, a minimum 4.7µF of capacitance is needed for stability.

To increase the overall PSRR of the solution at higher frequencies, use a PI-filter or ferrite bead before the input capacitor.

7.4 Layout

7.4.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, connect the capacitance on IN and BIAS as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, connect the top side of R_1 in 図 7-4 as close as possible to the load. If BIAS is connected to IN, connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turn-on response.

7.4.1.1 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions, and can be calculated using 式 4:

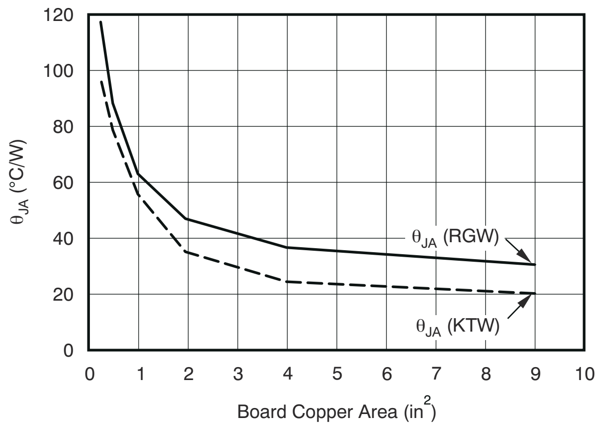
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VQFN (RGW) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can be connected to ground or left floating; however, the pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the DDPAK (KTW) package, the primary conduction path for heat is through the tab to the PCB. Connect that tab to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be estimated using 式 5:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \quad (5)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heat sinking can be estimated using 図 7-7.



$R_{\theta JA}$ value at board size of 9 in^2 (that is, 3 inches × 3 inches) is a JEDEC standard.

図 7-7. $R_{\theta JA}$ versus Board Size

図 7-7 shows the variation of $R_{\theta JA}$ as a function of ground plane copper area in the board. 図 7-7 is intended only as a guideline to demonstrate the affects of heat spreading in the ground plane; do not use 図 7-7 to estimate actual thermal performance in real application environments.

注

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the *Thermal Considerations* section.

7.4.1.2 Thermal Considerations

A better method of estimating the thermal measure comes from using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in 式 6. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with the corresponding formulas given in 式 6.

$$\Psi_{JT}: \; T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \; T_J = T_B + \Psi_{JB} \bullet P_D \quad (6)$$

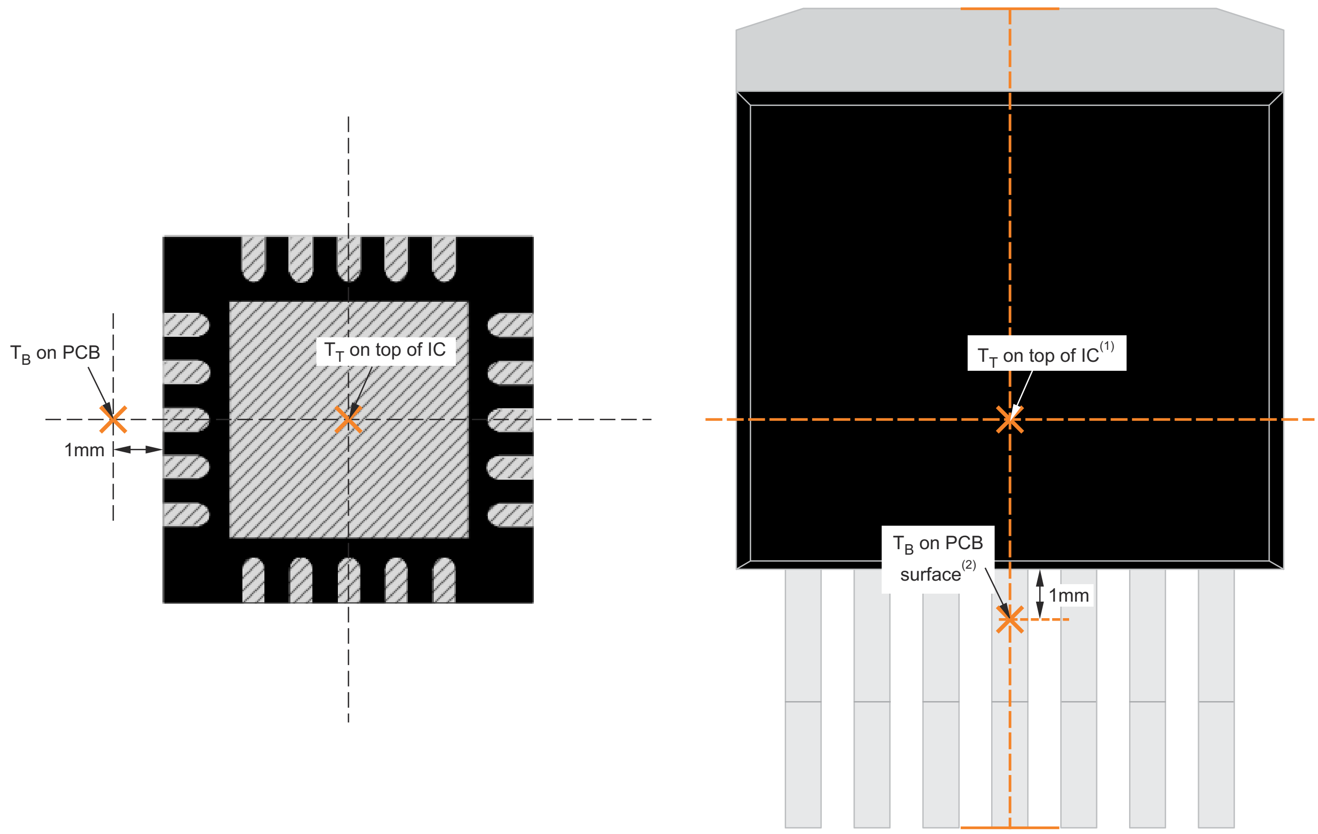
where:

- P_D is the power dissipation shown by 式 4
- T_T is the temperature at the center-top of the device package
- T_B is the PCB temperature measured 1mm away from the device package *on the PCB surface* (see 図 7-8)

注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.



(a) Example RGW (VQFN) Package Measurement

(b) Example KTW (DDPAK) Package Measurement

A. T_T is measured at the center of both the X- and Y-dimensional axes.

B. T_B is measured below the package lead on the PCB surface.

図 7-8. Measuring Points for T_T and T_B

Compared with $R_{\theta JA}$, the thermal metrics Ψ_{JT} and Ψ_{JB} are less independent of board size but do have a small dependency on board size and layout. 図 7-9 shows characteristic performance of Ψ_{JT} and Ψ_{JB} versus board size.

Referring to 図 7-9, the RGW package thermal performance has negligible dependency on board size. The KTW package, however, does have a measurable dependency on board size. This dependency exists because the package shape is not point symmetric to the center of a device. In the KTW package, for example (see 図 7-8), silicon is not beneath the measuring point of T_T that is the center of the X and Y dimension, so that Ψ_{JT} has a dependency. Also, because of that non-point symmetry, device heat distribution on the PCB is not point symmetric either, so that Ψ_{JB} has a greater dependency on board size and layout.

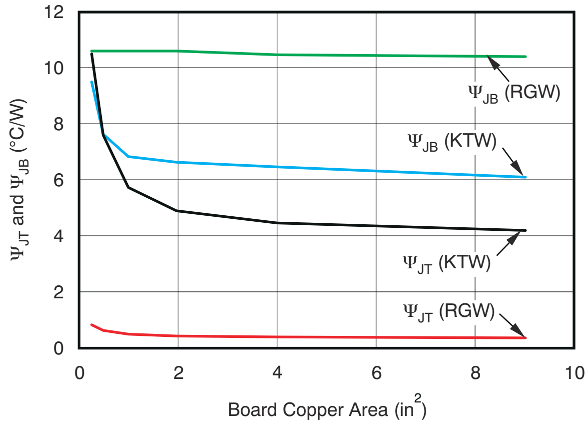


図 7-9. Ψ_{JT} and Ψ_{JB} versus Board Size

For a more detailed discussion of why TI does not recommend using $R_{\theta JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note, available for download at www.ti.com. Also, see the *IC Package Thermal Metrics* application note (also available on the TI website) for further information.

7.4.2 Layout Example

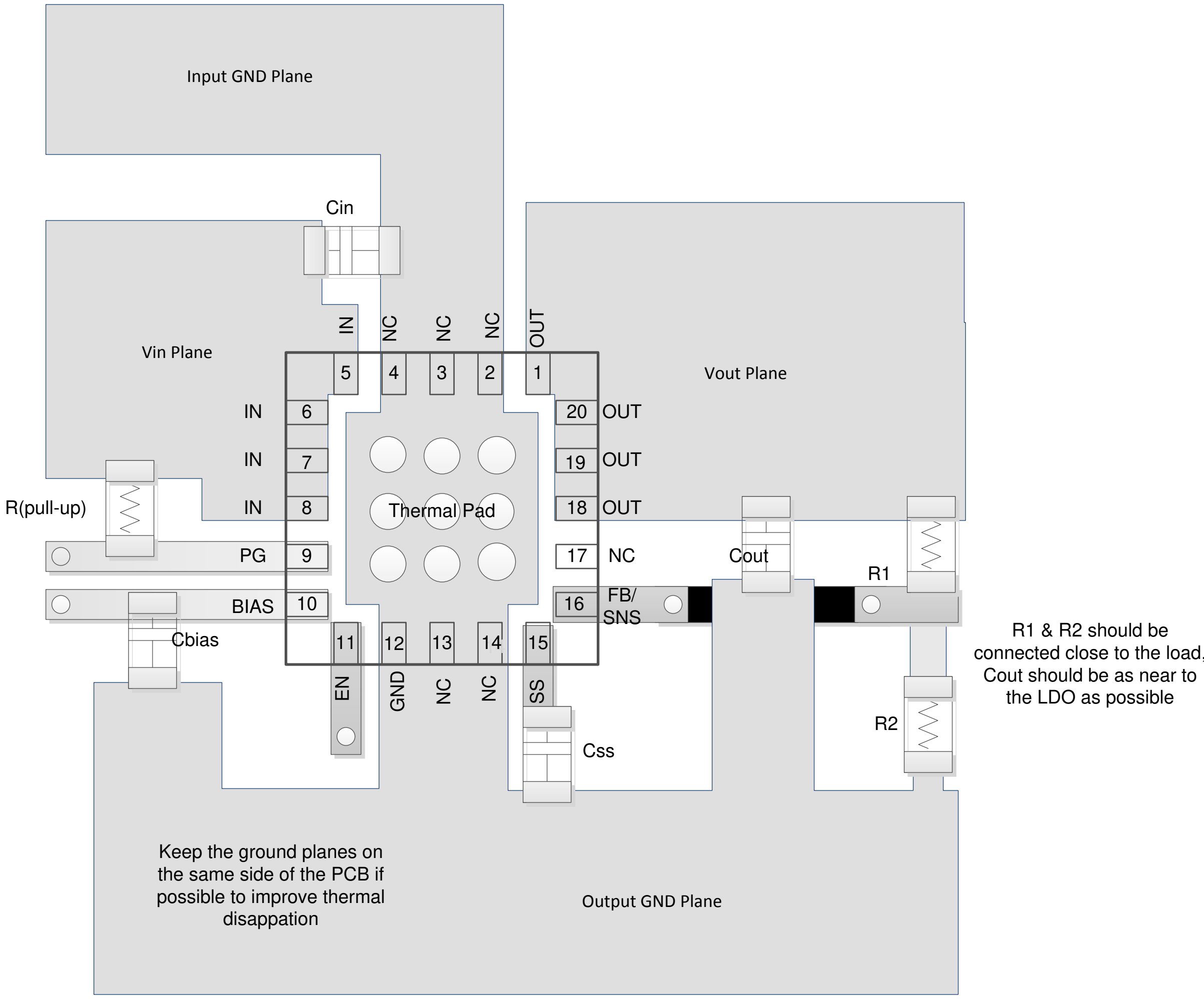


図 7-10. Layout Schematic (RGW Package)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT(1)	V_{OUT}
TPS74901**yyyzM3**	**yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is used. The device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.1.2 Development Support

8.1.2.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS74901. The TPS74901EVM-210 evaluation module and related user's guide (SLVU190) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

8.1.2.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS74901 is available through the product folders under *Tools & Software*.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using New Thermal Metrics* applicatin note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Ultimate Regulation with Fixed Output Version of TPS742xx/TPS743xx/TPS744xx* application note
- Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note
- Texas Instruments, *TPS74901EVM-210* user's guide

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision J (April 2023) to Revision K (June 2024) **Page**

- M3 への参照を新しいチップに変更「概要」セクションに「*入力、負荷、温度に関する精度: 1% (新チップ)*」を追加 .. 1
- Added (Legacy Chip) to KTW package.. 3
- Changed *Typical Characteristics: I_{OUT} = 50mA* section and added new chip curves.................. 8
- Changed *Typical Characteristics: I_{OUT} = 1 A* section, added new chip curves side by side to legacy curves.. 14
- Changed *Legacy Chip Functional Block Diagram* to include pulldown resistor for legacy chip and added *New Chip Functional Block Diagram* 16
- Added active pulldown circuit discussion and equation to *Enable and Shutdown* section.................. 17
- Added *SOFT-START TIME (New Chip)* column and changed footnote in *Standard Capacitor Values for Programming the Soft-Start Time* table.. 22
- Added feed-forward capacitor discussion to *Programmable Soft-Start* section.................. 22
- Changed *Application Curves* section to only show new chip curves.................. 25
- Changed last sentence of *Layout Recommendations and Power Dissipation* section; added 図 7-7 25
- Deleted (previously numbered) Figure 35 through Figure 39.................. 26
- Added *Device Nomenclature* section.................. 30

Changes from Revision I (May 2016) to Revision J (April 2023) **Page**

- *ドキュメント全体にわたって表、図、相互参照の採番方法を更新* 1
- ドキュメントに M3 サフィックス デバイスを追加.................. 1
- 「アプリケーション」セクションにリンクを追加 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS74901DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11S
TPS74901DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11S
TPS74901DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11S
TPS74901DRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11S
TPS74901DRCRM3	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11S
TPS74901DRCRM3.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11S
TPS74901DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11S
TPS74901DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11S
TPS74901KTWR	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	TPS74901
TPS74901KTWR.A	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS74901
TPS74901RGWR	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901
TPS74901RGWR.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901
TPS74901RGWRM3	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901
TPS74901RGWRM3.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901
TPS74901RGWT	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901
TPS74901RGWT.A	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901
TPS74901RGWTG4	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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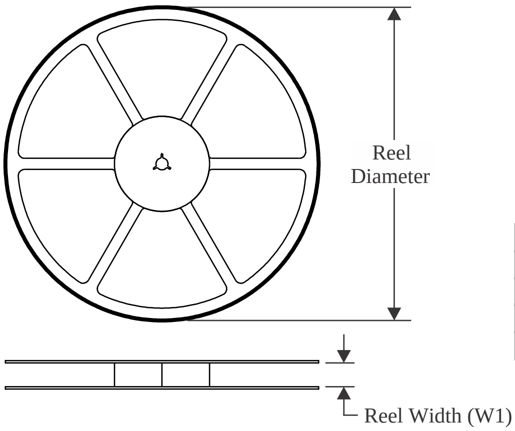
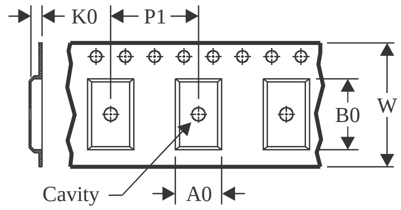
TAPE AND REEL INFORMATION

REEL DIMENSIONS

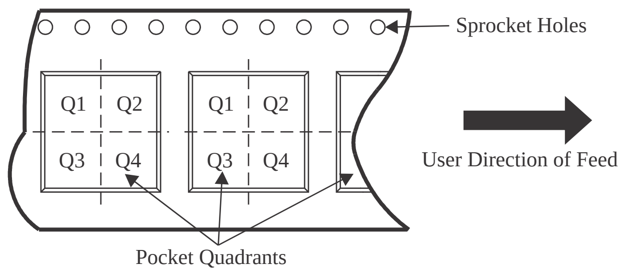


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

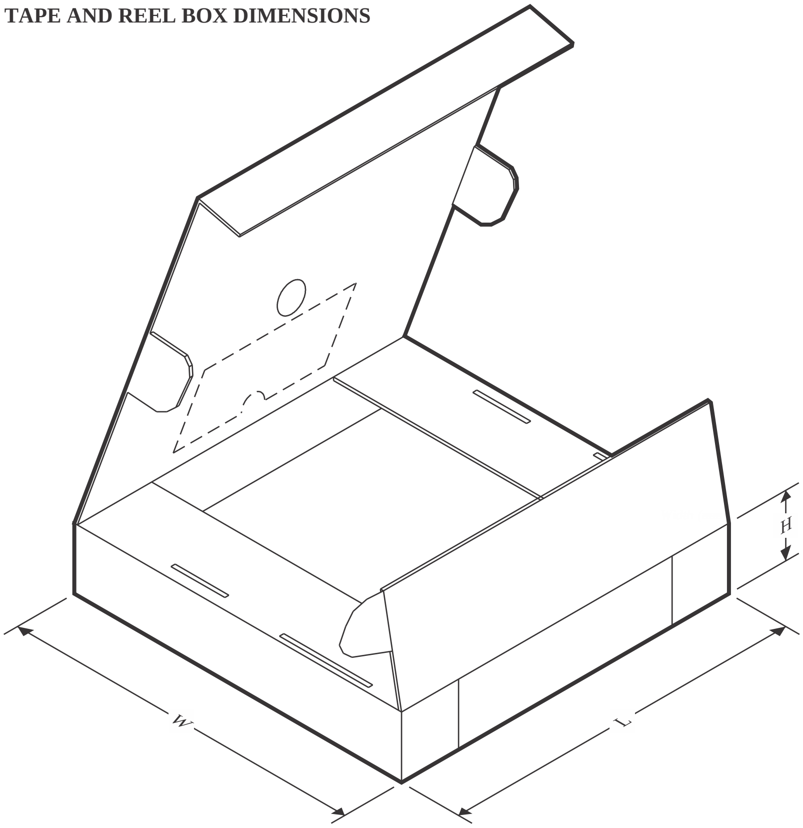
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74901DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74901DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74901DRCRM3	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74901DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74901RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74901RGWRM3	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74901RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

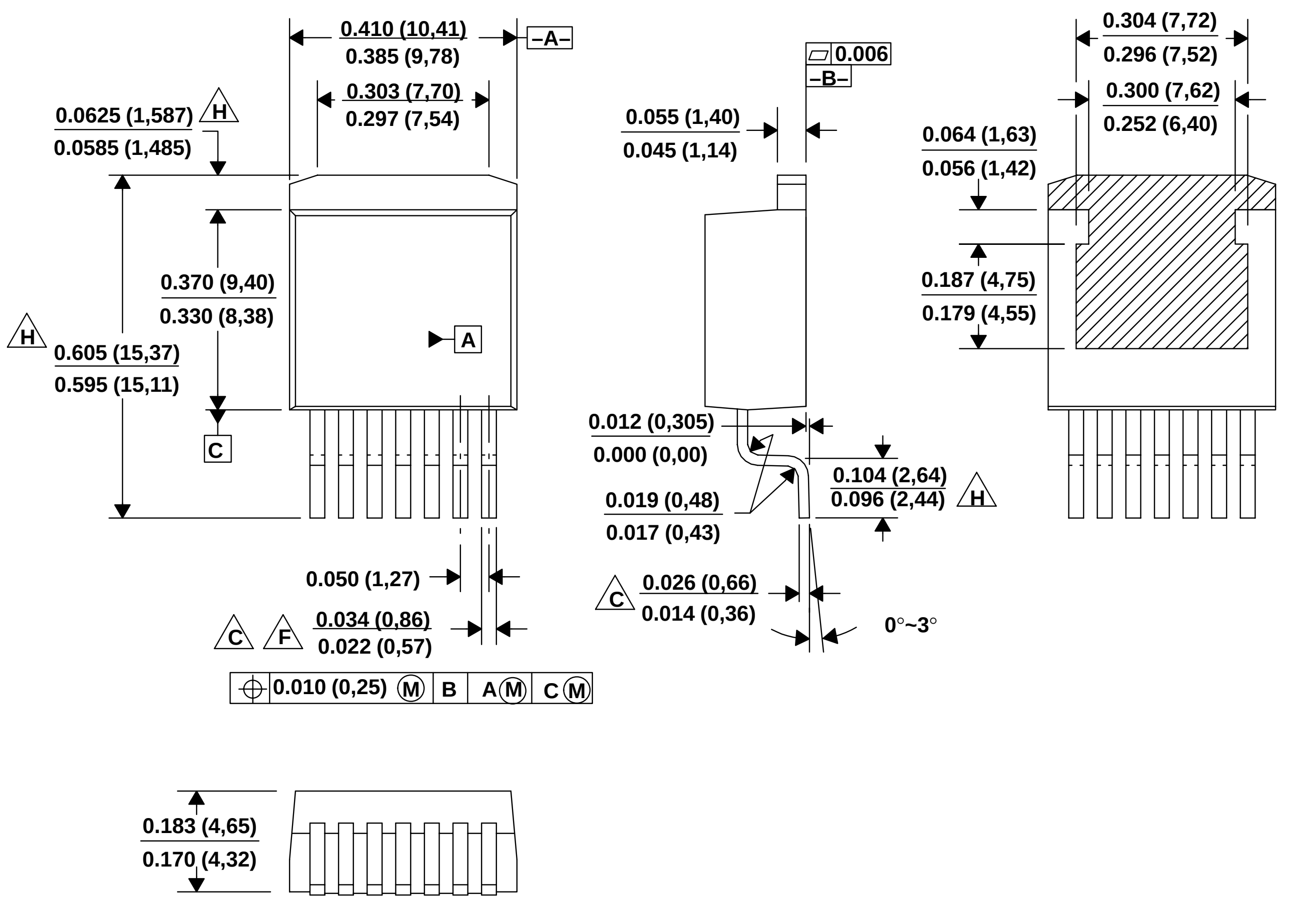
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

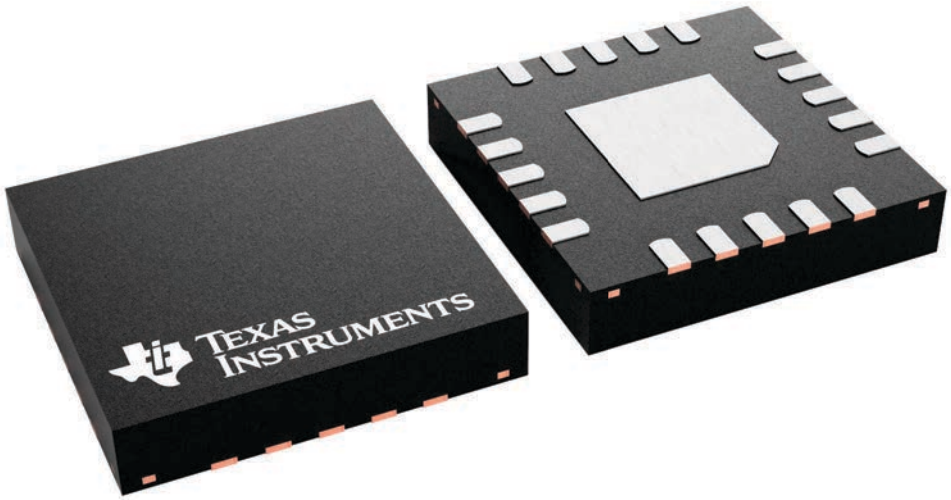
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74901DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74901DRCRG4	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74901DRCRM3	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74901DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS74901RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74901RGWRM3	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74901RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

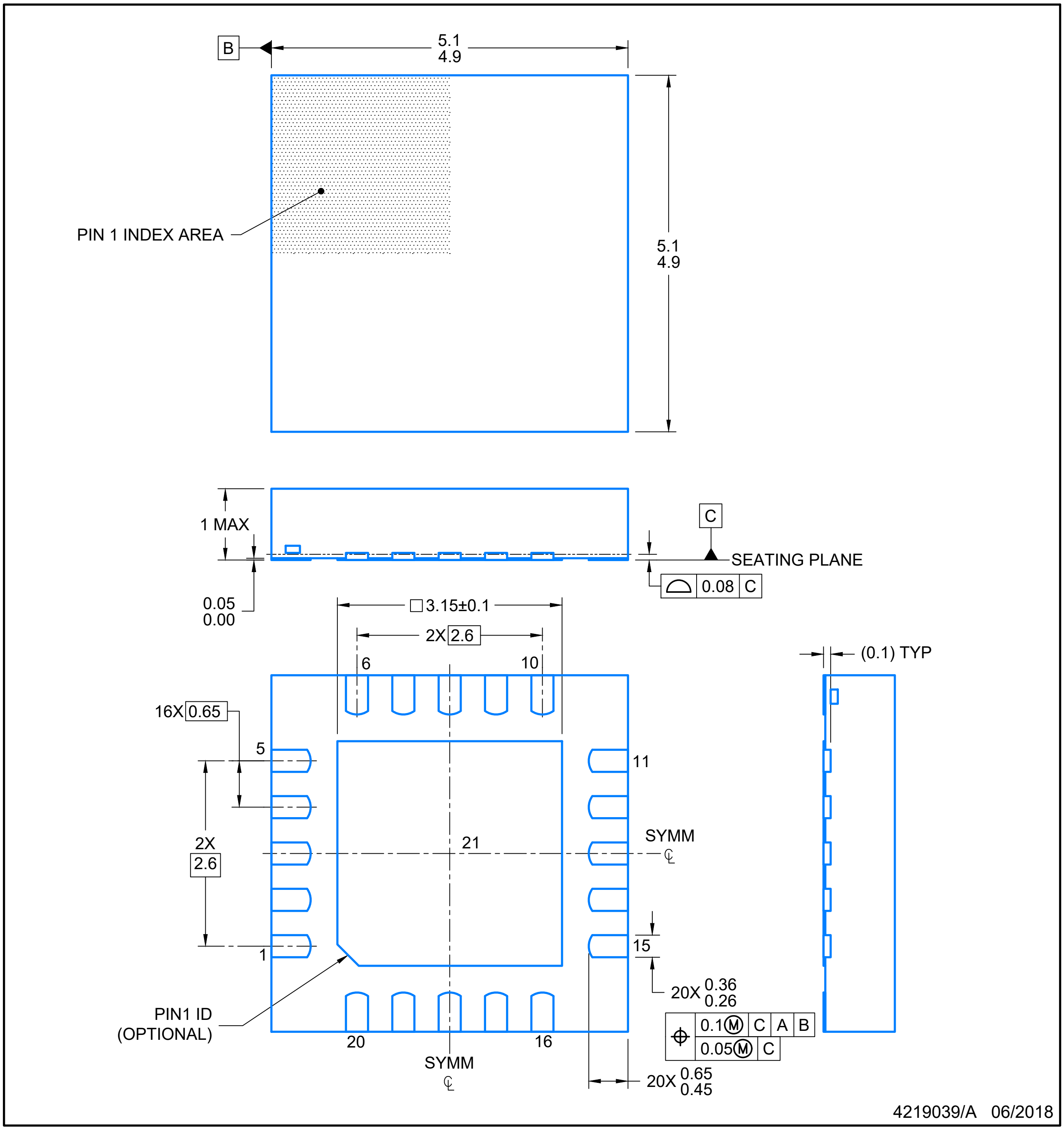
KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

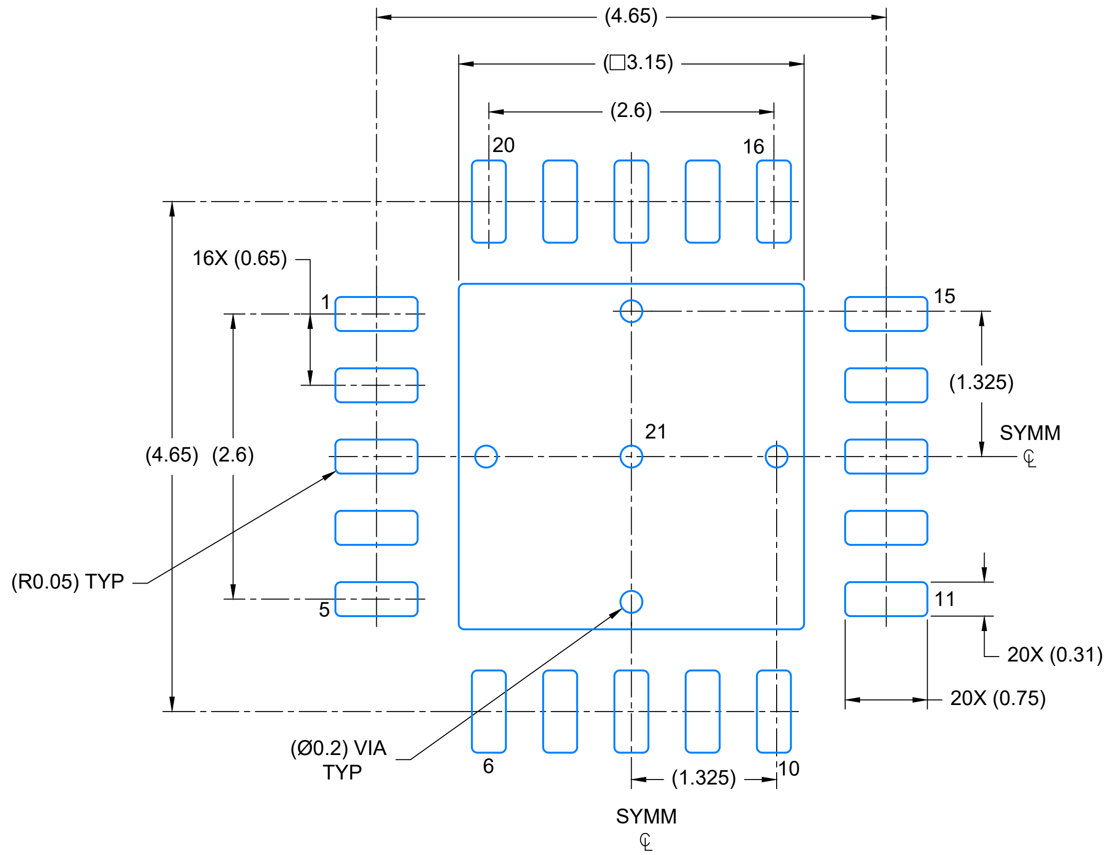
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



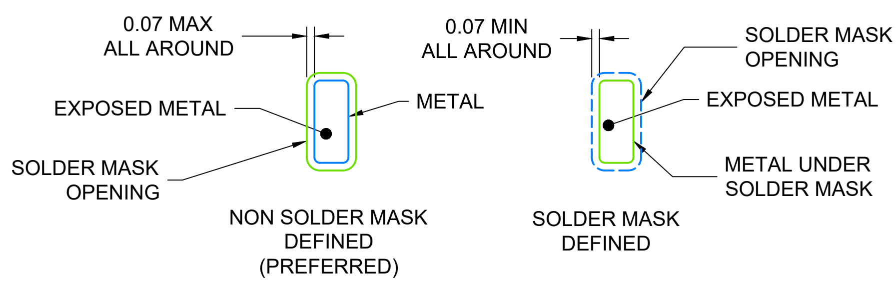


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X

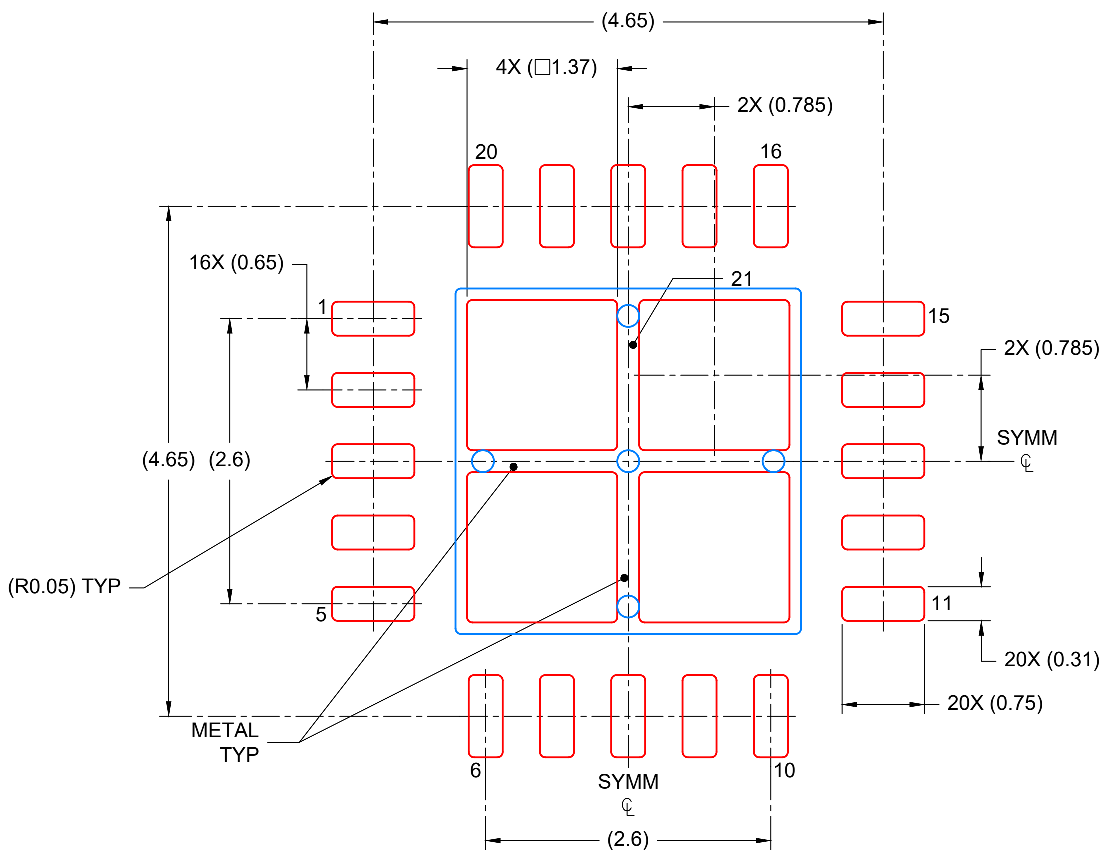


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

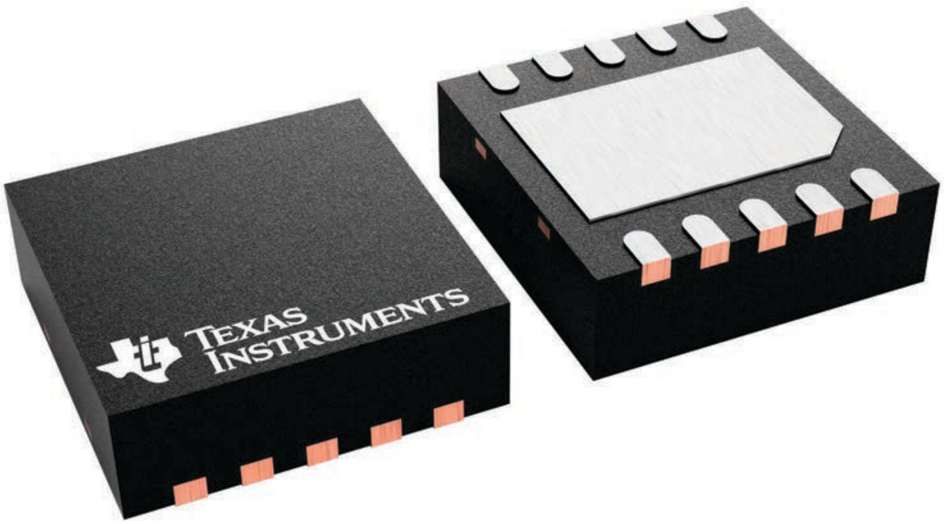
EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

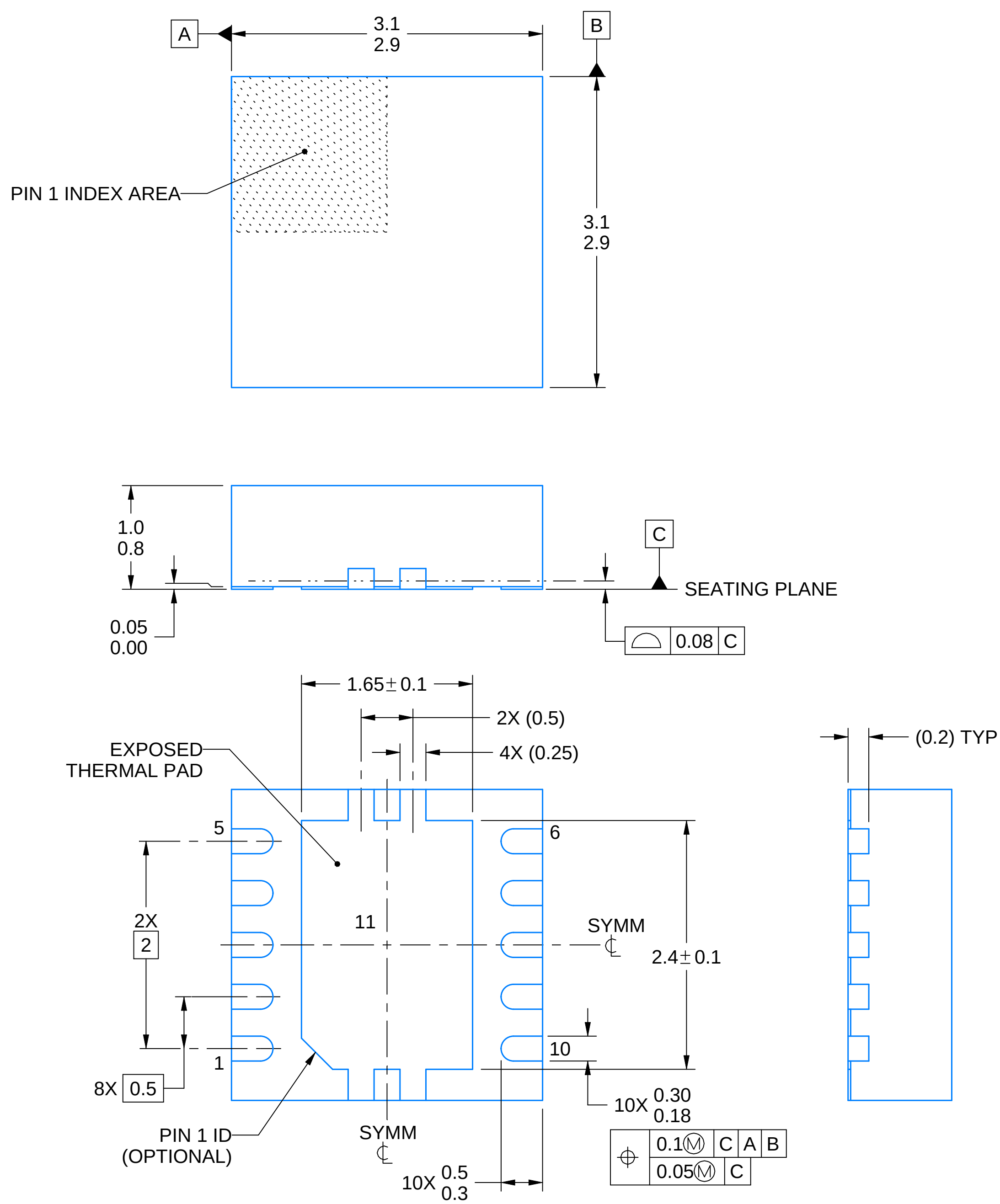
4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

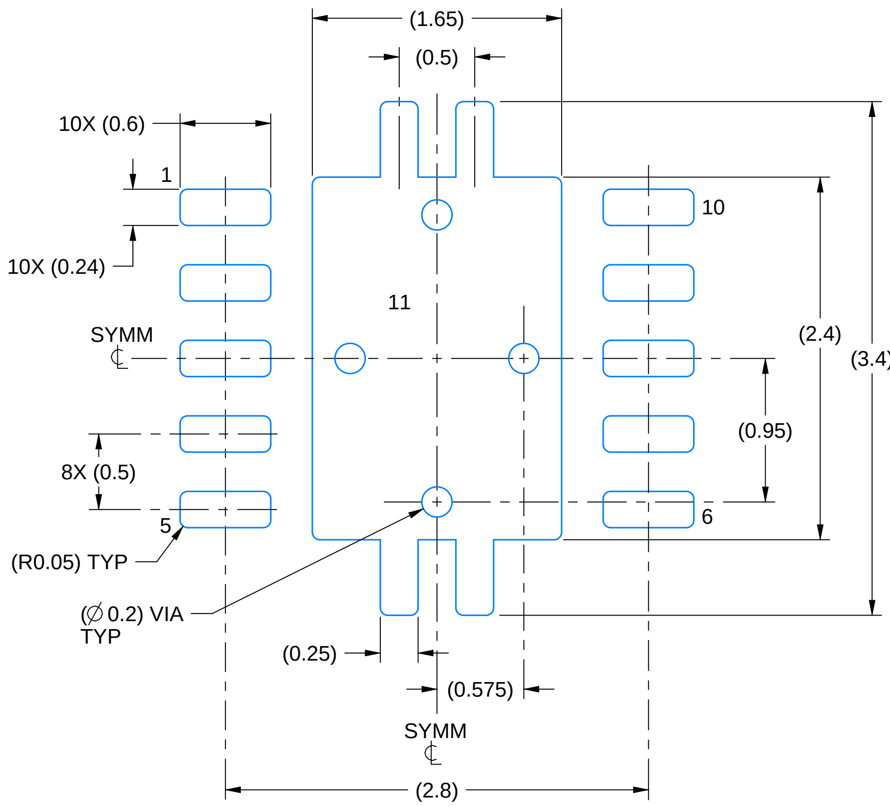
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



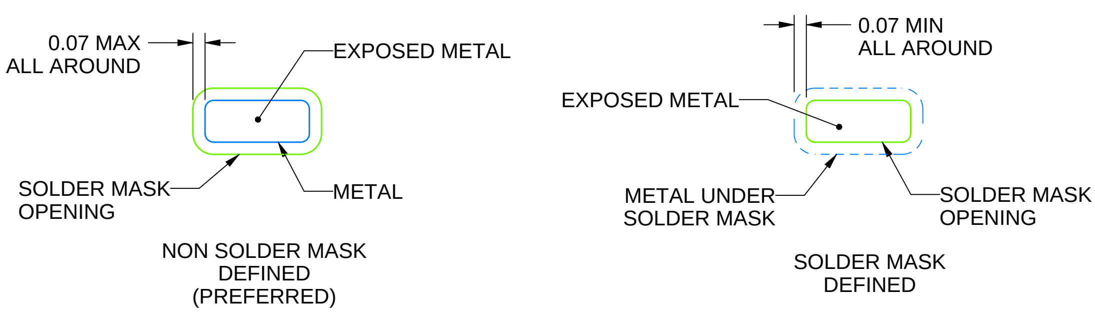


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

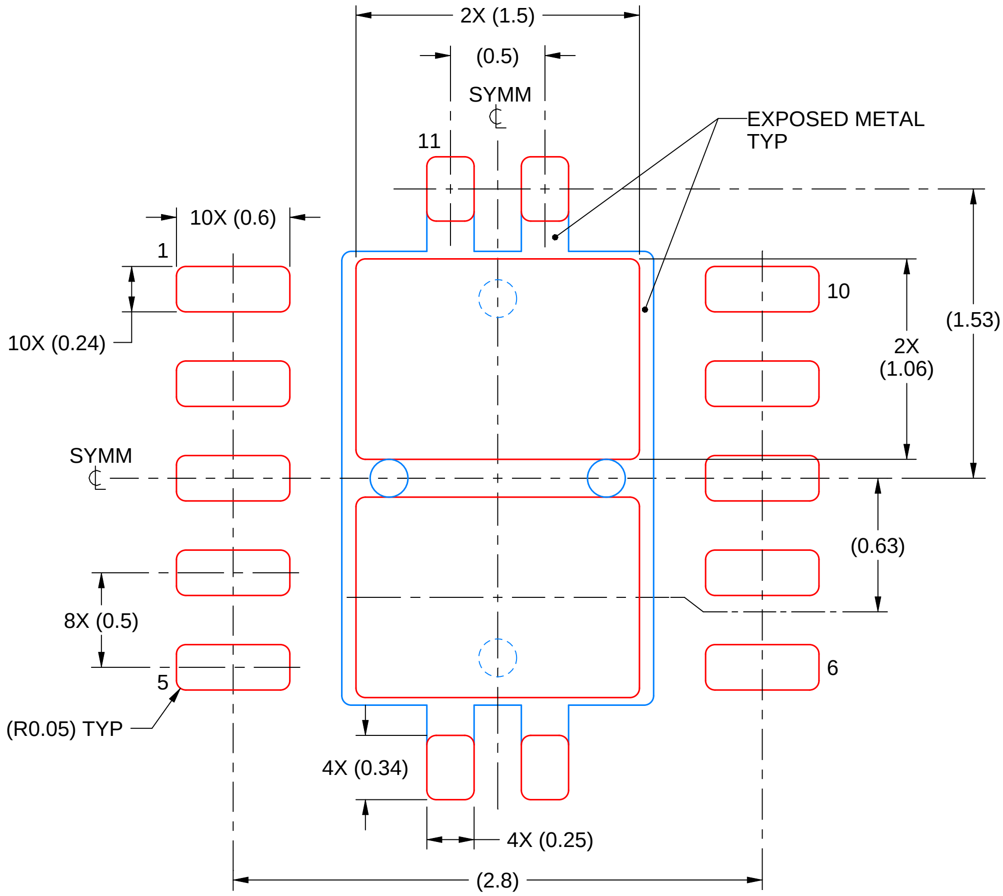


SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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