TPS720-Q1
350-mA, Ultra-Low V_{IN}, RF Low-Dropout Linear Regulator With BIAS Pin

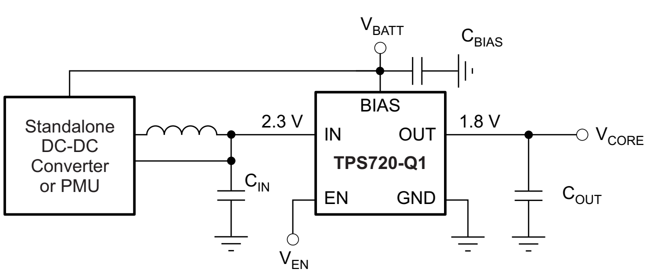
1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C6
- Input Voltage Range: 1.1 V to 4.5 V
- Output Voltage Range: 0.9 V to 3.6 V
- High-Performance LDO: 350 mA
- Low Quiescent Current: 38 µA
- Excellent Load Transient Response: ±15 mV for I_{LOAD} = 0 mA to 350 mA in 1 µs
- Low Noise: 48 μV_{RMS} (10 Hz to 100 kHz)
- 80-dB V_{IN} PSRR (10 Hz to 10 kHz)
- 70-dB V_{BIAS} PSRR (10 Hz to 10 kHz)
- Fast Start-Up Time: 140 µs
- Built-In Soft-Start With Monotonic V_{OUT} Rise and Start-Up Current Limited to 100 mA + I_{LOAD}
- Overcurrent and Thermal Protection
- Low Dropout: 110 mV at I_{LOAD} = 350 mA
- Stable With a 2.2-µF Output Capacitor
- Package: 2.00 mm × 2.00 mm, 6-Pin WSON

2 Applications

- Camera Modules
- FPD Link Power
- Automotive Infotainment
- USB HUB Power

Simplified Schematic



3 Description

The TPS720-Q1 family of dual-rail, low-dropout linear regulators (LDOs) offers outstanding ac performance (PSRR, load and line transient response) and consume a very low quiescent current of 38 µA.

The V_{BIAS} rail that powers the control circuit of the LDO draws very low current (on the order of the LDO quiescent current) and can be connected to any power supply that is equal to or greater than 1.4 V above the output voltage. The main power path is through V_{IN} and can be a lower voltage than V_{BIAS}; this path can be as low as V_{OUT} + V_{DO}, increasing the efficiency of the solution in many power-sensitive applications. For example, V_{IN} can be an output of a high-efficiency, dc-dc, step-down regulator.

The TPS720-Q1 supports a novel feature where the output of the LDO regulates under light loads when the IN pin is left floating. The light-load drive current is sourced from V_{BIAS} under this condition. This feature is particularly useful in power-saving applications where the dc-dc converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load.

The TPS720-Q1 is stable with ceramic capacitors and uses an advanced BICMOS fabrication process that yields a dropout of 110 mV at a 350-mA output load. The TPS720-Q1 provides a monotonic V_{OUT} rise (overshoot limited to 3%) with V_{IN} inrush current limited to 100 mA + I_{LOAD} with an output capacitor of 2.2 µF.

The TPS720-Q1 uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over load, line, process, and temperature extremes. The TPS720-Q1 is available in a 6-pin WSON package. This family of devices is fully specified over the temperature range of T_J = –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS720-Q1	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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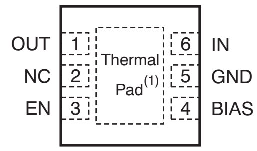
4 Revision History

Changes from Original (February 2016) to Revision A **Page**

- Changed Output Voltage Range bullet in *Features* section from "0.9 V to 3.0 V" to "0.9 V to 3.6 V" 1
- Changed maximum value of "output voltage" parameter from 3.0 V to 3.6 V in *Recommended Operating Conditions* table 4
- Reformatted *Thermal Information* table note 4
- Changed maximum value of *output voltage* parameter from 3.0 V to 3.6 V in *Electrical Characteristics* table 5
- Changed output voltage range in table note from "0.9 V to 3.0 V" to "0.9 V to 3.3 V" in *Device Nomenclature* section..... 18
- Changed formatting of *Related Documentation* section 18
- Added *Receiving Notification of Documentation Updates* section 18

5 Pin Configuration and Functions

DRV Package
6-Pin WSON With Exposed Thermal Pad
Top View



(1) TI recommends connecting the WSON (DRV) package thermal pad to ground.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output pin. A 2.2-µF ceramic capacitor is connected from this pin to ground for stability and to provide load transients; see *Input and Output Capacitor Requirements*
NC	2	—	No connection.
EN	3	I	Enable pin. A logic high signal on this pin turns the device on and regulates the voltage from IN to OUT. A logic low on this pin turns the device off.
BIAS	4	I	Bias supply pin. For better transient performance, TI recommends bypassing this input with a ceramic capacitor to ground; see *Input and Output Capacitor Requirements*
GND	5	—	Ground pin.
IN	6	I	Input pin. This pin can be a maximum of 4.5 V; V_{IN} must not exceed V_{BIAS}. Bypass this input with a ceramic capacitor to ground; see *Input and Output Capacitor Requirements*.

6 Specifications

6.1 Absolute Maximum Ratings

at T_J = –40°C to +125°C (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
V_{IN} (2)	Input voltage (steady-state)	–0.3	V_{BIAS} or 5 (3)	V
V_{IN_PEAK} (4)	Peak transient input		5.5	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	5	V
I_{OUT}	Peak output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Total continuous power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–55	125	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To ensure proper device operation, V_{IN} must be less than or equal to V_{BIAS} under all conditions.
(3) Whichever is less.
(4) For durations no longer than 1 ms each, for a total of no more than 1000 occurrences over the lifetime of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	
		Machine model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage (steady-state)	1.1		V_{BIAS} or 4.5 (1)	V
V_{BIAS}	Bias voltage	2.6 or V_{OUT} + 1.4 (2)		5.5	V
V_{OUT}	Output voltage	0.9		3.6	V
I_{OUT}	Peak output current	0		350	mA
V_{EN}	Enable voltage	0		5.5	V
C_{IN}	Input capacitance		1		µF
C_{BIAS}	Bias capacitance		0.1		µF
C_{OUT} (3)	Output capacitance	2.2			µF

(1) Whichever is less.
(2) Whichever is greater.
(3) Maximum ESR must be less than 250 mΩ.

6.4 Thermal Information

THERMAL METRIC (1)		TPS720-Q1 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.4	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.6 V (whichever is greater), $V_{IN} \geq V_{OUT}$ + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, and C_{OUT} = 2.2 µF (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		1.1 (1)		V_{BIAS} or 4.5 (2)	V
V_{BIAS}	Bias voltage		2.6		5.5	V
V_{OUT} (3)	Output voltage (4)		0.9		3.6	V
	Output accuracy: Over V_{BIAS}, V_{IN}, I_{OUT}, T_J = –40°C to +125°C	V_{OUT} + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, V_{OUT} + 0.5 V ≤ V_{IN} ≤ 4.5 V, 0 mA ≤ I_{OUT} ≤ 350 mA	–2%		2%	
	Output accuracy: Over V_{BIAS}, V_{IN}, I_{OUT}, T_J = –40°C to +125°C	V_{OUT} + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, V_{OUT} + 0.5 V ≤ V_{IN} ≤ 4.5 V, 0 mA ≤ I_{OUT} ≤ 350 mA, V_{OUT} < 1.2 V	–25		25	mV
	Output accuracy: V_{IN} floating	V_{OUT} + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 0 µA ≤ I_{OUT} ≤ 500 µA		±1%		
$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} line regulation	V_{IN} = (V_{OUT} + 0.5 V) to 4.5 V, I_{OUT} = 1 mA		16		µV/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	V_{BIAS} line regulation	V_{BIAS} = (V_{OUT} + 1.4 V) or 2.6 V (whichever is greater) to 5.5 V, I_{OUT} = 1 mA		16		µV/V
	V_{IN} line transient	ΔV_{IN} = 400 mV, t_{RISE} = t_{FALL} = 1 µs		±200		µV
	V_{BIAS} line transient	ΔV_{BIAS} = 600 mV, t_{RISE} = t_{FALL} = 1 µs		±0.8		mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 350 mA (no load to full load)		–15		µV/mA
	Load transient	0 mA ≤ I_{OUT} ≤ 350 mA, t_{RISE} = t_{FALL} = 1 µs		±15		mV
V_{DO_IN}	V_{IN} dropout voltage (5)	V_{IN} = $V_{OUT(NOM)}$ – 0.1 V, (V_{BIAS} – $V_{OUT(NOM)}$) = 1.4 V, I_{OUT} = 350 mA		110	200	mV
V_{DO_BIAS}	V_{BIAS} dropout voltage (6)	V_{IN} = $V_{OUT(NOM)}$ + 0.3 V, I_{OUT} = 350 mA		1.09	1.4	V
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	420	600	800	mA
I_{GND}	Ground pin current	I_{OUT} = 100 µA		38		µA
		I_{OUT} = 0 mA to 350 mA		54	80	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4 V		0.5	2.5	µA
PSRR	V_{IN} power-supply rejection ratio	V_{IN} – V_{OUT} ≥ 0.5 V, V_{BIAS} = V_{OUT} + 1.4 V, I_{OUT} = 350 mA; f = 10 Hz		85		dB
		f = 100 Hz		85		dB
		f = 1 kHz		85		dB
		f = 10 kHz		80		dB
		f = 100 kHz		70		dB
		f = 1 MHz		50		dB
PSRR	V_{BIAS} power-supply rejection ratio	V_{IN} – V_{OUT} ≥ 0.5 V, V_{BIAS} = V_{OUT} + 1.4 V, I_{OUT} = 350 mA; f = 10 Hz		80		dB
		f = 100 Hz		80		dB
		f = 1 kHz		75		dB
		f = 10 kHz		65		dB
		f = 100 kHz		55		dB
		f = 1 MHz		35		dB
V_N	Output noise voltage	Bandwidth = 10 Hz to 100 kHz, V_{BIAS} ≥ 2.6 V, V_{IN} = V_{OUT} + 0.5 V		48		$µV_{RMS}$
I_{VIN_INRUSH}	Inrush current on V_{IN}	V_{BIAS} = (V_{OUT} +1.4 V) or 2.6 V (whichever is greater), V_{IN} = V_{OUT} + 0.5 V		100 + I_{LOAD}		mA
$V_{EN(HI)}$	Enable pin high (enabled)		1.1			V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V

(1) Performance specifications are ensured to a minimum V_{IN} = V_{OUT} + 0.5 V.
(2) Whichever is less.
(3) Minimum V_{BIAS} = (V_{OUT} + 1.4 V) or 2.6 V (whichever is greater) and V_{IN} = V_{OUT} + 0.5 V.
(4) V_O nominal value is factory programmable through the on-chip EEPROM.
(5) Measured for devices with $V_{OUT(NOM)}$ ≥ 1.2 V.
(6) V_{BIAS} – V_{OUT} with V_{OUT} = $V_{OUT(NOM)}$ – 0.1 V. Measured for devices with $V_{OUT(NOM)}$ ≥ 1.8 V.

Electrical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.6 V (whichever is greater), V_{IN} ≥ V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, and C_{OUT} = 2.2 µF (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EN}	Enable pin current	V_{EN} = 5.5 V, V_{IN} = 4.5 V, V_{BIAS} = 5.5 V			1	µA
UVLO	Undervoltage lockout	V_{BIAS} rising	2.35	2.45	2.59	V
	UVLO hysteresis	V_{BIAS} falling		150		mV
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		
T_J	Operating junction temperature		–40		125	°C

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
t_{STR}	Start-up time	V_{OUT} = 95%, $V_{OUT\ (NOM)}$, I_{OUT} = 350 mA, C_{OUT} = 2.2 µF		140		µs

6.7 Typical Characteristics

over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.6 V (whichever is greater), V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, and C_{OUT} = 2.2 μF (unless otherwise noted); typical values are at T_J = 25°C

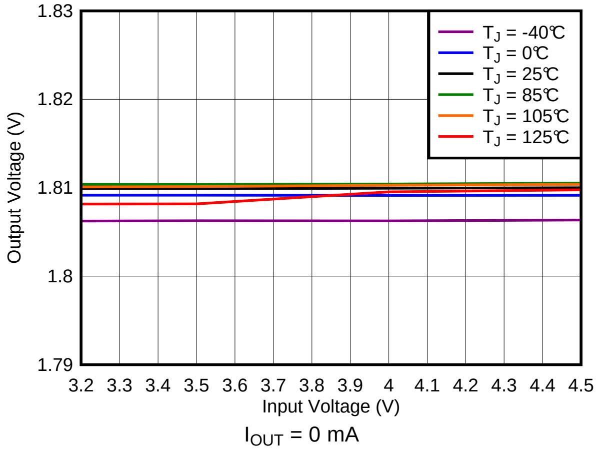


Figure 1. V_{IN} Line Regulation (No Load)

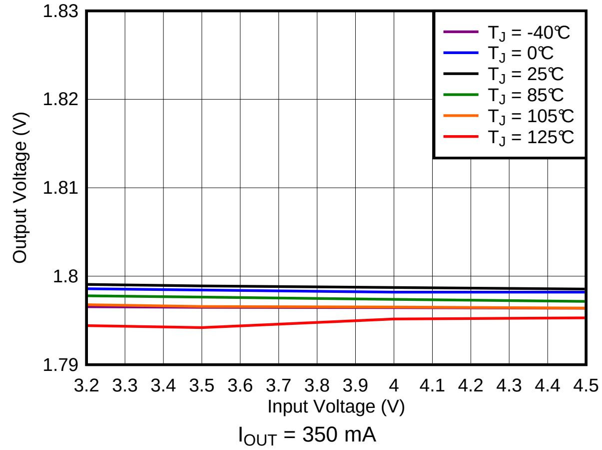


Figure 2. V_{IN} Line Regulation (350 mA)

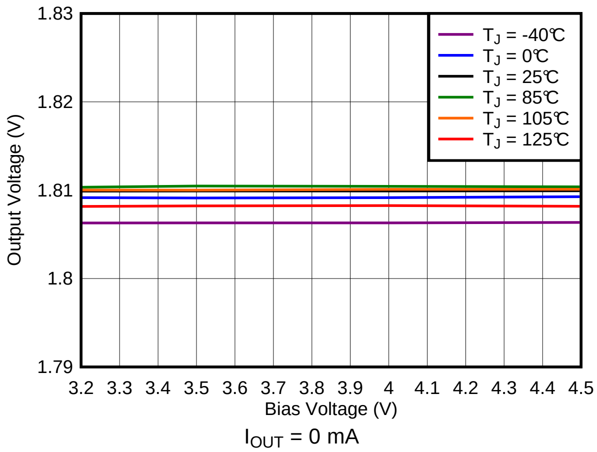


Figure 3. V_{BIAS} Line Regulation (No Load)

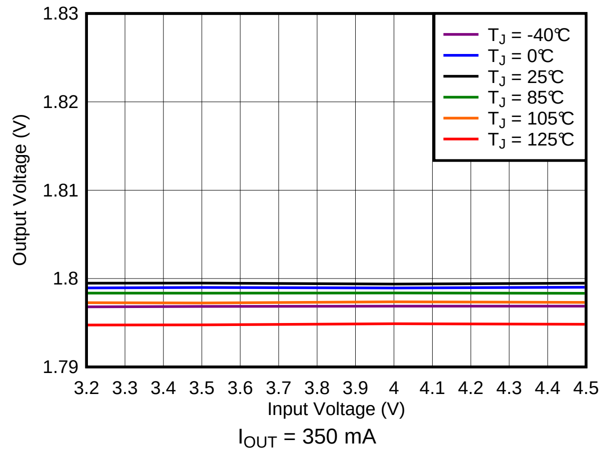


Figure 4. V_{BIAS} Line Regulation (350 mA)

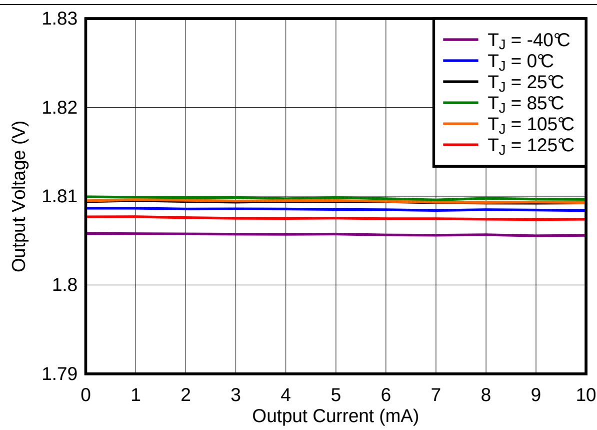


Figure 5. Load Regulation Under Light Loads

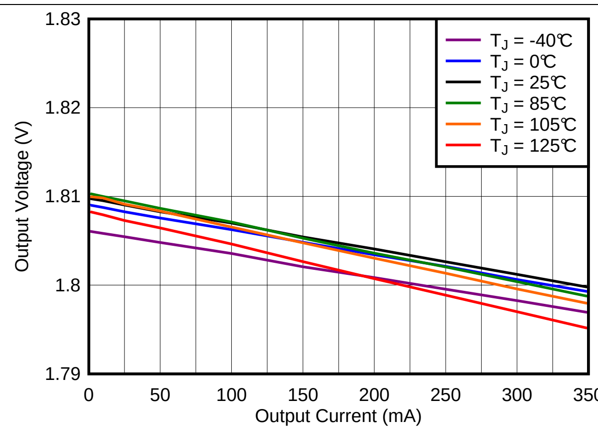


Figure 6. Load Regulation

Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.6 V (whichever is greater), V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, and C_{OUT} = 2.2 µF (unless otherwise noted); typical values are at T_J = 25°C

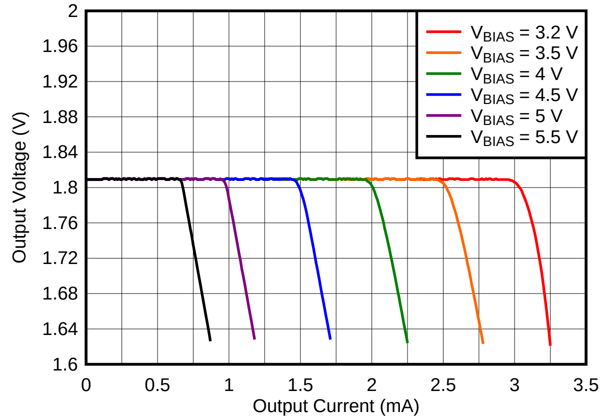
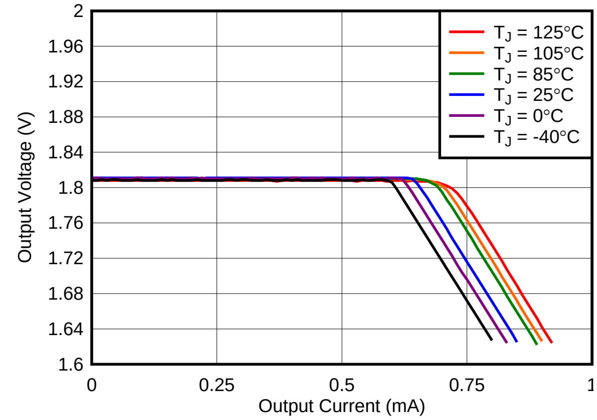


Figure 7. Load Regulation With V_{IN} Floating



V_{BIAS} = 3.2 V

Figure 8. Load Regulation With V_{IN} Floating

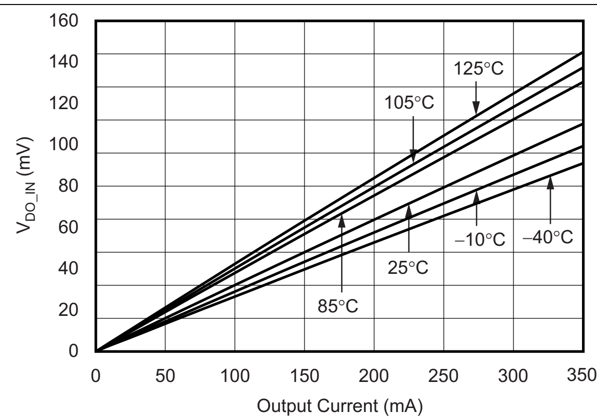
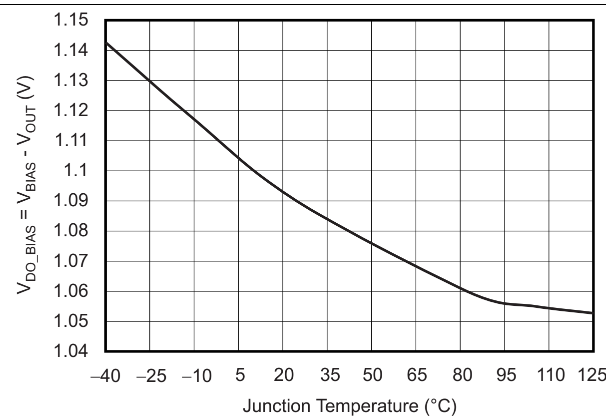


Figure 9. V_{IN} Dropout Voltage vs Output Current



V_{OUT} = $V_{OUT(NOM)}$ – 0.1 V I_{OUT} = 350 mA

Figure 10. V_{BIAS} Dropout Voltage vs Junction Temperature

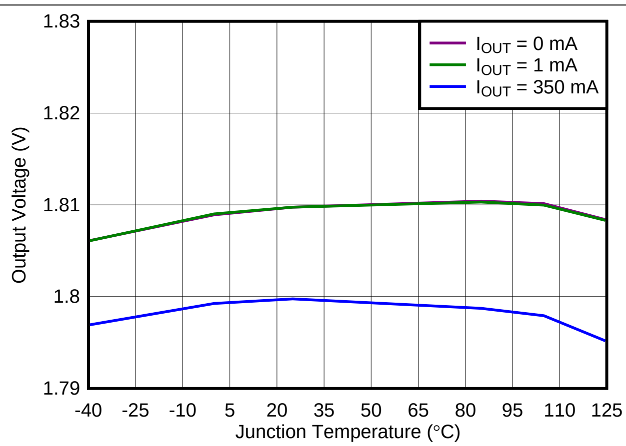
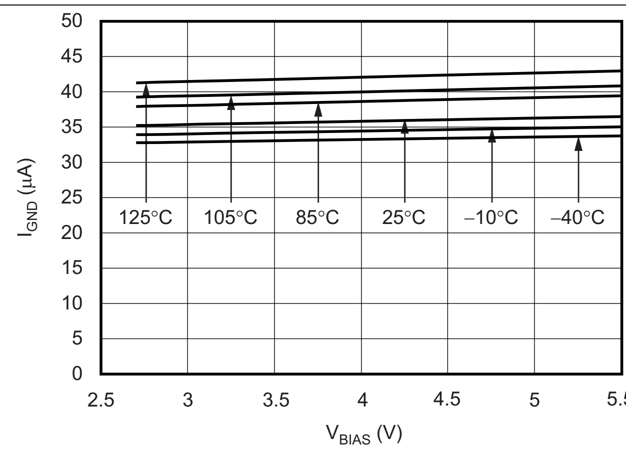


Figure 11. Output Voltage vs Junction Temperature



I_{OUT} = 1 mA

Figure 12. Ground Pin Current vs V_{BIAS} Voltage

Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.6 V (whichever is greater), V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, and C_{OUT} = 2.2 µF (unless otherwise noted); typical values are at T_J = 25°C

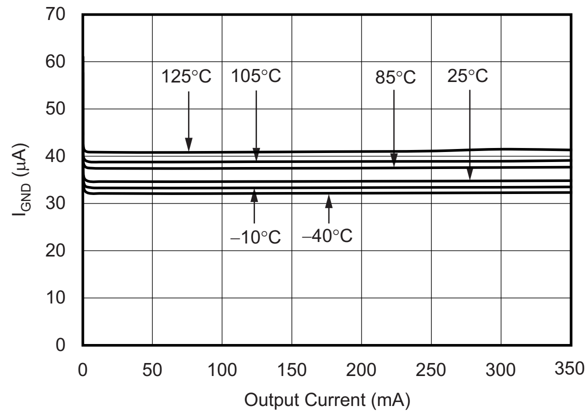


Figure 13. Ground Pin Current vs Output Current

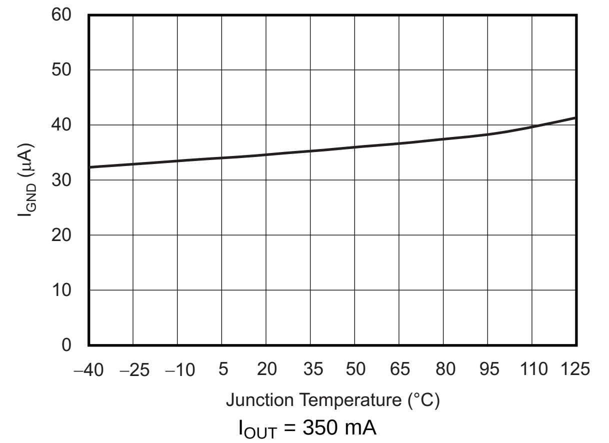


Figure 14. Ground Pin Current vs Junction Temperature

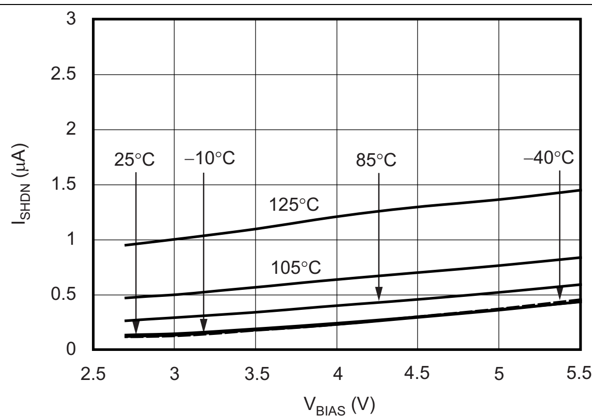


Figure 15. Shutdown Current vs V_{BIAS} Voltage

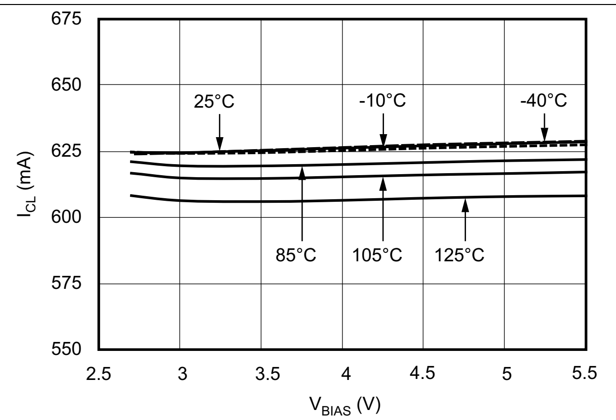


Figure 16. Current Limit vs V_{BIAS} Voltage

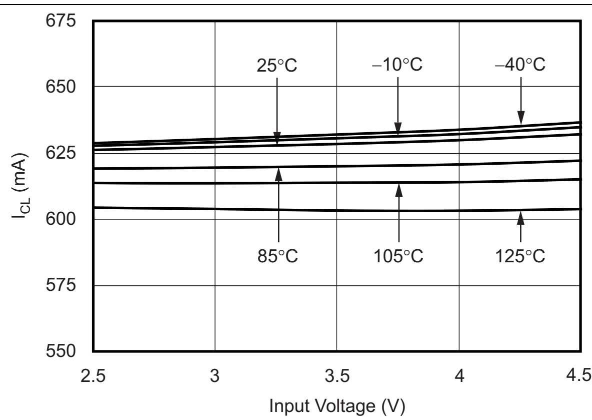


Figure 17. Current Limit vs Input Voltage

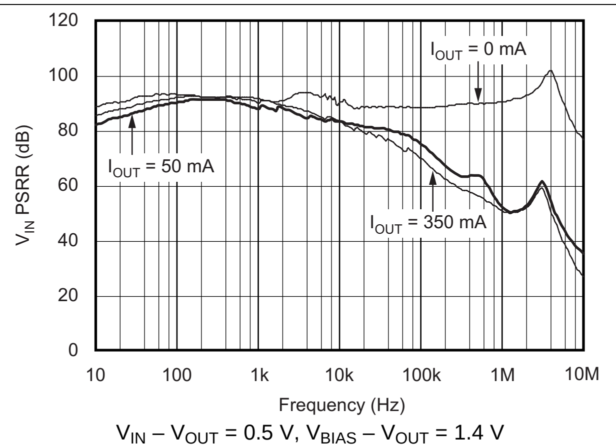
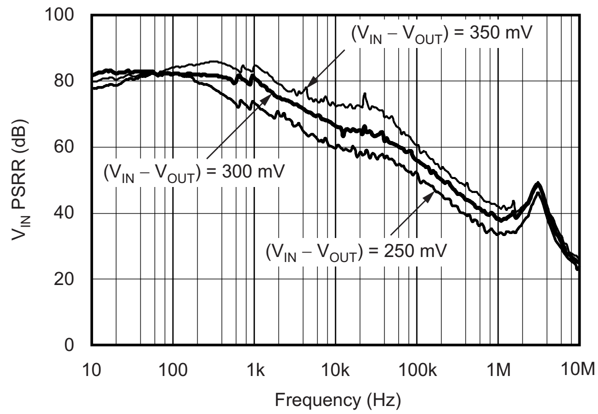


Figure 18. V_{IN} Power-Supply Rejection Ratio vs Frequency

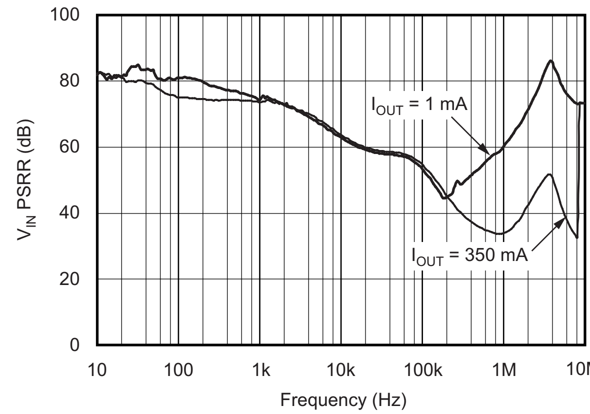
Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.6 V (whichever is greater), V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, and C_{OUT} = 2.2 μF (unless otherwise noted); typical values are at T_J = 25°C



I_{OUT} = 350 mA

Figure 19. V_{IN} Power-Supply Rejection Ratio vs Frequency



V_{IN} – V_{OUT} = 0.5 V V_{BIAS} – V_{OUT} = 1.4 V

Figure 20. V_{BIAS} Power-Supply Rejection Ratio vs Frequency

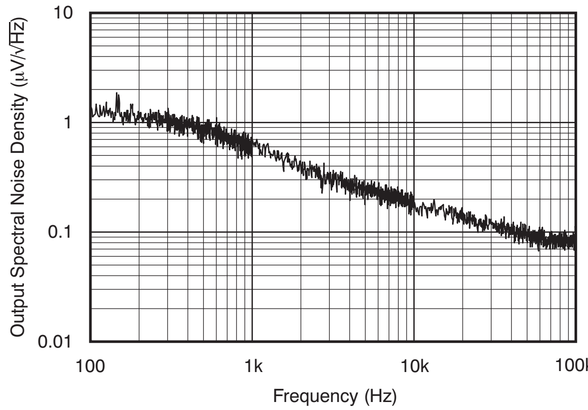
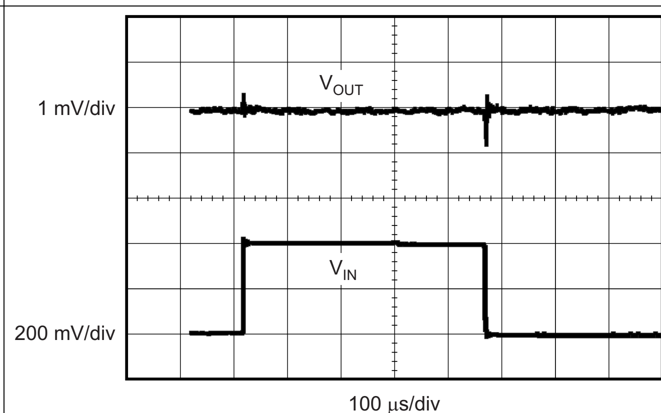
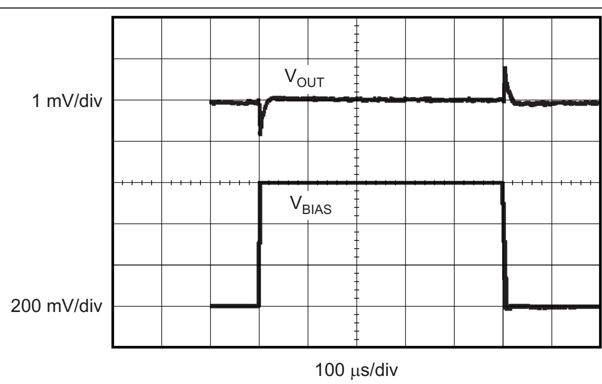


Figure 21. Output Spectral Noise Density vs Frequency



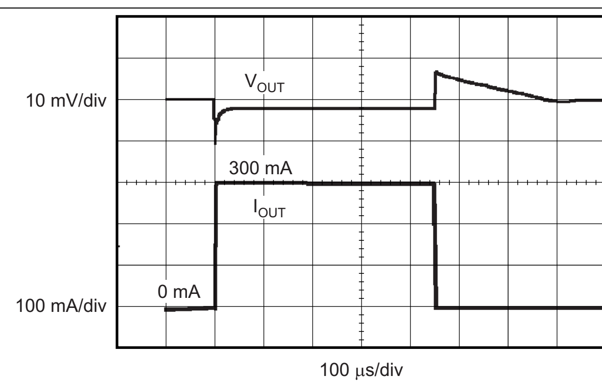
V_{IN} = 2.1 to 2.5 V V_{OUT} = 1.8 V V_{BIAS} = 3.2 V
V_{IN} slew rate = 1 V/μs I_{OUT} = 350 mA

Figure 22. V_{IN} Line Transient Response



V_{IN} = 2.3 V V_{OUT} = 1.8 V V_{BIAS} = 3.2 V to 3.8 V
V_{BIAS} slew rate = 600 m/μs I_{OUT} = 350 mA

Figure 23. V_{BIAS} Line Transient Response



V_{IN} = 2.3 V V_{OUT} = 1.8 V V_{BIAS} = 3.2 V
t_{RISE} = 1 μs

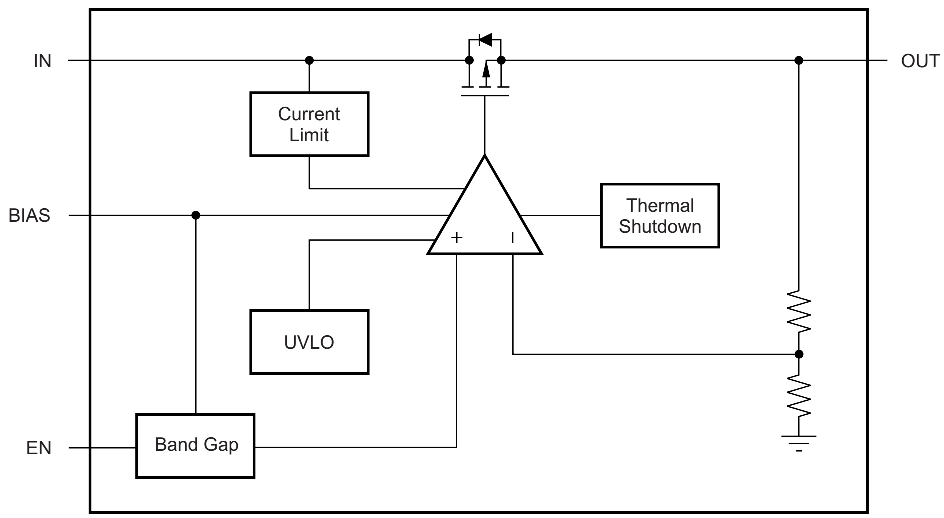
Figure 24. Load Transient Response

7 Detailed Description

7.1 Overview

The TPS720-Q1 family of LDO regulators uses innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1 MHz) at very low headroom (V_{IN} – V_{OUT}). The implementation of the BIAS pin on the TPS720-Q1 vastly improves efficiency of low V_{OUT} applications by allowing the use of a pre-regulated, low-voltage input supply. The TPS720-Q1 supports a novel feature where the output of the LDO regulates under light loads (< 500 µA) when the IN pin is left floating. The light-load drive current is sourced from V_{BIAS} under this condition. This feature is particularly useful in power-saving applications where the dc-dc converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load. These features, combined with low noise, low ground pin current, and ultra-small packaging, make this device ideal for portable applications. This family of regulators offers sub-band-gap output voltages, current limit, and thermal protection, and is fully specified from –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TPS720-Q1 internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The NMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{OUT}$ until thermal shutdown is triggered and the device is turned off. When the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see *Thermal Considerations* for more details.

The NMOS pass element in the TPS720-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, TI recommends external limiting to 5% of rated output current.

7.3.2 Inrush Current Limit

The TPS720-Q1 family of LDO regulators implements a novel inrush current limit circuit architecture: the current drawn through the IN pin is limited to a finite value. This $I_{INRUSHLIMIT}$ charges the output to the final voltage. All current drawn through V_{IN} charges the output capacitance when the load is disconnected. Equation 1 shows the inrush current limit performed by the circuit.

$$I_{INRUSHLIMIT}(A) = C_{OUT}(\mu F) \times 0.454545(V/\mu s) + I_{LOAD}(A) \quad (1)$$

Feature Description (continued)

Assuming a C_{OUT} of 2.2 μF with the load disconnected (that is, I_{LOAD} = 0), the $I_{INRUSHLIMIT}$ is calculated to be 100 mA. The inrush current charges the LDO output capacitor. If the output of the LDO regulates to 1.3 V, then the LDO charges the output capacitor to the final output value in approximately 28.6 μs.

Another consideration is when a load is connected to the output of an LDO. The TPS720-Q1 inrush current limit circuit employs a technique that supplies not only the $I_{INRUSHLIMIT}$, but the additional current required by the load. If I_{LOAD} = 350 mA, then $I_{INRUSHLIMIT}$ calculates to be approximately 450 mA (from Equation 1).

7.3.3 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

7.3.4 Undervoltage Lockout (UVLO)

The TPS720-Q1 uses an undervoltage lockout circuit on the BIAS pin to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature that typically ignores undershoot transients on the input if these transients are less than 50 μs in duration.

7.4 Device Functional Modes

Driving the EN pin over 1.1 V turns on the regulator. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is typically reduced to 500 nA.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Requirements

Although a capacitor is not required for stability on the IN pin, good analog design practice is to connect a 0.1-µF to 1-µF low equivalent series resistance (ESR) capacitor across the IN pin input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located far from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The BIAS pin does not require an input capacitor because BIAS does not source high currents. However, if source impedance is not sufficiently low, TI recommends a small 0.1-µF bypass capacitor.

The TPS720-Q1 is designed to be stable with standard ceramic capacitors with values of 2.2 µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 250 mΩ.

8.1.2 Output Regulation With the IN Pin Floating

The TPS720-Q1 supports a novel feature where the output of the LDO regulates under light loads when the IN pin is left floating. Under normal conditions when the IN pin is connected to a power source, the BIAS pin draws only tens of milliamperes. However, when the IN pin is floating, an innovative circuit allows a maximum current of 500 µA to be drawn by the load through the BIAS pin and maintains the output in regulation. This feature is particularly useful in power-saving applications where a dc-dc converter connected to the IN pin is disabled, but the LDO is required to regulate the output voltage to a light load.

Figure 25 shows an application example where a microcontroller is not turned off (to maintain the state of the internal memory), but where the regulated supply (shown as the TPS62xxx) is turned off to reduce power. In this case, the TPS720-Q1 BIAS pin provides sufficient load current to maintain a regulated voltage to the microcontroller.

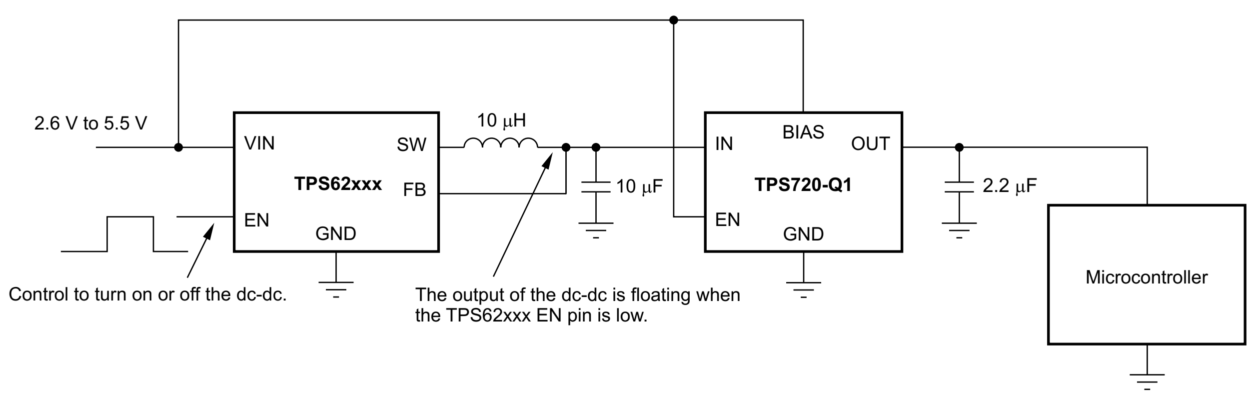


Figure 25. Floating IN Pin Regulation Example

Application Information (continued)

8.1.3 Dropout Voltage

The TPS720-Q1 uses a NMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the NMOS pass element. V_{DO} approximately scales with output current because the NMOS device behaves like a resistor in dropout.

PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 19.

8.1.4 Transient Response

Increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response.

8.1.5 Minimum Load

The TPS720-Q1 is stable with no output load. Although some LDOs suffer from low loop gain at very light output loads, the TPS720-Q1 employs an innovative, low-current mode circuit under very light or no-load conditions which improves output voltage regulation performance.

8.2 Typical Application

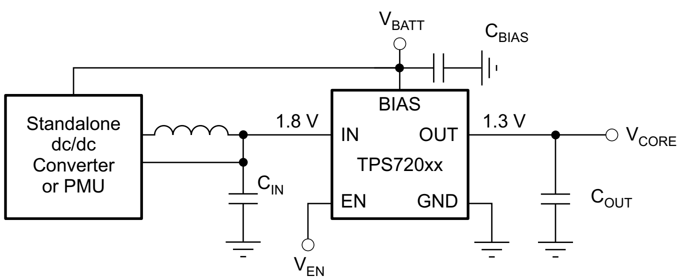


Figure 26. Typical Application Schematic

8.2.1 Design Requirements

Table 1 lists the parameters for this design example.

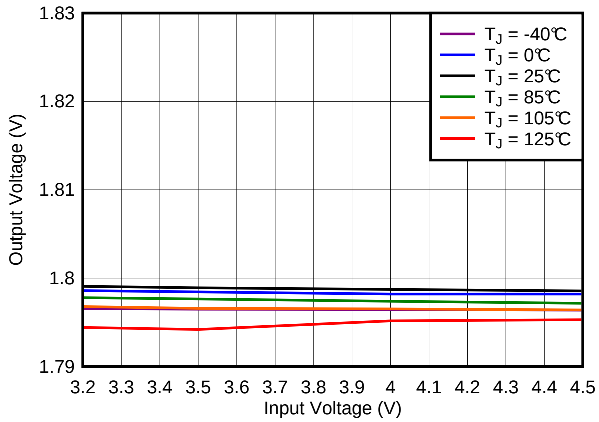
Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	2.3 V
V_{BIAS}	3.2 V
V_{OUT}	1.8 V
I_{OUT}	10-mA typical, 350-mA peak

8.2.2 Detailed Design Procedures

TI recommends selecting the minimum component size; a small size solution for this design example is desired. Set C_{IN} = 1 µF, C_{BIAS} = 100 nF, and C_{OUT} = 2.2 µF.

8.2.3 Application Curves



I_{OUT} = 350 mA

Figure 27. V_{IN} Line Regulation

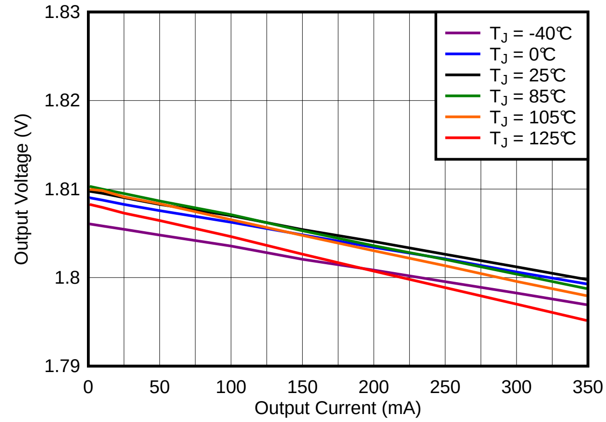


Figure 28. Load Regulation

9 Power Supply Recommendations

The input supply and bias supply for the LDO must be within the recommended operating conditions and must provide adequate headroom for the device to have a regulated output. The minimum capacitor requirements must be met, and if the input supply is noisy, additional input capacitors with low ESR can improve transient performance.

10 Layout

10.1 Layout Guidelines

TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device to improve ac performance (such as PSRR, output noise, and transient response.) In addition, the ground connection for the output capacitor must be connected directly to the GND pin of the device. High equivalent series resistance (ESR) capacitors can degrade PSRR. The BIAS pin draws very little current and can be routed as a signal. Take care to shield the BIAS pin from high frequency coupling.

10.2 Layout Example

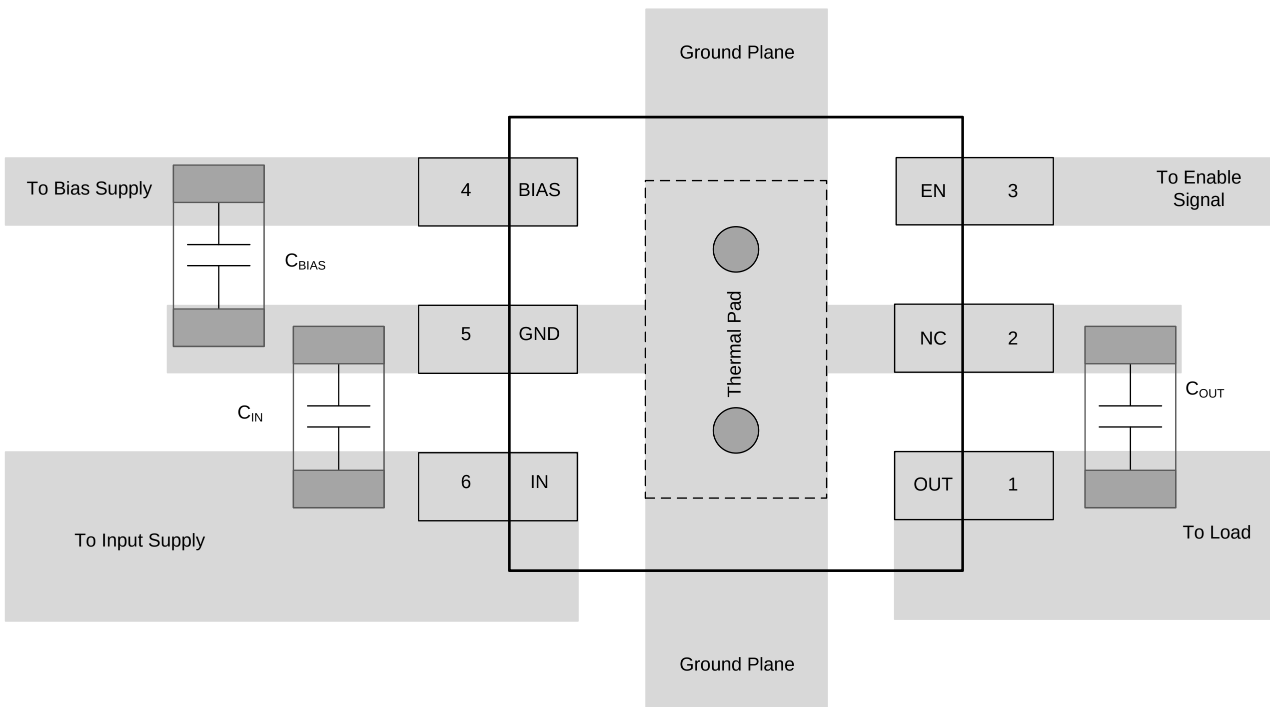


Figure 29. Recommended Layout

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to a maximum of +125°C. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS720-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS720-Q1 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The printed-circuit-board (PCB) area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS720-Q1. The TPS720xxDRVEVM evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.2 Device Nomenclature

Table 2. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TPS720**xx(x)**Q**yyyz**Q1	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **yyy** is the package designator. **z** is the package quantity. R is for 3000 pieces, T is for 250 pieces.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.9 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *High-Efficiency Step-Down Low Power DC-DC Converter* (SGLS243).
- *TPS720xxDRVEVM Evaluation Module* (SBVU024).
- *Using New Thermal Metrics* (SBVA025).

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS72009QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11P
TPS72009QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11P
TPS720105QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15G
TPS720105QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15G
TPS72010QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11Q
TPS72010QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11Q
TPS720115QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15H
TPS720115QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15H
TPS72011QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11I
TPS72011QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11I
TPS72012QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11R
TPS72012QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11R
TPS72015QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11J
TPS72015QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11J
TPS72018QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11K
TPS72018QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11K
TPS72025QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11W
TPS72025QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11W
TPS72027QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15I
TPS72027QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15I
TPS720285QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11M
TPS720285QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11M
TPS72028QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11L
TPS72028QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11L
TPS72029QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11N
TPS72029QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11N
TPS72030QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11O
TPS72030QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11O
TPS72033QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15J

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS72033QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

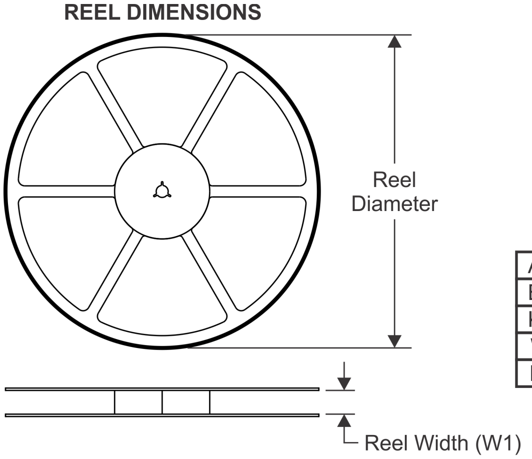
OTHER QUALIFIED VERSIONS OF TPS720-Q1 :

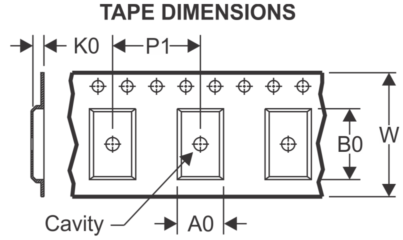
- Catalog : TPS720

NOTE: Qualified Version Definitions:

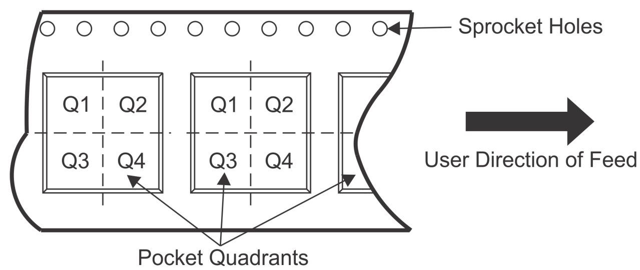
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





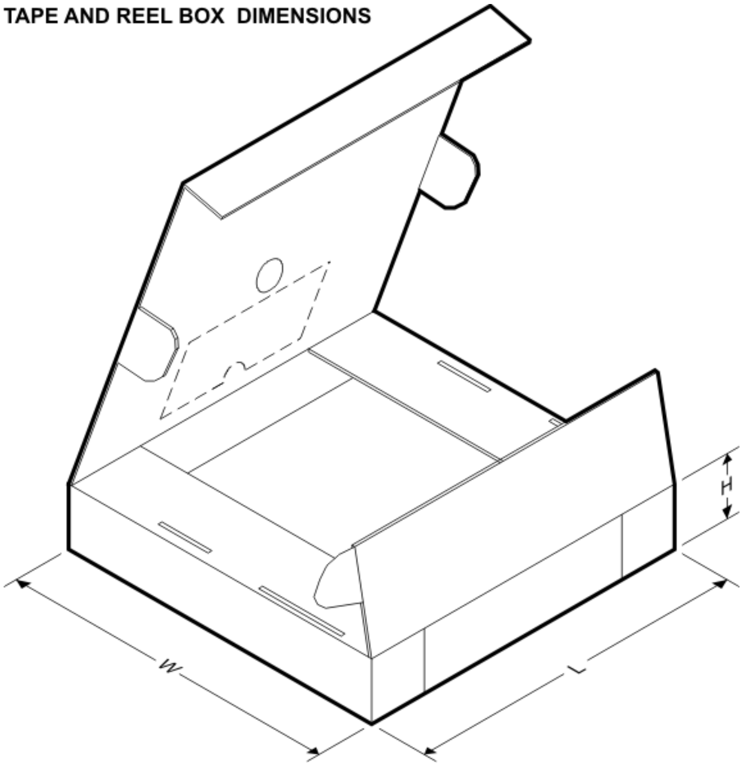
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72009QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS720105QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72010QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS720115QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72011QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72012QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72015QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72018QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72025QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72027QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS720285QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72028QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72029QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72030QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72033QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

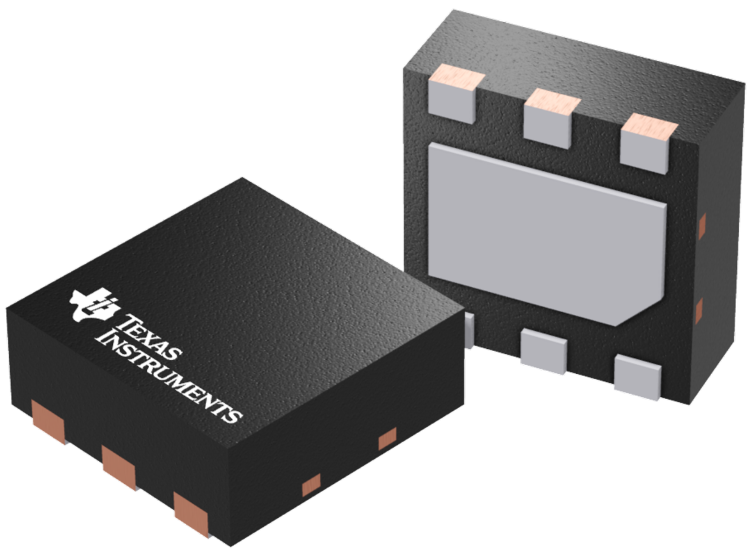


*All dimensions are nominal

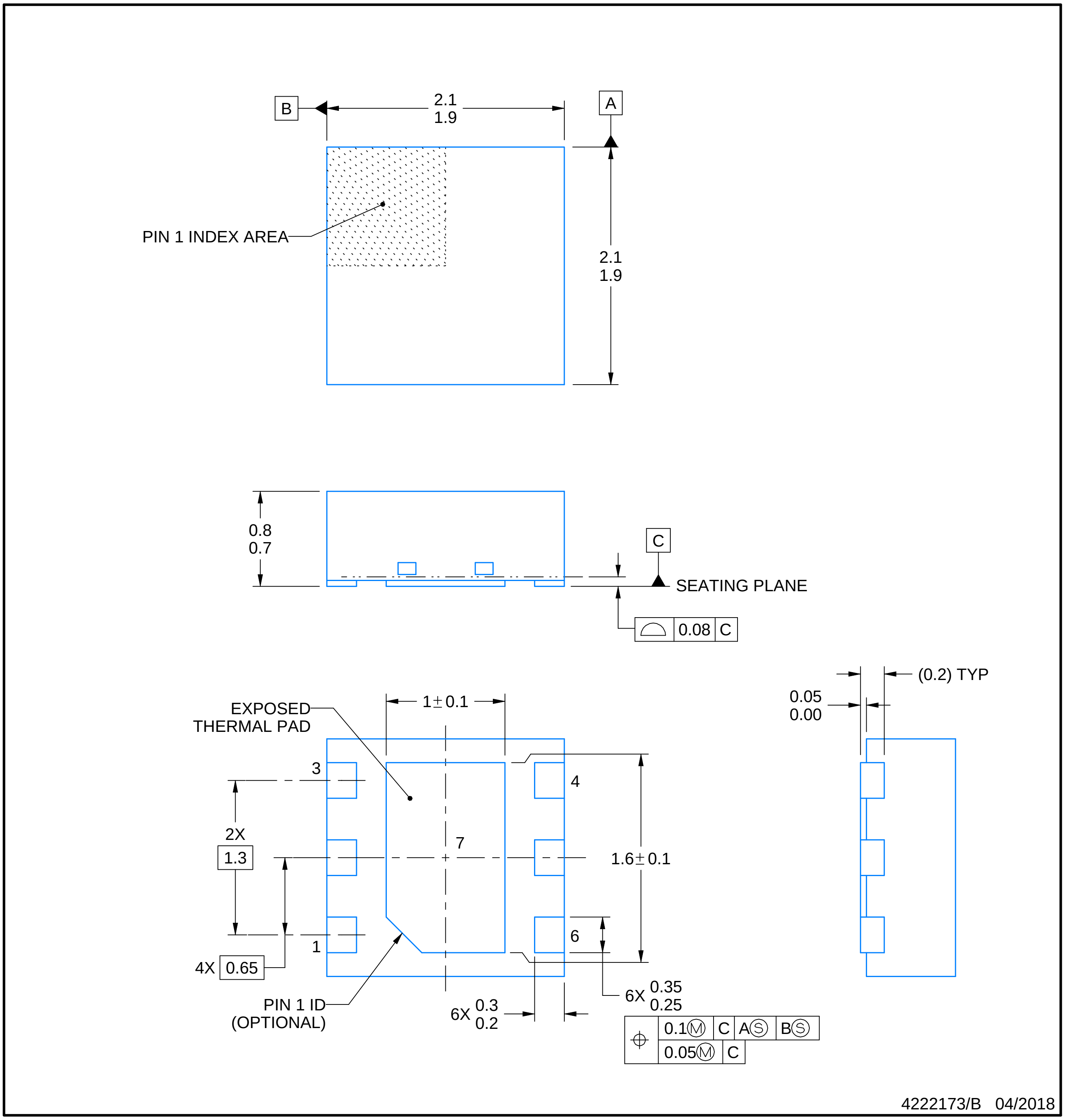
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72009QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS720105QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72010QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS720115QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72011QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72012QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72015QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72018QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72025QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72027QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS720285QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72028QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72029QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72030QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
TPS72033QDRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0

DRV 6 — WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

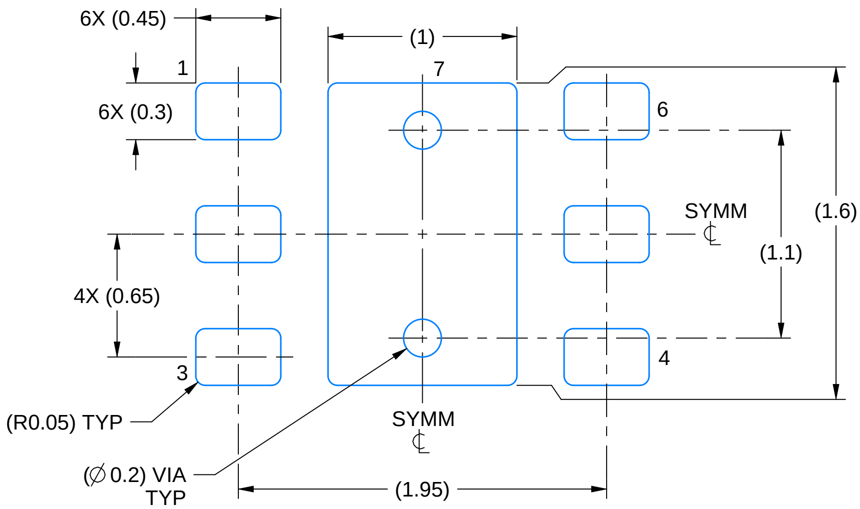


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

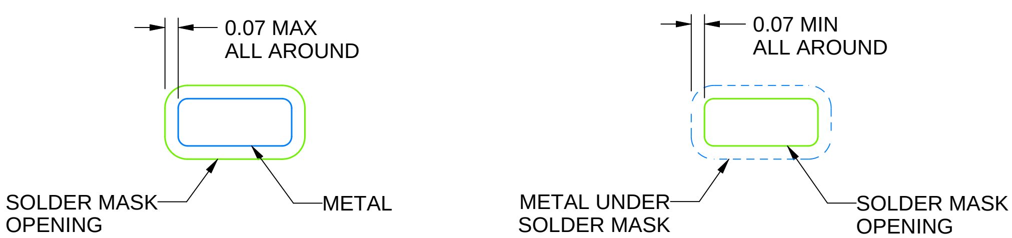


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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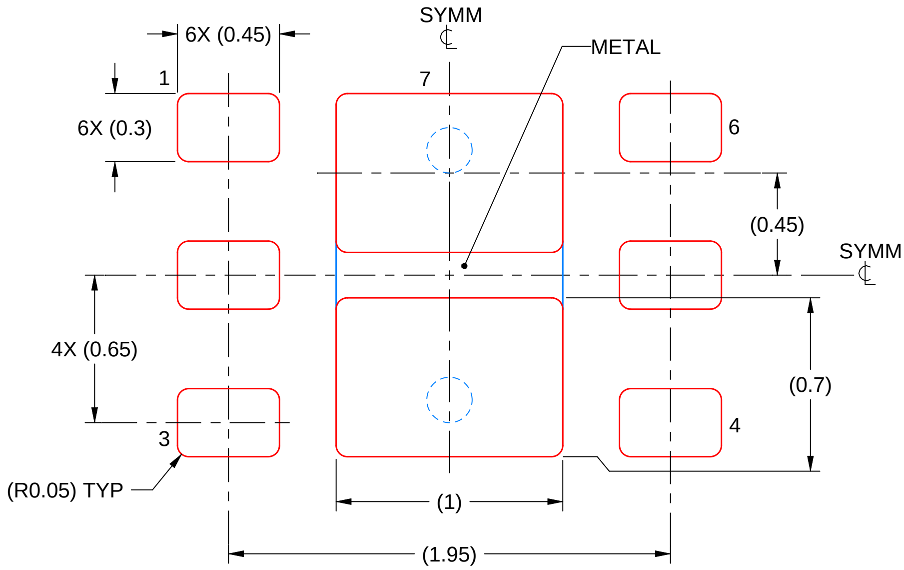
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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