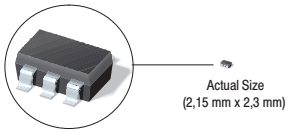


50-mA, 24-V, 3.2-μA SUPPLY CURRENT, LOW-DROPOUT LINEAR REGULATOR

FEATURES

- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree(1)**
- **24-V Maximum Input Voltage**
- **Low 3.2-μA Quiescent Current at 50 mA**
- **Stable With Any Capacitor (≥ 0.47 μF)**
- **50-mA Low-Dropout Regulator**
- **Adjustable Output Voltage (1.2 V to 15 V)**
- **Designed to Support MSP430 Families:**
  - **1.9-V Version Ensured to be Higher Than Minimum V_{IN} of 1.8 V**
  - **2.3-V Version Ensured to Meet 2.2-V Minimum V_{IN} for Flash on MSP430F2xx**
  - **3.45-V Version Ensured to be Lower Than Maximum V_{IN} of 3.6 V**
  - **Wide Variety of Fixed Output Voltage Options to Match V_{IN} to the Minimum Required for Desired MSP430 Speed**
- **Minimum/Maximum Specified Current Limit**
- **5-Pin SC70/SOT-323 (DCK) Package**
- **For 80-mA Rated Current and Higher Power Package, See TPS715Axx**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

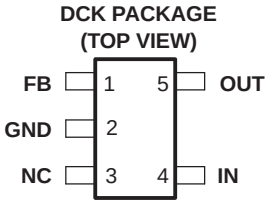
APPLICATIONS

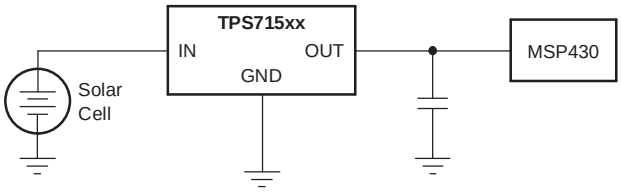
- **Ultra-Low Power Microcontrollers**
- **Cellular/Cordless Handsets**
- **Portable/Battery-Powered Equipment**

DESCRIPTION

The TPS71501 low-dropout (LDO) voltage regulators offer the benefits of high input voltage, low dropout voltage, low-power operation, and miniaturized packaging. The device, which operates over an input range of 2.5 V to 24 V, is stable with any capacitor (≥0.47 μF). The low dropout voltage and low quiescent current allow operation at extremely low power levels. Therefore, the devices are ideal for powering battery-management ICs. Specifically, because the devices are enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously operating battery-charging ICs.

The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the low dropout voltage, typically 415 mV at 50 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 μA typically) is stable over the entire range of output load current (0 mA to 50 mA).





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SC70 – DCK	Reel of 3000	TPS71501MDCKREP	CVP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted(1)(2)

V_{IN}	Input voltage range	IN	–0.3 V to 24 V
V_{OUT}	Output voltage range	OUT	–0.3 V to 6 V
	Peak output current		Internally limited
	Continuous total power dissipation		See Dissipation Ratings Table
T_J	Junction temperature range		–55°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
ESD	Electrostatic discharge rating	Human-Body Model (HBM)	2000 V
		Charged-Device Model (CDM)	500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$°C/W	$R_{\theta JA}$°C/W	DERATING FACTOR ABOVE T_A = +25°C	$T_A \le 25$°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(1)	DCK	165	395	2.52 mW/°C	250 mW	140 mW	100 mW
High-K(2)	DCK	165	315	3.18 mW/°C	320 mW	175 mW	130 mW

(1) The JEDEC Low-K (1s) board design used to derive this data was a 3-in × 3-in, two-layer board with 2-oz copper traces on top of the board.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3-in × 3-in, multilayer board with 1-oz internal power and ground planes and 2-oz copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating junction temperature range (T_J = –55°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage(1)		V_{IN}	I_O = 10 mA	2.5		24	V
			I_O = 50 mA	3		24	
V_{OUT} voltage range				1.2		15	V
V_{OUT} accuracy(1)	Over V_{IN}, I_{OUT}, and temperature		V_{IN} + 1.0 V ≤ V_{IN} ≤ 24 V 100 µA ≤ I_{OUT} ≤ 50 mA	–6.25		+6.25	%
Ground pin current(2)		I_{GND}	0 ≤ I_{OUT} ≤ 50 mA, T_J = –40°C to +85°C		3.2	4.2	µA
			0 mA ≤ I_{OUT} ≤ 50 mA		3.2	4.8	
			0 mA ≤ I_{OUT} ≤ 50 mA, V_{IN} = 24 V			5.8	
Load regulation	$\Delta V_{OUT}/\Delta I_{OUT}$		I_{OUT} = 100 µA to 50 mA		22		mV
Output voltage line regulation (1)	$\Delta V_{OUT}/\Delta V_{IN}$		V_{OUT} + 1 V < V_{IN} ≤ 24 V		20	75	mV
Output noise voltage		V_n	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms
Output current limit		I_{CL}	V_{OUT} = 0 V, V_{IN} ≥ 3.5 V	125		750	mA
			V_{OUT} = 0 V, V_{IN} < 3.5 V	90		750	mA
Power-supply ripple rejection		PSRR	f = 100 kHz, C_{OUT} = 10 µF		60		dB
Dropout voltage V_{IN} = $V_{OUT(NOM)}$ – 1 V		V_{DO}	I_{OUT} = 50 mA		415	750	mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or the value shown for *Input voltage* in this table, whichever is greater.
(2) See Figure 1. The TPS71501 employs a leakage null control circuit. This circuit is active only if output current is less than pass FET leakage current. The circuit is typically active when output load is less than 5 µA, V_{IN} is greater than 18 V, and die temperature is greater than 100°C.

FUNCTIONAL BLOCK DIAGRAM

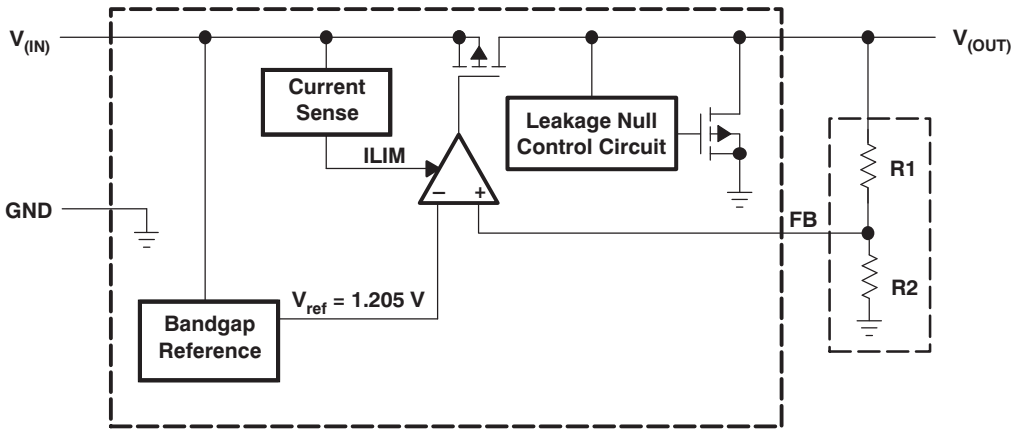


Figure 1. Functional Block Diagram

Table 1. Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
FB	1	Feedback. This terminal is used to set the output voltage.
GND	2	Ground
NC	3	No connection
IN	4	Input supply
OUT	5	Output of the regulator, any output capacitor ≥ 0.47 μF can be used for stability.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT CURRENT

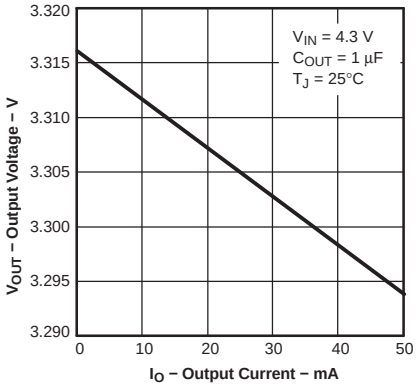


Figure 2.

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

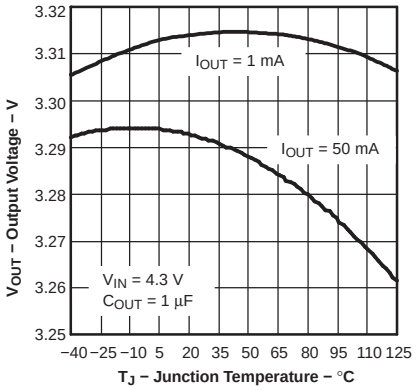


Figure 3.

QUIESCENT CURRENT vs JUNCTION TEMPERATURE

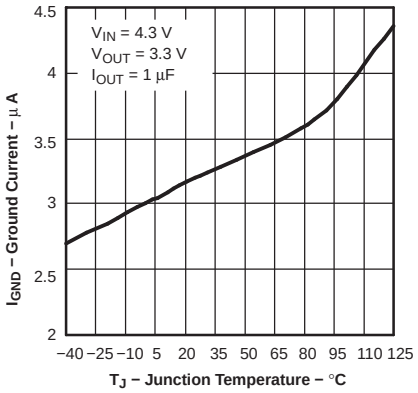


Figure 4.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

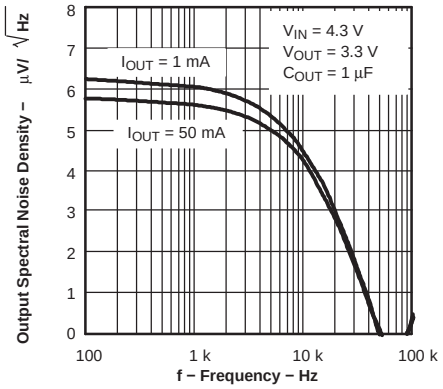


Figure 5.

OUTPUT IMPEDANCE vs FREQUENCY

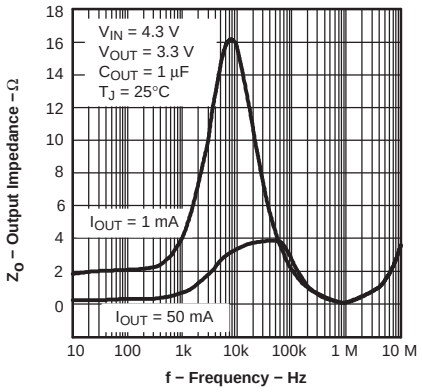


Figure 6.

DROPOUT VOLTAGE vs OUTPUT CURRENT

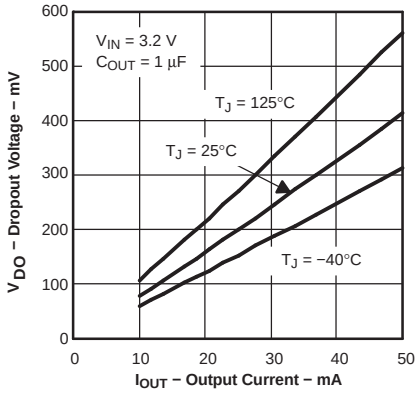


Figure 7.

TPS71501 DROPOUT VOLTAGE vs INPUT VOLTAGE

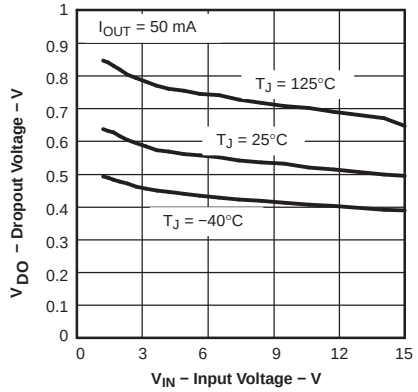


Figure 8.

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

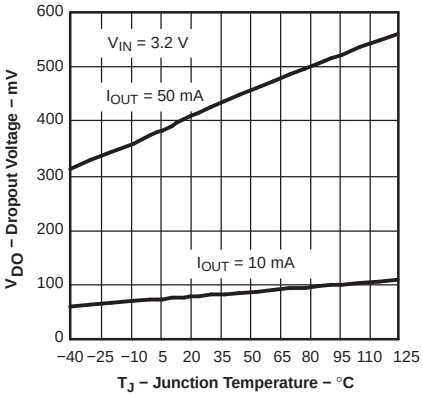


Figure 9.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

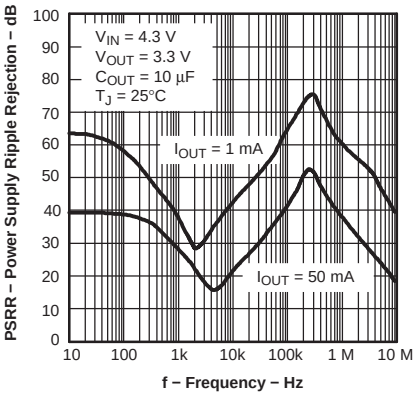


Figure 10.

TYPICAL CHARACTERISTICS (continued)

POWER UP / POWER DOWN

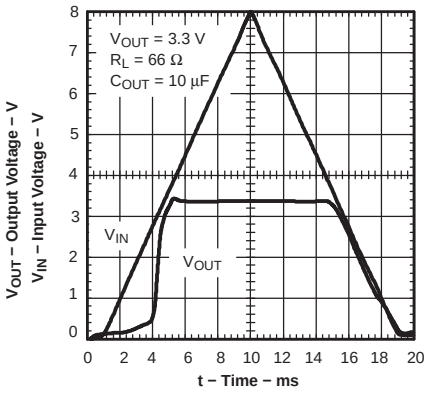


Figure 11.

LINE TRANSIENT RESPONSE

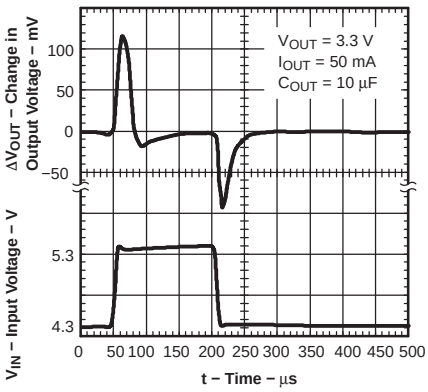


Figure 12.

LOAD TRANSIENT RESPONSE

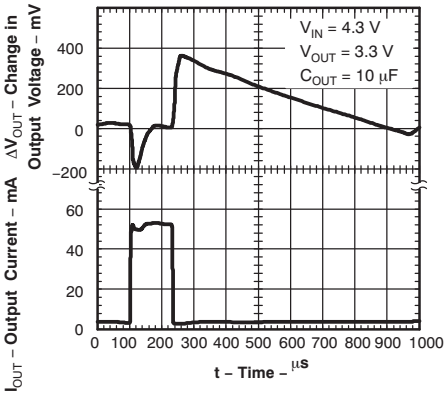


Figure 13.

APPLICATION INFORMATION

The TPS71501 LDO regulator has been optimized for ultra-low power applications such as the MSP430 microcontroller. Its ultra-low supply current maximizes efficiency at light loads, and its high input voltage range makes it suitable for supplies such as unconditioned solar panels.

External Capacitor Requirements

Although not required, a 0.047-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS71501 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) ≥ 0.47 µF properly stabilizes this loop. X7R type capacitors are recommended but X5R and others may be used.

Power Dissipation and Junction Temperature

To ensure reliable operation, worst-case junction temperature should not exceed +125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the Dissipation Ratings table).
- T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

For a higher power package version of the TPS715xx, see the TPS715Axx.

Regulator Protection

The TPS71501 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS71501 features internal current limiting. During normal operation, the TPS71501 limits output current to approximately 500 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

Programming the TPS71501 Adjustable LDO Regulator

The output voltage of the TPS71501 adjustable regulator is programmed using an external resistor divider as shown in Figure 14. The output voltage operating range is 1.2 V to 15 V, and is calculated using:

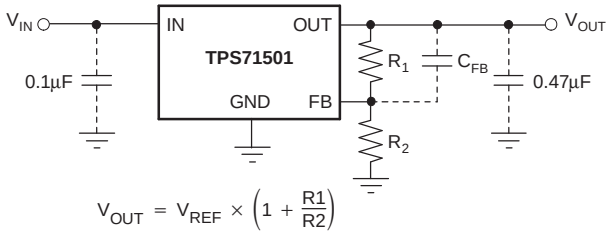
$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

where:

- V_{REF} = 1.205 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 1.5-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_{OUT}. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using Equation 4:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (4)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2
1.8 V	0.499 MΩ	1 MΩ
2.8 V	1.33 MΩ	1 MΩ
5.0 V	3.16 MΩ	1 MΩ

Figure 14. TPS71501 Adjustable LDO Regulator Programming

Power the MSP430 Microcontroller

Several versions of the TPS715xx are ideal for powering the MSP430 microcontroller. Table 2 shows potential applications of some voltage versions.

Table 2. Typical MSP430 Applications

DEVICE	V_{OUT} (TYP)	APPLICATION
TPS71519	1.9 V	$V_{OUT, MIN}$ > 1.800 V required by many MSP430s. Allows lowest power consumption operation.
TPS71523	2.3 V	$V_{OUT, MIN}$ > 2.200 V required by some MSP430s FLASH operation.
TPS71530	3.0 V	$V_{OUT, MIN}$ > 2.700 V required by some MSP430s FLASH operation.
TPS715345	3.45 V	$V_{OUT, MIN}$ < 3.600 V required by some MSP430s. Allows highest speed operation.

The TPS715xx family offers many output voltage versions to allow designers to minimize the supply voltage for the processing speed required of the MSP430. This minimizes the supply current consumed by the MSP430.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS71501MDCKREP	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	CVP
TPS71501MDCKREP.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	CVP
V62/08619-01XE	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	CVP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

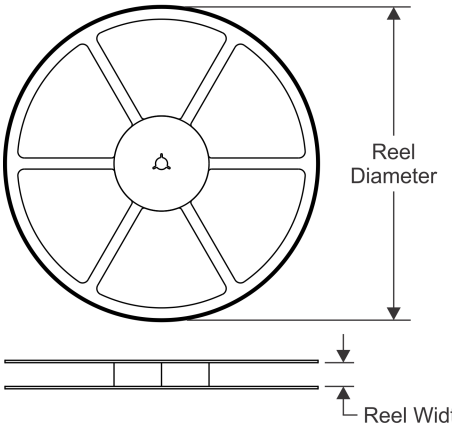
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

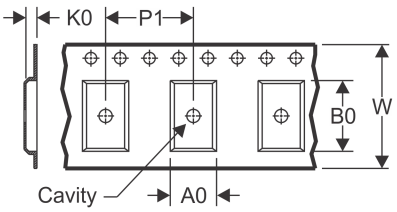
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

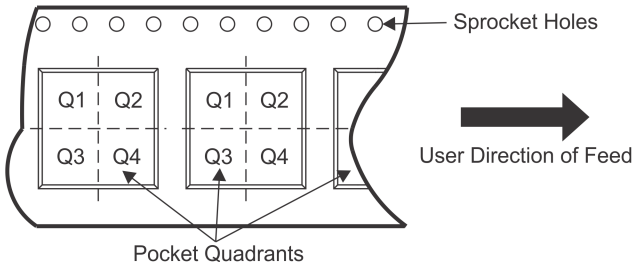


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

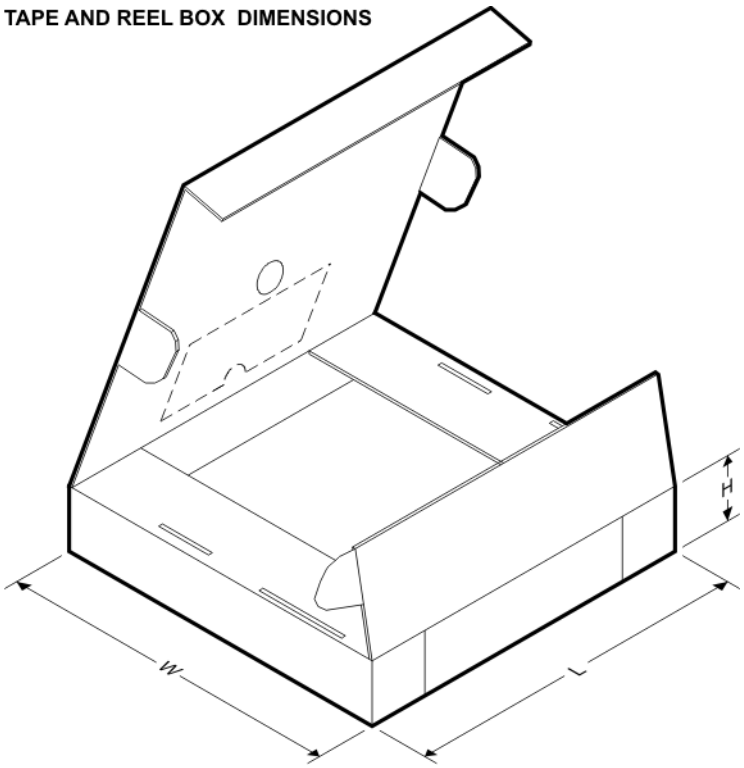
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71501MDCKREP	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

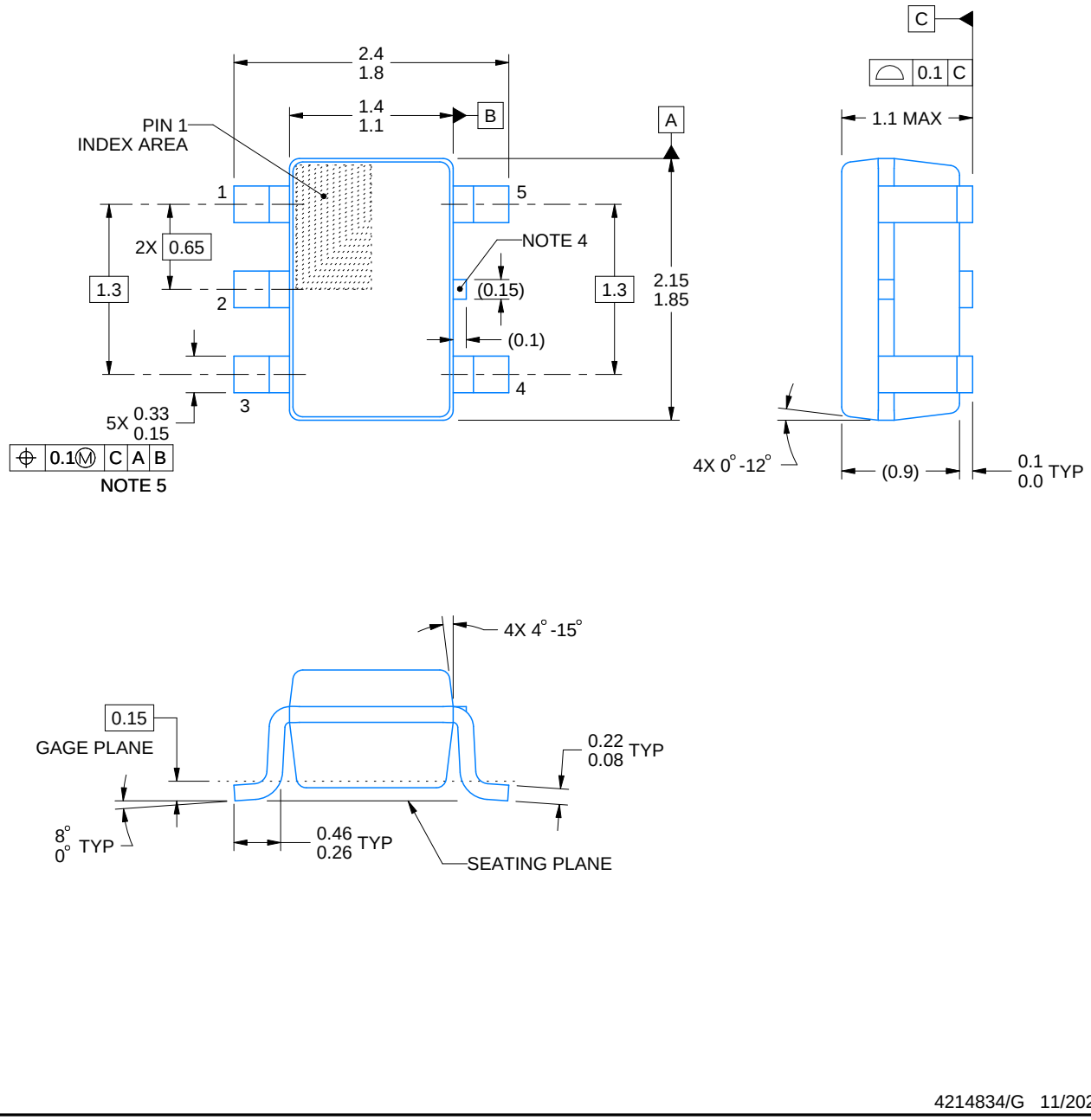
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71501MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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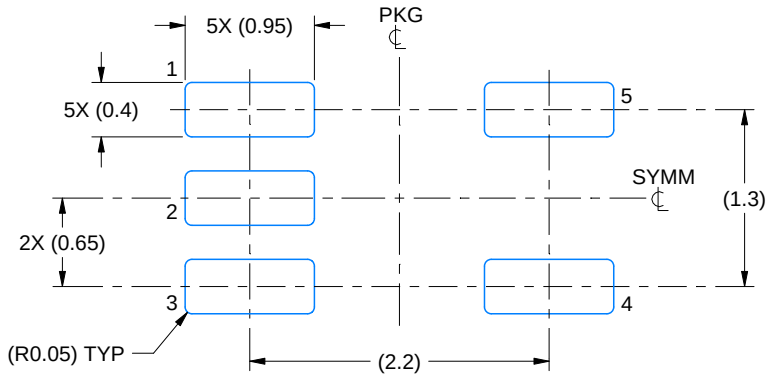
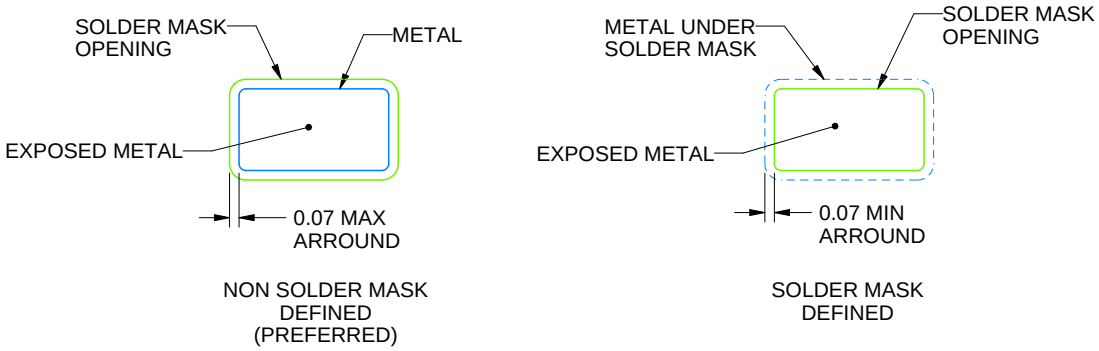
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

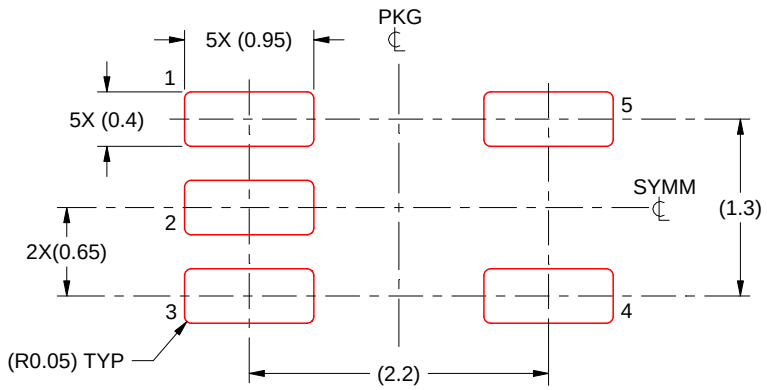


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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