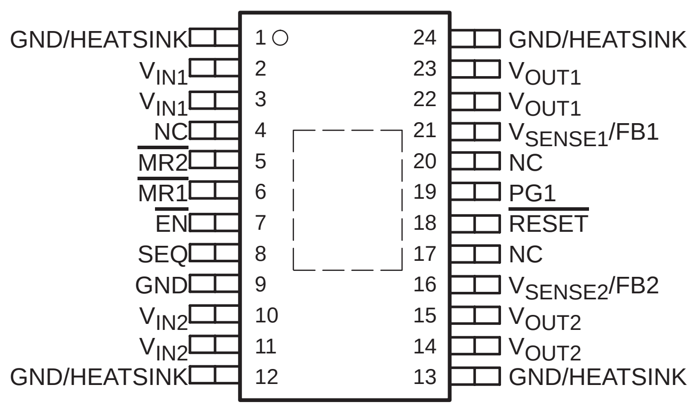
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree**[†]
- **Dual Output Voltages for Split-Supply Applications**
- **Selectable Power Up Sequencing for DSP Applications (See TPS704xx for Independent Enabling of Each Output)**
- **Output Current Range of 1 A on Regulator 1 and 2 A on Regulator 2**
- **Fast Transient Response**
- **Output Voltages of 3.3−V/1.2−V**
- **Open Drain Power-On Reset With 120-ms Delay**
- **Open Drain Power Good for Regulator 1**
- **Ultralow 185 μA (typ) Quiescent Current**
- **2 μA Input Current During Standby**
- **Low Noise: 78 μV_{RMS} Without Bypass Capacitor**
- **Quick Output Capacitor Discharge Feature**
- **Two Manual Reset Inputs**
- **2% Accuracy Over Load and Temperature**
- **Undervoltage Lockout (UVLO) Feature**
- **24-Pin PowerPAD™ TSSOP Package**
- **Thermal Shutdown Protection**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description

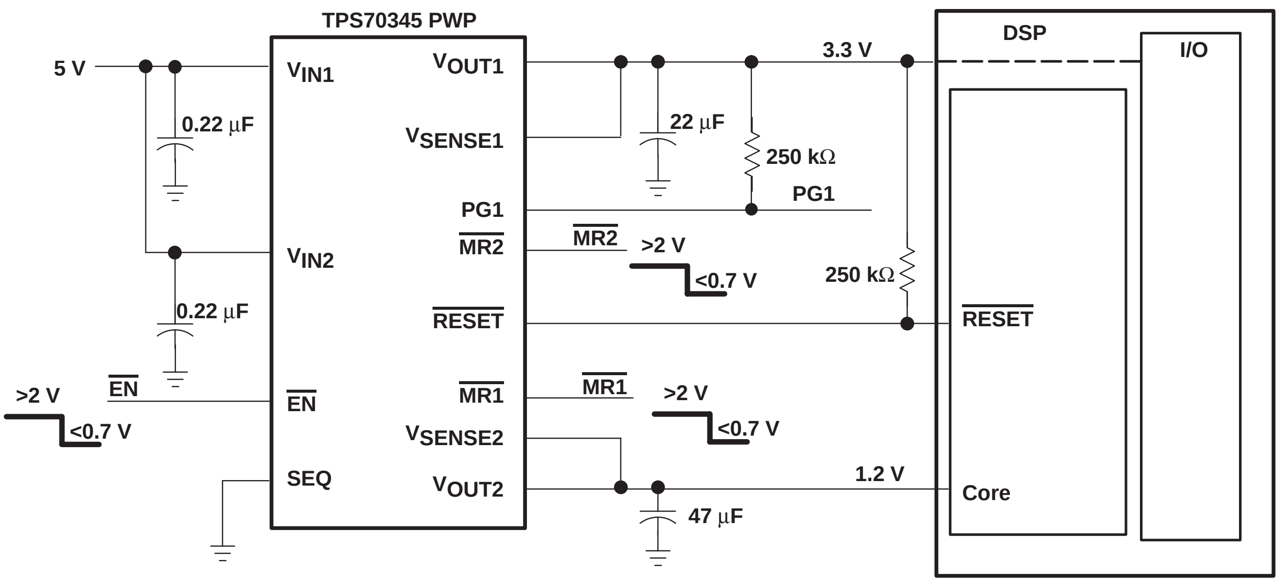
The TPS70345 is designed to provide a complete power management solution for Texas Instruments DSP, processor power, ASIC, FPGA, and digital applications where dual output voltage regulators are required. Easy programmability of the sequencing function makes this family ideal for any Texas Instruments DSP applications with power sequencing requirement. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power on reset), manual reset inputs, and enable function, provide a complete system solution.

PWP PACKAGE
(TOP VIEW)



NC − No internal connection

description (continued)



The TPS70345 voltage regulator offers low dropout voltage and dual outputs with power up sequence control, which is designed primarily for DSP applications. This device has a low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 47 µF low ESR capacitors.

This device has a fixed output voltage 3.3 V/1.2 V. Regulator 1 can support up to 1 A, and regulator 2 can support up to 2 A. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low (typically 160 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is low and independent of output loading (maximum of 250 µA over the full range of output current). This LDO family also features a sleep mode; applying a high signal to $\overline{EN}$ (enable) shuts down both regulators, reducing the input current to 1 µA at T_J = 25°C.

The device is enabled when the $\overline{EN}$ pin is connected to a low-level input voltage. The output voltages of the two regulators are sensed at the V_{SENSE1} and V_{SENSE2} pins respectively.

The input signal at the SEQ pin controls the power-up sequence of the two regulators. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. At that time V_{OUT1} is turned on. If V_{OUT2} is pulled below 83% (i.e. overload condition) of its regulated voltage, V_{OUT1} will be turned off. Pulling the SEQ terminal low reverses the power-up order and V_{OUT1} is turned on first. The SEQ pin is connected to an internal pullup current source.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage conditions at V_{OUT1}. The PG1 pin can be used to implement a SVS (power on reset) for the circuitry supplied by regulator 1.

description (continued)

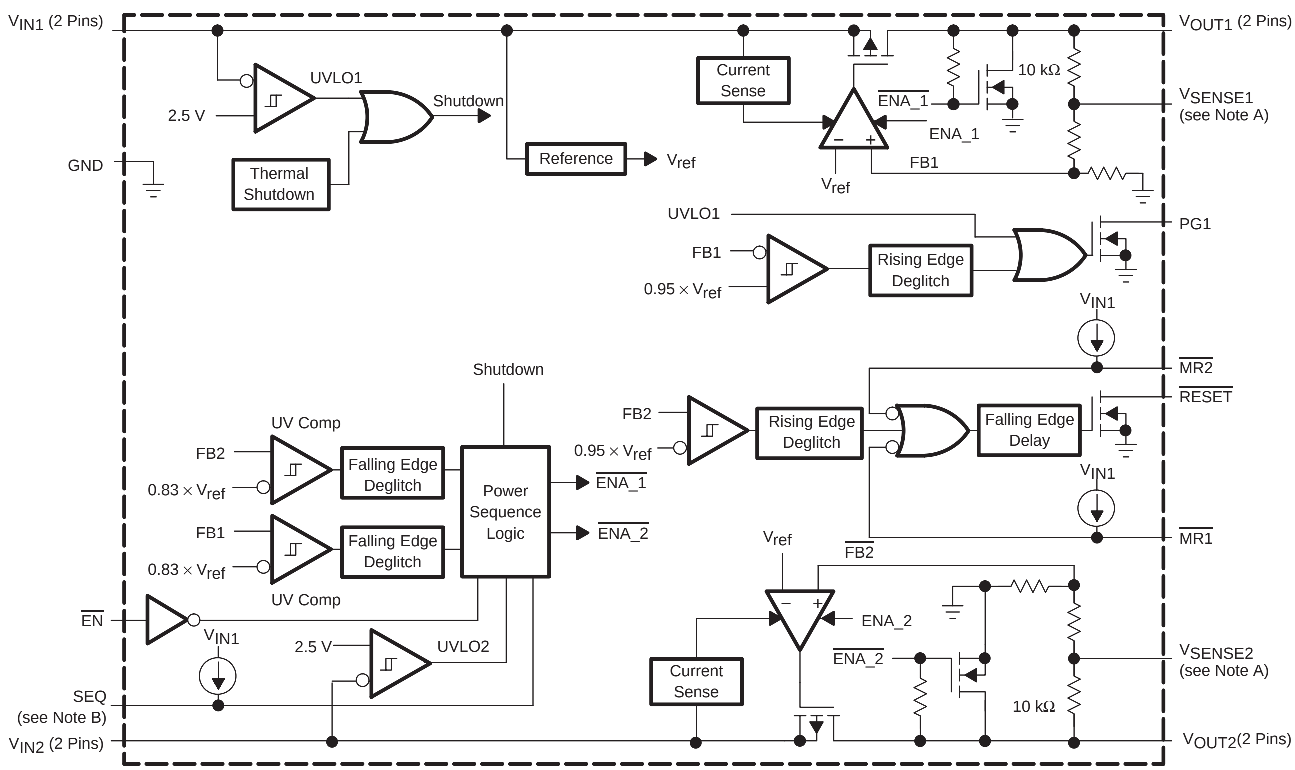
The TPS70345 features a $\overline{\text{RESET}}$ (SVS, POR, or power on reset). $\overline{\text{RESET}}$ is an active low, open drain output and requires a pullup resistor for normal operation. When pulled up, $\overline{\text{RESET}}$ goes to a high impedance state (i.e. logic high) after a 120 ms delay when all three of the following conditions are met. First, V_{IN1} must be above the undervoltage condition. Second, the manual reset ($\overline{\text{MR}}$) pin must be in a high impedance state. Third, V_{OUT2} must be above approximately 95% of its regulated voltage. To monitor V_{OUT1}, the PG1 output pin can be connected to $\overline{\text{MR1}}$ or $\overline{\text{MR2}}$. $\overline{\text{RESET}}$ can be used to drive power on reset or a low-battery indicator. If $\overline{\text{RESET}}$ is not used, it can be left floating.

Internal bias voltages are powered by V_{IN1} and require 2.7 V for full functionality. Each regulator input has an undervoltage lockout circuit that prevents each output from turning on until the respective input reaches 2.5 V.

AVAILABLE OPTIONS

T_J	REGULATOR 1 V_O (V)	REGULATOR 2 V_O (V)	TSSOP (PWP)
−55°C to 125°C	3.3 V	1.2 V	TPS70345MPWPREP

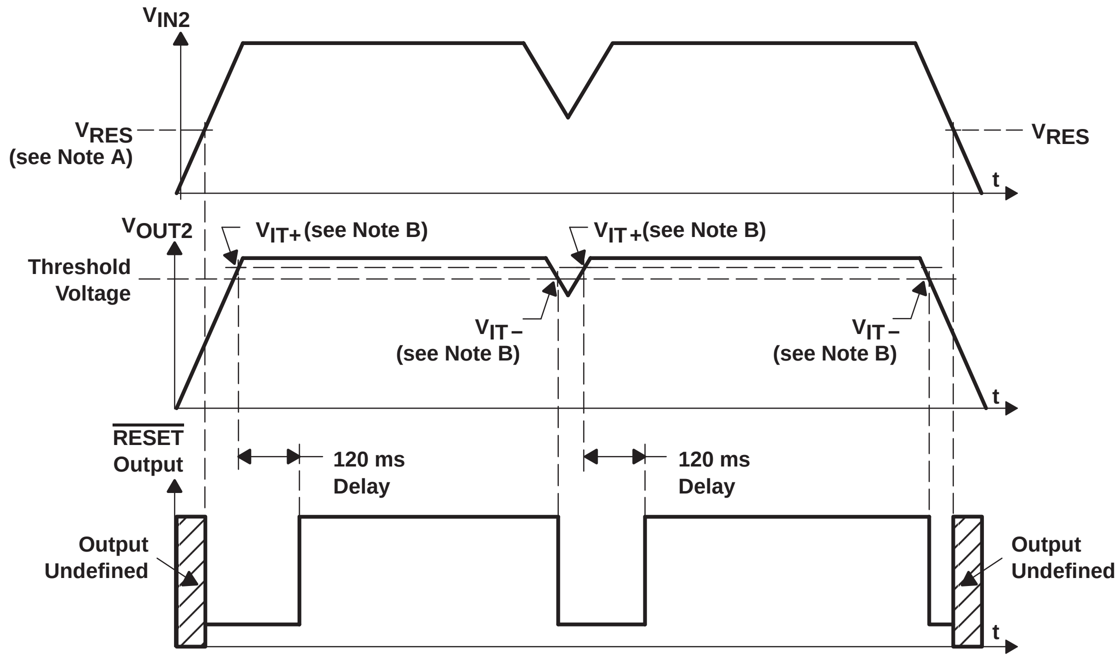
detailed block diagram − fixed voltage version



NOTES: A. For most applications, V_{SENSE1} and V_{SENSE2} should be externally connected to V_{OUT} as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the Application Information section.

B. If the SEQ terminal is floating at the input, V_{OUT2} powers up first.

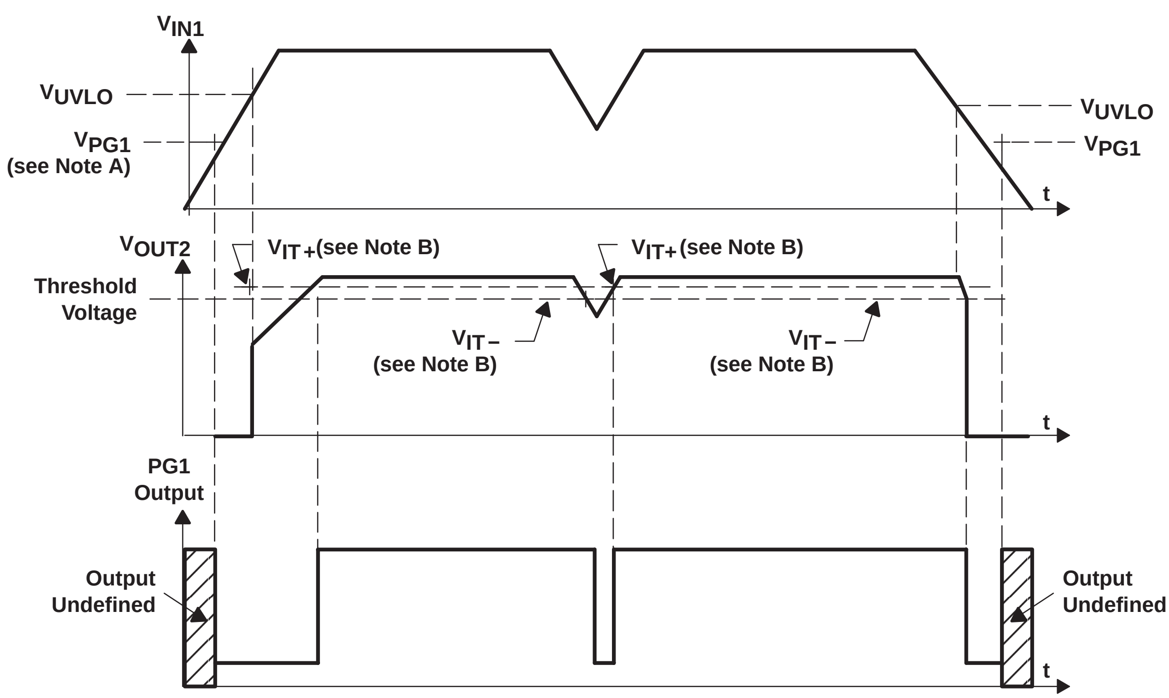
$\overline{\text{RESET}}$ timing diagram (with V_{IN1} powered up and $\overline{\text{MR1}}$ and $\overline{\text{MR2}}$ at logic high)



NOTES: A. V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{RES} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} −Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

PG1 timing diagram



NOTES: A. V_{PG} is the minimum input voltage for a valid PG. The symbol V_{PG} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} −Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	7	I	Active low enable
GND	9		Regulator ground
GND/HEATSINK	1, 12, 13, 24		Ground/heatsink
MR1	6	I	Manual reset input 1, active low, pulled up internally
MR2	5	I	Manual reset input 2, active low, pulled up internally
NC	4, 17, 20		No connection
PG1	19	O	Open drain output, low when V_{OUT1} voltage is less than 95% of the nominal regulated voltage
RESET	18	O	Open drain output, SVS (power on reset) signal, active low
SEQ	8	I	Power up sequence control: SEQ=High, V_{OUT2} powers up first; SEQ=Low, V_{OUT1} powers up first, SEQ terminal pulled up internally.
V_{IN1}	2, 3	I	Input voltage of regulator 1
V_{IN2}	10, 11	I	Input voltage of regulator 2
V_{OUT1}	22, 23	O	Output voltage of regulator 1
V_{OUT2}	14, 15	O	Output voltage of regulator 2
V_{SENSE2}	16	I	Regulator 2 output voltage sense
V_{SENSE1}	21	I	Regulator 1 output voltage sense

detailed description

The TPS70345 low dropout regulator provides dual regulated output voltages for DSP applications that require a high performance power management solution. These devices provide fast transient response and high accuracy, while drawing low quiescent current. Programmable sequencing provides a power solution for DSPs without any external component requirements. This reduces the component cost and board space while increasing total system reliability. The TPS70345 has an enable feature which puts the device in sleep mode reducing the input current to 1 μA. Other features are the integrated SVS (power on reset, $\overline{\text{RESET}}$) and power good (PG1). These monitor output voltages and provide logic output to the system. These differentiated features provide a complete DSP power solution.

The TPS70345, unlike many other LDOs, features low quiescent current which remains virtually constant even with varying loads. Conventional LDO regulators use a PNP pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS70345 uses a PMOS transistor to pass current. Because the gate of the PMOS is voltage driven, operating current is low and stable over the full load range.

pin functions

enable

The $\overline{\text{EN}}$ terminal is an input which enables or shuts down the device. If $\overline{\text{EN}}$ is at a logic high signal the device is in shutdown mode. When the $\overline{\text{EN}}$ goes to voltage low, then the device is enabled.

sequence

The SEQ terminal is an input that programs which output voltage (V_{OUT1} or V_{OUT2}) is turned on first. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. If V_{OUT2} is pulled below 83% (i.e., over load condition) V_{OUT1} is turned off. This terminal has a 6-μA pullup current to V_{IN1}.

Pulling the SEQ terminal low reverses the power-up order and V_{OUT1} is turned on first. For detailed timing diagrams see Figure 26 through Figure 30.

detailed description (continued)

power good (PG1)

The PG1 terminal is an open drain, active high output terminal which indicates the status of the V_{OUT1} regulator. When the V_{OUT1} reaches 95% of its regulated voltage, PG1 goes to a high impedance state. PG1 goes to a low impedance state when V_{OUT1} is pulled below 95% (i.e., over load condition) of its regulated voltage. The open drain output of the PG1 terminal requires a pullup resistor.

manual reset pins ($\overline{MR1}$ and $\overline{MR2}$)

$\overline{\text{MR1}}$ and $\overline{\text{MR2}}$ are active low input terminals used to trigger a reset condition. When either $\overline{\text{MR1}}$ or $\overline{\text{MR2}}$ is pulled to logic low, a POR ($\overline{\text{RESET}}$) occurs. These terminals have a 6-µA pullup current to V_{IN1}. It is recommended that these pins be pulled high to V_{IN} when they are not used.

sense (V_{SENSE1}, V_{SENSE2})

The sense terminals of fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, the sense terminals connect to high-impedance wide-bandwidth amplifiers through resistor-divider networks and noise pickup feeds through to the regulator output. It is essential to route the sense connections in such a way to minimize/avoid noise pickup. Adding RC networks between the V_{SENSE} terminals and V_{OUT} terminals to filter noise is not recommended because it can cause the regulators to oscillate.

$\overline{RESET}$ indicator

$\overline{\text{RESET}}$ is an active low, open drain output and requires a pullup resistor for normal operation. When pulled up, $\overline{\text{RESET}}$ goes to a high impedance state (i.e. logic high) after a 120 ms delay when all three of the following conditions are met. First, V_{IN1} must be above the undervoltage condition. Second, the manual reset ($\overline{\text{MR}}$) pin must be in a high impedance state. Third, V_{OUT2} must be above approximately 95% of its regulated voltage. To monitor V_{OUT1}, the PG1 output pin can be connected to $\overline{\text{MR1}}$ or $\overline{\text{MR2}}$.

V_{IN1} and V_{IN2}

V_{IN1} and V_{IN2} are inputs to the regulators.

V_{OUT1} and V_{OUT2}

V_{OUT1} and V_{OUT2} are output terminals of each regulator.

absolute maximum ratings over operating junction temperature (unless otherwise noted)†

Input voltage range‡: V_{IN1}	−0.3 V to 7 V
V_{IN2}	−0.3 V to 7 V
Voltage range at $\overline{EN}$	−0.3 V to 7 V
Output voltage range (V_{OUT1}, V_{SENSE1})	5.5 V
Output voltage range (V_{OUT2}, V_{SENSE2})	5.5 V
Maximum $\overline{RESET}$, PG1 voltage	7 V
Maximum $\overline{MR1}$, $\overline{MR2}$, and SEQ voltage	V_{IN1}
Peak output current	Internally limited
Operating virtual junction temperature range, T_J	−55°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
ESD rating, HBM	2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are tied to network ground.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I¶	2.7	6	V
Output current, I_O (regulator 1)	0	1	A
Output current, I_O (regulator 2)	0	2	A
Operating virtual junction temperature, T_J	−55	125	°C

¶ To calculate the minimum input voltage for maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

electrical characteristics over recommended operating junction temperature (T_J = −55°C to 125°C) V_{IN1} or V_{IN2} = $V_{OUTX(nom)}$ + 1 V, I_{OUTX} = 1 mA, $\overline{EN}$ = 0, C_{OUT1} = 22 μF, C_{OUT2} = 47 μF(unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage (see Note 1 and Note 3)	Reference voltage	2.7 V < V_I < 6 V, FB connected to V_O T_J = 25°C		1.224		V
			2.7 V < V_I < 6 V, FB connected to V_O	1.196		1.248	
		1.2 V Output (V_{OUT2})	2.7 V < V_I < 6 V, T_J = 25°C		1.2		
			2.7 V < V_I < 6 V	1.176		1.224	
Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{EN}$ = 0 V, (see Note 1)			See Note 3, T_J = 25°C		185		μA
			See Note 3			250	
Output voltage line regulation ($\Delta V_O/V_O$) for regulator 1 and regulator 2 (see Note 2)			V_O + 1 V < V_I ≤ 6 V, T_J = 25°C, See Note 1		0.01%		V
			V_O + 1 V < V_I ≤ 6 V, See Note 1			0.1%	
Load regulation for V_{OUT1} and V_{OUT2}			T_J = 25°C, See Note 3		1		mV
Output current limit		Regulator 1	V_O = 0 V		1.75	2.35	A
		Regulator 2			3.8	4.8	
Thermal shutdown junction temperature					150		°C
$I_{I(standby)}$	Standby current		$\overline{EN}$ = V_I, T_J = 25°C		1	2	μA
			$\overline{EN}$ = V_I			10	
RESET terminal							
Minimum input voltage for valid $\overline{RESET}$			$I_{(RESET)}$ = 300 μA, $V_{(RESET)}$ ≤ 0.8 V		1	1.3	V
Trip threshold voltage			V_O decreasing	92%	95%	98%	V_O
Hysteresis voltage			Measured at V_O		0.5%		V_O
$t_{(RESET)}$			$\overline{RESET}$ pulse duration	80	120	160	ms
$t_{r(RESET)}$			Rising edge deglitch		30		μs
Output low voltage			V_I = 3.5 V, $I_{(RESET)}$ = 1 mA		0.15	0.4	V
Leakage current			$V_{(RESET)}$ = 6 V			1	μA
PG terminal							
Minimum input voltage for valid PG			$I_{(PG)}$ = 300 μA, $V_{(PG1)}$ ≤ 0.8 V		1.0	1.3	V
Trip threshold voltage			V_O decreasing	92%	95%	98%	V_O
Hysteresis voltage			Measured at V_O		0.5%		V_O
$t_{r(PG1)}$			Rising edge deglitch		30		μs
Output low voltage			V_I = 2.7 V, $I_{(PG)}$ = 1 mA		0.15	0.4	V
Leakage current			$V_{(PG1)}$ = 6 V			1	μA
EN terminal							
High-level $\overline{EN}$ input voltage				2			V
Low-level $\overline{EN}$ input voltage						0.7	V
Input current ($\overline{EN}$)				−1		1	μA

NOTES: 1. Minimum input operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum input voltage = 6 V, minimum output current is 1 mA.

2. If V_O < 1.8 V then V_{Imax} = 6 V, V_{Imin} = 2.7 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

If V_O > 2.5 V then V_{Imax} = 6 V, V_{Imin} = V_O + 1 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\right)\right)}{100} \times 1000$$

3. I_O = 1 mA to 1 A for regulator 1 and 1 mA to 2 A for regulator 2.

electrical characteristics over recommended operating junction temperature (T_J = −55°C to 125°C) V_{IN1} or V_{IN2} = $V_{OUTX(nom)}$ + 1 V, I_{OUTX} = 1 mA, $\overline{EN}$ = 0, C_{OUT1} = 22 µF, C_{OUT2} = 47 µF(unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SEQ TERMINAL					
High-level SEQ input voltage		2			V
Low-level SEQ input voltage				0.7	V
SEQ pullup current source			6		µA
MR1 / MR2 TERMINALS					
High-level input voltage		2			V
Low-level input voltage				0.7	V
Pullup current source			9.5		µA
V_{OUT2} TERMINAL					
V_{OUT2} UV comparator − positive-going input threshold voltage of V_{OUT1} UV comparator		80% V_O	83% V_O	86% V_O	V
V_{OUT2} UV comparator − hysteresis			3% V_O		mV
V_{OUT2} UV comparator − falling edge deglitch	V_{SENSE2} decreasing below threshold		140		µs
Peak output current	2 ms pulse width		3		A
Discharge transistor current	V_{OUT2} = 1.5 V		7.5		mA
V_{OUT1} TERMINAL					
V_{OUT1} UV comparator − positive-going input threshold voltage of V_{OUT1} UV comparator		80% V_O	83% V_O	86% V_O	V
V_{OUT1} UV comparator − hysteresis			3% V_O		mV
V_{OUT1} UV comparator − falling edge deglitch	V_{SENSE1} decreasing below threshold		140		µs
Dropout voltage (see Note 4)	I_O = 1 A, V_{IN1} = 3.2 V, T_J = 25°C		160		mV
	I_O = 1 A, V_{IN1} = 3.2 V			255	
Peak output current	2 ms pulse width		1.2		A
Discharge transistor current	V_{OUT1} = 1.5 V		7.5		mA
V_{IN1} / V_{IN2} TERMINAL					
UVLO threshold		2.3		2.65	V
UVLO hysteresis			110		mV

NOTE 4: Input voltage(V_{IN1} or V_{IN2}) = V_O(Typ) − 100 mV. For the 1.5-V, 1.8-V and 2.5-V regulators, the dropout voltage is limited by input voltage range. The 3.3 V regulator input voltage is set to 3.2 V to perform this test.

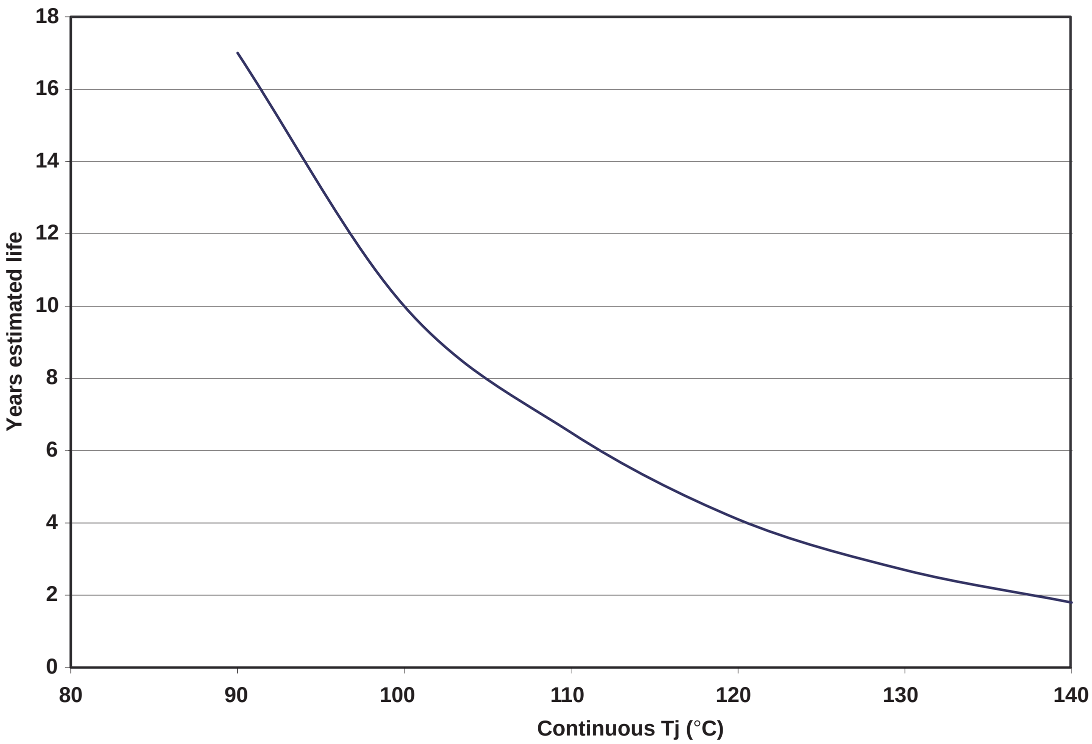


Figure 1. TPS70345-PWP-EP Estimated Device Life at Elevated Temperature Wirebond Voiding Fail Modes

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Output spectral noise density	vs Frequency	2 − 5
z_O	Output impedance	vs Frequency	6 − 9
	Load transient response		10, 11
	Line transient response		12, 13
V_O	Output voltage and enable voltage	vs Time (start-up)	14, 15
	Equivalent series resistance	vs Output current	16 − 20

TYPICAL CHARACTERISTICS

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

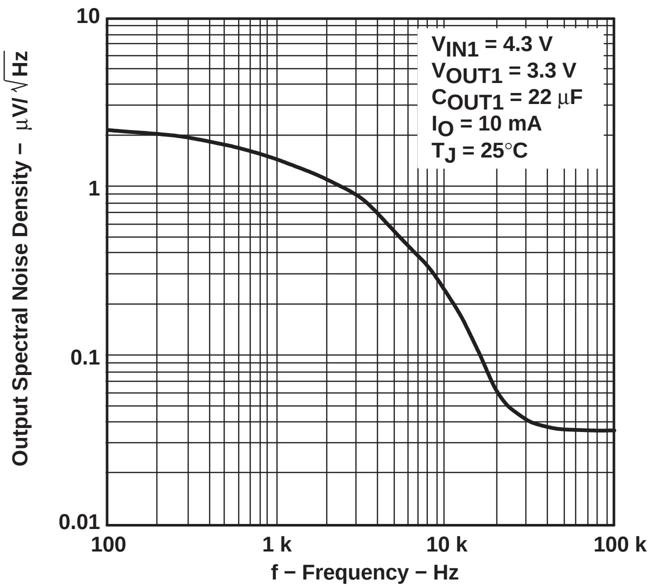


Figure 2

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

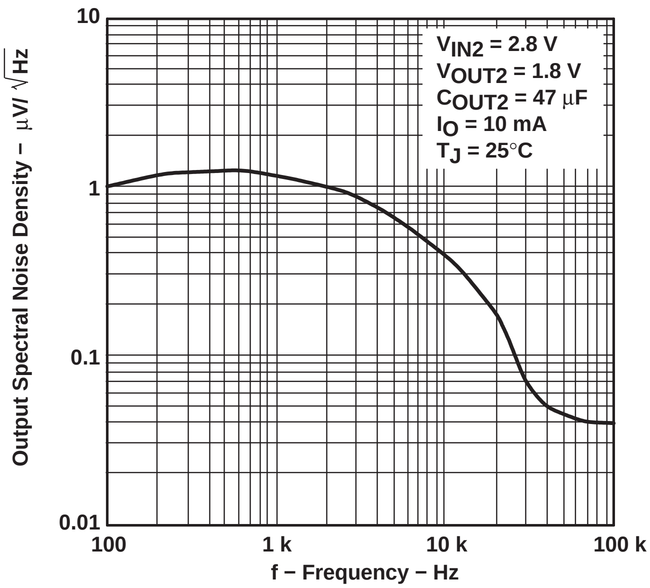


Figure 3

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

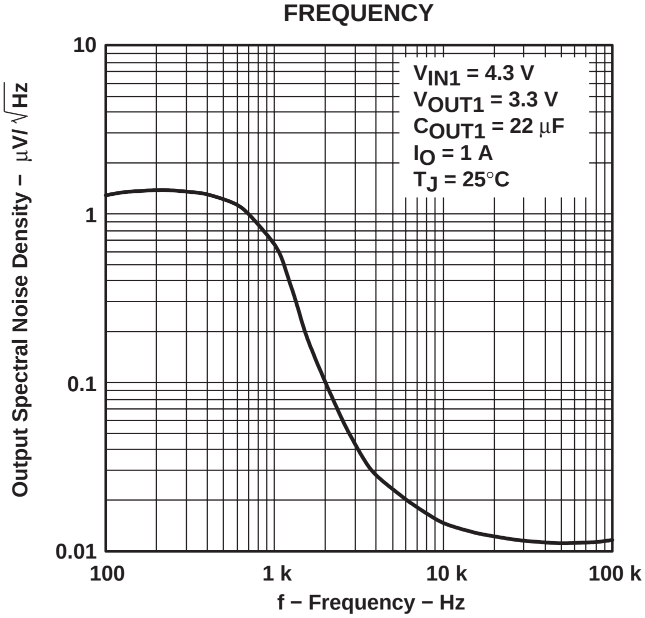


Figure 4

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

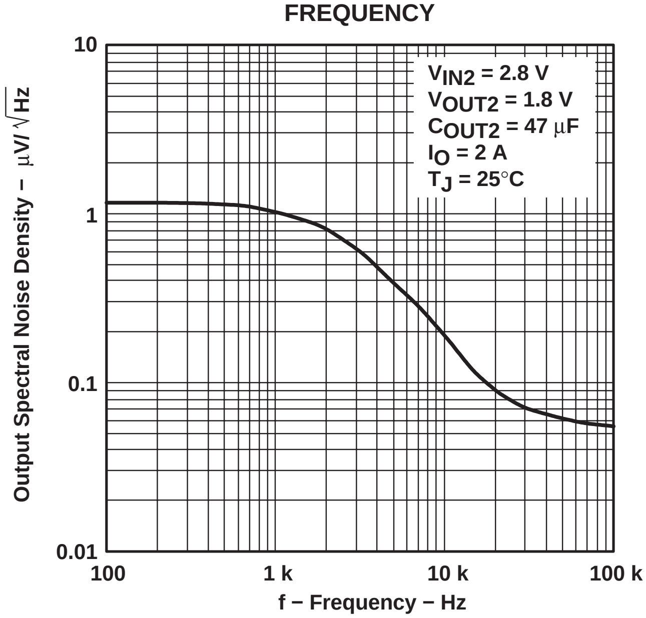


Figure 5

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

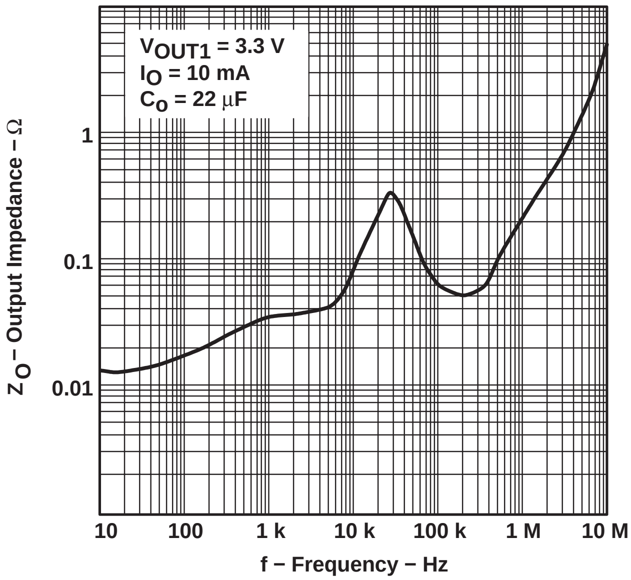


Figure 6

OUTPUT IMPEDANCE vs FREQUENCY

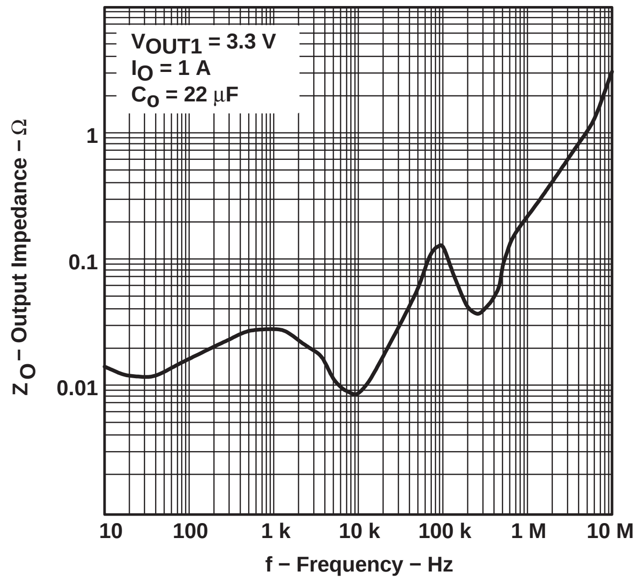


Figure 7

OUTPUT IMPEDANCE vs FREQUENCY

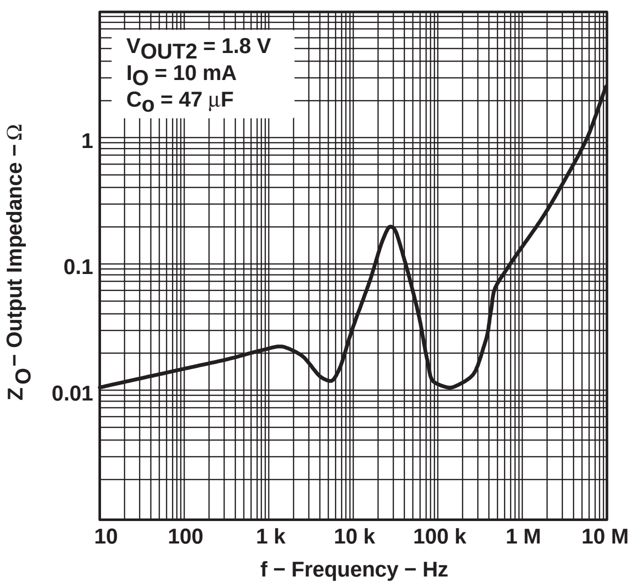


Figure 8

OUTPUT IMPEDANCE vs FREQUENCY

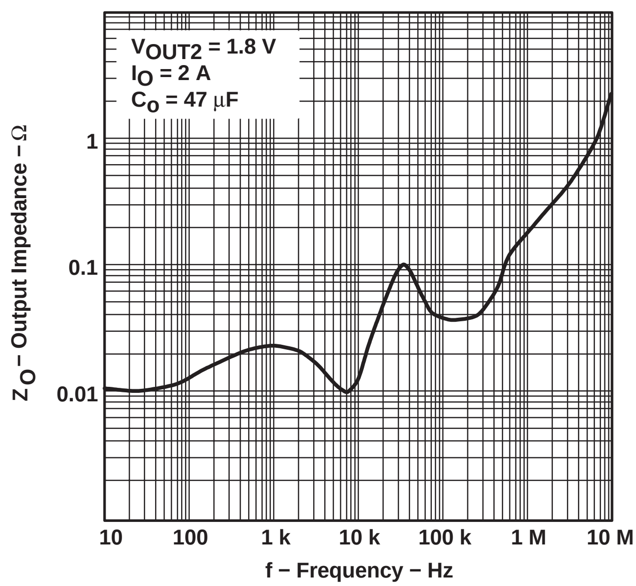


Figure 9

TYPICAL CHARACTERISTICS

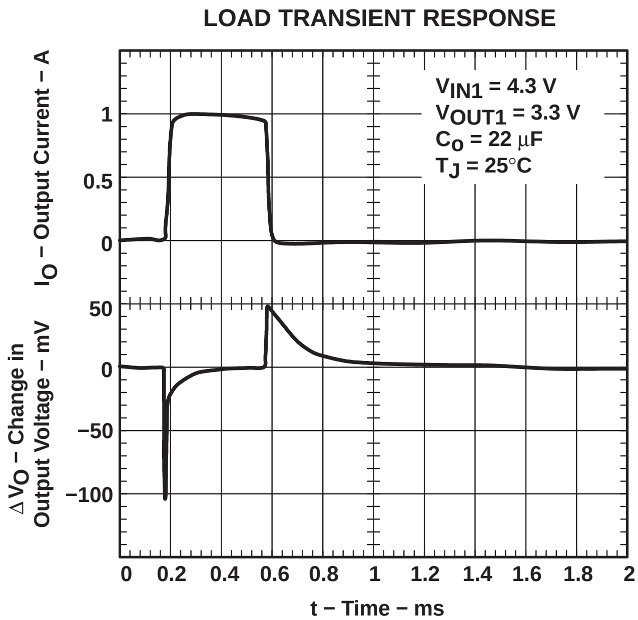


Figure 10

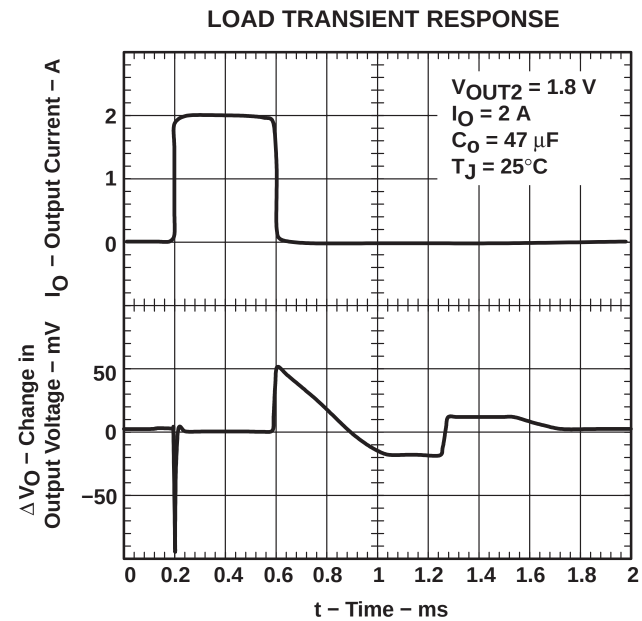


Figure 11

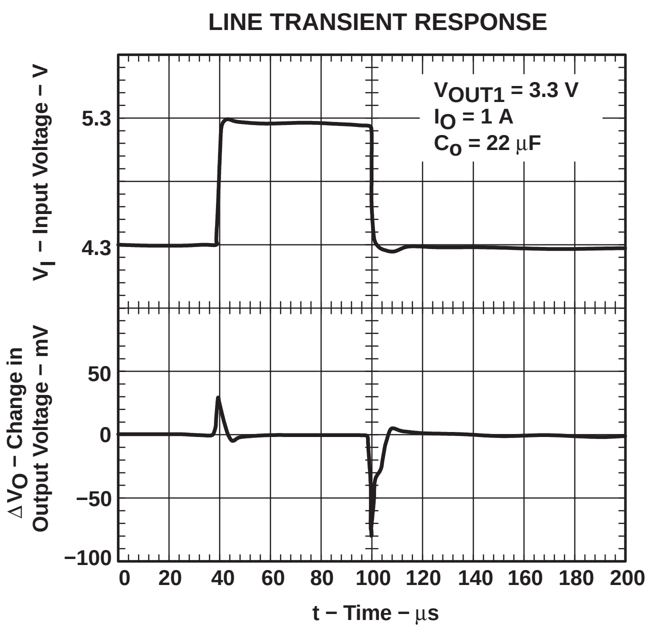


Figure 12

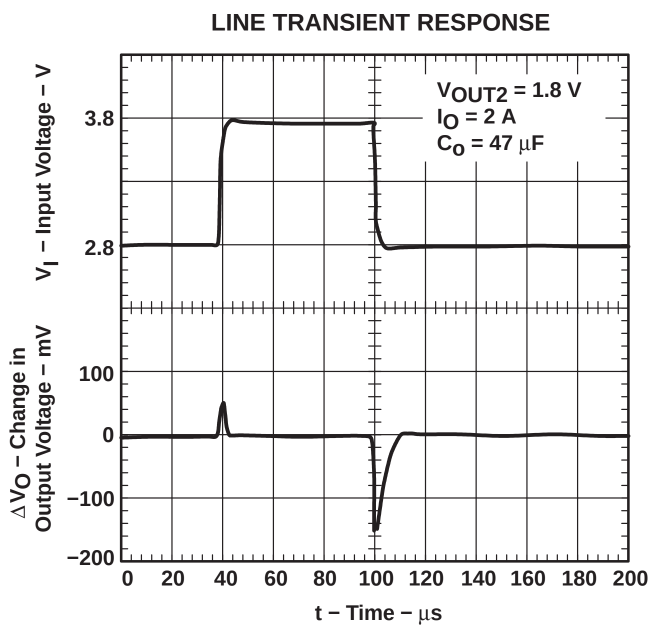


Figure 13

TYPICAL CHARACTERISTICS

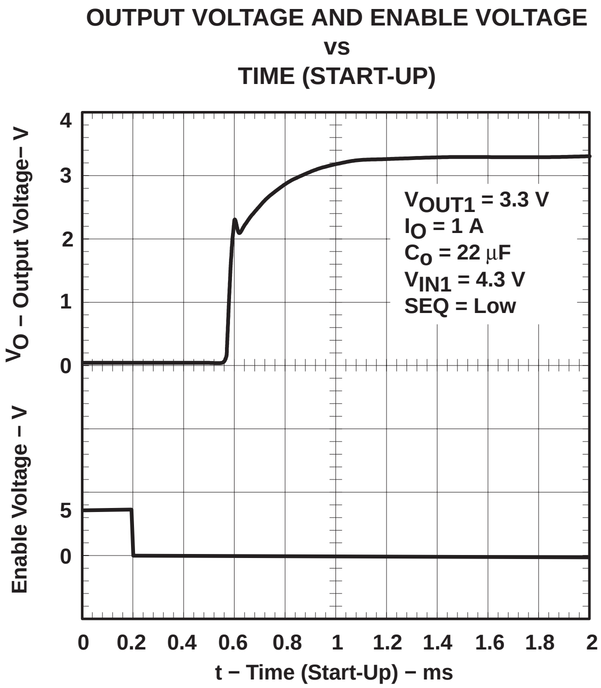


Figure 14

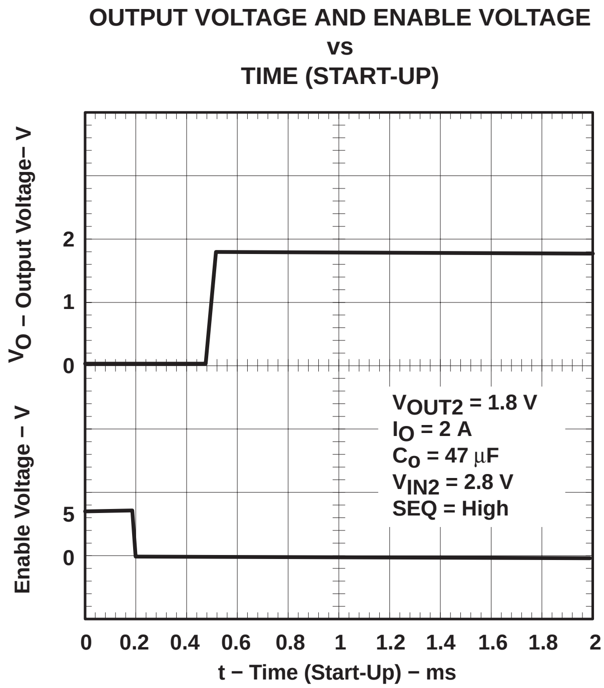


Figure 15

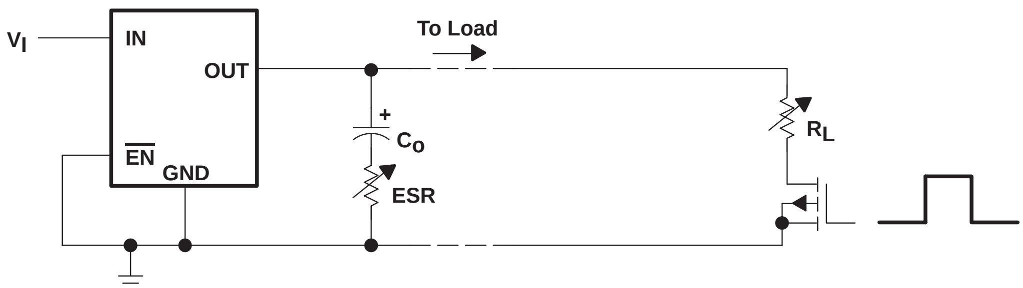


Figure 16. Test Circuit for Typical Regions of Stability

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)†
vs
OUTPUT CURRENT

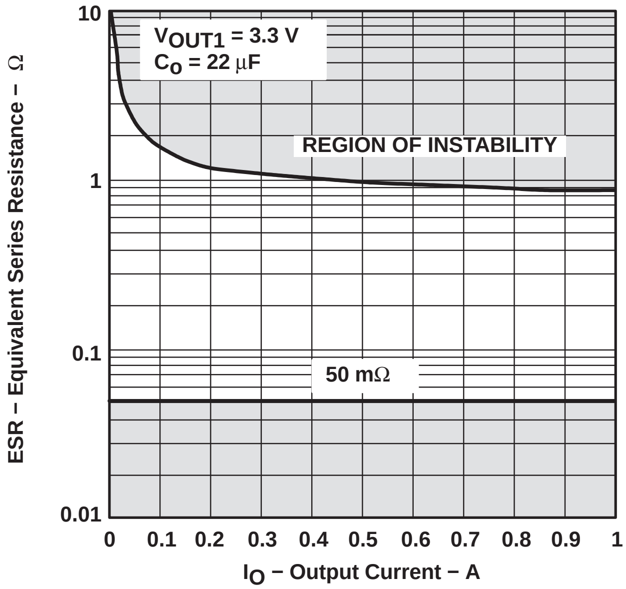


Figure 17

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)†
vs
OUTPUT CURRENT

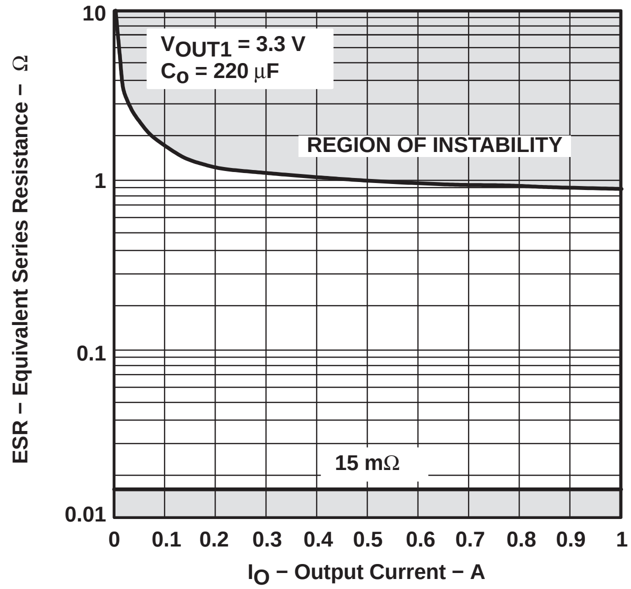


Figure 18

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)†
vs
OUTPUT CURRENT

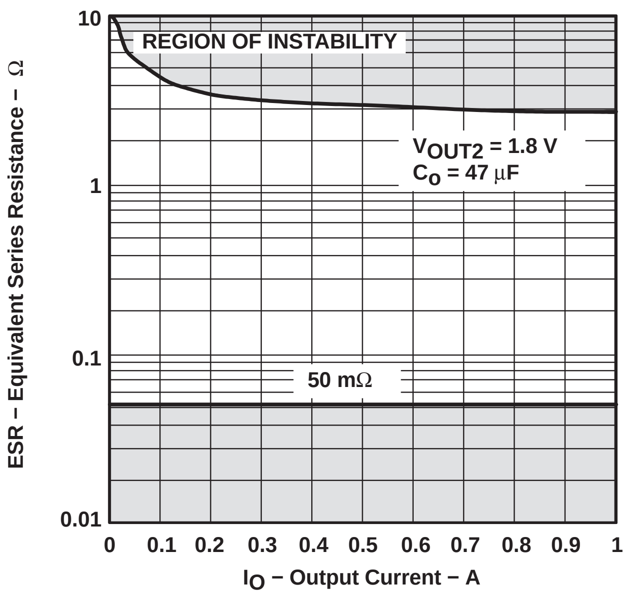


Figure 19

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)†
vs
OUTPUT CURRENT

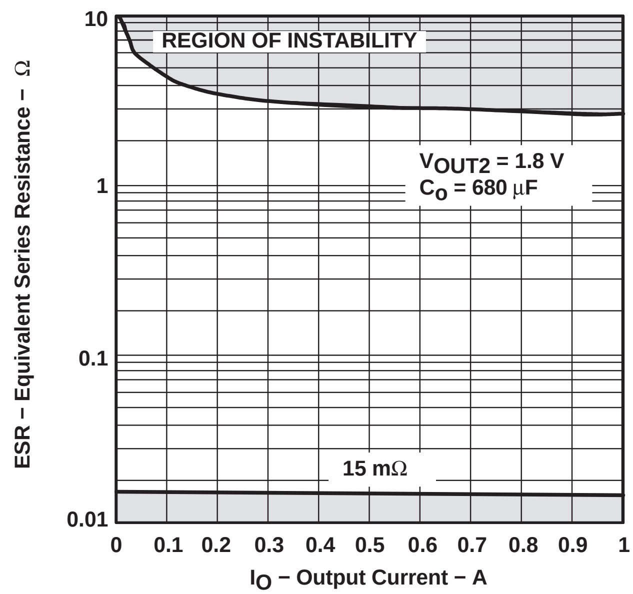


Figure 20

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

THERMAL INFORMATION

thermally enhanced TSSOP-24 (PWP − PowerPad™)

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 21(c)] to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

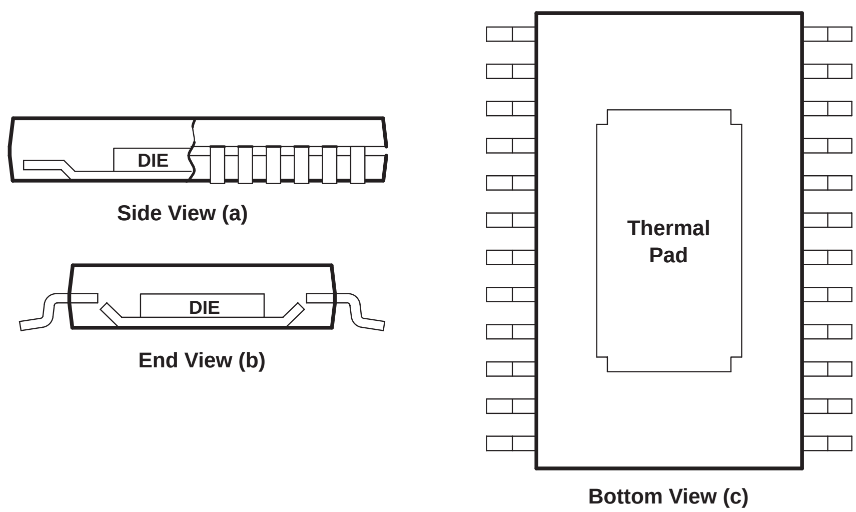


Figure 21. Views of Thermally Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 23(a), 8 cm^2 of copper heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figure 22 and Figure 23). The line drawn at 0.3 cm^2 in Figure 22 and Figure 23 indicates performance at the minimum recommended heat-sink size, illustrated in Figure 24.

THERMAL INFORMATION

thermally enhanced TSSOP-24 (PWP − PowerPad™) (continued)

The thermal pad is directly connected to the substrate of the IC, which for the TPS70345 series is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWP can be a ground plane or left electrically isolated. In TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 24 independent leads that can be used as inputs and outputs (Note: leads 1, 12, 13, and 24 are internally connected to the thermal pad and the IC substrate).

THERMAL RESISTANCE
vs
COPPER HEAT-SINK AREA

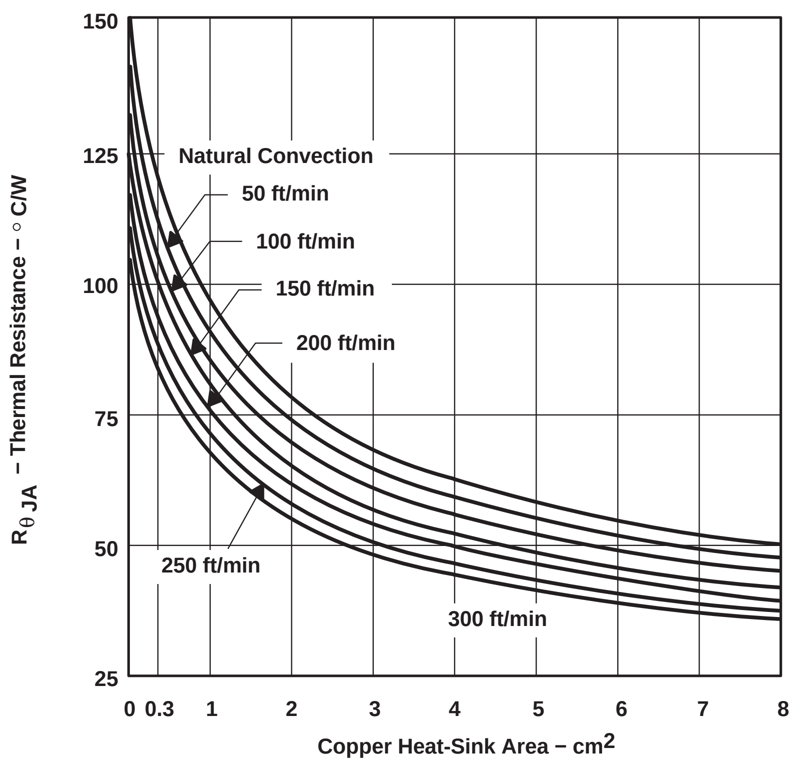


Figure 22

THERMAL INFORMATION

thermally enhanced TSSOP-24 (PWP − PowerPad™) (continued)

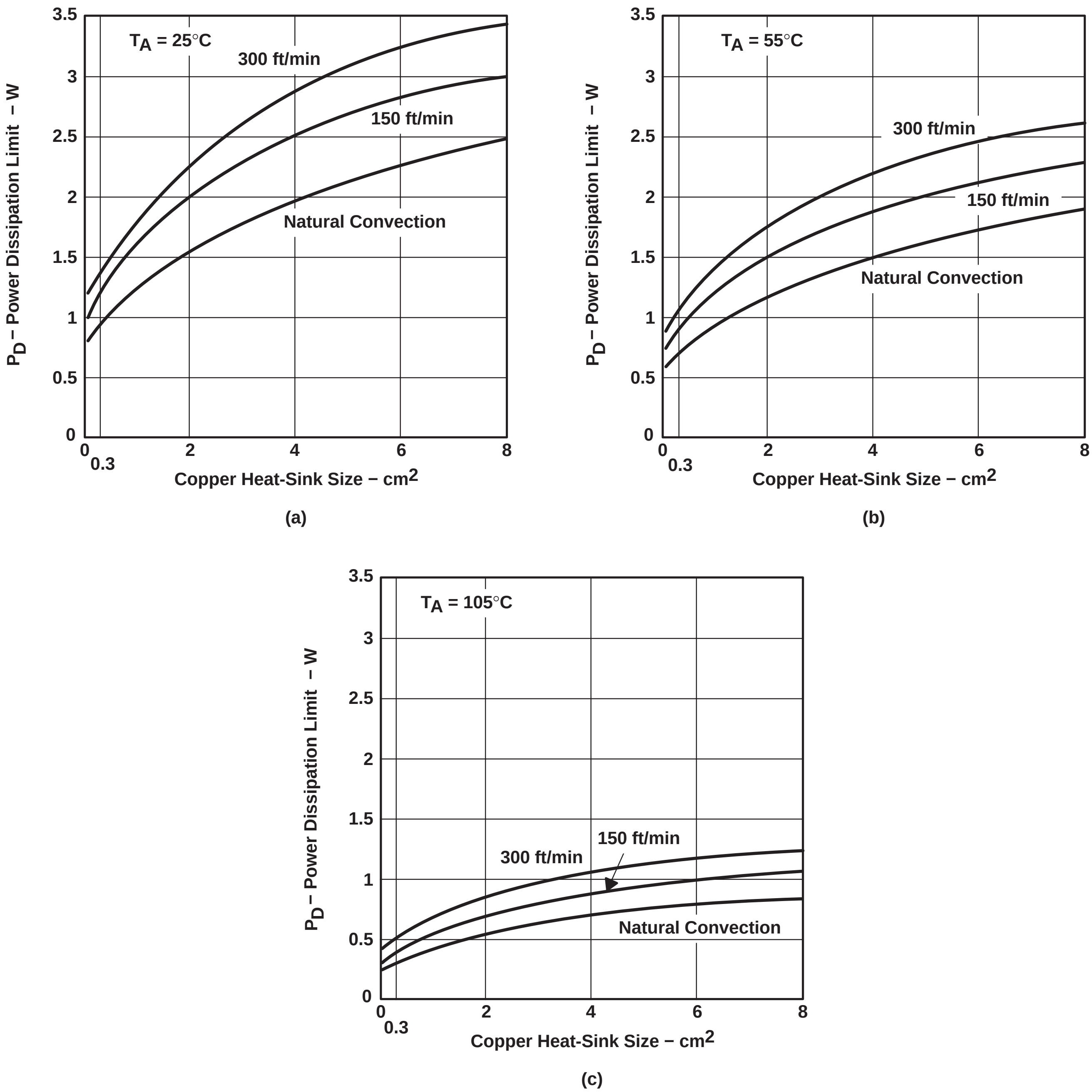
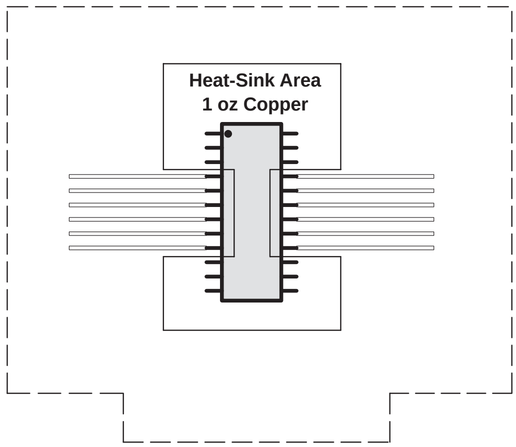


Figure 23. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

THERMAL INFORMATION

thermally enhanced TSSOP-24 (PWP − PowerPad™) (continued)

Figure 24 is an example of a thermally enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figure 22 and Figure 23. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 22 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.



Board thickness	62 mils
Board size	3.2 in. × 3.2 in.
Board material	FR4
Copper trace/heat sink	1 oz
Exposed pad mounting	63/67 tin/lead solder

Figure 24. PWB Layout (Including Copper Heatsink Area) for Thermally Enhanced PWP Package

From Figure 22, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA(system)}} \tag{1}$$

where

$T_J$max is the maximum specified junction temperature (150°C absolute maximum limit, 125°C recommended operating limit) and T_A is the ambient temperature.

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS70345 regulator. The equation for calculating total internal power dissipation of the TPS70345 is:

$$P_{D(total)} = \left(V_{IN1} - V_{OUT1}\right) \times I_{OUT1} + V_{IN1} \times \frac{I_Q}{2} + \left(V_{IN2} - V_{OUT2}\right) \times I_{OUT2} + V_{IN2} \times \frac{I_Q}{2} \tag{2}$$

Since the quiescent current of the TPS703xx is low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_{IN1} - V_{OUT1}\right) \times I_{OUT1} + \left(V_{IN2} - V_{OUT2}\right) \times I_{OUT2} \tag{3}$$

For the case where T_A = 55°C, airflow = 200 ft/min, copper heat-sink area = 4 cm^2, the maximum power-dissipation limit can be calculated. First, from Figure 22, we find the system $R_{\theta JA}$ is 50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA(system)}} = \frac{125^{\circ}C - 55^{\circ}C}{TBD\ ^{\circ}C/W} = TBD\ W \tag{4}$$

THERMAL INFORMATION

thermally enhanced TSSOP-24 (PWP − PowerPad™) (continued)

If the system implements a TPS70345 regulator, where V_I = 5 V and I_O = 800 mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_{IN1} - V_{OUT1}\right) \times I_{OUT1} + \left(V_{IN2} - V_{OUT2}\right) \times I_{OUT2} \qquad (5)$$

$$= (4.3 - 3.3) \times 0.8 + (2.8 - 1.8) \times 1 = 1.8\ \text{W}$$

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters. This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 2 oz. copper traces on 4-in × 4-in ground layer. Simultaneous and continuous operation of both regulator outputs at full load may exceed the power dissipation rating of the PWP package.

mounting information

The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figure 22 and Figure 23 is for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 25 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 12, 13, and 24.

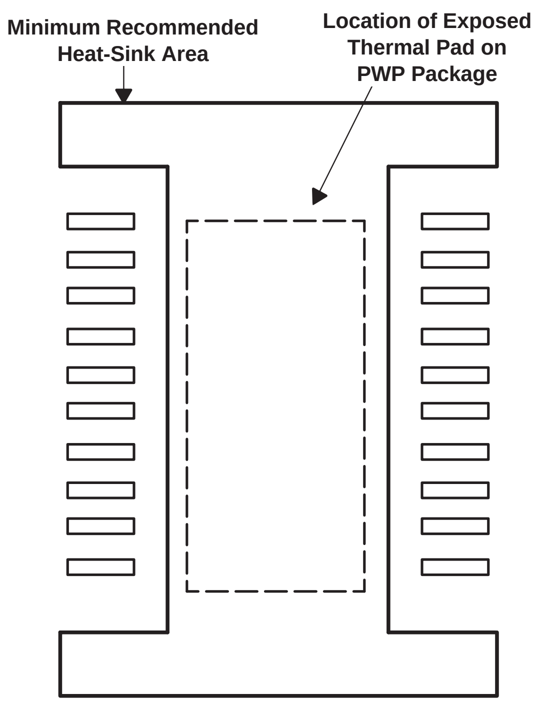


Figure 25. PWP Package Land Pattern

APPLICATION INFORMATION

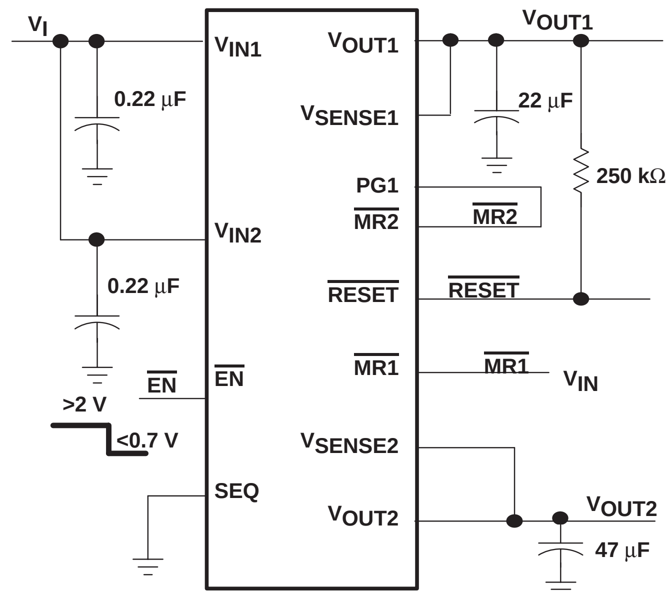
sequencing timing diagrams

The following figures provide a timing diagram of how this device functions in different configurations.

application conditions not shown in block diagram:

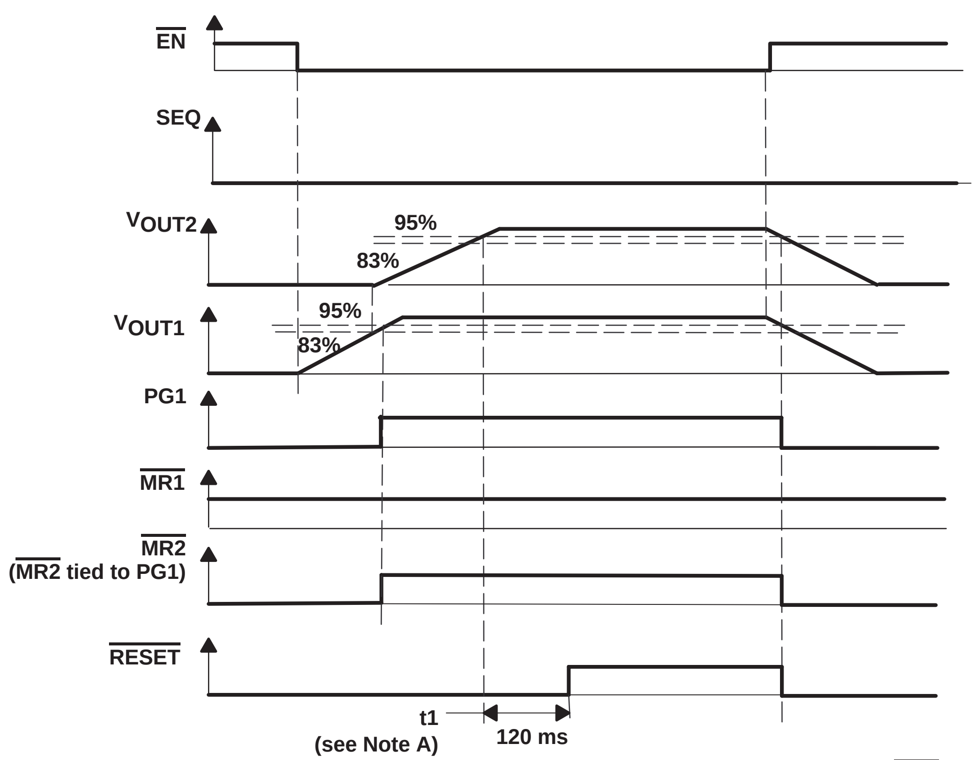
V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic low; PG1 is tied to $\overline{\text{MR2}}$; $\overline{\text{MR1}}$ is not used and is connected to V_{IN}.

TPS70345PWP
(Fixed Output Option)



explanation of timing diagrams:

$\overline{\text{EN}}$ is initially high; therefore, both regulators are off and PG1 and $\overline{\text{RESET}}$ are at logic low. With SEQ at logic low, when $\overline{\text{EN}}$ is taken to logic low, V_{OUT1} turns on. V_{OUT2} turns on after V_{OUT1} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{\text{MR2}}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{\text{MR1}}$ and $\overline{\text{MR2}}$ (tied to PG1) are at logic high, $\overline{\text{RESET}}$ is pulled to logic high after a 120 ms delay. When $\overline{\text{EN}}$ is returned to logic high, both devices power down and both PG1 (tied to $\overline{\text{MR2}}$) and $\overline{\text{RESET}}$ return to logic low.



NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{\text{MR1}}$ is logic high.

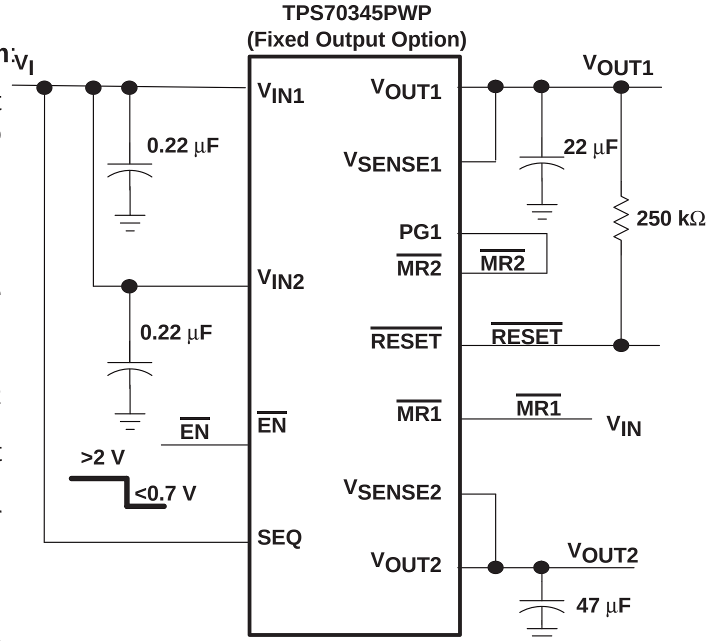
Figure 26. Timing When SEQ = Low

APPLICATION INFORMATION

sequencing timing diagrams (continued)

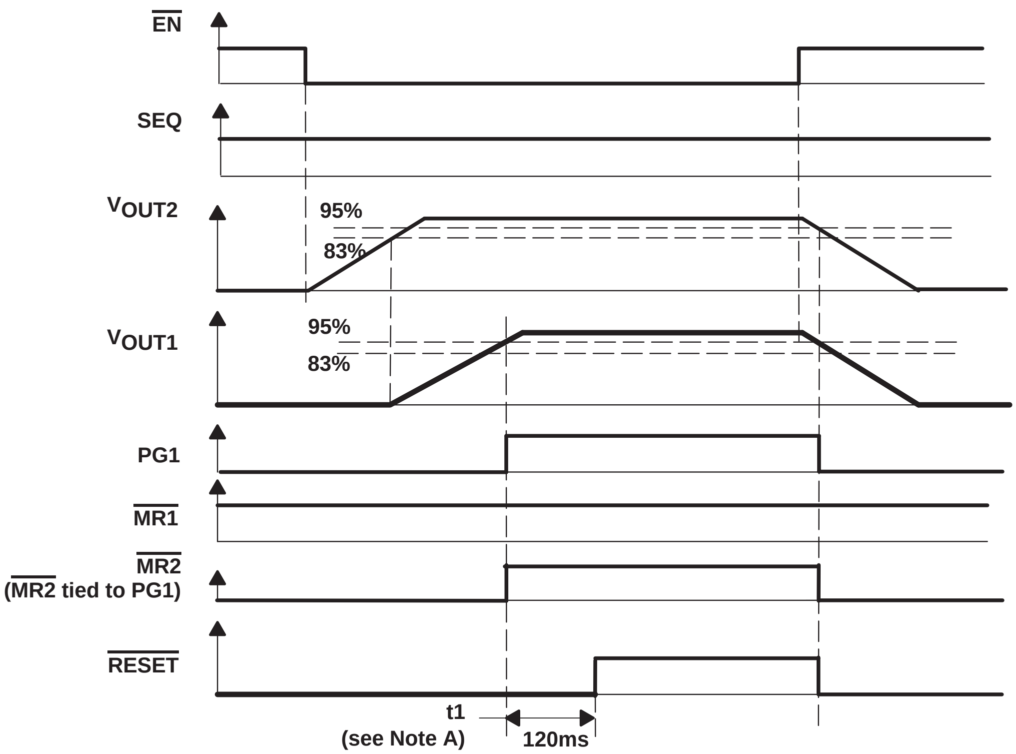
application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is not used and is connected to V_{IN}.



explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken to logic low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When $\overline{EN}$ is returned to logic high, both devices turn off and both PG1 (tied to $\overline{MR2}$) and $\overline{RESET}$ return to logic low.



NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

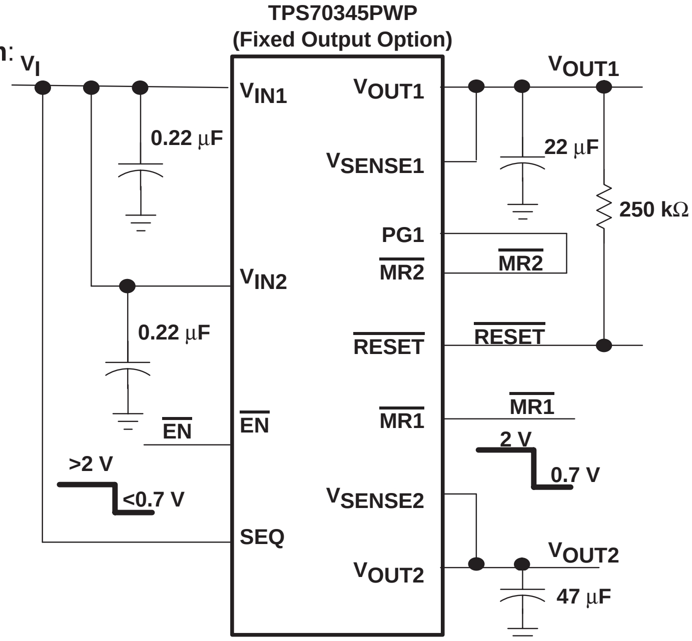
Figure 27. Timing When SEQ = High

APPLICATION INFORMATION

sequencing timing diagrams (continued)

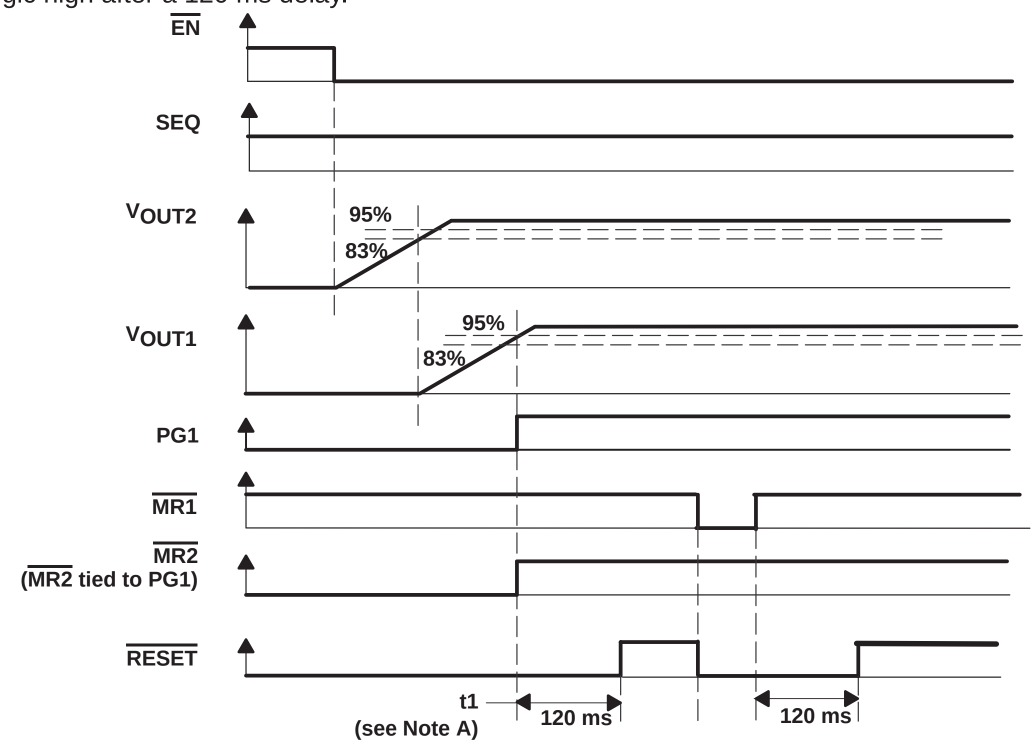
application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is initially at logic high but is eventually toggled.



explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When $\overline{MR1}$ is taken low, $\overline{RESET}$ returns to logic low but the outputs remain in regulation. When $\overline{MR1}$ is returned to logic high, since both V_{OUT1} and V_{OUT2} remain above 95% of their respective regulated output voltages and $\overline{MR2}$ (tied to PG1) remains at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay.



NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

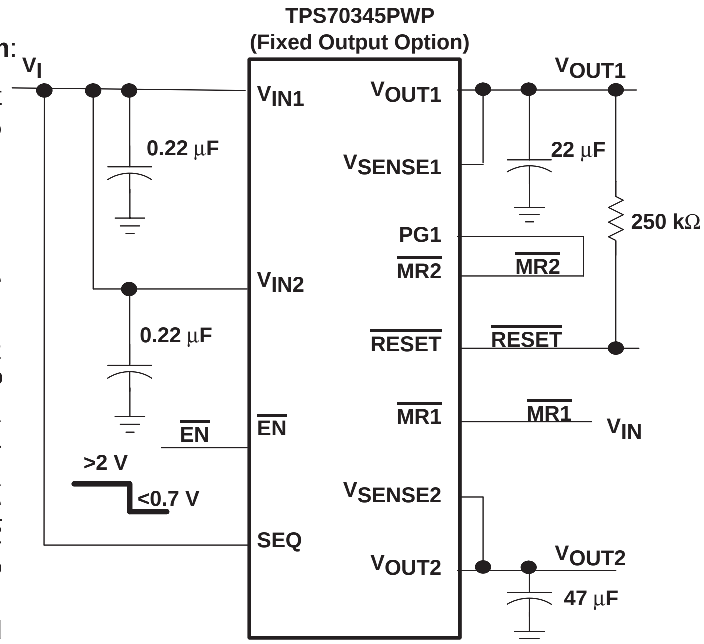
Figure 28. Timing When $\overline{MR1}$ Is Toggled

APPLICATION INFORMATION

sequencing timing diagrams (continued)

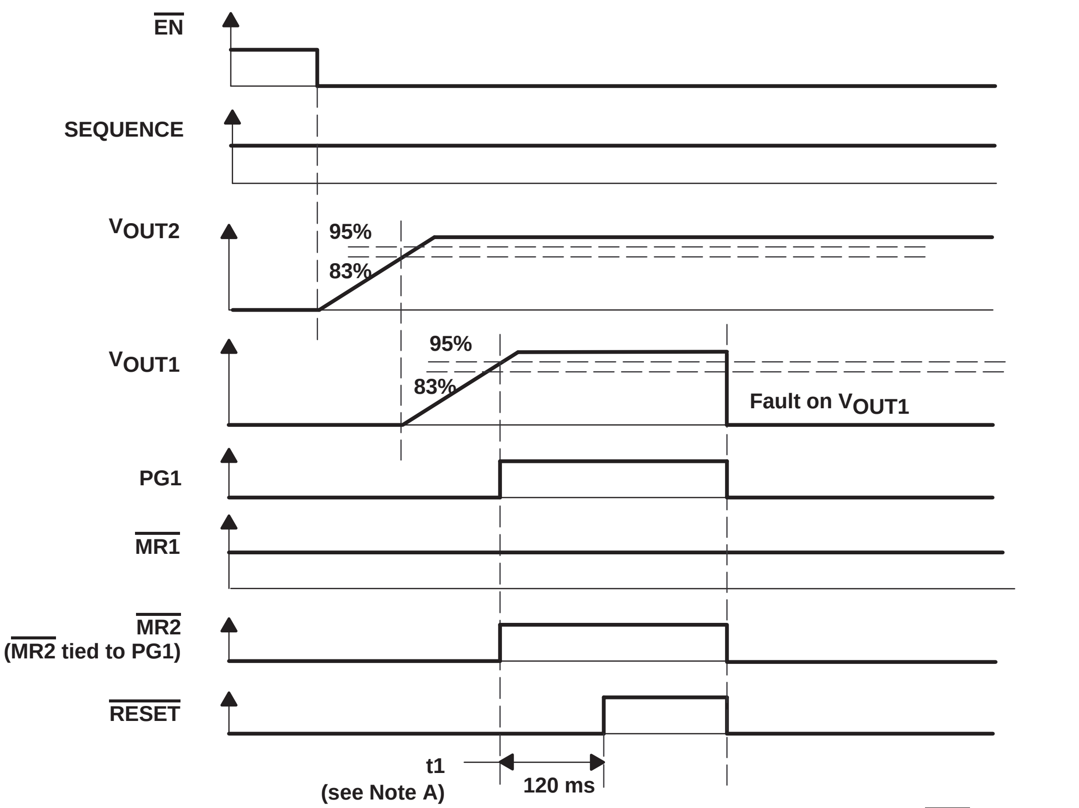
application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{\text{MR2}}$; $\overline{\text{MR1}}$ is not used and is connected to V_{IN}.



explanation of timing diagrams:

$\overline{\text{EN}}$ is initially high; therefore, both regulators are off and PG1 and $\overline{\text{RESET}}$ are at logic low. With SEQ at logic high, when $\overline{\text{EN}}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{\text{MR2}}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{\text{MR1}}$ and $\overline{\text{MR2}}$ (tied to PG1) are at logic high, $\overline{\text{RESET}}$ is pulled to logic high after a 120 ms delay. When a fault on V_{OUT1} causes it to fall below 95% of its regulated output voltage, PG1 (tied to $\overline{\text{MR2}}$) goes to logic low.



NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{\text{MR1}}$ is logic high.

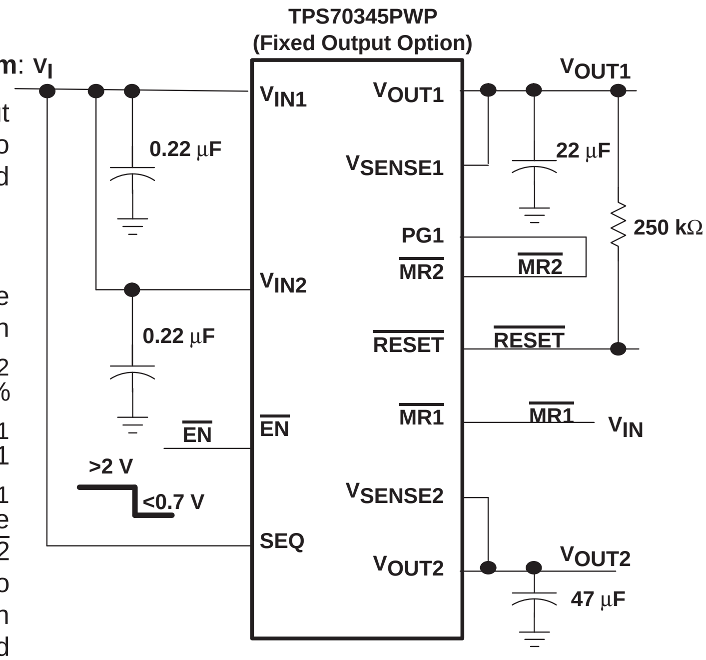
Figure 29. Timing When a Fault Occurs on V_{OUT1}

APPLICATION INFORMATION

sequencing timing diagrams (continued)

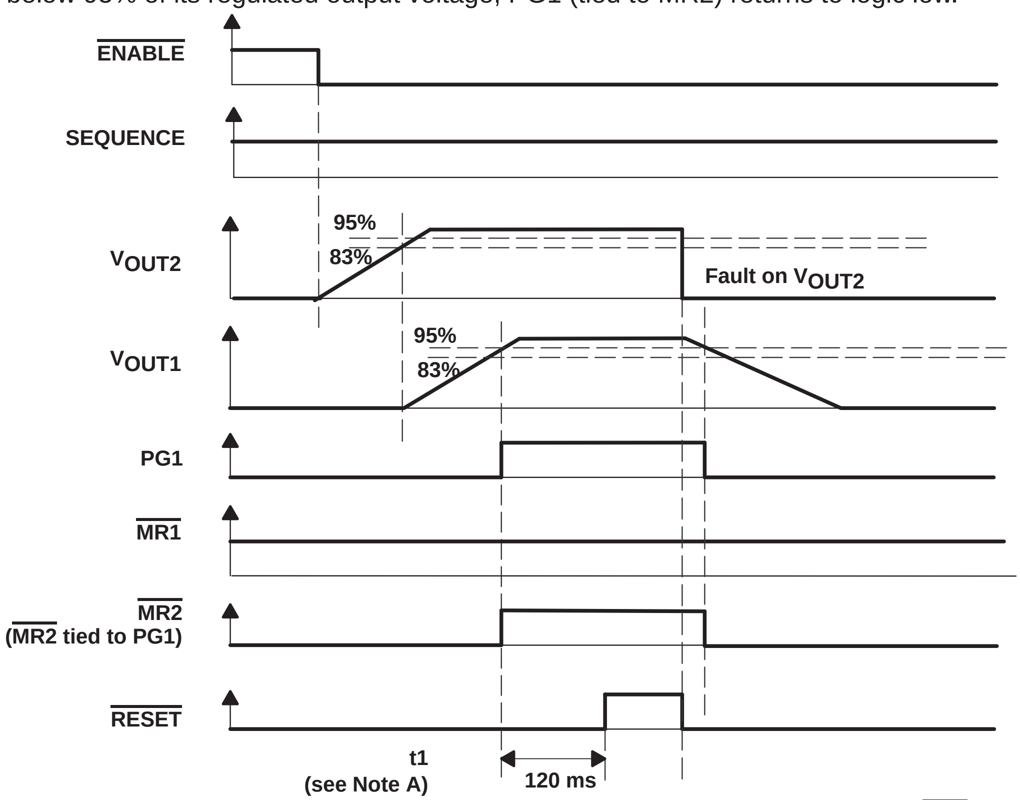
application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is not used and is connected to V_{IN}.



explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When a fault on V_{OUT2} causes it to fall below 95% of its regulated output voltage, $\overline{RESET}$ returns to logic low and V_{OUT1} begins to power down because SEQ is high. When V_{OUT1} falls below 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) returns to logic low.



NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 30. Timing When a Fault Occurs on V_{OUT2}

APPLICATION INFORMATION

input capacitor

For a typical application, a ceramic input bypass capacitor (0.22 μF − 1 μF) is recommended to ensure device stability. This capacitor should be as close as possible to the input pin. Due to the impedance of the input supply, large transient currents causes the input voltage to droop. If this droop causes the input voltage to drop below the UVLO threshold, the device turns off. Therefore, it is recommended that a larger capacitor be placed in parallel with the ceramic bypass capacitor at the regulator's input. The size of this capacitor depends on the output current, response time of the main power supply, and the main power supply's distance to the regulator. At a minimum, the capacitor should be sized to ensure that the input voltage does not drop below the minimum UVLO threshold voltage during normal operating conditions.

output capacitor

As with most LDO regulators, the TPS70345 requires an output capacitor connected between each OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value for V_{OUT1} is 22 μF and the ESR (equivalent series resistance) must be between 50 mΩ and 800 mΩ. The minimum recommended capacitance value for V_{OUT2} is 47 μF and the ESR must be between 50 mΩ and 2 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. Below is a partial listing of surface-mount capacitors usable with the TPS70345 for fast transient response application.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

VALUE	MFR.	PART NO.
680 μF	Kemet	T510X6871004AS
470 μF	Sanyo	4TPB470M
150 μF	Sanyo	4TPC150M
220 μF	Sanyo	2R5TPC220M
100 μF	Sanyo	6TPC100M
68 μF	Sanyo	10TPC68M
68 μF	Kemet	T495D6861006AS
47 μF	Kemet	T495D4761010AS
33 μF	Kemet	T495C3361016AS
22 μF	Kemet	T495C2261010AS

regulator protection

Both TPS70345 PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS70345 also features internal current limiting and thermal protection. During normal operation, the TPS70345 regulator 1 limits output current to approximately 1.75 A (typ) and regulator 2 limits output current to approximately 3.8 A (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS70345MPWPREP	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	T70345MEP
TPS70345MPWPREP.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	T70345MEP
V62/06616-01XE	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	T70345MEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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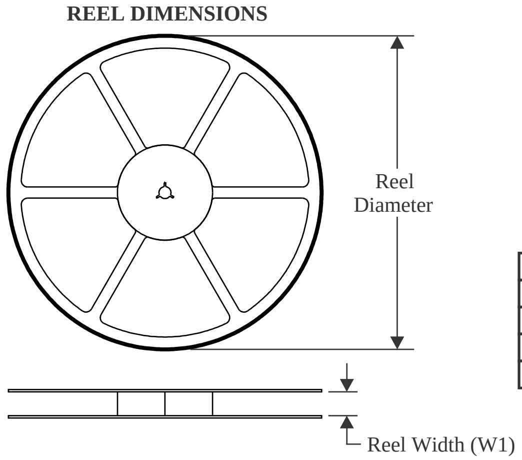
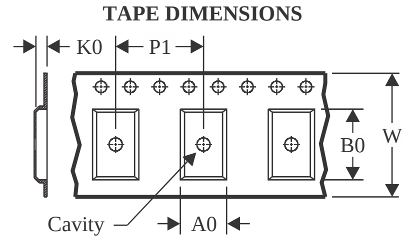
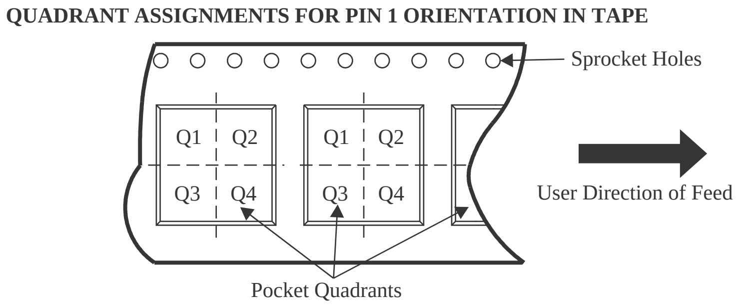
TAPE AND REEL INFORMATION





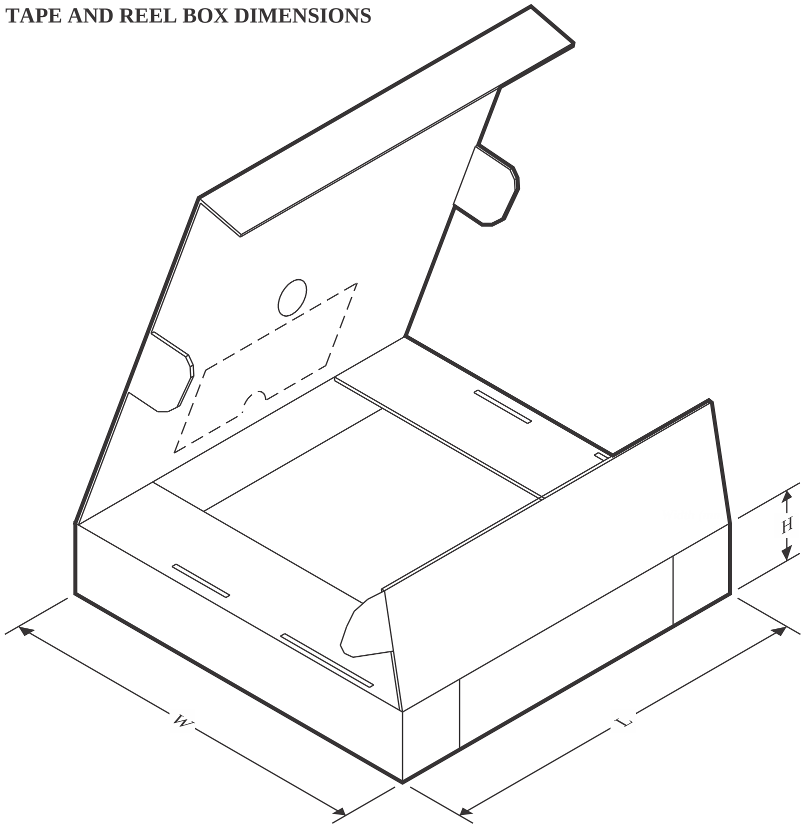
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70345MPWPREP	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70345MPWPREP	HTSSOP	PWP	24	2000	350.0	350.0	43.0

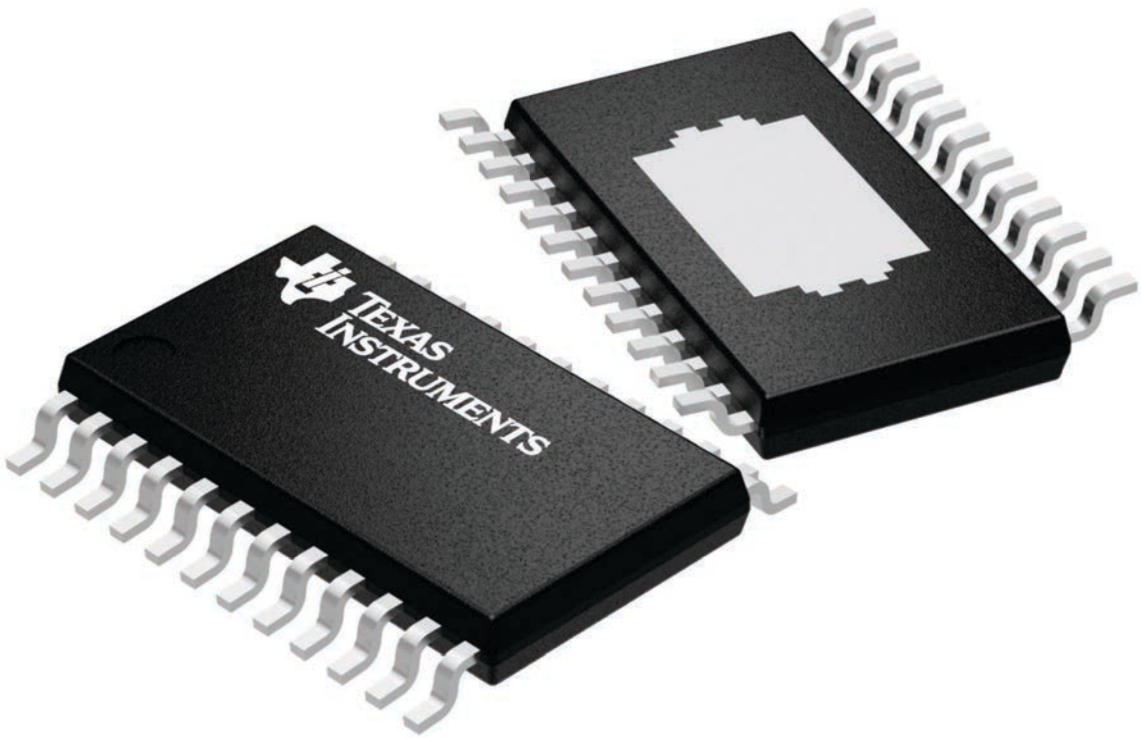
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

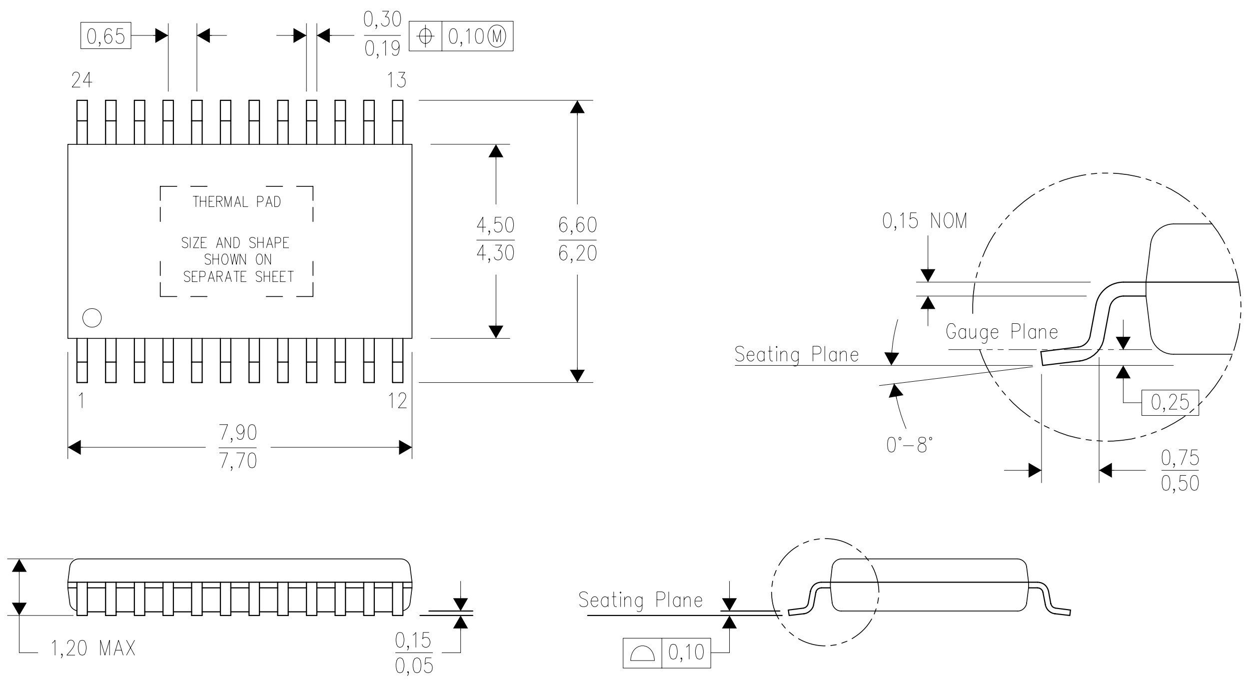
4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



4073225–5/I 05/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

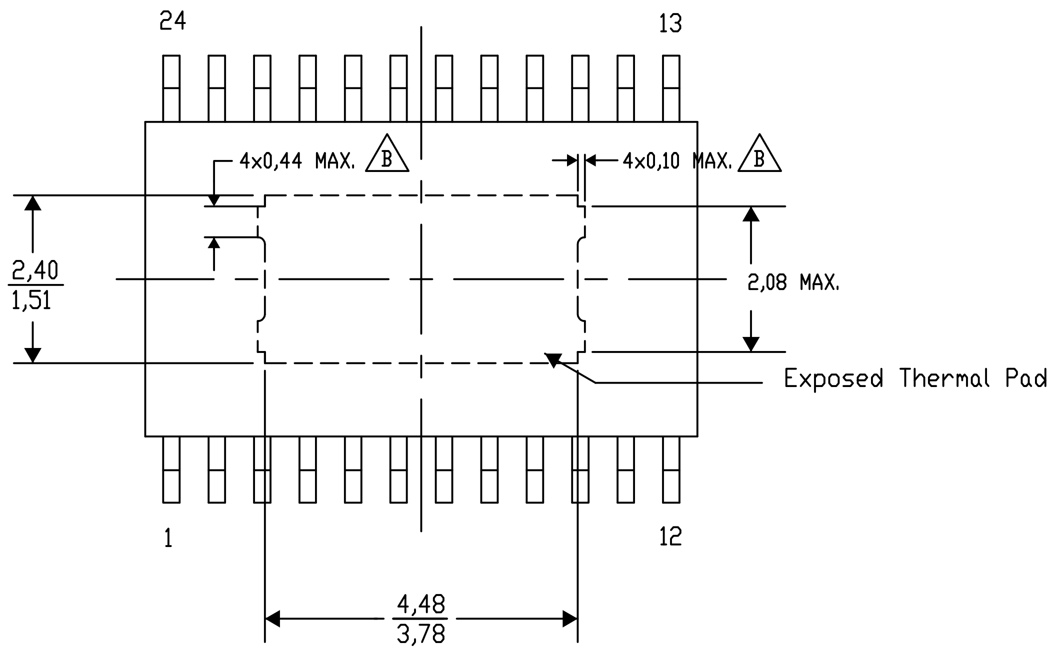
PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

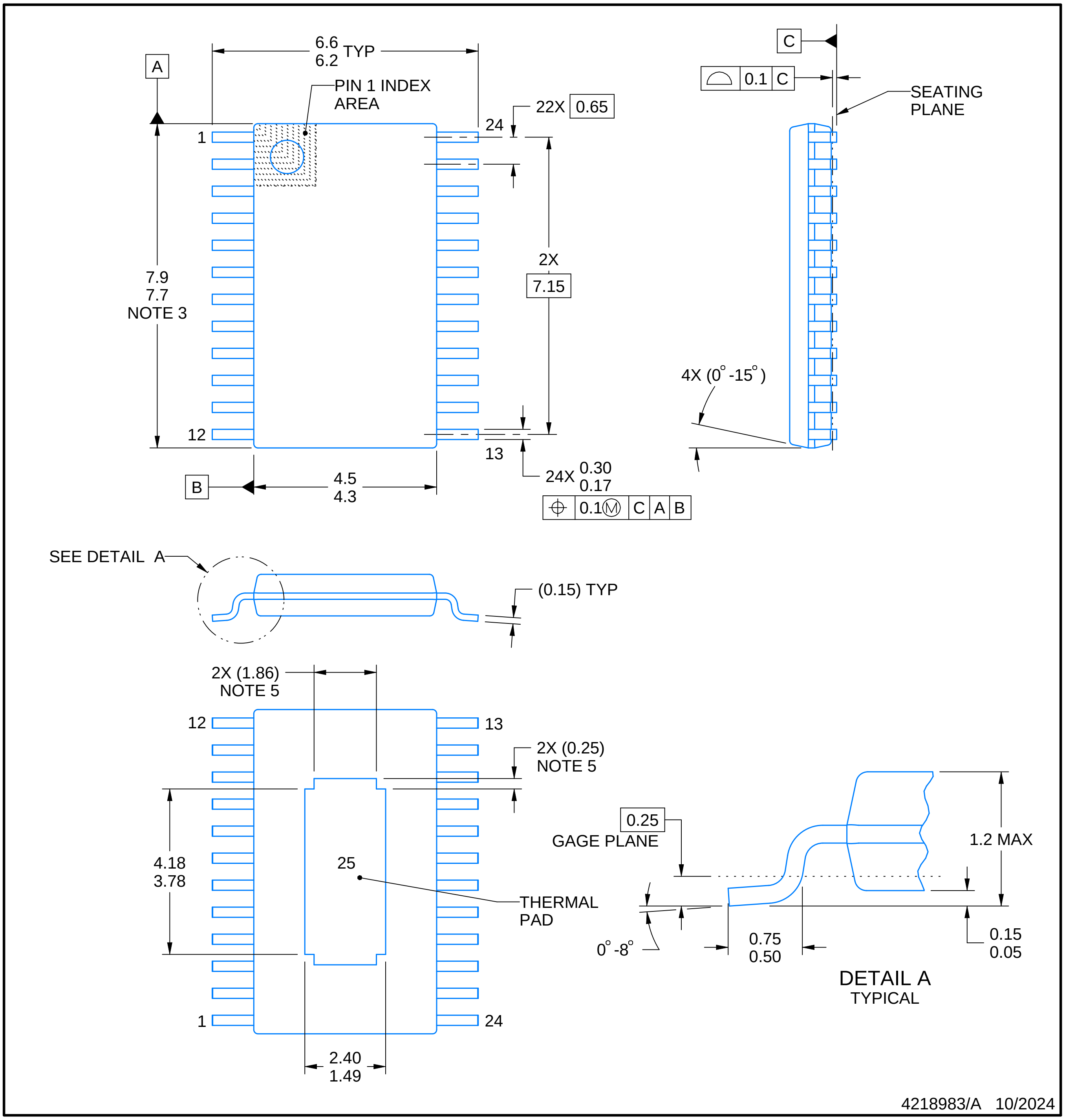
Exposed Thermal Pad Dimensions

4206332-42/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments



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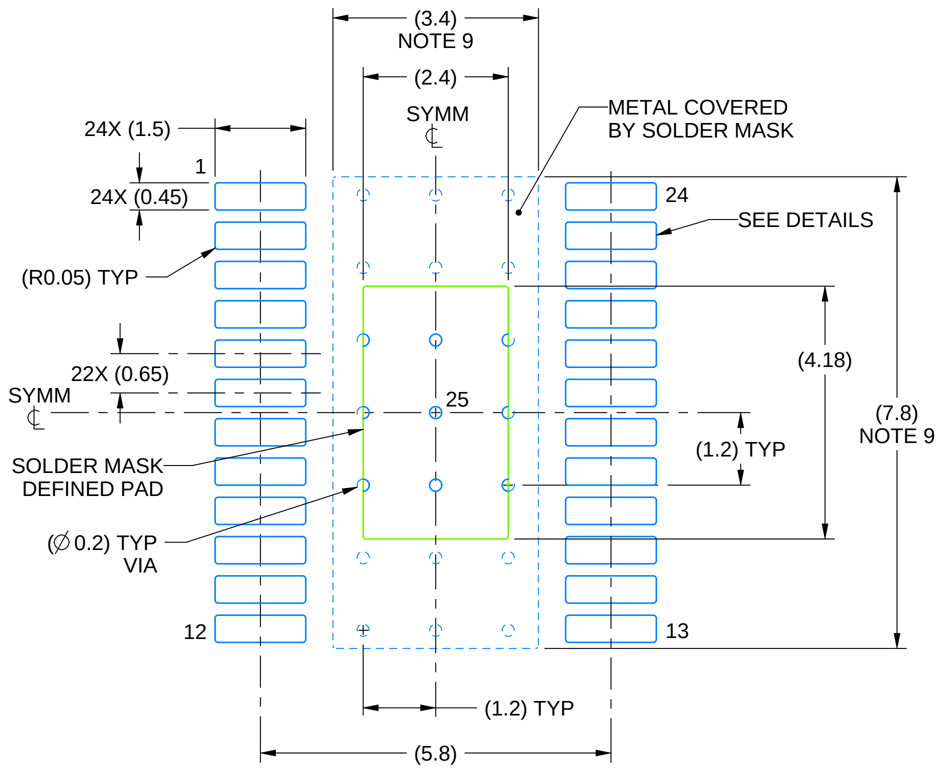
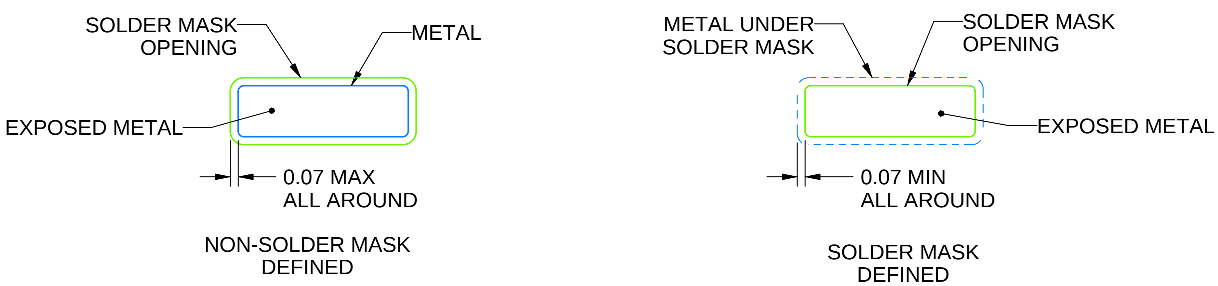
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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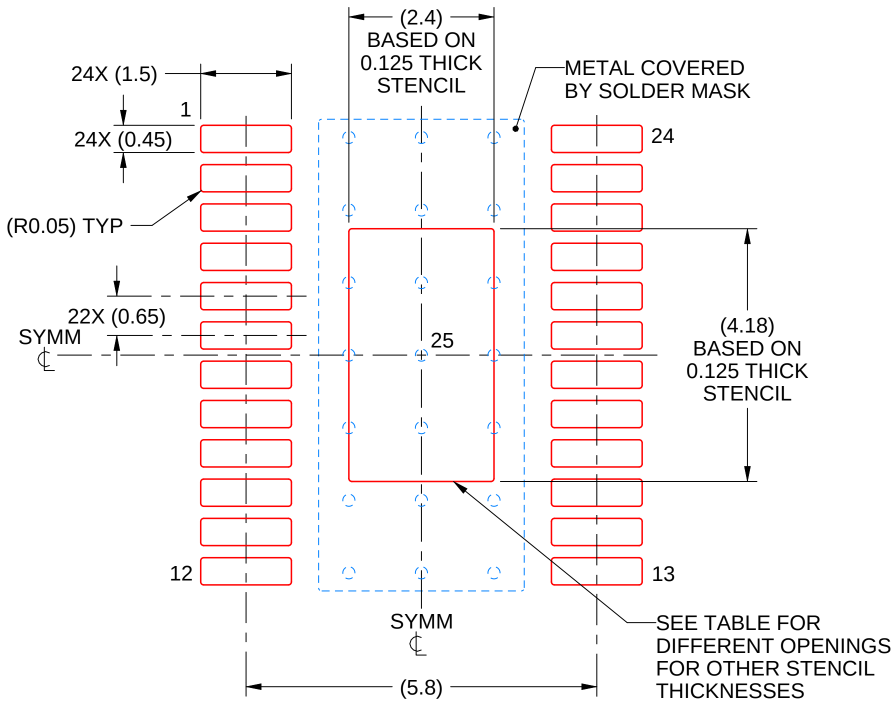
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 4.67
0.125	2.40 X 4.18 (SHOWN)
0.15	2.19 X 3.82
0.175	2.03 X 3.53

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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