TPS65313-Q1 VIN 範囲の広い車載アプリケーション向けのパワー・マネージメント IC

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃、T_A
- ASIL-C (ISO 26262)/SIL-2 (IEC 61508) に準じたシステム・レベルの機能安全性要件に対応
- 同期整流降圧プリレギュレータ (BUCK1)
  - 4V～36V の入力電圧範囲
  - 最大 3.1A の出力電流
  - 工場で選択可能な出力電圧:3.3V または 3.6V
- 同期整流降圧レギュレータ (BUCK2)
  - 固定入力電圧:3.3V または 3.6V
  - 最大 2A の出力電流
  - 工場で選択可能な出力電圧:1.2V、1.25V、1.8V、または 2.3V
- 同期整流昇圧コンバータ (BOOST)
  - 3.3V または 3.6V の固定入力電圧
  - 最大 600mA の出力電流
  - 5V の出力電圧
- フェーズ・ロック・ループ (PLL)
  - 2.2MHz 前後の出力周波数
  - SYNC_IN ピンで変調または非変調の外部クロックをサポート
- すべてのレギュレータ用
  - ソフトスタート機能
  - 独立した電圧監視と診断機能
  - 過電流、過負荷、過電圧、低電圧、熱保護
  - ループ補償内蔵
- レギュレータのスイッチング・クロック用に適応型ランダム化スペクトラム拡散 (ARSS) 変調を内蔵
- OFF 状態の静止電流 3μA
- SPI による制御および診断
- 2 つの汎用外部電圧モニタ
- MCU または DSP 用の Q&A ウォッチドッグおよびリセット・スーパバイザを内蔵
- 熱的に強化された 40 ピン、0.5mm ピッチの VQFNP パッケージ

2 アプリケーション

- 車載用レーダーおよびカメラ・アプリケーション
- 車載用センサ・フュージョン・アプリケーション
- 産業用レーダー・アプリケーション
- ビルディングおよびファクトリ・オートメーション・アプリケーション

3 概要

TPS65313-Q1 デバイスは電力管理 IC (PMIC)で、MCU 制御または DSP 制御の車載用、工業用、機械、または輸送システムの要件を満たしています。このデバイスには一般的に使用される機能が統合されているため、基板面積とシステムのコストを削減するのに役立ちます。™

このデバイスには、1 つの VIN 範囲が広い同期整流降圧レギュレータ (BUCK1)、1 つの低電圧 (LV) 降圧レギュレータ (BUCK2)、および VIN 範囲の広い降圧レギュレータ (BUCK1) から給電される 1 つの昇圧コンバータ (BOOST) が搭載されています。このデバイスは、OFF 状態の静止電流が小さいのが特長で、システムが恒久的に電源に接続されている場合、消費電流が減少します。すべての出力は、過電圧、過負荷、過熱状態から保護されています。

製品情報

部品番号	パッケージ (1) (2)	本体サイズ (公称)
TPS65313-Q1	VQFNP (40)	6.00mm × 6.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) 2 ビットの 16 進数のデバイス構成値は、DEV_ID レジスタにマップされます。

4 デバイスの機能ブロック図

機能ブロック図

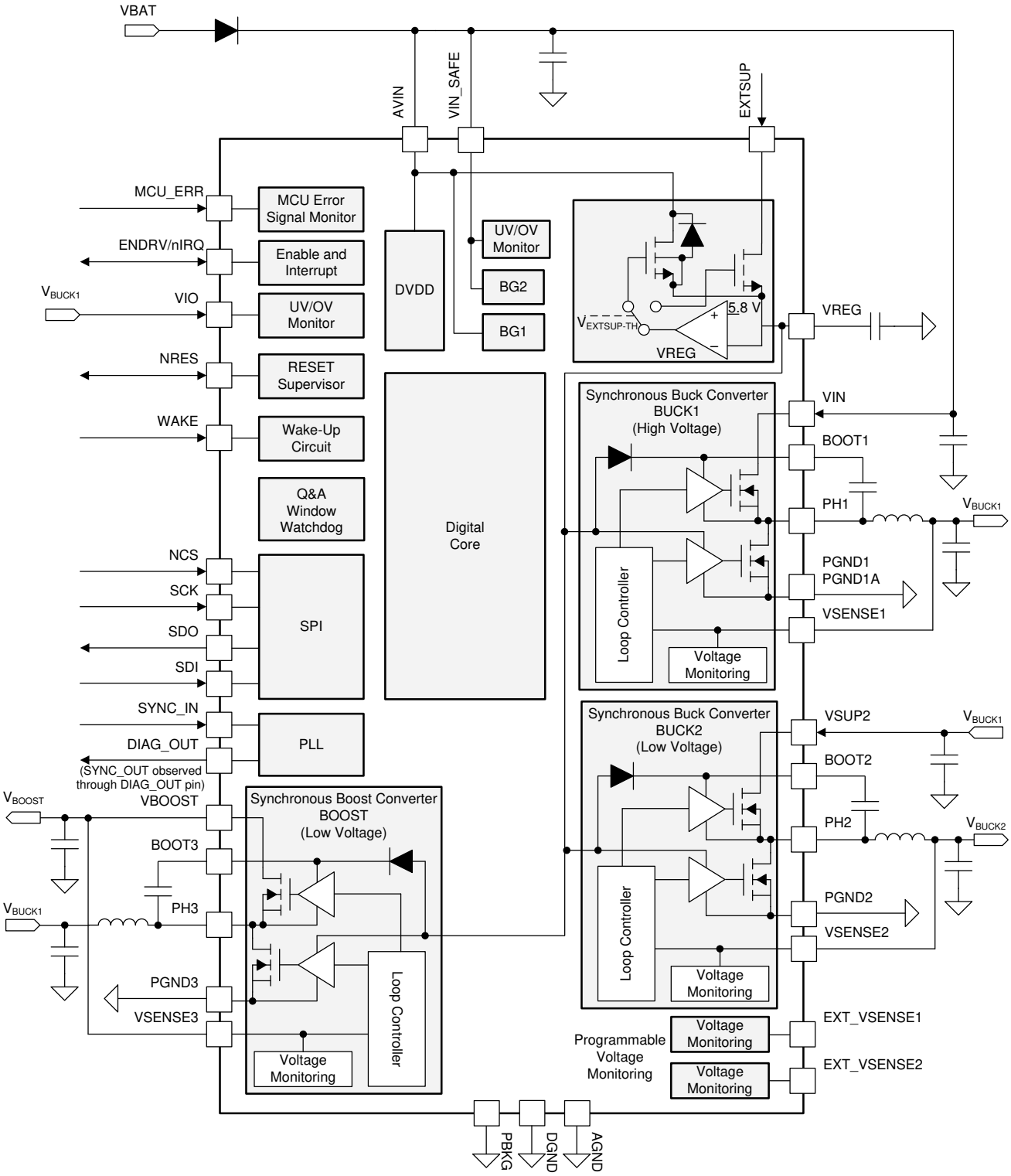

図 4-1. デバイスの機能ブロック図

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5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (March 2020) to Revision C (October 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Deleted digital system clock monitor slow clock error detection and fast clock error detection specification	14
• Added note to 図 11-4	38
• Updated text	45
• Added table note to 表 11-2	48
• Added more information to this topic to more clearly explain the ABIST function	53
• Updated WD_ANSWER_RESP_0 to WD_ANSWER_RESP_1 in 図 11-17	72
• Updated content in 表 11-10	74
• Changed "inversion enabled" to "inversion not enabled" to reflect the actual device operation	94
• Added descriptive information to the setting EE_CRC_ERR bit in SAFETY_ERR_STAT1 during EEPROM CRC diagnostic test run	95

- Changed "inversion enabled" to "inversion not enabled" to reflect the actual device operation 95
- Updated 図 11-34 100
- Changed "inversion enabled" to "inversion not enabled" to reflect the actual device operation 109
- Added note to SAFETY_CLK_STAT Register Field Descriptions table..... 113
- Added note to SAFETY_LBIST_CTRL Register Field Descriptions..... 113

Changes from Revision A (September 2018) to Revision B (March 2020) **Page**

- データシートの最初の公開リリース..... 1

6 概要 (続き)

独立の監視および保護機能を持つ、すべてのレギュレートされる電源出力は、ASIL-C/SIL-2 のシステム・レベル機能安全性要件に対応できます。潜在的なフォルトを防止するための必須およびプログラム可能診断機能 (アナログおよびロジックの組み込み自己テスト) も含まれています。 デバイスにはプログラム可能なスーパバイザ、ウォッチドッグ機能、MCU または DSP のエラー・ピン監視機能も内蔵されています。

7 Device Option Table

OPTION VALUE (1)	BUCK1	BUCK2	f_{SW} MODULATION	EXT_VMON1 ENABLED AT POWER-UP	EXT_VMON2 ENABLED AT POWER-UP	DEFAULT NRES EXTENSION DELAY
For device 2-bit hexadecimal option value and configuration setting refer to device Technical Reference Manual (TRM)	3.6 V and 3.3 V	1.2 V, 1.25 V, 1.8 V, and 2.3 V	Internal and External	YES and NO	YES and NO	LONG and SHORT

(1) 2-bit hexadecimal device configuration value is mapped to the DEV_ID register.

8 Pin Configuration and Functions

図 8-1 shows the 40-pin RWG Plastic Quad Flatpack - No Lead Outline.

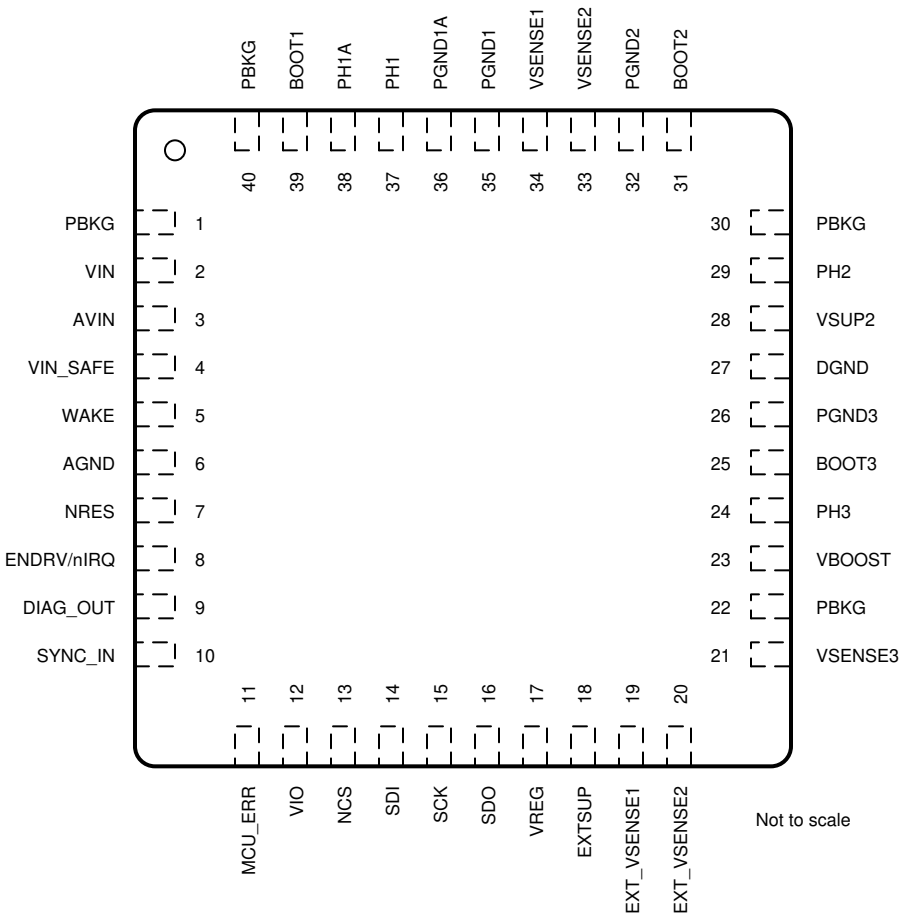


図 8-1. 40-Pin RWG VQFNP (Top View)

表 8-1. Pin Attributes

PIN(1)		TYPE	DESCRIPTION
NO.	NAME		
1	PBKG	GND	Die substrate. Connect this pin to the system ground.
22			
30			
40			
2	VIN	PWR	Supply input for the BUCK1.
3	AVIN	PWR	Supply input for the internal reference and supply-rail generations for the output voltage regulations.
4	VIN_SAFE	I	Supply input for monitoring circuits.
5	WAKE	I	Wake-up input
6	AGND	GND	Analog ground
7	NRES	I/O	Active-low reset output to the system MCU or warm reset input from the system MCU. If pin is not used it can be left open since it has an internal pull up.
8	ENDRV/nIRQ	I/O	Enable drive output for external peripherals or interrupt output for system MCU. If pin is not used it can be left open since it has an internal pull up.
9	DIAG_OUT	O	Diagnostic output (analog MUX and digital MUX output). If pin is not used it can be left open.
10	SYNC_IN	I	PLL input clock. If pin is not used it can be left open since it has an internal pull down.
11	MCU_ERR	I	MCU error-signal input. If pin is not used it can be left open since it has an internal pull down.
12	VIO	PWR	IO supply input for the digital interface pins from and to the system MCU.
13	NCS	I	Active-low SPI pin for the chip-select input. If pin is not used it can be left open since it has an internal pull up.
14	SDI	I	SPI pin for the slave-data input. If pin is not used it can be left open since it has an internal pull down.
15	SCK	I	SPI pin for the clock input. If pin is not used it can be left open since it has an internal pull down.
16	SDO	O	SPI pin for the slave-data output (push-pull output). If this pin is not used, then it can be left open.
17	VREG	O	Internal regulator output for the high-side and low-side gate drivers.
18	EXTSUP	PWR	External low-voltage supply input for the VREG. If pin is not used it has to be connected to GND.
19	EXT_VSENSE1	I	External general-purpose voltage monitor input 1. If pin is not used it has to be connected to GND.
20	EXT_VSENSE2	I	External general-purpose voltage monitor input 2. If pin is not used it has to be connected to GND.
21	VSENSE3	I	BOOST external sense-voltage input
23	VBOOST	PWR	BOOST output
24	PH3	O	Switch node of the BOOST converter
25	BOOT3	I	Bootstrap supply for the BOOST high-side FET driver circuit. A 100-nF capacitor (minimum) is required between the BOOT3 and PH3 pins.
26	PGND3	GND	BOOST power ground
27	DGND	GND	Ground for the digital circuitry
28	VSUP2	PWR	BUCK2 supply input
29	PH2	O	Switch node of the BUCK2 regulator
31	BOOT2	I	Bootstrap supply for the BUCK2 high-side FET driver circuit. A 100-nF capacitor (minimum) is required between the BOOT2 and PH2 pins.
32	PGND2	GND	BUCK2 power ground
33	VSENSE2	I	BUCK2 external sense-voltage input
34	VSENSE1	I	BUCK1 external sense-voltage input
35	PGND1	GND	BUCK1 power ground
36	PGND1A	GND	BUCK1 power ground
37	PH1	O	Switch node of the BUCK1 regulator
38	PH1A	O	Switch node of the BUCK1 regulator
39	BOOT1	I	Bootstrap supply for the BUCK1 high-side FET driver circuit. A 100-nF capacitor (minimum) is required between the BOOT1 and PH1 or the PH1A pins.
—	Thermal Pad	GND	Connect to the thermal pad to the printed circuit board (PCB) ground planes using multiple vias for good thermal performance.

(1) I = input, O = output, I/O = input and output, PWR = power, GND = ground.

9 Specifications

9.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

GROUP	PIN NAME	MIN	MAX	UNIT
Supply Inputs	VIN, AVIN, VIN_SAFE	-0.3	40	V
	VSUP2	-0.3	5.5	V
	VBOOST	-0.3	10	V
	VIO, EXTSUP	-0.3	5.5	V
Wide-VIN BUCK Regulator	BOOT1	-0.3	V_{PH1} + 5.5	V
	PH1	-1(3)	40	V
	VSENSE1	-0.3	5.5	V
LV Buck Regulator	BOOT2	-0.3	V_{PH2} + 5.5	V
	PH2	-1(3)	5.5	V
	VSENSE2	-0.3	5.5	V
Boost Converter	VSENSE3	-0.3	10	V
	BOOT3	-0.3	V_{PH3} + 5.5	V
	PH3	-1	10(4)	V
Digital Interface	NCS, SCK, SDO, SDI, MCU_ERR, SYNC_IN, DIAG_OUT/ SYNC_OUT, NRES, ENDRV/nIRQ	-0.3	5.5	V
Wake Input	WAKE	-7(2)	40	V
General Purpose Monitors	EXT_VSENSE1/2	-0.3	5.5	V
Driver Supply Decoupling	VREG	-0.3	5.5	V
Temperature Ratings	Junction temperature, T_J	-40	150	°C
	Storage temperature, T_{stg}	-55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) I_{max} = 40 mA max allowed current in substrate diode for t < 2 ms. For more negative voltage level series resistor is required.
(3) -2V for 10 ns.
(4) V_{BOOST} + 2V for 10 ns

9.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 10, 11, 20, 21, 30, 31, and 40)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

9.3 Recommended Operating Conditions

POS		MIN	NOM	MAX	UNIT
R1.1	Input supply voltage range on VIN, AVIN, and VIN_SAFE pins for initial power-up (startup from the OFF State) to one of the powered-up states (RESET, DIAGNOSTIC, ACTIVE, or SAFE state).(1)	5.8		36	V
R1.2a	Input supply voltage range on VIN, AVIN and VIN_SAFE pins to maintain the device in powered-up state when the BOOST converter (or other min 4.5 V external supply) supplies the EXTSUP pin. V_{BUCK1} = 3.3 V	4.0		36	V
R1.2b	Input supply voltage range on VIN, AVIN and VIN_SAFE pins to maintain the device in powered-up state when the BOOST converter (or other min 4.5 V external supply) supplies the EXTSUP pin. V_{BUCK1} = 3.6 V	4.3		36	V

9.3 Recommended Operating Conditions (続き)

POS		MIN	NOM	MAX	UNIT
R1.2c	Input supply voltage range on VIN, AVIN, and VIN_SAFE pins to maintain the device in powered-up state when there is no power supply connected to the EXTSUP pin.	5.3		36	V
R1.3	Input supply voltage range at which full device functionality and performance is assured	6		18	V
R1.4	Input supply voltage range at which full device functionality is assured while some performance parameters may be compromised.	18		36	V
R1.5	Input supply voltage range at which Wide-VIN Synchronous BUCK regulator is allowed to operate in a pulse-skipping mode.	25		36	V
R1.6	VIO supply voltage	3		5.1	V
R1.7	Operating free air temperature, T_A	-40		125	°C

(1) This initial voltage needs to be present for >100 ms and device must be started-up from the OFF State to one of the powered-up states (RESET, DIAGNOSTIC, ACTIVE or SAFE State) before battery voltage is allowed to drop to ranges specified in R1.2a

9.4 Thermal Information

THERMAL METRIC(1)		TPS65313-Q1 RWG (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

9.5 Power-On-Reset, Current Consumption, and State Timeout Characteristics

VIN/AVIN/VIN_SAFE = 4V to 36V, T_A = -40°C to 125°C,T_J up to 150°C, unless otherwise noted

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.0a	$V_{IN\_POR\_F}$	Power On Reset assertion threshold	Falling VIN	3.8		4.0	V
1.0b	$V_{IN\_POR\_R}$	Power On Reset de-assertion threshold	Rising VIN	5.3		5.8	V
1.1	I_{OFF}	Total current consumption in the OFF state from VIN, AVIN, and VIN_SAFE pins	T_J = 25°C, all regulator outputs disabled, WAKE = 0 V, 2.3 V ≤ VIN/AVIN/VIN_SAFE ≤ 12 V		3	12	µA
			T_J = 125°C, all regulator outputs disabled, WAKE = 0 V, 2.3 V ≤ VIN/AVIN/VIN_SAFE ≤ 12 V			20	µA
			T_J = 150°C, all regulator outputs disabled, WAKE = 0 V, 2.3 V ≤ VIN/AVIN/VIN_SAFE ≤ 12 V			50	µA
1.2a	I_{IN_PU}	Total current consumption in one of the powered-up state (RESET, DIAGNOSTIC, ACTIVE or SAFE) from VIN, AVIN, and VIN_SAFE pins	All regulators are enabled with 0 A load. VIN/AVIN/VIN_SAFE = 14 V, VREG powered from BOOST.		47		mA
1.4	$t_{START\_UP\_TO}$	Start-up/Power-up timeout interval	Measured from WAKE input rising edge until all switched-mode regulators are enabled. If regulators are not enabled in this time interval device transitions to OFF state.	550		1700	ms
1.5	$t_{RESET\_STATE\_TO}$	RESET state timeout interval	Measured from the start of active RESET state condition until RESET state condition is removed and NRES extension is started		1.2		s
1.6	$t_{DIAG\_STATE\_TO}$	DIAGNOSTIC state timeout interval	Measured from NRES rising edge until the device enters SAFE state		640		ms
1.7	$t_{SAFE\_STATE\_TO}$	SAFE state timeout interval range	Measured from time when the device enters SAFE state from DIAGNOSTIC or ACTIVE or RESET state and based on SAFE_TO [1:0] bits setting.	1.25		640	ms

9.6 PLL/Oscillator and SYNC_IN Pin Characteristics

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.0b	f_{PLL_UNLOCK}	Free-running PLL output clock frequency range as DC-DC converters switching frequency clock source		2.0	2.2	2.4	MHz
2.1	f_{PLL_LOCK}	PLL output clock frequency while synchronized to SYNC_IN input clock		2.0	2.2	2.4	MHz
2.2	$D_{f/f}$	Spread spectrum variation for internally generated and modulated around 2.2 MHz clock	Spread Spectrum type/mode for internally generated f_{SW} clock is set through EEPROM mapped bits	1.79	2.1	2.398	MHz
2.3	$f_{SSM\_STEP\_INT\_OSC}$	Internal clock spread spectrum modulation steps	f_{SSM_STEP}/f_{SW}		1.25		%
2.4	$f_{DITHER\_STEP\_SYNC}$	SYNC_IN input clock dithering steps for 2.2 MHz of nominal frequency(1)	$f_{DITHER\_STEP}/f_{SYNC\_IN}$ =100 kHz / 2.2 MHz			5	%
2.5	$f_{PLL\_UNLOCK\_ACC}$	PLL Clock Output accuracy when VCO is in free-running mode.		-5		5	%
2.6	$f_{PLL\_LOCK\_ACC}$	PLL Clock Output accuracy when PLL is locked to SYNC_IN input clock		-1		1	%
2.7	t_{PLL_LOCK}	PLL Lock time(2)	When SYNC_IN clock frequency changes from 0 Hz to 2.2 MHz ±5%		100	150	µs
2.8	$V_{SYNC\_HIGH\_THR}$	SYNC_IN clock input high level threshold		1.84			V
2.9	$V_{SYNC\_LOW\_THR}$	SYNC_IN clock input low level threshold				0.76	V
2.10	D_{SYNC}	SYNC_IN clock input duty cycle		10		90	%
2.13	f_{SYSCLK}	System Clock Frequency		7.6	8	8.4	MHz
2.14	f_{MODCLK}	Internal Modulation Clock Frequency		2.09	2.2	2.31	MHz

(1) The input SYNC_IN clock can be modulated in a staircase (triangular) fashion step-by-step, with minimum step duration of 50 µs and clock frequency change of 50 kHz to 100 kHz.
(2) After the PLL is locked, SYNC_IN clock can change within ranges defined by f_{PLL_LOCK} with maximum frequency step defined by $f_{DITHER\_STEP\_SYNC}$.

9.7 Wide-VIN Synchronous Buck Regulator (Wide-VIN BUCK) Characteristics

TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.0	f_{SW_BUCK1}	Wide-VIN BUCK switching frequency	6V ≤ VIN/AVIN/VIN_SAFE ≤ 36V	2.0	2.2	2.4	MHz
3.1a	VIN	Wide-VIN BUCK supply voltage	V_{BUCK1} = 3.3 V	4.0		36	V
3.1b	VIN	Wide-VIN BUCK supply voltage	V_{BUCK1} = 3.6 V	4.3		36	V
3.2a	V_{BUCK1}	Wide-VIN BUCK output voltage			3.3		V
3.2b	V_{BUCK1}	Wide-VIN BUCK output voltage			3.6		V
3.3	$V_{BUCK1\_DC\_ACCURACY}$	Wide-VIN BUCK DC output voltage accuracy	6 V ≤ VIN/AVIN/ VIN_SAFE ≤ 18 V, measured at VSENSE1 pin(3)	–1.7		1.7	%
3.4a	I_{BUCK1_LOAD}	Wide-VIN BUCK load current(2)	min(VIN) ≤ VIN/AVIN/ VIN_SAFE ≤ 6V (4)			Refer to Figure 9.5	A
			6 V ≤ VIN/AVIN/ VIN_SAFE ≤ 18 V			3.1	A
3.5a	V_{BUCK1_RIPPLE}	Wide-VIN BUCK output peak voltage ripple (0.5 × V_{PP}), in percentage of target regulation voltage	6 V ≤ VIN/AVIN/ VIN_SAFE ≤ 18 V, I_{BUCK1_LOAD} = 0 A to max(I_{BUCK1_LOAD}) (3)		0.3		%
3.5b	$V_{BUCK1\_RIPPLE\_SSM}$	Wide-VIN BUCK output peak voltage ripple (0.5 × V_{PP}), in percentage of target regulation voltage, when f_{SW} clock spread spectrum modulation is enabled	6 V ≤ VIN/AVIN/ VIN_SAFE ≤ 18 V, I_{BUCK1_LOAD} = 0 A to max(I_{BUCK1_LOAD}) (3)		0.3		%
3.6	$R_{DSON\_HS\_BUCK1}$	ON resistance of high-side switch FET	V_{GS}=4.5V, I_{DS} = 0.7A		150	250	mΩ
3.7	$R_{DSON\_LS\_BUCK1}$	ON resistance of low-side switch FET	V_{GS}=4.5V, I_{DS} = 0.7A		80	150	mΩ
3.10	t_{SS_BUCK1}	Wide-VIN BUCK internal soft-start duration	Measured from Wide-VIN BUCK enable event to V_{BUCK1} crossing its UV threshold. C_{BUCK1} = 100 µF		1		ms
3.12a	$I_{HS\_SCG\_ILIM\_BUCK1}$	High side switch current limit for weak-short/hard-short conditions		4	5.5	7	A

9.7 Wide-VIN Synchronous Buck Regulator (Wide-VIN BUCK) Characteristics (続き)

TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.12b	$I_{HS\_OVC\_ILIM\_BUCK1}$	High side switch current limit for over-load conditions.			3.8	5	A
3.12c	$I_{HS\_SCG\_ILIM\_BUCK1}$ / $I_{HS\_OVC\_ILIM\_BUCK1}$	Ratio between short-circuit current limit and over-load current limit for high-side switch			1.43		A/A
3.13a	$I_{LS\_SCG\_ILIM\_BUCK1}$	Low side switch current limit for weak-short/hard-short conditions		4	5.5	7	A
3.13b	$I_{LS\_OVC\_ILIM\_BUCK1}$	Low side switch current limit for over-load conditions			3.8	5	A
3.13c	$I_{LS\_SCG\_ILIM\_BUCK1}$ / $I_{LS\_OVC\_ILIM\_BUCK1}$	Ratio between short-circuit current limit and over-load current limit for low-side switch			1.43		A/A
3.14	$I_{LS\_SINK\_BUCK1}$	Low side sinking current limit		-2.5	-2	-1.40	A
3.18a	R_{DISCH_BUCK1}	Wide-VIN BUCK internal discharge resistance when device is in RESET state	Wide-VIN BUCK disabled, V_{BUCK1} = 1 V	100	180	400	Ω
3.18b	$R_{DISCH\_BUCK1\_OFF}$	Wide-VIN BUCK internal discharge resistance when device is in OFF state	Wide-VIN BUCK disabled, V_{BUCK1} = 1 V	400	800	1200	Ω
3.19	$\Delta V_{BUCK1\_LINEREG\_DC}$	Output voltage line regulation NOTE: DC line regulation as output voltage change in % (ΔV_{BUCK1} / V_{BUCK1}) as VIN is changing from 6 V to 18 V	6 V ≤ VIN/AVIN/ VIN_SAFE ≤ 18 V, I_{BUCK1_LOAD} = 1.5 A (3)		0.1	0.2	%
3.20	$\Delta V_{BUCK1_LOADREG_DC}$Wide-VIN	Output voltage load regulation NOTE: DC load regulation as output voltage change in % (ΔV_{BUCK1} / V_{BUCK1}) as I_{BUCK1_LOAD} changes from 0A to max(I_{BUCK1_LOAD})	6 V ≤ VIN/AVIN/ VIN_SAFE ≤ 18 V (3)		0.1	0.2	%
3.21a	$V_{BUCK1\_BUCK1\_LOAD\_TRAN1}$	Load transient regulation, in percentage of steady-state regulation voltage	6 V ≤ VIN/AVIN/ VIN_SAFE ≤ 18 V, I_{BUCK1_LOAD} load steps: - 0.5 A to 1.5 A - 1.5 A down to 0.5 A dI_{BUCK1_LOAD}/dt = 300 mA/µs (3)	-3		3	%
3.21b	$V_{BUCK1\_LOAD\_TRAN2}$	Load transient regulation, in percentage of steady-state regulation voltage	6 V ≤ VIN/AVIN/ VIN_SAFE ≤ 18 V, I_{BUCK1_LOAD} load steps: - 2 A to 3.1 A dI_{BUCK1_LOAD}/dt = 60 mA/µs (3)	-3		3	%
3.21c	$V_{BUCK1\_LOAD\_TRAN3}$	Load transient regulation, in percentage of steady-state regulation voltage	6 V ≤ VIN/AVIN/ VIN_SAFE ≤ 18 V, I_{BUCK1_LOAD} load steps: - 3.1 A to 1 A dI_{BUCK1_LOAD}/dt = 100 mA/µs (3)	-3		3	%
3.22	t_{SETTLE_BUCK1}	Load transient recovery time to 1% below starting point or 1% above starting point.	Refer to 3.21a, 3.21b, and 3.21c.			20	µs
3.24a	η_{BUCK1}	Wide-VIN BUCK Efficiency	VIN/AVIN/VIN_SAFE = 13 V, V_{BUCK1}=3.3V, I_{BUCK1_LOAD} = 1.5 A Other conditions covered in efficiency plot diagram		83		%
3.26	$V_{BUCK1\_RESTART\_LEVEL}$	Wide-VIN BUCK output voltage level before ramp-up starts, in percentage of target regulation voltage	After wide-VIN BUCK regulator is shutdown its output voltage is discharged below this level before a new start-up event.			45	%

(1) Total output capacitance, C_{BUCK1}, including board parasitic capacitance, should not exceed 100 µF.
(2) Advanced thermal design may be required to avoid thermal shutdown.
(3) Refer to Regulator LC Selection table for inductor and capacitor values.
(4) Some of the BUCK1 performance electrical parameters may not be met when VIN/AVIN/VIN_SAFE ≤ 6.

9.8 Low-Voltage Synchronous Buck Regulator (LV BUCK) Characteristics

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.0	f_{SW_BUCK2}	LV BUCK switching frequency		2.0	2.2	2.4	MHz
4.1	V_{SUP2_NOM}	LV BUCK supply voltage			3.3		V

9.8 Low-Voltage Synchronous Buck Regulator (LV BUCK) Characteristics (続き)

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.1	V_{SUP2_NOM}	LV BUCK supply voltage			3.6		V
4.1a	V_{SUP2}	LV BUCK supply voltage range, in percentage of V_{SUP2_NOM}		94		106	%
4.2	V_{BUCK2}	LV BUCK output voltage			1.2		V
4.2	V_{BUCK2}	LV BUCK output voltage			1.25		V
4.2	V_{BUCK2}	LV BUCK output voltage			1.8		V
4.2	V_{BUCK2}	LV BUCK output voltage			2.3		V
4.3	$V_{BUCK2\_DC\_ACCURACY}$	LV BUCK DC output voltage accuracy	I_{BUCK2_LOAD} = 0 A to max(I_{BUCK2_LOAD}), measured at VSENSE2 pin(3)	-1.5		+1.5	%
4.4a	I_{BUCK2_LOAD}	LV BUCK load current(2)	VSUP2 = 3.3 V for V_{BUCK2} = 1.2 V, 1.25 V, 1.8 V			2	A
4.4b	I_{BUCK2_LOAD}	LV BUCK load current(2)	VSUP2 = 3.3 V , V_{BUCK2} = 2.3 V			1.5	A
4.5a	V_{BUCK2_RIPPLE}	LV BUCK output peak voltage ripple (0.5 × V_{PP}), in percentage of target regulation voltage	I_{BUCK2_LOAD} = max(I_{BUCK2_LOAD})(3)		0.6		%
4.5b	$V_{BUCK2\_RIPPLE\_SSM}$	LV BUCK output peak voltage ripple (0.5 × V_{PP}), in percentage of target regulation voltage, when f_{SW} spread spectrum clock modulation is enabled	I_{BUCK2_LOAD} = max(I_{BUCK2_LOAD}) (3)		0.6		%
4.6	$I_{SUP\_BUCK2\_NO\_LOAD}$	LV BUCK no-load supply current	I_{BUCK2_LOAD} = 0 A(3)		3	6.5	mA
4.7	$R_{DSON\_HS\_BUCK2}$	ON resistance of high-side switch FET	V_{GS}=4.5V, I_{DS} = 1.0A		90	180	mΩ
4.8	$R_{DSON\_LS\_BUCK2}$	ON resistance of low-side switch FET	V_{GS}=4.5V, I_{DS} = 1.0A		110	220	mΩ
4.11	t_{SS_BUCK2}	LV BUCK soft-start duration	Measured from LV BUCK enable event to V_{BUCK2} crossing its UV threshold. C_{OUT} = 100µF		0.85		ms
4.12	$I_{HS\_LIMIT\_BUCK2}$	High-side switch current limit for weak-short/hard-short conditions		2.6	3.5	4.5	A
4.13	$I_{LS\_LIMIT\_BUCK2}$	Low-side switch current limit for functional over-load conditions		2.1	2.7	3.3	A
4.14	$I_{LS\_SINK\_BUCK2}$	Low-side switch sinking current limit		-1.1	-0.8	-0.5	A
4.18a	R_{DISCH_BUCK2}	LV BUCK internal discharge resistance when the device is in RESET state	LV BUCK disabled, V_{BUCK2} = 1 V	100	200	400	Ω
4.18b	$R_{DISCH\_BUCK2\_OFF}$	LV BUCK internal discharge resistance when the device is OFF state	LV BUCK disabled, V_{BUCK2} = 1 V	400	800	1200	Ω
4.19	$\Delta V_{BUCK2\_LINEREG\_DC}$	Output voltage line regulation NOTE: DC line regulation as output voltage change in % (ΔV_{BUCK2} / V_{BUCK2}) as V_{SUP2} is changing from V_{SUP2_MIN} to V_{SUP2_MAX}	0.97 × V_{SUP2_NOM} ≤ V_{SUP2} ≤ 1.03 × V_{SUP2_NOM}, I_{BUCK2_LOAD} = 1.5 A(3)		0.1	0.2	%
4.20	$\Delta V_{BUCK2\_LOADREG\_DC}$	Output voltage load regulation NOTE: DC load regulation as output voltage change in % (ΔV_{BUCK2} / V_{BUCK2}) as I_{BUCK2} changes from 0A to 2A	I_{BUCK2_LOAD} = 0 A to max(I_{BUCK2_LOAD})(3)		0.2	0.3	%
4.21	$V_{BUCK2\_LOAD\_TRAN1}$	LV BUCK load transient regulation, in percentage of steady-state regulation voltage	I_{BUCK2_LOAD} load step: - 0.5 A to 1.5 A - 1.5 A down to 0.5 A dI_{BUCK2_LOAD}/dt = 300 mA/µs	-6		6	%
4.22	t_{SETTLE_BUCK2}	Load transient recovery time to 1% below starting point, or 1% above starting point.	I_{BUCK2_LOAD} load step: - 0.5 A to 1.5 A - 1.5 A down to 0.5 A dI_{BUCK2_LOAD}/dt = 300 mA/µs			20	µs
4.24	$V_{BUCK2\_RESTART\_LEVEL}$	LV BUCK output voltage level before ramp-up starts, in percentage of target regulation voltage	NOTE: when there is a shutdown event followed by new start-up event, device cannot start-up again until LV BUCK2 discharges below this level			45	%

(1) Total output capacitance, C_{BUCK2}, including board parasitic capacitance, should not exceed 100 µF.
(2) Advanced thermal design may be required to avoid thermal shutdown.
(3) Refer to Regulator LC Selection table for inductor and capacitor values.

9.9 Synchronous Boost Converter (BOOST) Characteristics

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.0	$V_{SUP\_BOOST\_NOM}$	BOOST supply voltage			3.3		V
5.0	$V_{SUP\_BOOST\_NOM}$	BOOST supply voltage			3.6		V
5.0a	V_{SUP_BOOST}	BOOST supply voltage range, in percentage of $V_{SUP\_BOOST\_NOM}$		94		106	%
5.1	V_{BOOST}	Boost output voltage			5		V
5.2	f_{SW_BOOST}	BOOST switching frequency		2.0	2.2	2.4	MHz
5.3	$V_{BOOST\_DC\_ACCURACY}$	BOOST DC output voltage accuracy	I_{BOOST_LOAD} = 0 A to max(I_{BOOST_LOAD}), measured at VSENSE3 pin(3)	-1.5		1.5	%
5.4a	V_{BOOST_RIPPLE}	BOOST output peak voltage ripple (0.5 × V_{PP}), in percentage of target regulation voltage	I_{BOOST_LOAD} = max(I_{BOOST_LOAD})(3)		0.3		%
5.4b	$V_{BOOST\_SSM\_RIPPLE}$	BOOST output peak voltage ripple (0.5 × V_{PP}), in percentage of target regulation voltage, when f_{SW} clock modulation is enabled	I_{BOOST_LOAD} = max(I_{BOOST_LOAD})(3)		0.3		%
5.5	$V_{BOOST\_LOAD\_TRAN}$	Load transient regulation, in percentage of steady-state regulation voltage	I_{BOOST_LOAD} load step #1 • 520 mA to 600 mA • 600 mA down to 520 mA I_{BOOST_LOAD} load step #2 • 60 mA to 140 mA • 140 mA to 60 mA dI_{BOOST_LOAD}/dt = 300 mA/µs	-3		3	%
5.6	t_{SETTLE_BOOST}	Load transient recovery time to 1% below starting point or 1% above starting point.				20	µs
5.7	$R_{DS\_ON\_HS\_BOOST}$	ON resistance of high-side switch FET	V_{GS}=4.5V, I_{DS} = 1.0A		110	140	mΩ
5.8	$R_{DS\_ON\_LS\_BOOST}$	ON resistance of low-side switch FET	V_{GS}=4.5V, I_{DS} = 1.0A		210	350	mΩ
5.10a	R_{DISCH_BOOST}	BOOST internal discharge resistance when the device is in powered states		100	200	400	Ω
5.10b	$R_{DISCH\_BOOST\_OFF}$	BOOST internal discharge resistance when device is in OFF state			800		Ω
5.11	t_{SS_BOOST}	BOOST internal soft-start duration	Measured from BOOT enable event to V_{BOOST} crossing its UV threshold. C_{OUT} = 100 µF		2		ms
5.14a	I_{BOOST_LOAD}	BOOST load current(2)				600	mA
5.15	$I_{LS\_LIMIT\_BOOST}$	Low-side switch source current limit (weak/short current limit)		1.9	2.3	2.7	A
5.16	$I_{HS\_LIMIT\_BOOST}$	High-side switch source current limit		1	1.4	1.8	A
5.17	$I_{CL\_HS\_SINK\_BOOST}$	Internal high-side switch sink current limit		-1.30		-0.75	A
5.20	$I_{VSUP\_BOOST\_NO\_LOAD}$	BOOST no-load supply current	I_{BOOST_LOAD} = 0 A		7	8	mA
5.21	$V_{BOOST\_START\_UP}$	V_{BOOST} start-up time	Measured from WAKE event to V_{BOOST} ramps above its UV threshold level		4	8	ms
5.22	$\Delta V_{BOOST\_LINEREG\_DC}$	Output voltage line regulation NOTE: DC line regulation as output voltage change in % (ΔV_{BOOST} / V_{BOOST}) as V_{SUP_BOOST} changes from MIN to MAX	0.97 × $V_{SUP\_BOOST\_NOM}$ ≤ V_{SUP_BOOST} ≤ 1.03 × $V_{SUP\_BOOST\_NOM}$, I_{BOOST_LOAD} = 0.3 A		0.1	0.2	%
5.23	$\Delta V_{BOOST\_LOADREG\_DC}$	Output voltage load regulation NOTE: DC load regulation as output voltage change in % (ΔV_{BOOST} / V_{BOOST}) as I_{BOOST_LOAD} changes from MIN to MAX	I_{BOOST_LOAD} = 0 A to max(I_{BOOST_LOAD})		0.2		%
5.24	$V_{BOOST\_RESTART\_LEVEL}$	BOOST output voltage level before ramp-up starts, in percentage of target regulation voltage	NOTE: when there is a BOOST shutdown event followed by new start-up event, the device cannot start-up again until BOOST discharges below this level			88	%

(1) Total capacitance, C_{BOOST}, including board parasitic capacitance, should not exceed 100 µF.

(2) Advanced thermal design may be required to avoid thermal shutdown.
(3) Refer to Regulator LC Selection table for inductor and capacitor values.

9.10 Internal Voltage Regulator (VREG) Characteristics

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.0	V_{EXTSUP}	V_{REG} External Supply (EXTSUP) range when internal circuitry is in unregulated switch-mode		4.8		5.25	V
6.1	$V_{REG\_OUT\_SWITCH}$	Internal unregulated supply output in switch-mode	I_{VREG} = 0mA to 75mA	4.0	5.0	5.25	V
6.2	$V_{REG\_OUT\_LDO}$	Internal regulated supply output in LDO-mode	I_{VREG} = 0mA to 75mA, VIN/AVIN/VIN_SAFE= 5.3V to 36V, no external supply at EXTSUP pin.(1)	4.0	4.5	5	V
6.3	$V_{EXTSUP\_RISE\_TH}$	LDO-mode to switch-mode switch-over threshold for rising EXTSUP input	Measured at the EXTSUP pin, I_{VREG} = 0mA to 75mA, V_{EXTSUP} ramping, the device in RESET state.(1)	4.6	4.7	4.8	V
6.4	$V_{EXTSUP\_FALL\_TH}$	Switch-mode to LDO-mode switch-over threshold for falling EXTSUP input	Measured at the EXTSUP pin, I_{VREG} = 0mA to 75mA, V_{EXTSUP} falling, the device in ACTIVE/RESET/SAFE state	4.5	4.6	4.7	V

(1) C_{VREG_OUT} = 1.2 µF to 3.3 µF

9.11 Voltage Monitors for Regulators Characteristics

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.0	V_{REF_MON}	Voltage reference for monitoring circuits derived from BG2	V_{BG2} = 1.2V (TYP)		1.0		V
7.0a	V_{REF_REG}	Voltage reference for regulator circuits derived from BG1	V_{BG1} = 1.2V (TYP)		1.2		V
7.1	$V_{REF\_MON\_ACC}$	Voltage reference accuracy for monitoring circuits		-1		+1	%
7.1a	$V_{REF\_REG\_ACC}$	Voltage reference accuracy for regulator circuits		-1		+1	%
7.2a	$t_{SMPS\_UV\_OV\_OVP}$	Deglitch time between Under-Voltage/Over-Voltage/Over-Voltage-Protection event to NRES output low	Measured from the start of Wide-VIN BUCK1/LV BUCK2/BOOST UV, OV, or OVP event to the NRES pin falling edge as the TPS65313B-Q1 transitions to either the RESET state or OFF state. It takes up to 5 system clock cycles from detected valid UV/OV/OVP event until device transitions to RESET state or OFF state.	21	30	39	µs
7.2b	$t_{SMPS\_UV\_OV\_OVP}$	Deglitch time between Under-Voltage/Over-Voltage/Over-Voltage-Protection event to ENDRV/nIRQ output low	Measured from Wide-VIN BUCK1/LV BUCK2/BOOST UV, OV, or OVP event to the ENDRV/nIRQ pin falling edge as the TPS65313B-Q1 transitions to the SAFE state. It takes up to 5 system clock cycles from detected valid UV/OV/OVP event until device transitions to SAFE state.	21	30	39	µs
7.2c	t_{VREG_UV}	Deglitch time from Under-Voltage event to NRES output low	Measured from the start of VREG UV event to the NRES pin falling edge as the TPS65313B-Q1 transitions to the OFF state. It takes up to 5 system clock cycles from detected valid UV event until device transitions to OFF state and drives NRES low.	24	32	40	µs
7.2d	t_{VREG_OV}	Deglitch time between Over-Voltage event to NRES output low	Measured from the start of VREG OV event to the NRES pin falling edge as the TPS65313B-Q1 transitions to the OFF state. It takes up to 5 system clock cycles from detected valid OV event until device transitions to OFF state and drives NRES low.	10	15	20	µs
7.2e	t_{VIO_OV}	VIO Over-Voltage deglitch time	Measured from the start of VIO OV event to the VIO_OV status bit is set.	10	15	20	µs
7.5a	$t_{BUCK2\_OVP\_OFF}$	Deglitch time for disabling Wide-VIN BUCK1 if LV BUCK2 Over-Voltage-Protection event is detected after LV BUCK2 is disabled due to prior LV BUCK2 Over-Voltage-Protection event detection	Measured from the start of LV BUCK2 OVP event to the NRES pin falling edge as the TPS65313B-Q1 transitions to the OFF state. It takes up to 5 system clock cycles from detected valid OVP event until device transitions to OFF state and drives NRES low.	21	30	39	µs
7.5b	$t_{BOOST\_OVP\_OFF}$	Deglitch time for disabling Wide-VIN BUCK1 if BOOST Over-Voltage-Protection event is detected after BOOST is disabled due to prior BOOST Over-Voltage-Protection event detection.	Measured from the start of BOOST OVP event to the NRES pin falling edge as the TPS65313B-Q1 transitions to the OFF state. It takes up to 5 system clock cycles from detected valid OVP event until device transitions to OFF state and drives NRES low.	60	76	90	µs
7.6	V_{IO_OV}	VIO Over-Voltage threshold		5.9		6.5	V

9.11 Voltage Monitors for Regulators Characteristics (続き)

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.7	V_{BUCK1_UV}	Wide-VIN BUCK1 Under-Voltage detection threshold, expressed in percentage from V_{BUCK1} nominal voltage.	VSENSE1 falling	-5.0		-2.5	%
7.8	V_{BUCK1_OV}	Wide-VIN BUCK1 Over-Voltage detection threshold, expressed in percentage from V_{BUCK1} nominal voltage.	VSENSE1 rising	2.5		5.0	%
7.9	V_{BUCK1_OVP}	Wide-VIN BUCK1 Over-Voltage Protection threshold, expressed in percentage from V_{BUCK1} nominal voltage.	VSENSE1 rising	6		10	%
7.9b	V_{BUCK1_EOVP}	Wide-VIN BUCK1 Extreme Over-Voltage Protection threshold	VSENSE1 rising	3.84	4	4.1610	V
7.10	V_{BUCK2_UV}	LV BUCK2 Under-Voltage detection threshold, expressed in percentage from VBUCK2 nominal voltage.	VSENSE2 falling	-5.0		-2.5	%
7.11	V_{BUCK2_OV}	LV BUCK2 Over-Voltage detection threshold, expressed in percentage from VBUCK2 nominal voltage.	VSENSE2 rising	2.5		5.0	%
7.12	V_{BUCK2_OVP}	LV BUCK2 Over-Voltage Protection threshold, expressed in percentage from VBUCK2 nominal voltage.	VSENSE2 rising	6		10	%
7.13	V_{BOOST_UV}	LV BOOST Under-Voltage detection threshold, expressed in percentage from VBOOST nominal voltage.	VSENSE3 falling	-5.0		-2.5	%
7.14	V_{BOOST_OV}	LV BOOST Over-Voltage detection threshold, expressed in percentage from VBOOST nominal voltage.	VSENSE3 rising	2.5		5.0	%
7.15	V_{BOOST_OVP}	LV BOOST Over-Voltage Protection threshold, expressed in percentage from VBOOST nominal voltage.	VSENSE3 rising	6		10	%
7.18	V_{REG_UV}	VREG under-voltage detection threshold	VREG falling	3.7		3.9	V
7.19	V_{REG_OV}	VREG over-voltage threshold	VREG rising	5.9		6.5	V
7.26a	$f_{SYSCLK\_ACKMNT\_SLOW}$	Analog System Clock Monitor slow clock error detection threshold before EEPROM download		455	700	945	kHz
7.26b	$f_{SYSCLK\_ACKMNT\_SLOW}$	Analog System Clock Monitor slow clock error detection threshold after EEPROM download		4.75	5.60	6.45	MHz
7.27a	$f_{SYSCLK\_ACKMNT\_FAST}$	Analog System Clock Monitor fast clock error detection threshold before EEPROM download		3.38	5.20	7.02	MHz
7.27b	$f_{SYSCLK\_ACKMNT\_FAST}$	Analog System Clock Monitor fast clock error detection threshold after EEPROM download		8.84	10.40	11.96	MHz
7.31	$f_{PLL\_SMPS\_DCKMNT\_SLOW\_ERR}$	Digital PLL/SMPS Clock Monitor slow clock error detection threshold		1.58	1.66	1.75	MHz
7.33	$f_{PLL\_SMPS\_DCKMNT\_FAST\_ERR}$	Digital PLL/SMPS Clock Monitor fast clock error detection threshold		2.40	2.53	2.67	MHz

9.12 External General Purpose Voltage Monitor Characteristics

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
8.0	$V_{REF\_EXTVMON}$	Reference voltage for general-purpose external voltage monitors at EXT_VSENSEx pins			0.8		V
8.1	$V_{REF\_EXTVMON\_ACC}$	Accuracy of reference voltage for general-purpose external voltage monitors at EXT_VSENSEx pins		-1		1	%
8.2	$t_{EXT\_VSENSE1\_RESET}$	Deglitch time between EXT_VMON1 Under-Voltage/ Over-Voltage event to NRES output low.	Measured from the start of UV or OV event at the EXT_VSENSE1 pin to the NRES pin falling edge as the TPS65313B-Q1 transitions to the RESET state. It takes up to 5 system clock cycles from detected valid UV or OV event until device transitions to RESET state.	21	30	39	µs
8.3	$t_{EXT\_VSENSE2\_RESET}$	Deglitch time between EXT_VMON2 Under-Voltage/ Over-Voltage event to NRES output low.	Measured from the start of UV or OV event at the EXT_VSENSE2 pin to the NRES pin falling edge as the TPS65313B-Q1 transitions to the RESET state. It takes up to 5 system clock cycles from detected valid UV or OV event until device transitions to RESET state.	21	30	39	µs
8.4	$t_{EXT\_VSENSE1\_SAFE}$	Deglitch time between reaching EXT_VMON1 Under-Voltage/Over-Voltage condition to ENDRV/nIRQ output interrupt driven low and setting corresponding SPI status bit.	Measured from the start of UV or OV event at the EXT_VSENSE1 pin to the ENDRV/nIRQ pin falling edge as the TPS65313B-Q1 transitions to the SAFE state. It takes up to 5 system clock cycles from detected valid UV or OV event until device transitions to SAFE state.	21	30	39	µs
8.5	$t_{EXT\_VSENSE2\_SAFE}$	Deglitch time between reaching EXT_VMON2 Under-Voltage/Over-Voltage condition to ENDRV/nIRQ output interrupt driven low and setting corresponding SPI status bit.	Measured from the start of UV or OV event at the EXT_VSENSE2 pin to the ENDRV/nIRQ pin falling edge as the TPS65313B-Q1 transitions to the SAFE state. It takes up to 5 system clock cycles from detected valid UV or OV event until device transitions to SAFE state.	21		39	µs
8.6	$V_{EXT\_MON1\_UV}$	EXT_VMON1 Under-Voltage expressed in percentage of external sense voltage 1 defined by 8.0 and 8.1 parameters	EXT_VSENSE1 falling Note: the sense voltage at EXT_VSENSE1 pin has to be kept below 1 V to assure that the parameter remains in the defined range	-5.0		-3.0	%
8.7	$V_{EXT\_MON2\_UV}$	EXT_VMON2 Under-Voltage, expressed in percentage of external sense voltage 2 defined by 8.0 and 8.1 parameter	EXT_VSENSE2 falling Note: the sense voltage at EXT_VSENSE2 pin has to be kept below 1 V to gurantee parameter remains in the defined range	-5.0		-3.0	%
8.8	$V_{EXT\_MON1\_OV}$	EXT_VMON1 Over-Voltage expressed in percentage of external sense voltage 1 defined by 8.0 and 8.1 parameter	EXT_VSENSE1 rising Note: the sense voltage at EXT_VSENSE1 pin has to be kept below 1 V to gurantee parameter remains in the defined range	3.0		5.0	%
8.9	$V_{EXT\_MON2\_OV}$	EXT_VMON2 Over-Voltage expressed in percentage of external sense voltage 2 defined by 8.0 and 8.1 parameter	EXT_VSENSE2 rising Note: the sense voltage at EXT_VSENSE2 pin has to be kept below 1 V to gurantee parameter remains in the defined range	3		5.0	%

9.13 VIN and VIN_SAFE Under-Voltage and Over-Voltage Warning Characteristics

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
9.0a	$VIN_{BAD\_FALL\_TH}$	VIN_BAD falling threshold range(1)	VIN_BAD_TH [1:0] = b00	5.8		6.6	V
9.0b	$VIN_{BAD\_FALL\_TH}$	VIN_BAD falling threshold range(1)	VIN_BAD_TH [1:0] = b01	6.8		7.6	V
9.0c	$VIN_{BAD\_FALL\_TH}$	VIN_BAD falling threshold range(1)	VIN_BAD_TH [1:0] = b10	7.8		8.6	V
9.1	$t_{VIN\_BAD\_BLK}$	VIN_BAD falling detection blanking time		91		106	µs
9.2	$t_{VIN\_GD\_BLK}$	VIN_GD(2) rising detection blanking time		10		33	µs
9.3	VIN_{OV_TH}	VIN_OV shutdown threshold		36		40	V

9.13 VIN and VIN_SAFE Under-Voltage and Over-Voltage Warning Characteristics (続き)

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
9.4	$t_{VIN\_OV\_BLK}$	VIN_OV detection blanking time		10		20	µs

(1) Default setting can be modified after power-up event through SPI mapped register bits VIN_BAD_TH [1:0]. Default setting is VIN_BAD_TH [1:0] = b00 (5.8 V to 6.6 V)
(2) VIN_GD is asserted when battery voltage at AVIN pin is greater than POR threshold AND less than OV threshold

9.14 WAKE Input Characteristics

VIN/AVIN/VIN_SAFE = 4 V to 36 V, T_A = -40°C to 125°C, T_J up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
10.0	$V_{WAKE-ON}$	Voltage threshold to enable the device	Wake pin is a level and edge sensitive input.	4.2	4.6	5.0	V
10.1	$V_{WAKE-ON-HYS}$	WAKE input hysteresis			100	200	mV
10.2	$I_{L\_WAKE\_26V\_VIN\_26V}$	WAKE pin leakage current	WAKE = 26 V, VIN = 26 V, device is starting-up or it is powered-up			110	µA
10.3	$I_{L\_WAKE\_3.5V\_VIN\_26V}$	WAKE pin leakage current	WAKE = 3.5 V, VIN = 26 V, device is starting-up or it is powered-up			20	µA
10.4	t_{WAKE_DEG}	MIN pulse width at WAKE input to set analog wake-up latch (or power-on latch) (or WAKE input de-glitch time)	V_{WAKE} = 5.0 V or higher to suppress short spikes at the WAKE pin	79	130	235	µs

9.15 NRES (nRESET) Output Characteristics

VIN/AVIN/VIN_SAFE = 4V to 36V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
11.0	V_{NRES_LOW}	NRES low level output voltage	I_{EX_NRES} = 5 mA, (external open-drain current)	0		0.2	V
11.1	R_{NRES_PU}	NRES internal pull-up resistance to VIO	The device in normal operation and no VIO over-voltage condition	2.4		6.8	kΩ
11.3	t_{NRES_EXT}	NRES extension time	Set through NRES_EXT [1:0] bits in DEV_CFG4 configuration register	2		32	ms
11.4	$V_{NRES\_IN\_TH}$	NRES input read-back logic '1' threshold		325	400	475	mV
11.5	$t_{NRES\_ERR\_DEG}$	NRES read-back error de-glitch time(1)		3		5	µs

(1) Total external capacitance on NRES pin should be less than 200 pF.

9.16 ENDRV/nIRQ Output Characteristics

VIN/AVIN/VIN_SAFE = 4V to 36V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
12.0	V_{ENDRV_LOW}	ENDRV/nIRQ low level output voltage	I_{EX_ENDRV} = 5mA, (external open-drain current)	0		0.2	V
12.1	R_{ENABLE_PU}	ENDRV/nIRQ internal pull-up resistance to VIO	The device in normal operation and no VIO over-voltage condition	2.4		6.8	kΩ
12.4	$t_{ENDRV\_RDBK\_ERR\_DEG}$	ENDRV/nIRQ read-back error de-glitch time		3		5	µs

(1) Total external capacitance on ENDRV/nIRQ pin should be less than 200 pF.

9.17 Analog DIAG_OUT

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
13.0	$I_{DIAGOUT\_MAX}$	DIAG_OUT output current in Analog MUX mode				300	µA
13.1	$V_{OFFSET\_AMUX\_BUF}$	Input offset of AMUX buffer		-7		7	mV

9.17 Analog DIAG_OUT (続き)

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
13.2	$C_{AMUX\_DIAG\_OUT}$	AMUX buffer output capacitor	Directly at DIAG_OUT pin			100	pF
13.3	$C_{AMUX\_LOW\_PASS}$	Low pass filter capacitance	Requires > 1kΩ series resistor between DIAG_OUT and $C_{AMUX\_LOW\_PASS}$			100	nF
13.4	DR_{VIN_SAFE}	AMUX output division ratio for VIN_SAFE, VIN_SAFE/V_{DIAG_OUT}	DIAG_MUX_SEL [7:0] = 0000 0001b	19.6	20	20.4	
13.5	DR_{VIN}	AMUX output division ratio for VIN, VIN/V_{DIAG_OUT}	DIAG_MUX_SEL [7:0] = 0000 0010b	19.6	20	20.4	
13.6	DR_{VREF_MON}	AMUX output division ratio for Voltage Monitor bandgap reference, V_{REF_MON}/V_{DIAG_OUT}	DIAG_MUX_SEL [7:0] = 0000 0011b, V_{REF_MON} = 1.0V (TYP)		1		
13.7	DR_{VREF_REG}	AMUX output division ratio for Regulators bandgap voltage reference, V_{REF_REG}/V_{DIAG_OUT}	DIAG_MUX_SEL [7:0] = 0000 0100b, V_{REF_REG} = 1.2V (TYP)		1		
13.8	DR_{AVDDx}	AMUX output division ratio for AVDD1 and AVDD2, V_{AVDDx}/ V_{DIAG_OUT} (1)	DIAG_MUX_SEL [7:0] = 0000 0101b - 0000 0110b	4.29	4.385	4.48	

(1) As nominal regulation voltage of AVDD1 and AVDD2, V_{ADDx} is 3.5 V. The nominal voltage measured at the DIAG_OUT pin is 0.8 V. Tolerance range of V_{AVDDx} is ±5 %.

9.18 Digital INPUT/OUTPUT IOs (SPI Interface IOs, DIAG_OUT/SYNC_OUT, MCU_ERROR)

VIN/AVIN/VIN_SAFE = 4 V to 36 V, T_A = -40°C to 125°C, T_J up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
14.0	$V_{DIG\_IN\_HIGH}$	Digital input low to high threshold	Threhold is independent of VIO. Input level > $V_{DIG\_IN\_HIGH}$ is detected as "logic-1"	1.84			V
14.1	$V_{DIG\_IN\_LOW}$	Digital input high to low threshold	Threshold is independent of VIO. Input level < $V_{DIG\_IN\_LOW}$ is detected as "logic-0".			0.76	V
14.2	$V_{DIG\_IN\_HYS}$	Digital input hysteresis (independent of VIO)		0.1			V
14.3	$V_{DIG\_OUT\_H-VIO}$	Digital output high level with respect to VIO	I_{OUT} = -2mA, VIO = 3.3V	3.1			V
14.4	$V_{DIG\_OUT\_LOW}$	Digital output low level (SPI SDO)	I_{OUT} = 2 mA			0.2	V
14.5	$R_{PD\_MCU\_ERROR}$	Internal pull-down resistor for MCU ERROR pin		30	70	110	kΩ
14.6a	$t_{MCU\_ERR\_PWM\_DEG}$	MCU ERROR pin deglitch time in PWM mode		10		14	µs
14.6b	$t_{MCU\_ERR\_TMS\_DEG}$	MCU ERROR pin deglitch time in TMS570 mode		3		5	µs

9.19 BUCK1, BUCK2, BOOST Thermal Shutdown / Over Temperature Protection Characteristics

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
15.0	T_{WARN_TH}	Thermal warning threshold	T_J rising	145		175	°C
15.1	$T_{WARN\_TH\_HYS}$	Thermal warning threshold hysteresis	T_J falling		10		°C
15.2	T_{STD_TH}	Thermal shutdown threshold	T_J rising	165		195	°C
15.3	$T_{STD\_TH\_HYS}$	Thermal shutdown threshold hysteresis	T_J falling		10		°C

9.19 BUCK1, BUCK2, BOOST Thermal Shutdown / Over Temperature Protection Characteristics (続き)

VIN/AVIN/VIN_SAFE = 4 V to 36 V, TA = -40°C to 125°C, TJ up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
15.4	t_{THERM_BLK}	Thermal detection blanking time	Applies to both thermal warning and thermal shutdown detection circuits.	60		80	µs

9.20 PGNDx Loss Detection Characteristics

VIN/AVIN/VIN_SAFE = 4 V to 36 V, T_A = -40°C to 125°C, T_J up to 150°C, unless otherwise noted.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16.0	V_{GLTH_LOW}	PGNDx loss threshold low	AGND to PGNDx	-0.35	-0.27	-0.18	V
16.1	V_{GLTH_HIGH}	PGNDx loss threshold high	AGND to PGNDx	0.18	0.27	0.35	V
16.2	t_{GL_BLK}	Blanking time between PGNDx loss condition and transition to SAFE state	The time from the start of PGNDx loss event until device transitions to SAFE state. It takes up to 5 system clock cycles from detection of valid PGNDx loss to device transition to SAFE state.	10		20	µs

9.21 SPI Timing Requirements

VIN/AVIN/VIN_SAFE = 4 V to 36 V, T_A = -40°C to 125°C, T_J up to 150°C, unless otherwise noted.(1)

POS	PARAMETER		MIN	NOM	MAX	UNIT
17.0	t_{SPI}	SCK period	125		1000	ns
17.1	$t_{(high)}$	SCK logic high duration	45			ns
17.2	$t_{(low)}$	SCK logic low duration	45			ns
17.3	$t_{su(cs)}$	NCS setup time (time between NCS falling edge and SCK rising edge)	45			ns
17.4	$t_{d(1)}$	Delay time (time delay from NCS falling edge to SDO transition from tri-state to 0)			30	ns
17.5	$t_{su(si)}$	SDI setup time before SCK falling edge	20			ns
17.6	$t_{d(2)}$	Delay time (time delay from SCK rising edge to valid SDO data)	0		70	ns
17.7	$t_{h(cs)}$	Hold time (time between SCK falling edge and NCS rising edge)	45			ns
17.8	$t_{hl(cs)}$	SPI transfer inactive time during which NCS remains high (time between two SPI transfers)	788			ns
17.9	t_{tri}	Tri-state time delay (time between NCS rising edge and SDO transitions to tri-state)			70	ns

(1) Capacitance at C_{SDO} = 100 pF

9.22 SPI Characteristics

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
17.10	R_{NCS_PU}	NCS internal pull-up to VIO		30	70	110	kΩ
17.11	$R_{SCK\_SDI\_PD}$	SCK and SDI internal pull-down		30	70	110	kΩ

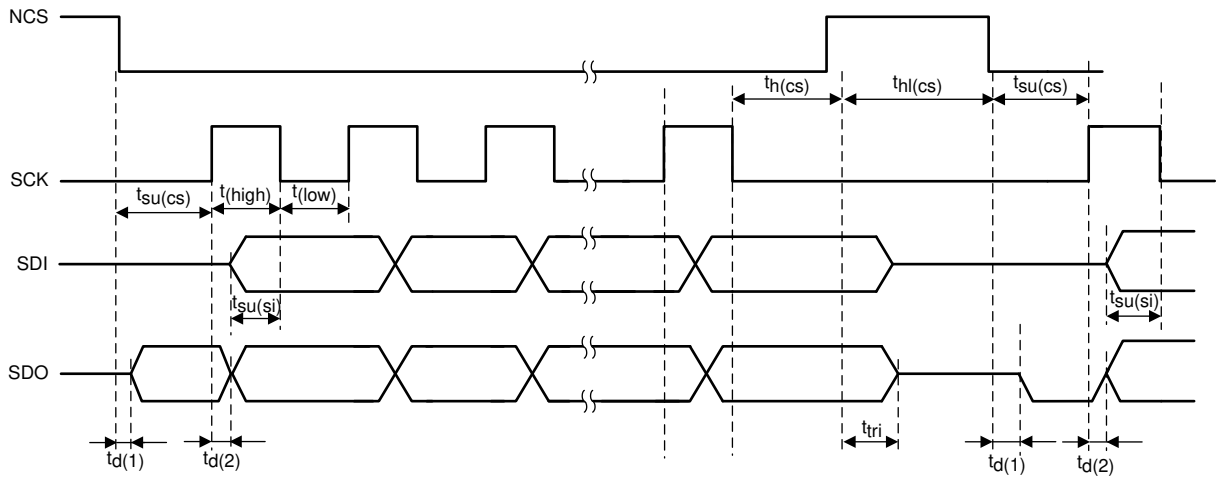
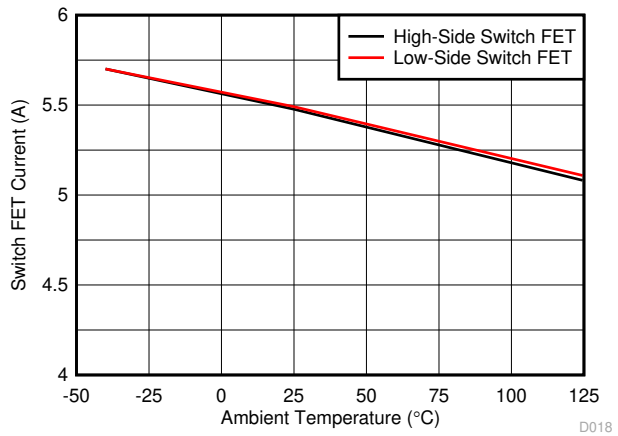


図 9-1. SPI Timing Parameters

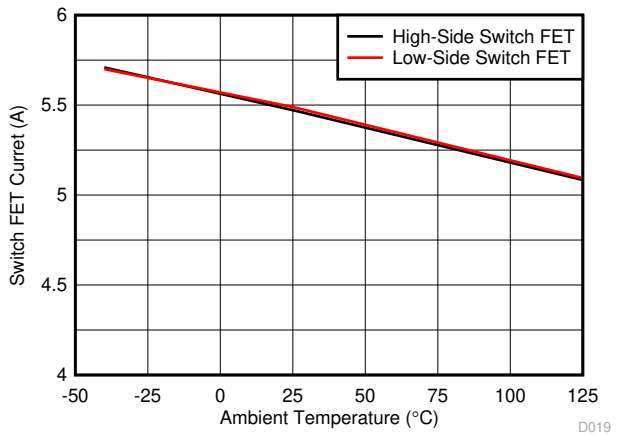
9.23 Typical Characteristics



注

V_{BUCK1} = 3.3 V　　V_{IN} = 6 V

図 9-2. BUCK1 Current Limit ($I_{HS\_SCG\_ILIM\_BUCK1}$ and $I_{LS\_SCG\_ILIM\_BUCK1}$)

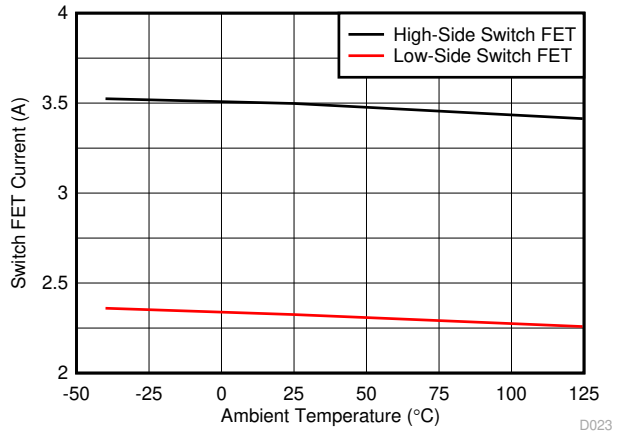


注

V_{BUCK1} = 3.6 V　　V_{IN} = 6 V

図 9-3. BUCK1 Current Limit ($I_{HS\_SCG\_ILIM\_BUCK1}$ and $I_{LS\_SCG\_ILIM\_BUCK1}$)

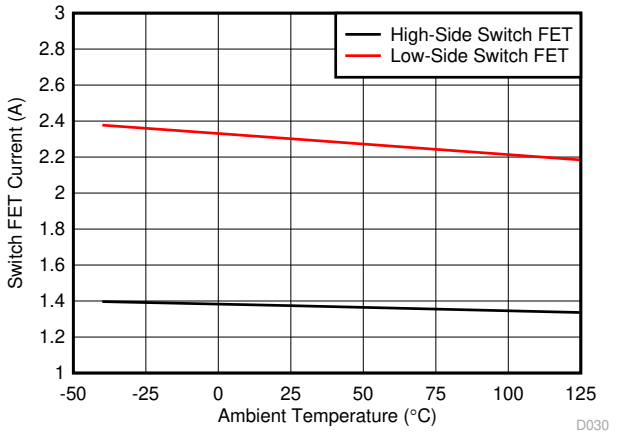
9.23 Typical Characteristics (continued)



注

V_{BUCK2} = 1.8 V　　V_{BUCK1} = 3.3 V

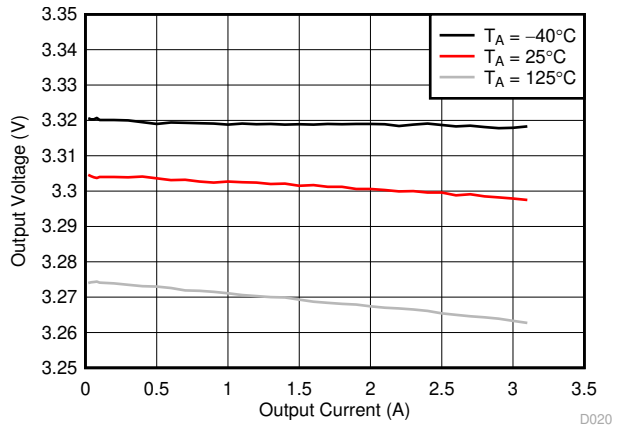
図 9-4. BUCK2 Current Limit ($I_{HS\_LIMIT\_BUCK2}$ and $I_{LS\_LIMIT\_BUCK2}$)



注

V_{BOOST} = 5 V　　V_{BUCK1} = 3.3 V

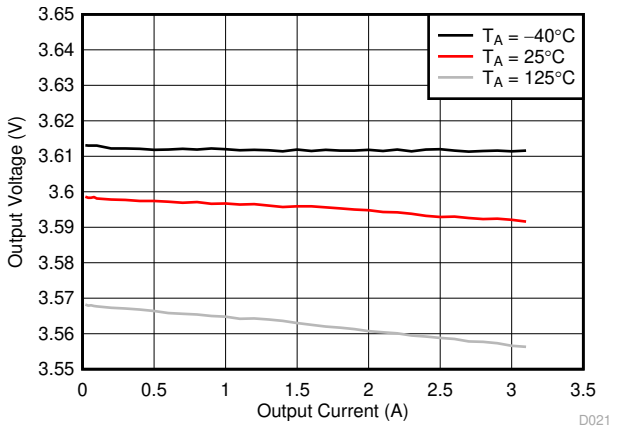
図 9-5. BOOST Current Limit ($I_{LS\_LIMIT\_BOOST}$ and $I_{HS\_LIMIT\_BOOST}$)



注

V_{BUCK1} = 3.3 V　　V_{IN} = 13 V

図 9-6. BUCK1 Output Voltage

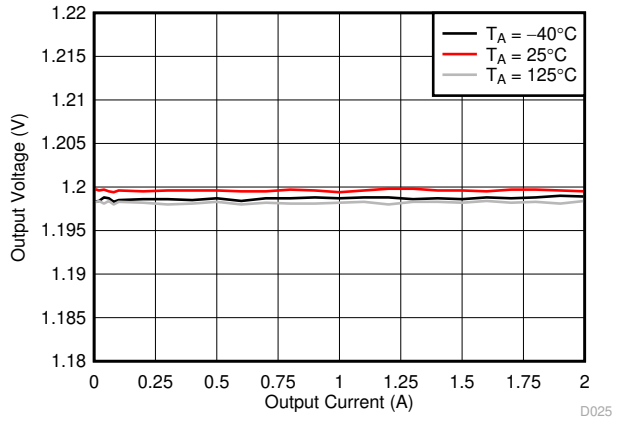


注

V_{BUCK1} = 3.6 V　　V_{IN} = 13 V

図 9-7. BUCK1 Output Voltage

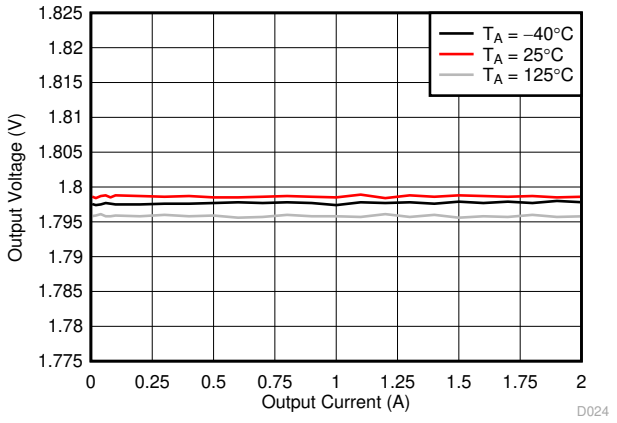
9.23 Typical Characteristics (continued)



注

V_{BUCK2} = 1.2 V　　V_{BUCK1} = 3.3 V

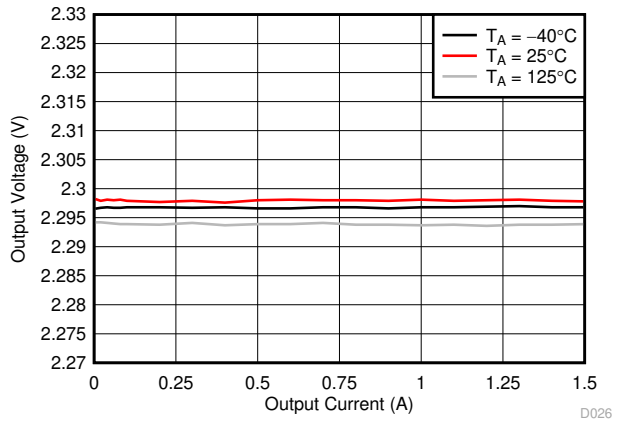
図 9-8. BUCK2 Output Voltage



注

V_{BUCK2} = 1.8 V　　V_{BUCK1} = 3.3 V

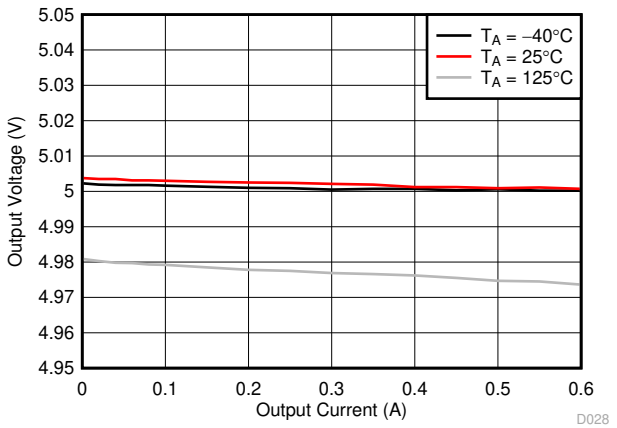
図 9-9. BUCK2 Output Voltage



注

V_{BUCK2} = 2.3 V　　V_{BUCK1} = 3.3 V

図 9-10. BUCK2 Output Voltage



注

V_{BOOST} = 5 V　　V_{BUCK1} = 3.3 V

図 9-11. BOOST Output Voltage

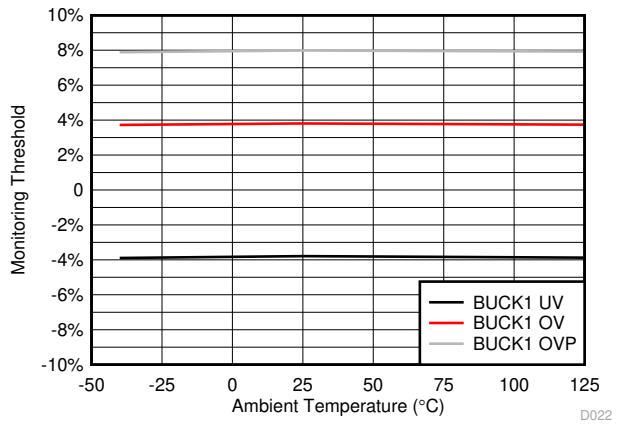


図 9-12. BUCK1 UV, OV, and OVP Threshold

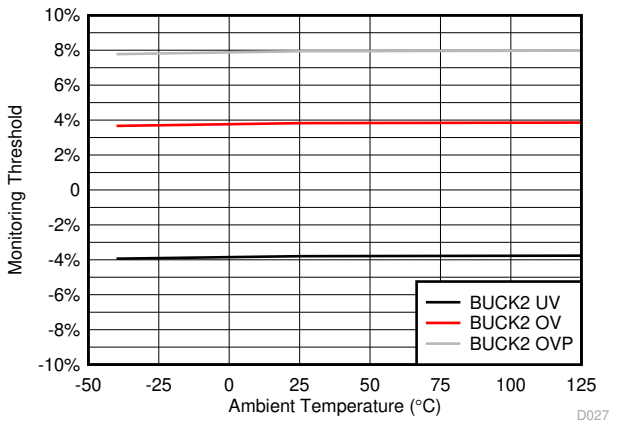


図 9-13. BUCK2 UV, OV, and OVP Threshold

9.23 Typical Characteristics (continued)

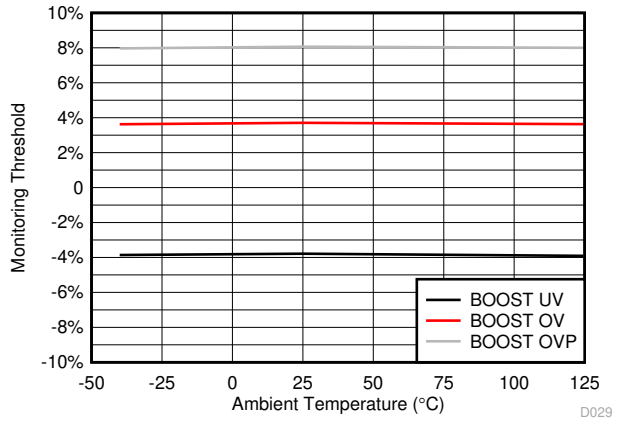


図 9-14. BOOST UV, OV, and OVP Threshold

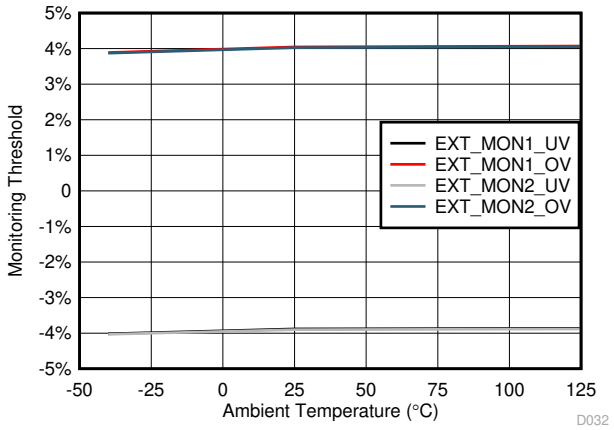


図 9-15. EXT_VMON1, EXT_VMON2 UV, and OV Threshold

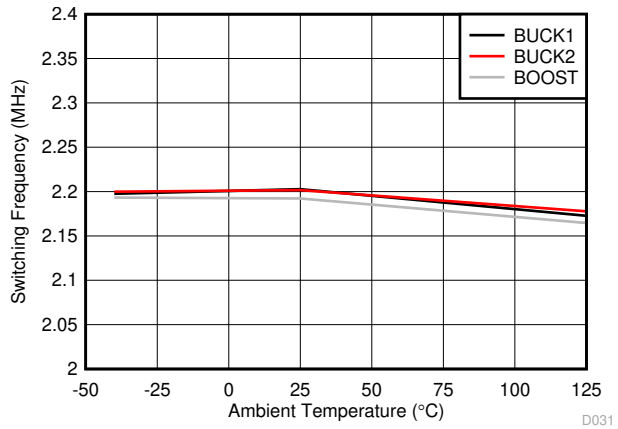


図 9-16. BUCK1, BUCK2, and BOOST Switching Frequency

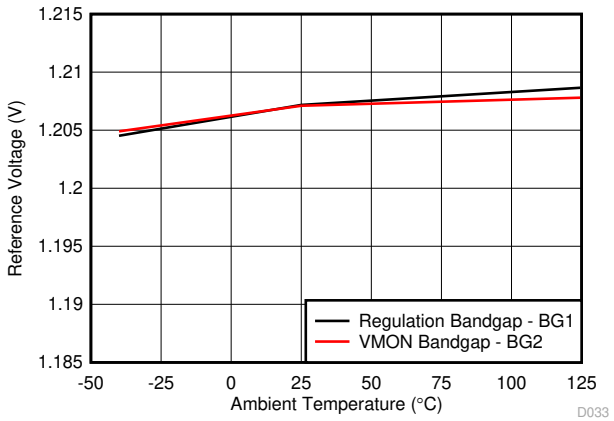


図 9-17. Regulation Bandgap (BG1) and Monitoring Bandgap (BG2)

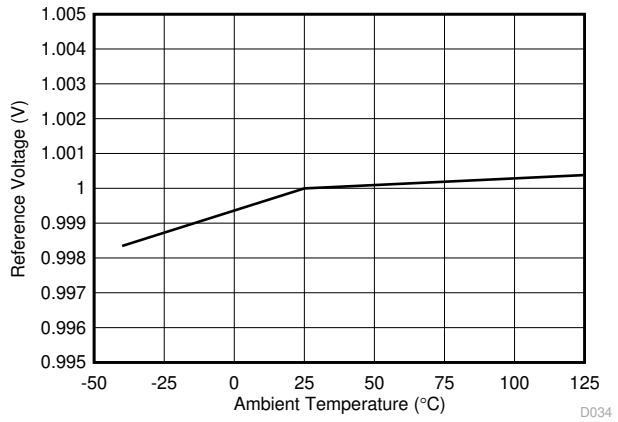


図 9-18. Voltage Monitoring Reference Voltage (V_{REF_MON})

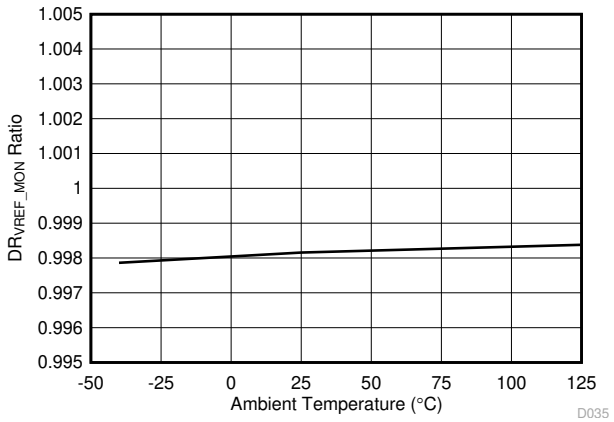


図 9-19. AMUX Output Division Ratio (DR_{VREF_MON})

9.23 Typical Characteristics (continued)

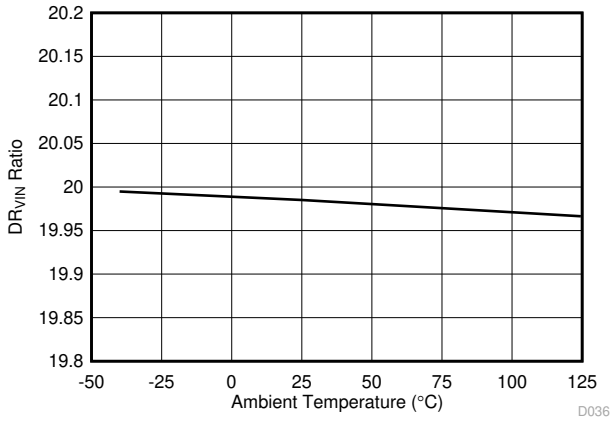


図 9-20. AMUX Output Division Ratio (DR_{VIN})

10 Parameter Measurement Information

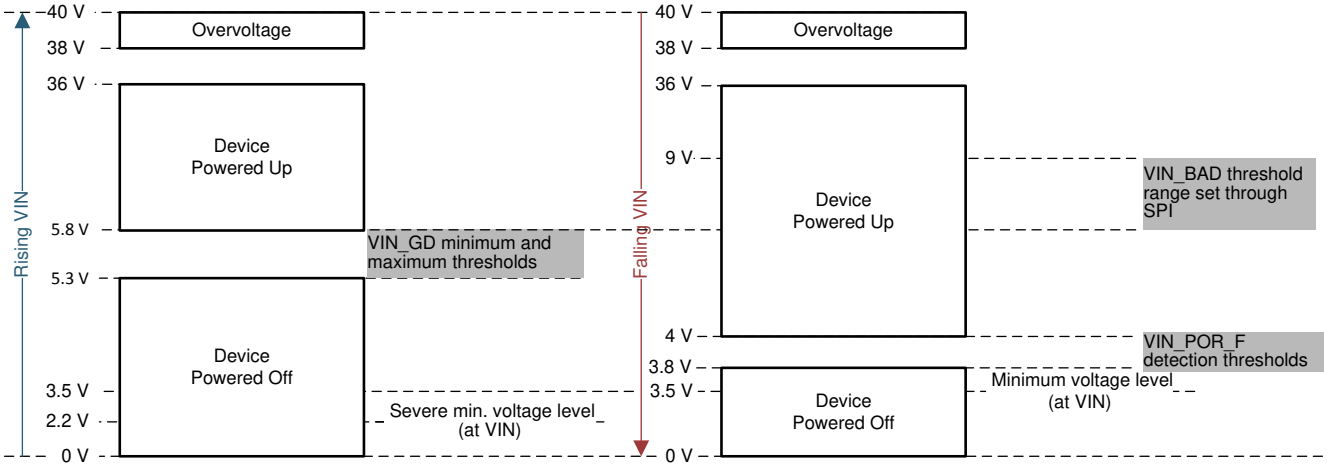


図 10-1. VIN Rising and Falling Ranges (With EXTSUP Supplied by VBOOST and V_{BUCK1} = 3.3 V)

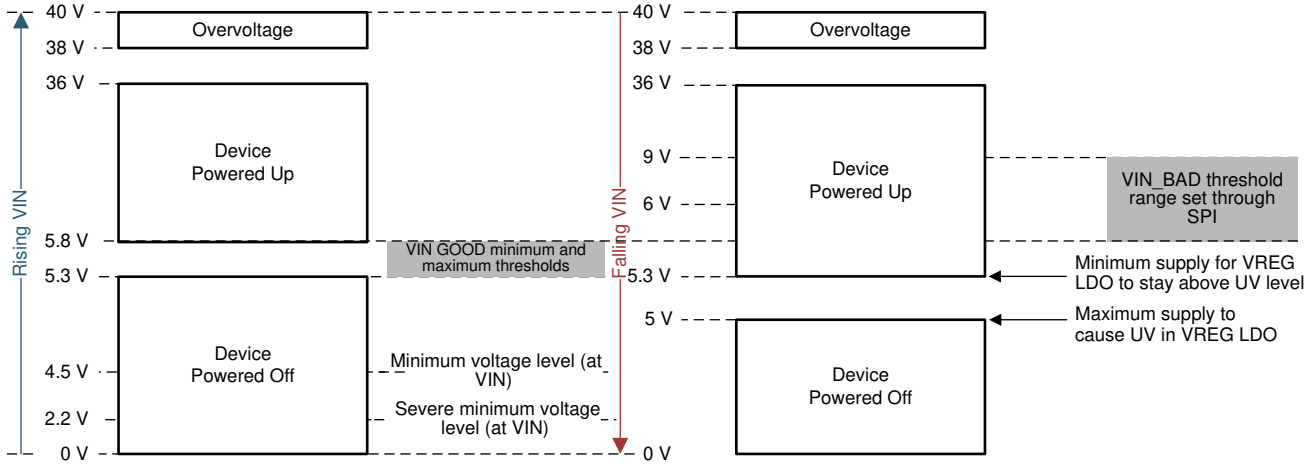


図 10-2. VIN Rising and Falling Ranges (With EXTSUP Not Present or Connected, and V_{BUCK1} = 3.3 V)

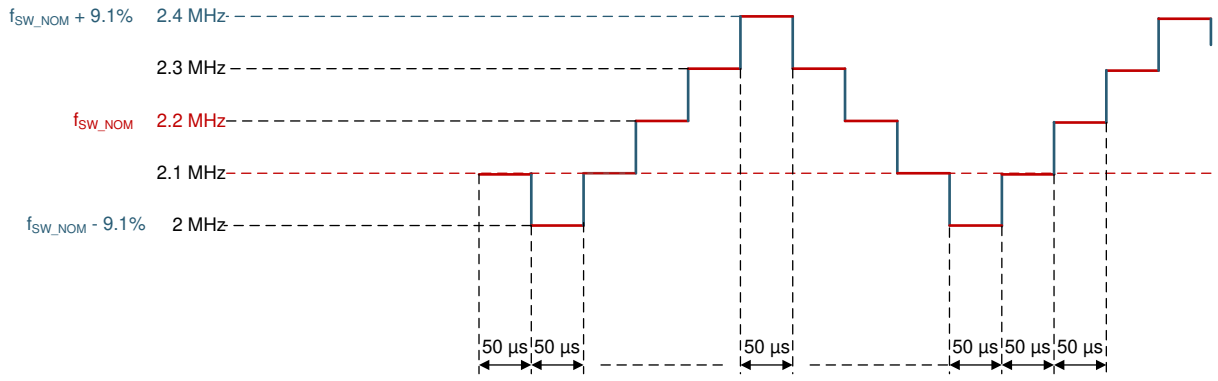


図 10-3. Modulated SYNC Input Clock (General Example With ±14% Variation and 100-kHz Steps)

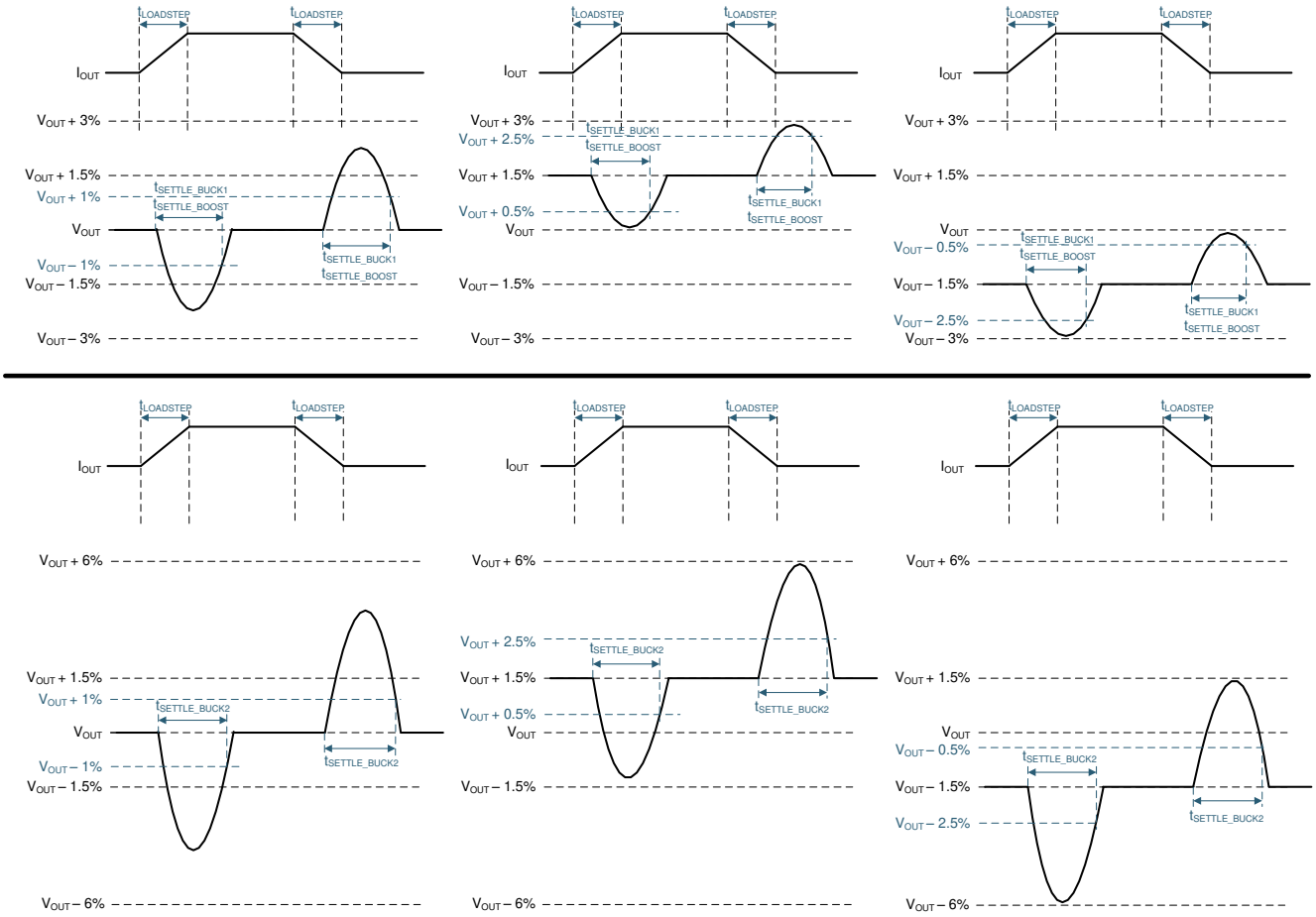


図 10-4. Regulator Load-Step Response

表 10-1. Regulator LC Selection

REGULATOR	PARAMETER	CFG1	CFG2	CFG3	CFG4	CFG5	CFG6	CGF7	CGF8
BUCK1	V_{OUT}	3.6 V	3.3 V	3.3 V	3.3 V	3.3 V	3.6 V	3.6 V	3.6 V
	L(1)	2.2 µH	2.2 µH	2.2 µH	2.2 µH	2.2 µH	2.2 µH	2.2 µH	2.2 µH
BUCK2	V_{OUT}	1.25 V	2.3 V	1.2 V	1.25 V	1.8 V	2.3 V	1.2 V	1.8 V
	L(1)	1.0 µH	1.0 µH	1.0 µH	1.0 µH	1.0 µH	1.0 µH	1.0 µH	1.0 µH
BOOST	V_{OUT}	5 V							
	L(1)	1.5 µH	1.5 µH	1.5 µH	1.5 µH	1.5 µH	1.5 µH	1.5 µH	1.5 µH
ALL	f_{SW}	2.2 MHz	2.2 MHz	2.2 MHz	2.2 MHz	2.2 MHz	2.2 MHz	2.2 MHz	2.2 MHz
	ESR_{MAX}	10 mΩ							
	C_{OUT_MIN} (2)	25 µF							
	C_{OUT_MAX} (2)	100 µF							
	C_{BOOTx_MIN}	100 nF							

(1) Inductor variation is ±30% (including 10% variation for standard component-value selection).
(2) The C_{OUT_MIN} and C_{OUT_MAX} parameters are the total capacitance values and proper capacitor selection must consider capacitor variation and derating.

11 Detailed Description

11.1 Overview

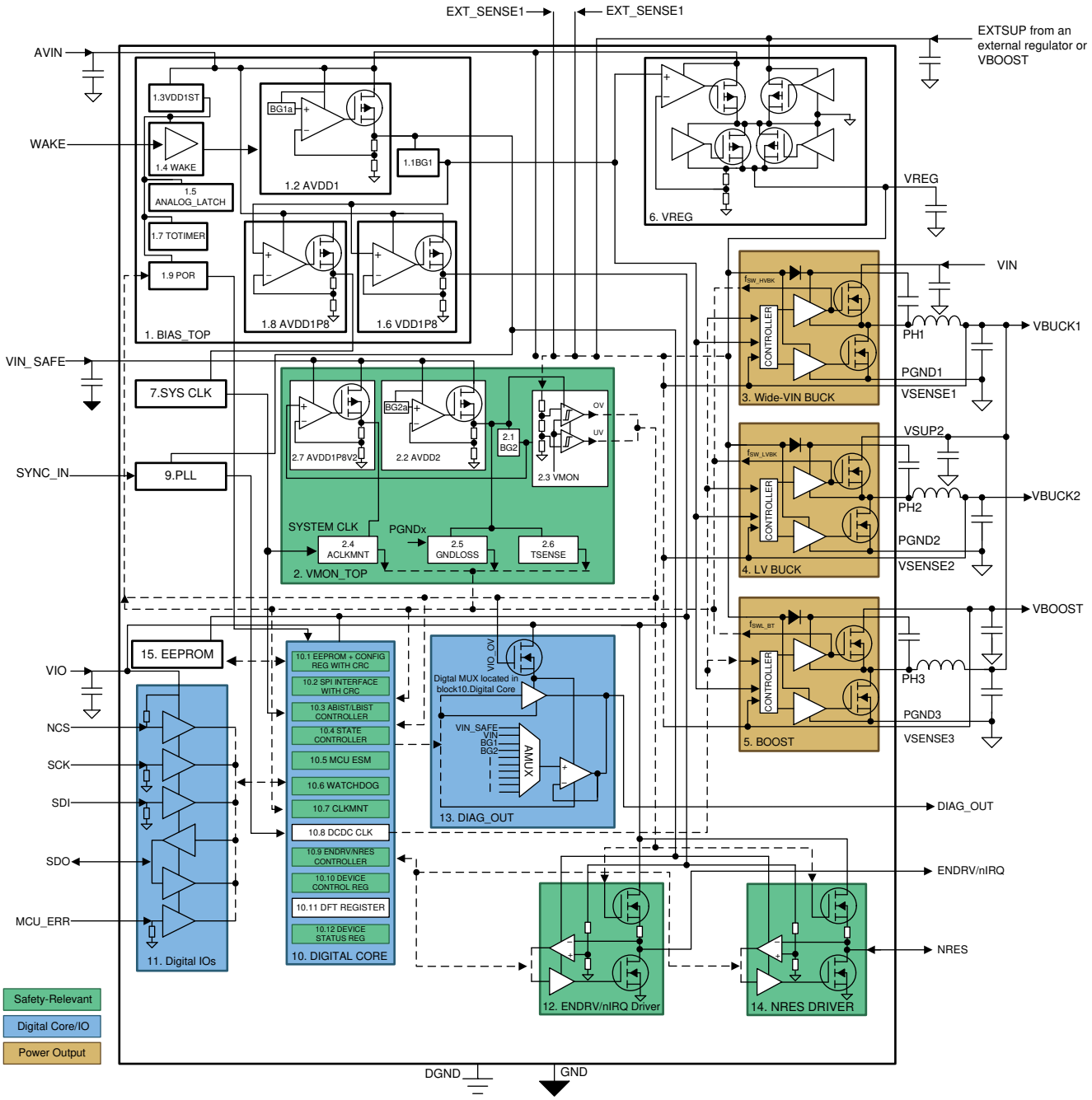
The TPS65313-Q1 device is a power management IC (PMIC), and meets the requirements of the MCU-controlled and DSP-controlled automotive systems (such as advanced driver assistance, industrial, machinery, and transportation systems). With its integration of commonly used features, it helps to significantly reduce board space and system costs.

The device includes one wide-VIN synchronous buck regulator that is connected to an input supply, one low-voltage buck regulator, and one low-voltage boost converter, which are powered by the wide-VIN buck regulator. The device has a minimum circuitry and monitors the WAKE pin for the device power-up, which reduces the current consumption in case the system is constantly connected to the supply line (like KL30 in case of automotive applications). All outputs are protected against overvoltage, overload, and overtemperature events.

An internal soft-start feature makes sure startup is controlled for all supplies.

All regulated supply outputs, along with supply monitoring and protection functions, fulfill up to ASIL-C system level requirements. The TPS65313-Q1 device also integrates programmable supervisor function, watchdog function, and MCU or DSP error pin monitors to detect malfunction of the system MCU or DSP.

11.2 Functional Block Diagram



11.3 Wide-VIN Buck Regulator (BUCK1)

11.3.1 Fixed-Frequency Voltage-Mode Step-Down Regulator

The BUCK1 regulator is a wide input-voltage range, low quiescent current, high performance regulator with internal compensation. This regulator is designed to minimize end-product cost and size while operating in demanding automotive, industrial, transportation, and heavy machinery environments. A fixed 2.2-MHz switching frequency allows the use of small passive components, and keeps the fundamental and higher harmonics greater than the AM band, which enables a simple input filtering scheme.

11.3.2 Operation

The BUCK1 regulator operates with a constant switching frequency even under light-load conditions. During low input-voltage and output-voltage conditions where the BUCK1 regulator must reduce the on-time or off-time to less than the specified minimum, the frequency is reduced to maintain the effective duty cycle required for regulation. This reduction can occur for light loads or for high input-voltage and output-voltage ratios. During high input-voltages greater than 28 V, the BUCK1 regulator can go to the pulse-skipping mode.

11.3.3 Voltage Monitoring (Monitoring and Protection)

The voltage-regulation loop regulates output voltage by maintaining the voltage on the VSENSE1 pin to be the same as the internal regulation-voltage reference. Two sets of independent programmable resistor-dividers are integrated; one for regulation loop and another one for under-voltage (UV), overvoltage (OV) and overvoltage protection (OVP) monitoring.

If the VSENSE1 pin is shorted to ground, the output voltage does not exceed the threshold level for BUCK1 overvoltage protection. Eventually, the BUCK1 regulator is disabled by setting the overvoltage-protection flag status bit.

11.3.4 Overcurrent Protection (Monitoring and Protection)

Currents through both the high-side (HS) power MOSFET and the low-side (LS) power MOSFET are continuously monitored to protect the internal power MOSFETs from damage. Current through each MOSFET is compared against two threshold levels ($I_{HS/LS\_SCG\_ILIM\_BUCK1}$ and $I_{HS/LS\_OVC\_LIM\_BUCK1}$). The former is to detect a short-circuit event and the latter is to detect an overload condition where the BUCK1 regulator is loaded with a current higher than what is specified.

If either the HS MOSFET current or the LS MOSFET current exceeds their respective overload current limits ($I_{HS\_OVC\_ILIM\_BUCK1}$ and $I_{LS\_OVC\_ILIM\_BUCK1}$) an overload event is detected and the BUCK1_OVC status bit is set in the SAFETY_BUCK1_STAT1 register; however, the regulator does not shut down. As the external inductor current continues to increase, and if either the HS MOSFET current or the LS MOSFET current exceeds their respective short-circuit current limit ($I_{HS\_SCG\_ILIM\_BUCK1}$ and $I_{LS\_SCG\_ILIM\_BUCK1}$), then the HS MOSFET is turned off immediately and the LS MOSFET is turned on, until the inductor current decreases to less than the overload threshold ($I_{LS\_OVC\_ILIM\_BUCK1}$). The BUCK1 regulator is then disabled and the BUCK1_SCG status bit is set in the SAFETY_BUCK1_STAT1 register. This double-sampling scheme allows for any overcurrent event to be detected either through a HS or LS MOSFET, especially when the BUCK1 regulator operates at a low duty cycle with a high input supply voltage. The BUCK1_SCG_OFF_EN configuration bit setting selects the device response after a short-circuit detection.

If the BUCK1_SCG_OFF_EN bit is set to 1b, the following occurs:

- The BUCK1 regulator, BUCK2 regulator, and BOOST converter are disabled, while enabling discharge through the internal resistor.
- The device goes into the OFF state.
- The BUCK1_SCG status bit is latched in the Analog_Latch (to preserve it) while the device is in the OFF state and presented to the system MCU during the next power-up event from the OFF state.

If the BUCK1_SCG_OFF_EN bit is set to 0b, the following occurs:

- The BUCK1 regulator, BUCK2 regulator, and BOOST converter are disabled, while disabling discharge through the internal resistor.
- The device goes into the SAFE state.
  - Eventually, as the BUCK1 regulator, BUCK2 regulator, and BOOST converter discharges to less than the UV threshold, a global RESET state condition is met, as long as one regulator UV event is configured as a RESET state event (as an example, the BUCK1_UV_RST_EN bit is set to 1b) and the device goes into the RESET state. When the device goes into the RESET state, the BUCK1 regulator is enabled again (its default value). After the BUCK1 output exceeds the UV threshold, the BUCK2 regulator is enabled, followed by the BOOST converter.

  - All the BUCK1 monitoring and protection mechanisms are active, and if any critical condition is still present, the BUCK1 regulator stays disabled. If the BUCK1 regulator never recovers while in the RESET state, the RESET state time-out event puts the device in the OFF state.
- The ENDRV/nIRQ pin is driven low.
- The device error counter increments.

The LS MOSFET is also protected by detection circuitry for cycle-by-cycle sink-current limit. This detection circuitry protects the LS MOSFET from excessive reverse current caused by switching the PH1 or PH1A pin to PGND1 or PGND1A. If the LS sinking current exceeds the $I_{LS\_SINK\_BUCK1}$ sink-current limit, an event is detected and the BUCK1_LS_SINK_OVC SPI status bit is set in the SAFETY_BUCK1_STAT1 register. If the event duration is longer than 20 µs (typical) the BUCK1 regulator is turned off. The inductor current continues to flow to the supply at the VIN pin through the body diode of the HS MOSFET. The BUCK1_LS_SINK_OVC_OFF_EN configuration bit setting selects the device response after the LS sink current-limit detection.

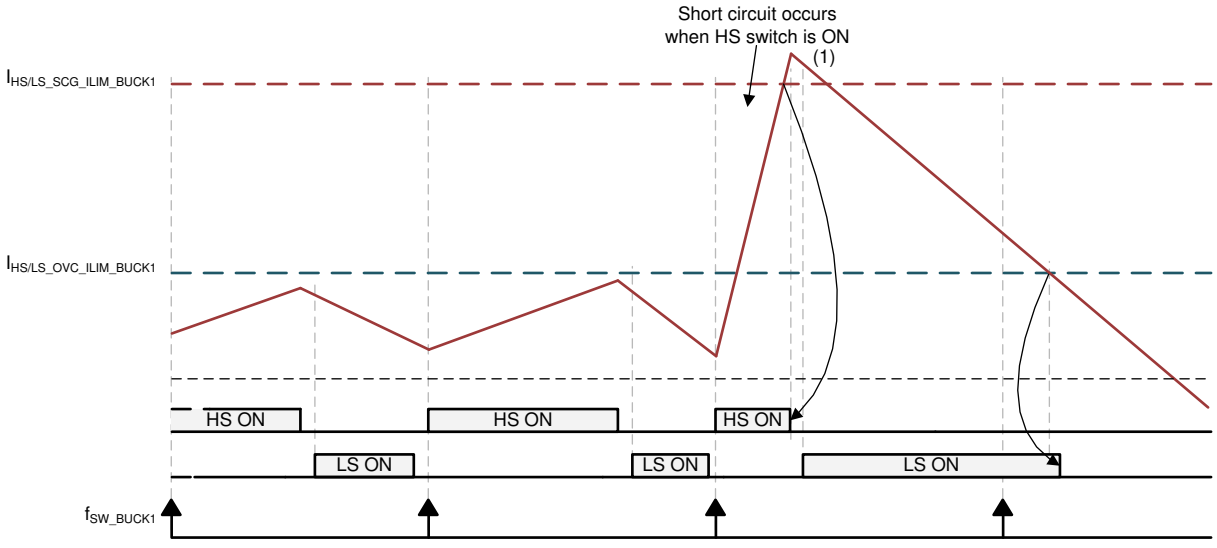
If the BUCK1_LS_SINK_OVC_OFF_EN bit is set to 1b, the following occurs:

- The device goes into the OFF state.
- The LS sink current limit of the BUCK1 regulator is latched in the Analog_Latch (to preserve it) while the device is in the OFF state and presented to the system MCU during the next power-up event from the OFF state.

If the BUCK1_LS_SINK_OVC_OFF_EN bit is set to 0b, the following occurs:

- The device goes into the SAFE state with all switched-mode regulators disabled and with the resistive discharge circuit disabled.
- The ENDRV/nIRQ pin is driven low to interrupt the system MCU.
- The device error counter increments.

The LS sink current-limit event can also be detected when the regulator is enabled and when its output has not been discharged to less than the voltage level defined by the $V_{BUCK1\_RESTART\_LEVEL}$ voltage. Therefore, the LS sink current-limit event is masked when the BUCK1 regulator is enabled, until the BUCK1 output voltage (V_{BUCK1}) exceeds its UV-threshold level.



1. When the BUCK1 load current continues to increase to greater than the maximum specified load, an UV event can occur.

図 11-1. The Wide-VIN BUCK1 Short-Circuit Event

11.3.5 Thermal Warning and Shutdown Protection (Monitoring and Protection)

Wide-VIN BUCK regulator integrates a dedicated thermal sense cell with thermal warning and shutdown thresholds. Thermal warning and shutdown are built-in monitoring and self-protection mechanisms that limit junction temperature and help prevent damage due to thermal overstress.

If the junction temperature exceeds the thermal warning level (T_{WARN_TH}), then the BUCK1_OT_WARN status bit is set. If the BUCK1_OT_WARN_IRQ_EN bit is set to 1b and if the ENDRV/nIRQ pin is driven high, then the ENDRV/nIRQ is driven low to interrupt the external MCU.

If the junction temperature exceeds the thermal shutdown level ($T_{STD\_TH\_R}$), the state of the device and BUCK1 regulator depends on the setting of the BUCK1_OT_OFF_EN configuration bit.

If the BUCK1_OT_OFF_EN bit is set to 1b, all of the following occurs:

- The device goes into the OFF state and all regulators are disabled.
- The BUCK1_OT_STD status bit is set and latched in the Analog_Latch, (to preserve it) while the device is in the OFF state, and is presented to the system MCU during the next power-up event from the OFF state.

If the BUCK1_OT_OFF_EN bit is set to 0b, all of the following occurs:

- The BUCK1_OT_STD status bit is set.
- The BUCK1 regulator, BUCK2 regulator, and BOOST converter are disabled, but the resistive discharge circuit is not enabled.
- The device goes into the SAFE state.

注

Eventually, as the BUCK1 regulator, BUCK2 regulator, and BOOST converter discharges to less than the UV threshold, a global RESET condition is met (as long as one regulator UV event is configured as a RESET event) and the device goes into the RESET state. When the device enters the RESET state, the BUCK1 regulator is enabled again (its default state). After the BUCK1 output exceeds its UV threshold, the BUCK2 regulator is enabled followed by the BOOST converter.

All the BUCK1 monitoring and protection mechanisms are active and, if any critical condition is still present, the BUCK1 regulator is disabled again. If the BUCK1 regulator never recovers while in the RESET state, the RESET state time-out event puts the device in the OFF state.

- The ENDRV/nIRQ pin is asserted low.
- The device error counter increments.

The junction temperature decreases after the BUCK1 regulator is disabled. In the OFF state, the junction temperature monitor is disabled to reduce power dissipation. The junction temperature monitor is enabled again after the device detects a valid wake-up event. The BUCK1 regulator (and the device) can be restarted only when the junction temperature decreases to less than $T_{WARN\_TH} - T_{WARN\_TH\_HYS}$.

The device error counter and its power-down threshold is a protection mechanism against multiple restarts caused by a persistent failure condition.

11.3.6 Overvoltage Protection (OVP) (Monitoring and Protection)

The BUCK1 overvoltage protection (OVP) is a built-in self-protection to limit the maximum output voltage of the BUCK1 regulator and protect external system peripherals supplied by the BUCK1 regulator. When a BUCK1 OVP condition is detected, the BUCK1_OVP_OFF_EN configuration bit setting selects the state of the device and BUCK1 regulator.

If the BUCK1_OVP_OFF_EN configuration bit is set to 1b, all of the following occurs:

- The device goes into the OFF state and all regulators are disabled.
- The BUCK1_OVP status bit is set and latched in the Analog_Latch to be preserved while the device is in the OFF state and presented to the system MCU during the next power-up event from the OFF state.

If the BUCK1_OVP_OFF_EN bit is set to 0b, all of the following occurs:

- The BUCK1 regulator is disabled.
- The device goes into the SAFE state.

注

As the BUCK1 output discharges to less than its UV threshold, a global RESET condition is met and the device eventually goes into the RESET state. When the device enters the RESET state, the BUCK1 regulator is enabled again (its default state). All the BUCK1 monitoring and protection mechanisms are active and, if any critical condition is still present, the BUCK1 regulator is disabled again. If the BUCK1 regulator never recovers while in the RESET state, the RESET state time-out event puts the device in the OFF state.

- The BUCK1 OVP status bit is set.
- The device error counter increments.
- The ENDRV/nIRQ pin is driven low.

The device error counter and its power-down threshold is a protection mechanism against multiple restarts caused by a persistent failure condition.

11.3.7 Extreme Overvoltage Protection (EOVP) (Monitoring and Protection)

The BUCK1 extreme overvoltage protection (EOVP) detects fast voltage increases that are caused by a fault, either internal or external, to the TPS65313-Q1 device. A built-in protection mechanism is implemented to protect the downstream switched-mode BUCK2 regulator and BOOST converter.

The thresholds is set at 4 V (with ±4% variation) regardless of the setting of the BUCK1 output voltage. When a BUCK1 EOVP condition is detected, the BUCK1 regulator, the BUCK2 regulator, and the BOOST converter are immediately disabled and the device goes into the OFF state.

11.4 Low-Voltage Buck Regulator (BUCK2)

11.4.1 Fixed-Frequency Peak-Current Mode Step-Down Regulator

The BUCK2 regulator is a low voltage, low quiescent current, and high performance regulator with internal compensation. The BUCK2 regulator is designed to reduce cost and size of the system while meeting requirements for demanding automotive, industrial, transportation, and heavy machinery environments. The operating switching frequency is fixed at 2.2 MHz. This regulator uses small passive components and reduces AM band noise filtering costs.

11.4.2 Operation

The BUCK2 regulator operates with a constant switching frequency under any load condition. Under low input-voltage and output-voltage conditions, where the BUCK2 regulator must decrease the on-time or off-time to less than the specified minimum, the switching frequency decreases to maintain the effective duty cycle required for regulation.

11.4.3 Output Voltage Monitoring (Monitoring and Protection)

The voltage-regulation loop regulates output voltage by maintaining the voltage on the VSENSE2 pin to be the same as the internal regulation-voltage reference. Two independent resistor dividers are integrated from the VSENSE2 pin to ground. One resistor divider is for the regulation loop and the other resistor divider is for output undervoltage (UV), overvoltage (OV) and overvoltage protection (OVP) monitoring.

If the VSENSE2 pin is shorted to ground, then the output voltage does not exceed the threshold level for BUCK2 overvoltage protection. Eventually, the BUCK2 regulator is disabled while the status bit for the BUCK2 overvoltage protection flag is set.

注

The comparator for BUCK2 overvoltage protection stays enabled even after the BUCK2 regulator is disabled. If the comparator still detects an overvoltage condition even after the BUCK2 regulator is disabled, then the BUCK1 regulator is disabled and the device goes into the OFF state.

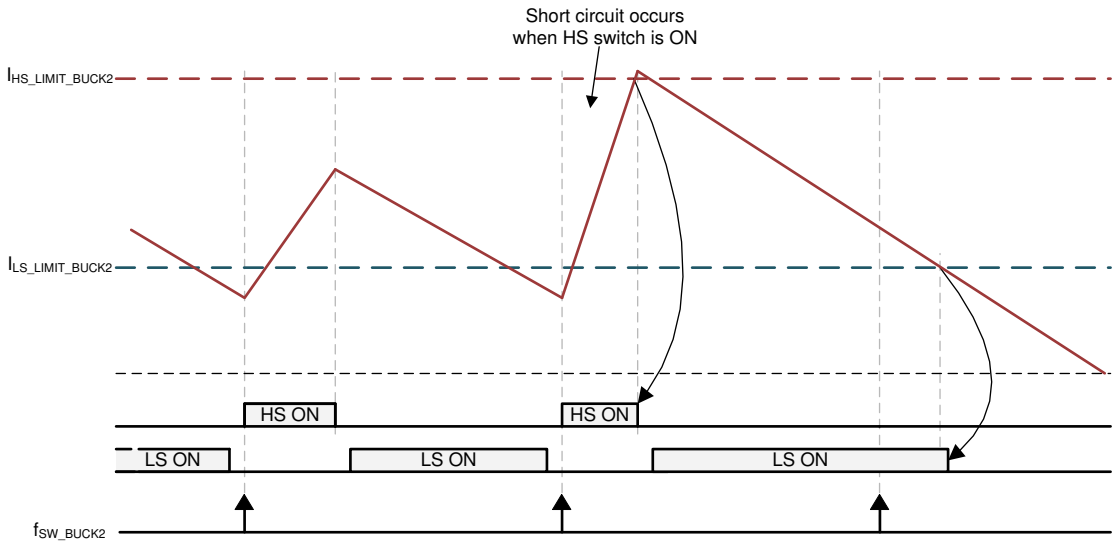
11.4.4 Overcurrent Protection (Monitoring and Protection)

Currents through both the high-side (HS) power MOSFET and the low-side (LS) power MOSFET are continuously monitored to protect the internal power MOSFETs from damage. Cycle-by-cycle currents through the HS MOSFET and LS MOSFET are compared against the $I_{HS\_LIMIT\_BUCK2}$ and $I_{LS\_LIMIT\_BUCK2}$ current limits, respectively. The former current limit is to detect short-circuit events and the latter is to detect overload conditions when the BUCK2 regulator load current exceeds the specified current limit threshold value.

As the load current increases to greater than the maximum I_{BUCK2_LOAD} current defined in セクション 9.8, the LS MOSFET current exceeds the $I_{LS\_LIMIT\_BUCK}$ current limit. Consequently, an overload event is detected and the BUCK2_LS_OVC status bit is set in the SAFETY_BUCK2_STAT1 register. However, the regulator does not shut down. If the load current continues to increase, the HS-MOSFET current exceeds the short-circuit current limit ($I_{HS\_LIMIT\_BUCK}$). The HS MOSFET is turned off immediately and the LS MOSFET is turned on until the inductor current drops to less than the overload threshold value ($I_{LS\_LIMIT\_BUCK2}$). The BUCK2 regulator is then disabled and the BUCK2_HS_OVC (BUCK2_SCG) status bit is set in the SAFETY_BUCK2_STAT1 register. The BUCK2_EN control bit is cleared and the device does not change the state, if the BUCK2_UV_RST_EN bit is 0b. If the BUCK2_UV_RST_EN bit is set to 1b (BUCK2 UV event configured as a RESET state event), as the V_{BUCK2} voltage rail is discharged to less than its UV-threshold level, then the device goes into the RESET state.

The LS MOSFET is also protected by detection circuitry for cycle-by-cycle sink-current limit. This detection circuitry protects the LS MOSFET from excessive reverse current caused by switching the PH2 pin to the PGND2 pin. If the LS sinking current exceeds the $I_{LS\_SINK\_BUCK2}$ sink-current limit, an event is detected and the BUCK2_LS_SINK_OVC SPI status bit is set in the SAFETY_BUCK2_STAT1 register. If the event occurs for more than 20 µs (typical), the BUCK2 regulator is turned off. The inductor current continues to flow to the supply at the VSUP2 pin through the body diode of the HS MOSFET. The device response after detection of a LS sink-current limit is identical to that of a short-circuit event.

The LS sink current-limit event can also be detected when the regulator is enabled while the V_{BUCK2} voltage rail has not been discharged to less than the voltage level defined by the $V_{BUCK2\_RESTART\_LEVEL}$ level. Therefore, the LS sink current-limit event is masked when the BUCK2 regulator is enabled, and until the V_{BUCK2} voltage rail exceeds its UV-threshold level.



1. When the BUCK2 load current continues to increase to greater than the IBUCK2_LOAD maximum value, an UV event can occur.

図 11-2. The BUCK2 Short-Circuit Event

11.4.5 Thermal Sensor Warning and Thermal Shutdown Protection (Monitoring and Protection)

The BUCK2 regulator integrates a dedicated thermal sense cell with thermal warning and shutdown thresholds. Thermal warning and shutdown are built-in monitoring and self-protection mechanisms to limit junction temperature and help prevent damage due to thermal overstress.

If the junction temperature exceeds the thermal warning threshold level (T_{WARN_TH}), the BUCK2_OT_WARN status bit is set and the ENDRV/nIRQ pin is driven low to interrupt the external MCU, if the BUCK2_OT_WARN_IRQ_EN bit is set to 1b.

If the junction temperature exceeds the thermal shut-down threshold level (T_{STD_TH}), the results are as follows:

- The device goes into the SAFE state.
- The BUCK2 regulator is switched off.

注

The device goes into the RESET state as the BUCK2 output discharges to less than its UV-threshold level, if the BUCK2 UV event is configured as a RESET state condition (the BUCK2_UV_RST_EN bit is set to 1b).

- The BUCK2_EN control bit is cleared.
- The BUCK2_OT_STD status bit is set.
- The device error counter (DEV_ERR_CNT) increments.
- The ENDRV/nIRQ output is driven low.

After receiving an interrupt (the ENDRV/nIRQ pin is driven low), the system MCU can try to enable the BUCK2 regulator again by setting the BUCK2_EN control bit. However, the BUCK2 regulator stays disabled until the junction temperature decreases to less than the $T_{WARN\_TH} - T_{WARN\_TH\_HYS}$ threshold, while the BUCK2_EN control bit stays set.

The device error counter and its power-down threshold is a protection mechanism that protects against multiple repeats caused by a persistent failure condition.

11.4.6 Overvoltage Protection (OVP) (Monitoring and Protection)

Overvoltage protection is a built-in self-protection to limit the BUCK2 maximum output voltage and help protect external peripherals.

If the BUCK2 output voltage exceeds the OVP threshold level, the results are as follows:

- The device goes into the SAFE state.
- The BUCK2 regulator is shut-down.

注

The device goes into the RESET state as the BUCK2 output discharges to less than its UV-threshold level, if the BUCK2 UV event is configured as a RESET state condition (the BUCK2_UV_RST_EN bit is set to 1b).

- The BUCK2_EN control bit is cleared.
- The BUCK2_OVP status bit is set.
- The device error counter (DEV_ERR_CNT) increments.
- The ENDRV/nIRQ pin is driven low.

The MCU can try to enable the BUCK2 regulator again by setting the BUCK2_EN control bit after receiving an interrupt (the ENDRV/nIRQ pin is driven low), and after the BUCK2 output voltage discharges. To re-enable the BUCK2 regulator the MCU must send a SPI command to clear the CTRL_LOCK bit and set the BUCK2_EN control bit.

The device error counter and its power-down threshold are protections against multiple repeats caused by a persistent failure condition.

The OVP monitoring stays active even when the BUCK2 regulator is disabled. If a BUCK2 overvoltage condition is still detected for the $t_{BUCK2\_OVP\_OFF}$ duration, after the BUCK2 regulator is disabled, then the device enters the OFF state and the BUCK2_OVP status bit is latched in the Analog_Latch.

11.5 Low-Voltage Boost Converter (BOOST)

The BOOST converter is a synchronous converter with a fixed frequency and current-mode PWM control for exceptional line and load regulation. The PWM switching frequency is 2.2 MHz. The BOOST converter has its own enable bit (the BOOST_EN control bit in the PWR_CTRL control register). By default, this bit is enabled at power-up, and can be disabled after power-up by the MCU.

The output voltage of the BOOST converter is fixed at 5 V. At low loads, the boost converter stays in the fixed-frequency mode.

The BOOST converter integrates circuitry to provide a closed-loop soft-start operation. The BOOST output voltage initially starts to ramp with wide-vin BUCK1 ramp rate. Once wide-vin BUCK1 output voltage completes its ramp-up, the BOOST starts its soft-start. The soft-start circuit uses a linear increase of the internal reference voltage from 0 V to its nominal value. This linear increase occurs in 2 ms while the internal control loop drives the V_{BOOST} voltage from 0 V to 5 V, limits the inrush current drawn by the external load, and prevents the soft-start from being affected by the size of the output capacitor or the output regulation voltage. The soft-start interval is reset by a shutdown event (the WAKE pin driven low or global transition the OFF state condition).

When the BOOST converter is disabled while the BUCK1 regulator stays enabled, the BOOST output voltage is not 0 V, because it is connected to the input supply (essentially, the BUCK1 output) through the body diode of the HS power MOSFET.

11.5.1 Output Voltage Monitoring (Monitoring and Protection)

The output voltage of the BOOST converter is continuously monitored by an independent voltage-monitoring circuit, which compares the voltage against an independent band gap reference. The respective BOOST status bit is set to detected a valid BOOST Under-Voltage (UV) event, Over-Voltage (OV) event, or Over-Voltage Protection (OVP) event.

11.5.2 Overcurrent Protection (Monitoring and Protection)

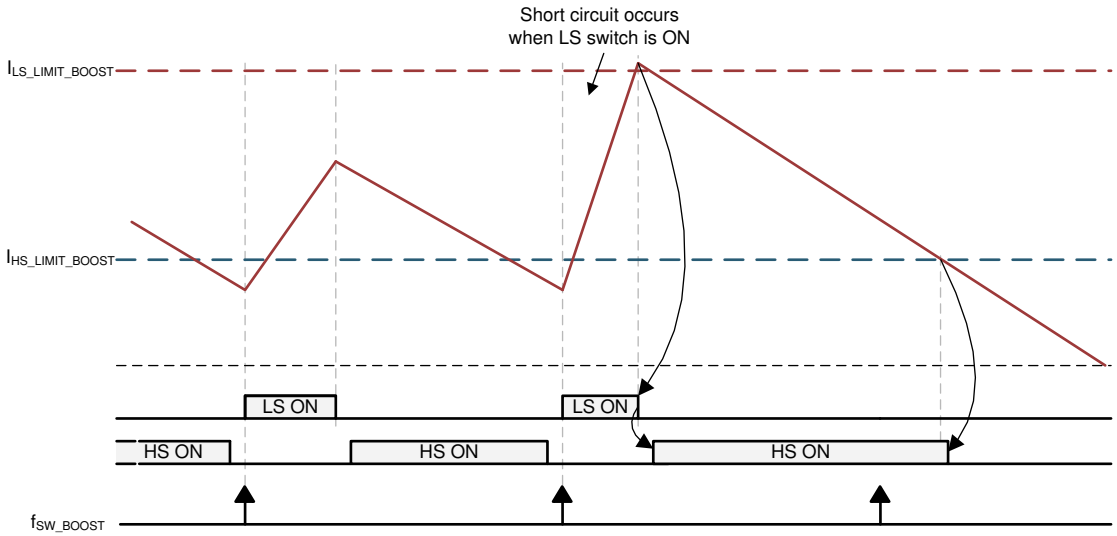
The currents through the high-side (HS) power MOSFET and the low-side (LS) power MOSFET are continuously monitored to protect the internal MOSFETs from damage. Cycle-by-cycle currents through the HS MOSFET and LS MOSFET are compared against the $I_{HS\_LIMIT\_BOOST}$ and $I_{LS\_LIMIT\_BOOST}$ current limits, respectively.

As load current increases to greater than the maximum I_{BOOST_LOAD} current defined in セクション 9.9, the HS MOSFET current exceeds the $I_{HS\_LIMIT\_BOOST}$ current limit. Consequently, an overload event is detected and the BOOST_HS_OVC status bit is set in the SAFETY_BOOST_STAT1 register. However, the regulator does not shut down. If the load current continues to increase, the LS MOSFET current exceeds the short-circuit current limit ($I_{LS\_LIMIT\_BOOST}$). The LS MOSFET is turned off immediately and the HS MOSFET is turned on until the inductor current decreases to less than the overload threshold ($I_{HS\_LIMIT\_BOOST}$). The BOOST converter is then disabled and the BOOST_SCG status bit is set in the SAFETY_BOOST_STAT1 register. The BOOST_EN control bit is cleared and the device goes into the SAFE state, where the device error counter increments and the ENDRV/nIRQ pin is driven low. If the BOOT_UV_RST_EN bit is set to 1b (BOOST UV event configured as RESET state condition), as the V_{BOOST} voltage rail is discharged to less than its UV-threshold level, the device goes into the RESET state.

The HS MOSFET is also protected by detection circuitry for a cycle-by-cycle sink-current limit. This detection circuitry protects the HS MOSFET from excessive reverse current caused by switching the PH3 pin to the VSUP2 supply pin. If the HS sinking current exceeds the $I_{CL\_HS\_SINK\_BOOST}$ sink-current limit, an event is detected and the BOOST_HS_SINK_OVC SPI status bit is set in the SAFETY_BOOST_STAT1 register. If the event occurs for more than 20 µs (typical), the BOOST converter is turned off. The inductor current continues to flow to the supply (V_{BUCK1} voltage rail) through the body diode of the LS MOSFET. The device response after detection of a HS sink-current limit is identical to that of a short-circuit event.

The HS sink current-limit event can also be detected when the regulator is enabled while its output has not been discharged to less than the voltage level defined by the $V_{BOOST\_RESTART\_LEVEL}$ level. Therefore, the HS sink current-limit event is masked when the BOOST converter is enabled until it the output voltage ramps to greater than its UV-threshold level.

After receiving an interrupt, the MCU can try to enable the BOOST converter again by sending command to set the BOOST_EN control bit. If a current-limit condition is still present, the BOOST converter is switched off again and the device error counter increments.



1. When the BOOST load current continues to increase to greater than the IBOOST_LOAD maximum value, an UV event can occur.

図 11-3. BOOST Short-Circuit Event

11.5.3 Thermal Sensor Warning and Shutdown Protection (Monitoring and Protection)

The BOOST converter integrates a dedicated thermal sense cell with thermal warning and shutdown thresholds. Thermal warning and shutdown are built-in monitoring and self-protection mechanisms that limit junction temperature and help prevent damage due to thermal overstress.

If the junction temperature exceeds the thermal warning level (T_{WARN_TH}), the BOOST_OT_WARN status bit is set. Also, if the ENDRV/nIRQ pin is high, then the ENDRV/nIRQ pin is driven low to interrupt the external MCU, if the BOOST_OT_WARN_IRQ_EN bit has been set to 1b.

If the junction temperature exceeds the thermal shut-down level (T_{STD_TH}), the results are as follows:

- The device goes into the SAFE state.
- The BOOST is switched off.

注

The device goes into the RESET state as the BOOST output discharges to less than its UV-threshold level, if the BOOST UV event is configured as RESET state condition (the BOOST_UV_RST_EN bit is set to 1b).

- The BOST_EN control bit is cleared.
- The BOOST_OT_STD status bit is set.
- The device error counter (DEV_ERR_CNT) increments.
- The ENDRV/nIRQ output is driven low.

The system MCU can try to enable the BOOST converter again by setting the BOOST_EN control bit, after receiving an interrupt when ENDRV/nIRQ pin toggles from high to low. However, the BOOST converter stays disabled until the junction temperature decreases to less than the $T_{WARN\_TH} - T_{WARN\_TH\_HYS}$ threshold, and while the BOOST_EN control bit stays set. To re-enable the BOOST converter, the MCU must send a SPI command to clear the CTRL_LOCK bit and set the BOOST_EN control bit.

11.5.4 Overvoltage Protection (OVP) (Monitoring and Protection)

Overvoltage protection is a built-in self-protection mechanism that limits the BOOST maximum output voltage and helps protect the external components powered by the BOOST converter. When the BOOST output voltage exceeds the set overvoltage protection-threshold level, the results are as follows:

- The device goes into the SAFE state.
- The BOOST is shut-down.

注

The device goes into the RESET state as the BOOST output discharges to less than the UV-threshold level, if the BOOST UV event is configured as RESET state condition (the BOOST_UV_RST_EN bit is set to 1b).

- The BOOST_EN control bit is cleared.
- The BOOST_OVP status bit is set.
- The device error counter (DEV_ERR_CNT) increments.
- The ENDRV/nIRQ pin is driven low.

The MCU can try to enable the BOOST converter again by setting the BOOST_EN control bit, after receiving an interrupt when the ENDRV/nIRQ pin toggles from high to low, and if the BOOST output voltage has discharged below the $V_{BOOST\_RESTART\_LEVEL}$. The OVP monitoring stays active even when the BOOST converter is disabled. If the BOOST overvoltage condition is still detected for $t_{BOOST\_OVP\_OFF}$ time after the BOOST converter is disabled, then the device goes into the OFF state and the BOOST_OVP status bit is set and latched in the Analog_Latch.

11.6 VREG Regulator

The switched-mode regulators internal power MOSFETs gate drivers are supplied by the VREG internal linear regulator. The VREG regulator operates either in regulated LDO mode or in unregulated switch mode, depending on the availability of an external supply at the EXTSUP pin. The internal linear-regulator output at the VREG pin should be decoupled to ground using a 2.2-µF (typical) ceramic capacitor. This pin has internal current-limit protection in regulated LDO mode only and must not be used to power any other circuit.

The VREG regulator is powered from the AVIN pin by default when the EXTSUP voltage is less than 4.7 V (typical value with the V_{EXTSUP} voltage rising). If the VIN pin is expected to be at high voltage levels, excessive power dissipation can occur in this regulator. In this case, TI recommends powering the VREG regulator from the EXTSUP pin, which can be connected to a 5-V power-supply source. When the EXTSUP pin is connected to a power-supply source that has a sufficiently high voltage, the VREG regulator is automatically switched off and an alternative path with a linear pass switch from the EXTSUP pin to the VREG pin is turned on to improve efficiency. 5.25 V is the maximum voltage that must be applied to the EXTSUP pin. The source for the EXTSUP pin can be the BOOST output voltage.

In case of the VREG undervoltage event, the following occurs:

- All switched-mode regulators are disabled.
- The device goes into the OFF state.
- The VREG_UV bit is latched in the Analog_Latch.

In case of the VREG overvoltage event, the following occurs:

- All switched-mode regulators are disabled.
- The device goes into the OFF state.
- The VREG_OV bit is latched in the Analog_Latch.

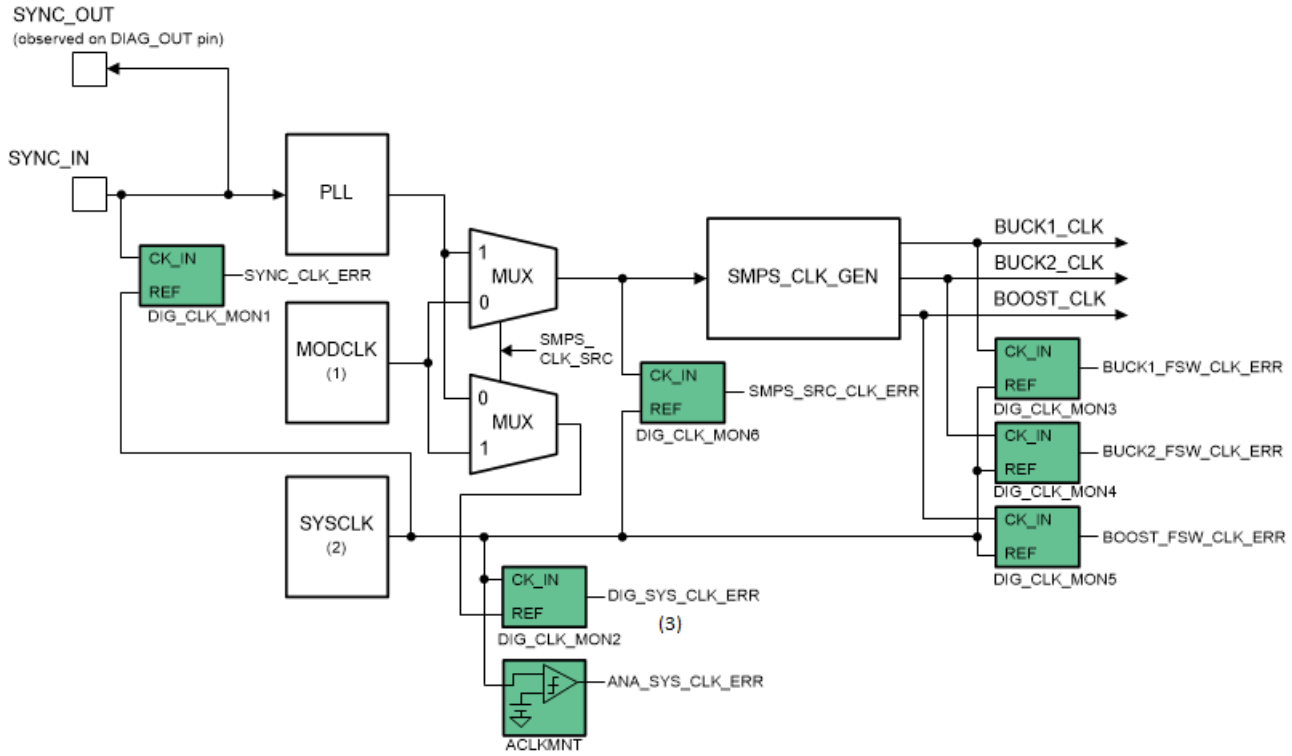
11.7 BUCK1, BUCK2, and BOOST Switching Clocks and Synchronization (SYNC_IN) Clock

The integrated phase-locked loop (PLL) allows the device to synchronize the switched-mode regulator clocks to an external SYNC_IN input clock to help reduce EMI. When the TPS65313-Q1 device powers up, the device monitors the SYNC_IN pin for the presence of recurring clock edges. If the device detects activity on the SYNC_IN pin, the clock for the switched-mode regulators is derived from the external SYNC_IN clock. If the device does not detect any activity on the SYNC_IN pin, then the switched-mode regulators get a clock from the free-running VCO clock in the PLL.

When the system initially powers up without an external clock present at the SYNC_IN pin, the device enables the switched-mode regulators with the clock derived from the free-running VCO clock in the PLL. The device switches to an external clock source present at the SYNC_IN pin when the system powers up. The start of the regulator switching cycle is synchronized to the falling edge of the input clock at the SYNC_IN pin. If a loss-of-external clock event is detected, the clock source is switched to the free-running VCO clock to continue to regulate the output voltages.

An external clock should be connected to the SYNC_IN pin with a proper high-speed termination to avoid excessive ringing. The requirements on the external clock are as follows:

- A high-level voltage that is not lower than 2 V.
- A low-level voltage that is not higher than 0.4 V.
- A duty cycle that is from 10% to 90%.
- Both a positive and negative pulse width that are not shorter than 80 ns.



1. MODCLK: Internal spread spectrum modulated clock source for switching regulators.
2. SYSCLK: Internal system clock source.
3. DIG_SYSCLK_ERR / DIG_CLK_MON2 error / fault reaction by the device state machine is masked/disabled in device EEPROM and this has no impact to device overall functionality. However, if the fault is detected by this clock monitor, DIG_SYS_CLK_ERR and SYSCLK_ERR status bit will be still set and should be ignored.

図 11-4. Device Clock Tree and Monitors

11.7.1 Internal f_{SW} Clock Configuration (f_{SW} Derived from an Internal Oscillator)

If a digital clock-monitor warning is detected, the response depends on the CLK_WARN_RESP_EN configuration bit setting as follows:

- If the CLK_WARN_RESP_EN configuration bit is set to 1b, the following occurs:
  - The respective clock warning status bit is set in the SAFETY_CLK_WARN_STAT register.
  - The device goes into the SAFE state.
  - All switched-mode regulators stay enabled.
  - The device error counter increments.
  - The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.
- If the CLK_WARN_RESP_EN configuration bit is set to 0b, the following occurs:
  - The respective clock warning status bit is set in the SAFETY_CLK_WARN_STAT register.
  - The device does not change the state.
  - A software interrupt is set through the SPI status bit (STAT[3]) in response to the status word, and the bit stays set until the respective clock-error status bit is cleared.

11.7.2 BUCK1 Switching Clock-Monitor Error (Internal f_{SW} Clock Configuration)

In any of the operating states (RESET, DIAGNOSTIC, ACTIVE, or SAFE), if the BUCK1 switching-clock error is detected, and while the internal OSC clock source is in good condition, the following occurs:

- The BUCK1_FSW_CLK_ERR status bit is set.
- The BUCK1 regulator, BUCK2 regulator, and BOOST converter are disabled, but without enabling resistive discharge.

- The device goes into the SAFE state.
- The device error counter increments.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

As rails discharge to less than the respective UV-threshold levels, the device enters the RESET state. While the device is in the RESET state, the switched-mode regulators can be enabled by the internal start-up control circuit, only when the internal OSC clock monitor and the respective f_{SW} clocks are in good condition, or when the BUCK1 regulator, the BUCK2 regulator, and the BOOST converter discharges to less than the corresponding restart voltage level ($V_{BUCK1\_RESTART\_LEVEL}$, $V_{BUCK2\_RESTART\_LEVEL}$, and $V_{BOOST\_RESTART\_LEVEL}$).

At least one UV event and one switched-mode regulator must be set as a RESET condition, otherwise the device can be locked in the SAFE state when the SAFE state time-out event is disabled (the SAFE_TO_DIS bit is set to 1b). After the BUCK1 regulator is enabled and the BUCK1 output exceeds its UV-threshold level, the BUCK2 regulator followed by the BOOST converter are enabled.

11.7.3 BUCK2 Switching Clock-Monitor Error (Internal f_{SW} Clock Configuration)

In any of the operating states (RESET, DIAGNOSTIC, ACTIVE, and SAFE), if the BUCK2 switching-clock error is detected, while the internal OSC clock source is in good condition, the following occurs:

- The BUCK2_FSW_CLK_ERR status bit is set.
- The BUCK2 regulator is disabled without activating resistive discharge.
- The device goes into the SAFE state.
- The device error counter increments.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

If the BUCK2 regulator is configured as an NRES source and when the BUCK2 output discharges to less than its UV-threshold level, the device goes into the RESET state. In the RESET state, the BUCK2 regulator is enabled again only after the BUCK2 regulator has discharged below the $V_{BUCK2\_RESTART\_LEVEL}$ voltage level and the f_{SW_BUCK2} clock monitor indicates that the clock is in good condition. Enabling the BUCK2 regulator again is followed by a full ABIST run during the NRES extension after there is no active RESET state condition.

If an ABIST run in the RESET state fails, the device goes into the SAFE state again, repeating the same procedure until the device error counter reaches its power-down threshold (the PWD_TH[3:0] bits). When the device error counter reaches its programmed power-down threshold, the device goes into the OFF state.

While the device is in the SAFE state, the system MCU can detect if a reported clock failure occurred because of a clock-monitor failure or true clock failure. A false clock failure occurs when a clock monitor fails. In case of false clock-failure detection, the system MCU can disable the clock monitoring. As a single-point failure, the clock monitoring failure is not a critical failure, and therefore, the system MCU can ignore it.

While the device is in the RESET state and when the BUCK2 regulator is enabled again, the device goes into the OFF state, if the BUCK2 regulator does not ramp-up within the time-out interval for the RESET state.

If the BUCK2 regulator is not configured as a RESET state condition (BUCK2_UV_RST_EN = 0b), the device does not change the state as the BUCK2 output discharges to less than its UV threshold level. The system MCU can enable the BUCK2 regulator by setting the BUCK2_EN control bit in the PWR_CTRL control register.

11.7.4 BOOST Switching Clock-Monitor Error (Internal f_{SW} Clock Configuration)

In the operating states (RESET, DIAGNOSTIC, ACTIVE, and SAFE), if the BOOST switching-clock error is detected while the internal OSC clock source is in good condition, the following occurs:

- The BOOST_FSW_CLK_ERR status bit is set.
- The BOOST converter is disabled without activating resistive discharge.
- The device goes into the SAFE state.
- The device error counter increments.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

If the BOOST converter is configured as a RESET state condition (BOOST_UV_RST_EN = 1b), and when the BOOST output discharges to less than its UV-threshold level, then the device goes into the RESET state. In the

RESET state, the BOOST converter is enabled again only after the BOOST converter discharges below the $V_{BOOST\_RESTART\_LEVEL}$ voltage level and after the SYNC_IN, PLL/VCO and f_{SW_BOOST} clock monitors indicate that the clocks are in good condition. Enabling the BOOST converter again is followed by a full ABIST run during an NRES extension, after there is no active RESET state condition.

If an ABIST run in the RESET state fails (because of a clock-monitor failure or any other failure) the device goes into the SAFE state again, repeating the same procedure until the device error counter reaches its programmed power-down threshold level and the device goes into the OFF state.

While the device is in the SAFE state, the system MCU can detect if a reported clock failure occurred because of a clock-monitor failure or true clock failure. A false clock failure occurs when a clock monitor fails. In case of a false clock-failure detection, the system MCU can disable clock monitoring.

While the device is in the RESET state and when the BOOST converter is enabled again, the device goes into the OFF state, if the BOOST converter does not ramp-up within the time-out interval for the RESET state.

If the BOOST is not configured as a RESET state condition (BOOST_UV_RST_EN = 0b), the device stays in the SAFE state as the BOOST output discharges to less than its UV-threshold level. The system MCU can enable the BOOST converter by setting the BOOST_EN control bit in the PWR_CTRL control register.

While the device is in the SAFE state, the system MCU can command a clock-monitor diagnostic test to be performed. If this diagnostic test fails, the system MCU can disable the clock monitoring function. As a single-point failure, a clock monitoring circuit failure is not a critical failure, and therefore, the system MCU can ignore it.

11.7.5 External f_{SW} Clock Configuration (f_{SW} Derived from SYNC_IN and PLL Clocks)

11.7.5.1 SYNC_IN, PLL, and VCO Clock Monitors

If a SYNC_IN clock error is detected, the following occurs:

- The SYNC_CLK_ERR status bit is set in the SAFETY_CLK_STAT register.
- The device goes into the SAFE state.
- The PLL clock is disabled and the VCO clock is switched to free-running mode to provide an alternative clock source for the switched-mode regulators.
- The device error counter increments.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

If a PLL or VCO clock error is detected, the following occurs:

- The FSW_SRC_CLK_ERR status bit is set in the SAFETY_CLK_STAT register.
- The device goes into the SAFE state.
- The BUCK1 regulator, BUCK2 regulator, and BOOST converter are disabled without enabling resistive discharge.
- The device error counter increments.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

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Eventually, as the BUCK1 regulator, BUCK2 regulator, and BOOST converter discharge to less than the respective UV-threshold level, a global RESET condition is met (as long as one regulator UV event is configured as a RESET state condition) and the device goes into the RESET state. When the device enters the RESET state, the BUCK1 regulator is enabled again (its default state) only if the SYNC_IN clock monitor and PLL (or VCO) clock monitor no longer indicates an error, the BUCK1 and BUCK2 regulators are discharged below the $V_{BUCK1\_RESTART\_LEVEL}$ and $V_{BUCK2\_RESTART\_LEVEL}$ voltage levels, and the BOOST converter is discharged below the $V_{BOOST\_RESTART\_LEVEL}$ voltage levels. After the BUCK1 regulator is enabled, the BUCK2 regulator and the BOOST converter are enabled after the BUCK1 output exceeds its UV-threshold level.

All the BUCK1 monitoring and protection mechanisms are active, and if any critical conditions are still present, the BUCK1 regulator is disabled again. If the BUCK1 regulator never recovers while in the RESET state, the RESET state time-out event places the device into the OFF state.

As the rails discharge to less than their UV-threshold levels, the device enters the RESET state. While in the RESET state, the SYNC_IN clock monitor is disabled, PLL synchronization to the SYNC_IN input clock is stopped, and the PLL starts a gradual transition to the free-running VCO clock. The switched-mode regulators are enabled by internal start-up circuit only when neither the PLL (or VCO) clock monitor (DIG_CLK_MON6) nor the respective clock monitors (DIG_CLK_MON3 – DIG_CLK_MON5) for the switched-mode regulators detect any errors.

In the RESET state, the SYNC_IN clock monitor is disabled (the DIG_SYNC_CLK_MON_EN control bit is cleared) because the MCU stops driving the clock when rebooting. The regulators are enabled as soon as the PLL (or VCO) clock monitor reports that the clock is in good condition. The SYNC_IN clock monitor stays disabled until the MCU gets out of reset and completes re-boot (after NRES rising edge and the device goes into the DIAGNOSTIC state). After reboot the MCU sends a SPI command to enable the SYNC_IN clock monitor (to set the DIG_SYNC_CLK_MON_EN control bit). The MCU should enable the SYNC_IN clock monitor only after it has started to drive the SYNC_IN clock input.

If the failure is because of the PLL (or VCO) clock failure, the device stays in the RESET state until the PLL (or VCO) clock recovers. If the PLL (or VCO) clock does not recover, the RESET state time-out event occurs and the device goes into the OFF state and latches the RESET state time-out event in the Analog_Latch.

11.7.5.2 BUCK1 Switching Clock-Monitor Error (External f_{SW} Clock Configuration)

In the operating states (RESET, DIAGNOSTIC, ACTIVE, and SAFE), if a BUCK1 switching-clock error is detected while the internal OSC clock source is in good condition, the following occurs:

- The BUCK1_FSW_CLK_ERR status bit is set.
- the BUCK1 regulator, BUCK2 regulator, and BOOST converter are disabled without enabling resistive discharge.
- The device goes into the SAFE state.
- The device error counter increments.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

注

Eventually, as the BUCK1 regulator, BUCK2 regulator, and BOOST converter discharge to less than the respective UV-threshold level, a global RESET condition is met (as long as one regulator UV event is configured as an NRES source) and the device goes into the RESET state. When the device enters the RESET state, the BUCK1 regulator is enabled again (its default state) only if the SYNC_IN clock monitor and the PLL (or VCO) clock monitor no longer indicates an error, the BUCK1 and BUCK2 regulators are discharged 60% less than the nominal value, and the BOOST converter is discharged below the $V_{BOOST\_RESTART\_LEVEL}$ voltage value. After the BUCK1 regulator is enabled and the BUCK1 output exceeds its UV-threshold level, the BUCK2 regulator and BOOST converter are enabled.

All the BUCK1 monitoring and protection mechanisms are active, and if any critical conditions are still present, the BUCK1 regulator is disabled again. If the BUCK1 regulator never recovers while in the RESET state, the RESET state time-out event places the device into the OFF state.

As the rails discharge to less than their UV-threshold level, the device enters the RESET state. While in the RESET state, the switched-mode regulators are enabled by internal start-up control circuit only when none of the DIG_CLK_MONx monitors detect any errors and when the regulator outputs have discharged to less than the $V_{BUCKx/BOOST\_RESTART\_LEVEL}$ voltage level of the respective target regulation voltage. After the BUCK1 regulator is enabled and the BUCK1 output exceeds its UV-threshold level, the BUCK2 regulator and the BOOST converter are enabled. While in the RESET state, the SYNC_IN clock monitor is disabled, the PLL synchronization to the SYNC_IN clock is stopped and the PLL starts a gradual transition to the free-running VCO clock.

11.7.5.3 BUCK2 Switching Clock-Monitor Error (External f_{SW} Clock Configuration)

In any of the operating states (RESET, DIAGNOSTIC, ACTIVE, and SAFE), if the BUCK2 switching-clock error is detected while the internal OSC clock source is in good condition, the following occurs:

- The BUCK2_FSW_CLK_ERR status bit is set.
- The BUCK2 regulator is disabled without activating resistive discharge.
- The device goes into the SAFE state.
- The device error counter increments.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

If the BUCK2 is configured as an NRES source and when the BUCK2 output discharges to less than its UV-threshold level, the device goes into the RESET state. In the RESET state, the BUCK2 regulator is enabled again only after the BUCK2 regulator discharges below the $V_{BUCK2\_RESTART\_LEVEL}$ voltage level and the SYNC_IN, and when the PLL (or VCO) and f_{SW_BUCK2} clock monitors indicate that the clocks are in good condition. Enabling again the BUCK2 regulator is followed by a full ABIST run during an NRES extension after there is no active RESET state condition.

If an ABIST run in the RESET state fails (because of a clock monitor failure or any other failure), the device goes into the SAFE state again, repeating the same procedure until the device error counter reaches its programmed power-down threshold value and the device goes into the OFF state.

While the device is in the SAFE state, the system MCU can detect if a reported clock failure occurred because of a clock-monitor failure or a true clock failure. A false clock failure occurs when a clock monitor fails. In case of false clock-failure detection, the system MCU can disable clock monitoring. As a single-point failure, clock monitoring failure is not a critical failure, and therefore, the system MCU can ignore it.

While the device is in the RESET state and when the BUCK2 regulator is enabled again, the device goes into the OFF state if the BUCK2 output does not ramp up within the time-out interval for the RESET state.

If the BUCK2 regulator is not configured as a RESET state condition, as the BUCK2 output discharges to less than its UV-threshold level, then the device stays in the SAFE state. The system MCU can enable the BUCK2 regulator by setting the BUCK2_EN control bit in the PWR_CTRL control register.

11.7.5.4 BOOST Switching Clock-Monitor Error (External f_{SW} Clock Configuration)

In the operating states (RESET, DIAGNOSTIC, ACTIVE, and SAFE), if the BOOST switching-clock error is detected while the internal OSC clock source is in good condition, then the following occurs:

- The BOOST_FSW_CLK_ERR status bit is set.
- The BOOST converter is disabled without activating resistive discharge.
- The device goes into the SAFE state.
- The device error counter increments.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

If the BOOST converter is configured as a RESET state condition, and when the BOOST output discharges to less than its UV-threshold level, then the device goes into the RESET state. In the RESET state, the BOOST converter is enabled again only after the BOOST has discharged below the $V_{BOOST\_RESTART\_LEVEL}$ voltage level and the f_{SW_BOOST} clock monitor indicates that clock is in good condition. Enabling the BOOST converter again is followed by a full ABIST run during an NRES extension after there is no active RESET state condition.

If an ABIST run in the RESET state fails (because of a clock monitor failure or any other failure) the device goes into the SAFE state again, repeating the same procedure until the device error counter reaches its programmed power-down threshold value and the device goes into the OFF state.

While the device is in the SAFE state, the system MCU can detect if a reported clock failure occurred because of a clock-monitor failure or true clock failure. A false clock failure occurs when a clock monitor fails. In case of false clock-failure detection, the system MCU can disable the clock monitoring. As a single-point failure, clock monitoring failure is not a critical failure, and therefore, the system MCU can ignore it.

While the device is in the RESET state, and when the BOOST converter is enabled again, the device goes into the OFF state, if the BOOST does not ramp-up within the time-out interval for the RESET state, and the device transitions to the OFF state.

If the BOOST converter is not configured as a RESET state condition, the device stays in the SAFE state as the BOOST output discharges to less than its UV-threshold level. The system MCU can enable the BOOST converter by setting the BOOST_EN control bit in the PWR_CTRL control register.

While the device is in the SAFE state, the system MCU can command the clock-monitor to perform a diagnostic test. If this diagnostic test fails, the system MCU can disable the clock monitoring function. As a single-point failure clock monitoring failure is not a critical failure, and therefore, the system MCU can ignore it.

11.8 BUCK1, BUCK2, and BOOST Switching-Clock Spread-Spectrum Modulation

The device supports spread-spectrum modulation of the regulator's switching clocks. Two factory-selectable modulation modes are available The first mode is external modulation which modulates the input clock at the SYNC_IN pin. The second mode is internal Adaptively Randomized Spread-Spectrum (ARSS) modulation which is based on the internal oscillator (MODCLK).

An external modulation is limited by the PLL bandwidth. The minimum time step between any two frequency changes is 50 µs. The maximum frequency change with each frequency step is 100 kHz. When the switching clocks are configured for external modulation, the device starts up with the regulator switching clocks generated from the free-running VCO clock. After the regulators ramp up and the NRES pin is driven high, an MCU can provide the input clock for the SYNC_IN pin.

The internal modulation from the MODCLK oscillator allows for maximum frequency spread from 1.79 MHz to 2.398 MHz and with a center frequency of 2.1 MHz. More details about internal Adaptively Randomized Spread-Spectrum (ARSS) modulation are covered in application note TPS65313-Q1 EMC Validation Report.

For both modulation modes, the maximum ±17% modulation spread is required to prevent false clock monitoring errors because of ±20% clock monitoring accuracy. If this maximum modulation spread exceeds ±17%, then it could result in false clock-monitoring warnings, which have a threshold set at ±17% from the nominal monitoring clock frequency.

The internal ARSS modulation is disabled by default and can be enabled and configured after power up when the device is in the DIAGNOSTIC state. Internal ARSS modulation is activated by setting the SSM_EN control bit in the SAFETY_CFG3 register.

When an internal ARSS modulation is enabled and configured, it can be disabled by the system MCU when the device is in the DIAGNOSTIC state or when the device goes into the OFF state. The device transition to the RESET state does not impact the internal ARSS modulation when it is enabled and configured.

11.9 Monitoring, Protection and Diagnostics Overview

11.9.1 Safety Functions and Diagnostic Overview

The TPS65313-Q1 device is intended for use in a safety-relevant applications such as automotive, industrial, transportation, and heavy machinery. The following list of monitoring, protection, and diagnostic functions achieve high fault-detection coverage:

- Voltage monitor (VMON)
- Clock monitors (analog and digital domain)
- Analog built-in-self-test (ABIST) for monitoring and protecting analog blocks
- Logic built-in-self-test (LBIST) for monitoring and protecting digital core functions
- Junction temperature monitoring for all power supplies
- Current limit for all power supplies
- Loss of ground detection
- Analog MUX (AMUX) for external diagnostics or debug
- Digital MUX (DMUX) for external diagnostics or debug
- Configurable open and close window watchdog timer with configurable question and answer scheme
- MCU error signal monitor (ESM) as a secondary system-watchdog function
- MCU reset supervisor with diagnostics for the NRES output pin
- Controlled and protected enable and interrupt output (ENDRV/nIRQ) for external power stage or peripherals with output pin diagnostics
- Device configuration register CRC
- Device EEPROM data CRC
- SPI command decoder with SPI frame CRC
- SPI data output feedback check
- Device fail-safe controller with SAFE state and RESET state for detected error events

11.9.2 Supply Voltage Monitor (VMON)

The supply voltage monitor (VMON) monitors the device supply voltage, all regulator output voltages, the internal regulators, and up to two external supply rails. The SPI register has VMON status bits (UV, OV, and OVP) to indicate an undervoltage or overvoltage event (error event) for each monitored voltage rail. The device keeps the VMON status bits set to 0b during the ramp up of the monitored rails. The device sets the status bit to 1b when the monitored rail is outside the specified range. The status bit stays set until it is cleared by a valid SPI read command if the corresponding fault condition is removed.

The complete VMON block is supplied by a separate supply pin (VIN_SAFE). The reference voltages for the VMON module (V_{REF_MON}) are derived from a redundant band-gap reference (BG2) which is independent of the primary band-gap reference (BG1). BG1 provides reference voltages (V_{REF_REG}) for the regulators and other functional blocks. The VMON module has a deglitch timer for each monitored supply rail. If the error event occurs for a time period shorter than the deglitch time, the VMON module does not set the corresponding VMON status bit. The device keeps the VMON status bits set to 0b during the ramp up of the monitored voltage rails to make sure monitoring is reliable without false setting of the VMON status bits. When the device is in the operating states, the voltage monitoring is continuous and stays active even after the respective regulator has been disabled.

The analog-built-in self-test (ABIST) runs the VMON modules' diagnostic check. The ABIST is executed during device power-up or when activated by the system MCU when the device is in the DIAGNOSTIC, ACTIVE, or SAFE state. Each monitored voltage rail is emulated for an undervoltage, overvoltage, and overvoltage

protection condition on the corresponding comparator inputs which forces the corresponding comparator to toggle multiple times. The comparator output toggling pattern is observed and checked by the ABIST digital controller. The monitored voltage rails are not affected during the ABIST. No undervoltage or overvoltage events occur on any of monitored rails because of these diagnostic tests.

表 11-1 provides an overview of the voltage monitoring.

表 11-1. Voltage Monitoring Overview

VOLTAGE RAIL	MONITORED PIN	DETECTION THRESHOLD RANGE			DEGLITCH TIME		DEVICE BEHAVIOR UPON DETECTION (SPI FLAG, STATE TRANSITION, NRES/ENDRV PIN STATUS)			ABIST
		UV	OV	OVP	UV/OV	OVP	UV	OV	OVP	
VBAT	AVIN	5.8 V to 6.6 V(1)	36 V to 40 V	—	UV: 90 µs to 110 µs OV: 10 µs to 20 µs	—	VMON_UV_STAT[6] No change in state No change in NRES, ENDRV/nIRQ = 0 if VIN_BAD_IRQ_EN = 1(2)	VMON_OV_STAT[6] OFF state NRES = 0, ENDRV/nIRQ = 0	—	NO
V_{BUCK1} (3)	VSENSE1	–5.0% to –2.5%	2.5% to 5.0%	6% to 10%	21 µs to 39 µs	21 µs to 39 µs	VMON_UV_STAT[0] RESET state if BUCK1_UV_RST_EN = 1, SAFE state if BUCK1_UV_RST_EN = 0 NRES = 0, ENDRV/nIRQ = 0 if BUCK1_UV_RST_EN = 1, NRES = 1, ENDRV/nIRQ = 0 if BUCK1_UV_RST_EN = 0	VMON_OV_STAT[0] RESET state if BUCK1_OV_RST_EN = 1, SAFE state if BUCK1_OV_RST_EN = 0 NRES = 0, ENDRV/nIRQ = 0 if BUCK1_OV_RST_EN = 1, NRES = 1, ENDRV/nIRQ = 0 if BUCK1_OV_RST_EN = 0	SAFETY_BUCK1_STAT1[3] OFF state if BUCK1_OVP_OFF_EN = 1, SAFE state if BUCK1_OVP_OFF_EN = 0 NRES = 0, ENDRV/nIRQ = 0 if BUCK1_OVP_OFF_EN = 1, NRES = 1, ENDRV/nIRQ = 0 if BUCK1_OVP_OFF_EN = 0	YES
V_{BUCK2}	VSENSE2	–5.0% to –2.5%	2.5% to 5.0%	6% to 10%	21 µs to 39 µs	21 µs to 39 µs	VMON_UV_STAT[1] RESET state if BUCK2_UV_RST_EN = 1, No state change if BUCK2_UV_RST_EN = 0 NRES = 0, ENDRV/nIRQ = 0 if BUCK2_UV_RST_EN = 1, NRES = 1, ENDRV/nIRQ = 0 if BUCK2_UV_RST_EN = 0	VMON_OV_STAT[1] RESET state if BUCK2_OV_RST_EN = 1, SAFE state if BUCK2_OV_RST_EN = 0 NRES = 0, ENDRV/nIRQ = 0 if BUCK1_OV_RST_EN = 1, NRES = 1, ENDRV/nIRQ = 0 if BUCK2_OV_RST_EN = 0	SAFETY_BUCK2_STAT1[3] SAFE state(4) NRES = 1, ENDRV/nIRQ = 0	YES

表 11-1. Voltage Monitoring Overview (続き)

VOLTAGE RAIL	MONITORED PIN	DETECTION THRESHOLD RANGE			DEGLITCH TIME		DEVICE BEHAVIOR UPON DETECTION (SPI FLAG, STATE TRANSITION, NRES/ENDRV PIN STATUS)			ABIST
		UV	OV	OVP	UV/OV	OVP	UV	OV	OVP	
V_{BOOST}	VSENSE3	–5.0% to –2.5%	2.5% to 5.0%	6% to 10%	21 µs to 39 µs	21 µs to 39 µs	VMON_UV_STAT[3] RESET state if BOOST_UV_RST_EN = 1, *No change in state* if BOOST_UV_RST_EN = 0 NRES = 0, ENDRV/nIRQ = 0 if BOOST_UV_RST_EN = 1, No change in NRES or ENDRV/nIRQ if BOOST_UV_RST_EN = 0	VMON_OV_STAT[3] RESET state if BOOST_OV_RST_EN = 1, SAFE state if BOOST_OV_RST_EN = 0 NRES = 0, ENDRV/nIRQ = 0 if BOOST_OV_RST_EN = 1, NRES = 1, ENDRV/nIRQ = 0 if BOOST_OV_RST_EN = 0	SAFETY_BOOST_STAT1[3] SAFE state[5] NRES = 1, ENDRV/nIRQ = 0	YES
EXT_VSENSEx	EXT_VSENSEx	–4.8% to –3.0%	3.0% to 4.8%	—	21 µs to 39 µs	—	EXT_VMON_STAT[1:0] RESET state if EXT_VMONx_UV_RST_EN = 1, SAFE state if EXT_VMONx_UV_RST_EN = 0 AND EXT_VMONx_UV_IRQ_EN = 1 NRES = 0, ENDRV/nIRQ = 0 if EXT_VMONx_UV_RST_EN = 1, NRES = 1, ENDRV/nIRQ = 0 if EXT_VMONx_UV_RST_EN = 0 AND EXT_VMONx_UV_IRQ_EN = 1	EXT_VMON_STAT[5:4] RESET state if EXT_VMONx_OV_RST_EN = 1, SAFE state if EXT_VMONx_OV_RST_EN = 0 AND EXT_VMONx_OV_IRQ_EN = 1 NRES = 0, ENDRV/nIRQ = 0 if EXT_VMONx_OV_RST_EN = 1, NRES = 1, ENDRV/nIRQ = 0 if EXT_VMONx_OV_RST_EN = 0 AND EXT_VMONx_OV_IRQ_EN = 1	—	YES
VREG	VREG	3.7 V to 3.9 V	5.9 V to 6.5 V	—	UV: 24 µs to 40 µs OV: 10 µs to 20 µs	—	VMON_UV_STAT[4] OFF state NRES = 0, ENDRV/nIRQ = 0	VMON_OV_STAT[4] OFF state NRES = 0, ENDRV/nIRQ = 0	—	YES
VIO	VIO	—	5.9 V to 6.5 V	—	10 µs to 20 µs	—	—	VMON_OV_STAT[7] No change in state NRES and ENDRV/nIRQ HiZ as VIO gets disconnected[6]	—	NO

(1) VIN bad falling threshold; VIN_BAD_TH[1:0] bit is set to 0b.
(2) No change in the ENDRV/nIRQ output if the VIN_BAD_IRQ_EN bit is set to 0b.
(3) The BUCK1 EOVP results in a transition to the OFF state.
(4) If the BUCK2 OVP event is still present for the $t_{BUCK2\_OVP\_OFF}$ duration after the BUCK2 regulator is disabled, then the TPS65313-Q1 device goes into the OFF state.
(5) If the BOOST OVP event is still present for the $t_{BOOST\_OVP\_OFF}$ duration after the BOOST converter is disabled, then the TPS65313-Q1 device goes into the OFF state.
(6) The pins can still be pulled down if that is the intended status, but the pins cannot be pulled up as the pin drivers get disconnected from their supply, VIO.

11.9.3 Clock Monitors

The TPS65313-Q1 device includes one clock monitor in the analog domain (ACLKMNT) and six clock monitors in the digital domain (DCLKMNT) as shown in 表 11-2. The stable system clock (SYSCLK) for the digital core with reasonable frequency accuracy is a prerequisite to device power-up. The analog clock monitor (ACLKMNT) monitors the SYSCLK frequency before the download of trim data from the EEPROM. During a device power-up event, if the SYSCLK does not start switching with defined accuracy limits within the $t_{START\_UP\_TO}$ time, the device goes back to the OFF state and latches the failure conditions (SYSCLK error and power-up time-out) in the Analog_Latch.

The EEPROM trim content is downloaded when the digital core is out of the NPOR condition. If the EEPROM content is downloaded without error, the DCLKMNT monitors are enabled.

DCLKMNT monitors monitor the health of the clocks along the clock tree. The clock tree generates three switching clocks for the BUCK1 regulator, BUCK2 regulator, and BOOST converter. 表 11-2 summarizes the DCLKMNT monitors. For more information on device behavior when each DCLKMNT monitor detects a clock error condition, see セクション 11.7.

表 11-2. The Digital Clock Monitors

MONITOR	MONITORED CLOCK	REFERENCE CLOCK	STATUS BIT IN SAFETY_CLK_STAT REGISTER	STATUS BIT IN SAFETY_CLK_WARN_STAT REGISTER
DIG_CLK_MON1	SYNC_IN clock	SYSCLK	Bit 2, SYNC_CLK_ERR	Bit 2, SYNC_CLK_WARN
DIG_CLK_MON2 (3)	SYSCLK	MODCLK or PLL clock(1)	Bit 0, DIG_SYSCLK_ERR	—
DIG_CLK_MON3	BUCK1_CLK(2)	SYSCLK	Bit 3, BUCK1_FSW_CLK_ERR	Bit 3, BUCK1_FSW_CLK_WARN
DIG_CLK_MON4	BUCK2_CLK(2)	SYSCLK	Bit 4, BUCK2_FSW_CLK_ERR	Bit 4, BUCK2_FSW_CLK_WARN
DIG_CLK_MON5	BOOST_CLK(2)	SYSCLK	Bit 6, BOOST_FSW_CLK_ERR	Bit 6, BOOST_FSW_CLK_WARN
DIG_CLK_MON6	PLL VCO clock, or MODCLK	SYSCLK	Bit 1, SMPS_SRC_CLK_ERR	Bit 1, SMPS_SRC_CLK_WARN

(1) The clock is the PLL clock when the SMPS_CLK_SRC bit is set to 0b and is the MODCLK clock when the SMPS_CLK_SRC bit is set to 1b.
(2) The BUCK1_CLK clock is the BUCK1 switching clock, the BUCK2_CLK clock is the BUCK2 switching clock, and the BOOST_CLK is the BOOST switching clock.
(3) DIG_SYSCLK_ERR / DIG_CLK_MON2 error / fault reaction by the device state machine is masked/disabled in device EEPROM and this has no impact to device overall functionality. However, if the fault is detected by this clock monitor, DIG_SYS_CLK_ERR and SYSCLK_ERR status bit will be still set and should be ignored.

The clock monitors detect if the monitored clock is either too fast or too slow.

As defined in the SAFETY_CLK_WARN_STAT register, the DIG_CLK_MONs monitors provide an early-warning flag before a clock error is detected. Depending on the SYSCLK frequency variation (8 MHz ± 5 %), the switched-mode regulators can operate for some time with a clock in a range where electrical parameters and performance cannot be ensured before a clock error is detected. This detection interval can be up to 143 cycles of an 8-MHz SYSCLK clock, or up to 18 µs.

All the DCLKMNT monitors are enabled by default except the SYNC_IN clock monitor (DIG_CLK_MON1). These clock monitors do not have considerable impact on the device functional safety coverage and critical regulator faults are covered with other safety mechanisms in the device. The system MCU can disable DCLKMNT clock monitors through the CLK_MON_CTRL register, if these clock monitors are generating false clock monitoring warnings or errors due to system level noise issues. The ACLKMNT monitor cannot be disabled. When enabled, the DCLKMNT monitors continuously monitor clocks within the defined limits for fast and slow clock. All clock monitors are checked by the built-in-self-test diagnostics.

11.9.4 Analog Built-In Self-Test

The analog built-in self-test (ABIST) is a set of diagnostic functions for critical analog monitoring and protection functions that follow:

- Analog and digital clock monitors
- UV, OV, and OVP voltage monitors

- CRC protection for a check of the EEPROM analog trim content
- Current limit for all regulated supplies
- Overtemperature monitors

The ABIST is activated in each device power-up event before the regulated supplies are enabled or during an NRES extension when the device is in the RESET state. The ABIST can also be activated by the system MCU when the device is in one of the other operating states (DIAGNOSTIC, ACTIVE, or SAFE state).

The ABIST diagnostic test of each comparator includes two pulse responses. This test does not include the deglitch function and the respective status bits which are covered by the LBIST.

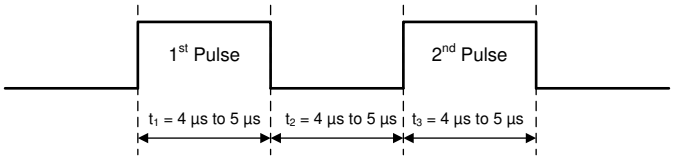


図 11-5. ABIST Test-Pulse Timing

11.9.4.1 ABIST During Power-Up or Start-Up Event

Checks on the current limit comparators of the switched-mode regulators and the VREG U and OV comparators are done during a power-up event before the switched-mode regulators are enabled. When the regulators are enabled, the ABIST on these comparators cannot be activated. The power-up ABIST run time is 150 µs (typical).

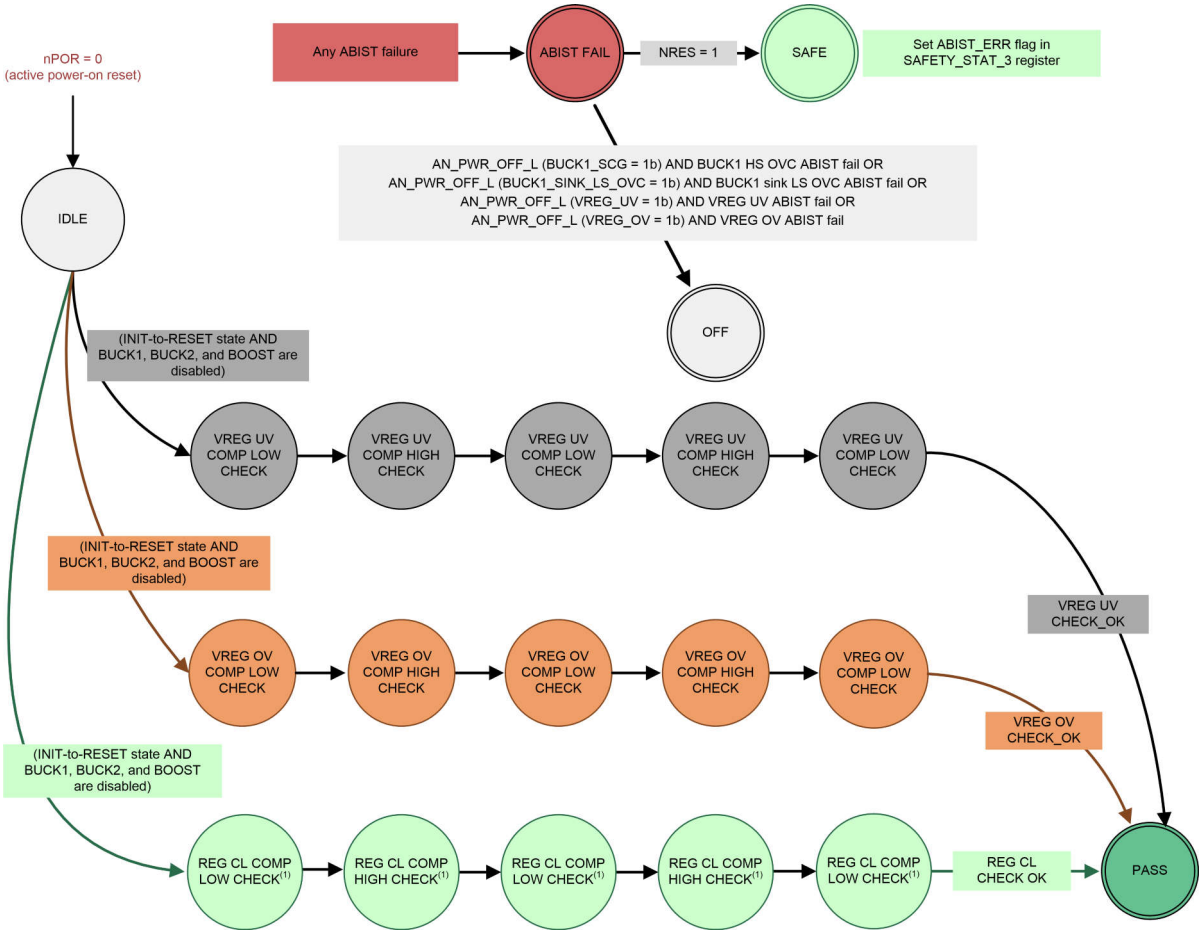
If checks on the BUCK1 current-limit comparators or VREG UV and OV comparators fail, the state controller in the digital core samples the latched status bits in the OFF_STATE_L status register to select the next action.

If any of the checks for the BUCK1 current-limit comparator fail, and if the BUCKx_BOOST_VREG_FAIL bit and corresponding status bit are set, the device goes back to the OFF state. The restart from the OFF state is controlled by the AUTO_START_DIS configuration bit. If the AUTO_START_DIS bit is set to 0b, the device can restart immediately if the WAKE pin voltage is still above its $V_{WAKE-ON}$ threshold. If the AUTO_START_DIS bit is set to 1b, the device can restart only when the WAKE pin is toggled from low to high.

If either of the checks for the VREG UV or OV comparator fails, and if the BUCKx_BOOST_VREG_FAIL bit and corresponding status bit are set, the device goes back to the OFF state. The restart from the OFF state is controlled by the AUTO_START_DIS configuration bit. If the AUTO_START_DIS bit is set to 0b, the device can restart immediately, if the WAKE pin voltage is still above its $V_{WAKE-ON}$ threshold. If the AUTO_START_DIS bit is set to 1b, the device can restart only when the WAKE pin is toggled from low to high. The AUTO_START_DIS bit is set to 1b every time a valid VREG OV event is detected.

If any other current limit comparator check fails, the following occurs:

- The respective status bit for the ABIST current-limit failure is set.
- The device continues with the power-up sequence.
- The device goes into the SAFE state after the NRES pin is driven high.



1. The regulator current-limit test (REG CL) includes the BUCK1, BUCK2, and BOOST current-limit circuits.

図 11-6. ABIST Run During Power-Up as the Device Transitions from the INIT State to the RESET State and Before the BUCK1, BUCK2, and BOOST are Enabled

11.9.4.2 ABIST in the RESET state

An ABIST run, when the device is in the RESET state, occurs during the NRES extension time and can be disabled by setting the AUTO_BIST_DIS bit in the SAFETY_CFG2 register after initial device power-up is complete. This ABIST run includes a diagnostic check of the error monitor for the ENDRV/nIRQ output driver. The primary purpose of this check is to confirm that the ENDRV/nIRQ error monitor can detect the failure. During this test, the ENDRV/nIRQ output pin is toggled while observing if the feedback from the input pin matches the output pin state after the propagation delay. The error monitor of the NRES output driver is checked by the LBIST.

This ABIST run consists of four ABIST groups that run sequentially. A completed ABIST run in the RESET state is indicated by all the ABIST_GROUPx_DONE bits (bits 3 through 0 in the SAFETY_ABIST_ERR_STAT1 register). These bits are cleared to 0b while the corresponding ABIST group is running, and is set to 1b when the corresponding ABIST group is complete. The duration of the ABIST run in the RESET state is 400 µs (typical).

If any of scheduled diagnostic tests fail during this ABIST run, the following occurs:

- The device goes into the SAFE state.
- One or more ABIST error status bits in the SAFETY_ABIST_ERR_STAT1 through the SAFETY_ABIST_ERR_STAT6 registers are set.
- The ENDRV/nIRQ interrupt to the MCU is asserted.

Driving the ENDRV/nIRQ from high to low generates an interrupt to the external MCU in case of a detected-ABIST failure and allows the MCU to confirm the root cause of the ABIST failure by reading the SAFETY_ABIST_ERR_STAT1 through the SAFETY_ABIST_ERR_STAT6 status register.

This ABIST run does not check the current limit circuit of the regulators and the circuits of the VREG UV, VREG OV, VIN UV, and VIN OV voltage monitors. When the VREG regulator is enabled, running the VREG UV and VREG OV diagnostics would cause the VREG output to become uncontrollable. This ABIST run also does not include any general purpose external voltage monitor (EXT_VMONx) that is not enabled.

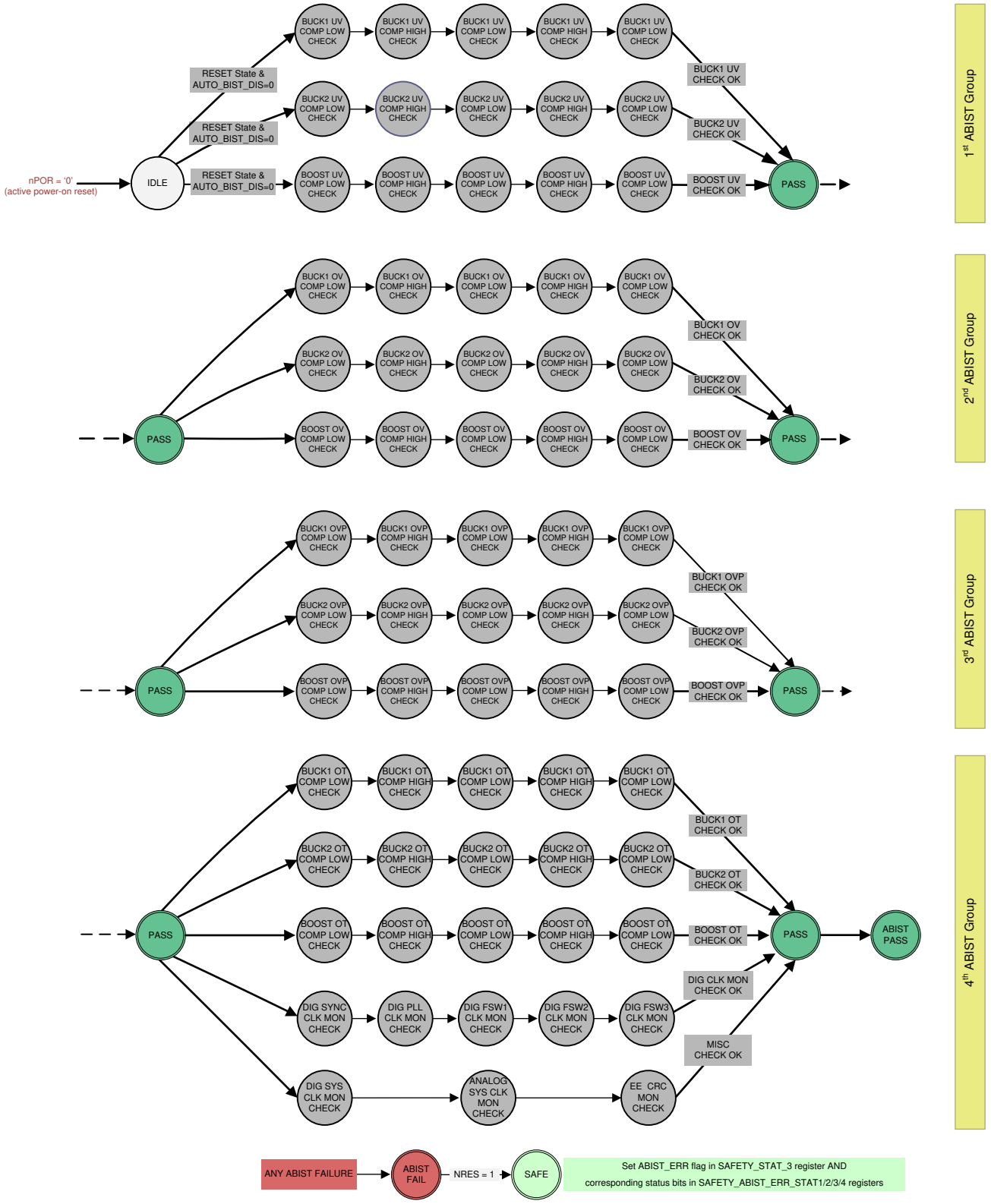


図 11-7. Full ABIST Run During NRES Extension When the Device is in the RESET State (when EXT_VMONx is not enabled)

11.9.4.3 ABIST in the DIAGNOSTIC, ACTIVE, and SAFE State

The system MCU can activate the ABIST when the device is in the DIAGNOSTIC, ACTIVE, or SAFE state through the ABIST_GROUPx_START control bits in the SAFETY_ABIST_CTRL register when the ABIST_SCHED_EN configuration bit in the SAFETY_CFG2 register is not set.

In SAFE and DIAGNOSTIC states, ABIST runs immediately after setting ABIST_GROUPx_START bit in SAFETY_ABIST_CTRL register. In ACTIVE state, if ABIST_SCHED_EN ="0", ABIST runs only once after the ABIST_SCHED_DLY has expired. In ACTIVE state, if ABIST_SCHED_EN ="1", ABIST runs indefinitely with cycle time determined by ABIST_SCHED_DLY and it is stopped when ABIST_GROUPx_START bit is cleared.

The number of ABIST groups of tests depends on how many ABIST_GROUPx_START bits have been set while the ABIST_SCHED_EN configuration bit in the SAFETY_CFG2 register is not set. The options are four ABIST group of tests (or a full ABIST run), three ABIST group of tests, two ABIST group of tests, or just one ABIST group of tests. Examples of the different groups of tests include any of the following:

- ABIST Group 1 → ABIST Group 2 → ABIST Group 3 → ABIST Group 4, or
- ABIST Group 1 → ABIST Group 2 → ABIST Group 3, or
- ABIST Group 1 → ABIST Group 3 → ABIST Group 4, or
- ABIST Group 2 → ABIST Group 3 → ABIST Group 4, or
- ABIST Group 1 → ABIST Group 2, or
- ABIST Group 1 → ABIST Group 3, or
- ABIST Group 1 → ABIST Group 4, or
- ABIST Group 2 → ABIST Group 3, or
- ABIST Group 2 → ABIST Group 4, or
- ABIST Group 3 → ABIST Group 4, or
- ABIST Group 1, or
- ABIST Group 2, or
- ABIST Group 3, or
- ABIST Group 4

The full ABIST run, when the device is in the DIAGNOSTIC or ACTIVE state, includes a diagnostic check of the error monitor for the ENDRV/nIRQ output driver by allowing comparators in the overtemperature monitors (ABIST Group 4) to toggle the ENDRV/nIRQ pin in a known pattern for the duration of an analog comparator test, if any of the BUCKx/BOOST_OT_WARN_IRQ_EN bits are set. The ABIST of the overtemperature monitors includes both the warning and shutdown comparators. When the device is in the SAFE state, the ENDRV/nIRQ pin is always pulled to logic 0.

The diagnostics of the error monitor for the NRES output driver is performed by the LBIST.

At any time when an ABIST group of tests is set to run, the ABIST tests are activated only during the analog comparator output steady state (sampled analog comparator output matches respective deglitched output and SPI status bit).

If none of these conditions are met, then initiation of an ABIST run is delayed. The maximum wait time of an ABIST start is limited by its ABIST time-out function, which is ≈112 µs.

The full ABIST run is activated by setting all four ABIST_GROUPx_START control bits in the SAFETY_ABIST_CTRL register. As each ABIST group of tests are complete, a corresponding ABIST_GROUPx_DONE status bit is set in the SAFETY_ABIST_ERR_STAT1 status register. This ABIST_GROUPx_DONE status bit is cleared when the corresponding ABIST group of tests are running and is set to 1b when the corresponding ABIST group of tests are complete.

If any of scheduled diagnostic tests fail during an ABIST run or an ABIST time-out occurs and the ABIST_ACTIVE_FAIL_RESP bit is set to 0b, then the following occurs:

- The device goes into the SAFE state.
- One or more ABIST error status bits in the SAFETY_ABIST_ERR_STAT1 through

the SAFETY_ABIST_ERR_STAT6 registers are set.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

This enables an interrupting of the external MCU in case of a detected ABIST failure and confirms its root cause by reading the SAFETY_ABIST_ERR_STAT1 through the SAFETY_ABIST_ERR_STAT6 status registers.

If any of the scheduled diagnostic tests fail during an ABIST run or an ABIST time-out occurs, and the ABIST_ACTIVE_FAIL_RESP bit is set to 1b, then the following occurs:
- The device does not change state.
- One or more ABIST error status bits in the SAFETY_ABIST_ERR_STAT1 through the SAFETY_ABIST_ERR_STAT6 registers are set.

Undervoltage and overvoltage comparator diagnostic tests do not impact the regulated output-voltage rails. This ABIST run does not include a circuit check of the regulator current-limit, VREG UV and VREG OV, and VIN UV and VIN OV diagnostic checks. When the VREG regulator is enabled, running the VREG UV and VREG OV diagnostics causes the VREG output to become uncontrollable, and for that reason it is excluded from this ABIST run.

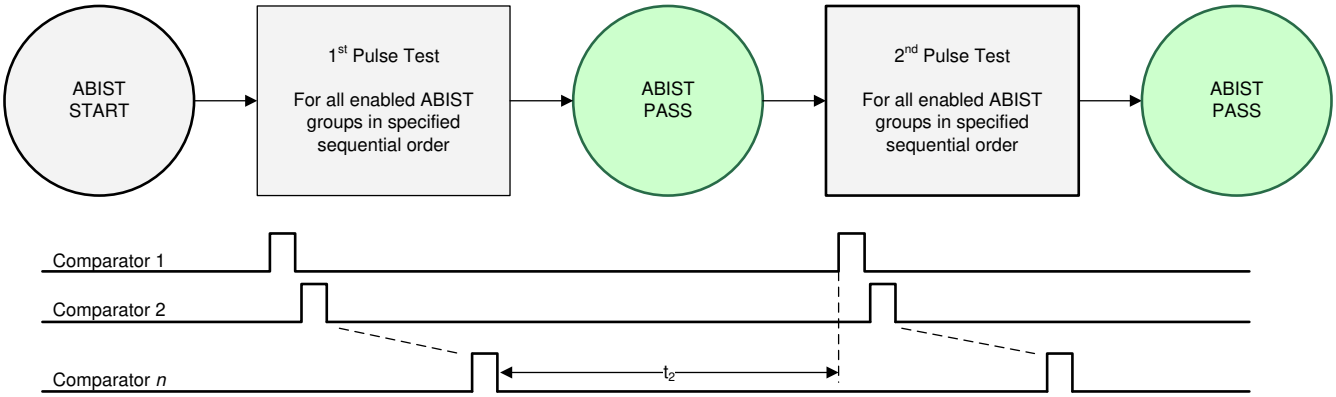
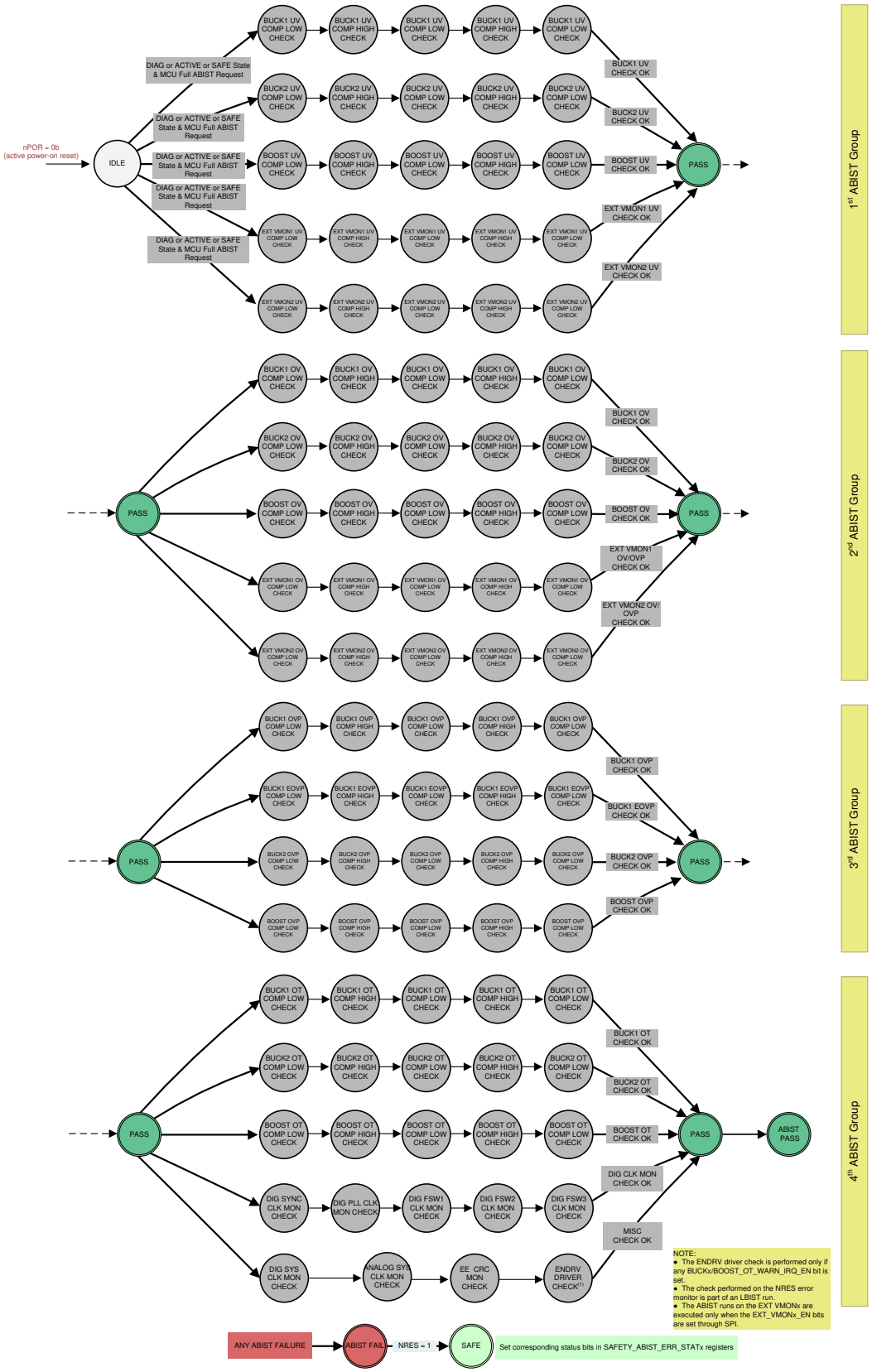


図 11-8. ABIST Delayed Test Pulses

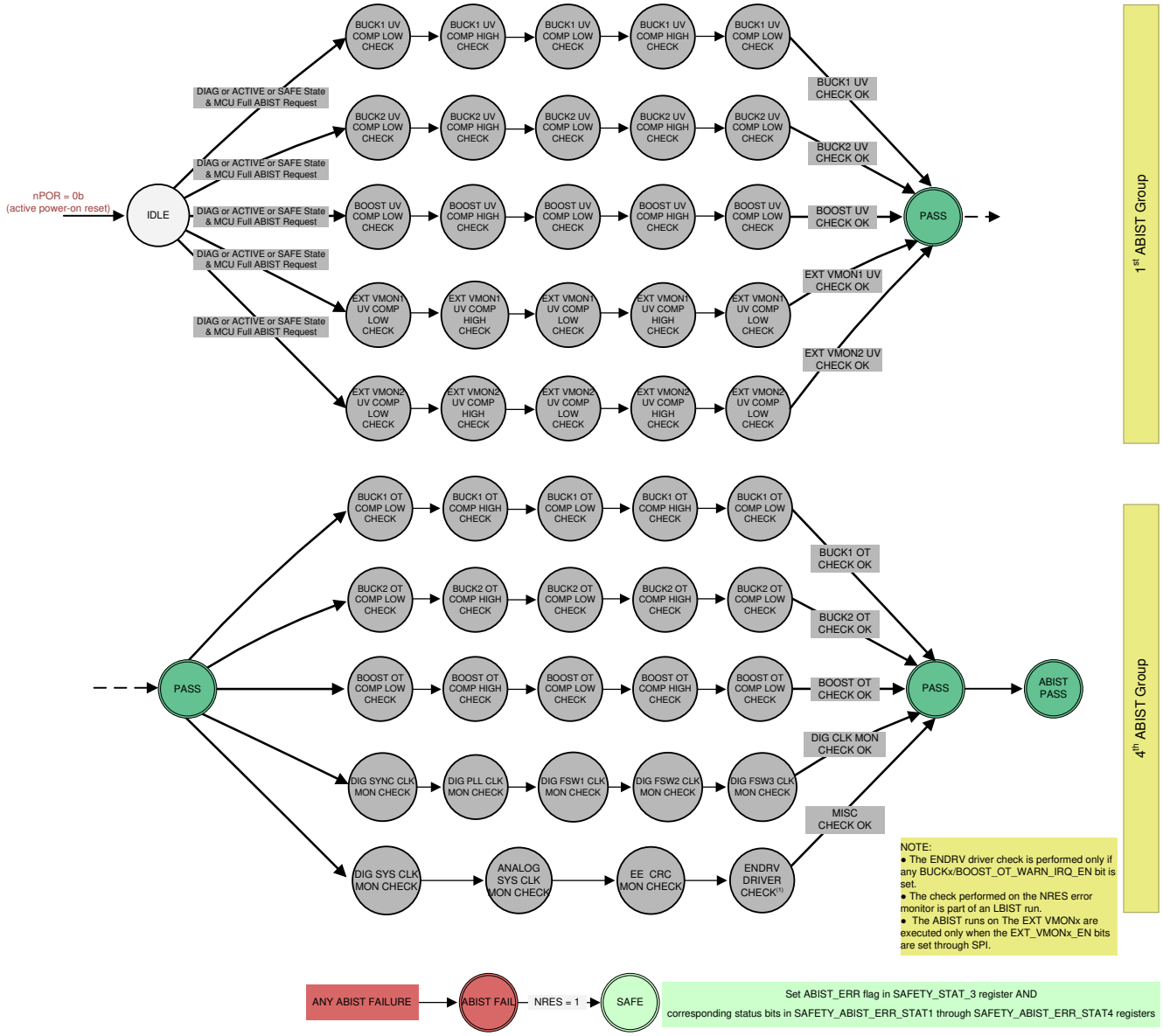
In the DIAGNOSTIC and SAFE state, the time interval, t_2 (time delay measured from the falling edge of test pulse n and the next rising edge of test pulse n+1), is a couple of system clock cycles.


nPOR = 0b
(active power-on reset)
IDLE
DIAG or ACTIVE or SAFE State & MCU Full ABIST Request
BUCK1 UV COMP LOW CHECK
BUCK1 UV COMP HIGH CHECK
BUCK2 UV COMP LOW CHECK
BUCK2 UV COMP HIGH CHECK
BOOST UV COMP LOW CHECK
BOOST UV COMP HIGH CHECK
EXT VMON1 UV COMP LOW CHECK
EXT VMON1 UV COMP HIGH CHECK
EXT VMON2 UV COMP LOW CHECK
EXT VMON2 UV COMP HIGH CHECK
BUCK1 UV CHECK OK
BUCK2 UV CHECK OK
BOOST UV CHECK OK
EXT VMON1 UV CHECK OK
EXT VMON2 UV CHECK OK
PASS
1st ABIST Group
BUCK1 OV COMP LOW CHECK
BUCK1 OV COMP HIGH CHECK
BUCK2 OV COMP LOW CHECK
BUCK2 OV COMP HIGH CHECK
BOOST OV COMP LOW CHECK
BOOST OV COMP HIGH CHECK
EXT VMON1 OV COMP LOW CHECK
EXT VMON1 OV COMP HIGH CHECK
EXT VMON2 OV COMP LOW CHECK
EXT VMON2 OV COMP HIGH CHECK
BUCK1 OV CHECK OK
BUCK2 OV CHECK OK
BOOST OV CHECK OK
EXT VMON1 OV/OVP CHECK OK
EXT VMON2 OV/ OVP CHECK OK
2nd ABIST Group
BUCK1 OVP COMP LOW CHECK
BUCK1 OVP COMP HIGH CHECK
BUCK1 EOVP COMP LOW CHECK
BUCK1 EOVP COMP HIGH CHECK
BUCK2 OVP COMP LOW CHECK
BUCK2 OVP COMP HIGH CHECK
BOOST OVP COMP LOW CHECK
BOOST OVP COMP HIGH CHECK
BUCK1 OVP CHECK OK
BUCK1 EOVP CHECK OK
BUCK2 OVP CHECK OK
BOOST OVP CHECK OK
3rd ABIST Group
BUCK1 OT COMP LOW CHECK
BUCK1 OT COMP HIGH CHECK
BUCK2 OT COMP LOW CHECK
BUCK2 OT COMP HIGH CHECK
BOOST OT COMP LOW CHECK
BOOST OT COMP HIGH CHECK
DIG SYNC CLK MON CHECK
DIG PLL CLK MON CHECK
DIG FSW1 CLK MON CHECK
DIG FSW2 CLK MON CHECK
DIG FSW3 CLK MON CHECK
DIG SYS CLK MON CHECK
ANALOG SYS CLK MON CHECK
EE_CRC MON CHECK
ENDRV DRIVER CHECK(1)
BUCK1 OT CHECK OK
BUCK2 OT CHECK OK
BOOST OT CHECK OK
DIG CLK MON CHECK OK
MISC CHECK OK
ABIST PASS
4th ABIST Group
NOTE:
• The ENDRV driver check is performed only if any BUCKx/BOOST_OT_WARN_IRQ_EN bit is set.
• The check performed on the NRES error monitor is part of an LBIST run.
• The ABIST runs on the EXT VMONx are executed only when the EXT_VMONx_EN bits are set through SPI.
ANY ABIST FAILURE
ABIST FAIL
NRES = 1
SAFE
Set corresponding status bits in SAFETY_ABIST_ERR_STATx registers

1. ENDRV toggling is checked by the system MCU.

図 11-9. Full ABIST When the Device is in the DIAGNOSTIC, ACTIVE, or SAFE State

図 11-10 shows an example for running only the tests for the ABIST Group 1 and ABIST Group 4 groups by setting the ABIST_GROUP1_START and ABIST_GROUP42_START control bits in the SAFETY_ABIST_CTRL register.



1. ENDRV toggling is checked by the system MCU.

図 11-10. Partial ABIST Run When the Device is in the DIAGNOSTIC, ACTIVE, or SAFE State

11.9.4.4 ABIST Scheduler in the ACTIVE State

The system MCU can activate the ABIST scheduler in the ACTIVE state through the ABIST_GROUPx_START control bits in the SAFETY_ABIST_CTRL register when the ABIST_SCHED_EN configuration bit in the SAFETY_CFG2 register is set. When enabled, the scheduler runs continuously until it is commanded to stop by clearing the ABIST_GROUP_xSTART control bits or when the device goes from the ACTIVE state. The ABIST

scheduler cannot run in the DIAGNOSTIC and SAFE state (setting the ABIST_SCHED_EN configuration bit has no impact on ABIST runs in the DIAGNOSTIC and SAFE states when the ABIST_GROUPx_START control bits are set).

At any time when an ABIST group of tests is set to run, the ABIST tests are activated only during the analog comparator output steady state (sampled analog comparator output matches respective deglitched output and SPI status bit).

If none of the previously listed conditions are met, initiation of an ABIST run will be delayed. The maximum wait time to start an ABIST is time limited by its ABIST time-out function.

If any of the scheduled diagnostic tests fail during an ABIST run when the device is in the ACTIVE state or an ABIST start time-out event occurs, the device response depends on the ABIST_ACTIVE_FAIL_RESP configuration bit setting in the SAFETY_CFG2 register.

If the ABIST_ACTIVE_FAIL_RESP bit is set to 0b, the following occurs:

- The device goes into the SAFE state.
- One or more (out of seven) of the ABIST error status bits in the SAFETY_ABIST_ERR_STAT1 through the SAFETY_ABIST_ERR_STAT4 registers are set.
- The ENDRV/nIRQ pin is asserted low to interrupt the external system MCU.

If the ABIST_ACTIVE_FAIL_RESP bit is set to 1b, the following occurs:

- The device stays in the SAFE state.
- One or more (out of seven) of the ABIST error status bits in the SAFETY_ABIST_ERR_STAT1 through SAFETY_ABIST_ERR_STAT4 registers are set.
- The SW interrupt bits are asserted in the SPI status word for each SPI access until the respective ABIST fail status bits are cleared by reading the SAFETY_ABIST_ERR_STATx status registers.

An ABIST-start time-out event can indicate a deglitch function failure, which can be detected by observing the GROUPx_ERR bit being set, but none of the individual status bits in the SAFETY_ABIST_ERR_STATx registers are set. A deglitch function failure can be detected by the LBIST as well. Before a scheduled ABIST run, two cases of analog comparator failures can occur. These cases are defined as follows:

Case 1 An analog comparator fails in such a way that always indicates an active condition (for an example, driving HIGH and signaling all the time that an OV event occurred).

After the deglitch time, the analog comparator output propagates through the deglitch function and is latched in a SPI-mapped register bit.

The ABIST start condition is met (the analog comparator output is equal to the deglitch function output) and the ABIST run starts.

Because the analog comparator is stuck HIGH (for an example, driving HIGH all the time even when a monitored voltage is in the nominal range) the ABIST run detects an analog comparator failure and signals an ABIST run fail.

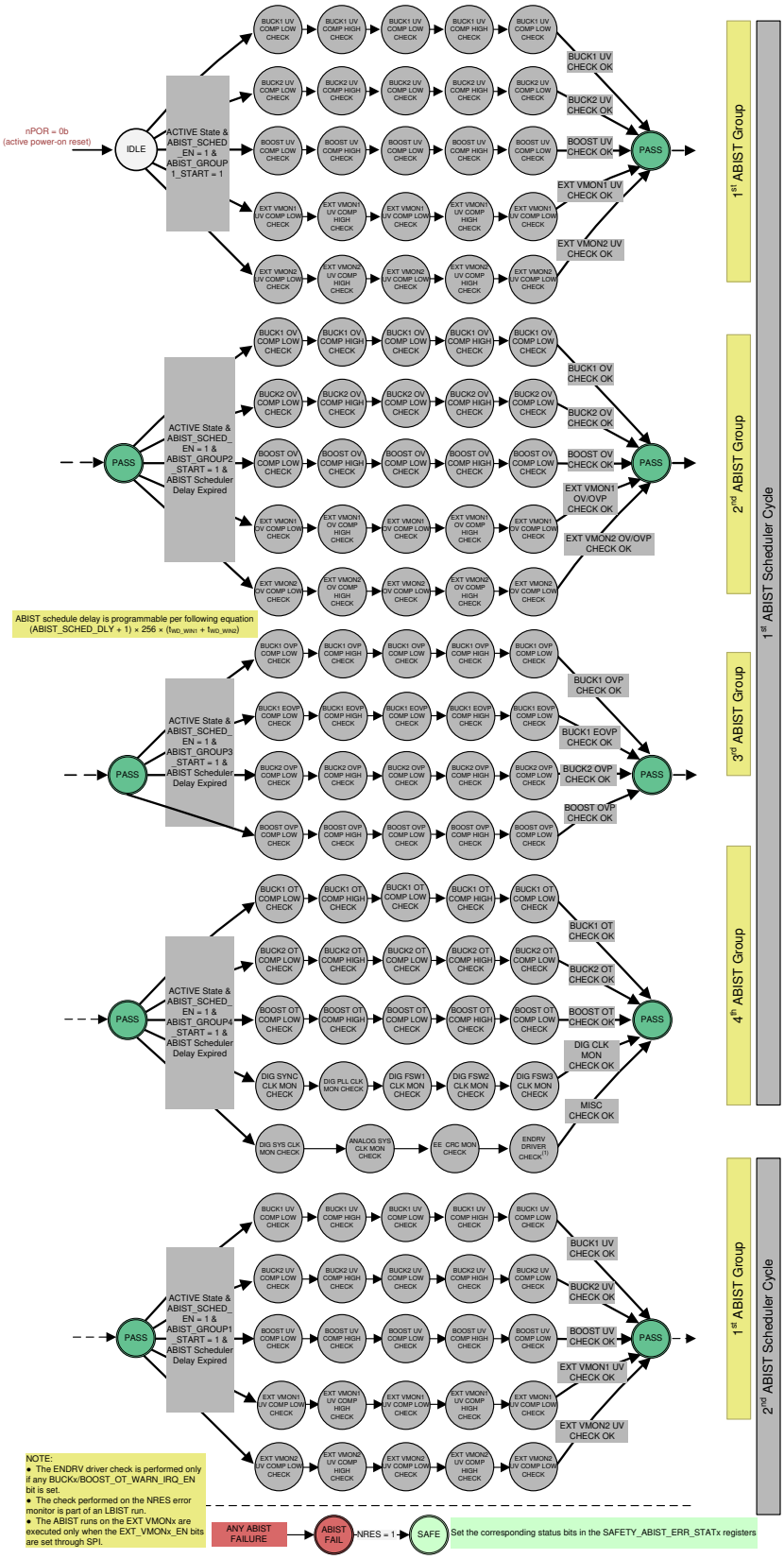
Case 2 An analog comparator fails in such a way that the LBIST cannot detect an active condition (for an example, driving LOW all the time and unable to detect a valid OV event).

The ABIST start condition is met (the analog comparator output is equal to the deglitch function output) and the ABIST run starts.

Because the analog comparator is stuck LOW (for an example, driving LOW all the time even when a monitored voltage is in the OV range) the ABIST run detects an analog comparator failure and signals an ABIST run fail.

Undervoltage and overvoltage comparator diagnostic tests do not impact the regulated output-voltage rails. This ABIST run does not check the current limit circuit of the regulators and the circuits of the VREG UV, VREG OV, VIN UV, and VIN OV voltage monitors. When the VREG regulator is enabled, running the VREG UV and VREG OV diagnostics causes the VREG output to become uncontrollable and for that reason not included in this ABIST run.

図 11-11 shows an example with tests for all four ABIST groups when the ABIST_GROUP1_START, ABIST_GROUP2_START, ABIST_GROPU_START3, and ABIST_GROUP_START4 control bits are set.


nPOR = 0b
(active power-on reset)
IDLE
ACTIVE State & ABIST_SCHED_EN = 1 & ABIST_GROUP1_START = 1
PASS
BUCK1 UV CHECK OK
BUCK2 UV CHECK OK
BOOST UV CHECK OK
EXT VMON1 UV CHECK OK
EXT VMON2 UV CHECK OK
1st ABIST Group
ACTIVE State & ABIST_SCHED_EN = 1 & ABIST_GROUP2_START = 1 & ABIST Scheduler Delay Expired
BUCK1 OV CHECK OK
BUCK2 OV CHECK OK
BOOST OV CHECK OK
EXT VMON1 OV/OVP CHECK OK
EXT VMON2 OV/OVP CHECK OK
2nd ABIST Group
ABIST schedule delay is programmable per following equation
(ABIST_SCHED_DLY + 1) × 256 × (tWD_WIN1 + tWD_WIN2)
ACTIVE State & ABIST_SCHED_EN = 1 & ABIST_GROUP3_START = 1 & ABIST Scheduler Delay Expired
BUCK1 OVP CHECK OK
BUCK1 EOVP CHECK OK
BUCK2 OVP CHECK OK
BOOST OVP CHECK OK
3rd ABIST Group
ACTIVE State & ABIST_SCHED_EN = 1 & ABIST_GROUP4_START = 1 & ABIST Scheduler Delay Expired
BUCK1 OT CHECK OK
BUCK2 OT CHECK OK
BOOST OT CHECK OK
DIG CLK MON CHECK OK
MISC CHECK OK
4th ABIST Group
ACTIVE State & ABIST_SCHED_EN = 1 & ABIST_GROUP1_START = 1 & ABIST Scheduler Delay Expired
BUCK1 UV CHECK OK
BUCK2 UV CHECK OK
BOOST UV CHECK OK
EXT VMON1 UV CHECK OK
EXT VMON2 UV CHECK OK
1st ABIST Group
2nd ABIST Scheduler Cycle
NOTE:
• The ENDRV driver check is performed only if any BUCKx/BOOST_OT_WARN_IRQ_EN bit is set.
• The check performed on the NRES error monitor is part of an LBIST run.
• The ABIST runs on the EXT VMONx are executed only when the EXT_VMONx_EN bits are set through SPI.
ANY ABIST FAILURE
ABIST FAIL
NRES = 1
SAFE
Set the corresponding status bits in the SAFETY_ABIST_ERR_STATx registers

1. ENDRV toggling is checked by the system MCU.

図 11-11. The ABIST Scheduler in the ACTIVE State

図 11-12 shows an example with tests for two ABIST groups when only the ABIST_GROUP1_START and ABIST_GROUP3_START control bits are set.

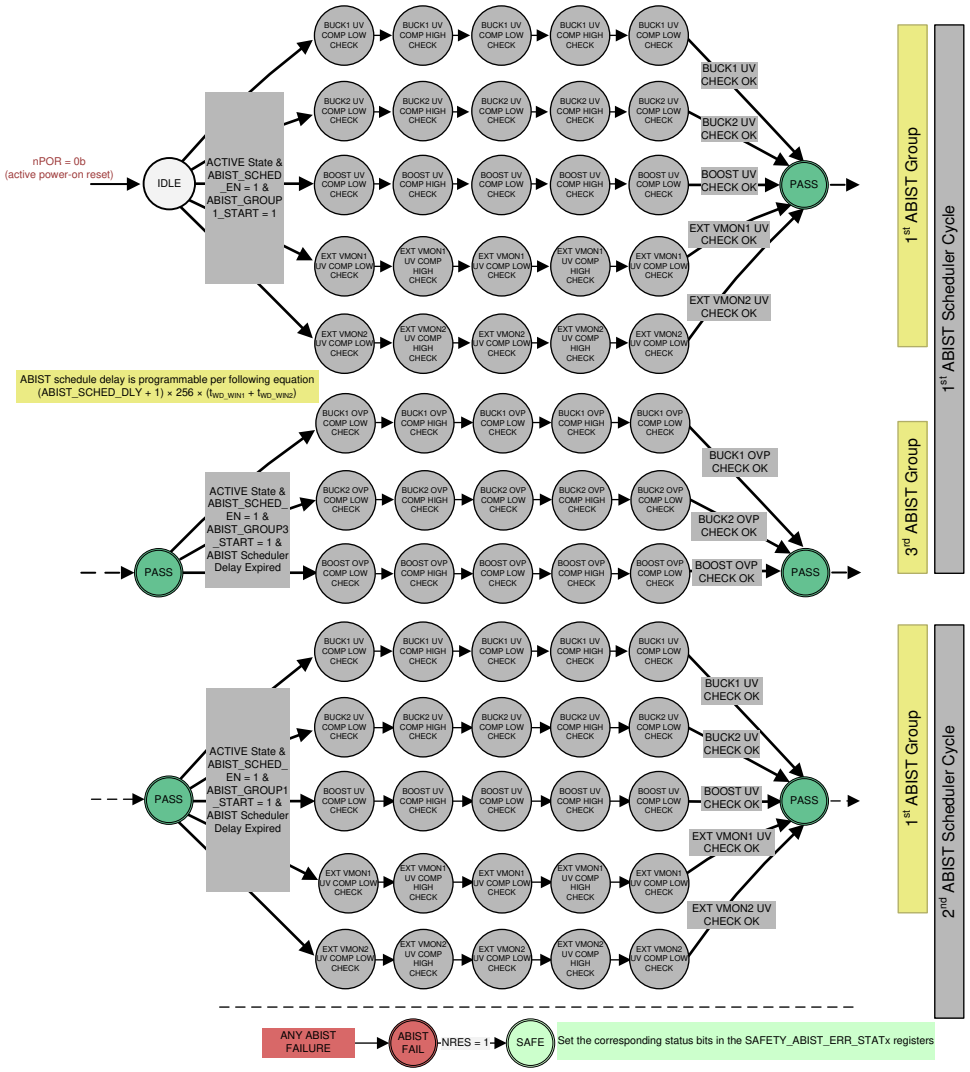


図 11-12. ABIST Scheduler in the ACTIVE State

The ABIST scheduler runs the activated ABIST group of tests periodically in the ACTIVE state when at least one of the ABIST_GROUPx_START bits is set and while the ABIST_SCHED_EN configuration bit is set. The test repetition period is programmable through the ABIST_SCHED_DLY configuration bits in the SAFETY_CFG8 register. This time period is defined by 図 11-10. The time delay between any two ABIST groups of tests can be from 281.6 ms to 10380.9 s.

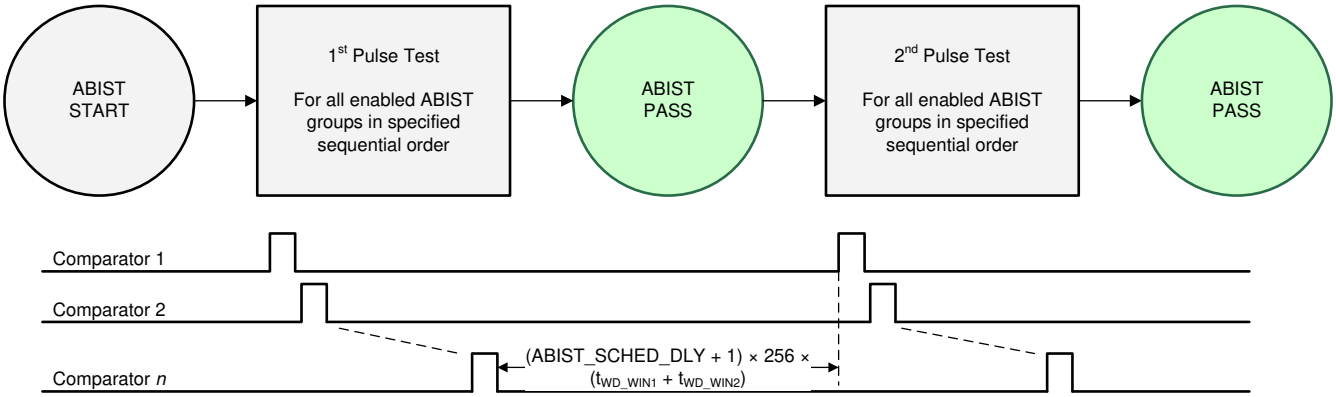


図 11-13. ABIST Scheduler

In the ACTIVE state, the t2 time interval is defined by 式 1

$$t2 = (ABIST\_SCHED\_DLY + 1) \times 256 \times (tWD\_WIN1 + tWD\_WIN2) \quad (1)$$

where

- ABIST_SCHED_DLY is set by the configuration bits in the SAFETY_CFG8 register.
- tWD_WIN1 is a Watchdog Window #1 duration set by the configuration bits in the WDT_WIN1_CFG register.
- tWD_WIN2 is a Watchdog Window #2 duration set by the configuration bits in the WDT_WIN2_CFG register.

11.9.5 Logic Built-In Self-Test

The logic built-in self-test (LBIST) tests the following monitoring and protection circuits in the digital core:

- The digital clock monitors (DIG_CLK_MON1, DIG_CLK_MON2, DIG_CLK_MON3, DIG_CLK_MON4, DIG_CLK_MON5, and DIG_CLK_MON6)
- The watchdog
- The MCU error signal monitor
- The ENDRV/nIRQ pin error detector
- The NRES pin error detector
- The SPI status registers
- The EEPROM controller
- The ABIST controller
- The SPI controller
- The deglitch circuits

The digital core LBIST implementation is using an at-speed capture cycle with a run time of approximately 1.7 ms.

In case of an LBIST failure, the device goes into the SAFE state, and the LBIST_CORE_ERR bit in the SAFETY_LBIST_ERR_STAT register is set.

The LBIST runs in the RESET state when the RESET state extension is in progress. The LBIST can also run in the other operating states by setting the LBIST_EN bit, if the system fault-response time can allow the total 1.7 ms (typical) of run time to occur. During the LBIST, the device cannot monitor the supply outputs or the system MCU with the ESM and the watchdog. When the LBIST is complete, the LBIST_DONE status bit is set and the LBIST_EN control bit in the SAFETY_LBIST_CTRL register is cleared.

When the LBIST is activated in the DIAGNOSTIC state, the device clears the DIAG_EXIT_MASK bit in the DEV_STAT2 register. The DIAGNOSTIC state time-out timer continues to run while the LBIST is in progress. To keep the device in the DIAGNOSTIC state, the system MCU must set the DIAG_EXIT_MASK bit after the LBIST completion.

When the LBIST is activated while the device is in the ACTIVE state or the SAFE state, the state of the ENDRV/nIRQ driver is latched. The state of the ENDRV/nIRQ drive is restored when the LBIST is complete.

The diagnostic test on the LBIST can run by setting the LBIST_DIAG_EN control bit. The test on the LBIST signature check is performed by modifying either the expected signature value, input data string modification or both to force an LBIST error. The LBIST_DIAG_EN bit is cleared when the LBIST diagnostic test is complete.

The 表 11-3 summarizes the consequences of the LBIST runs.

表 11-3. LBIST Control and Status

LBIST_EN(3)	LBIST_DIAG_EN(3)	LBIST_DONE (4)	LBIST_CORE_ERR	LBIST_DIAG_ERR	DEVICE STATE
0b	0b	No change	No change	No change	No state change
0b	1b	1b	No change	0(1)	No state change
0b	1b	1b	No change	1b	SAFE
1b	0b	1b	0b(2)	No change	No state change
1b	0b	1b	1b	No change	SAFE

(1) This value assumes that the LBIST_DIAG_ERR bit was set to 0b prior to setting the LBIST_DIAG_EN bit.
(2) This value assumes that the LBIST_CORE_ERR bit was set to 0b prior to setting the LBIST_EN bit.
(3) TI does not recommended setting both the LBIST_EN and LBIST_DIAG_EN bits at the same time. In this case, the LBIST_DIAG_EN bit setting has higher priority.
(4) If the system MCU keeps polling the LBIST_DONE status bit while the LBIST is in progress, the bit reads 0b until the LBIST is complete and until the SPI communication is restored. However, the first read command after the LBIST completion can generate a SPI format error, which is noted by the SPI_ERR[1:0] bit when set to 10b at the next read command. The LBIST_DONE bit is then the accurate representation of the LBIST status during this same SPI read command. TI recommends that the MCU read the bit again and confirm the bit is cleared back to 0b.

11.9.6 Junction Temperature Monitors

The device has three die junction temperature monitors that sense the die temperature near the power MOSFETs in the BUCK1 regulator, BUCK2 regulator, and BOOST converter. Each monitor has a warning threshold (T_{WARN_TH}) and a shutdown threshold (T_{STD_TH}), and the SPI register has separate status bits to indicate an overtemperature warning event and overtemperature shutdown event. In addition to the status bit in the SPI register, an overtemperature warning event from each regulator can be configured by writing to the DEV_CFG2 register, to interrupt the system MCU by pulling the ENDRV/nIRQ pin low.

If an overtemperature shutdown condition is detected from any regulator, then the device turns off the corresponding regulator. Refer to Thermal Warning and Shutdown Protection (Monitoring and Protection), Thermal Sensor Warning and Thermal Shutdown Protection (Monitoring and Protection), and Thermal Sensor Warning and Shutdown Protection (Monitoring and Protection) for details on device behavior in the event of junction overtemperature. The ABIST runs the diagnostic check on the junction temperature monitors.

表 11-4 provides an overview of junction temperature monitoring.

表 11-4. Junction Overtemperature Protection Overview

VOLTAGE RAIL	DETECTION THRESHOLD RANGE		DEGLITCH TIME	DEVICE BEHAVIOR UPON DETECTION (SPI FLAG, STATE TRANSITION, NRES/ENDRV PIN STATUS)	
	WARN	SHUTDOWN		WARN	SHUTDOWN(1)
BUCK1	150°C to 170°C	170°C to 190°C	60 µs to 80 µs	SAFETY_BUCK1_STAT2[0] No change in state NRES = 1, ENDRV/nIRQ = 0 if BUCK1_OT_WARN_IRQ_EN = 1b, No change in NRES and ENDRV/nIRQ if BUCK1_OT_WARN_IRQ_EN = 0b	SAFETY_BUCK1_STAT2[1] OFF state if BUCK1_OT_OFF_EN = 1b, SAFE state(2) if BUCK1_OT_OFF_EN = 0b NRES = 0, ENDRV/nIRQ = 0 if BUCK1_OT_OFF_EN = 1b NRES = 1, ENDRV/nIRQ = 0 if BUCK1_OT_OFF_EN = 0b
BUCK2				SAFETY_BUCK2_STAT2[0] No change in state NRES = 1, ENDRV/nIRQ = 0 if BUCK2_OT_WARN_IRQ_EN = 1b No change in NRES and ENDRV/nIRQ if BUCK2_OT_WARN_IRQ_EN = 0b	SAFETY_BUCK2_STAT2[1] SAFE state(3) NRES = 1, ENDRV/nIRQ = 0
BOOST				SAFETY_BOOST_STAT2[0] No change in state NRES = 1, ENDRV/nIRQ = 0 if BOOST_OT_WARN_IRQ_EN = 1b No change in NRES and ENDRV/nIRQ if BOOST_OT_WARN_IRQ_EN = 0b	SAFETY_BOOST_STAT2[1] SAFE state(4) NRES = 1, ENDRV/nIRQ = 0

(1) After the regulator is turned off because of an overtemperature shutdown condition, the regulator cannot be enabled again until the die junction temperature decreases to less than the $T_{WARN\_TH} - T_{WARN\_TH\_HYS}$.
(2) All three regulators are turned off.
(3) The BUCK2 regulator is turned off with the BUCK2_EN control bit cleared to 0b.
(4) The BOOST converter is turned off with the BOOST_EN control bit cleared to 0b.

11.9.7 Current Limit

The integrated power MOSFETs of all switched-mode regulators are protected by current-limit circuits that detect overcurrent events. The current-limit circuit in each regulator detects an overload and short-circuits event. An overload event occurs when a regulator is loaded with a load greater than the value specified in Specifications. As the output load continues to increase, the current-limit circuit detects short-circuit events and the corresponding regulator is turned off. The LS power MOSFETs in the BUCK1 and BUCK2 regulators and the HS power MOSFET in the BOOST converter are also protected from an reverse sink overcurrent event, which can occur if the switch pins (PHx) are short-circuited either to supply or to ground, depending on the regulator topology. The SPI register has separate status bits for the overload, short-circuit, and reverse sink overcurrent events for each regulator. For more information on the device behavior when an overcurrent event is detected, see Overcurrent Protection (Monitoring and Protection), セクション 11.4.4, and Output Voltage Monitoring (Monitoring and Protection). The ABIST runs the diagnostic check on the current-limit circuits.

表 11-5 provides an overview of current-limit protection.

表 11-5. Current-Limit Protection Overview

VOLTAGE RAIL	CURRENT LIMIT THRESHOLD(1)			DEVICE BEHAVIOR UPON DETECTION (SPI FLAG, STATE TRANSITION, NRES/ENDRV PIN STATUS)		
	OVERLOAD	SHORT-CIRCUIT	REVERSE OVERCURRENT	OVERLOAD	SHORT-CIRCUIT	REVERSE OVERCURRENT
BUCK1	5 A	7 A	–2.5 A	SAFETY_BUCK1_STAT1[1] No change in state NRES = 1, ENDRV/nIRQ = 1	SAFETY_BUCK1_STAT1[0] OFF state if BUCK1_SCG_OFF_EN = 1, SAFE state(2) if BUCK1_SCG_OFF_EN = 0 NRES = 0, ENDRV/nIRQ = 0 if BUCK1_SCG_OFF_EN = 1 NRES = 1, ENDRV/nIRQ = 0 if BUCK1_SCG_OFF_EN = 0	SAFETY_BUCK1_STAT1[2] OFF state if BUCK1_LS_SINK_OVC_OFF_EN = 1b, SAFE state(2) if BUCK1_LS_SINK_OVC_OFF_EN = 0b NRES = 0, ENDRV/nIRQ = 0 if BUCK1_LS_SINK_OVC_OFF_EN = 1b NRES = 1, ENDRV/nIRQ = 0 if BUCK1_LS_SINK_OVC_OFF_EN = 0b
BUCK2	3.1 A	4. A	–1.1 A	SAFETY_BUCK2_STAT1[1] No change in state NRES = 1, ENDRV/nIRQ = 1	SAFETY_BUCK2_STAT1[0] SAFE state(3) NRES = 1, ENDRV/nIRQ = 0	SAFETY_BUCK2_STAT1[2] SAFE state(3) NRES = 1, ENDRV/nIRQ = 0

表 11-5. Current-Limit Protection Overview (続き)

VOLTAGE RAIL	CURRENT LIMIT THRESHOLD(1)			DEVICE BEHAVIOR UPON DETECTION (SPI FLAG, STATE TRANSITION, NRES/ENDRV PIN STATUS)		
	OVERLOAD	SHORT-CIRCUIT	REVERSE OVERCURRENT	OVERLOAD	SHORT-CIRCUIT	REVERSE OVERCURRENT
BOOST	1.8 A	2.7 A	–1.25 A	SAFETY_BOOST_STAT1[1] No change in state NRES = 1, ENDRV/nIRQ = 1	SAFETY_BOOST_STAT1[0] SAFE state(4) NRES = 1, ENDRV/nIRQ = 0	SAFETY_BOOST_STAT1[2] SAFE state(4) NRES = 1, ENDRV/nIRQ = 0

(1) Inductor and switch peak current.
(2) All three regulators are turned off.
(3) The BUCK2 regulator is turned off with the BUCK2_EN control bit cleared to 0b.
(4) The BOOST controller is turned off with the BOOST_EN control bit cleared to 0b.

11.9.8 Loss of Ground (GND)

A loss-of-GND detection circuit monitors the voltage difference between the power-ground pins (PGNDx) of the switched-mode regulator and the analog ground pin (AGND). If the voltage difference is either less than the V_{GLTH_LOW} or greater than the V_{GLTH_HIGH}, the related switched-mode regulator is disabled and cannot be enabled again as long as the condition is still present. The device state after a loss-of-GND detection is determined by the device configuration.

In case of a loss-of-PGND event on the BUCK1 regulator, the following occurs for the bit settings listed as follows:

- If the BUCK1_PGND_LOSS_OFF_EN bit is set to 1b the following occurs:
  - The BUCK1 regulator, BUCK2 regulator, and BOOST converter are disabled with activated internal resistor discharge.
  - The BUCK1_PGND_LOSS status bit is set.
  - The device goes into the OFF state.
  - The BUCK1 PGND-loss bit is latched in the Analog_Latch.
- If the BUCK1_PGND_LOSS_OFF_EN bit is set to 0b the following occurs:
  - The BUCK1 regulator, BUCK2 regulator, and BOOST converter are disabled without activating internal resistive discharge.
  - The BUCK1_PGND_LOSS status bit is set.
  - The BUCK2_EN and BOOST_EN control bits are cleared.
  - The device goes into the SAFE state.
  - The device error counter increments.
  - An interrupt to the system MCU is generated (driving the ENDRV/nIRQ pin low).

> 注
>
> Because at least one undervoltage event of the three regulators should be configured as a global RESET condition, the device eventually goes into to the RESET state as the regulator outputs discharge to less than its UV-threshold levels. When the device is in the RESET state, the BUCK1 regulator is automatically enabled again if the BUCK1 loss-of-GND event is no longer detected.

In case of a loss-of-PGND event for the BUCK2 regulator the following occurs:

- The BUCK2 regulator is disabled without activating internal resistive discharge.
- The BUCK2_EN control bit is cleared.
- The BUCK2_PGND_LOSS status bit is set.
- The device goes into the SAFE state.
- The device error counter increments.
- An interrupt to the system MCU is generated (driving the ENDRV/nIRQ pin low).
- If the BUCK2 undervoltage event is configured as a global RESET state condition (the BUCK2_UV_RST_EN bit is set to 1b), the device goes into the RESET state as the V_{BUCK2} output voltage discharges to less than its UV-threshold level.
- If the BUCK2 undervoltage event is not configured as a global RESET state condition (the

BUCK2_UV_RST_EN bit is set to 0b), the device does not change the state. The system MCU can try to enable the BUCK2 regulator by setting the BUCK2_EN control bit.

In case of a loss-of-PGND event on the BOOST converter the following occurs:

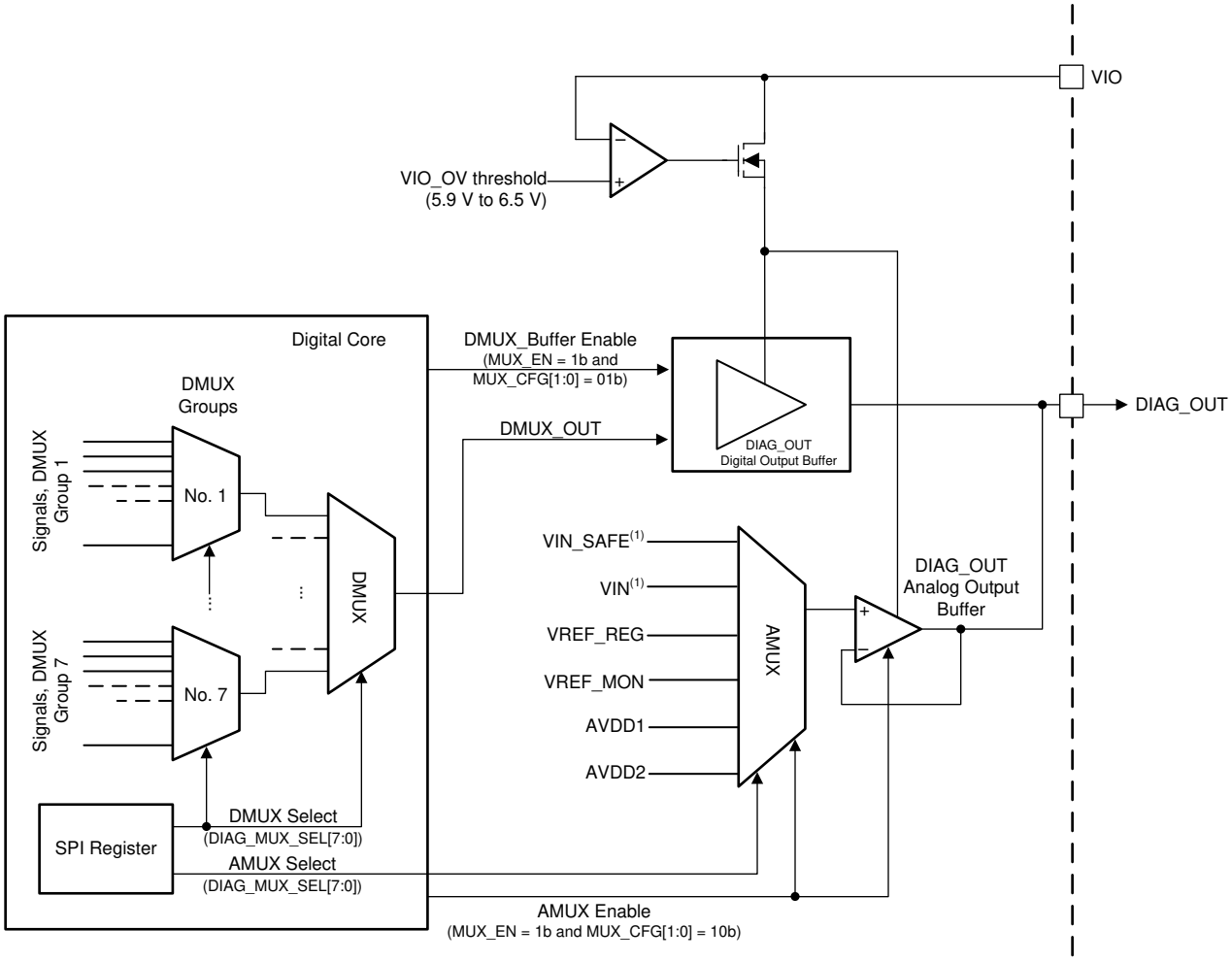
- The BOOST converter is disabled.
- The BOOST_EN control bit is cleared.
- The BOOST_PGND_LOSS status bit is set.
- If the BOOST undervoltage event is configured as a global RESET condition (the BOOST_UV_RST_EN bit is set to 1b), the device goes into the RESET state as the V_{BOOST} output voltage discharges to less than its UV-threshold level.
- If the BOOST undervoltage event is not configured as a global RESET condition (the BOOST_UV_RST_EN bit is set to 0b), the device stays in the current state. The system MCU can try to enable the BOOST converter by setting the BOOST_EN control bit.

11.9.9 Diagnostic Output Pin (DIAG_OUT)

The multiplexer switches internal analog and digital signals to the DIAG_OUT pin. The SPI register DIAG_MUX_SEL sets the mode of this multiplexer. Both the analog and digital signals have separate buffers (AMUX buffer and DMUX buffer) for sufficient drive capability.

The MUX_CFG[1:0] bits in the DIAG_CTRL register selects the type of signal (either analog or digital) on the DIAG_OUT pin. The MUX_EN control bit in the DIAG_CTRL register enables the DIAG_OUT multiplexer output. When disabled, the DIAG_OUT pin is in the high-impedance state.

The VIO pin supplies both the AMUX buffer and DMUX buffer. When an overvoltage event occurs on the VIO pin, the device disconnects the supply to the AMUX and DMUX buffers as shown in 図 11-14.



1. The marked analog signals are connected to the AMUX through a resistor divider.

図 11-14. DIAG_OUT Analog and Digital MUX

11.9.9.1 Analog MUX Mode on DIAG_OUT

表 11-6 lists the selectable analog internal signals on the DIAG_OUT pin. In the DIAG_CTRL register, the MUX_CFG[1:0] bits must be set to 10b for the analog MUX mode. In this mode, the digital output buffer (see DIAG_OUT Analog and Digital MUX) is in the high-impedance state.

表 11-6. AMUX Channel Selection

CHANNEL NUMBER	VOLTAGE RAIL OR SIGNAL NAME	DESCRIPTION	DIVIDE RATIO	CHANNEL NUMBER SELECTION THROUGH DIAG_MUX_SEL[7:0]
A.0	RESERVED	No signal (analog driver disabled)	—	0xx
A.1	VIN_SAFE	Device input supply for monitoring circuitry	20 ± 2%	0x01
A.2	VIN	Device input supply for switched-mode regulators	20 ± 2%	0x02
A.3	VREF_REG	Voltage reference for regulators	1	0x03
A.4	VREF_MON	Voltage reference for monitoring circuitry	1	0x04
A.5	AVDD1	Internal LDO for low-voltage circuitry in regulators	4.375	0x05
A.6	AVDD2	Internal LDO for monitoring circuitry	4.375	0x06

表 11-6. AMUX Channel Selection (続き)

CHANNEL NUMBER	VOLTAGE RAIL OR SIGNAL NAME	DESCRIPTION	DIVIDE RATIO	CHANNEL NUMBER SELECTION THROUGH DIAG_MUX_SEL[7:0]
A7–A.255	RESERVED	No signal (analog driver disabled)	—	0x07 through 0xFF

11.9.9.2 Digital MUX Mode on DIAG_OUT

表 11-7 lists the selectable digital internal signals on the DIAG_OUT pin. In the DIAG_CTRL register, the MUX_CFG[1:0] bits must be set to 01b for DMUX mode. In this mode, the analog output buffer (see DIAG_OUT Analog and Digital MUX) is in the high-impedance state.

Most of these signals are internal error signals which influence the device state and behavior of the NRES and ENDRV pins.

表 11-7. DMUX Channel Selection

CHANNEL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL[6:4]	CHANNEL NUMBER SELECTION THROUGH DIAG_MUX_SEL[3:0]
D0.0	RESERVED	Reserved, logic 0	000b	0000b
D0.1	VREG_UV	VREG undervoltage comparator output	000b	0001b
D0.2 - D0.6	RESERVED	Reserved, logic 0	000b	0010b through 0110b
D0.7	BUCK1_UV	BUCK1 undervoltage comparator	000b	0111b
D0.8	BUCK1_OV	BUCK1 overvoltage comparator	000b	1000b
D0.9	BUCK2_UV	BUCK2 undervoltage comparator	000b	1001b
D0.10	BUCK2_OV	BUCK2 overvoltage comparator	000b	1010b
D0.11	BOOST_UV	BOOST undervoltage comparator	000b	1011b
D0.12	BOOST_OV	BOOST overvoltage comparator	000b	1100b
D0.13	RESERVED	Reserved, logic 0	000b	1101b
D0.14	RESERVED	Reserved, logic 0	000b	1110b
D0.15	VIO_OV	VIO overvoltage comparator	000b	1111b
D1.0	SYNC_OUT	Synchronization SYNC_OUT clock output	001b	0000b
D1.1	SYSCLK	System-clock source (8 MHz ± 5%)	001b	0001b
D1.2	PLL_CLK	PLL clock output	001b	0010b
D1.3	SYNC_IN	Synchronization SYNC_IN clock source	001b	0011b
D1.4	$f_{SW\_BUCK1\_CLK}$	BUCK1 switched-mode regulator clock source	001b	0100b
D1.5	$f_{SW\_BUCK2\_CLK}$	BUCK2 switched-mode regulator clock source	001b	0101b
D1.6	RESERVED	Reserved, logic 0	001b	0110b
D1.7	$f_{SW\_BOOST\_CLK}$	BOOST switched-mode regulator clock source	001b	0111b
D1.8–D1.15	RESERVED	Reserved, logic 0	001b	1000b through 1111b
D2.0	RESERVED	Reserved, logic 0	010b	0000b
D2.1	BUCK1_HS_ILIM	BUCK1 HS current-limit signal	010b	0001b
D2.2	BUCK1_LS_ILIM	BUCK1 LS current-limit signal	010b	0010b
D2.3	BUCK1_LS_S_ILIM	BUCK1 LS sink current-limit signal	010b	0011b
D2.4	BUCK1_OVP	BUCK1 overvoltage protection comparator	010b	0100b
D2.5	BUCK1_OT	BUCK1 overtemperature	010b	0101b
D2.6	BUCK2_HS_ILIM	BUCK2 HS current-limit signal	010b	0110b

表 11-7. DMUX Channel Selection (続き)

CHANNEL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL[6:4]	CHANNEL NUMBER SELECTION THROUGH DIAG_MUX_SEL[3:0]
D2.7	BUCK2_LS_ILIM	BUCK2 LS current-limit signal	010b	0111b
D2.8	BUCK2_LS_S_ILIM	BUCK2 LS sink current-limit signal	010b	1000b
D2.9	BUCK2_OVP	BUCK2 overvoltage protection comparator	010b	1001b
D2.10	BUCK2_OT	BUCK2 overtemperature	010b	1010b
D2.11	BOOST_LS_ILIM	BOOST LS current-limit signal	010b	1011b
D2.12	BOOST_HS_ILIM	BOOST HS current-limit signal	010b	1100b
D2.13	BOOST_HS_S_ILIM	BOOST HS sink current-limit signal	010b	1101b
D2.14	BOOST_OVP	BOOST overvoltage protection comparator	010b	1110b
D2.15	BOOST_OT	BOOST overtemperature	010b	1111b
D3.0	RESERVED	Reserved, logic 0	011b	0000b
D3.1	BUCK1_OT_WARN	BUCK1 overtemperature warning	011b	0001b
D3.2	BUCK2_OT_WARN	BUCK2 overtemperature warning	011b	0010b
D3.3	BOOST_OT_WARN	BOOST overtemperature warning	011b	0011b
D3.4 – D3.15	RESERVED	Reserved, logic 0	011b	0100b through 1111b
D4.0 – D4.15	RESERVED	Reserved, logic 0	100b	0000b through 1111b
D5.0 – D5.15	RESERVED	Reserved, logic 0	101b	0000b through 1111b
D6.0 – D6.15	RESERVED	Reserved, logic 0	110b	0000b through 1111b
D7.0 - D7.15	RESERVED	Reserved, logic 0	111b	0000b through 1111b

11.9.9.2.1 MUX-Output Control Mode

For a diagnostic interconnect check between the DIAG_OUT pin and the analog-and-digital input pin of the MCU, the state of the DIAG_OUT pin is controlled with the MUX_OUT SPI bit in the DIAG_CTRL register. To use this mode, the MUX_CFG[1:0] bits must be set to 00b in the DIAG_CTRL register for MUX output-control mode.

11.9.9.2.2 Device Interconnect Mode

To perform a diagnostic interconnect check at the digital input pins (the MCU_ERR, NCS, SDI, and SCK pins), the MUX_CFG[1:0] bits in the DIAG_CTRL register must be set to 11b for device interconnect mode. Use the INT_CON[2:0] bits in the DIAG_CTRL register to select which of these digital inputs are multiplexed to the DIAG_OUT pin.

A diagnostic check at the SDO digital-output pin is also possible in DMUX mode. This check uses the sequence that follows:

- Set the INT_CON[2:0] bits in the DIAG_CTRL register to 111b.
- Keep the SPI NCS pin HIGH.
- Use the SPI_SDO bit (bit D6 in the DIAG_CTRL register) to control the state of the SPI_SDO output buffer.

During this SPI_SDO output buffer check, the SPI_SDO input buffer is observed on the DIAG_OUT pin.

11.9.10 Watchdog

The TPS65313-Q device includes a closed-loop digital-watchdog (WD) function that operates in two different modes to monitor the external MCU. The WD requires specific triggers sent by the MCU as SPI messages based on specific, periodic requests (or questions) from the TPS65313-Q1 in both operating modes. The MCU

must send the SPI trigger messages (or answers) at specific timing intervals to correctly service the device WD function, and enable operation of the safing path driver or MCU error interrupt (the ENDRV/nIRQ output pin).

セクション 11.9.10.5.1 explains the WD initialization events.

11.9.10.1 WD Question and Answer Configurations

The TPS65313-Q1 WD function has two different functional modes of operation defined as follows:

Q&A Multi-Answer mode An MCU WD answer is a sequence of four distinct SPI messages in a specific sequence order and timing during RESPONSE WINDOW 1 and RESPONSE WINDOW 2. This functional mode configuration is selected by setting the WD_CFG bit to 0b in the SAFETY_CFG3 register.

Q&A Single-Answer mode An MCU WD answer is a single SPI message sent during the watchdog OPEN WINDOW. This functional mode configuration is selected by setting the WD_CFG bit to 1b.

For both WD modes and when the device is in the DIAGNOSTIC state, the device provides a WD pending question through the SPI-mapped WDT_QUESTION_VALUE register and its WD_QUESTION[3:0] bits. The MCU performs a fixed series of arithmetic operations on the WD question value and returns a single WD answer (in a Q&A single-answer mode) or four WD answers (in a Q&A multi-answer mode) to the device by writing to the WDT_ANSWER register.

The WD answers provided by the system MCU are considered correct when the following occurs:

- For WD Q&A multi-answer mode:
  - All answers have the correct value.
  - Answers were received in the correct sequence order.
  - Answers were received in the correct timing intervals during RESPONSE WINDOW 1 and RESPONSE WINDOW 2.
- For WD Q&A single-answer mode:
  - The answer has the correct value.
  - The answer was received during the active OPEN WINDOW.

The WD answer provided by the system MCU is considered incorrect when one of the following occurs:

- The MCU returns SPI answers before or after the correct timing window.
- The MCU returns an incorrectly calculated WD answer.
- The MCU returns the correct answers in the wrong sequence.

A WD time-out event occurs if the MCU fails to send any WD-related SPI responses during programmed WD windows (RESPONSE WINDOW 1 and RESPONSE WINDOW 2 for WD Q&A multi-answer mode, or OPEN WINDOW and CLOSE WINDOW for WD Q&A single-answer mode). A WD time-out event is considered a *no answer event* and the TIME_OUT status bit is set. Each WD TIME_OUT event increments the WD_FAIL_CNT[3:0] counter by 1 and is followed by the start of a new WD Q&A sequence run.

The WD TIME_OUT event can be used by the MCU application software (SW) to establish synchronization between the device and MCU SW and HW processes. Each WD TIME_OUT event is followed by the start of a new WD Q&A sequence run. Another way to synchronize the MCU and the device WD function is updating the device WD configuration or WD window duration. Each configuration update increments the WD_FAIL_CNT[3:0] counter by 1, followed by the start of a new WD Q&A sequence run. All events that trigger new WD cycle start are covered in WD Function Initialization 表 11-13. The default setting for WD_RST_EN bit is 1b.

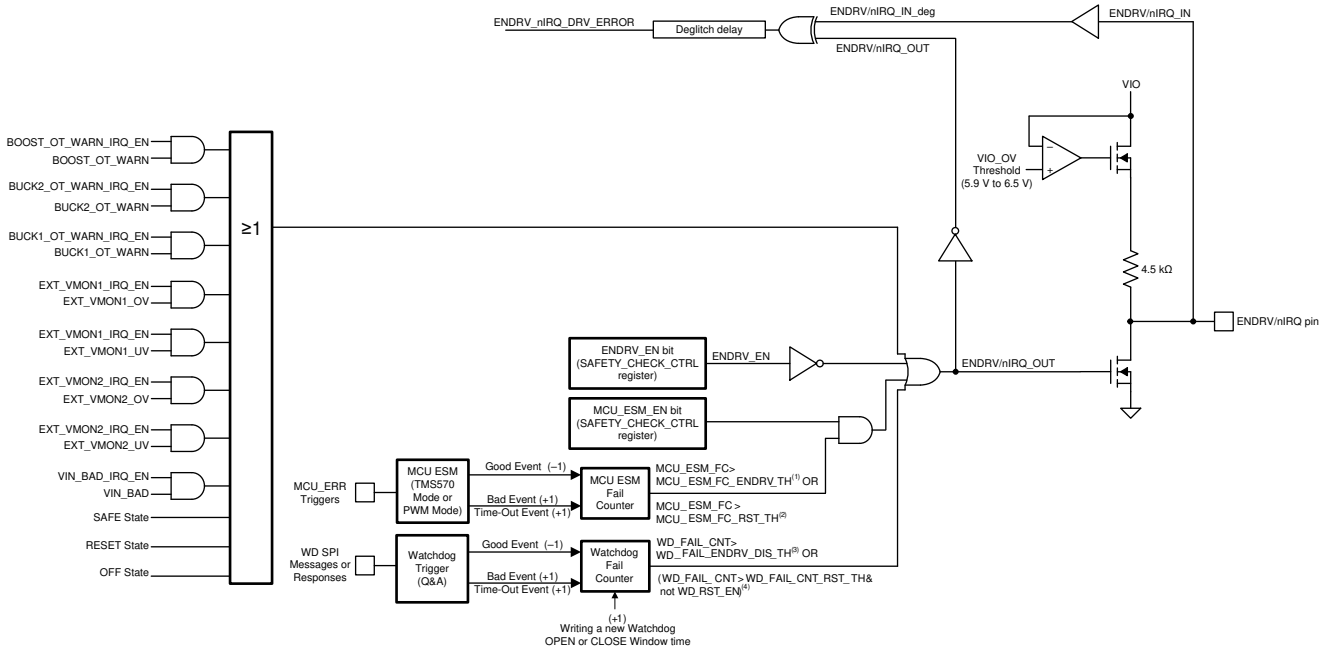
11.9.10.2 WD Failure Counter and WD Status

The WD function uses a WD failure counter (WD_FAIL_CNT[3:0]) to track correct and incorrect MCU answers. The WD_FAIL_CNT[3:0] counter increments for each incorrect answer and decrements for each correct answer.

The WD_FAIL_CNT[3:0] counter is updated by the following events when the device is in the DIAGNOSTIC or ACTIVE or SAFE state:

- A correct WD answer decrements the WD_FAIL_CNT[3:0] counter by 1.
- A wrong WD answer increments the WD_FAIL_CNT[3:0] counter by 1.
- An incomplete or missing WD answer for the duration of the programmed WD sequence duration (or WD time-out event) increments the WD_FAIL_CNT[3:0] counter by 1 and sets the TIME_OUT status bit in the WDT_STATUS register.
- Any change in the WD_CFG bit, WD window time durations (WDT_WIN1_CFG or WDT_WIN2_CFG register), or WD answer generation configurations (WDT_QA_CFG register) increments the WD_FAIL_CNT[3:0] counter by 1.

When the value of the WD_FAIL_CNT[3:0] counter is less than the value set by the WD_FC_ENDRV_TH[3:0] bits, the WD function is considered to be *in range*, and the device keeps the WD-enabled function active (the ENDRV/nIRQ driver can be activated and the ENDRV/nIRQ pin is pulled high). The WD-enabled function is enabled by setting the ENDRV_EN control bit in the SAFETY_CHECK_CTRL register. When the value of the WD_FAIL_CNT[3:0] counter is greater than the value set by the WD_FC_ENDRV_TH[3:0] bits in the SAFETY_CFG4 register, the WD function is considered to be *out of range*, and the device disables the WD-enabled ENDRV/nIRQ function by driving ENDRV/nIRQ pin low. 図 11-15 summarizes the settings of the WD status bits depending on the WD_FAIL_CNT[3:0] counter value with respect to the WD_FC_ENDRV_TH[3:0] bits value.



1. When the condition is met, the device goes from the ACTIVE or DIAGNOSTIC state to the SAFE state. No action occurs if the device is in the SAFE state.
2. When the condition is met, the device stays in the ACTIVE state if the MCU_ESM_RST_EN bit is 0b. When the condition is met, the device goes from the ACTIVE or DIAGNOSTIC state to the RESET state if the MCU_ESM_RST_EN bit is 1b
3. When the condition is met, the device does not go from the ACTIVE or DIAGNOSTIC state to the SAFE state.
4. When the condition is met, the device goes from the ACTIVE or DIAGNOSTIC state to the SAFE state.

図 11-15. Watchdog Impact on ENDRV/nIRQ Output Function

表 11-8. WD Fail Counter Ranges for ENDRV Function

WD STATUS BITS	WD_FAIL_CNT[3:0] = 0b	0b < WD_FAIL_CNT[3:0] < WD_FC_ENDRV_TH[3:0](2)	WD_FAIL_CNT[3:0] ≥ WD_FC_ENDRV_TH[3:0](3)
WD_FAIL(1)	0b	1b	1b

表 11-8. WD Fail Counter Ranges for ENDRV Function (続き)

WD STATUS BITS	WD_FAIL_CNT[3:0] = 0b	0b < WD_FAIL_CNT[3:0] < WD_FC_ENDRV_TH[3:0](2)	WD_FAIL_CNT[3:0] ≥ WD_FC_ENDRV_TH[3:0](3)
WD_ENDRV_FAIL	0b	0b	1b

(1) The WD_FAIL status bit is set each time the WD_FAIL_CNT[3:0] counter increments.
(2) The WD is in range.
(3) The WD is out of range.

If the WD_RST_EN configuration bit in the SAFETY_CFG3 register is set to 1b, the WD generates a reset to the MCU by driving NRES pin low when the WD_FAIL_CNT[3:0] counter reaches the programmed threshold set by the WD_FC_RST_TH[3:0] bits. 表 11-9 summarizes the WD status bits and device state depending on the WD_FAIL_CNT[3:0] counter value with respect to WD_FC_RST_TH[3:0] bits value.

表 11-9. WD Fail Counter Ranges for WD Reset

WD STATUS BITS	WD_FAIL_CNT[3:0] = 0b	0b < WD_FAIL_CNT[3:0] < WD_FC_RST_TH[3:0](2)	WD_FAIL_CNT[3:0] = WD_FC_RST_TH[3:0] and WD_RST_EN = 1b(3)	WD_FAIL_CNT[3:0] = WD_FC_RST_TH[3:0] and WD_RST_EN = 0b(3)
WD_FAIL(1)	0b	1b	1b	1b
WD_RST_FAIL	0b	0b	1b	1b
Device State	No change	No change	RESET state (4)	SAFE state

(1) The WD_FAIL status bit is set each time the WD_FAIL_CNT[3:0] increments.
(2) The WD is in range.
(3) The WD is out of range.
(4) When device was in DIAGNOSTIC or ACTIVE state, or device was in SAFE state and SAFE_EXIT SPI command is received.

When a NPOR event occurs, the WD_FAIL_CNT[3:0] counter is initialized to 0x05, which is the initial value of the WD_FC_ENDRV_TH[3:0] bits. While the device is in the DIAGNOSTIC state, the MCU can set the desired WD_FC_ENDRV_TH[3:0] and WD_FC_RST_TH[3:0] values. Setting new WD_FC_ENDRV_TH[3:0] value in DIAGNOSTIC state causes the WD_FAIL_CNT[3:0] counter to be set to the same new value. This WD_FAIL_CNT[3:0] bits update is to make sure that the ENDRV function is initially disabled until correct WD answers are provided by the MCU.

When the WD_FAIL_CNT[3:0] counter reaches a count of 0xF, any new incorrect answer from the MCU does not change the counter value. The counter stays at 0xF. Similarly, when the WD_FAIL_CNT[3:0] counter reaches a count of 0x0, any new correct WD answers do not change the counter value. The counter stays at 0x0.

11.9.10.3 WD SPI Event Definitions

The WD SPI events are defined as follows:

WD Question

The WD question is a 4-bit word (see セクション 11.9.10.5).

This event occurs after a SPI request by the MCU SPI to read the WD question value register (WD_QUESTION[3:0]).

If the SPI frame is not successfully transmitted (a SPI fault is detected), the WD question event does not occur.

The MCU can request the pending active question value at the start of the new WD Q&A sequence run, but this MCU request is not a required condition for achieving a correct WD answer. The MCU can calculate the expected question value by running a question-generation algorithm.

WD Answers in WD Q&A Multi-Answer mode

The WD answer is a 32-bit word containing 4 bytes (WD_ANSWER_RESP_3, WD_ANSWER_RESP_2, WD_ANSWER_RESP_1, and WD_ANSWER_RESP_0).

The response occurs with an MCU write access to the WD_ANSWER[7:0] bits in the WDT_ANSWER register.

	Each WD question requires four WD answers (three answers during RESPONSE WINDOW 1 and one answer during RESPONSE WINDOW 2). The WD_ANSW_CNT[1:0] value is at 0x3 when the WD enters RESPONSE WINDOW 1 and decrements by 1 for each received WD answer.
WD Answers in WD Q&A Single-Answer mode	The WD answer is an 8-bit word, WD_ANSWER_RESP_1. The WD answer occurs with an MCU write access to the WD_ANSWER[7:0] bits during an OPEN WINDOW. WD_ANSW_CNT[1:0] value stays at 0x1.

11.9.10.4 WD Q&A Sequence Run

A new WD Q&A sequence run starts after one of the following:

- A WD time-out event (after the OPEN WINDOW and the CLOSE WINDOW elapse in WD Q&A Single-Answer mode or after RESPONSE WINDOW 1 and RESPONSE WINDOW 2 elapse in WD Q&A Multi-Answer mode without a complete answer from the MCU).
- The modifying of the WD configuration mode or updating of the WD window duration times.
- The writing of the final answer byte (WD_ANSWER_RESP_0) for the previous WD Q&A sequence run.

In the WD Multi-Answer Mode the WD Q&A sequence run starts with RESPONSE WINDOW 1 followed by RESEPONSE WINDOW 2 in WD Q&A multi-answer mode. The WD window duration times ($t_{WD\_RESP\_WIN1}$ and $t_{WD\_RESP\_WIN2}$) are configurable through the WDT_WIN1_CFG and WDT_WIN2_CFG configuration registers when the device is in the DIAGNOSTIC state. Use 式 2 to calculate the time period for RESPONSE WINDOW 1. Use 式 3 to calculate the time period for RESPONSE WINDOW 2.

$$t_{WD\_RESP\_WIN1} = (WD\_RW1C[7:0] + 1) \times 0.55\ ms \quad (2)$$

where the WD_RW1C[7:0] bits are located in the WDT_WIN1_CFG SPI register.

$$t_{WD\_RESP\_WIN2} = (WD\_RW2C[4:0] + 1) \times 0.55\ ms \quad (3)$$

where the WD_RW2C[4:0] bits are located in the WDT_WIN2_CFG SPI register.

In the WD Q&A Single-Answer Mode the WD &A sequence run starts with a CLOSE WINDOW followed by an OPEN WINDOW in WD Q&A single-answer mode. The WD window duration times ($t_{WD\_CLOSE\_WIN}$ and $t_{WD\_OPEN\_WIN}$) are configurable through the WDT_WIN1_CFG and WDT_WIN2_CFG configuration registers when the device is in the DIAGNOSTIC state. Use 式 4 to calculate the time period for CLOSE WINDOW. Use 式 5 to calculate the time period for OPEN WINDOW.

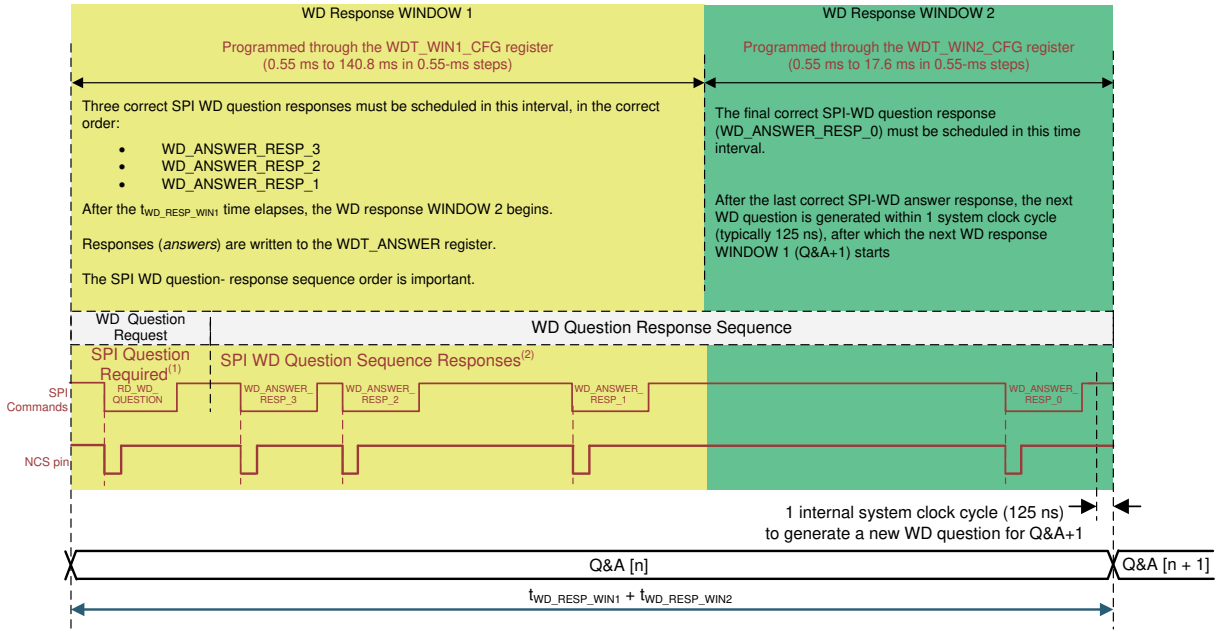
$$t_{WD\_CLOSE\_WIN} = (WD\_CWC[7:0] + 1) \times 0.55\ ms \quad (4)$$

where the WD_CWC[7:0] bits are located in the WDT_WIN1_CFG SPI register.

$$t_{WD\_OPEN\_WIN} = (WD\_OWC[4:0] + 1) \times 0.55\ ms \quad (5)$$

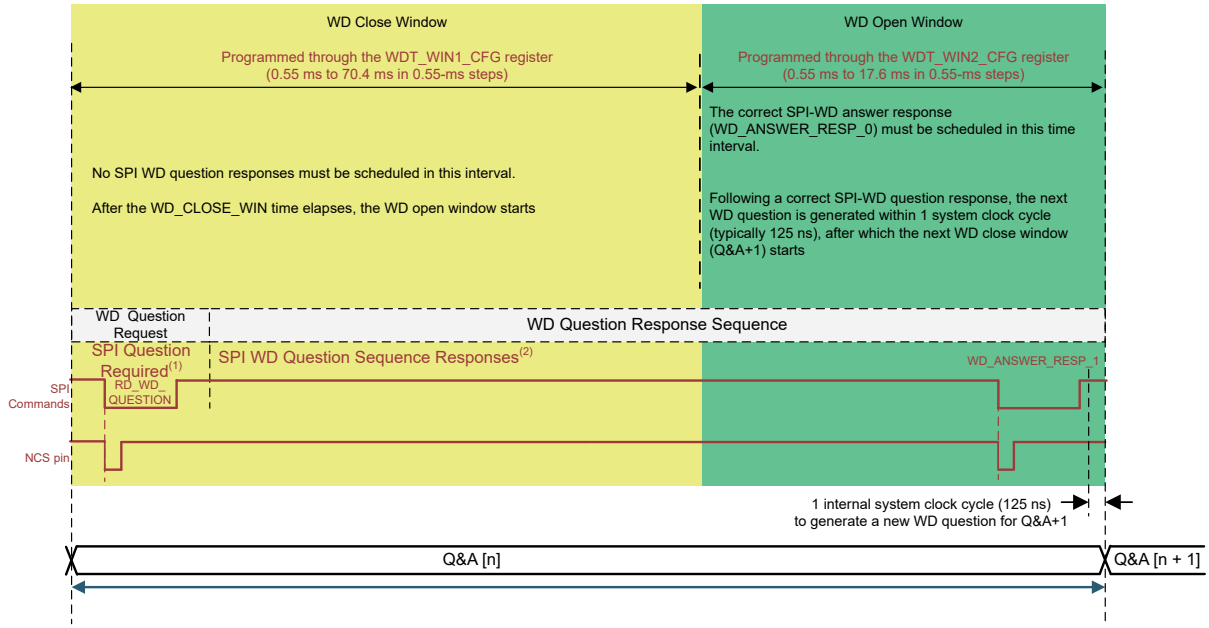
where the WD_OWC[4:0] bits are located in the WDT_WIN2_CFG SPI register.

The WD function uses the internal 8-MHz (with ± 5% accuracy) and the SYSCLK clock as a time reference for creating the 0.55-ms time-step resolution. The SPI SW_LOCK command can be used to lock write access to the WDT_WIN1_CFG and WDT_WIN2_CFG registers.



1. The MCU is not required to request the WD question. The MCU can start with correct answers, WD_ANSWER_RESP_x bytes anywhere within the RESPONSE WINDOW 1. The new WD question is always generated within one system clock cycle after the final WD_ANSWER_RESP_0 answer during the previous WD Q&A sequence run.
2. The MCU can schedule other SPI commands between the WD_ANSWER_RESPx responses (even a command requesting the WD question) without any impact to the WD function as long as the WD_ANSWER_RESP_[3:1] bytes are provided within the RESPONSE WINDOW 1 and WD_ANSWER_RESP_0 is provided within the RESPONSE WINDOW 2.

図 11-16. WD Q&A Sequence Run for WD Q&A Multi-Answer Mode



1. The MCU is not required to request the WD question. The new WD question is always generated within one system clock cycle after the correct WD_ANSWER_RESP_1 byte is provided during the previous WD Q&A sequence run.
2. The MCU must provide a correct answer in the OPEN WINDOW.

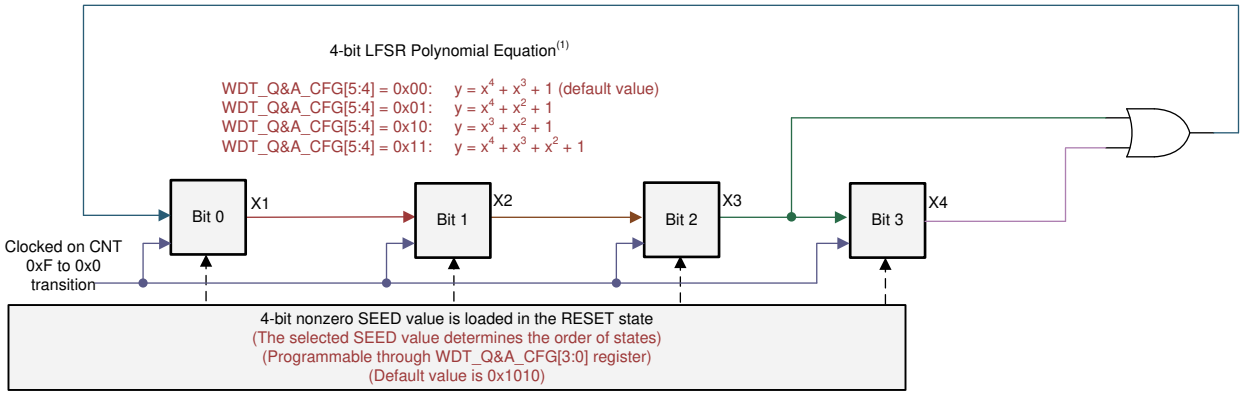
図 11-17. WD Q&A Sequence Run for WD Q&A Single-Answer Mode

11.9.10.5 WD Question and Answer Value Generation

The 4-bit WD question, WD_QUESTION[3:0], is generated by 4-bit Markov chain process. A Markov chain is a stochastic process with Markov property, which means that state changes are probabilistic, and the future state depends only on the current state. The valid and complete WD answer sequence for each WD Q&A mode is as follows:

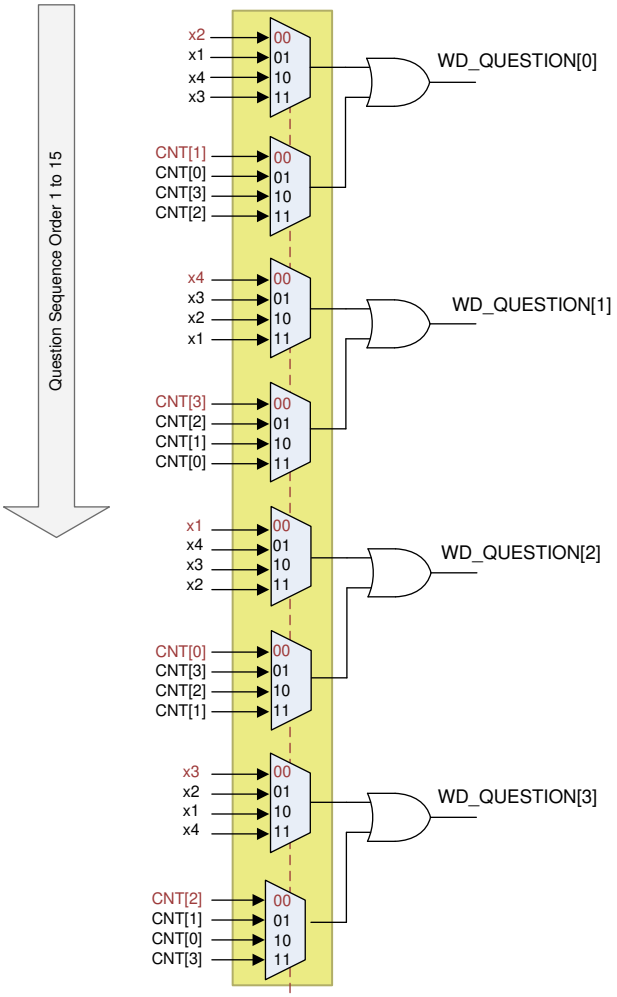
- In WD Q&A multi-answer mode:
  1. Three correct SPI WD answers are received during RESPONSE WINDOW 1.
  2. One correct SPI WD answer is received during RESPONSE WINDOW 2.
  3. In addition to the previously listed timing, the sequence of four responses shall be correct.
- In WD Q&A single-answer mode:
  1. No SPI WD answer is received during the CLOSE WINDOW.
  2. One correct SPI WD answer is received during the OPEN WINDOW.

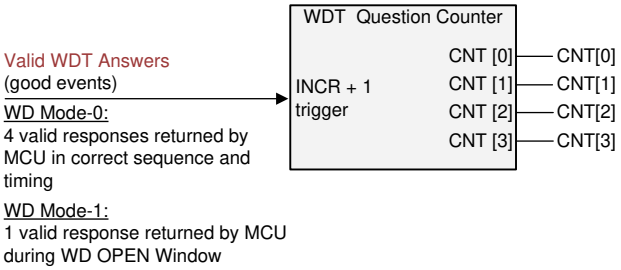
The WD question value is latched in the WD_QUESTION[3:0] bits of the WDT_QUESTION_VALUE register and can be read out at any time.



	X1	X2	X3	X4
SEED	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

The default question-sequence order with the default QUESTION_SEED and FDBK bit values





Feedback settings are controlled through the WDT_Q&A_CFG[7:6] register bit settings (default value 0x00; the signal marked in red)

1. If the current y value is 0000, the next y value will be 0001. The next watchdog question generation process starts from that value.

図 11-18. Watchdog Question Generation

表 11-10. Set of WD Questions and Corresponding WD Answers Using Default Setting

QUESTION IN WD_QUESTION_VALUE REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WDT_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1 (1)	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT[1:0] 11b	WD_ANSW_CNT[1:0] 10b	WD_ANSW_CNT[1:0] 01b	WD_ANSW_CNT[1:0] 00b
0x0	0xFF	0x0F	0xF0	0x00
0x1	0xB0	0x40	0xBF	0x4F
0x2	0xE9	0x19	0xE6	0x16
0x3	0xA6	0x56	0xA9	0x59
0x4	0x75	0x85	0x7A	0x8A
0x5	0x3A	0xCA	0x35	0xC5
0x6	0x63	0x93	0x6C	0x9C
0x7	0x2C	0xDC	0x23	0xD3
0x8	0xD2	0x22	0xDD	0x2D
0x9	0x9D	0x6D	0x92	0x62
0xA	0xC4	0x34	0xCB	0x3B
0xB	0x8B	0x7B	0x84	0x74
0xC	0x58	0xA8	0x57	0xA7
0xD	0x17	0xE7	0x18	0xE8
0xE	0x4E	0xBE	0x41	0xB1
0xF	0x01	0xF1	0x0E	0xFE

(1) This option is used for the WD Q&A Single-Answer mode (the WD_CFG bit is set to 1b).

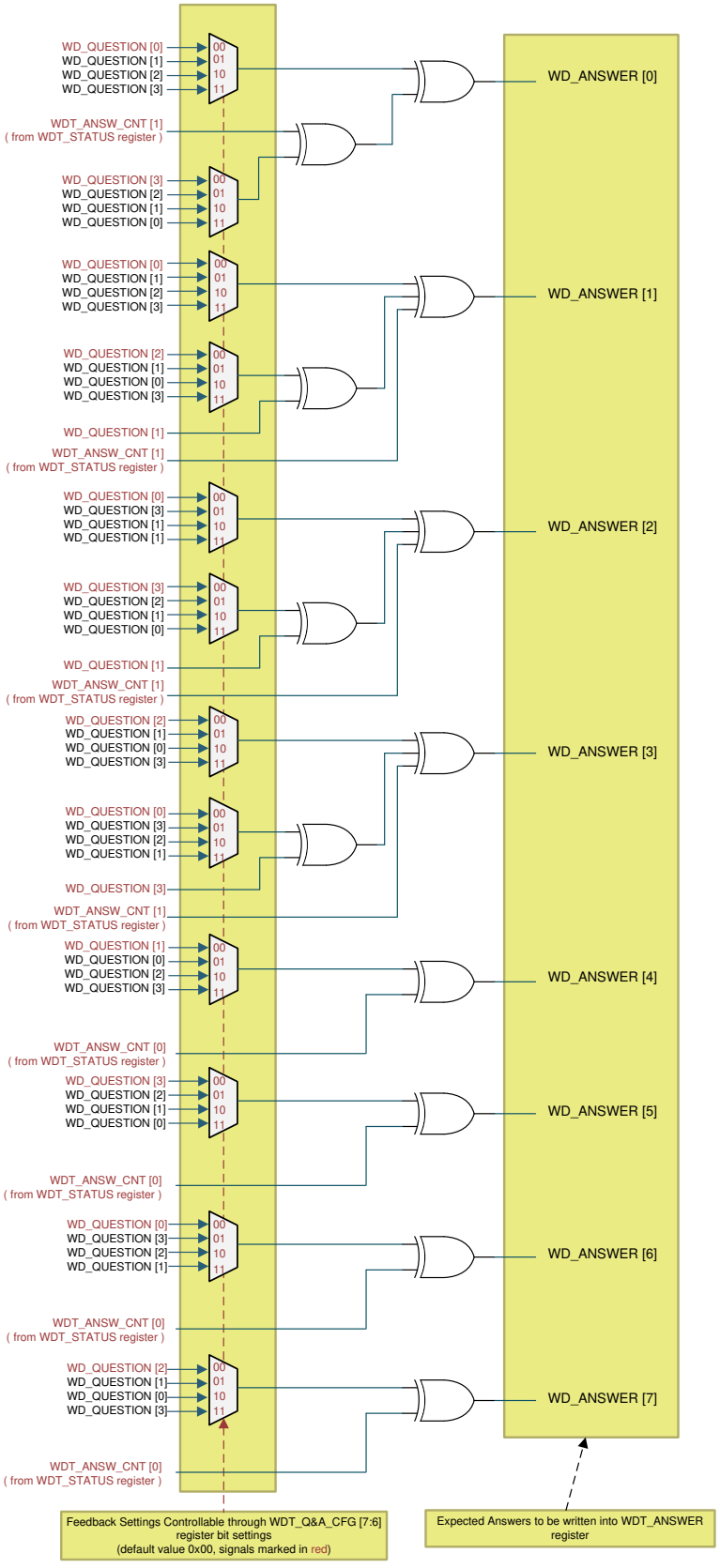


図 11-19. WD Expected Answer Generation

表 11-11. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode (WD_CFG = 0b)

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WDT_STATUS REGISTER				COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		ANSW_ERR	ANSW_EARLY	SEQ_ERR	TIME_OUT	
0 answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	1b	No answers
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	0b	Total WD_ANSW_CNT[1:0] = 4
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	0b	Total WD_ANSW_CNT[1:0] = 4
0 answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 CORRECT answer						
2 CORRECT answer	1 CORRECT answer						
0 answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 INCORRECT answer						
2 CORRECT answer	1 INCORRECT answer						
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	0b	Less than 3 CORRECT ANSWER in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 CORRECT answer						
2 CORRECT answer	2 CORRECT answer						
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	0b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 INCORRECT answer						
2 CORRECT answer	2 INCORRECT answer						
0 answer	3 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	1b	
2 INCORRECT answer	1 CORRECT answer						
0 answer	3 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 INCORRECT answer						
2 INCORRECT answer	1 INCORRECT answer						
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	0b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 CORRECT answer		1b	0b	1b	0b	
2 INCORRECT answer	2 CORRECT answer						
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	0b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 INCORRECT answer						
2 INCORRECT answer	2 INCORRECT answer						

表 11-11. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode (WD_CFG = 0b) (続き)

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WDT_STATUS REGISTER				COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		ANSW_ERR	ANSW_EARLY	SEQ_ERR	TIME_OUT	
3 CORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	0b	0b	0b	1b	Less than 4 CORRECT ANSW in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
2 CORRECT answer	0 answer		0b	0b	1b	1b	
1 CORRECT answer	0 answer						
3 CORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	0b	0b	0b	CORRECT SEQUENCE
3 CORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b	Total WD_ANSW_CNT[1:0] = 4
3 INCORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	1b	Total WD_ANSW_CNT[1:0] < 4
3 INCORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b	Total WD_ANSW_CNT[1:0] = 4
3 INCORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b	Total WD_ANSW_CNT[1:0] = 4
4 CORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	0b	0b	
3 CORRECT answer + 1 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	0b	0b	4 CORRECT or INCORRECT ANSWER in RESPONSE WINDOW 1
2 CORRECT answer + 2 NCORRECT answer	Not applicable						
1 CORRECT answer + 3 NCORRECT answer	Not applicable						

表 11-12. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Single-Answer Mode

NUMBER OF WD ANSWERS AND TIMING		ACTION	WD STATUS BITS IN WDT_STATUS REGISTER			
CLOSE WINDOW	OPEN WINDOW		ANSW_ERR	ANSW_EARLY	SEQ_ERR	TIME_OUT
0 answer	0 answer	-New WD cycle starts after the end of WIN2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	0b	1b
1 CORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 1 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	0b	0b
1 INCORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 1 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	0b	0b
0 answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Decrement WD failure counter -New WD cycle starts with the same WD question	0b	0b	0b	0b

表 11-12. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Single-Answer Mode (続き)

NUMBER OF WD ANSWERS AND TIMING		ACTION	WD STATUS BITS IN WDT_STATUS REGISTER			
CLOSE WINDOW	OPEN WINDOW		ANSW_ERR	ANSW_EARLY	SEQ_ERR	TIME_OUT
0 answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b

The watchdog status bits (ANSW_ERR, ANSW_EARLY, SEQ_ERR, and TIME_OUT) in the WDT_STATUS register are updated at the end of each WD cycle. Read access to the WDT_STATUS register during an active WD cycle returns the status of previous WD cycle and clears the WD status bits.

11.9.10.5.1 WD Initialization Events

表 11-13 lists the multiple events that initialize the WD function and details on what gets initialized by each event.

表 11-13. WD Function Initialization

IMPACT	INITIALIZATION-TRIGGERING EVENT				
	RESET TO DIAGNOSTIC STATE TRANSITION	CHANGE OF THE WD_CFG BIT	CHANGE OF WDT_WINx_CFG OR WD_Q&A_CFG REG	DIAGNOSTIC TO ACTIVE OR SAFE TO DIAGNOSTIC STATE TRANSITION	LBIST RUN COMPLETION
A new WD cycle start	YES	YES	YES	YES	YES
WD_ANSW_CNT[1:0](1)	YES	YES	YES	YES	YES
The WD status flags(2)	YES	YES	YES	YES	YES
WD_CFG_CHG(3)	NO	YES	YES	NO	NO
WDT_QUESTION_VALUE(4)	YES	YES	N/A(10)	NO	YES
WDT_Q&A_CFG register(4)	YES	YES	N/A(10)	NO	NO
WDT_WIN1_CFG and WDT_WIN2_CFG	YES	YES	N/A(10)	NO	NO
WD_FAIL_CNT[3:0]	YES(5)	YES(5)	YES(6)	YES(7)	YES(7)
WD_FC_ENDRV_TH[3:0](5)	YES	YES	NO	NO	NO
WD_FC_RST_TH[3:0](8)	YES	YES	NO	NO	NO
WD_CFG(9)	YES	N/A(10)	NO	NO	NO

(1) This bit is initialized to 0x3 when the WD_CFG bit is set to 0b (WD Q&A multi-answer mode) and to 0x01 when the WD_CFG bit is set to 1 (WD Q&A single-answer mode).
(2) The TIME_OUT, ANSW_ERR, ANSW_EARLY, and SEQ_ERR bits in the WDT_STATUS register and the WD_FAIL bit in the SAFETY_ERR_STAT2 register are all initialized to 0x0.
(3) A YES for this bit means that it is set to 1b.
(4) Along with these registers, the WD question-generation engine is also initialized.
(5) This bit is initialized to 0x5 which is the initial value of the WD_FC_ENDRV_TH[3:0] value.
(6) Increments by 1.
(7) This bit is initialized to the current WD_FC_ENDRV_TH[3:0] value.
(8) This bit is Initialized to 0xF.
(9) This bit is Initialized to 0x0.
(10) The bits or registers will change to reflect the actual values written in each initialization-triggering event.

11.9.11 MCU Error Signal Monitor

The MCU error signal monitor (ESM) monitors the system MCU-error events signaled over the MCU_ERR input pin. The ESM is configurable for two different operating modes. The first mode is TMS570 mode, in which the ESM detects a low-pulse signal with a programmable low-pulse width duration threshold. The second mode is PWM mode, in which the ESM detects a PWM signal with a programmable minimum and maximum pulse-width threshold for the low pulse and high pulse.

The operating mode of the ESM is controlled through the MCU_ESM_CFG bit in the SAFETY_CFG3 SPI register. The ESM is disabled by default, and can be activated by setting the MCU_ESM_EN bit to 1b in the SAFETY_CHECK_CTRL SPI register.

In TMS570 mode, the SAFETY_ERR_PWM_LMAX register sets the threshold of the low-signal duration. When TMS570 mode is enabled and monitoring signal is high, monitoring starts after the first high to low signal transition. If monitoring signal is low when TMS570 mode is enabled and monitoring signal does not transition high for the duration of the $t_{TMS570\_START\_TO}$ start-up time-out window, an error is detected, the ESM failure counter (MCU_ESM_FC[3:0]) is incremented, and the $t_{TMS570\_START\_TO}$ start-up time-out window is restarted again. The duration of the start-up time-out window $t_{TMS570\_START\_TO}$ is set by the SAFETY_ERR_PWM_LMAX register and SAFETY_ERR_PWM_HMAX register setting (t_{PWM_LOWMAX} + $t_{PWM\_HIGHMAX}$).

In PWM mode, the SAFETY_ERR_PWM_LMIN and SAFETY_ERR_PWM_LMAX registers set the thresholds for the minimum and maximum low-pulse durations. The SAFETY_ERR_PWM_HMIN and SAFETY_ERR_PWM_HMAX registers set the thresholds for the minimum and maximum high-pulse durations.

When the PWM mode is enabled, monitoring starts after the rising or falling edge of the signal. If no edge is detected within the time-out window (t_{PWM_LOWMAX} + $t_{PWM\_HIGHMAX}$), then an error is detected and the ESM failure counter (MCU_ESM_FC[3:0]) increments. If the monitored signal duration is shorter than the $t_{PWM\_HIGHMIN}$ or t_{PWM_LOWMIN} time or if the monitored signal duration is longer than the $t_{PWM\_HIGHMAX}$ or t_{PWM_LOWMAX} time, the following occurs:

- An error is detected.
- The MCU_ESM_FC[3:0] failure counter increments.
- A new monitoring cycle starts.

Correct signaling is detected for the low signal when the low-signal duration is from the t_{PWM_LOWMIN} time interval to the t_{PWM_LOWMAX} time interval and is followed by a high-signal width duration from the $t_{PWM\_HIGHMIN}$ time interval to the $t_{PWM\_HIGHMAX}$ time interval. Correct signaling is detected for the high signal when the high-signal duration is from the $t_{PWM\_HIGHMIN}$ time interval to the $t_{PWM\_HIGHMAX}$ time interval and is followed by a low signal with a duration from the SAFETY_ERR_PWM_LMIN interval to the SAFETY_ERR_PWM_LMAX interval.

The MCU_ESM_FC[3:0] counter decrements when a correct signal is detected. When monitoring starts, a new monitoring event starts any time after an error is detected or when correct signaling is detected.

The MCU_ESM_FC[3:0] counter increments after an MCU signaling error is detected. If the device is in the ACTIVE state, the MCU_ESM_FC[3:0] counter is greater than the programmed threshold (MCU_ESM_FC_ENDRV_TH) and MCU_ESM_RST_EN configuration bit is set to 0b, the following occurs:

- The device goes into the SAFE state.
- The ENDRV/nIRQ pin is disabled (driven low).
- The MCU_ESM_FAIL and MCU_ESM_RST_FAIL status bits are set in the SAFETY_ERR_STAT3 register.

If the device is in the DIAGNOSTIC or ACTIVE state, the MCU_ESM_FC[3:0] counter is greater than the MCU_ESM_FC_RST_TH[3:0] threshold, and the MCU_ESM_RST_EN configuration bit is set to 1b, the device goes into the RESET state. The MCU_ESM_FAIL and MCU_ESM_RST_FAIL status bits are also set in the SAFETY_ERR_STAT3 register.

If the device is in the DIAGNOSTIC or ACTIVE state, the MCU_ESM_FC[3:0] counter is greater than the MCU_ESM_FC_RST_TH[3:0] threshold, and the MCU_ESM_RST_EN configuration bit is set to 0b, the device goes into the SAFE state. The MCU_ESM_FAIL and MCU_ESM_RST_FAIL status bits are also set in the SAFETY_ERR_STAT3 register. If the device is already in the SAFE state and if the MCU_ESM_FC_RST_TH[3:0] threshold is equal to or less than the MCU_ESM_FC_ENDRV_TH[3:0] threshold, no action occurs.

Regardless of the configuration mode of the MCU ESM, a new MCU ESM cycle starts and the MCU_ESM_FC[3:0] and MCU_ESM_FAIL status bits are initialized each time one of the following occurs:

- When a NPOR event occurs.
- When the device goes to the RESET state.

- After the LBIST run is complete.
- After the MCU_ESM_CFG bit toggles when changing the ESM configuration mode.
- After the MCU_ESM_EN bit is set to 0b.

Regardless of the configuration mode of the MCU ESM, the MCU_ESM_FC[3:0] bit is initialized to its default value each time one of the following occurs:

- When the device goes into the DIAGNOSTIC state from the SAFE state.
- When the device goes into the RESET state.
- After the LBIST run is complete.
- After the MCU_ESM_EN bit toggles from 0b to 1b.
- After the MCU_ESM_CFG bit toggles from 0b to 1b or from 1b to 0b.

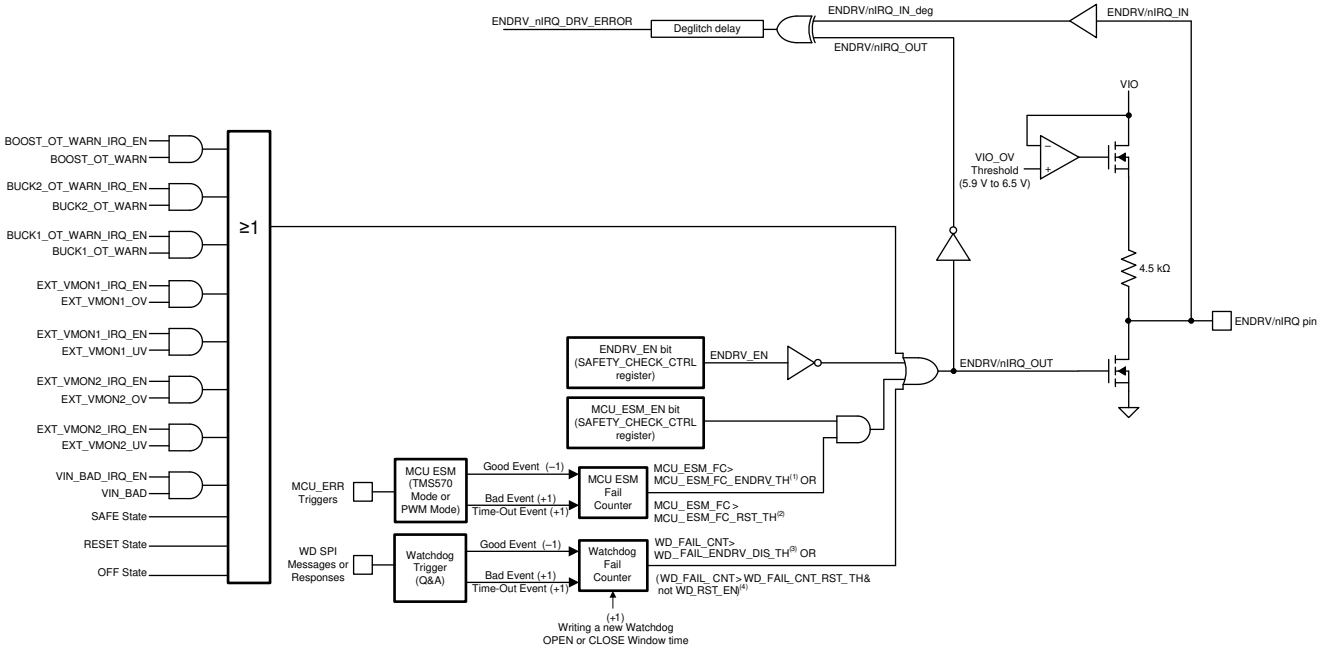


図 11-20. MCU Error Signaling Monitor (ESM) With MCU ESM Failure Counter and WD Failure Counter

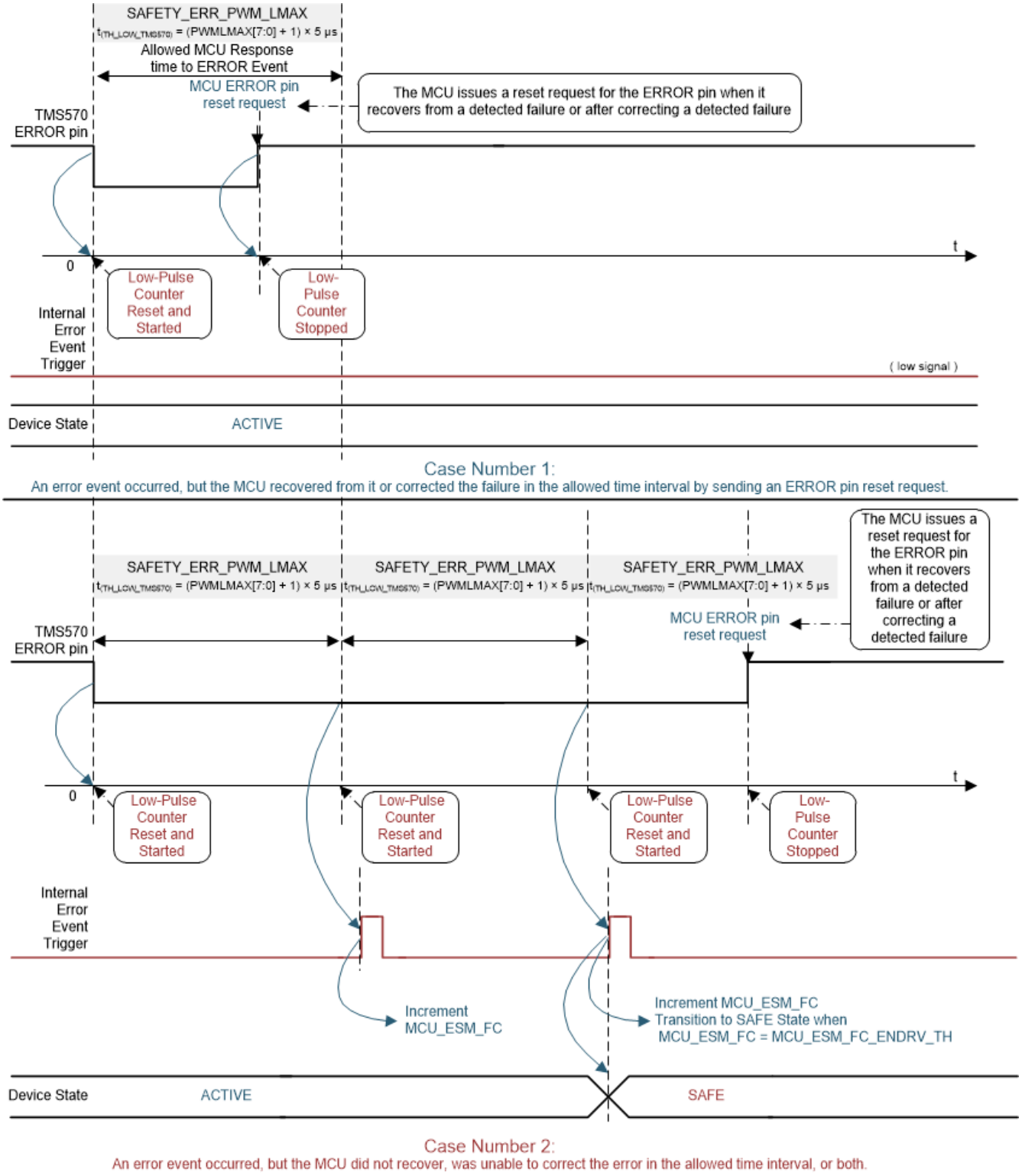


図 11-21. MCU ESM TMS570 Mode

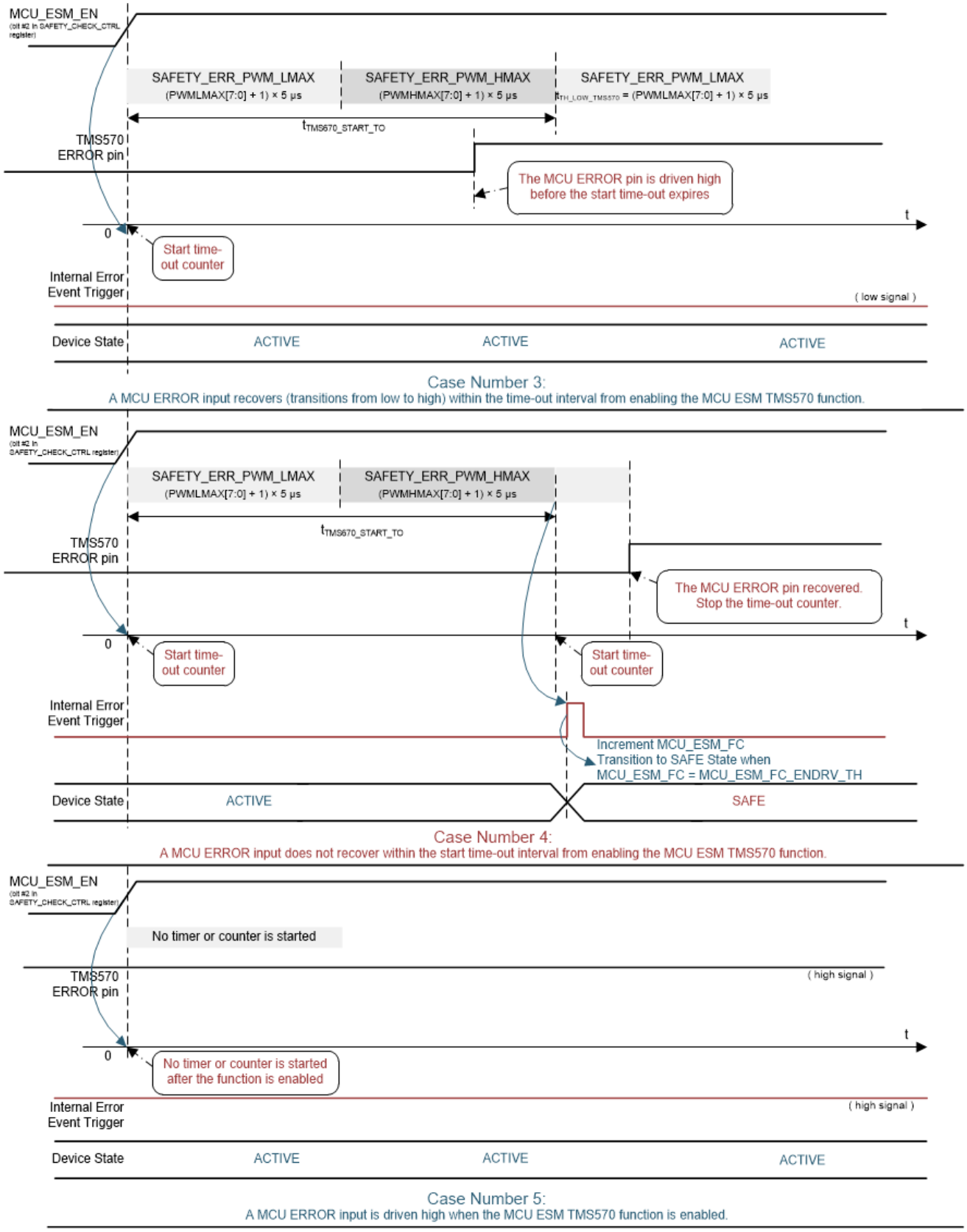


図 11-22. MCU ESM TMS570 Mode (Time-Out)

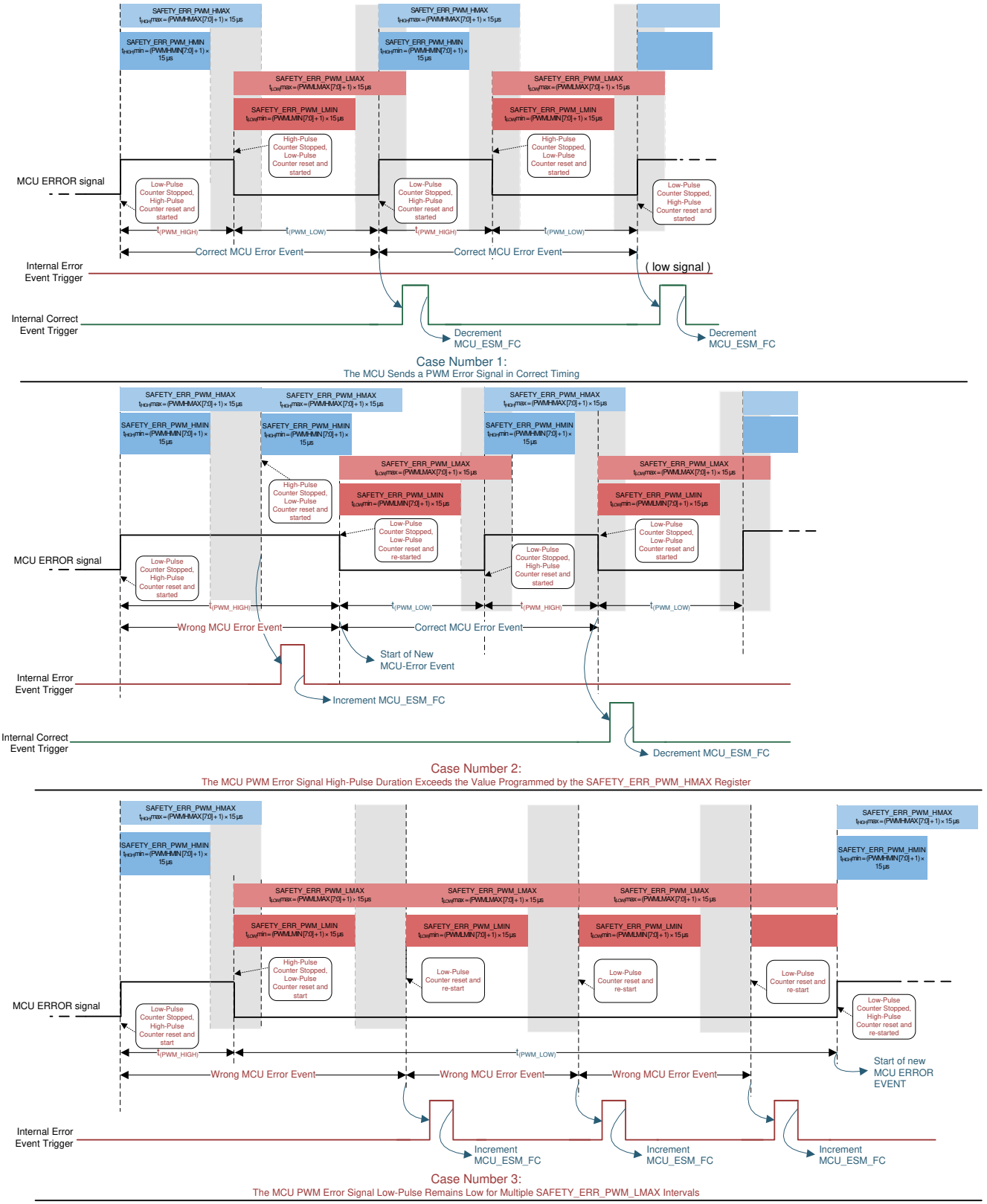


図 11-23. MCU ESM PWM Mode (Case Scenarios 1, 2, and 3)

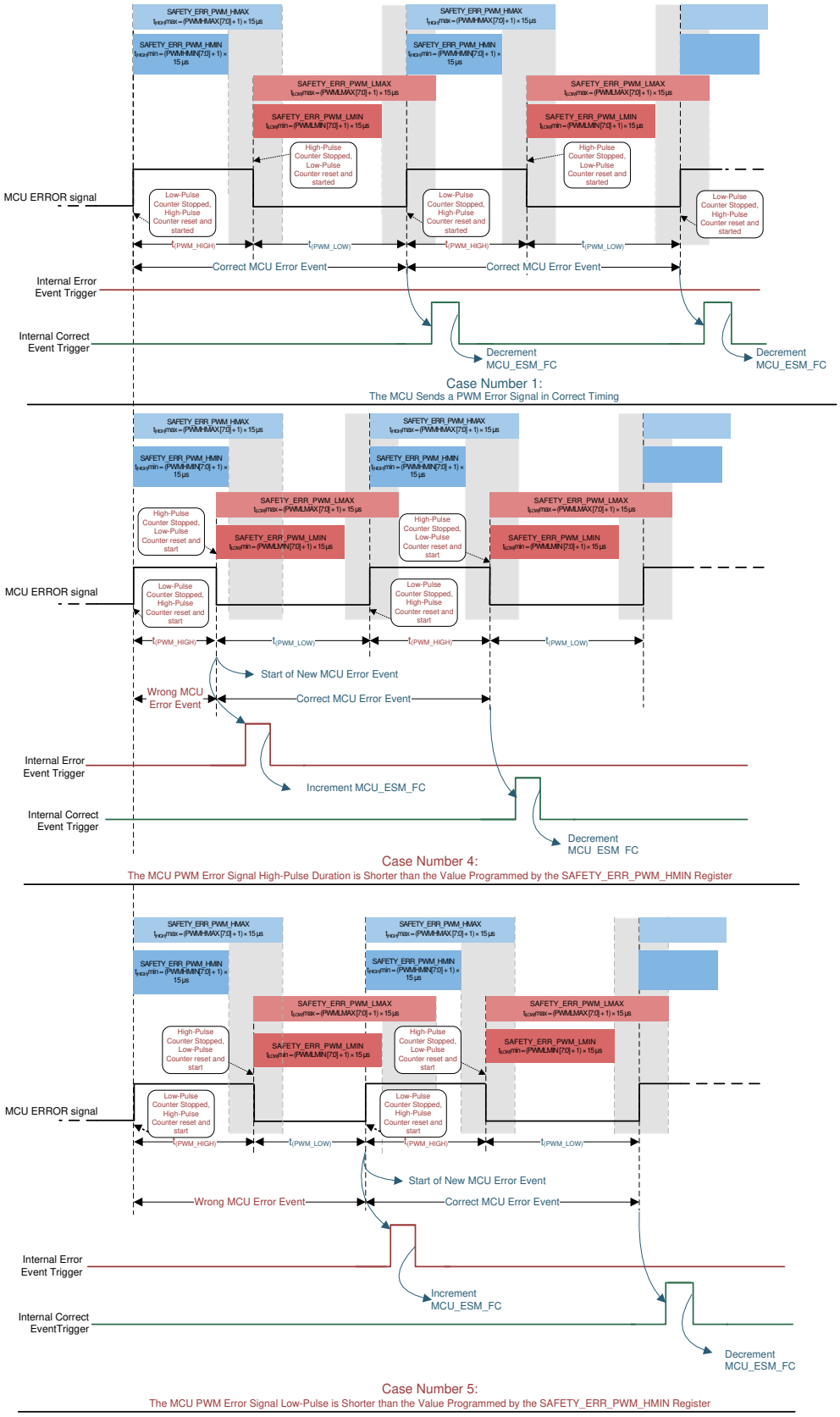


図 11-24. MCU ESM PWM Mode (Case Scenarios 1, 4, and 5)

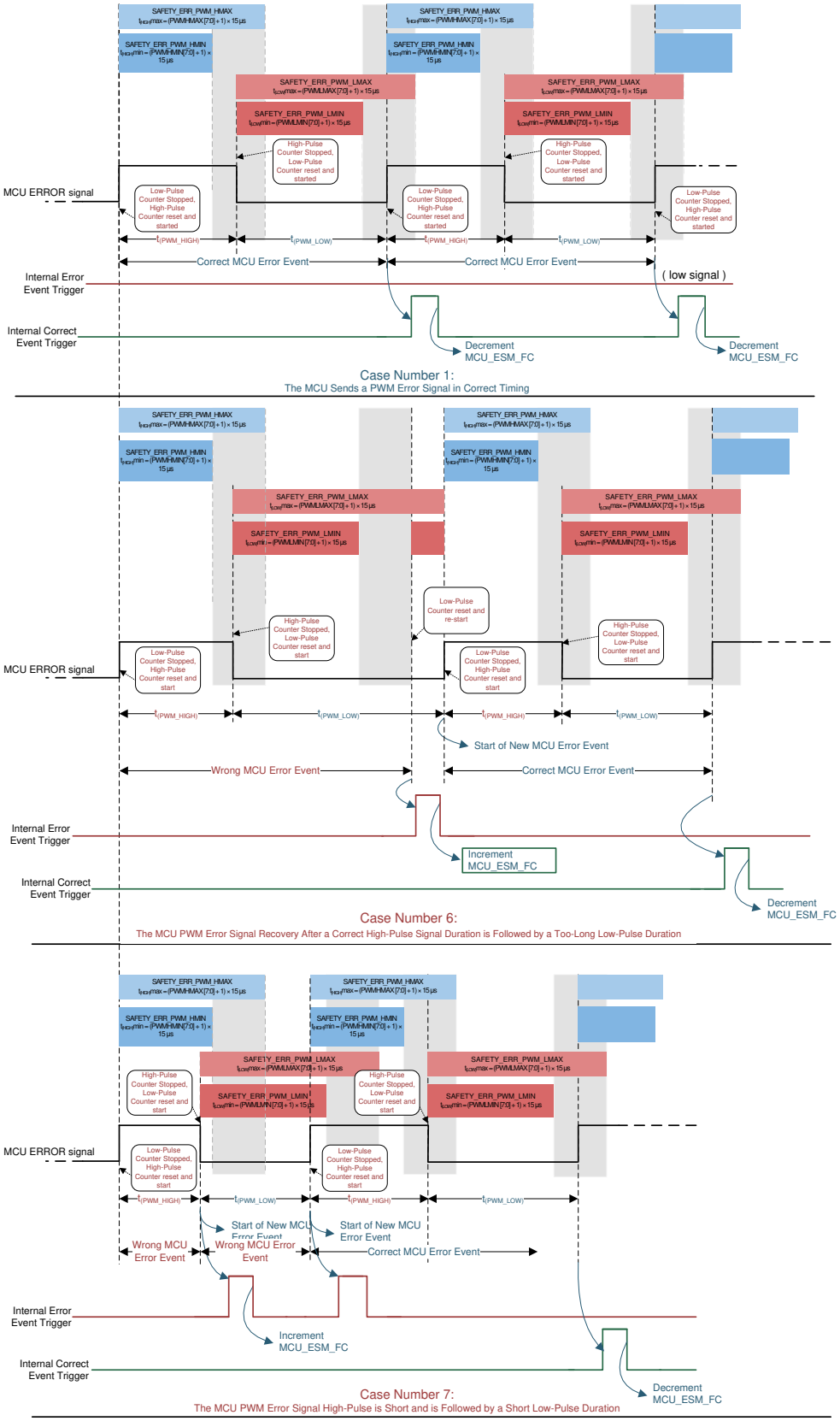


図 11-25. MCU ESM PWM Mode (Case Scenarios 1, 6, and 7)

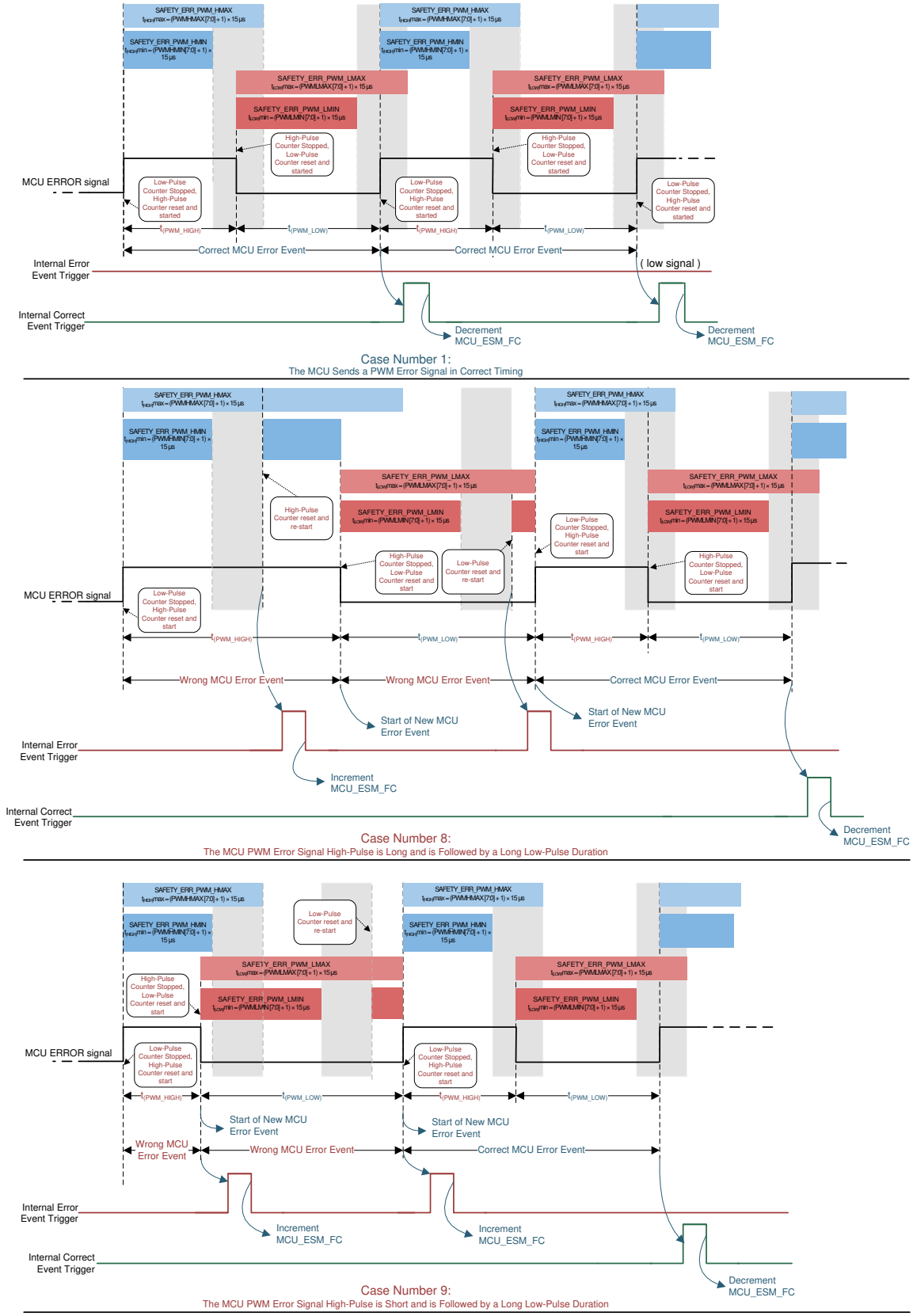


図 11-26. MCU ESM PWM Mode (Case Scenarios 1, 8, and 9)

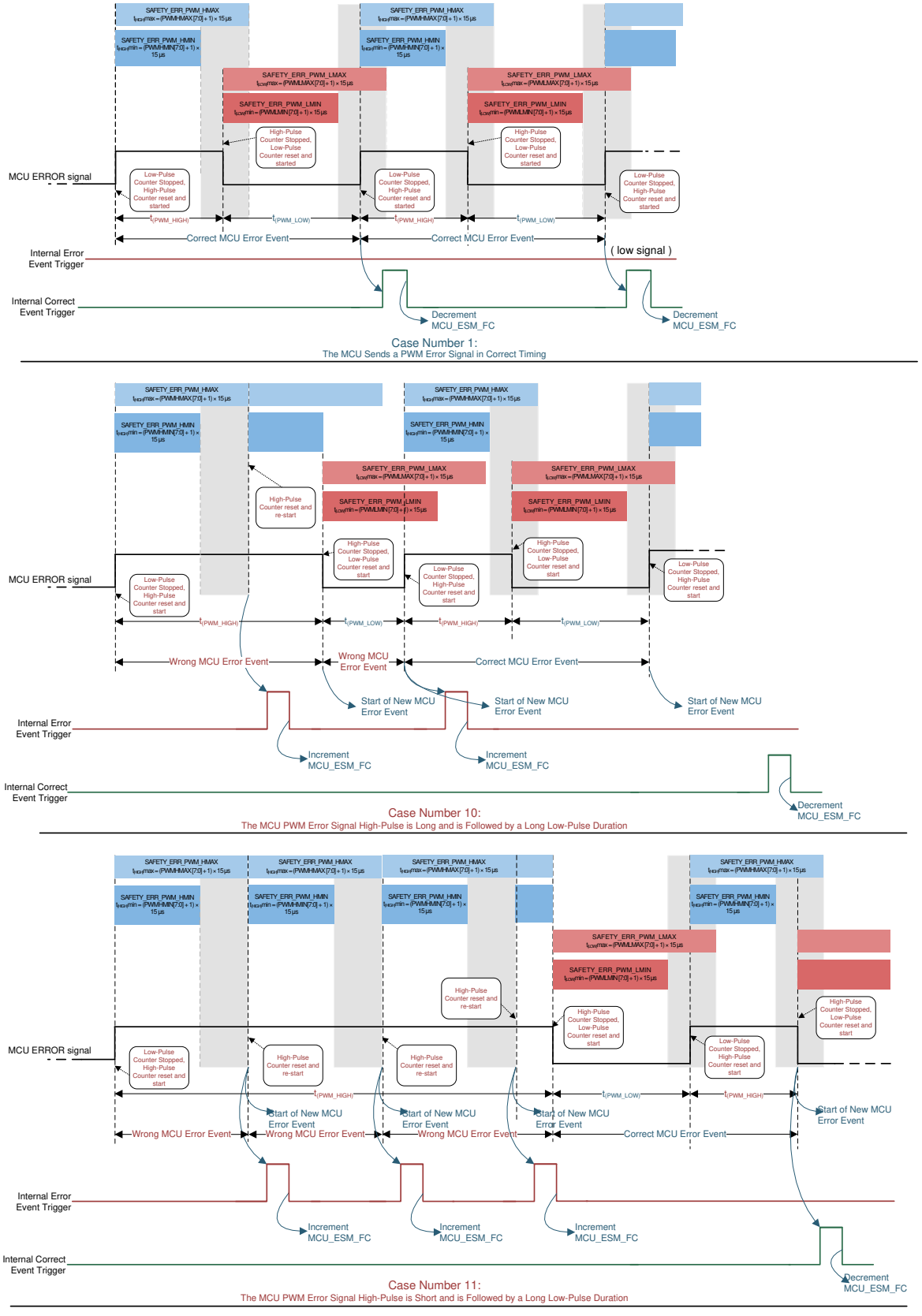


図 11-27. MCU ESM PWM Mode (Case Scenarios 1, 10, and 11)

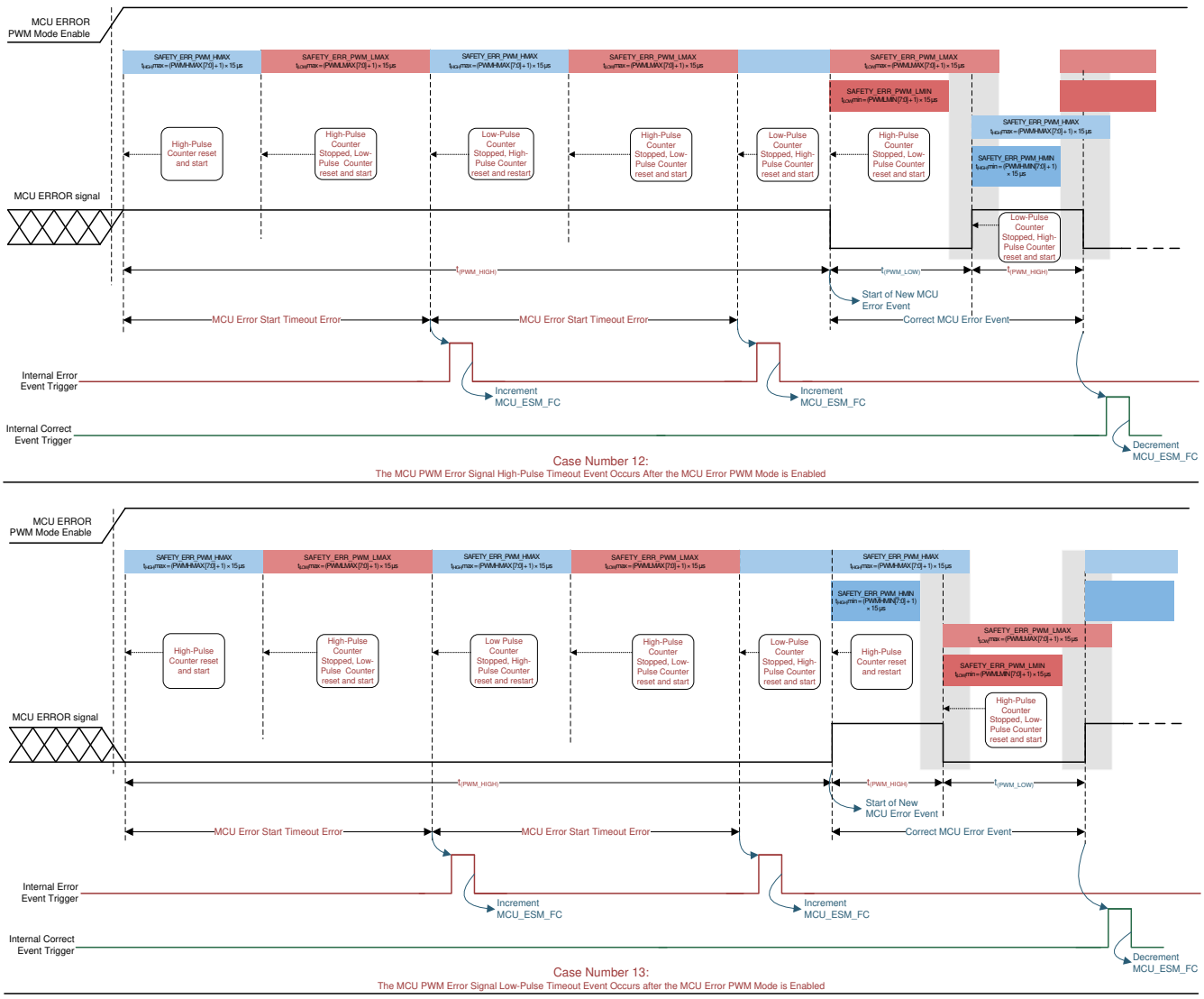


図 11-28. MCU ESM PWM Mode Time-Out Events After PWM Mode is Enabled (Case Scenarios 12 and 13)

11.9.12 NRES Driver

The NRES pin drives the reset of the primary system MCU or DSP. This pin must keep the primary MCU or DSP and peripheral devices in a defined state during power up and power down when the supply voltages are out of range or a critical failure is detected. Therefore, the NRES pin is always held at a low level when the NRES pin is asserted even if the VIN supply decreases to less than the NPOR voltage threshold ($V_{IN\_POR\_F}$) or if the device is in the OFF state. The NRES pin is an open-drain output with an internal pullup resistor. The NRES pin is driven low when any of the NRES conditions are met. These conditions are defined as follows:

NPOR event	The device power-on reset occurs with each device power-up from the OFF state. It is the master reset source that initializes the complete device.
Device is in OFF state	Any time the device enters the OFF state.
Device is in RESET state	Any time the device enters the RESET state.
BUCK1 undervoltage event	This event occurs when the BUCK1 output voltage is less than its UV-threshold level.

BUCK2 undervoltage event	This event occurs when the BUCK2 output voltage is less than its UV-threshold level. The BUCK2 UV event must be enabled as a global RESET state event.
BOOST undervoltage event	This event occurs when the BOOST output voltage is less than its UV-threshold level. The BOOST UV event must be enabled as a global RESET state event.
External VMON1 and VMON2 undervoltage event	This event occurs when the monitored voltage of the external VMON1 or VMON2 is less than its UV-threshold level. The external VMON1 UV event and the external VMON2 UV event must be enabled as a global RESET state event.
BUCK1 overvoltage event	This event occurs when the BUCK1 output voltage is greater than its OV-threshold level. The BUCK1 OV event must be enabled as a global RESET state event.
BUCK2 overvoltage event	This event occurs when the BUCK2 output voltage is greater than its OV-threshold level. The BUCK2 OV event must be enabled as a global RESET state event.
BOOST overvoltage event	This event occurs when the BOOST output voltage is greater than its OV-threshold level. The BOOST OV event must be enabled as a global RESET state event.
External VMON1 and VMON2 overvoltage event	This event occurs when the monitored voltage of the external VMON1 or VMON2 is greater than its OV-threshold level. The external VMON1 OV event and the external VMON2 OV event must be enabled as a global RESET state event.
MCU watchdog reset	This event occurs when the WD failure counter is greater than the RESET state threshold value of the programmed WD-failure counter while WD reset is enabled.
MCU ESM error reset	This event occurs when the MCU ESM failure counter is greater than the RESET state threshold value of the programmed MCU ESM failure counter while MCU ESM reset is enabled.
MCU SW reset request	This event occurs when the MCU sends a SPI SW reset command.
MCU warm reset	This event occurs when the NRES pin driven low by the external MCU (the nRES_IN bit is set to 0b, the nRES_OUT bit is set to 1b, and the NRES_ERR_RST_EN bit is set to 1b).

The TPS65313-Q1 device keeps the NRES pin low for the programmed delay time (the RESET extension time) after all reset conditions are removed. The NRES_EXT[1:0] bits in DEV_CFG4 configuration register set the programmable reset-extension time.

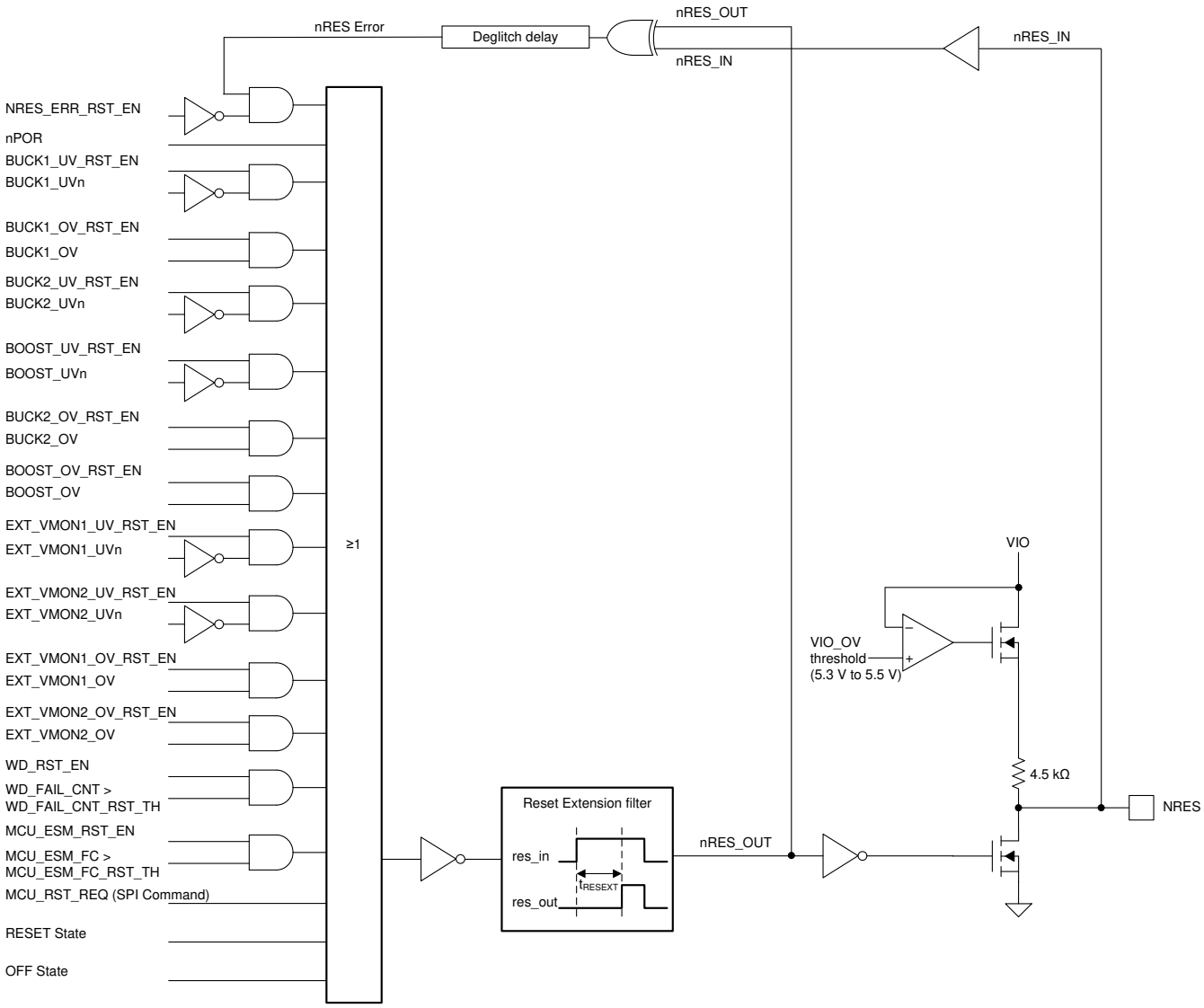


図 11-29. The NRES Driver and Logic

The error detection circuit for NRES driver compares the external logic level on the output of NRES pin input buffer (nRES_IN) against the logic level on the input of the NRES pin output buffer (nRES_OUT). If a mismatch between the output of the NRES pin input buffer (nRES_IN) and the input of the NRES pin output buffer (nRES_OUT) logic levels is detected, the NRES_ERR status bit in the SAFETY_ERR_STAT1 register is set. The result of a detected mismatch is configured by the NRES_ERR_RST_EN bit and NRES_ERR_SAFE_EN bit in the SAFETY_CFG2 register.

In the DIAGNOSTIC state, the system MCU can run the diagnostics on the error detection circuit for the NRES driver if the system MCU can externally control the NRES pin interconnect.

注

The system MCU can only externally control the NRES pin interconnect if the system MCU has a single bi-direction pin used as power-on reset input and warm reset output.

The sequence to perform diagnostics on the error detection circuit for the NRES driver is as follows:

- Force the NRES pin low externally and confirm that the NRES_ERR status bit is set while the device stays in the DIAGNOSTIC state, and when both the NRES_ERR_RST_EN and NRES_ERR_SAFE_EN bits are cleared.
- Force the NRES pin low externally and confirm that the NRES_ERR status bit is set while the device goes into the SAFE state, when the NRES_ERR_RST_EN is cleared, and while the NRES_ERR_SAFE_EN bit is set.

11.9.13 ENDRV/nIRQ Driver

The ENDRV/nIRQ pin can be used in the system as an enable driver (ENDRV), independent safing enable or safety power-stage enable control signal, an external error interrupt (nIRQ) to the system MCU, or both. The device has no dedicated configuration bit to configure the mode (ENDRV mode or nIRQ mode) of the ENDRV/nIRQ pin. System-level requirements select how the ENDRV/nIRQ pin is used.

The default state of the ENDRV/nIRQ output driver is LOW. The state of the ENDRV/nIRQ pin can be activated in the DIAGNOSTIC and ACTIVE states. System-level diagnostics by the system MCU occur in the DIAGNOSTIC state, to confirm that the ENDRV/nIRQ output driver is controllable (as a system-level safety diagnostics requirement). In the ACTIVE state, the system MCU can use ENDRV to control (either activate or deactivate, or enable or disable) system-level peripherals or an nIRQ external interrupt to the system MCU. Activating the ENDRV/nIRQ driver (driving it high) requires system MCU activation (or MCU enable) by a SPI command, after the system's MCU services watchdog function to decrement watchdog failure counter to less than a programmed threshold value for ENDRV activation as defined by the WD_FC_ENDRV_TH[3:0] bits.

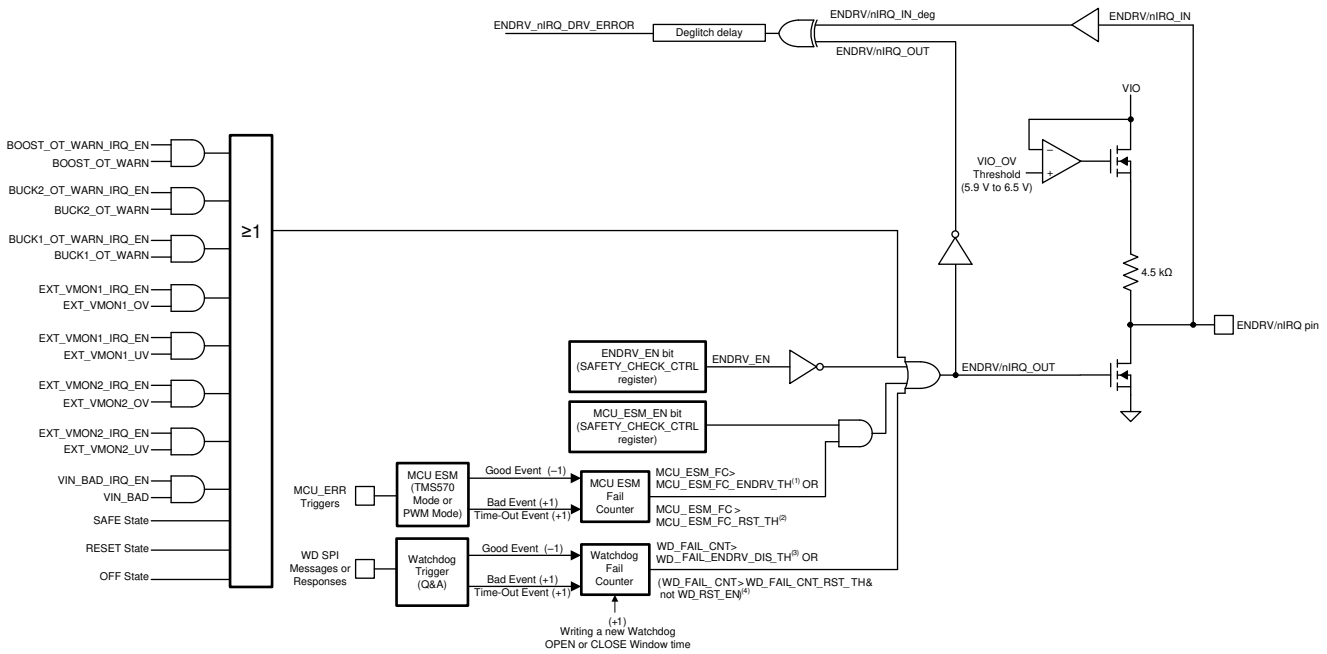
The ENDRV/nIRQ driver has a driver-error monitoring function that is enabled after the driver is activated (driven high). An error is detected each time the ENDRV/nIRQ pin is pulled low externally while the ENDRV/nIRQ pin output buffer is trying to drive it high.

During an active ABIST run when the device is in the DIAGNOSTIC or ACTIVE state, and if the ENDRV/nIRQ output driver is activated (driven high), the active ABIST comparator test toggles the activated ENDRV/nIRQ driver low for the duration of the ABIST run pulse test if any of the BUCKx/BOOST_OT_WARN_IRQ_EN bits are set. Driving the ENDRV/nIRQ driver low during the active ABIST test when the device is in the DIAGNOSTIC or ACTIVE state does not clear the ENDRV_EN control bit and the device does not change states.

When the activated ENDRV/nIRQ driver toggles from HIGH to LOW, the potential impact to the system could be one or a combination of the following:

- Disabled power stages
- Disabled safing switch (this switch is a redundant high-side switch for connecting the VBAT supply to the system-power stages.)
- Generated interrupt to the system MCU (when connected to the system MCU, the GPIO pin that is configured as an external interrupt source, edge, or level triggered.)

図 11-30 shows the driver and enable logic of the ENDRV/nIRQ pin.



1. When the condition is met, the device goes from the ACTIVE state to the SAFE state. No action occurs if the device is in the DIAGNOSTIC or SAFE state.
2. When the condition is met, the device stays in the ACTIVE state, if the MCU_ESM_RST_EN bit is set to 0b. When the condition is met, the device goes from the ACTIVE state to the RESET state, if the MCU_ESM_RST_EN bit is set to 1b. This transition occurs only if the MCU_ESM_FC_RST_TH[3:0] bit value is equal to or less than the MCU_ESM_FC_ENDRV_TH[3:0] bit value.
3. When the condition is met, the device does not go from the ACTIVE state to the SAFE state. No action occurs if the device is in the DIAGNOSTIC or SAFE state.
4. When the condition is met, the device goes from the ACTIVE state to the SAFE state.

図 11-30. ENDRV/nIRQ Driver and Logic

11.9.14 CRC Protection for the Device Configuration Registers

The CRC-8 engine continuously checks the device configuration registers when the DEV_CFG_CRC_EN bit is set. The expected CRC-8 value is stored in the SAFETY_DEV_CFG_CRC register. Anytime a mismatch between the calculated and expected CRC-8 value is detected, the DEV_CFG_CRC_ERR bit in the SAFETY_ERR_STAT1 register is set and the device goes from the operating state (RESET, DIAGNOSTIC, or ACTIVE) to the SAFE state.

The CRC-8 protection of the device configuration registers is configured and enabled only when the device is in the DIAGNOSTIC state. The device configuration change is not allowed when the device is in the ACTIVE state.

The CRC-8 engine is based on polynomial: $X^8 + X^2 + X + 1$

- Initial value for remainder is all 1 s.
- Big-endian bit stream order.
- Inversion of calculated result is not enabled.

The protected registers are as follows:

- DEV_CFG1 register
- DEV_CFG2 register
- DEV_CFG3 register
- DEV_CFG4 register
- SAFETY_CFG1 register
- SAFETY_CFG2 register
- SAFETY_CFG3 register

- SAFETY_CFG4 register
- SAFETY_CFG5 register
- SAFETY_CFG6 register
- SAFETY_CFG8 register
- EXT_VMON1_CFG register
- EXT_VMON2_CFG register
- WDT_WIN1_CFG register
- WDT_WIN2_CFG register
- WDT_Q&A_CFG register

11.9.15 CRC Protection for the Device EEPROM Registers

The CRC-8 engine continuously checks the device EEPROM registers. The expected CRC-8 value is stored in the EEPROM. Anytime a mismatch between the calculated and expected CRC-8 values are detected, the EE_CRC_ERR status bit in the SAFETY_ERR_STAT1 register is set and the device goes from the operating state (RESET, DIAGNOSTIC, ACTIVE, or SAFE) to the OFF state. The EE_CRC_ERR status flag is latched in the Analog_Latch and is loaded to the SAFETY_ERR_STAT1 register during the next device power-up event.

Diagnostic test can be run on EEPROM by setting CRC EE_CRC_DIAG_EN bit. During the diagnostic testing EE_CRC_ERR bit in SAFETY_ERR_STAT1 is set and can be cleared by MCU after successful completion of this diagnostic check.

The CRC-8 engine uses a standard CRC-8 polynomial to calculate the internal known-good checksum-value which is $X^8 + X^2 + X + 1$.

The initial value for the remainder of the polynomial is all 1 s and is in big-endian bit-stream order. The inversion of the calculated result is not enabled.

11.10 General-Purpose External Supply Voltage Monitors

The device has two general-purpose supply voltage monitors at the EXT_VSENSE1 and EXT_VSENSE2 pins. The nominal voltage level at the pins must be set to 0.8 V by the external resistor divider as shown in 図 11-31. Each monitor detects undervoltage and overvoltage events. These events set the corresponding status bit in the EXT_VMON_STAT register. The TPS65313-Q1 device can be factory-programmed such that each monitor is either enabled or disabled during a device start up (NPOR) event. If either of the voltage monitors is programmed to be enabled during an NPOR event, the voltage monitor does not detect an undervoltage event before the RESET extension starts. After the device goes to the DIAGNOSTIC state, the system MCU can set the EXT_VMONx_EN control bits in the PWR_CTRL register to either enable or disable the voltage monitors. When these bits are set by the MCU, the bits stay unchanged when the device goes into the RESET state for any reason.

A corresponding UV flag in the EXT_VMON_STAT register is set after a power-up (NPOR) event, if the external supply voltage at the EXT_VSENSEx pin was below its undervoltage threshold, and when the voltage monitor was enabled. The device goes into the OFF state, if the external supply does not reach the target regulation voltage within the $t_{RESET\_STATE\_TO}$ time, and after the voltage monitor was enabled.

The device response to fault detection from the monitors is configured by writing the desired data to the EXT_VMON1_CFG and EXT_VMON2_CFG registers.

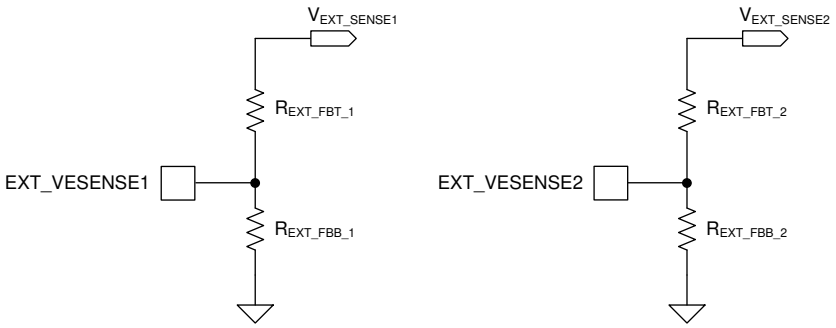


図 11-31. External VSENSEx

11.11 Analog Wake-up and Failure Latch

The analog wake-up detection circuit monitors the WAKE pin when the device is in the OFF state. With a valid power supply at the supply input pins (VIN, AVIN, and VIN_SAFE), this circuit is the only active circuit in the device when the device is in the OFF state, reducing device power consumption.

When the WAKE pin is driven high, the device deglitches the input wake-up signal using a low-power oscillator clock for approximately 130 µs and latches the signal in the analog wake-up latch (indicated as a WAKE_L bit). When the WAKE_L bit is set, the wake-up latch is cleared only by the device NPOR event, a SPI command (CLR_WAKE_LATCH), or failure conditions that force the device to go to the OFF state (fault events 2 through 17). The wake-up latch is also cleared anytime when the device goes into the OFF state.

The wake-up latch is cleared as the device starts to go to the OFF state. The internal signal that clears the wake-up latch remains active (keep clearing the power wake-up latch) until the device goes to the OFF state. This prevents the wake-up latch from getting set again and triggers a new power-up before the device goes into the OFF state.

In addition to the power wake-up latch, the analog wake-up latch includes additional analog latches (Analog_Latch) to retain failure conditions that force the device to go to the OFF state. The list of latches includes the following:

1. NPOR latch
2. Analog or digital system-clock-monitor failure latch
3. RESET state time-out latch
4. EEPROM CRC failure latch
5. BUCK1 overtemperature latch
6. BUCK1 short-circuit-to-ground latch
7. BUCK1 overvoltage protection latch
8. BUCK1 low-side sink overcurrent latch
9. BUCK1 extreme overvoltage protection latch
10. BUCK1 power ground loss latch
11. BUCK2 overvoltage protection latch

注

In case the BUCK2 overvoltage condition is still detected 28 µs to 30 µs after the BUCK2 regulator is disabled, the device goes to the OFF state and the BUCK2_OVP status bit is latched in the Analog_Latch.

12. BOOST overvoltage protection latch

注

In case the BOOST overvoltage condition is still detected 72 µs to 80 µs after the BOOST converter is disabled, the device goes to the OFF state and the BOOST OVP status bit is latched in the Analog_Latch.

13. VREG undervoltage latch
14. VREG overvoltage latch
15. VIN overvoltage latch
16. Device error-counter power-down latch
17. Start-up time-out latch

These status latches are set in the analog power domain of the TPS65313-Q1 device as the device goes into the OFF state. These latches are cleared only if the device loses battery supply at the AVIN pin or when the device wakes up and exits the OFF state after a valid WAKE input event. As the device starts up after a valid WAKE input event, the content of the analog status latches are copied to the OFF_STATE_L_STAT and the corresponding BUCK1, VMON, and SAFETY status registers after an internal NPOR is asserted high and the EEPROM has been downloaded. Then the analog status latches are cleared.

表 11-14. OFF-State Conditions and Corresponding Status Bits

NUMBER	OFF STATE CONDITION	OFF_STATE_L REGISTER BIT	CORRESPONDING STATUS REGISTER BIT
1.	Power-on reset	POWER_ON_RST	
2.	Analog or digital system clock-monitor error	SYSCLK_ERR	ANA_SYSCLK_ERR bit and DIG_SYSCLK_ERR bit in SAFETY_CLK_STAT register
3.	RESET state time-out	RESET_TO	
4.	EEPROM CRC error	EE_CRC_ERR	EE_CRC_ERR bit in SAFETY_ERR_STAT1 register
5.	BUCK1 overtemperature	BUCKx_BOOST_VREG_FAIL	BUCK1_OT_STD bit in SAFETY_BUCK1_STAT1 register
6.	BUCK1 short-circuit to GND	BUCKx_BOOST_VREG_FAIL	BUCK1_SCG bit in SAFETY_BUCK1_STAT1 register
7.	BUCK1 overvoltage protection	BUCKx_BOOST_VREG_FAIL	BUCK1_OVP bit in SAFETY_BUCK1_STAT1 register
8.	BUCK1 low-side sink overcurrent	BUCKx_BOOST_VREG_FAIL	BUCK1_LS_SINK_OVC bit in SAFETY_BUCK1_STAT1 register
9.	BUCK1 extreme overvoltage protection	BUCKx_BOOST_VREG_FAIL	BUCK1_EOVP bit in SAFETY_BUCK1_STAT1 register
10.	BUCK1 power GND loss	BUCKx_BOOST_VREG_FAIL	BUCK1_PGND_LOSS bit in SAFETY_BUCK1_STAT1 register
11.	BUCK2 overvoltage protection	BUCKx_BOOST_VREG_FAIL	BUCK2_OVP bit in SAFETY_BUCK2_STAT1 register
12.	BOOST overvoltage protection	BUCKx_BOOST_VREG_FAIL	BOOST_OVP bit in SAFETY_BOOST_STAT1 register
13.	VREG undervoltage	BUCKx_BOOST_VREG_FAIL	VREG_UV bit in VMON_UV_STAT register
14.	VREG overvoltage	BUCKx_BOOST_VREG_FAIL	VREG_OV bit in VMON_OV_STAT register
15.	VIN overvoltage	VIN_OV	VIN_OV bit in VMON_OV_STAT register
16.	Device error-counter power down	DEV_EC_PDWN	
17.	Start-up time-out	START_UP_TO	

If a power-up time-out failure that puts the device in the OFF state is followed by a new power-up event (because the WAKE pin is driven above its $V_{WAKE-ON}$ threshold level), the number of analog-latched bits could be more than the START_UP_TO bit. The reason for this increased number of latched bits is because the previous OFF state transition condition could be caused by any of the previously listed OFF-state failure conditions.

The AUTO_START_DIS configuration bit is latched in the analog wake-up latch as well as in the DEV_STAT1 register. This bit is initialized to 0b at a NPOR event, only when an NPOR event is preceded by loss of battery supply at the VIN, VINA, and VIN_SAFE pins. The AUTO_START_DIS bit can be set to 1b by the SET_AUTO_START_DIS command with data 0xAA, or when a valid VREG OV event is detected. This bit can be cleared by the CLR_AUTO_START_DIS command with data 0x55. This bit controls whether the device's auto-restart is allowed, when the device goes to the OFF state, and while the WAKE input pin is still driven above its $V_{WAKE-ON}$ threshold level.

When the device is in the INIT state during power-up, the device NPOR stays asserted if the system-clock error, VIN overvoltage, or both are detected. The NPOR is asserted until the INIT state time-out event puts the device to the OFF state, and the START_UP_TO bit is latched in the Analog_Latch (the SYSCLK_ERR and VIN_OV bits are not latched in the Analog_Latch).

When the device starts and the NPOR for the digital core is released, the device goes into the OFF state with respective status bits latched in the Analog_Latch, if the SYSCLK failure, VIN supply overvoltage, or both are detected.

11.12 Power-Up and Power-Down Sequences

図 11-32 shows a power-up sequence and 図 11-33 shows a power-down sequence.

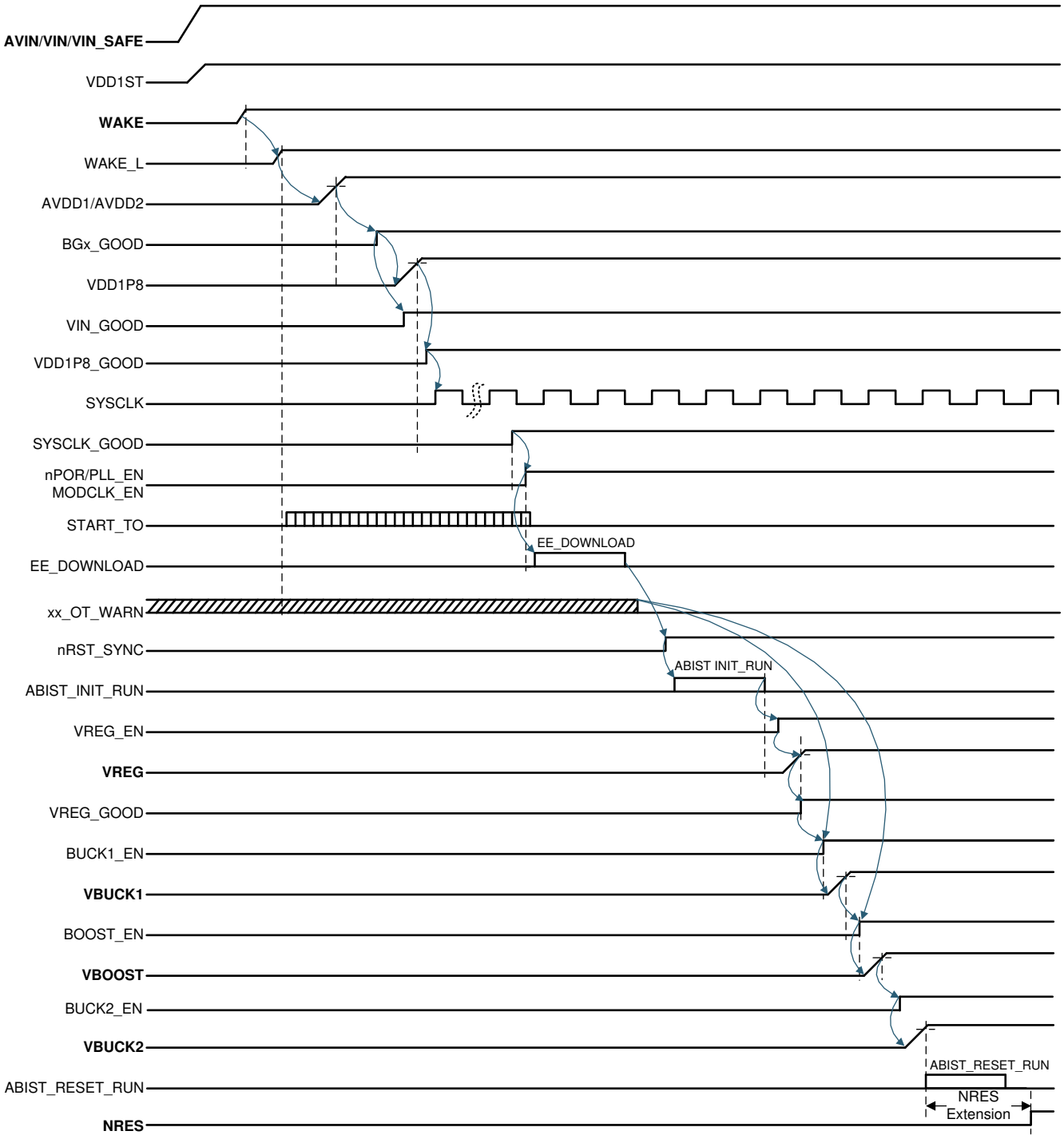


図 11-32. Power-Up Sequence Example

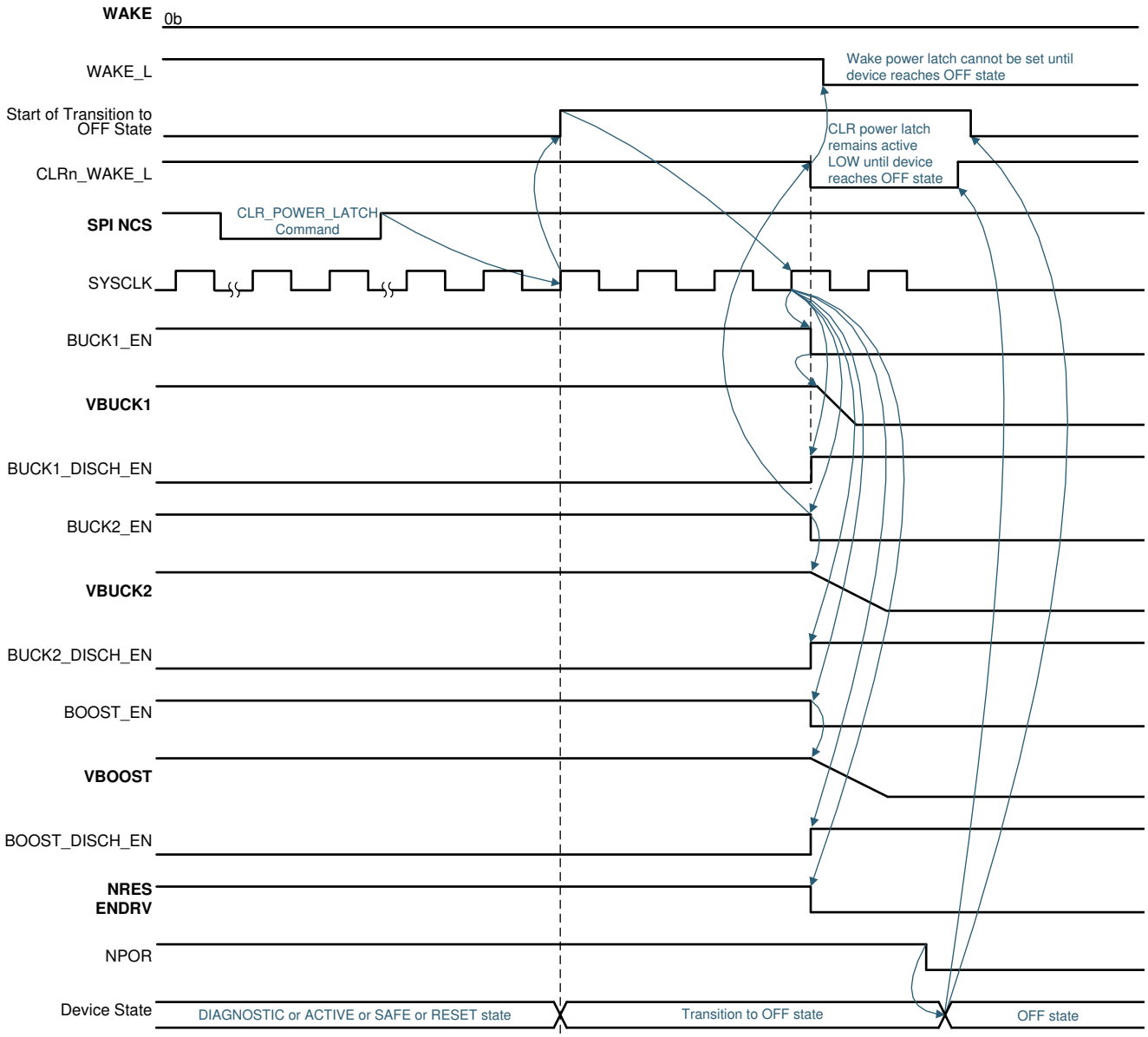
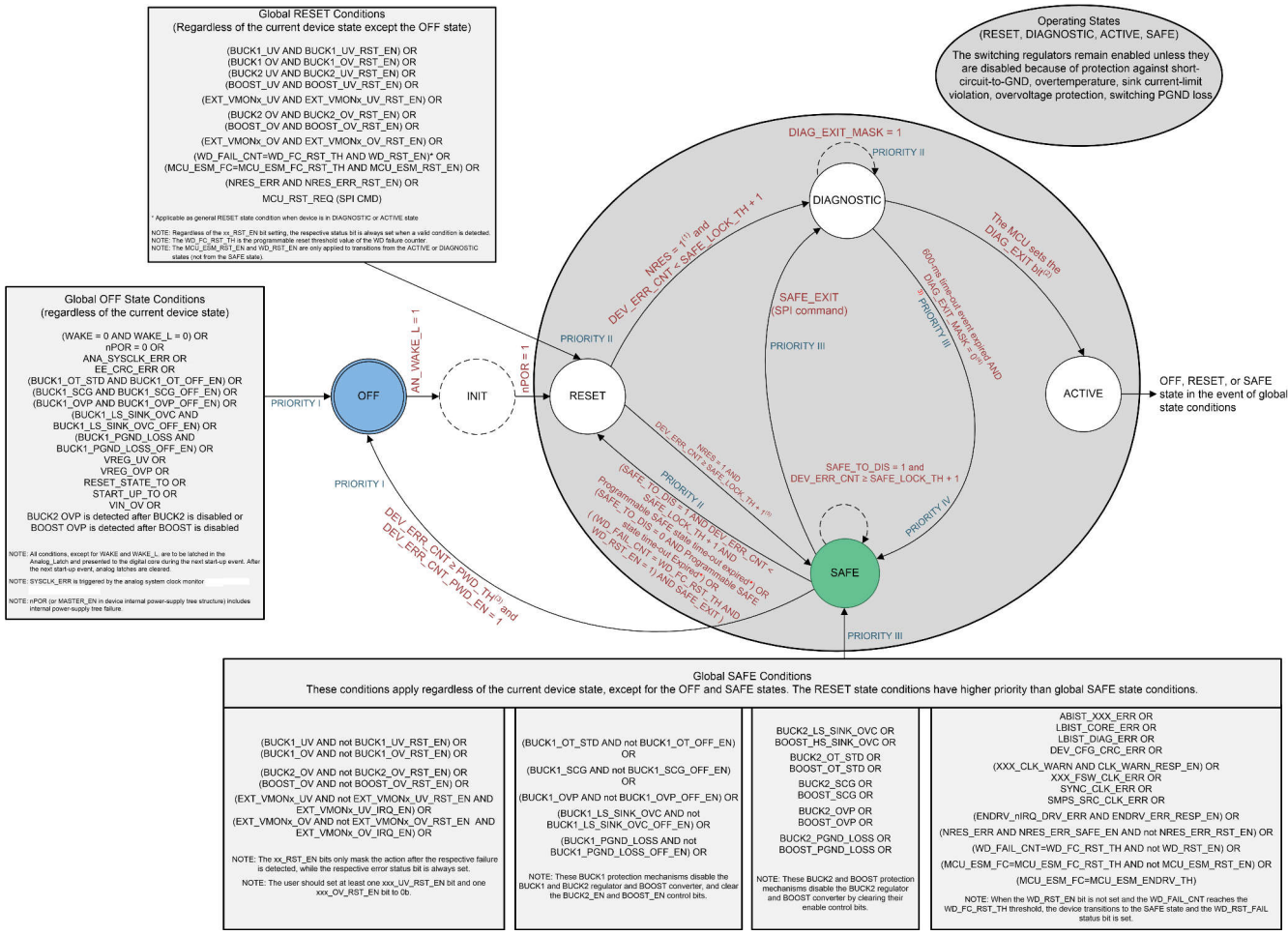


図 11-33. An Example of Power-Down Sequence Initiated by SPI CLR_POWER_LATCH Command

11.13 Device Fail-Safe State Controller (Monitoring and Protection)

図 11-34 shows the device state diagram of TPS65313-Q1 device. The state diagram contains four operating states (RESET, DIAGNOSTIC, ACTIVE, and SAFE) and two nonoperating states (OFF and INIT).



1. All RESET state conditions are removed and the reset extension is completed while monitoring the NRES input stage.
2. The DIAG_EXIT bit is bit 0 in the SAFETY_CHECK_CTRL register.
3. The PWD_TH is set by the SAFETY_PWD_TH_CFG register.
4. The DIAG_EXIT_MASK bit is bit 1 in the SAFETY_CHECK_CTRL register.
5. For transition from the RESET to SAFE state, the DEV_ERR_CNT counter is not incremented.
6. Some differences between general RESET state conditions and global SAFE state conditions are as follows:
   - The general RESET state conditions have higher priority compared to global SAFE state conditions.
   - If any global SAFE state condition occurs while the device is in the RESET state, then the device stays in the RESET state until no active RESET state condition exists, and then the device goes into the SAFE state.

図 11-34. Device Fail-Safe Controller State Diagram

11.13.1 OFF State

The device is powered-down in the OFF state, and a battery power supply may or may not be available for the device. If a valid power source is available, and if the WAKE pin is driven low, the only active circuit in the device is the WAKE input detection circuit to reduce device power consumption.

The device goes into the OFF state because of either a CLR_WAKE_LATCH command from the MCU or any global OFF-state condition as listed in Device Fail-Safe Controller State Diagram . All global OFF state conditions are latched in the analog wake-up detection circuit and serves two purposes. The first purpose is to preserve the root-cause information for an OFF state shutdown (or system shutdown). The information is latched in the Analog_Latch, and is passed on to the digital core during the next device power-up event. The system

MCU can verify the information by reading bits in the OFF_STATE_L register and the corresponding status bits defined in 表 11-14. The second purpose is to prevent auto-restart when the device auto-start is disabled and the device enters the OFF state while the WAKE pin is still driven above its $V_{WAKE-ON}$ threshold level. If the device was powered down because of a failure either in the device or in the system and the device auto-start is disabled, then the device can be enabled, only when a new rising edge is detected at the WAKE pin which is an indication of the user trying to restart the system. After each new power-up event, information in the Analog_Latch is copied to the respective SPI-mapped status registers in the digital core.

The device auto-start behavior can be configured through the AUTO_START_DIS latch. This latch is physically located in the analog wake-up detection circuit. The AUTO_START_DIS latch is cleared to 0b during the device NPOR event only if a NPOR event was preceded by loss of battery supply at the VIN, VINA, and VIN_SAFE pins. This bit is set to 1b by the system MCU through the SET_AUTO_START_DIS SPI command or when a valid VREG OV event is detected. If the AUTO_START_DIS latch is set to 1b and if the device goes into the OFF state because of one of the global OFF state conditions is detected and while the WAKE pin is still driven above its $V_{WAKE-ON}$ threshold level, then the device does not restart until the WAKE pin is driven below its $V_{WAKE-ON}$ threshold level and then driven above its $V_{WAKE-ON}$ threshold level.

The analog wake-up circuit implements a filter to prevent false device power-up because of noise at the WAKE input. When a valid WAKE input is detected, the filtered signal is latched in the analog power latch (AN_WAKEUP_L) followed by a check of the supply voltage at the VIN pin while the device overtemperature check is performed after EEPROM download in the RESET state. The device can continue with the power-up sequence and goes into the INIT state only if the supply voltage is greater than the minimum required voltage level for the power-up and when there is no junction overtemperature condition (junction temperature is less than the warning threshold level). Otherwise, the device goes back to the OFF state and clears the AN_WAKEUP_L latch and latch failure conditions (VIN UV, over-temperature, or both) in the Analog_Latch.

When the device is in the OFF state, the NRES and ENDRV/nIRQ outputs are driven low even if the supply at the supply pins are less than the minimum required level for the device power-up.

11.13.2 INIT State

The internal regulators are enabled in the INIT state to provide the power supply for important blocks, such as the digital core and SYSCLK clock, that are required to enable the switching voltage regulators.

The device NPOR event is preceded by several internal events. The INIT state start-up time-out timer ($t_{START\_UP\_TO}$) is implemented as a safety mechanism against power-up lock-up failures from which the device cannot recover even if the power supply voltage increases to greater than the minimum required level for the power-up voltage. Under such conditions, without the INIT time-out timer, the device cannot exit the OFF state until the power cycling is performed, which for some systems, may require disconnecting and then reconnecting the device supply. The minimum required value for the INIT state time-out is $t_{START\_UP\_TO}$ to allow the supply voltage to recover during the power-up supply voltage transient (like the automotive cold-crank battery supply transient) above the minimum device power-up voltage level.

If a SYSCLK error, VIN overvoltage condition, or both are detected, the device NPOR stays asserted low until the INIT state time-out event puts the device in the OFF state and the START_UP_TO bit is latched in the Analog_Latch (the SYSCLK_ERR or VIN_OV bits are not latched in the Analog_Latch). Otherwise, the device goes into the RESET state when a NPOR is deasserted.

11.13.3 RESET State (ON Transition From the INIT State)

The device starts with downloading the EEPROM trim and configuration content to the EEPROM-mapped registers. The EEPROM mapped register content is protected by a CRC. The CRC is a safety mechanism to protect the device from failure during an EEPROM content download, corruption of EEPROM-mapped register content, or both. If an EEPROM register-content CRC error is detected, the device goes into the OFF state and latches the EE_CRC error in the Analog_Latch.

After the trim settings are downloaded from the EEPROM without error, the device checks for any overtemperature conditions by confirming that the die junction temperature is less than its warning threshold

level (T_{WARN_TH} – $T_{WARN\_TH\_HYS}$). If the die junction temperature is greater than this level, the device stays in the RESET state. If the die junction temperature does not drop below its warning threshold level, before the timer for the RESET state time-out expires, then the device goes back to the OFF state and flag for the RESET state time-out is latched in the Analog_Latch.

The device also starts the power-up ABIST to check the monitoring and protection mechanisms for the VREG regulator and current-limit comparators of the switched-mode regulators. The ABIST diagnostic test runs before enabling switched-mode regulators to make sure system reset is not released before the regulated supplies exceed their UV-threshold levels. This is because a failure of the voltage monitoring circuit or the protection circuit cannot protect the regulators in case of device power-up with an external short present or internal regulator failure. If the ABIST diagnostic test passes, the switching voltage regulators can be enabled.

When all regulators exceed their undervoltage threshold levels, an NRES system extension starts. The NRES extension time is configurable through the NRES_EXT[1:0] bits in the DEV_CFG4 configuration register. The extension time is configurable from 2 ms to 32 ms with a 10-ms increment.

During an NRES extension time, the device runs the ABIST and then runs the logic BIST (LBIST). The ABIST in the RESET state is performed on all voltage, temperature, and clock monitors except the on the monitoring and protection circuits that are checked by the power-up ABIST. The power-up ABIST is performed when the device goes from the INIT state to the RESET state before the switched-mode regulators are enabled. Therefore, the minimum NRES extension time is longer than the total run time of both the ABIST and LBIST, which is less than 2 ms. If any BIST fails, the device goes into the SAFE state after the NRES extension time elapses. The system MCU selects how to continue in the SAFE state.

All monitoring and protection functions stay enabled in the RESET state except the watchdog function.

11.13.4 RESET State (ON Transition From DIAGNOSTIC, ACTIVE, and SAFE State)

While the device is in any of the powered states (DIAGNOSTICS, ACTIVE, or SAFE), and if any global RESET state condition occurs, then the device goes into the RESET state. The NRES and ENDRV/nIRQ outputs are then driven low while all switched-mode regulators stay enabled. When the RESET state condition no longer exists, the device starts the NRES extension.

During an NRES extension, the device runs the ABIST and then the LBIST, unless the AUTO_BIST_DIS bit in the DEV_STAT1 configuration register is set. If any BIST fails, the device goes into the SAFE state after the NRES extension time elapses. The system MCU selects how to continue in the SAFE state.

The over temperature monitoring stays enabled even after the respective regulator is turned off and it is only disabled when the device is in the OFF state. If the BUCK1 regulator is disabled when the device goes into the RESET state, the regulator is enabled again (while device is in the RESET state) only if the BUCK1 junction temperature drops below its warning threshold level ($T_{WARN\_TH\_F}$). If the BUCK1 junction temperature does not drop to less than its warning threshold level ($T_{WARN\_TH\_F}$) and the RESET state time-out occurs, the device goes into the OFF state and the RESET state time-out flag is latched in the Analog_Latch.

When the device goes into the RESET state from one of three operating states, all control registers and some of the configuration registers set by the MCU in the DIAGNOSTIC state are initialized to their default values. For more information, see セクション 11.16.1.1.

11.13.5 DIAGNOSTIC State

The device enters the DIAGNOSTIC state when one of two conditions occur. The first condition is from the RESET state after the NRES extension, if the device error counter (DEV_ERR_CNT) is equal to or less than the threshold value for the SAFE state lock (SAFE_LOCK_TH). The second condition is from the SAFE state after the system MCU sends the SAFE_EXIT SPI command.

All monitoring and protection functions stay enabled in the DIAGNOSTIC state. The following events occur as the device goes into the DIAGNOSTIC state:

- The NRES output is driven high when the device goes from the RESET state.
- The NRES pin stays high when the device goes from the SAFE state.

- The watchdog function is initialized when the device goes from the RESET state (all status and configuration bits are initialized).
- The watchdog function is not fully initialized when the device goes from the SAFE state.
- The MCU ESM function is initialized when the device goes from the RESET state (function is disabled and all status and configuration bits are initialized).
- The MCU ESM function is not fully initialized when the device goes from the SAFE state.
- The ENDRV/nIRQ driver function is disabled when the device goes from the RESET state.
- The ENDRV/nIRQ driver function is not fully initialized when the device goes from the SAFE state.
  - The ENDRV_EN control bit does not change the setting (if enabled, the ENDRV error monitoring is uninterrupted).
  - The ENDRV/nIRQ error monitor status bits are initialized.
- The NRES driver-error monitoring function is initialized when the device goes from the RESET state.
- The NRES driver-error monitoring function is not fully initialized when the device goes from the SAFE state.
  - The NRES_ERR_RST_EN and NRES_ERR_SAFE_EN bits do not change the setting.
  - The NRES error monitor status bits are initialized.

The primary purpose of the DIAGNOSTIC state is for the system MCU to perform the device and system-level diagnostics prior to enabling or configuring the primary system protection functions listed in セクション 11.9. If any diagnostic test fails, the system MCU can command the device to go to the OFF state by clearing the wake-up latch (by sending the CLR_WAKE_LATCH SPI command).

The system MCU changes the device configuration registers only when the device is in the DIAGNOSTIC state and when the write-lock protection is removed by executing the CLR_CFG_LOCK command. The device configuration registers are also protected by CRC. When the desired configuration is set, the system MCU must write the expected configuration CRC value (DEV_CFG_CRC in SAFETY_DEV_CFG_CRC register) and enable the configuration CRC.

If the device stays in the DIAGNOSTIC state for the time-out interval and the DIAGNOSTIC state ($t_{DIAG\_STATE\_TO}$), the device goes into the SAFE state and the DIAG_STATE_TO status bit is set. Therefore, all device and system-level diagnostics must be completed within the $t_{DIAG\_STATE\_TO}$ time. To support software development, however, the TPS65313-Q1 device allows the user to mask the DIAGNOSTIC state time-out event and to keep the device in the DIAGNOSTIC state. This ability is achieved through the DIAG_EXIT_MASK SPI bit which can be set by the MASK_DIAG_EXIT command.When DIAG_EXIT_MASK bit is set to 1b device transitions to RESET state if WD_RTS_EN bit is set to 1b and accumulated watchdog failure counter (WD_FC) reached watchdog reset threshold value WD_FC_RST_TH.

While the device is in DIAGNOSTIC state the WD TIME_OUT event can be used by the MCU application software (SW) to establish synchronization between the device and MCU SW and HW processes. Each WD TIME_OUT event is followed by the start of a new WD Q&A sequence run. Another way to synchronize the MCU and the device WD function is updating the device WD configuration or WD window duration. Each watchdog configuration update increments the WD_FAIL_CNT[3:0] counter by 1, followed by the start of a new WD Q&A sequence run. All events that trigger new WD cycle start are covered in WD Function Initialization 表 11-13. Default setting for WD_RST_EN bit is 1b.

11.13.6 ACTIVE State

The device can enter the ACTIVE state only from the DIAGNOSTIC state, when the MCU sets the DIAG_EXIT control bit and the WD_FAIL, and when the MCU_ESM_FAIL status bits have been cleared. As the device goes into the ACTIVE state, the watchdog failure counter (WD_FC) and failure counter for the MCU error-pin (MCU_ESM_FC) are initialized to their default values.

While the device is in the ACTIVE state, the system MCU cannot change any device configuration register bit but can read them out through the SPI. All monitoring and protection functions stay enabled in the ACTIVE state.

To activate the ENDRV/nIRQ output driver, the system MCU must service the watchdog function to decrement the watchdog failure counter (WD_FC) to less than the default (or programmed) WD_FC_ENDRV_TH threshold value. The ENDRV_EN control bit is then set to 1b.

While the device is in the ACTIVE state, the system MCU can enable the device ABIST scheduler to run analog diagnostic tests in synchronization with the watchdog-function scheduler. If the ENDRV/nIRQ driver is activated, and if any of the BUCK1_OT_WARN_IRQ_EN, BUCK12_OT_WARN_IRQ_EN, or BOOST_OT_WARN_IRQ_EN bits are set, then the ABIST comparator diagnostic test toggles the ENDRV/nIRQ pin for the ABIST test-pulse duration shown in 図 11-5. This diagnostic test does not clear the ENDRV_EN control bit and does not cause the device to go to the SAFE state.

11.13.7 SAFE State

The device goes into the SAFE state from the DIAGNOSTIC state or the ACTIVE state when one of the global SAFE state conditions is met or when the MCU_ESM_FC failure counter accumulates to the threshold levels defined in the SAFETY_CFG4 register. The device goes from the RESET state to the SAFE state if the device error counter (DEV_ERR_CNT) reaches the threshold level for the SAFE state lock defined by the SAFE_LOCK_TH[3:0] bits in the SAFETY_CFG1 register. The device goes from the SAFE sate and to the DIAGNOSTIC state when the system MCU sends the SAFE_EXIT command.

When the device goes into the SAFE state, the following occurs:

- The device error counter (DEV_ERR_CNT) increments (except when the device goes from the RESET state).
- The WD_RST_EN bit is masked (no watchdog RESET event is generated if the WD_RST_EN bit is set to 1b and the WD failure counter reaches the reset threshold). After SAFE_EXIT SPI command device transitions to RESET state if WD_RST_EN bit is set to 1b and the WD failure counter reached the WD reset threshold value WD_FC_RST_TH.
- The ENDRV_EN control bit is cleared.
- The ENDRV/nIRQ output is driven low, which functions as an interrupt to the system MCU, as a way to disable external safing paths or peripherals, or both.
- The NRES stays driven high.

The SAFE state time-out is a protection feature against an unresponsive MCU that would keep the device locked in the SAFE state (SAFE LOCK condition). The SAFE state time-out duration is configurable through the SAFE_TO_CFG[1:0] configuration bits in the SAFETY_CFG1 register. To support customer software development, the SAFE state time-out protection feature can be disabled. Disabling this feature is done through the SAFE_TO_DIS bit in addition to the programmed SAFE state device error counter lock threshold value, SAFE_LOCK_TH. The SAFE state time-out is disabled when the SAFE_TO_DIS bit is set to 1b and the accumulated device error counter is greater than the SAFE state device error counter lock threshold value, SAFE_LOCK_TH.

During a SAFE LOCK condition, the device could go to the RESET state because of a global RESET event. When a global RESET condition is removed and the NRES extension is complete (and the NRES pin driven high), the device goes back to the SAFE state because the SAFE LOCK condition still occurs.

By default, the SAFE state time-out feature is disabled (the SAFE_TO_DIS bit is set to 1b) and the SAFE_LOCK_TH[3:0] bit is set to 0b. Disabling the SAFE state time-out enables easier system-software development because the system starts-up with the unprogrammed MCU. The SAFE_TO_DIS bit and the SAFE_LOCK_TH bits can only be changed when the device is in the DIAGNOSTIC state.

While the device is in the SAFE state, the system MCU can activate either a full ABIST run or an individual ABIST diagnostic test through the SPI.

While the device is in SAFE state the WD TIME_OUT event can be used by the MCU application software (SW) to establish synchronization between the device and MCU SW and HW processes. Each WD TIME_OUT event is followed by the start of a new WD Q&A sequence run. Default setting for WD_RST_EN bit is 1b.

11.13.8 State Transition Priorities

The device state transitions have different priorities. The order of priorities are as follows:

1. All global conditions for the OFF state transition (priority I).

2. All global conditions for the RESET state transition (priority II).
3. All global conditions to stay in the SAFE state (priority III).

All other state transitions have a lower priority than the global state transitions with priority I through priority III.

11.14 Wakeup

The TPS65313-Q1 device has a single wake-up pin (WAKE) that detects wake-up requests when the voltage at the WAKE pin increases to greater than 4.6 V (typical $V_{WAKE-ON}$ threshold level). The WAKE pin is edge sensitive and has a deglitch time of 130 µs (typical).

The wake-up signal after the deglitch time is latched in the WAKE_L status bit. and the deglitched WAKE input signal is latched in the WAKE status bit. When a valid wake-up event is detected (the WAKE_L bit is set to 1b), the device enables the internal references, regulators, and monitoring circuits. The device also runs basic diagnostics on the battery input voltage, internal references and supplies, and the SYSCLK clock before releasing the NPOR signal to the digital core. Otherwise, the device goes back to the OFF state with the failure conditions latched in the Analog_Latch.

Under normal operating conditions, the TPS65313-Q1 device stays in one of the operating states (RESET, DIAGNOSTIC, ACTIVE, or SAFE) until the MCU clears the WAKE_L latch status bit by sending a CLR_WAKE_LATCH SPI command.

If the TPS65313-Q1 device enters the OFF state, it stays in the OFF state even if the WAKE pin is kept high with the AUTO_START_DIS bit in the DEV_STAT1 register set to 1b. In this case, the device only restarts in response to a low-high toggle at the WAKE pin. If the AUTO_START_DIS bit is cleared by the CLR_AUTO_START_DIS command, and if the device goes into the OFF state, then the TPS65313-Q1 device tries to power up again as long as the WAKE pin voltage stays above its $V_{WAKE-ON}$ threshold level. The SET_AUTO_START_DIS and CLR_AUTO_START_DIS commands can be executed after the device powers up and reaches one of the three operating states (DIAGNOSTIC, ACTIVE, or SAFE).

Many automotive applications that are powered from KL15 (or switched bather supply) benefit from the employment of an enable divider (R_{ENT} and R_{ENB}) as shown in 図 11-35. Establishing an input voltage UVLO level in a precision system for the BUCK1 regulator, if starting up the device or system at less than the minimum input voltage level is not allowed. The device has an input-voltage monitor to detect the minimum required supply level to start up the device. In the OFF state, the input-voltage monitor is disabled to reduce device-power consumption.

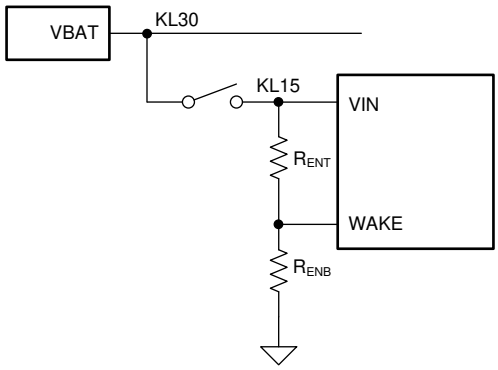


図 11-35. System UVLO by Enable Dividers

11.15 Serial Peripheral Interface (SPI)

The primary communication between the device and the system MCU is through a SPI bus. The SPI bus provides full-duplex communication in a master-slave configuration. The system MCU is always a SPI master device that sends command requests on the SDI pin and receives device responses on the SDO pin. The TPS65313-Q1 device is always a SPI slave device that receives command requests and sends responses (status and measured values) to the external MCU over the SDO line.

The features of the SPI are listed as follows:

- A four-pin interface that includes the following pins:
  - NCS, which is the SPI chip select (active low).
  - SCK, which is the SPI clock.
  - SDI, which is the SPI slave-in and master-out (SIMO) pin.
  - SDO, which is the SPI slave-out and master-in (SOMI) tri-state output.
- A frame size of 24 bits or 16 bits that includes the following:
  - 24 bits
    - 8 bits for commands
    - 8 bits for data
    - 8 bits for CRC when SPI CRC protection is enabled
  - 16 bits
    - 8 bits for commands
    - 8 bits for data
- Data rate of up to 8 Mbps
- The commands and data shift with the most significant bit (MSB) first and the least significant bit (LSB) last.
- On the falling edge of the SCK pin, the SPI samples the SDI line.
- On the rising edge of the SCK pin, the SPI shifts out the data on the SDO pin.

The SPI communication starts with the falling edge of the NCS pin, and ends with the rising edge of the NCS pin. A logic-high level on the NCS pin of the device keeps the SPI of the device in the RESET state and the SDO pin in the high-impedance state (tri-state). The SPI is disabled when the device is in the OFF, INIT, or RESET state (the device returns all 0 s to any SPI command request).

When the TPS65313-Q1 device releases the NRES pin output buffer driver in the DIAGNOSTIC, ACTIVE, or SAFE state, the SPI is accessible regardless of the state of the NRES pin. The NRES_ERR status bit in the SAFETY_ERR_STAT register is set to 1b in case a mismatch between the input of NRES output buffer driver and the output of the NRES input buffer driver is detected.

The size configuration of the SPI frame occurs only in the DIAGNOSTIC state. The default SPI frame is 16-bits (without the CRC-protection field). The SPI frame-size configuration bit is protected by the device-configuration CRC (DEV_CFG_CRC) protection mechanism.

The SPI does not support back-to-back (burst) SPI-frame operation. Instead, after each SPI command (either a SPI read or SPI write access), the NCS pin must change from low to high before the next SPI transfer can start. The minimum time, $t_{hl(cs)}$, between two SPI commands during which the NCS pin must stay high is 788 ns.

11.15.1 SPI Command Transfer Phase

表 11-15 shows the transfer frame format of SPI data during a command or read access.

表 11-15. Transfer Frame Format of SPI Data—Command or Read Access

7	6	5	4	3	2	1	0
CMD[7]	CMD[6]	CMD[5]	CMD[4]	CMD[3]	CMD[2]	CMD[1]	CMD[0]

CMD[7:0] Register WR or RD Command

11.15.2 SPI Data Transfer Phase

表 11-16 shows the transfer frame format of SPI data during a write access.

表 11-16. Transfer Frame Format of SPI Data—Write Access

7	6	5	4	3	2	1	0
DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]

DATA[7:0] Data value for write access (8 bits)

11.15.3 Device SPI Status Flag Response Byte

表 11-17 shows the response frame format of the SPI data status during a command or a read or write access.

表 11-17. Response Frame Format of the Device SPI Data—Command or Read or Write Access

7	6	5	4	3	2	1	0
STAT[7]	STAT[6]	STAT[5]	STAT[4]	STAT[3]	STAT[2]	STAT[1]	STAT[0]

STAT[7:5] These status bits are in a fixed toggling pattern (101) for protection against short-to-ground or short-to-supply-voltage conditions.

STAT[4] This status bit indicates that device is in the SAFE state.

STAT[3] This status bit indicates a software (SW) Interrupt event when one or more status bits are set in the SAFETY_ERR_STATx, SAFETY_CLK_STAT, SAFETY_CLK_WARN_STAT, or SAFETY_ABIST_ERR_STATx registers. This bit stays set until all error status bits are cleared by reading the listed status registers.

STAT[2] This status bit indicates that the watchdog has detected a WD Q&A sequence run error, (indicated by the ANSW_ERR status bit), a sequence error (indicated by SEQ_ERR status bit), or a WD Q&A sequence run time-out event. The SPI sets this bit only in the first SPI-frame after the watchdog has detected such a failure. In the next SPI-frame after that, the SPI clears this bit.
The SPI clears this bit when the device goes into the RESET state.

注

A write access to the WDT_WIN1_CFG or WDT_WIN2_CFG register does not set the STAT[2] status bit.

STAT[1] This status bit indicates that the ESM has detected an incorrect event (indicated by MCU_ESM_FAIL status bit which increments the MCU_ESM_FC[3:0] counter). The SPI sets this bit only in the fist SPI frame after the ESM detects the incorrect event. In the next SPI frame after that, the SPI clears this bit.
The SPI clears this bit when the device goes into the RESET state.

STAT[0] This status bit indicates that the previous SPI frame was invalid. This bit clears when the next SPI frame transmission is valid or when the device goes to the RESET state. This bit is set only when one of events latched in the SPI_TRANSFER_STAT register are detected during the previous SPI frame. The STAT[0] status bit indicates different invalid SPI transfer events that are latched in the SPI_INV_TRAN_STAT register. The events are as follows:

1. A SPI SDO error (mismatch between the SPI driver output and SDO pin feedback input).
2. A SPI frame shorter than 24 or 16 SPI-clock cycles (or prematurely terminated SPI frame).
3. A SPI frame longer than 24 or 16 SPI-clock cycles.
4. An invalid SPI command (essentially a command reserved for production test).
5. An undefined SPI command (essentially an unassigned command).
6. Master CRC error on the received SPI frame.
7. A logic-high level on the SCK pin at the moment the logic level on the NCS pin changes from high to low.
8. A logic-high level on the SCK pin at the moment the logic level on the NCS pin changes from low to high.
9. A SPI transfer terminated by a RESET event.

The SPI frame, or command, is ignored each time when one of the error conditions, condition 2 through condition 7, is detected. A SPI SDO error does not cause the device to ignore a valid SPI command received from the MCU SPI master device.

11.15.4 Device SPI Data Response

表 11-18 shows the response frame format of the SPI device data during a read access.

表 11-18. Response Frame Format of the Device SPI Data—Read Access

7	6	5	4	3	2	1	0
R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]

R[7:0] Internal registers value. All unused bits are set to zero.

11.15.5 Device SPI Master CRC (MCRC) Input

表 11-19 shows the input frame format of the MCRC-checksum value (received by the device on the SDI pin).

表 11-19. Input Frame Format of the MCRC Checksum Value

7	6	5	4	3	2	1	0
MCRC[7]	MCRC[6]	MCRC[5]	MCRC[4]	MCRC[3]	MCRC[2]	MCRC[1]	MCRC[0]

MCRC[7:0] An 8-bit checksum value from the SPI master device. The device calculates the MCRC[7:0] checksum based on the CMD[7:0] command bits and DATA[7:0] bits which the device receives on the SDI pin.

A master CRC8 check is performed in SPI receive engine of the device. The check starts when the SPI NCS pin is driven low and the status is reported after the SPI NCS pin is driven high. If the master CRC8 error is detected, the following occurs:

- A SPI command or request from the MCU SPI master device is ignored.
- The SPI_MASTER_CRC_ERR status bit is set in the SPI_TRANSFER_STAT register.
- After the SPI frame, the device returns the SPI status word with the STAT[0] bit set.

11.15.6 Device SPI Slave CRC (SCRC) Output

表 11-20 shows the output frame format of the SCRC-checksum value (transmitted by the device on the SDO pin).

表 11-20. Output Frame Format of the SCRC Checksum Value

7	6	5	4	3	2	1	0
SCRC[7]	SCRC[6]	SCRC[5]	SCRC[4]	SCRC[3]	SCRC[2]	SCRC[1]	SCRC[0]

SCRC[7:0] An 8-bit checksum value from the SPI slave device (TPS65313-Q1). The device calculates the SCRC[7:0] checksum based on the STAT[7:0] status Bits and the data which the device transfers on the SDO pin.

A slave CRC8 check is performed by the MCU SPI master device. The check starts when the SPI NCS pin is driven low and the status is reported after the SPI NCS pin is driven high.

Both the master and slave devices use a standard CRC-8 polynomial to calculate the checksum value: $X^8 + X^2 + X + 1$.The CRC algorithm details are as follows:

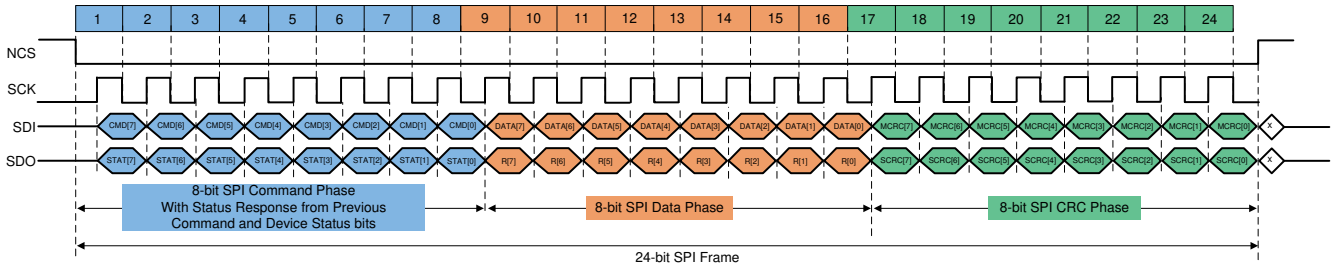
- Initial value for the remainder is all 1 s.
- Big-endian bit stream order.
- The CRC calculated for the following string {CMD[7:0], DATA[7:0]}, with the CMD[7] bit as the first bit that is shifted out and the DATA[0] bit as the last bit shifted out (see 表 11-21).
- Result inversion is not enabled.

表 11-21. SPI Frame for Command and Data Phases

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CMD[7]	CMD[6]	CMD[5]	CMD[4]	CMD[3]	CMD[2]	CMD[1]	CMD[0]	DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]

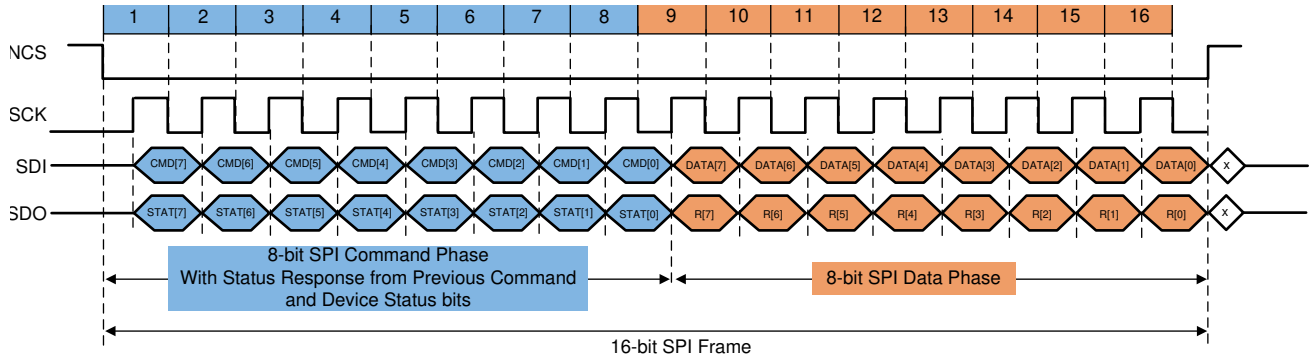
11.15.7 SPI Frame Overview

図 11-36 shows an overview of a complete 24-bit SPI frame with the CRC field. 図 11-37 shows an overview of a complete 16-bit SPI frame without the CRC field.



1. The SPI master device (MCU) and SPI slave device (TPS65313-Q1) sample the received data on the falling SCK edge and transmit data on the rising SCK edge.

図 11-36. SPI Timing (24-Bit With CRC Field)



1. The SPI master device (MCU) and SPI slave device (TPS65313-Q1) sample the received data on the falling SCK edge and transmit data on the rising SCK edge.

図 11-37. SPI Timing (16-Bit Without CRC Field)

11.16 Register Maps

11.16.1 Device SPI Mapped Registers

The tables in this section lists the available SPI registers and includes an explanation of each bit function. For each SPI register, the bit names are given, with the default values, which are the values after internal logic reset and when the device is in the RESET state. These default values apply after each wake-up event when the device goes to the RESET state.

表 11-22 lists the SPI commands. The name of a SPI read command starts with the *RD_* prefix and the name of a SPI write command name starts with the *WR_* prefix.

表 11-22. SPI Command Space Table

Command No.	Register No.	Command Code	Command Type	WR SW Lock Protection	Command Name
1		0xC1	Single SPI execution commands without associated memory-mapped register	—	SET_CTRL_LOCK with data 0x55 (to lock SPI WR access to listed control registers)
2		0xC2		—	CLR_CTRL_LOCK with data 0xAA (to unlock SPI WR access to listed control registers)
3		0xF1		—	SET_CTRL_BIST_LOCK with data 0x55 (to lock SPI WR access to listed ABIST and LBIST control registers)
4		0xF2		—	CLR_CTRL_BIST_LOCK with data 0xAA (to unlock SPI WR access to listed ABIST and LBIST control registers)
5		0xC4		—	SET_CFG_LOCK with data 0x55 (to lock SPI WR access to listed configuration registers)
6		0xC7		—	CLR_CFG_LOCK with data 0xAA (to unlock SPI WR access to listed configuration registers)
7		0xDE		—	CLR_WAKE_LATCH with data 0x8E (to clear WAKE_L status bit)
8		0xF8		—	MCU_RST_REQ with data 0x5A (to initiate the device transition to the RESET state)
9		0xF4		—	CLR_AUTO_START_DIS with data 0x55 (to clear AUTO_START_DIS bit)
10		0xF7		—	SET_AUTO_START_DIS with data 0xAA (to set AUTO_START_DIS bit)
11	1	0x01		—	RD_DEV_REV
12	2	0x02		—	RD_DEV_ID
13	3	0x07	SPI status register commands	—	RD_DEV_STAT1
14	4	0x08		—	RD_DEV_STAT2
15	5	0xFB	SPI configuration register commands (with WR SW lock state controlled by SET_CFG_LOCK and CLR_CFG_LOCK commands)	YES	WR_DEV_CFG1 (SPI WR update can occur only in the DIAGNOSTIC state)
16		0x0B		—	RD_DEV_CFG1
17	6	0xFD		YES	WR_DEV_CFG2 (SPI WR update can occur only in the DIAGNOSTIC state)
18		0x0D		—	RD_DEV_CFG2
19	7	0xFE		YES	WR_DEV_CFG3 (SPI WR update can occur only in the DIAGNOSTIC state)
20		0x0E		—	RD_DEV_CFG3
21	8	0xE1		YES	WR_DEV_CFG4 (SPI WR update can occur only in the DIAGNOSTIC state)
22		0x11		—	RD_DEV_CFG4
23	9	0xE2		YES	WR_SAFETY_CFG1 (SPI WR update can occur only in the DIAGNOSTIC state)
24		0x12		—	RD_SAFETY_CFG1
25	10	0xE4		YES	WR_SAFETY_CFG2 (SPI WR update can occur only in the DIAGNOSTIC state)
26		0x14		—	RD_SAFETY_CFG2
27	11	0xE7		YES	WR_SAFETY_CFG3 (SPI WR update can occur only in the DIAGNOSTIC state)
28		0x17		—	RD_SAFETY_CFG3
29	12	0xE8		YES	WR_SAFETY_CFG4 (SPI WR update can occur only in the DIAGNOSTIC state)
30		0x18		—	RD_SAFETY_CFG4
31	13	0xEB		YES	WR_SAFETY_CFG5 (SPI WR update can occur only in the DIAGNOSTIC state)
32		0x1B		—	RD_SAFETY_CFG5
33	14	0xED		YES	WR_SAFETY_CFG6 (SPI WR update can occur only in the DIAGNOSTIC state)
34		0x1D		—	RD_SAFETY_CFG6
37	16	0xD2		YES	WR_SAFETY_CFG8 (SPI WR update can occur only in the DIAGNOSTIC state)
38		0x22		—	RD_SAFETY_CFG8
39	17	0xD4		YES	WR_EXT_VMON1_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
40		0x24		—	RD_EXT_VMON1_CFG
41	18	0xD7		YES	WR_EXT_VMON2_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
42		0x27		—	RD_EXT_VMON2_CFG
43	19	0xD8	SPI control register commands (with WR SW lock state controlled by SET_CTRL_LOCK and CLR_CTRL_LOCK commands)	YES	WR_PWR_CTRL
44		0x28		—	RD_PWR_CTRL
45	20	0xDD		YES	WR_CLK_MON_CTRL
46		0x2D		—	RD_CLK_MON_CTRL

表 11-22. SPI Command Space Table (続き)

Command No.	Register No.	Command Code	Command Type	WR SW Lock Protection	Command Name
47	21	0x2E	SPI status register commands	—	RD_VMON_UV_STAT
48	22	0x31		—	RD_VMON_OV_STAT
49	23	0x32		—	RD_EXT_VMON_STAT
50	24	0x34		—	RD_SAFETY_BUCK1_STAT1
51	25	0x37		—	RD_SAFETY_BUCK1_STAT2
52	26	0x38		—	RD_SAFETY_BUCK2_STAT1
53	27	0x3B		—	RD_SAFETY_BUCK2_STAT2
54	28	0x3D		—	RD_SAFETY_BOOST_STAT1
55	29	0x3E		—	RD_SAFETY_BOOST_STAT2
56	30	0x41		—	RD_SAFETY_ERR_STAT1
57	31	0x42		—	RD_SAFETY_CLK_STAT
58	32	0xCE		—	RD_SAFETY_CLK_WARN_STAT
59	33	0x44		—	RD_SAFETY_ABIST_ERR_STAT1
60	34	0x47		—	RD_SAFETY_ABIST_ERR_STAT2
61	35	0x48		—	RD_SAFETY_ABIST_ERR_STAT3
62	36	0x4B		—	RD_SAFETY_ABIST_ERR_STAT4
63	37	0x4D		—	RD_SAFETY_ABIST_ERR_STAT5
64	38	0x4E		—	RD_SAFETY_ABIST_ERR_STAT6
65	39	0x51		—	RD_SAFETY_LBIST_ERR_STAT
66	40	0x52		—	RD_SAFETY_ERR_STAT2
67		0xA4	SPI status register commands (with WR SW lock state controlled by SET_CFG_LOCK and CLR_CFG_LOCK commands)	YES	WR_WD_FC (SPI WR update can occur only in the DIAGNOSTIC state and updates only the WD_FAIL_CNT[3:0] bits in the SAFETY_ERR_STAT2 register)
68	41	0x54		—	RD_SAFETY_ERR_STAT3
69		0xA7		YES	WR_MCU_ESM_FC (SPI WR update can occur only in the DIAGNOSTIC state and updates only the MCU_ESM_FC[3:0 bits in the SAFETY_ERR_STAT3 register)
70	42	0x57		—	RD_SAFETY_ERR_STAT4
71		0xA8		YES	WR_DEV_ERR_CNT (SPI WR update can occur only in the DIAGNOSTIC state and updates only the DEV_ERR_CNT[3:0 bits in the SAFETY_ERR_STAT4 register)
72	45	0x58		—	RD_SPI_TRANSFER_STAT
73	46	0xAB	SPI control register commands	NO	WR_SAFETY_ABIST_CTRL
74		0x5B		—	RD_SAFETY_ABIST_CTRL
75	47	0xAD		NO	WR_SAFETY_LBIST_CTRL
76		0x5D		—	RD_SAFETY_LBIST_CTRL
77	48	0xAE		NO	WR_SAFETY_CHECK_CTRL
78		0x5E		—	RD_SAFETY_CHECK_CTRL

表 11-22. SPI Command Space Table (続き)

Command No.	Register No.	Command Code	Command Type	WR SW Lock Protection	Command Name
79	49	0x91	SPI configuration register commands (with WR SW lock state controlled by SET_CFG_LOCK and CLR_CFG_LOCK commands)	YES	WR_SAFETY_ERR_PWM_HMAX_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
80		0x61		—	RD_SAFETY_ERR_PWM_HMAX_CFG
81	50	0x92		YES	WR_SAFETY_ERR_PWM_HMIN_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
82		0x62		—	RD_SAFETY_ERR_PWM_HMIN_CFG
83	51	0x94		YES	WR_SAFETY_ERR_PWM_LMAX_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
84		0x64		—	RD_SAFETY_ERR_PWM_LMAX_CFG
85	52	0x97		YES	WR_SAFETY_ERR_PWM_LMIN_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
86		0x67		—	RD_SAFETY_ERR_PWM_LMIN_CFG
87	53	0x98		YES	WR_SAFETY_PWD_TH_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
88		0x68		—	RD_SAFETY_PWD_TH_CFG
89	54	0x9B		YES	WR_SAFETY_DEV_CFG_CRC (SPI WR update can occur only in the DIAGNOSTIC state)
90		0x6B		—	RD_SAFETY_DEV_CFG_CRC
91	55	0x9D		YES	RESERVED
92		0x6D		—	RESERVED
93	56	0x9E		YES	RESERVED
94		0x6E		—	RESERVED
95	57	0xA1		YES	RESERVED
96		0x71		—	RESERVED
97	58	0xA2		YES	RESERVED
98		0x72		—	RESERVED
99	59	0xB7		YES	WR_SPI_STORAGE_REGISTER1
100		0x74		—	RD_SPI_STORAGE_REGISTER1
101	60	0xB8		YES	WR_SPI_STORAGE_REGISTER2
102		0x77		—	RD_SPI_STORAGE_REGISTER2
103	61	0xBE	SPI control register commands	NO	WR_DIAG_CTRL
104		0x78		—	RD_DIAG_CTRL
105	62	0x8B		NO	WR_DIAG_MUX_SEL
106		0x7B		—	RD_DIAG_MUX_SEL
107	63	0x8D	SPI configuration register commands (with WR SW lock state controlled by SET_CTRL_LOCK and CLR_CTRL_LOCK commands)	YES	WR_WDT_WIN1_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
108		0x7D		—	RD_WDT_WIN1_CFG
109	64	0x8E		YES	WR_WDT_WIN2_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
110		0x7E		—	RD_WDT_WIN2_CFG
111	65	0xB1		YES	WR_WDT_Q&A_CFG (SPI WR update can occur only in the DIAGNOSTIC state)
112		0x81		—	RD_WDT_Q&A_CFG
113	66	0x82	Single SPI execution commands without associated memory-mapped register	—	RD_WDT_QUESTION_VALUE
114	67	0x84		—	RD_WDT_STATUS
115	68	0xB2		NO	WR_WDT_ANSWER
116	69	0x88	SPI status register commands	—	RD_OFF_STATE_L_STAT
117		0x04	Single SPI execution commands without associated memory-mapped register		MASK_DIAG_EXIT
118		0x87			UNMASK_DIAG_EXIT
119		0xC8			EN_SAFE_TO
120		0xCB			DIS_SAFE_TO
121		0xCD			SAFE_EXIT

11.16.1.1 Memory Maps

11.16.1.1.1 SPI Registers

表 11-23 lists the memory-mapped registers for the SPI. All registers not listed in 表 11-23 should be considered as reserved locations and the register contents should not be modified.

表 11-23. SPI Registers

Acronym	Register Name	Section
DEV_REV	Device Revision	Go
DEV_ID	Device ID	Go
DEV_STAT1	Device Status 1	Go
DEV_STAT2	Device Status 2	Go
DEV_CFG1	Device Configuration 1	Go
DEV_CFG2	Device Configuration 2	Go
DEV_CFG3	Device Configuration 3	Go
DEV_CFG4	Device Configuration 4	Go
SAFETY_CFG1	Safety Configuration 1	Go
SAFETY_CFG2	Safety Configuration 2	Go
SAFETY_CFG3	Safety Configuration 3	Go
SAFETY_CFG4	Safety Configuration 4	Go
SAFETY_CFG5	Safety Configuration 5	Go
SAFETY_CFG6	Safety Configuration 6	Go
SAFETY_CFG8	Safety Configuration 8	Go
EXT_VMON1_CFG	External VMON1 Configuration	Go
EXT_VMON2_CFG	External VMON2 Configuration	Go
PWR_CTRL	Power Control	Go
CLK_MON_CTRL	Clock Monitor Control	Go
VMON_UV_STAT	VMON Undervoltage Status	Go
VMON_OV_STAT	VMON Overvoltage Status	Go
EXT_VMON_STAT	External VMON Status	Go
SAFETY_BUCK1_STAT1	Safety BUCK1 Status 1	Go
SAFETY_BUCK1_STAT2	Safety BUCK1 Status 2	Go
SAFETY_BUCK2_STAT1	Safety BUCK2 Status 1	Go
SAFETY_BUCK2_STAT2	Safety BUCK2 Status 2	Go
SAFETY_BOOST_STAT1	Safety BOOST Status 1	Go
SAFETY_BOOST_STAT2	Safety BOOST Status 2	Go
SAFETY_ERR_STAT1	Safety Error Status 1	Go
SAFETY_CLK_STAT	Safety Clock Status	Go
SAFETY_CLK_WARN_STAT	Safety Clock Warning Status	Go
SAFETY_ABIST_ERR_STAT1	Safety ABIST Error Status 1	Go
SAFETY_ABIST_ERR_STAT2	Safety ABIST Error Status 2	Go
SAFETY_ABIST_ERR_STAT3	Safety ABIST Error Status 3	Go
SAFETY_ABIST_ERR_STAT4	Safety ABIST Error Status 4	Go
SAFETY_ABIST_ERR_STAT5	Safety ABIST Error Status 5	Go
SAFETY_ABIST_ERR_STAT6	Safety ABIST Error Status 6	Go
SAFETY_LBIST_ERR_STAT	Safety LBIST Error Status	Go
SAFETY_ERR_STAT2	Safety Error Status 2	Go
SAFETY_ERR_STAT3	Safety Error Status 3	Go
SAFETY_ERR_STAT4	Safety Error Status 4	Go
SPI_TRANSFER_STAT	SPI Transfer Status	Go
SAFETY_ABIST_CTRL	Safety ABIST Control	Go
SAFETY_LBIST_CTRL	Safety LBIST Control	Go
SAFETY_CHECK_CTRL	Safety Check Control	Go

表 11-23. SPI Registers (続き)

Acronym	Register Name	Section
SAFETY_ERR_PWM_HMAX_CFG	Safety Error PWM HMAX Configuration	Go
SAFETY_ERR_PWM_HMIN_CFG	Safety Error PWM HMIN Configuration	Go
SAFETY_ERR_PWM_LMAX_CFG	Safety Error PWM LMAX Configuration	Go
SAFETY_ERR_PWM_LMIN_CFG	Safety Error PWM LMIN Configuration	Go
SAFETY_PWD_TH_CFG	Safety PWD Threshold Configuration	Go
SAFETY_DEV_CFG_CRC	Safety Device Configuration CRC	Go
DIAG_CTRL	Diagnostic Mux Control	Go
DIAG_MUX_SEL	Diagnostic Mux Select	Go
WDT_WIN1_CFG	Watchdog Window 1 Configuration	Go
WDT_WIN2_CFG	Watchdog Window 2 Configuration	Go
WDT_Q&A_CFG	Watchdog Q&A Configuration	Go
WDT_QUESTION_VALUE	Watchdog Question Value	Go
WDT_STATUS	Watchdog Status	Go
WDT_ANSWER	Watchdog Answer	Go
OFF_STATE_L_STAT	OFF State L Status	Go

Complex bit access types are encoded to fit into small table cells. 表 11-24 shows the codes that are used for access types in this section.

表 11-24. SPI Register Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value.
-X		Value depends on the orderable part number or as described.

DEV_REV Register

DEV_REV is shown in 図 11-38 and described in 表 11-25.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read-Only (RD_DEV_REV)

図 11-38. Device Revision (DEV_REV) Register

7	6	5	4	3	2	1	0
MAJOR_REV[3:0]				MINOR_REV[3:0]			
R-0010b				R-0000b			

表 11-25. DEV_REV Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-4	MAJOR_REV[3:0]	R	0010b	Device major revision.
3-0	MINOR_REV[3:0]	R	0001b	Device minor revision.

DEV_ID Register

DEV_ID is shown in 図 11-39 and described in 表 11-26. For DEV_ID register bits initial values refer to device Technical Reference Manual (TRM).

Return to 表 11-23

Initialization source: NPOR
Controller access: Read-Only (RD_DEV_ID1)
No dedicated EEPROM bits are required.

図 11-39. Device ID (DEV_ID) Register

7	6	5	4	3	2	1	0

表 11-26. DEV_ID Register Field Descriptions

Bit	Field	Type	Initial State	Description
4	NRES_EXT_DELAY	R	0b	NRES Extension Delay configuration 0b = LONG NRES Extension Delay (32 ms - 33 ms). 1b = SHORT NRES Extension Delay (2 ms - 3 ms)
3	RESERVED	R	0b	Reserved.

DEV_STAT1 Register

DEV_STAT1 is shown in 図 11-40 and described in 表 11-27.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read-Only (RD_DEV_STAT1)

図 11-40. Device Status 1 (DEV_STAT1) Register

7	6	5	4	3	2	1	0
FSM[2:0]			RESERVED	AUTO_START_DIS	CFG_LOCK	CTRL_BIST_LOCK	CTRL_LOCK
R-000b			R-0b	R-0b	R-1b	R-1b	R-1b

表 11-27. DEV_STAT1 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-5	FSM[2:0]	R	000b	Current device state. In the RESET state, the devices SPI communication is disabled and the device returns all 0 s to any SPI command. In the OFF state, the device is fully powered down including the digital core. 000b = Not used. 001b = DIAGNOSTIC state. 010b = ACTIVE state. 100b = SAFE state.
4	RESERVED	R	0b	Reserved

表 11-27. DEV_STAT1 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
3	AUTO_START_DIS	R	0b	Auto restart enable-latch value which controls whether device automatic restart is allowed when the device goes to the OFF state while the WAKE input is high. This bit is set by the SET_AUTO_START_DIS command with data 0xAA and cleared by the CLR_AUTO_START_DIS command with data 0x55. NOTE: This bit is NOT initialized by an NPOR event unless the event is preceded by loss of battery supply at the VIN, VINA, and VIN_SAFE pins. This bit is set to 1b every time a valid VREG OV event is detected. 0b = Auto restart is enabled when the device reaches the OFF state and the WAKE input is still high. 1b = Auto restart is disabled when the device goes to the OFF state and the WAKE input is still high. To start up the device, the WAKE input must toggle from low to high.
2	CFG_LOCK	R	1b	Write-protect flag for the device configuration registers. This bit is set by the SET_CFG_LOCK SPI command with data 0x55 while the device is in the DIAGNOSTIC, or when the device exits the DIAGNOSTIC state, or on completion of the LBIST run. This bit is cleared by the CLR_CFG_LOCK SPI command with data 0xAA while the device is in the DIAGNOSTIC state.
1	CTRL_BIST_LOCK	R	1b	Write-protect flag for the SAFETY_ABIST_CTRL and SAFETY_LBIST_CTRL registers. This bit is set by the SET_CTRL_LOCK SPI command with data 0x55 while the device is in the DIAGNOSTIC, ACTIVE or SAFE state, or when the device exits the DIAGNOSTIC, ACTIVE or SAFE state, or on completion of the LBIST run. This bit is cleared by the CLR_CTRL_LOCK SPI command with data 0xAA while the device is in the DIAGNOSTIC, ACTIVE or SAFE state.
0	CTRL_LOCK	R	1b	Write-protect flag for device control registers. This bit is set by the SET_CTRL_LOCK SPI command with data 0x55 while the device is in the DIAGNOSTIC, ACTIVE, or SAFE state, or when the device exits the DIAGNOSTIC state, or on completion of the LBIST run. This bit is cleared by the CLR_CTRL_LOCK SPI command with data 0xAA while the device is in the DIAGNOSTIC, ACTIVE, or SAFE state.

DEV_STAT2 Register

DEV_STAT2 is shown in 図 11-41 and described in 表 11-28.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_DEV_STAT2)

図 11-41. Device Status 2 (DEV_STAT2) Register

7	6	5	4	3	2	1	0
RESERVED	DIAG_EXIT_MASK	SAFE_TO_DIS	MCU_RST_REQ_FLAG	SYNC_IN	MCU_ERR_IN	WAKE_L	WAKE
R-0b	R-0b	R-1b	R-0b	R-0b	R-0b	R-0b	R-0b

表 11-28. DEV_STAT2 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	RESERVED	R	0b	Reserved.
6	DIAG_EXIT_MASK	R	0b	Status of the exit-mask bit for the DIAGNOSTIC state. This bit is set by the MASK_DIAG_EXIT command with 0x55h data and cleared by the UNMASK_DIAG_EXIT command with 0xAA data. 0b = The device transitions to the SAFE state from the DIAGNOSTIC state when the DIAGNOSITC state time-out timer expires. 1b = The device does not transition to the SAFE state from the DIAGNOSTIC state as the DIAGNOSITC state time-out timer is kept in reset.
5	SAFE_TO_DIS	R	1b	Status of the SAFE state time-out function. This bit is set by the DIS_SAFE_TO SPI command with data 0x55 and only when the device is in the DIAGNOSTIC state, and is cleared by the EN_SAFE_TO SPI command with data 0xAA only when the device is in the DIAGNOSTIC state. 0b = The device transitions to the RESET state from the SAFE state when the SAFE state time-out timer (SAFE_TO[1:0]) expires. 1b = The device does not transition to the RESET state from the SAFE state unless following event occurs: — Global RESET condition. — Global OFF state condition. — MCU SW RESET request (through the NCU_RST_RQ SPI command with data 0x5A). — MCU request transition to the DIAGNOSTIC state (SAFE_EXIT command).
4	MCU_RST_REQ_FLAG	R	0b	Flag indicating that the last transition to the RESET state was caused by the MCU through the MCU_RST_REQ SPI command with data 0x5A. The MCU_RST_REQ command can be issued while the device is in the DIAGNOSTIC, ACTIVE, or SAFE state. This bit is not cleared by read command. 0b = No reset requested by the MCU. 1b = Reset requested by the MCU.
3	SYNC_IN	R	0b	Detection of an external clock at the SYNC_IN pin. This bit is valid only when the SMPS_CLK_SRC bit in the DEV_ID register is set to 1b. This bit is set when the SYNC_IN clock monitor detects that clock is driven to SYNC_IN input pin. When the SYNC_IN clock monitor is disabled, this bit is set to 0b. When the SYNC_IN clock monitor is enabled, this bit is set to 1b (when the clock at the SYNC_IN pin is in range) or 0 (when the clock at the SYNC_IN pin is not in range). 0b = No valid clock is detected at the SYNC_IN pin, or DIG_CLK_MON1 is not enabled. 1b = Valid clock detected at the SYNC_IN pin while DIG_CLK_MON1 is enabled.
2	MCU_ERR_IN	R	0b	The MCU_ERR pin state. 0b = MCU_ERR input pin is in low state. 1b = MCU_ERR input pin is in high state.

表 11-28. DEV_STAT2 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
1	WAKE_L	R	0b	Wake-up event detection (latched and deglitched). 0b =No rising-edge event detected at WAKE pin, or previous rising-edge event on the WAKE pin is cleared by the CLR_WAKE_LATCH command with data 0x8E or failure conditions that force the device transition to the OFF state (or anytime the device transitions to the OFF state). 1b = Rising-edge event detected at WAKE pin.
0	WAKE	R	0b	The WAKE pin state (deglitched). 0b = The WAKE pin is in low state. 1b = The WAKE pin is in high state.

DEV_CFG1 Register

DEV_CFG1 is shown in 図 11-42 and described in 表 11-29.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_DEV_CFG1)
Write (WR_DEV_CFG1). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the device-configuration CRC (DEV_CFG_CRC).

図 11-42. Device Configuration 1 (DEV_CFG1) Register

7	6	5	4	3	2	1	0
BOOST_OV_RST_EN	RESERVED	BUCK2_OV_RST_EN	BUCK1_OV_RST_EN	BOOST_UV_RST_EN	RESERVED	BUCK2_UV_RST_EN	BUCK1_UV_RST_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-1b

表 11-29. DEV_CFG1 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	BOOST_OV_RST_EN	R/W	0b	Configuration of BOOST OV event for a global RESET event. 0b = BOOST OV is not a global RESET event. 1b = BOOST OV is a global RESET event.
6	RESERVED	R/W	0b	Reserved
5	BUCK2_OV_RST_EN	R/W	0b	Configuration of BUCK2 OV event for a global RESET event. 0b = BUCK2 OV is not a global RESET event. 1b = BUCK2 OV is a global RESET event.
4	BUCK1_OV_RST_EN	R/W	0b	Configuration of BUCK1 OV event for a global RESET event. 0b = BUCK1 OV is not a global RESET event. 1b = BUCK1 OV is a global RESET event.
3	BOOST_UV_RST_EN	R/W	1b	Configuration of BOOST UV event for a global RESET event. 0b = BOOST UV is not a global RESET event. 1b = BOOST UV is a global RESET event.
2	RESERVED	R/W	0b	Reserved
1	BUCK2_UV_RST_EN	R/W	1b	Configuration of BUCK2 UV event for a global RESET event. 0b = BUCK2 UV is not a global RESET event. 1b = BUCK2 UV is a global RESET event.

表 11-29. DEV_CFG1 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
0	BUCK1_UV_RST_EN	R/W	1b	Configuration of BUCK1 UV event for a global RESET event. 0b = BUCK1 UV is not a global RESET event. 1b = BUCK1 UV is a global RESET event.

DEV_CFG2 Register

DEV_CFG2 is shown in 図 11-43 and described in 表 11-30.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_DEV_CFG2)
Write (WR_DEV_CFG2). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.
Note: Anytime a x_IRQ_EN bit is set to 1b and the respective analog condition occurs, the activated ENDRV/nIRQ driver is disabled (drives the activated ENDRV/nIRQ pin low), the ENDRV_EN control bit is cleared, and the device transitions to the SAFE state.

図 11-43. Device Configuration 2 (DEV_CFG2) Register

7	6	5	4	3	2	1	0
RESERVED				BOOST_OT_WARN_IRQ_EN	RESERVED	BUCK2_OT_WARN_IRQ_EN	BUCK1_OT_WARN_IRQ_EN
R-0000b				R/W-0b	R-0b	R/W-0b	R/W-0b

表 11-30. DEV_CFG2 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-4	RESERVED	R/W	0000b	Reserved.
3	BOOST_OT_WARN_IRQ_EN	R/W	0b	Configuration of BOOST OT warning event for a global nIRQ event. 0b = BOOST OT WARN is not a global nIRQ event. The BOOST_OT_WARN status bit is set. 1b = BOOST OT WARN is a global nIRQ event. The BOOST_OT_WARN status bit is set. The device pulls the ENDRV/nIRQ pin low and clears the ENDRV_EN control bit.
2	RESERVED	R/W	0b	Reserved
1	BUCK2_OT_WARN_IRQ_EN	R/W	0b	Configuration of BUCK2 OT warning event for a global nIRQ event. 0b = BUCK2 OT WARN is not a global nIRQ event. The BUCK2_OT_WARN status bit is set. 1b = BUCK2 OT WARN is a global nIRQ event. The BUCK2_OT_WARN status bit is set. The device pulls the ENDRV/nIRQ pin low and clears the ENDRV_EN control bit.
0	BUCK1_OT_WARN_IRQ_EN	R/W	0b	Configuration of BUCK1 OT warning event for a global nIRQ event. 0b = BUCK1 OT WARN is not a global nIRQ event. The BUCK1_OT_WARN status bit is set. 1b = BUCK1 OT WARN is a global nIRQ event. The BUCK1_OT_WARN status bit is set. The device pulls the ENDRV/nIRQ pin low and clears the ENDRV_EN control bit.

DEV_CFG3 Register

DEV_CFG3 is shown in 図 11-44 and described in 表 11-31.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_DEV_CFG3)
Write (WR_DEV_CFG3). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-44. Device Configuration 3 (DEV_CFG3) Register

7	6	5	4	3	2	1	0
RESERVED			VIN_BAD_IRQ_EN	RESERVED			
R-000b			R/W-0b	R-0000b			

表 11-31. DEV_CFG3 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-5	RESERVED	R	000b	Reserved.
4	VIN_BAD_IRQ_EN	R/W	0b	Configuration of VIN BAD event for a global nIRQ event. 0b = VIN BAD is not a global nIRQ event. 1b = VIN BAD is a global nIRQ event. The device pulls the ENDRV/nIRQ pin low and clears the ENDRV_EN control bit.
3-0	RESERVED	R	0000b	Reserved.

DEV_CFG4 Register

DEV_CFG4 is shown in 図 11-45 and described in 表 11-32.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_DEV_CFG4)
Write (WR_DEV_CFG4). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-45. Device Configuration 4 (DEV_CFG4) Register

7	6	5	4	3	2	1	0
RESERVED		VIN_BAD_TH[1:0]		RESERVED		NRST_EXT	
R-00b		R/W-00b		R-00b		R/W-11	

表 11-32. DEV_CFG4 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-6	RESERVED	R	00b	Reserved
5-4	VIN_BAD_TH[1:0]	R	00b	VIN BAD detection threshold level. 00b = 6.2 V 01b = 7.2 V 00b = 8.2 V 11b = 8.2 V
3-2	RESERVED	R	00b	Reserved

表 11-32. DEV_CFG4 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
1-0	NRES_EXT	R	11b	MCU RESET extension delay (t_{NRES_EXT}). The extension delay range ordering is controlled by EEPROM bit NRES_EXT_DELAY latched as DEV_ID register bit #4. When EEPROM mapped configuration NRES_EXT_DELAY bit is 0b: 00b = 2 ms to 3 ms 01b = 11 ms to 12 ms 10b = 21 ms to 22 ms 11b = 31 ms to 32 ms When EEPROM mapped configuration NRES_EXT_DELAY bit is 1b: 00b = 31 ms to 32 ms 01b = 21 ms to 22 ms 10b = 11 ms to 12 ms 11b = 2 ms to 3 ms

SAFETY_CFG1 Register

SAFETY_CFG1 is shown in 図 11-46 and described in 表 11-33.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_CFG1)
Write (WR_SAFETY_CFG1). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-46. Safety Configuration 1 (SAFETY_CFG1) Register

7	6	5	4	3	2	1	0
RESERVED		SAFE_TO[1:0]		SAFE_LOCK_TH[3:0]			
R-00b		R-00b		R-0000b			

表 11-33. SAFETY_CFG1 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-6	RESERVED	R	00b	Reserved
5-4	SAFE_TO[1:0]	R	00b	The SAFE state time-out 00b = 640 ms 01b = 320 ms 00b = 5 ms 00b = 1.25 ms

表 11-33. SAFETY_CFG1 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
3-0	SAFE_LOCK_TH[3:0]	R	0000b	The SAFE state lock threshold. These bits set the corresponding DEV_ERR_CNT[3:0] threshold at which the device remains in the SAFE state depending on the SAFE_TO_DIS bit setting (bit 5 in the SAFETY_STAT2 register). — When the SAFE_TO_DIS bit is set to 0b, regardless of the SAFE_LOCK_TH[3:0] bit settings, the device transitions to the RESET state from the SAFE state when the SAFE state time-out timer expires. — When the SAFE_TO_DIS bit is set to 1b: — If DEV_ERR_CNT[3:0] ≤ SAFE_LOCK_TH[3:0], the device transitions to the RESET state from the SAFE state when the SAFE state time-out timer expires. — If DEV_ERR_CNT[3:0] > SAFE_LOCK_TH[3:0], the device remains locked in the SAFE state.

SAFETY_CFG2 Register

SAFETY_CFG2 is shown in 図 11-47 and described in 表 11-34.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_CFG2)
Write (WR_SAFETY_CFG2). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-47. Safety Configuration 2 (SAFETY_CFG2) Register

7	6	5	4	3	2	1	0
CLK_WARN_RESP_EN	RESERVED	ABIST_SCHED_EN	AUTO_BIST_DIS	ABIST_ACTIVE_FAIL_RESP	ENDRV_ERR_RESP_EN	NRES_ERR_RST_EN	NRES_ERR_SAFE_EN
R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 11-34. SAFETY_CFG2 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	CLK_WARN_RESP_EN	R/W	0b	Enables and disables the device transition from the DIAGNOSTIC or ACTIVE state to the SAFE state when any digital clock monitor detects accuracy warning listed in the SAFETY_CLK_WARN_STAT register. 0b = Transition to the SAFE state disabled. 1b = Transition to the SAFE state enabled.
6	RESERVED	R	0b	Reserved
5	ABIST_SCHED_EN	R/W	0b	Enables and disables the ABIST scheduler in the ACTIVE state. 0b = ABIST scheduler is disabled in the ACTIVE state. 1b = ABIST scheduler is enabled when the device is in the ACTIVE state and if any of ABIST_GROUPx_START control bits in the SAFETY_ABIST_CTRL register is set.
4	AUTO_BIST_DIS	R/W	0b	Enables and disables automatic ABIST and LBIST run during NRES extension when the device enters the RESET state from one of the other operating states (DIAGNOSTIC, ACTIVE, or SAFE state). 0b = Automatic ABIST and LBIST enabled. 1b = Automatic ABIST and LBIST disabled.

表 11-34. SAFETY_CFG2 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
3	ABIST_ACTIVE_FAIL_RESP	R/W	0b	Enables and disables the device transition to the SAFE state from the DIAGNOSTIC or ACTIVE state when any of the ABIST fails. 0b = Transition to the SAFE state disabled. 1b = Transition to the SAFE state enabled.
2	ENDRV_ERR_RESP_EN	R/W	0b	Enables and disables the device transition to the SAFE state from the DIAGNOSTIC or ACTIVE state when the ENDRV/nIRQ driver error is detected. 0b = Transition to the SAFE state disabled. 1b = Transition to the SAFE state enabled.
1	NRES_ERR_RST_EN	R/W	0b	Enables and disables the device transition to the RESET state from the DIAGNOSTIC, ACTIVE, or SAFE state when the NRES driver error is detected. NOTE: If both the NRES_ERR_RST_EN and NRES_ERR_SAFE_EN bits are set, the NRES_ERR_RST_EN has priority. 0b = Transition to the RESET state disabled. 1b = Transition to the RESET state enabled.
0	NRES_ERR_SAFE_EN	R/W	0b	Enables and disables the device transition to the SAFE state from the DIAGNOSTIC or ACTIVE state when the NRES driver error is detected. 0b = Transition to the SAFE state disabled. 1b = Transition to the SAFE state enabled.

SAFETY_CFG3 Register

SAFETY_CFG3 is shown in 図 11-48 and described in 表 11-35.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_CFG3)
Write (WR_SAFETY_CFG3). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-48. Safety Configuration 3 (SAFETY_CFG3) Register

7	6	5	4	3	2	1	0
RESERVED	SSM_EN	RESERVED	SPI_CRC_CFG	WD_CFG	MCU_ESM_CFG	WD_RST_EN	MCU_ESM_RST_EN
R-0b	R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b

表 11-35. SAFETY_CFG3 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	RESERVED	R	0b	Reserved.
6	SSM_EN	R/W	0b	Enables and disables internal Adaptively Randomized Spread Spectrum (ARSS) modulation. 0b = Internal ARSS modulation is disabled. 1b = Internal ARSS modulation is enabled.
5	RESERVED	R	0b	Reserved.

表 11-35. SAFETY_CFG3 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
4	SPI_CRC_CFG	R/W	0b	Enables and disables CRC protection on SPI communication. 0b = SPI Frame CRC protection disabled. 1b = SPI Frame CRC protection enabled.
3	WD_CFG	R/W	0b	Watchdog mode configuration. NOTE: This bit is initialized when the device enters the RESET state. 0b = Q&A Configuration with total of 4 watchdog answers during watchdog cycle. 1b = Q&A Configuration with only single watchdog answer during the OPEN window.
2	MCU_ESM_CFG	R/W	0b	MCU Error signal monitor configuration. NOTE: This bit is initialized when the device enters the RESET state. 0b = MCU ERORR pin low condition monitor (TMS570 mode). 1b = PWM mode.
1	WD_RST_EN	R/W	1b	Enables the device transition either to the RESET state or to the SAFE state from the DIAGNOSTIC or ACTIVE state when WD_FAIL_CNT reaches WD_FC_RST_TH. NOTE: This bit is initialized when the device enters the RESET state. The bit is 'masked (but not cleared) when the device enters the SAFE state to prevent the device transition to the RESET state. 0b = The device transitions to the SAFE state. 1b = The device transitions to the RESET state.
0	MCU_ESM_RST_EN	R/W	0b	Enables the device transition either to the RESET state or to the SAFE state from the DIAGNOSTIC or ACTIVE state when MCU_ESM_FC reaches MCU_ESM_FC_RST_TH. NOTE: This bit is initialized when the device enters the RESET state. 0b = The device transitions to the SAFE state. 1b = The device transitions to the RESET state.

SAFETY_CFG4 Register

SAFETY_CFG4 is shown in 図 11-49 and described in 表 11-36.

Return to 表 11-23

Initialization source: NPOR, RESET
Controller access: Read (RD_SAFETY_CFG4)
Write (WR_SAFETY_CFG4). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-49. Safety Configuration 4 (SAFETY_CFG4) Register

7	6	5	4	3	2	1	0
MCU_ESM_FC_RST_TH				MCU_ESM_FC_ENDRV_TH			
R/W-1111b				R/W-1000b			

表 11-36. SAFETY_CFG4 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-4	MCU_ESM_FC_RST_TH	R/W	1111b	MCU_ESM_FC threshold at which the device transition to the RESET state when device is in the ACTIVE, DIAGNOSTIC, or SAFE state, if MCU_ESM_RST_EN = 1b. If MCU_ESM_RST_EN = 0b the device transition to the SAFE state at this threshold.
3-0	MCU_ESM_FC_ENDRV_TH	R/W	1000b	MCU_ESM_FC threshold at which the device transition to the SAFE state when device is in the ACTIVE state.

SAFETY_CFG5 Register

SAFETY_CFG5 is shown in 図 11-50 and described in 表 11-37.

Return to 表 11-23

Initialization source: NPOR, RESET, WD_CFG change
Controller access: Read (RD_SAFETY_CFG5)
Write (WR_SAFETY_CFG5). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-50. Safety Configuration 5 (SAFETY_CFG5) Register

7	6	5	4	3	2	1	0
WD_FC_RST_TH				WD_FC_ENDRV_TH			
R/W-1111b				R/W-0101b			

表 11-37. SAFETY_CFG5 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-4	WD_FC_RST_TH	R/W	1111b	WD_FAIL_CNT threshold at which the device sets the WD_RST_FAIL status bit and transitions either to the RESET state (when WD_RST_EN = 1b) or to the SAFE state (when WD_RST_EN = 0b).
3-0	WD_FC_ENDRV_TH	R/W	0101b	WD_FAIL_CNT threshold at which device sets the WD_ENDRV_FAIL status bit and drives the ENDRV/nIRQ output low. NOTE: No state transition to the SAFE state will occur.

SAFETY_CFG6 Register

SAFETY_CFG6 is shown in 図 11-51 and described in 表 11-38.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_CFG6)
Write (WR_SAFETY_CFG6). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-51. Safety Configuration 6 (SAFETY_CFG6) Register

7	6	5	4	3	2	1	0
RESERVED		BUCK1_SCG_OFF_EN	BUCK1_OVP_OFF_EN	BUCK1_LS_SINK_OVC_OFF_EN	RESERVED	BUCK1_PGND_LOSS_OFF_EN	BUCK1_OT_OFF_EN
R-00b		R/W-1b	R/W-1b	R/W-1b	R-0b	R/W-1b	R/W-1b

表 11-38. SAFETY_CFG6 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-6	RESERVED	R	00b	Reserved.
5	BUCK1_SCG_OFF_EN	R/W	1b	Enables device transition either to the OFF state or to the SAFE state when the BUCK1 short-circuit-to-ground event is detected. 0b = The device transitions to the SAFE state. 1b = The device transitions to the OFF state.
4	BUCK1_OVP_OFF_EN	R/W	1b	Enables device transition either to the OFF state or to the SAFE state when the BUCK1 overvoltage protection event is detected. 0b = The device transitions to the SAFE state. 1b = The device transitions to the OFF state.
3	BUCK1_LS_SINK_OVC_OFF_EN	R/W	1b	Enables device transition either to the OFF state or to the SAFE state when the BUCK1 LS sink overcurrent event is detected 0b = The device transitions to the SAFE state. 1b = The device transitions to the OFF state.
2	RESERVED	R	0b	Reserved.
1	BUCK1_PGND_LOSS_OFF_EN	R/W	1b	Enables device transition either to the OFF state or to the SAFE state when the BUCK1 loss-of-ground event is detected. 0b = The device transitions to the SAFE state. 1b = The device transitions to the OFF state.
0	BUCK1_OT_OFF_EN	R/W	1b	Enables device transition either to the OFF state or to the SAFE state when the BUCK1 die overtemperature event is detected. 0b = The device transitions to the SAFE state. 1b = The device transitions to the OFF state.

SAFETY_CFG8 Register

SAFETY_CFG8 is shown in 図 11-52 and described in 表 11-39.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_CFG8)
Write (WR_SAFETY_CFG8). Write access only in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-52. Safety Configuration 8 (SAFETY_CFG8) Register

7	6	5	4	3	2	1	0
ABIST_SCHED_DLY							
R/W-0001 0000b							

表 11-39. SAFETY_CFG8 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-0	ABIST_SCHED_DLY	R/W	0001 0000b	Programmable time interval between any two scheduled ABIST group of tests. Time interval, t_2, is multiple of programmed watchdog cycles per formula below: $t_2 = (ABIST\_SCHED\_DLY + 1) \times 256 \times (t_{WD\_WIN1} + t_{WD\_WIN2})$. The time delay between any two scheduled ABIST group of tests can be set in the range from 281.6 ms to 10380.9 s.

EXT_VMON1_CFG Register

EXT_VMON1_CFG is shown in 図 11-53 and described in 表 11-40.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_EXT_VMON1_CFG)
Write (WR_EXT_VMON1_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. - Protected by the DEV_CFG_CRC.

図 11-53. External VMON1 Configuration (EXT_VMON1_CFG) Register

7	6	5	4	3	2	1	0
RESERVED				EXT_VMON1_OV_IRQ_EN	EXT_VMON1_UV_IRQ_EN	EXT_VMON1_UV_RST_EN	EXT_VMON1_OV_RST_EN
R-0000b				R/W-0b	R/W-0b	R/W-Xb	R/W-0b

表 11-40. EXT_VMON1_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-4	RESERVED	R	0000b	Reserved
3	EXT_VMON1_OV_IRQ_EN	R/W	0b	Enables and disables device transition to the SAFE state when overvoltage event at EXT_VSENSE1 pin is detected. 0b = Transition to the SAFE state disabled. 1b = Transition to the SAFE state enabled.
2	EXT_VMON1_UV_IRQ_EN	R/W	0b	Enables and disables device transition to the SAFE state when undervoltage event at EXT_VSENSE1 pin is detected. 0b = Transition to the SAFE state disabled. 1b = Transition to the SAFE state enabled.
1	EXT_VMON1_UV_RST_EN	R/W	Xb	Enables and disables device transition to the RESET state when undervoltage event at EXT_VSENSE1 pin is detected. NOTE: If both the EXT_VMON1_UV_IRQ_EN and EXT_VMON1_UV_RST_EN bits are set, the EXT_VMON1_UV_RST_EN has priority. 0b = Transition to the RESET state disabled. 1b = Transition to the RESET state enabled. Default state of this bit controlled by EEPROM bit.
0	EXT_VMON1_OV_RST_EN	R/W	0b	Enables and disables device transition to the RESET state when overvoltage event at EXT_VSENSE1 pin is detected. NOTE: If both the EXT_VMON1_OV_IRQ_EN and EXT_VMON1_OV_RST_EN bits are set, the EXT_VMON1_OV_RST_EN has priority. 0b = Transition to the RESET state disabled. 1b = Transition to the RESET state enabled.

EXT_VMON2_CFG Register

EXT_VMON2_CFG is shown in 図 11-54 and described in 表 11-41.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_EXT_VMON2_CFG)
Write (WR_EXT_VMO2_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b.

図 11-54. External VMON2 Configuration (EXT_VMON2_CFG) Register

7	6	5	4	3	2	1	0
RESERVED				EXT_VMON2_OV_IRQ_EN	EXT_VMON2_UV_IRQ_EN	EXT_VMON2_UV_RST_EN	EXT_VMON2_OV_RST_EN
R-0000b				R/W-0b	R/W-0b	R/W-Xb	R/W-0b

表 11-41. EXT_VMON2_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-4	RESERVED	R	000b	Reserved
3	EXT_VMON2_OV_IRQ_EN	R/W	0b	Enables and disables device transition to the SAFE state when overvoltage event at EXT_VSENSE2 pin is detected. 0b = Transition to the SAFE state disabled. 1b = Transition to the SAFE state enabled.
2	EXT_VMON2_UV_IRQ_EN	R/W	0b	Enables and disables device transition to the SAFE state when undervoltage event at EXT_VSENSE2 pin is detected. 0b = Transition to the SAFE state disabled. 1b = Transition to the SAFE state enabled.
1	EXT_VMON2_UV_RST_EN	R/W	Xb	Enables and disables device transition to the RESET state when undervoltage event at EXT_VSENSE2 pin is detected. NOTE: If both the EXT_VMON2_UV_IRQ_EN and EXT_VMON2_UV_RST_EN bits are set, the EXT_VMON2_UV_RST_EN has priority. 0b = Transition to the RESET state disabled. 1b = Transition to the RESET state enabled. Default state of this bit controlled by EEPROM bit.
0	EXT_VMON2_OV_RST_EN	R/W	0b	Enables and disables device transition to the RESET state when overvoltage event at EXT_VSENSE1 pin is detected. NOTE: If both the EXT_VMON2_OV_IRQ_EN and EXT_VMON2OV_RST_EN bits are set, the EXT_VMON2_OV_RST_EN has priority. 0b = Transition to the RESET state disabled. 1b = Transition to the RESET state enabled.

PWR_CTRL Register

PWR_CTRL is shown in 図 11-55 and described in 表 11-42.

Return to 表 11-23

Initialization source: NPOR, RESET
Controller access: Read (RD_PWR_CTRL)
Write (WR_PWR_CTRL). Write access is only available when the CTRL_LOCK bit is set to 0b (DEV_STAT1.CTRL_LOCK bit).
NOTE:

- The BUCK1 is always enabled by default, and cannot be disabled through SPI mapped register. The enable or disable of the BUCK1 is controlled through WAKE input and WAKE_L latch under normal operating conditions.
- The BUCK1 can be disabled by the internal monitoring and protection circuit, and enabled again after its re-start conditions are met.

図 11-55. Power Control (PWR_CTRL) Register

7	6	5	4	3	2	1	0
RESERVED		EXT_VMON2_EN	EXT_VMON1_EN	BOOST_EN	RESERVED	BUCK2_EN	RESERVED
R-00b		R/W-Xb	R/W-Xb	R/W-1b	R-0b	R/W-1b	R-0b

表 11-42. PWR_CTRL Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-6	RESERVED	R	00b	Reserved.

表 11-42. PWR_CTRL Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
5	EXT_VMON2_EN	R/W-X	Xb	Enables and disables the external supply monitor at the EXT_VSENSE2 pin. This bit is NOT initialized when the device enters the RESET state. 0b = EXT VMON2 disabled. 1b = EXT VMON2 enabled.
4	EXT_VMON1_EN	R/W-X	Xb	Enables and disables the external supply monitor at the EXT_VSENSE1 pin. This bit is NOT initialized when the device enters the RESET state. 0b = EXT VMON1 disabled. 1b = EXT VMON1 enabled.
3	BOOST_EN	R/W	1b	Enables and disables the BOOST converter. This bit is also cleared to 0b when the BOOST is disabled due to a relevant fault event and when the device transitions to the SAFE state. 0b = The BOOST disabled. 1b = The BOOST enabled.
2	RESERVED	R/W	0b	Reserved
1	BUCK2_EN	R/W	1b	Enables and disables the BUCK2 regulator. This bit is also cleared to 0b when the BUCK2 is disabled due to a relevant fault event and when the device transitions to the SAFE state. 0b = The BUCK2 disabled. 1b = The BUCK2 enabled.
0	RESERVED	R/W	0b	Reserved.

CLK_MON_CTRL Register

CLK_MON_CTRL is shown in 図 11-56 and described in 表 11-43.

Return to 表 11-23

Initialization source: NPOR, RESET
Controller access: Read (RD_CLK_MON_CTRL)
Write (WR_CLK_MON_CTRL). Write access is only available when the CTRL_LOCK is set to 0b.

図 11-56. Clock Monitor Control Register (CLK_MON_CTRL) Register

7	6	5	4	3	2	1	0
RESERVED	DIG_CLK_MON 5_EN	RESERVED	DIG_CLK_MON 4_EN	DIG_CLK_MON 3_EN	DIG_CLK_MON 6_EN	DIG_CLK_MON 1_EN	RESERVED
R-0b	R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b	R/W-0b	R-0b

表 11-43. CLK_MON_CTRL Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	RESERVED	R	0b	Reserved.
6	DIG_CLK_MON5_EN		1b	Enables and disables the DIG_CLK_MON5 for the BOOST converter switching clock. 0b = Clock monitor is disabled. 1b = Clock monitor is enabled.
5	RESERVED	R	0b	Reserved.

表 11-43. CLK_MON_CTRL Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
4	DIG_CLK_MON4_EN	R/W	1b	Enables and disables the DIG_CLK_MON4 for the BUCK2 regulator switching clock. 0b = Clock monitor is disabled. 1b = Clock monitor is enabled.
3	DIG_CLK_MON3_EN	R/W	1b	Enables and disables the DIG_CLK_MON3 for the BUCK1 regulator switching clock. 0b = Clock monitor is disabled. 1b = Clock monitor is enabled.
2	DIG_CLK_MON6_EN	R/W	1b	Enables and disables the DIG_CLK_MON6 for clock source (PLL or MODCLK) for the switching regulators. 0b = Clock monitor is disabled. 1b = Clock monitor is enabled.
1	DIG_CLK_MON1_EN	R/W	0b	Enables and disables the DIG_CLK_MON1 for external clock at the SYNC_IN pin for synchronization. 0b = Clock monitor is disabled. 1b = Clock monitor is enabled.
0	RESERVED	R	0b	Reserved.

VMON_UV_STAT Register

VMON_UV_STAT is shown in 図 11-57 and described in 表 11-44.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_VMON_UV_STAT)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-57. VMON Undervoltage Status (VMON_UV_STAT) Register

7	6	5	4	3	2	1	0
RESERVED	VIN_BAD	RESERVED	VREG_UV	BOOST_UV	RESERVED	BUCK2_UV	BUCK1_UV
R-0b	RC-0b	R-0b	RC-0b	RC-0b	R-0b	RC-0b	RC-0b

表 11-44. VMON_UV_STAT Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	RESERVED	R	0b	Reserved.
6	VIN_BAD	RC	0b	VIN undervoltage error flag. 0b = No undervoltage. 1b = Undervoltage.
5	RESERVED	R	0b	Reserved.
4	VREG_UV	RC	0b	VREG undervoltage error flag. 0b = No undervoltage. 1b = Undervoltage.
3	BOOST_UV	RC	0b	BOOST undervoltage error flag. 0b = No undervoltage. 1b = Undervoltage.

表 11-44. VMON_UV_STAT Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
2	RESERVED	R	0b	Reserved.
1	BUCK2_UV	RC	0b	BUCK2 undervoltage error flag. 0b = No undervoltage. 1b = Undervoltage.
0	BUCK1_UV	RC	0b	BUCK1 undervoltage error flag. 0b = No undervoltage. 1b = Undervoltage.

VMON_OV_STAT Register

VMON_OV_STAT is shown in 図 11-58 and described in 表 11-45.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_VMON_OV_STAT)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-58. VMON Overvoltage Status (VMON_OV_STAT) Register

7	6	5	4	3	2	1	0
VIO_OV	VIN_OV	RESERVED	VREG_OV	BOOST_OV	RESERVED	BUCK2_OV	BUCK1_OV
RC-0b	RC-0b	R-0b	RC-0b	RC-0b	R-0b	RC-0b	RC-0b

表 11-45. VMON_OV_STAT Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	VIO_OV	RC	0b	VIO overvoltage error flag. 0b = No overvoltage. 1b = Overvoltage.
6	VIN_OV	RC	0b	VIN overvoltage error flag. NOTE: Identical to the VIN_OV bit in the OFF_STATE_L_STAT register. 0b = No overvoltage. 1b = Overvoltage.
5	RESERVED	R	0b	Reserved
4	VREG_OV	RC	0b	VREG overvoltage error flag 0b = No overvoltage. 1b = Overvoltage.
3	BOOST_OV	RC	0b	BOOST overvoltage error flag 0b = No overvoltage. 1b = Overvoltage.
2	RESERVED	R	0b	Reserved
1	BUCK2_OV	RC	0b	BUCK2 overvoltage error flag 0b = No overvoltage. 1b = Overvoltage.

表 11-45. VMON_OV_STAT Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
0	BUCK1_OV	RC	0b	BUCK1 overvoltage error flag 0b = No overvoltage. 1b = Overvoltage.

EXT_VMON_STAT Register

EXT_VMON_STAT is shown in 図 11-59 and described in 表 11-46.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_EXT_VMON_STAT)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.
- EXT VMON UV/OV monitoring is active only when EXT VMON-s is enabled. When EXT VMON-s are disabled UV/OV monitoring is masked.

図 11-59. External VMON Status (EXT_VMON_STAT) Register

7	6	5	4	3	2	1	0
RESERVED		EXT_VMON2_OV	EXT_VMON2_UV	RESERVED		EXT_VMON1_OV	EXT_VMON1_UV
R-00b		RC-0b	RC-0b	R-00b		RC-0b	RC-0b

表 11-46. EXT_VMON_STATC Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-6	RESERVED	R	00b	Reserved.
5	EXT_VMON2_OV	RC	0b	EXT VMON2 overvoltage error flag. 0b = No overvoltage. 1b = Overvoltage.
4	EXT_VMON2_UV	RC	0b	EXT VMON2 undervoltage error flag. 0b = No undervoltage. 1b = Undervoltage.
3-2	RESERVED	R	00b	Reserved.
1	EXT_VMON1_OV	RC	0b	EXT VMON1 overvoltage error flag. 0b = No overvoltage. 1b = Overvoltage.
0	EXT_VMON1_UV	RC	0b	EXT VMON1 undervoltage error flag. 0b = No undervoltage. 1b = Undervoltage.

SAFETY_BUCK1_STAT1 Register

SAFETY_BUCK1_STAT1 is shown in 図 11-60 and described in 表 11-47.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_BUCK1_STAT1)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-60. Safety BUCK1 Status 1 (SAFETY_BUCK1_STAT1) Register

7	6	5	4	3	2	1	0
RESERVED		BUCK1_EOVP	BUCK1_PGND_LOSS	BUCK1_OVP	BUCK1_LS_SINK_OVC	BUCK1_LS_OVC	BUCK1_SCG
R-00b		RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-47. SAFETY_BUCK1_STAT1 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-6	RESERVED	R	00b	Reserved.
5	BUCK1_EOVP	RC	0b	BUCK1 extreme overvoltage protection status flag. 0b = No extreme overvoltage protection. 1b = Extreme overvoltage protection.
4	BUCK1_PGND_LOSS	RC	0b	BUCK1 Loss of PGND status flag. 0b = No BUCK1 Loss-of-PGND. 1b = BUCK1 Loss-of-GND.
3	BUCK1_OVP	RC	0b	BUCK1 overvoltage protection status flag. 0b = No overvoltage protection. 1b = Overvoltage protection.
2	BUCK1_LS_SINK_OVC	RC	0b	BUCK1 LS sink current limit error flag. 0b = No BUCK1 LS sink current limit. 1b = BUCK1 LS sink current limit.
1	BUCK1_OVC	RC	0b	BUCK1 overload error flag. 0b = No overload condition. 1b = Overload condition.
0	BUCK1_SCG	RC	0b	BUCK1 short-circuit to ground error flag. 0b = No short-circuit condition. 1b = Short-circuit condition.

SAFETY_BUCK1_STAT2 Register

SAFETY_BUCK1_STAT2 is shown in 図 11-61 and described in 表 11-48.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_BUCK1_STAT2)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-61. Safety BUCK1 Status 2 (SAFETY_BUCK1_STAT2) Register

7	6	5	4	3	2	1	0
RESERVED						BUCK1_OT_STD	BUCK1_OT_WARN

図 11-61. Safety BUCK1 Status 2 (SAFETY_BUCK1_STAT2) Register (続き)

R-000000b	RC-0b	RC-0b

表 11-48. SAFETY_BUCK1_STAT2 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-2	RESERVED	R	000000b	Reserved.
1	BUCK1_OT_STD	RC	0b	BUCK1 overtemperature shutdown flag. 0b = No overtemperature shutdown. 1b = Overtemperature shutdown.
0	BUCK1_OT_WARN	RC	0b	BUCK1 overtemperature warning flag. 0b = No overtemperature warning. 1b = Overtemperature warning.

SAFETY_BUCK2_STAT1 Register

SAFETY_BUCK2_STAT1 is shown in 図 11-62 and described in 表 11-49.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_BUCK2_STAT1)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-62. Safety BUCK2 Status 1 (SAFETY_BUCK2_STAT1) Register

7	6	5	4	3	2	1	0
RESERVED			BUCK2_PGND_LOSS	BUCK2_OVP	BUCK2_LS_SINK_OVC	BUCK2_LS_OVC	BUCK2_SCG
R-000b			RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-49. SAFETY_BUCK2_STAT1 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-5	RESERVED	R	000b	Reserved.
4	BUCK2_PGND_LOSS	RC	0b	BUCK2 Loss of PGND status flag. 0b = No BUCK2 Loss-of-PGND. 1b = BUCK2 Loss-of-GND.
3	BUCK2_OVP	RC	0b	BUCK2 overvoltage protection status flag. 0b = No overvoltage protection. 1b = Overvoltage protection.
2	BUCK2_LS_SINK_OVC	RC	0b	BUCK2 LS sink current limit error flag. 0b = No BUCK2 LS sink current limit. 1b = BUCK2 LS sink current limit.
1	BUCK2_LS_OVC	RC	0b	BUCK2 overload error flag. 0b = No overload condition. 1b = Overload condition.
0	BUCK2_SCG	RC	0b	BUCK2 short-circuit to ground error flag. 0b = No short-circuit condition. 1b = Short-circuit condition.

SAFETY_BUCK2_STAT2 Register

SAFETY_BUCK2_STAT2 is shown in 図 11-63 and described in 表 11-50.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_BUCK2_STAT2)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-63. Safety BUCK2 Status 2 (SAFETY_BUCK2_STAT2) Register

7	6	5	4	3	2	1	0
RESERVED						BUCK2_OT_STD	BUCK2_OT_WARN
R-000000b						RC-0b	RC-0b

表 11-50. SAFETY_BUCK2_STAT2 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-2	RESERVED	R	000000b	Reserved.
1	BUCK2_OT_STD	RC	0b	BUCK2 overtemperature shutdown flag. 0b = No overtemperature shutdown. 1b = Overtemperature shutdown.
0	BUCK2_OT_WARN	RC	0b	BUCK2 overtemperature warning flag. 0b = No overtemperature warning. 1b = Overtemperature warning.

SAFETY_BOOST_STAT1 Register

SAFETY_BOOST_STAT1 is shown in and described in 図 11-64 and described in 表 11-51.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_BOOST_STAT1)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-64. Safety BOOST Status 1 (SAFETY_BOOST_STAT1) Register

7	6	5	4	3	2	1	0
RESERVED			BOOST_PGND_LOSS	BOOST_OVP	BOOST_HS_SINK_OVC	BOOST_HS_OVC	BOOST_SCG
R-000b			RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-51. SAFETY_BOOST_STAT1 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-5	RESERVED	R	000b	Reserved
4	BOOST_PGND_LOSS	RC	0b	BOOST Loss of PGND status flag. 0b = No BOOST Loss-of-PGND. 1b = BOOST Loss-of-GND.

表 11-51. SAFETY_BOOST_STAT1 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
3	BOOST_OVP	RC	0b	BOOST overvoltage protection status flag. 0b = No overvoltage protection. 1b = Overvoltage protection.
2	BOOST_HS_SINK_OVC	RC	0b	BOOST HS sink current limit error flag. 0b = No BOOST HS sink current limit. 1b = BOOST HS sink current limit.
1	BOOST_HS_OVC	RC	0b	BOOST overload error flag. 0b = No overload condition. 1b = Overload condition.
0	BOOST_SCG	RC	0b	BOOST short-circuit to ground error flag. 0b = No short-circuit condition. 1b = Short-circuit condition.

SAFETY_BOOST_STAT2 Register

SAFETY_BOOST_STAT2 is shown in and described in 図 11-65 and described in 表 11-52.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_ BOOST _STAT2)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-65. Safety BOOST Status 2 (SAFETY_BOOST_STAT2) Register

7	6	5	4	3	2	1	0
RESERVED						BOOST_OT_STD	BOOST_OT_WARN
R-000000b						RC-0b	RC-0b

表 11-52. SAFETY_BOOST_STAT2 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-2	RESERVED	R	000000b	Reserved.
1	BOOST_OT_STD	RC	0b	BOOST overtemperature shutdown flag. 0b = No overtemperature shutdown. 1b = Overtemperature shutdown.
0	BOOST_OT_WARN	RC	0b	BOOST overtemperature warning flag. 0b = No overtemperature warning. 1b = Overtemperature warning.

SAFETY_ERR_STAT1 Register

SAFETY_ERR_STAT1 is shown in and described in 図 11-66 and described in 表 11-53.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_ERR_STAT1)

Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-66. Safety Error Status 1 (SAFETY_ERR_STAT1) Register

7	6	5	4	3	2	1	0
RESERVED		DEV_CFG_CRC_ERR	EE_CRC_ERR	NRES_ERR	ENDRV_nIRQ_DRV_ERR	SPI_ERR[1:0]	
R-00b		RC-0b	RC-0b	RC-0b	RC-0b	RC-00b	

表 11-53. SAFETY_ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-6	RESERVED	R	00b	Reserved.
5	DEV_CFG_CRC_ERR	RC	0b	CRC error flag for the device configuration registers. This bit is set to 1b when calculated CRC8 value for device-configuration registers does not match expected CRC8 value stored in the SAFETY_DEV_CFG_CRC register. 0b = No CRC error. 1b = CRC error.
4	EE_CRC_ERR	RC	0b	CRC error flag for EEPROM registers. This bit is set to 1b when calculated CRC8 value for EEPROM registers does not match internally programmed CRC8 value. 0b = No CRC error. 1b = CRC error.
3	NRES_ERR	RC	0b	The NRES driver read-back error flag. 0b = No read-back error. 1b = Read-back error.
2	ENDRV_nIRQ_DRV_ERR	RC	0b	The ENDRV/nIRQ driver read-back error flag. 0b = No read-back error. 1b = Read-back error.
1-0	SPI_ERR[1:0]	RC	00b	SPI Error flags. NOTE: if a reset to the MCU is asserted during a SPI frame transfer (causing a truncated SPI frame), these SPI Error Status bits will not be cleared, but will keep the status according to the truncated previous SPI frame until SPI Read access to this register. 00b = No error. 01b = Command error. 10b = Format error (received bit count not equal to 24 or 16). 11b = Data output mismatch.

SAFETY_CLK_STAT Register

SAFETY_CLK_STAT is shown in and described in 図 11-67 and described in 表 11-54.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_CLK_STAT)
Note:

- A logic high is latched until the register is read.

- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-67. Safety Clock Status (SAFETY_CLK_STAT) Register

7	6	5	4	3	2	1	0
SYSCLK_ERR	BOOST_FSW_CLK_ERR	RESERVED	BUCK2_FSW_CLK_ERR	BUCK1_FSW_CLK_ERR	SYNC_CLK_ERR	SMPS_SRC_CLK_ERR	DIG_SYSCLK_ERR
RC-0b	RC-0b	R-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-54. SAFETY_CLK_STAT Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	SYSCLK_ERR	RC	0b	8-MHz system clock error flag from either the analog clock monitor or the digital clock monitor. NOTE: This bit is a replica of bit 2 in OFF_STATE_L_STAT register, and is cleared after read access to this register. 0b = No System Clock error. 1b = System Clock error.
6	BOOST_FSW_CLK_ERR	RC	0b	Clock error flag from DIG_CLK_MON5 for BOOST switching clock. 0b = No clock error. 1b = Clock error.
5	RESERVED	R	0b	Reserved.
4	BUCK2_FSW_CLK_ERR	RC	0b	Clock error flag from DIG_CLK_MON4 for BUCK2 switching clock. 0b = No clock error. 1b = Clock error.
3	BUCK1_FSW_CLK_ERR	RC	0b	Clock error flag from DIG_CLK_MON3 for BUCK1 switching clock . 0b = No clock error. 1b = Clock error.
2	SYNC_CLK_ERR	RC	0b	Clock error flag from DIG_CLK_MON1 for SYNC_IN clock input. 0b = No clock error. 1b = Clock error.
1	SMPS_SRC_CLK_ERR	RC	0b	Clock error flag from DIG_CLK_MON6 for either PLL clock output or MODCLK output. 0b = No clock error. 1b = Clock error.
0	DIG_SYSCLK_ERR	RC	0b	DIG_SYSCLK_ERR error / fault reaction by the device state machine is masked/ disabled in device EEPROM and this has no impact to device overall functionality. Ignore, if this bit is set.

SAFETY_CLK_WARN_STAT Register

SAFETY_CLK_WARN_STAT is shown in and described in 図 11-68 and described in 表 11-55.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_CLK_WARN_STAT)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-68. Safety Clock Warning Status (SAFETY_CLK_WARN_STAT) Register

7	6	5	4	3	2	1	0
RESERVED	BOOST_FSW_CLK_WARN	RESERVED	BUCK2_FSW_CLK_WARN	BUCK1_FSW_CLK_WARN	SYNC_CLK_WARN	SMPS_SRC_CLK_WARN	RESERVED
R-0b	RC-0b	R-0b	RC-0b	RC-0b	RC-0b	RC-0b	R-0b

表 11-55. SAFETY_CLK_WARN_STAT Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	RESERVED	R	0b	Reserved.
6	BOOST_FSW_CLK_WARN	RC	0b	Clock accuracy warning flag from DIG_CLK_MON5 for BOOST switching clock. 0b = No clock warning. 1b = Clock warning.
5	RESERVED	R	0b	Reserved
4	BUCK2_FSW_CLK_WARN	RC	0b	Clock accuracy warning flag from DIG_CLK_MON4 for BUCK2 switching clock. 0b = No clock warning. 1b = Clock warning.
3	BUCK1_FSW_CLK_WARN	RC	0b	Clock accuracy warning flag from DIG_CLK_MON3 for BUCK1 switching clock. 0b = No clock warning. 1b = Clock warning.
2	SYNC_CLK_WARN	RC	0b	Clock accuracy warning flag from DIG_CLK_MON1 for SYNC_IN clock. 0b = No clock warning. 1b = Clock warning.
1	SMPS_SRC_CLK_WARN	RC	0b	Clock accuracy warning flag from DIG_CLK_MON6 for either PLL clock output or MODCLK output. 0b = No clock warning. 1b = Clock warning.
0	RESERVED	R	0b	Reserved.

SAFETY_ABIST_ERR_STAT1 Register

SAFETY_ABIST_ERR_STAT1 is shown in and described in 図 11-69 and described in 表 11-56.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_ABIST_ERR_STAT1)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-69. Safety ABIST Error Status 1 (SAFETY_ABIST_ERR_STAT1) Register

7	6	5	4	3	2	1	0
ABIST_GROUP4_ERR	ABIST_GROUP3_ERR	ABIST_GROUP2_ERR	ABIST_GROUP1_ERR	ABIST_GROUP4_DONE	ABIST_GROUP3_DONE	ABIST_GROUP2_DONE	ABIST_GROUP1_DONE
RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-56. SAFETY_ABIST_ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	ABIST_GROUP4_ERR	RC	0b	ABIST Group 4 error flag. 0b = No ABIST Group 4 error. 1b = ABIST Group 4 error.
6	ABIST_GROUP3_ERR	RC	0b	ABIST Group 3 error flag. 0b = No ABIST Group 3 error. 1b = ABIST Group 3 error.
5	ABIST_GROUP2_ERR	RC	0b	ABIST Group 2 error flag. 0b = No ABIST Group 2 error. 1b = ABIST Group 2 error.
4	ABIST_GROUP1_ERR	RC	0b	ABIST Group 1 error flag. 0b = No ABIST Group 1 error. 1b = ABIST Group 1 error.
3	ABIST_GROUP4_DONE	RC	0b	ABIST Group 4 completion status flag. 0b = ABIST Group 4 is not completed. 1b = ABIST Group 4 is completed.
2	ABIST_GROUP3_DONE	RC	0b	ABIST Group 3 completion status flag. 0b = ABIST Group 3 is not completed. 1b = ABIST Group 3 is completed.
1	ABIST_GROUP2_DONE	RC	0b	ABIST Group 2 completion status flag. 0b = ABIST Group 2 is not completed. 1b = ABIST Group 2 is completed.
0	ABIST_GROUP1_DONE	RC	0b	ABIST Group 1 completion status flag. 0b = ABIST Group 1 is not completed. 1b = ABIST Group 1 is completed.

SAFETY_ABIST_ERR_STAT2 Register

SAFETY_ABIST_ERR_STAT2 is shown in and described in 図 11-70 and described in 表 11-57.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_ABIST_ERR_STAT2)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-70. Safety ABIST Error Status 2 (SAFETY_ABIST_ERR_STAT2) Register

7	6	5	4	3	2	1	0
ABIST_VREG_UV_ERR	RESERVED	ABIST_EXTVMON2_UV_ERR	ABIST_EXTVMON1_UV_ERR	ABIST_BOOST_UV_ERR	RESERVED	ABIST_BUCK2_UV_ERR	ABIST_BUCK1_UV_ERR
RC-0b	R-0b	RC-0b	RC-0b	RC-0b	R-0b	RC-0b	RC-0b

表 11-57. SAFETY_ABIST_ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	ABIST_VREG_UV_ERR	RC	0b	ABIST on VREG UV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
6	RESERVED	R	0b	Reserved.
5	ABIST_EXTVMON2_UV_ERR	RC	0b	ABIST on EXT VMON2 UV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
4	ABIST_EXTVMON1_UV_ERR	RC	0b	ABIST on EXT VMON1 UV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
3	ABIST_BOOST_UV_ERR	RC	0b	ABIST on BOOST UV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
2	RESERVED	R	0b	Reserved.
1	ABIST_BUCK2_UV_ERR	RC	0b	ABIST on BUCK2 UV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
0	ABIST_BUCK1_UV_ERR	RC	0b	ABIST on BUCK2 UV comparator error flag. 0b = No ABIST error. 1b = ABIST error.

SAFETY_ABIST_ERR_STAT3 Register

SAFETY_ABIST_ERR_STAT3 is shown in and described in 図 11-71 and described in 表 11-58.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_ABIST_ERR_STAT3)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-71. Safety ABIST Error Status 3 (SAFETY_ABIST_ERR_STAT3) Register

7	6	5	4	3	2	1	0
ABIST_VREG_OV_ERR	RESERVED	ABIST_EXTVMON2_OV_ERR	ABIST_EXTVMON1_OV_ERR	ABIST_BOOST_OV_ERR	RESERVED	ABIST_BUCK2_OV_ERR	ABIST_BUCK1_OV_ERR
RC-0b	R-0b	RC-0b	RC-0b	RC-0b	R-0b	RC-0b	RC-0b

表 11-58. SAFETY_ABIST_ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	ABIST_VREG_OV_ERR	RC	0b	ABIST on VREG OV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
6	RESERVED	R	0b	Reserved.

表 11-58. SAFETY_ABIST_ERR_STAT3 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
5	ABIST_EXTVMON2_OV_ERR	RC	0b	ABIST on EXT VMON2 OV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
4	ABIST_EXTVMON1_OV_ERR	RC	0b	ABIST on EXT VMON1 OV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
3	ABIST_BOOST_OV_ERR	RC	0b	ABIST on BOOST OV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
2	RESERVED	R	0b	Reserved.
1	ABIST_BUCK2_OV_ERR	RC	0b	ABIST on BUCK2 OV comparator error flag. 0b = No ABIST error. 1b = ABIST error.
0	ABIST_BUCK1_OV_ERR	RC	0b	ABIST on BUCK1 OV comparator error flag. 0b = No ABIST error. 1b = ABIST error.

SAFETY_ABIST_ERR_STAT4 Register

SAFETY_ABIST_ERR_STAT4 is shown in and described in 図 11-72 and described in 表 11-59.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_ABIST_ERR_STAT4)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-72. Safety ABIST Error Status 4 (SAFETY_ABIST_ERR_STAT4) Register

7	6	5	4	3	2	1	0
ABIST_BOOST_CL_ERR	RESERVED	ABIST_BUCK2_CL_ERR	ABIST_BUCK1_CL_ERR	ABIST_BOOST_OVP_ERR	RESERVED	ABIST_BUCK2_OVP_ERR	ABIST_BUCK1_OVP_ERR
RC-0b	R-0b	RC-0b	RC-0b	RC-0b	R-0b	RC-0b	RC-0b

表 11-59. SAFETY_ABIST_ERR_STAT4 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	ABIST_BOOST_CL_ERR	RC	0b	ABIST on BOOST current limit comparator error flag. 0b = No ABIST error. 1b = ABIST error.
6	RESERVED	R	0b	Reserved.
5	ABIST_BUCK2_CL_ERR	RC	0b	ABIST on BUCK2 current limit comparator error flag. 0b = No ABIST error. 1b = ABIST error.

表 11-59. SAFETY_ABIST_ERR_STAT4 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
4	ABIST_BUCK1_CL_ERR	RC	0b	ABIST on BUCK1 current limit comparator error flag. 0b = No ABIST error. 1b = ABIST error.
3	ABIST_BOOST_OVP_ERR	RC	0b	ABIST on BOOST OVP comparator error flag. 0b = No ABIST error. 1b = ABIST error.
2	RESERVED	R	0b	Reserved.
1	ABIST_BUCK2_OVP_ERR	RC	0b	ABIST on BUCK2 OVP comparator error flag. 0b = No ABIST error. 1b = ABIST error.
0	ABIST_BUCK1_OVP_ERR	RC	0b	ABIST on BUCK1 OVP comparator error flag. 0b = No ABIST error. 1b = ABIST error.

SAFETY_ABIST_ERR_STAT5 Register

SAFETY_ABIST_ERR_STAT5 is shown in and described in 図 11-73 and described in 表 11-60.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_ABIST_ERR_STAT5)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-73. Safety ABIST Error Status 5 (SAFETY_ABIST_ERR_STAT5) Register

7	6	5	4	3	2	1	0
RESERVED			ABIST_EE_CRC_MON_ERR	ABIST_BOOST_OT_ERR	RESERVED	ABIST_BUCK2_OT_ERR	ABIST_BUCK1_OT_ERR
R-000b			RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-60. SAFETY_ABIST_ERR_STAT5 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-5	RESERVED	R	000b	Reserved.
4	ABIST_EE_CRC_MON_ERR	RC	0b	ABIST on EEPROM CRC monitor error. 0b = No ABIST error. 1b = ABIST error.
3	ABIST_BOOST_OT_ERR	RC	0b	ABIST on BOOST OT monitor error. 0b = No ABIST error. 1b = ABIST error.
2	RESERVED	R	0b	Reserved.
1	ABIST_BUCK2_OT_ERR	RC	0b	ABIST on BUCK2 OT monitor error. 0b = No ABIST error. 1b = ABIST error.

表 11-60. SAFETY_ABIST_ERR_STAT5 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
0	ABIST_BUCK1_OT_ERR	RC	0b	ABIST BUCK1 OT monitor error. 0b = No ABIST error. 1b = ABIST error.

SAFETY_ABIST_ERR_STAT6 Register

SAFETY_ABIST_ERR_STAT6 is shown in and described in 図 11-74 and described in 表 11-61.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_ABIST_ERR_STAT6)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-74. Safety ABIST Error Status 6 (SAFETY_ABIST_ERR_STAT6) Register

7	6	5	4	3	2	1	0
RESERVED	ABIST_DSYSCLK_MON_ERR	ABIST_FSW3_CLK_MON_ERR	ABIST_FSW2_CLK_MON_ERR	ABIST_FSW1_CLK_MON_ERR	ABIST_PLL_CLK_MON_ERR	ABIST_SYNC_CLK_MON_ERR	ABIST_ACLK_MON_ERR
R-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-61. SAFETY_ABIST_ERR_STAT6 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	Reserved	R	0b	Reserved.
6	ABIST_DSYSCLK_MON_ERR	RC	0b	ABIST on digital system clock monitor (DIG_CLK_MON2) error. 0b = No ABIST error. 1b = ABIST error.
5	ABIST_FSW3_CLK_MON_ERR	RC	0b	ABIST on BOOST switching clock monitor (DIG_CLK_MON5) error. 0b = No ABIST error. 1b = ABIST error.
4	ABIST_FSW2_CLK_MON_ERR	RC	0b	ABIST on BUCK2 switching clock monitor (DIG_CLK_MON4) error. 0b = No ABIST error. 1b = ABIST error.
3	ABIST_FSW1_CLK_MON_ERR	RC	0b	ABIST on BUCK1 switching clock monitor (DIG_CLK_MON3) error. 0b = No ABIST error. 1b = ABIST error.
2	ABIST_PLL_CLK_MON_ERR	RC	0b	ABIST on the SMPS source clock monitor (DIG_CLK_MON6) error. 0b = No ABIST error. 1b = ABIST error.
1	ABIST_SYNC_CLK_MON_ERR	RC	0b	ABIST on SYNC_IN input clock monitor (DIG_CLK_MON1) error. 0b = No ABIST error. 1b = ABIST error.

表 11-61. SAFETY_ABIST_ERR_STAT6 Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
0	ABIST_ACLK_MON_ERR	RC	0b	ABIST on analog system clock monitor error. 0b = No ABIST error. 1b = ABIST error.

SAFETY_LBIST_ERR_STAT Register

SAFETY_LBIST_ERR_STAT is shown in and described in 図 11-75 and described in 表 11-62.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_LBIST_ERR_STAT)
Note: A

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.
- The Watchdog, NRES supervisor, MCU error signal monitoring diagnostics are covered by LBIST core test.

図 11-75. Safety LBIST Error Status (SAFETY_LBIST_ERR_STAT) Register

7	6	5	4	3	2	1	0
RESERVED	DEV_CFG_CRC_DIAG_ERR	EE_CRC_DIAG_ERR	NRES_ERR_DIAG_ERR	ENDRV/nIRQ_DIAG_ERR	LBIST_DIAG_ERR	LBIST_CORE_ERR	LBIST_DONE
R-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-62. SAFETY_LBIST_ERR_STAT Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	RESERVED	R	0b	Reserved.
6	DEV_CFG_CRC_DIAG_ERR	RC	0b	Device configuration register CRC8 diagnostic error flag. 0b = No diagnostic error. 1b = Diagnostic error.
5	EE_CRC_DIAG_ERR	RC	0b	EEPROM CRC8 diagnostic error flag. 0b = No diagnostic error. 1b = Diagnostic error.
4	NRES_ERR_DIAG_ERR	RC	0b	NRES error monitor diagnostic error flag. 0b = No diagnostic error. 1b = Diagnostic error.
3	ENDRV/nIRQ_DIAG_ERR	RC	0b	ENDRV/nIRQ diagnostic error flag. 0b = No diagnostic error. 1b = Diagnostic error.
2	LBIST_DIAG_ERR	RC	0b	LBIST diagnostic run error. 0b = No diagnostic error. 1b = Diagnostic error.
1	LBIST_CORE_ERR	RC	0b	LBIST core error flag. 0b = No LBIST core error. 1b = LBIST core error.

表 11-62. SAFETY_LBIST_ERR_STAT Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
0	LBIST_DONE	RC	0b	LBIST completion status flag. 0b = LBIST not completed. 1b = LBIST completed.

SAFETY_ERR_STAT2 Register

SAFETY_ERR_STAT2 is shown in and described in 図 11-76 and described in 表 11-63.

Return to 表 11-23

Initialization source: NPOR, RESET, SPI RD Access, LBIST run, WD_CFG change
Controller access: Read (RD_SAFETY_ERR_STAT2)
Write (WR_WD_FC) for the WD_FAIL_CNT bits write access only. The write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b.
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-76. Safety Error Status 2 (SAFETY_ERR_STAT2) Register

7	6	5	4	3	2	1	0
RESERVED	WD_RST_FAIL	WD_ENDRV_FAIL	WD_FAIL	WD_FAIL_CNT[3:0]			
R-0b	RC-0b	RC-1b	RC-0b	R/W-X			

表 11-63. SAFETY_ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	RESERVED	R	0b	Reserved.
6	WD_RST_FAIL	RC	0b	Watchdog reset failure flag. NOTE: This flag bit is not cleared by RESET event so that MCU can confirm that previous system reset was caused by watchdog failure as the device enters the DIAGNOSTIC state. This bit will get set regardless of WD_RST_EN bit setting. 0b = WD_FAIL_CNT < WD_FC_RST_TH 1b = WD_FAIL_CNT ≥ WD_FC_RST_TH
5	WD_ENDRV_FAIL	RC	1b	Watchdog ENDRV failure flag. 0b = WD_FAIL_CNT < WD_FC_ENDRV_TH 1b = WD_FAIL_CNT ≥ WD_FC_ ENDRV_TH
4	WD_FAIL	RC	0b	Watchdog failure flag that is set each time watchdog 'bad event' occurs, accompanied by the WD_FAIL_CNT increment. 0b = No watchdog failure. 1b = Watchdog failure.
3-0	WD_FAIL_CNT[3:0]	R/W	X	State of the watchdog failure counter. NOTE: The default value (X) is set by the WD_FC_ENDRV_TH[3:0] bits.

SAFETY_ERR_STAT3 Register

SAFETY_ERR_STAT3 is shown in and described in 図 11-77 and described in 表 11-64.

Return to 表 11-23

Initialization source: NPOR, REST, SPI RD Access, LBIST run, MCU_ESM_CFG bit change
Controller access: Read (RD_SAFETY_ERR_STAT3)
Write (WR_MCU_ESM_FC). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Write access only for the MCU_ESM_FC bits.
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-77. Safety Error Status 3 (SAFETY_ERR_STAT3) Register

7	6	5	4	3	2	1	0
RESERVED	MCU_ESM_RST_FAIL	MCU_ESM_ENDRV_FAIL	MCU_ESM_FAIL	MCU_ESM_FC[3:0]			
R-0b	RC-0b	RC-0b	RC-0b	R/W-0101b			

表 11-64. SAFETY_ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	RESERVED	R	0b	Reserved.
6	MCU_ESM_RST_FAIL	RC	0b	MCU ESM error flag. 0b = WD_FAIL_CNT < WD_FC_ENDRV_TH 1b = MCU_ESM_FC ≥ MCU_ESM_FC_RST_TH
5	MCU_ESM_ENDRV_FAIL	RC	0b	MCU ESM error flag. 0b = MCU_ESM_FC < MCU_ESM_FC_ENDRV_TH 1b = MCU_ESM_FC ≥ MCU_ESM_FC_ENDRV_TH
4	MCU_ESM_FAIL	RC	0b	MCU ESM failure flag that is set each time the ESM detects a failure, accompanied by the MCU_ESM_FC increment. 0b = No MCU ESM failure. 1b = MCU ESM failure detected.
3-0	MCU_ESM_FC[3:0]	R/W	0101b	State of the MCU ESM failure counter. - The default value is 5, and is initialized to this value upon entering the RESET state, DIAGNOSTIC State, after LBIST completion, anytime MCU_ESM_CFG bit toggles (when changing MCU ESM configuration mode) and after MCU_ESM_EN bit (bit D2 in SAFETY_CHECK_CTRL register) toggles from 0 to 1. - The MCU_ESM_FC increments by 1 every time MCU ESM error is detected and decrements by 1 each time correct response is received. When MCU_ESM_FC ≥ MCU_ESM_FC_ENDRV_TH, the MCU_ESM_FAIL bit and MCU_ESM_ENDRV_FAIL bit are set to 1b, and if device is in the ACTIVE State or DIAGNOSTIC state the device transitions to the SAFE state. When MCU_ESM_FC ≥ MCU_ESM_FC_RST_TH, the MCU_ESM_FAIL bit and MCU_ESM_RST_FAIL bit are set to 1b, and if device is in the ACTIVE or DIAGNOSTIC state device transitions to the RESET state.

SAFETY_ERR_STAT4 Register

SAFETY_ERR_STAT4 is shown in and described in 図 11-78 and described in 表 11-65.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SAFETY_ERR_STAT4)
Write (WR_DEV_ERR_CNT). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Write access only for DEV_ERR_CNT bits.
Note:

- A logic high is latched for DIAG_STATE_TO until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.

図 11-78. Safety Error Status 4 (SAFETY_ERR_STAT4) Register

7	6	5	4	3	2	1	0
RESERVED			DIAG_STATE_TO	DEV_ERR_CNT[3:0]			
R-0b			RC-0b	R/W-0000b			

表 11-65. SAFETY_ERR_STAT4 Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-5	Reserved	R	0b	Reserved
4	DIAG_STATE_TO	R/W	0b	Bit is set to 1b when the DIAGNOSTIC state time-out event is detected. This event causes the device to transition from the DIAGNOSTIC to the SAFE state and increments DEV_ERR_CNT by 1. This bit gets cleared to 0 upon MCU read-out.
3-0	DEV_ERR_CNT[3:0]	R/W	0b	State of the device error counter. NOTE: • The counter value increments by 1 when the device transitions to the SAFE state from the DIAGNOSTIC or ACTIVE state. It does not increments when the device transitions from the RESET state to the SAFE state while DEV_ERR_CNT > SAFE_LOCK_TH. • The bit can be overwritten by SPI WR access, but only in the DIAGNOSTIC state when CFG_LOCK = 0. • When DEV_ERR_CNT = PWD_TH, the device transitions to the OFF state, and wakes-up on new wake-up event.

SPI_TRANSFER_STAT Register

SPI_TRANSFER_STAT is shown in and described in 図 11-79 and described in 表 11-66.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_SPI_TRANSFER_STAT)
Note:

- A logic high is latched until the register is read.
- The read access clears set status flag bit if condition is not present anymore. Another read access is required to confirm status bit has been cleared and monitored condition is not present anymore.
- These SPI transfer status bits reflect state of previous SPI frame transfer.

図 11-79. SPI Transfer Status (SPI_TRANSFER_STAT) Register

7	6	5	4	3	2	1	0
SPI_SDO_ERR	SPI_SHORT_FRAME	SPI_LONG_FRAME	SPI_INVALID_UNDEF_CMD	SPI_SDI_CRC_ERR	SPI_CLK_CS_ERR2	SPI_CLK_CS_ERR1	SPI_RESET_TERM

図 11-79. SPI Transfer Status (SPI_TRANSFER_STAT) Register (続き)

RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-66. SPI_TRANSFER_STAT Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	SPI_SDO_ERR	RC	0b	SPI SDO error (mismatch between SPI driver output and feedback input) flag. 0b = No SPI SDO error. 1b = SPI SDO error.
6	SPI_SHORT_FRAME	RC	0b	SPI short frame error flag. The frame contains less than 24 SPI rising, falling clock cycles, or both. 0b = No SPI short frame error. 1b = SPI short frame error.
5	SPI_LONG_FRAME	RC	0b	SPI long frame error flag. The frame contain more than 24 SPI rising, falling clock cycles, or both. 0b = No SPI long frame error. 1b = SPI long frame error.
4	SPI_INVALID_UNDEF_CMD	RC	0b	SPI command error flag due to invalid or undefined SPI Command. 0b = No SPI command error. 1b = SPI command error.
3	SPI_SDI_CRC_ERR	RC	0b	SPI CRC error flag on received SPI frame. 0b = No SPI CRC error. 1b = SPI CRC error.
2	SPI_CLK_CS_ERR2	R/C	0b	SPI clock input error (high on SPI Chip Select high-to-low transition) flag. 0b = No SPI clock error. 1b = SPI clock error.
1	SPI_CLK_CS_ERR1	RC	0b	SPI clock input error (high on SPI Chip Select low-to-high transition) flag. 0b = No SPI clock error. 1b = SPI clock error.
0	SPI_RESET_TERM	RC	0b	SPI transfer error flag due to termination by RESET event. 0b = No SPI transfer terminated by RESET event. 1b = SPI transfer terminated by RESET event.

SAFETY_ABIST_CTRL Register

SAFETY_ABIST_CTRL is shown in and described in 図 11-80 and described in 表 11-67.

Return to 表 11-23

Initialization source: NPOR, RESET
Controller access: Read (RD_SAFETY_ABIST_CTRL)
Write (WR_SAFETY_ABIST_CTRL). Write access is only available when the CTRL_BIST_LOCK bit is set to 0b.

図 11-80. Safety ABIST Control (SAFETY_ABIST_CTRL) Register

7	6	5	4	3	2	1	0
RESERVED				ABIST_GROUP4_START	ABIST_GROUP3_START	ABIST_GROUP2_START	ABIST_GROUP1_START
R-0000b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 11-67. SAFETY_ABIST_CTRL Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-4	RESERVED	R	0000b	Reserved.
3	ABIST_GROUP4_START	R/W	0b	Initiates ABIST Group 4 of tests. Once ABIST is completed, the ABIST_GROUP4_DONE status bit is set in the SAFETY_ABIST_ERR_STAT1 register, the ABIST_GROUP4_ERR status bits is set if any of ABIST Group 4 of tests failed. The bit is self-cleared unless the ABIST scheduler is enabled in the ACTIVE state.
2	ABIST_GROUP3_START	R/W	0b	Initiates ABIST Group 3 of tests. Once ABIST is completed, the ABIST_GROUP3_DONE status bit is set in the SAFETY_ABIST_ERR_STAT1 register, the ABIST_GROUP3_ERR status bits is set if any of ABIST Group 3 of tests failed. The bit is self-cleared unless the ABIST scheduler is enabled in the ACTIVE state.
1	ABIST_GROUP2_START	R/W	0b	Initiates ABIST Group 2 of tests. Once ABIST is completed, the ABIST_GROUP2_DONE status bit is set in the SAFETY_ABIST_ERR_STAT1 register, the ABIST_GROUP2_ERR status bits is set if any of ABIST Group 2 of tests failed. The bit is self-cleared unless the ABIST scheduler is enabled in the ACTIVE state.
0	ABIST_GROUP1_START	R/W	0b	Initiates ABIST Group 1 of tests. Once ABIST is completed, the ABIST_GROUP1_DONE status bit is set in the SAFETY_ABIST_ERR_STAT1 register, the ABIST_GROUP1_ERR status bits is set if any of ABIST Group 1 of tests failed. The bit is self-cleared unless the ABIST scheduler is enabled in the ACTIVE state.

SAFETY_LBIST_CTRL Register

SAFETY_LBIST_CTRL is shown in and described in 図 11-81 and described in 表 11-68.

Return to 表 11-23

Initialization source: NPOR, RESET
Controller access: Read (RD_SAFETY_LBIST_CTRL)
Write (WR_SAFETY_LBIST_CTRL). Write access is only available when the CTRL_BIST_LOCK bit is set to 0b.

図 11-81. Safety LBIST Control (SAFETY_LBIST_CTRL) Register

7	6	5	4	3	2	1	0
RESERVED		LBIST_DIAG_EN	CFG_CRC_DIAG_EN	EE_CRC_DIAG_EN	NRES_ERR_DIAG_EN	ENDRV_DIAG_EN nIRQ_DIAG_EN	LBIST_EN
R-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 11-68. SAFETY_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-6	RESERVED	R	00b	Reserved.
5	LBIST_DIAG_EN	R/W	0b	Initiates LBIST diagnostic check to confirm LBIST run can detect a failure. It covers LBIST signature check by modifying expected signature value or input data string modification in order to force LBIST error. The self-test status is monitored through bits D0 and D2 in the SAFETY_LBIST_ERR_STAT register. The bit is self-cleared when the LBIST diagnostic test is completed.

表 11-68. SAFETY_LBIST_CTRL Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
4	CFG_CRC_DIAG_EN	R/W	0b	Initiates device configuration CRC8 diagnostic check. The self-test status is monitored through bits D6 in SAFETY_LBIST_ERR_STAT register. The bit is self-cleared when the CRC diagnostic test is completed.
3	EE_CRC_DIAG_EN	R/W	0b	Initiates EEPROM CRC8 diagnostic check. The self-test status is monitored through bits D5 in SAFETY_LBIST_ERR_STAT register. The bit is self-cleared when the CRC diagnostic test is completed. During this diagnostic testing EE_CRC_ERR bit in SAFETY_ERR_STAT1 is set and can be cleared by MCU after successful completion of this diagnostic check.
2	NRES_ERR_DIAG_EN	R/W	0b	Initiates NRES driver error monitor diagnostic check. It checks that NRES driver error monitor can detect mismatch between intended driver state and actual external pin state. The self-test status is monitored through bits D4 in SAFETY_LBIST_ERR_STAT register. The bit is self-cleared when the CRC diagnostic test is completed.
1	ENDRV_DIAG_EN nIRQ_DIAG_EN	R/W	0b	Initiates ENDRV/nIRQ diagnostic check. It checks that ENDRV/nIRQ pin error monitor can detect mismatch between intended driver state and actual external pin state. The self-test status is monitored through bits D3 in SAFETY_LBIST_ERR_STAT register. The bit is self-cleared when the CRC diagnostic test is completed.
0	LBIST_EN	R/W	0b	Initiates LBIST run in the DIAGNOSTIC, the ACTIVE, or the SAFE state. The self-test status is monitored through bits D0 and D1 in the SAFETY_LBIST_ERR_STAT register. If the bit is set to 1b in the DIAGNOSTIC state, the device clears the DIAG_EXIT_MASK bit to 0b and the DIAGNOSTIC state time-out timer continues to run while the LBIST is in progress. To stay in the DIAGNOSTIC State, the MCU must set the DIAG_EXIT_MASK bit to 1b after the LBIST completion. If the bit is set to 1b in the ACTIVE or SAFE state, the device latches the state of ENDRV/nIRQ pin, and releases it after the LBIST completion. The bit is self-cleared when the LBIST run is completed.

SAFETY_CHECK_CTRL Register

SAFETY_CHECK_CTRL is shown in and described in 図 11-82 and described in 表 11-69.

Return to 表 11-23

Initialization source: NPOR, RESET
Controller access: Read (RD_SAFETY_CHECK_CTRL)
Write (WR_SAFETY_CHECK_CTRL). Write access is only available when the CTRL_LOCK bit is set to 0b.

図 11-82. Safety Check Control (SAFETY_CHECK_CTRL) Register

7	6	5	4	3	2	1	0
RESERVED			CFG_CRC_EN	ENDRV_EN nIRQ_EN	MCU_ESM_EN	RESERVED	DIAG_EXIT
R-000b			R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b

表 11-69. SAFETY_CHECK_CTRL Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-5	RESERVED	R	000b	Reserved.

表 11-69. SAFETY_CHECK_CTRL Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
4	CFG_CRC_EN	R/W	0b	Enables and disables CRC8 check on the device configuration registers. It is recommended MCU change device configuration, followed by updating SAFTY_CFG_CRC register before setting this bit to 1b. The CRC8 check runs continuously as long as this bit is set to 1b. 0b = CRC8 disabled. 1b = CRC8 enabled.
3	ENDRV_EN	R/W	0b	Enables and disables the ENDRV/nIRQ output driver. This bit is cleared when device enters the SAFE state. 0b = The ENDRV/nIRQ pin is pulled low. 1b = The ENDRV/nIRQ pin is pulled high only when device is in the ACTIVE state or DIAGNOSTIC state, if the following conditions are all met: — WD_FAIL_CNT < WD_FC_ENDRV_TH — WD_FAIL_CNT < WD_FC_RST_TH — MCU_ESM_FC < MCU_ESM_FC_ENDRV_TH
2	MCU_ESM_EN	R/W	0b	Enabes and disables MCU Error Signal Monitor (ESM). 0b = MCU ESM disabled. 1b = MCU ESM enabled.
1	Reserved	R	0b	Reserved
0	DIAG_EXIT	R/W	0b	Initiate the exit from the DIAGNOSTIC state to ACTIVE state. This bit can be set only in the DIAGNOSTIC state. Anytime the device transitions from the DIAGNOSTIC state this bit is cleared to 0b. When this bit is set to 1b and DIAG_EXIT_MASK bit is set to 0b, the device transitions from the DIAGNOSTIC to the ACTIVE state.

SAFETY_ERR_PWM_HMAX_CFG Register

SAFETY_ERR_PWM_HMAX_CFG is shown in and described in 図 11-83 and described in 表 11-70.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_ERR_PWM_HMAX_CFG)
Write (WR_SAFETY_ERR_PWM_HMAX_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b.

図 11-83. Safety Error PWM HMAX Configuration (SAFETY_ERR_PWM_HMAX_CFG) Register

7	6	5	4	3	2	1	0
PWMH_MAX[7:0]							
R/W-1010 1000b							

表 11-70. SAFETY_ERR_PWM_HMAX_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-0	PWMH_MAX[7:0]	R/W	1010 1000b	Maximum high-phase duration, $t_{PWM\_HIGHMAX}$, of the signal at the MCU_ERR pin in PWM mode (MCU_ESM_CFG = 1b). $t_{PWM\_HIGHMAX}$ is calculated by the following formula: $t_{PWM\_HIGHMAX}$ = (PWMH_MAX[7:0] + 1) × 15 µs.

SAFETY_ERR_PWM_HMIN_CFG Register

SAFETY_ERR_PWM_HMIN_CFG is shown in and described in 図 11-84 and described in 表 11-71.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_ERR_PWM_HMIN_CFG)
Write (WR_SAFETY_ERR_PWM_HMIN_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b.

図 11-84. Safety Error PWM HMIN Configuration (SAFETY_ERR_PWM_HMIN_CFG) Register

7	6	5	4	3	2	1	0
PWMH_MIN[7:0]							
R/W-10100111b							

表 11-71. SAFETY_ERR_PWM_HMIN_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-0	PWMH_MIN[7:0]	R/W	10100111b	Minimum high-phase duration, $t_{PWM\_HIGHMIN}$, of the signal at the MCU_ERR pin in PWM mode (MCU_ESM_CFG = 1b). $t_{PWM_HIGHMIN}$is calculated by the following formula: $t_{PWM\_HIGHMIN}$ = (PWMH_MIN[7:0] + 1) × 15 µs.

SAFETY_ERR_PWM_LMAX_CFG Register

SAFETY_ERR_PWM_LMAX_CFG is shown in and described in 図 11-85 and described in 表 11-72.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_ERR_PWM_HMIN_CFG)
Write (WR_SAFETY_ERR_PWM_LMAX_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b.

図 11-85. Safety Error PWM LMAX Configuration (SAFETY_ERR_PWM_LMAX_CFG) Register

7	6	5	4	3	2	1	0
PWML_MAX[7:0]							
R/W-00111101b							

表 11-72. SAFETY_ERR_PWM_LMAX_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-0	PWML_MAX[7:0]	R/W	00111101b	Maximum low-phase duration of the signal at the MCU_ERR pin in PWM mode (MCU_ESM_CFG = 1b) or TM570 mode (MCU_ESM_CFG = 0b). t_{XXX_LOWMAX} is calculated by the following formula: t_{PWM_LOWMAX} = (PWML_MAX[7:0] + 1) × 15 µs, if MCU_ESM_CFG = 1 t_{TMS570_LOWMAX} = (PWML_MAX[7:0] + 1) × 5 µs, if MCU_ESM_CFG = 0

SAFETY_ERR_PWM_LMIN_CFG Register

SAFETY_ERR_PWM_LMIN_CFG is shown in and described in 図 11-86 and described in 表 11-73.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_ERR_PWM_LMIN_CFG)
Write (WR_SAFETY_ERR_PWM_LMIN_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b.

図 11-86. Safety Error PWM LMIN Configuration (SAFETY_ERR_PWM_LMIN_CFG) Register

7	6	5	4	3	2	1	0
PWML_MIN[7:0]							
R/W-00111100b							

表 11-73. SAFETY_ERR_PWM_LMIN_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-0	PWML_MIN[7:0]	R/W	00111100b	Minimum low-phase duration, $t_{PWM\_HIGHMIN}$, of the signal at the MCU_ERR pin in PWM mode (MCU_ESM_CFG = 1b). $t_{PWM_LOWMIN}$is calculated by the following formula: t_{PWM_LOWMIN} = (PWML_MIN[7:0] + 1) × 15 µs.

SAFETY_PWD_TH_CFG Register

SAFETY_PWD_TH_CFG is shown in and described in 図 11-87 and described in 表 11-74.

Return to 表 11-23

Initialization source: NPOR
Controller access: Read (RD_SAFETY_PWD_TH_CFG)
Write (WR_SAFETY_PWD_TH_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b.

図 11-87. Safety PWD Threshold Configuration (SAFETY_PWD_TH_CFG) Register

7	6	5	4	3	2	1	0
RESERVED			DEV_ERR_CNT_PWD_EN	PWD_TH[3:0]			
R-000b			R/W-0b	R/W-1111b			

表 11-74. SAFETY_PWD_TH_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-5	RESERVED	R	000b	Reserved.
4	DEV_ERR_CNT_PWD_EN	R/W	0b	Enables and disables device transition to the OFF state when DEV_ERR_CNT[3:0] = PWD_TH[3:0]. 0b = Transition to the OFF state disabled. 1b = Transition to the OFF state enabled.
3-0	PWD_TH[3:0]	R/W	1111b	Device error count threshold at which value the device transitions to the OFF state.

SAFETY_DEV_CFG_CRC Register

SAFETY_DEV_CFG_CRC is shown in and described in 図 11-88 and described in 表 11-75.

Return to 表 11-23

Initialization source: NPOR

Controller access: Read (RD_SAFETY_DEV_CFG_CRC)
Write (WR_SAFETY_DEV_CFG_CRC). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b.

図 11-88. Safety Device Configuration CRC (SAFETY_DEV_CFG_CRC) Register

7	6	5	4	3	2	1	0
DEV_CFG_CRC[7:0]							
R/W-1001 0110b							

表 11-75. SAFETY_DEV_CFG_CRC Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-0	DEV_CFG_CRC[7:0]	R/W	1001 0110b	Expected CRC8 value for the device configuration registers. MCU needs to write calculated CRC8 value for desired device configuration to this register. NOTE: Initial state value matches CRC8 Value for default device configuration after wake-up from the OFF state.

DIAG_CTRL Register

DIAG_CTRL is shown in and described in 図 11-89 and described in 表 11-76.

Return to 表 11-23

Initialization source: NPOR, RESET
Controller access: Read (RD_DIAG_CTRL)
Write (WR_DIAG_CTRL). Write access is only available when the CTRL_LOCK bit is set to 0b.

図 11-89. Diagnostic Control (DIAG_CTRL) Register

7	6	5	4	3	2	1	0
MUX_EN	SPI_SDO	MUX_OUT	INT_CON[2:0]			MUX_CFG[1:0]	
R/W-0b	R/W-0b	R/W-0b	R/W-000b			R/W-00b	

表 11-76. DIAG_CTRL Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	MUX_EN	R/W	0b	Enables and disables the diagnostic MUX output via the DIAG_OUT pin. 0b = Disabled (DIAG_OUT pin in tri-state). 1b = Enabled.
6	SPI_SDO	R/W	0b	SPI SDO interconnect control for SDO diagnostics. The state of the SDO pin is controlled by this bit when the NCS pin is pulled high, if the control bits in this register are set as follows: – MUX_EN = 1b – INT_CON[2:0] = 111b – MUX_CFG[1:0] = 11b 0b = SPI SDO driven low. 1b = SPI SDO driven high.
5	MUX_OUT	R/W	0b	Control bit for diagnostic MUX output state test. The state of the DIAG_OUT pin is controlled by this bit if the control bits in this register are set as follows: – MUX_EN = 1b – MUX_CFG[1:0] = 00b 0b = The DIAG_OUT pin driven low. 1b = The DIAG_OUT pin driven high.

表 11-76. DIAG_CTRL Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
4-2	INT_CON[2:0]	R/W	0b	Control bits for device Interconnect test. The signal mux'd out to the DIAG_OUT pin is controlled by these bits if the control bits in this register are set as follows: – MUX_EN = 1b – MUX_CFG[1:0] = 11b 000b = No active interconnect test. 001b = MCU_ERR input. 010b = NCS input. 011b = SDI input. 100b = SCK input. 101b = Not applicable. 110b = Not applicable. 111b = SDO input controlled by the SPI_SDO bit.
1-0	MUX_CFG[1:0]	R/W	0b	Diagnostic MUX configuration. 00b = MUX output controlled by MUX_OUT bit. 01b = Digital MUX mode. 10b = Analog MUX mode. 11b = Device Interconnect mode (input pin interconnect test).

DIAG_MUX_SEL Register

DIAG_MUX_SEL is shown in and described in 図 11-90 and described in 表 11-77.

Return to 表 11-23

Initialization source: NPOR, RESET
Controller access: Read (RD_DIAG_MUX_SEL)
Write (WR_DIAG_MUX_SEL)

図 11-90. Diagnostic Mux Select (DIAG_MUX_SEL) Register

7	6	5	4	3	2	1	0
MUX_SEL[7:0]							
R/W-00000000b							

表 11-77. DIAG_MUX_SEL Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-0	DIAG_MUX_SEL[7:0]	R/W	00000000b	Diagnostic MUX channel select bits (see セクション 11.9.9 for details). These bits become effective only when the INT_CON[2:0] bits are set to 000b.

WDT_WIN1_CFG Register

WDT_WIN1_CFG is shown in and described in 図 11-91 and described in 表 11-78.

Return to 表 11-23

Initialization source: NPOR, RESET, WD_CFG change
Controller access: Read (RD_WDT_WIN1_CFG)
Write (WR_WDT_WIN1_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-91. Watchdog Window 1 Configuration (WDT_WIN1_CFG) Register

7	6	5	4	3	2	1	0
WD_RESP_WIN1_CFG[7:0] (WD_RW1C)							
R/W-11111111b							

表 11-78. WDT_WIN1_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-0	WD_RESP_WIN1_CFG (WD_RW1C) WD_CLOSE_WIN_CFG (WD_CWC)	R/W	11111111b	Sets watchdog response window 1 (or close window) duration. $t_{WD\_RESP\_WIN1}$ (or $t_{WD\_CLOSE\_WIN}$) = (WD_RW1C[7:0] + 1) × 0.55 ms.

WDT_WIN2_CFG Register

WDT_WIN2_CFG is shown in and described in 図 11-92 and described in 表 11-79.

Return to 表 11-23

Initialization source: NPOR, RESET, WD_CFG change
Controller access: Read (RD_WDT_WIN2_CFG)
Write (WR_WDT_WIN2_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.

図 11-92. Watchdog Window 2 Configuration (WDT_WIN2_CFG) Register

7	6	5	4	3	2	1	0
RESERVED			WD_RESP_WIN2_CFG[4:0] (WD_RW2C)				
R-000b			R/W-11111b				

表 11-79. WDT_WIN2_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-5	RESERVED	R	000b	Reserved.
4-0	WD_RESP_WIN2_CFG (WD_RW2C) WD_OPEN_WIN_CFG (WD_OWC)	R/W	11111b	Sets watchdog response window 2 (or open window) duration. $t_{WD\_RESP\_WIN2}$ (or $t_{WD\_OPEN\_WIN}$) = (WD_RW2C[4:0] + 1) × 0.55 ms.

WDT_Q&A_CFG Register

WDT_Q&A_CFG is shown in and described in 図 11-93 and described in 表 11-80.

Return to 表 11-23

Initialization source: NPOR, RESET, LBIST run, WD_CFG change
Controller access: Read (RD_WDT_Q&A_CFG)
Write (WR_WDT_Q&A_CFG). Write access is only available in the DIAGNOSTIC state when the CFG_LOCK bit is set to 0b. Protected by the DEV_CFG_CRC.
Note: Confirm if this register must be initialized when device is in the RESET state.

図 11-93. Watchdog Q&A Configuration (WDT_Q&A_CFG) Register

7	6	5	4	3	2	1	0
WD_ANSW_GEN_CFG		WD_Q&A_POLY_CFG		WD_Q&A_SEED			
R/W-00b		R/W-00b		R/W-1010b			

表 11-80. WDT_Q&A_CFG Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-6	WD_ANSW_GEN_CFG	R/W	0b	WD answer generation configuration.
5-4	WD_Q&A_POLY_CFG	R/W	0b	WD Q&A polynomial configuration.
3-0	WD_Q&A_SEED	R/W	1010b	WD Q&A LFSR polynomial seed value loaded when device is in the RESET state.

WDT_QUESTION_VALUE Register

WDT_QUESTION_VALUE is shown in and described in 図 11-94 and described in 表 11-81.

Return to 表 11-23

Initialization source: NPOR, RESET, LBIST run, WD_CFG change
Controller access: Read-Only (RD_WDT_QUESTION_VALUE)

図 11-94. Watchdog Question Value (WDT_QUESTION_VALUE) Register

7	6	5	4	3	2	1	0
RESERVED				WD_QUESTION[3:0]			
R-0000b				R-1100b			

表 11-81. WDT_QUESTION_VALUE Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-4	RESERVED	R	0000b	Reserved
3-0	WD_QUESTION[3:0]	R	1100b	Current watchdog question value. MCU must read (or calculate) the current watchdog question value to generate correct SPI responses.

WDT_STATUS Register

WDT_STATUS is shown in and described in 図 11-95 and described in 表 11-82.

Return to 表 11-23

Initialization source: NPOR, RESET, LBIST run, WD_CFG change
Controller access: Read-Only (RD_WDT_STATUS)
Note: Refer to for details on initialization source for each bit.

図 11-95. Watchdog Status (WDT_STATUS) Register

7	6	5	4	3	2	1	0
WD_FC_ENDRV_DIS	WD_ANSW_CNT[1:0]		WD_CFG_CHG	ANSW_ERR	SEQ_ERR	TIME_OUT	ANSW_EARLY
RC-1b	R-11b		RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-82. WDT_STATUS Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	WD_FC_ENDRV_DIS	RC	1b	Error flag indicating WD_FAIL_CNT reaches or exceeds WD_FC_ENDRV_TH. NOTE: This flag bit is cleared on read access if WD_FAIL_CNT is below WD_FC_ENDRV_TH value. 0b = WD_FAIL_CNT ≥ WD_FC_ENDRV_TH 1b = WD_FAIL_CNT < WD_FC_ENDRV_TH
6-5	WD_ANSW_CNT[1:0]	R	11b	Current state of received watchdog answer counter. These status bits are updated with every received watchdog answer. NOTE: Initial state is 11b for WD_CFG = 0, and 01b for WD_CFG = 1. Initialization events for this bit is defined in セクション 11.9.10.5.1.
4	WD_CFG_CHG	RC	0b	Watchdog configuration change status. 0b = No change in watchdog configuration. 1b = Change in watchdog configuration. Change in any of the followings constitutes watchdog configuration change: – The WDT_WIN1_CFG register – The WDT_WIN2_CFG register – The WDT_Q&A_CFG register – The WD_CFG bit
3	ANSW_ERR	RC	0b	Watchdog answer error flag. This flag bit is updated at the end of every watchdog cycle and initialized in the events defined in セクション 11.9.10.5.1. 0b = All received WD_ANSWER_RESPx bytes were correct. 1b = Any of received WD_ANSWER_RESPx bytes was incorrect.
2	SEQ_ERR	RC	0b	Watchdog sequence error flag. This flag bit is updated at the end of every watchdog cycle and can be valid only for WD_CFG = 0. The bit is initialized in the events defined in セクション 11.9.10.5.1. 0b = The number of received WD_ANSWER_RESP_x bytes in the response window 1 is equal to greater than 3. 1b = The number of received WD_ANSWER_RESP_x bytes in the response window 1 is less than 3.
1	TIME_OUT	RC	0b	Watchdog time-out error flag indicating no single watchdog answer is received within active watchdog cycle. This flag bit is updated at the end of every WD cycle. NOTE: This flag is useful to achieve synchronization between MCU and the watchdog module in TPS65313-Q1 either on transition from the RESET to the DIAGNOSTIC state, or after changing the watchdog configuration. In order to do so, MCU should not send WD response directly until this TIME_OUT flag is set. 0b = The number of WD_ANSWER_RESP_x bytes in the entire watchdog cycle is either 4 (WD_CFG = 0b), or 1 (WD_CFG = 1b). 1b = Less than 4 WD_ANSWER_RESP_x bytes were received in the entire watchdog cycle (WD_CFG = 0b), or no WD_ANSWER_RESPx byte was received (WD_CFG = 1b).

表 11-82. WDT_STATUS Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
0	ANSW_EARLY	RC	0b	Watchdog early answer error flag indicating required number of answers were provided in the response window 1 or the Close window. This flag bit is updated at the end of every WD cycle. 0b = Less than 4 WD_ANSWER_RESP_x bytes were received in the response window 1 (WD_CFG = 0b), or no answer response was received in the Close window (WD_CFG = 1b). 1b = 4 WD_ANSWER_RESP_x bytes were received in the response window 1 (WD_CFG = 0b), or 1 answer response was received in the Close window (WD_CFG = 1b).

WDT_ANSWER Register

WDT_ANSWER is shown in and described in 図 11-96 and described in 表 11-83.

Return to 表 11-23

Initialization source: NPOR, RESET
Controller access: Write (WR_WD_ANSWER)

図 11-96. Watchdog Answer (WDT_ANSWER) Register

7	6	5	4	3	2	1	0
WD_ANSWER[7:0]							
W-N/A							

表 11-83. WDT_ANSWER Register Field Descriptions

Bit	Field	Type	Initial State	Description
7-0	WD_ANSWER[7:0]	W	N/A	MCU watchdog answer response byte. MCU must write the expected WD_ANSWER_RESPx byte into this register.

OFF_STATE_L_STAT Register

OFF_STATE_L_STAT is shown in and described in 図 11-97 and described in 表 11-84.

Return to 表 11-23

Initialization source: NPOR, SPI RD Access
Controller access: Read-Only (RD_OFF_STATE_L_STAT)

図 11-97. OFF_STATE_L_STAT Register

7	6	5	4	3	2	1	0
START_UP_TO	DEV_EC_PWDN	VIN_OV	BUCKx_BOOST_VREG_FAIL	EE_CRC_ERR	RESET_TO	SYSCLK_ERR	POWER_ON_RST
RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 11-84. OFF_STATE_L_STAT Register Field Descriptions

Bit	Field	Type	Initial State	Description
7	START_UP_TO	RC	0b	Start-up time-out event caused device transition to the OFF state.
6	DEV_EC_PWDN	RC	0b	Device error count exceeding programmed device error count power-down threshold caused device transition to the OFF state.

表 11-84. OFF_STATE_L_STAT Register Field Descriptions (続き)

Bit	Field	Type	Initial State	Description
5	VIN_OV	RC	0b	VIN overvoltage caused device transition to the OFF state. NOTE: Identical to VIN_OV bit in VMON_OV_STAT register.
4	BUCKx_BOOST_VREG_FAIL	RC	0b	BUCK1 or BUCK2 or BOOST or VREG Failure caused device transition to the OFF state. Read SAFETY_BUCK1_STAT, SAFETY_BUCK2_STAT, SAFETY_BOOST_STAT, VMON_UV and VMON_OV status registers to determine which BUCK1 and/or BUCK2 and/or BOOST and/or VREG failure occurred and forced device to the OFF state.
3	EE_CRC_ERR	RC	0b	EEPROM CRC error caused device transition to the OFF state.
2	RESET_TO	RC	0b	REST state time-out event caused device transition to the OFF state.
1	SYSCLK_ERR	RC	0b	Failure detection on SYSCLK by the analog clock monitor (ACLKMNT) caused device transition to the OFF state.
0	POWER_ON_RST	RC	0b	Power-on reset (POR) event caused device transition to the OFF state.

12 Applications, Implementation, and Layout

注

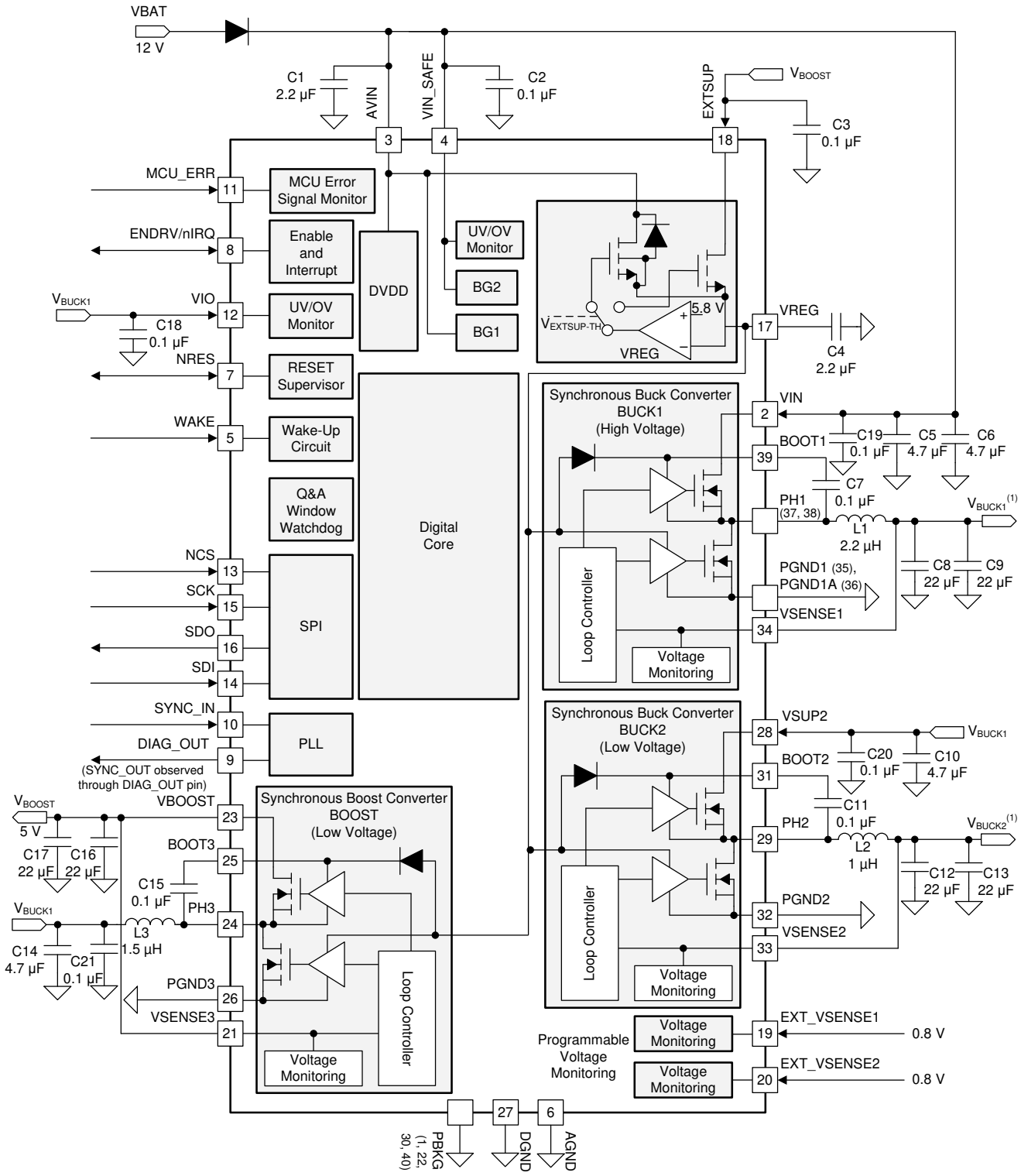
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

12.1 Application Information

The TPS65313-Q1 device is a multirail power management device (PMIC) providing the supply voltages for MCU-based or DSP-based systems. The device includes one wide-VIN synchronous buck regulator (BUCK1), one low-voltage synchronous buck regulator (BUCK2), and one low-voltage synchronous boost converter (BOOST). The device also has a SPI and several safety-relevant functions and pins. The device is designed specifically for automotive safety-relevant applications and is available in a space-saving 6-mm × 6-mm, 40 pin VQFNP package.

The BUCK1 regulator is used to convert a typical 12-V input voltage to a lower DC voltage which is then used as a preregulated input supply for the BUCK2 regulator and BOOST converter. All the regulators have predefined output voltage settings. Each regulator has integrated undervoltage (UV) and overvoltage (OV) monitoring and protection features. The BUCK1 regulator has either a 3.3-V output or 3.6-V output voltage. BUCK1 output voltage is used as input voltage for BUCK2 regulator and BOOST converter. The BUCK2 regulator has either a 1.2-V, 1.25-V, 1.8-V, or 2.3-V output voltage. The BOOST converter has a fixed 5-V output. To select the correct orderable part number for the application, see セクション 7. All the regulators have a fixed switching frequency of 2.2 MHz (typical) and the device has an optional external clock input pin to synchronize the switching regulators to the external clock input. The device also has optional spread-spectrum modulation of switching clocks of the regulators.

12.2 Typical Application



1. The VBUCK1 voltage is 3.3 V or 3.6 V. The VBUCK2 voltage is 1.2 V, 1.25 V, 1.8 V, or 2.3 V.

図 12-1. Typical Application Schematic

12.2.1 Design Requirements

For a typical automotive ADAS application featuring the TPS65313-Q1 device, use the parameters listed in 表 12-1.

表 12-1. Design Parameters

DESIGN PARAMETER	VALUE
VIN, VIN_SAFE,AVIN supply voltage range	6 V to 18 V
BUCK1 output voltage (V_{BUCK1})	3.3 V or 3.6 V
BUCK1 maximum output current	3.1 A
BUCK1 output voltage ripple	V_{PP} typical, 0.5% of VBUCK1
BUCK2 output voltage (V_{BUCK2})	1.2 V or 1.25 V or 1.8 V or 2.3 V
BUCK2 maximum output current	2 A
BUCK2 output voltage ripple	V_{PP} typical, 0.5% of V_{BUCK2}
BOOST output voltage (V_{BOOST})	5 V
BOOST maximum output current	0.6 A
BOOST output voltage ripple	V_{PP} typical 0.5% of V_{BOOST}

Make sure that the PMIC is always operating under the recommended operating conditions (see Recommended Operating Conditions) so that the device performs as desired.

Each regulator has integrated UV, OV and OVP monitoring. Having the optimum external component selections and layout design is required to avoid unintended device shutdown caused by the detection of an UV or OV or OVP condition during normal operation.

Each regulator has overcurrent monitoring. As soon as the inductor current reaches the detection threshold for the short-circuit current of the switching regulator, the regulator is disabled. Therefore, make sure that the regulators are not subjected to sudden transient load currents that are greater than the detection threshold for the short-circuit current during normal operation.

The device has a complex digital state machine and many configurable features. The device features a SPI-based question and answer (Q&A) watchdog and external MCU error-signal monitoring. Configure and service these functions correctly to avoid unintended device behavior.

12.2.2 Detailed Design Procedure

12.2.2.1 Selecting the BUCK1, BUCK2, and BOOST Output Voltages

The device has an internal feedback divider for setting the output voltage. Therefore, different output voltage options have a different orderable part number. To select the correct orderable part number for the application, see セクション 7.

The BUCK1 regulator can have either a 3.3-V or 3.6-V output. The BUCK1 output should be connected directly to the VSENSE1 pin. To measure the regulator loop response using gain-phase analyzer equipment on the prototype boards, add a 50-Ω resistor between the BUCK1 output and VSENSE1 pin. For production boards, make sure to replace the resistor with a 0-Ω resistor.

The BUCK2 regulator can have a 1.2-V, 1.25-V, 1.8-V, or 2.3-V output. The BUCK2 output should be connected directly to the VSENSE2 pin. To measure the regulator loop response using gain-phase analyzer equipment on the prototype boards, add a 50-Ω resistor between the BUCK2 output and VSENSE2 pin. For production boards, make sure to replace the resistor with a 0-Ω resistor.

The voltage of the BOOST converter is always set to 5 V. The BOOST output should be connected directly to the VSENSE3 pin. To measure the regulator loop response using gain-phase analyzer equipment on the prototype boards, add a 50-Ω resistor between the BOOST output and VSENSE3 pin. For production boards, make sure to replace the resistor with a 0-Ω resistor.

12.2.2.2 Selecting the BUCK1, BUCK2, and BOOST Inductors

Because all the regulators have internal compensation and limited output-voltage settings, inductor values and output capacitor values are limited to ensure stability of the regulator. To select the values of the output inductor and capacitors, see 表 10-1.

The BUCK1 regulator has a 2.2-µH inductor. Select the inductor with a saturation current rating more than 7 A. In this example, IHLP2525CZER2R2M5A inductor from Vishay is used.

The BUCK2 regulator has a 1-µH inductor. Select the inductor with a saturation current rating more than 4.5 A. In this example, TFM252012ALMA1R0MTAA inductor from TDK is used.

The BOOST converter has a 1.5-µH inductor. Select the inductor with a saturation current rating more than 2.7 A. In this example, TFM252012ALMA1R5MTAA inductor from TDK is used.

12.2.2.3 Selecting the BUCK1 and BUCK2 Output Capacitors

The minimum output capacitance for each regulator is 25 µF and the maximum output capacitance is defined as 100 µF. X7R-type, low-ESR ceramic capacitors are recommended. The minimum and maximum capacitance values specified are the effective capacitance values after considering all the tolerances, voltage derating, and aging effects. Therefore, users must use the value that is higher than the specified value to accommodate for these variations. Select the output capacitor value to be 1.5 times the minimum required capacitance value. The output capacitance range allows users to optimize the output voltage ripple and load transient performance according to their application conditions. Selecting the output capacitance value within the specified range is important to meet the stability requirements of the regulators. Stability performance must be measured on the application board to make sure that regulators are stable for the selected output capacitor.

Use 式 6 to calculate the output capacitance (C_{OUT}) value based on the load transient requirements.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \tag{6}$$

where

- ΔI_{OUT} is the change in output current.
- f_{SW} is the switching frequency of the regulator.
- ΔV_{OUT} is the allowable change in the output voltage.

Use 式 7 to calculate the peak-to-peak output voltage ripple.

$$V_{BUCKx\_RIPPLE(PP)} = I_{L\_RIPPLE}\left(\frac{1}{8 \times C_{OUT} \times f_{SW}} + ESR\right) + ESL\left(\frac{V_{IN\_MAX}}{L}\right) \tag{7}$$

where

- $V_{BUCKx\_RIPPLE(PP)}$ is the peak-to-peak-output voltage ripple of the buck regulator.
- I_{L_RIPPLE} is the inductor ripple current (A).
- ESR is the equivalent series resistance of the output capacitor (Ω).
- ESL is the equivalent series inductance of the output capacitor (H).
- V_{IN_MAX} is the maximum input voltage (V).
- L is the value of the inductor (H).

For this example, the BUCK1 voltage is 3.3 V with a 2% change in the output voltage for a load step from 0 A to 2 A. The resulting value of the BUCK1 output capacitance is approximately 28 µF. Considering the capacitor tolerances, derating, and aging effects, two 22-µF, 10-V rating, X7R-type capacitors (GCM31CR71A226KE02 from Murata) are used.

For this example, the calculated BUCK1 output voltage ripple is approximately 11 mV_{PP} for a typical 44-µF capacitor with 3-mΩ effective ESR, 1-nH ESL, 18-V input voltage, 3.3-V output voltage, 3-A maximum load current, and an inductor ripple current that is approximately 20% of the maximum load current.

For this example, the BUCK2 voltage is 1.8 V with a 2 % change in the output voltage for a load step from 0 A to 1 A. The resulting value of the BUCK2 output capacitance is approximately 25 µF. Considering the capacitor tolerances, derating, and aging effects, two 22-µF, 10-V rating, X7R-type capacitors (GCM31CR71A226KE02 from Murata) are used.

For this example, the calculated BUCK2 output voltage ripple is approximately 5 mV_{PP} for a typical 44-µF capacitor with 3-mΩ effective ESR, 1-nH ESL, 3.3-V input voltage, 1.8-V output voltage , 1-µH inductor, 2-A maximum load current, and an inductor ripple current that is approximately 20% of the maximum load current.

注

The calculated values of the output ripple are theoretical values and actual results should be obtained based on the measurements done on the application board.

12.2.2.4 Selecting the BOOST Output Capacitors

The minimum output capacitance for the BOOST converter is 25 µF and the maximum output capacitance is 100 µF. X7R-type, low-ESR ceramic capacitors are recommended. The capacitance value specified in this example is the effective capacitance value after considering all the tolerances, voltage derating, and aging effects. Select the output capacitor value to be 1.5 times the minimum required capacitance value. In this example, two 22-µF, 10-V rating, X7R-type capacitors (GCM31CR71A226KE02 from Murata) are used.

Use 式 8 to calculate the peak-to-peak output voltage ripple.

$$V_{BOOST\_RIPPLE(PP)} = \frac{I_{OUT\_MAX} \times D}{f_{SW} \times C_{OUT}} \tag{8}$$

where

- $V_{BOOST\_RIPPLE(PP)}$ is the peak-to-peak output voltage ripple of the boost converter.
- I_{OUT_MAX} is the maximum output current of the application (0.6 A).
- f_{SW} is the switching frequency of the converter (2.2 MHz).
- D is the duty cycle (see 式 9).

$$D = 1 - \frac{V_{IN\_MIN} \times \eta}{V_{OUT}} \tag{9}$$

where

- V_{IN_MIN} is the minimum input voltage.
- η is the efficiency of the converter (approximately 90%).
- V_{OUT} is the desired output voltage.

The ESR of the output capacitors has an impact on the output voltage ripple. Use 式 10 to calculate output voltage ripple as a result of ESR.

$$V_{OUT\_RIPPLE(ESR)} = ESR\left(\frac{I_{OUT\_MAX}}{1-D} + \frac{I_{L\_RIPPLE}}{2}\right) \tag{10}$$

where

- $V_{OUT\_RIPPLE(ESR)}$ is the additional output voltage ripple because of the ESR of the capacitor.
- ESR is the equivalent series resistance of the output capacitor that was used.

- I_{OUT_MAX} is the maximum output current of the application.
- I_{L_RIPPLE} is the inductor ripple current (see 式 11).

$$I_{L\_RIPPLE} = \frac{V_{IN\_MIN} \times D}{f_{SW} \times L} \quad (11)$$

where

- L is the selected inductor value

Use 式 12 to calculate the total peak-to-peak output ripple.

$$V_{OUT\_RIPPLE(PP)} = V_{BOOST\_RIPPLE} + V_{OUT\_RIPPLE(ESR)} \quad (12)$$

For this example, the calculated BOOST output voltage ripple is approximately 6 mV_{PP} for a typical 44-µF output capacitor with 3-mΩ effective ESR, 5-V BOOST output voltage (V_{BOOST}), 3.3-V BOOST input voltage, 0.6-A maximum load current, and 1.5-µH inductor.

注

The calculated values of the output ripple are theoretical values and actual results should be obtained based on the measurements done on the application board.

12.2.2.5 Input Filter Capacitor Selection for BUCK1, BUCK2, and BOOST

An effective capacitance of at least 4.7 µF is required very close to the VIN pin. In this example, considering capacitor tolerances and derating effects, two 4.7-µF, 50-V, X7R-type ceramic capacitors (CGA6P3X7R1H475K250AB from TDK) are used. A 100-nF, 50-V, X7R-type ceramic capacitor is also recommended for high frequency filtering. Depending on the load transient, line transient, and electromagnetic compatibility (EMC) requirements, additional capacitors or filters may be required on the VIN pin.

An effective capacitance value of at least 2.2 µF is required close to the VSUP2 and BOOST input pins. Considering capacitor tolerances and derating effects, one 4.7-µF, 16-V, X7R-type ceramic capacitor is recommended. A 100-nF, 16-V, X7R-type ceramic capacitor is also recommended for high frequency filtering. Depending on the load transient, line transient, and EMC requirements, additional capacitors or filters may be required on these pins.

12.2.2.6 Input Filter Capacitors on AVIN and VIN_SAFE Pins

The AVIN pin is used as the supply pin for the VREG regulator. TI recommends using a 2.2-µF, 50-V, X7R-type ceramic capacitor close to the AVIN pin. A 100-nF, 50-V, X7R-type ceramic capacitor is recommended close to the VIN_SAFE pin.

12.2.2.7 Bootstrap Capacitor Selection

The BUCK1 regulator, BUCK2 regulator, and BOOST converter require a bootstrap capacitor. This bootstrap capacitor must have a value of 100 nF and be a X7R-type capacitor. The capacitor should have a 16-V or higher voltage rating. For the BUCK1 regulator, the bootstrap capacitor is located between the PH1 pin and the BOOT1 pin. For the BUCK2 regulator, the bootstrap capacitor is located between the PH2 pin and the BOOT2 pin. For the BOOST converter, the bootstrap capacitor is located between the PH3 pin and the BOOT3 pin.

12.2.2.8 Internal Linear Regulator (VREG) Output Capacitor Selection

The device has a linear regulator to supply the gate drives of each regulator. A 2.2-µF, 16-V, X7R-type ceramic capacitor is recommended on the VREG pin.

12.2.2.9 EXTSUP Pin

To improve efficiency of the internal VREG regulator, connect the EXTSUP pin to the BOOST output. A 100-nF, 16-V, X7R-type ceramic capacitor is recommended close to the EXTSUP pin.

12.2.2.10 WAKE Input Pin

When the WAKE signal is greater than its detection threshold (4.6 V, typical) for more than its deglitch time (130 µs, typical), a valid WAKE signal is detected. The signal is internally latched (WAKE_L bit) and the device starts its power-up sequence. After the device is powered on, even if a high on the WAKE pin is removed, the device is still active. If the wake latch (WAKE_L bit) is cleared and the WAKE signal is low, the device goes to the OFF state. For more information on the WAKE pin, see セクション 11.14.

12.2.2.11 VIO Supply Pin

The VIO pin is the supply input for the digital interface pins. The voltage of the VIO pin should be more than 3 V. A 100-nF ceramic filter capacitor is recommended close to the pin. This pin is usually connected to the BUCK1 output.

12.2.2.12 External General-Purpose Voltage Monitor Input Pins (EXT_VSENSE1 and EXT_VSENSE2)

The EXT_VSENSE1 and EXT_VSENSE2 pins can be used to monitor UV or OV on any external supply rails in the system. The nominal voltage level at the pins is required to be set to 0.8 V by the external resistor divider. High precision resistors are required for the voltage divider because of the narrow range of the detection threshold. Use a 100-nF, X7R-type filter capacitor to filter the high frequency noise on this pin. In case of an UV or OV event on these pins, the corresponding SPI status bit is set and the device goes to the RESET state. Depending on the orderable part number used in the application, these monitoring pins are enabled during start-up or can be enabled through the SPI PWR_CTRL register. For more information on the functionality of these pins, see セクション 11.10.

注

If these two pins are not used in the application, connect these pins to ground.

12.2.2.13 SYNC_IN Pin

The SYNC_IN pin can be used as the external clock input. This input pin requires a 2.2-MHz (typ) clock with a low level less than 0.4 V, a high level more than 2 V, and a duty cycle from 10% to 90%. If the device does not detect any clock on the SYNC_IN pin, then the regulators get a clock from the free-running VCO in the PLL.

12.2.2.14 MCU_ERR Pin

The MCU ESM block monitors the system MCU error conditions signaled over the MCU_ERR input pin. The MCU_ERR pin is configurable for two different operating modes. The first mode is TMS570 mode and in this mode this pin detects an error if the low level on this pin exceeds the programmed low pulse duration. The second mode is PWM mode and in this mode this pin detects an error if a PWM input signal violates the programmed PWM low pulse and high pulse duration. For more information on the ESM, see セクション 11.9.11.

12.2.2.15 NRES Pin

The NRES pin is an open-drain output with an internal pullup resistor. The NRES pin is intended to drive the reset of the primary system processor. This pin must keep the primary processor and peripheral devices in a defined state during power up and power down when supply voltages are out of range or a critical failure is detected. For more information on the NRES pin, see セクション 11.9.12.

12.2.2.16 ENDRV/nIRQ Pin

This pin can be used in the system as the ENDRV input, an external error interrupt to the system MCU, or both functions. The device has no dedicated configuration bit to configure the ENDRV (enable drive) mode or nIRQ (interrupt) mode. How the ENDRV/nIRQ pin is used is determined by system-level requirements. For more information on the ENDRV/nIRQ driver, see セクション 11.9.13.

12.2.2.17 DIAG_OUT Pin

The internal analog and digital signals of the device can be observed through the multiplexer on the DIAG_OUT pin to support system diagnostics. For more information on the diagnostic output pin (DIAG_OUT), see セクション 11.9.9.

12.2.2.18 SPI Pins (NCS,SCK, SDI, SDO)

The TPS65313-Q1 device supports a SPI. No external pullup or pulldown resistors are required for these pins. For the electrical specifications of the SPI pins, see セクション 9.18, セクション 9.22, and セクション 9.21.

12.2.2.19 PBKGx, AGND, DGND, and PGNDx Pins

Connect all PBKGx, AGND, DGND, and PGNDx pins together at the device thermal pad to make a star connection below the device thermal pad.

12.2.2.20 Calculations for Power Dissipation and Junction Temperature

The TPS65313-Q1 device integrates three switching regulators in a small package. Depending on the load current on each regulator, at high temperature conditions, the junction temperature of the device can exceed 150°C. Therefore, understanding the device load currents and associated power dissipation early in the design cycle is critical. This section provides guidelines to calculate the device power dissipation and estimated junction temperature. To make the calculations easy, simple equations are provided. These equations should be used for approximate calculations only.

12.2.2.20.1 BUCK1 Output Current Calculation

The BUCK1 regulator is used as the input supply for the BUCK2 regulator and BOOST converter. The BUCK1 regulator can also supply other peripheral devices in the system that require a 3.3-V or 3.6-V supply. To calculate the total load current on the BUCK1 regulator, BUCK2 regulator, and BOOST converter, input current must be calculated. Use 式 13 to calculate the BUCK2 input current.

$$I_{IN\_BUCK2} = \frac{V_{BUCK2}}{V_{BUCK1}} \times \frac{I_{OUT\_BUCK2}}{\eta_{BUCK2}} \tag{13}$$

where

- I_{IN_BUCK2} is the input current of the BUCK2 regulator.
- I_{OUT_BUCK2} is the output load current on the BUCK2 regulator.
- η_{BUCK2} is the efficiency of the BUCK2 regulator.

Use 式 14 to calculate the BOOST input current.

$$I_{IN\_BOOST} = \frac{V_{BOOST}}{V_{BUCK1}} \times \frac{I_{OUT\_BOOST}}{\eta_{BOOST}} \tag{14}$$

where

- I_{IN_BOOST} is the input current of the BOOST converter.
- I_{OUT_BOOST} is the output load current on the BOOST converter.
- η_{BOOST} is the efficiency of the BOOST converter.

Use 式 15 to calculate the total current on the BUCK1 regulator.

$$I_{OUT\_BUCK1(tot)} = I_{OUT\_BUCK1\_LOAD} + I_{IN\_BUCK2} + I_{IN\_BOOST} \tag{15}$$

where

- $I_{OUT\_BUCK1(tot)}$ is the total current on the BUCK1 regulator.
- $I_{OUT\_BUCK1\_LOAD}$ is the stand-alone load current on BUCK1.

12.2.2.20.2 Device Power Dissipation Estimation

The power dissipation of the device can be estimated by adding the power dissipation of each regulator. The power dissipation of each regulator can be estimated based on the measured efficiency of each regulator. The measured efficiency of the regulator consists of device power losses and inductor power losses. To estimate the power dissipation within the device, the power dissipation of the inductor should be subtracted from the total regulator power dissipation that is calculated based on the efficiency measurement.

Use 式 16 to estimate the total regulator power dissipation for the BUCK1 regulator, BUCK2 regulator, and BOOST converter.

$$P_{D(tot)} = V_{OUT} \times I_{OUT} \times \left(\frac{1-\eta}{\eta} \right) \tag{16}$$

where

- $P_{D(tot)}$ is the total power dissipation of the BUCK1 regulator, BUCK2 regulator, or BOOST converter including inductor power dissipation.
- V_{OUT} is the output voltage of the regulator.
- I_{OUT} is the output current of the regulator.
- η is the efficiency of the regulator based on measurement results.

Use 式 17 to calculate the internal power dissipation of the BUCK1 regulator.

$$P_{D(BUCK1)} = P_{D(BUCK1\_tot)} - \left(I_{OUT\_BUCK1(tot)}{}^2 \times L_{DCR\_BUCK1} \right) \tag{17}$$

where

- $P_{D(BUCK1)}$ is the internal power dissipation of the device because of the BUCK1 regulator.
- $P_{D(BUCK1\_tot)}$ is the total power dissipation of the BUCK1 regulator including inductor power dissipation.
- L_{DCR_BUCK1} is the series resistance of the inductor as specified in the data sheet of the BUCK1 inductor.

Use 式 18 to calculate the internal power dissipation of the BUCK2 regulator.

$$P_{D(BUCK2)} = P_{D(BUCK2\_tot)} - \left(I_{OUT\_BUCK2}{}^2 \times L_{DCR\_BUCK2} \right) \tag{18}$$

where

- $P_{D(BUCK2)}$ is the internal power dissipation of the device because of the BUCK2 regulator.
- $P_{D(BUCK2\_tot)}$ is the total power dissipation of the BUCK2 regulator including inductor power dissipation.
- L_{DCR_BUCK2} is the series resistance of the inductor as specified in the data sheet of the BUCK2 inductor.

Use 式 19 to calculate the internal power dissipation of the device because of the BOOST converter.

$$P_{D(BOOST)} = P_{D(BOOST\_tot)} - \left(I_{IN\_BOOST}{}^2 \times L_{DCR\_BOOST} \right) \tag{19}$$

where

- $P_{D(BOOST)}$ is the internal power dissipation of the device because of the BOOST converter.
- $P_{D(BOOST\_tot)}$ is the total power dissipation of the BOOST converter including inductor power dissipation.
- I_{IN_BOOST} is the input current of the BOOST converter (see 式 14).
- L_{DCR_BOOST} is the series resistance of the inductor as specified in the data sheet of the BOOST inductor.

Use 式 20 to calculate the total internal power dissipation of the device.

$$P_{D(DEVICE)} = P_{D(BUCK1)} + P_{D(BUCK2)} + P_{D(BOOST)} \quad (20)$$

where

- $P_{D(DEVICE)}$ is the total internal power dissipation of the device.

12.2.2.20.3 Device Junction Temperature Estimation

Use 式 21 to estimate the junction temperature of the device (T_J).

$$T_J = T_A + \left(R_{th} \times P_{D(tot)}\right) \quad (21)$$

where

- T_A is the ambient temperature of the device.
- R_{th} is the thermal resistance of the device.

The thermal resistance of the device is highly dependent on external factors such as the PCB, housing, and thermal management. Therefore the thermal resistance should be estimated based on the actual measurements considering all the system-level parameters that influence this parameter. In this calculation example, the thermal resistance value, which is based on thermal simulation, is provided for two different PCB models with some assumptions. The values provided in this section are only for reference and are for initial estimations only.

12.2.2.20.3.1 Example for Device Junction Temperature Estimation

表 12-2 lists all the typical values required to estimate the junction temperature of the device. The efficiency values are from the measurements done on the evaluation module (EVM) for the TPS65313-Q1 device (TPS65313-EVM).

表 12-2. Parameters for Junction Temperature Estimation

REGULATOR	INPUT VOLTAGE	OUTPUT VOLTAGE	LOAD CURRENT(1)	EFFICIENCY AT SPECIFIED LOAD CURRENT(2)	INDUCTOR DCR
BUCK1	12 V	3.3 V	1 A	83%	0.018 Ω
BUCK2	3.3 V	1.8 V	1 A	88%	0.035 Ω
BOOST	3.3 V	5 V	0.3 A	93%	0.052 Ω

(1) The load current on the BUCK1 regulator is the stand-alone load current which does not include the BUCK1 current because of the BUCK2 regulator and BOOST converter.
(2) For V_{BUCK2} = 1.2 V, efficiency at 1 A = 83%. For V_{BUCK2} = 2.3 V, efficiency at 1 A = 90%

Based on the power dissipation equations, the results are as follows:

- The total load current on the BUCK1 regulator including the BUCK2 regulator and BOOST convert is approximately 2 A.
- The internal power dissipation of the device because of the BUCK1 regulator is approximately 1.28 W.
- The internal power dissipation of the device because of the BUCK2 regulator is approximately 0.21 W.
- The internal power dissipation of the device because of the BOOST converter is approximately 0.1 W.
- The total internal power dissipation of the device is approximately 1.59 W.

For this TI thermal simulation example, the ambient temperature is assumed to be the PCB temperature measured on the PCB, 1-mm away from the device. Also no additional heat sink was used and the device is assumed to be fully soldered to the thermal pad with thermal vias on the PCB. For this condition, the junction-to-board characterization parameter (ψ_{JB}) is the appropriate thermal resistance parameter to be used to estimate the device junction temperature. Unlike JEDEC standard simulation, this simulation does not assume uniform power distribution across the device when estimating the thermal resistance. But, hot spot-based simulation was done to estimate the thermal resistance.

表 12-3 lists the specifications and thermal results for the standard and custom PCBs.

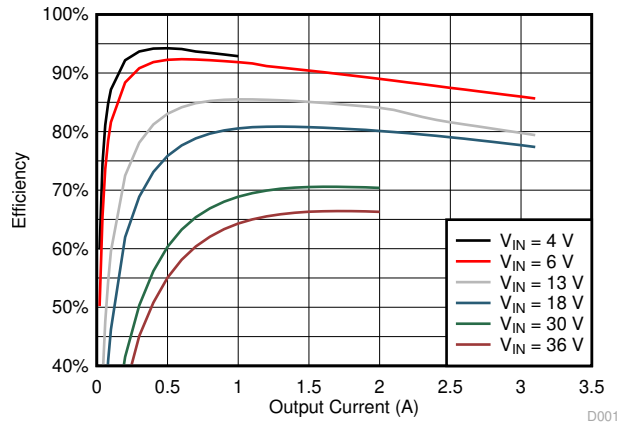
表 12-3. PCB Specifications and Thermal Results

SPECIFICATION	STANDARD BOARD	CUSTOM BOARD
Board size (l × w)	75 mm × 100 mm	30 mm × 30 mm
Board thickness	1.6 mm	1.6 mm
Number of layers	4	6
Size of thermal via array	4 × 4 with vias connected to one inner layer	4 × 4 with vias connected to each inner layer
Thermal pad	Fully soldered	Fully soldered
Thickness of each top and bottom copper layer	2 oz	2 oz
Thickness of inner layers	1 oz	1 oz
Simulated junction-to-board characterization parameter (ψ_{JB})	14°C/W	11°C/W
Based on 式 21, the calculated junction temperature at a PCB temperature of 125°C and 1.59-W internal power dissipation of the device	147°C	142°C

These calculations are only for the purpose of initial estimation and users must validate the thermal performance on their board to make sure that the junction temperature of the device is kept lower than 150°C. If the junction temperature of the device is greater than 150°C, special thermal management is required.

12.2.3 Application Curves

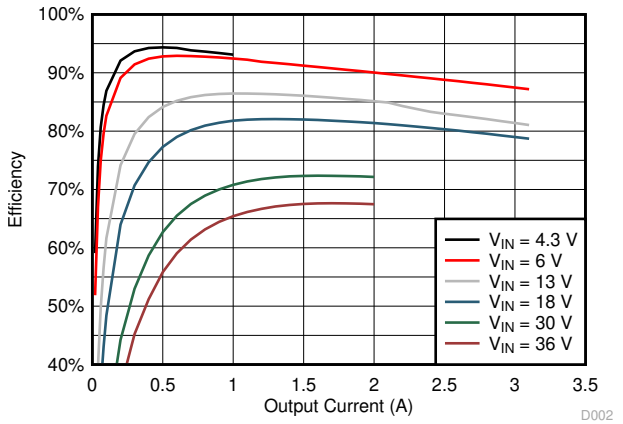
These parameters are not tested and represent typical performance only. Unless otherwise stated, the following conditions apply: V_{IN} = 13 V, T_A = 25°C, Spread Spectrum Modulation (SSM) Disabled, external components mentioned in セクション 12.2.



注

V_{BUCK1} = 3.3 V

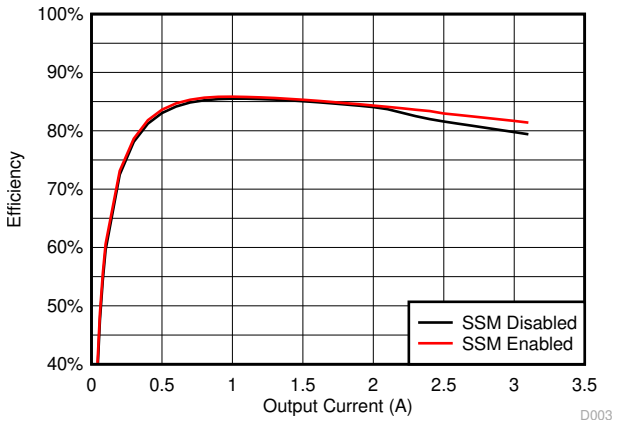
図 12-2. BUCK1 Efficiency



注

V_{BUCK1} = 3.6 V

図 12-3. BUCK1 Efficiency



注

V_{BUCK1} = 3.3 V V_{IN} = 13 V

図 12-4. BUCK1 Efficiency

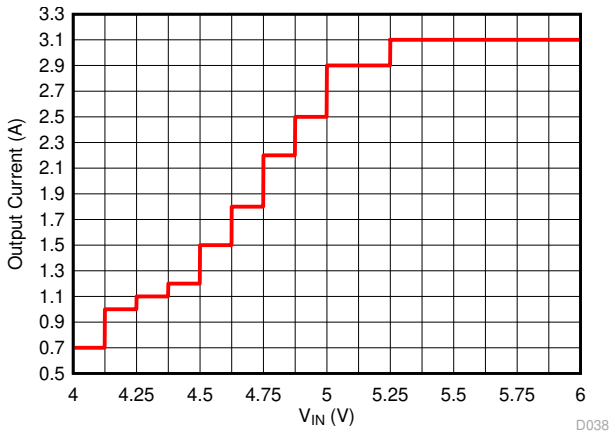
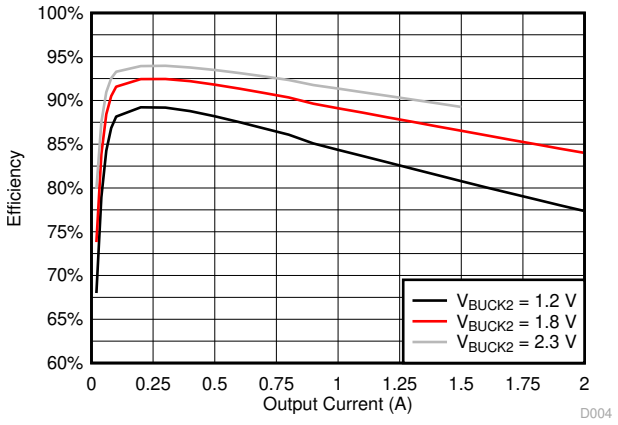


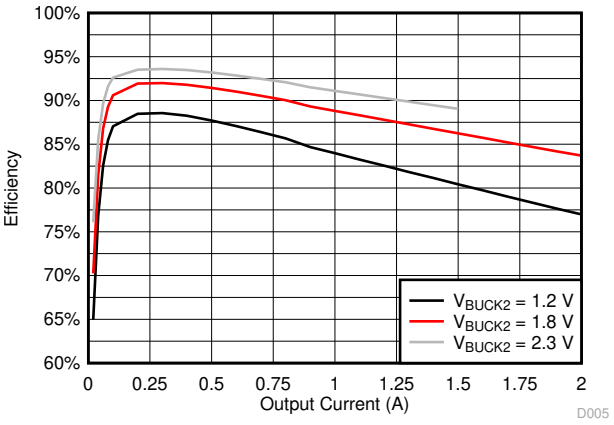
図 12-5. BUCK1 Output Current at Low V_{IN} Conditions



注

V_{BUCK1} = 3.3 V L_{OUT} = IHLP2525CZER1R0M5A

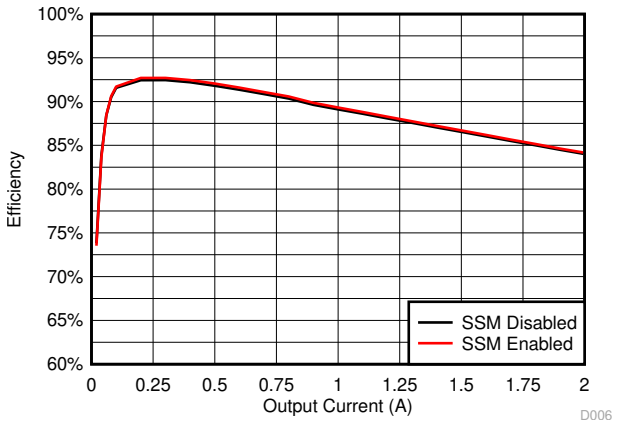
図 12-6. BUCK2 Efficiency



注

V_{BUCK1} = 3.6 V L_{OUT} = IHLP2525CZER1R0M5A

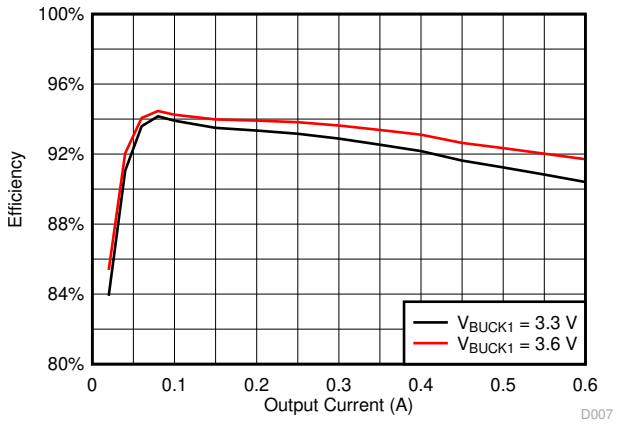
図 12-7. BUCK2 Efficiency



注

V_{BUCK1} = 3.3 V V_{BUCK2} = 1.8 V
L_{OUT} = IHLP2525CZER1R0M5A

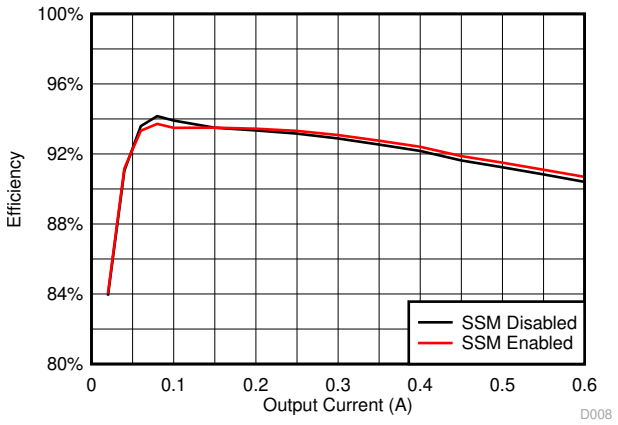
図 12-8. BUCK2 Efficiency



注

L_{OUT} = IHLP2525CZER1R5M5A

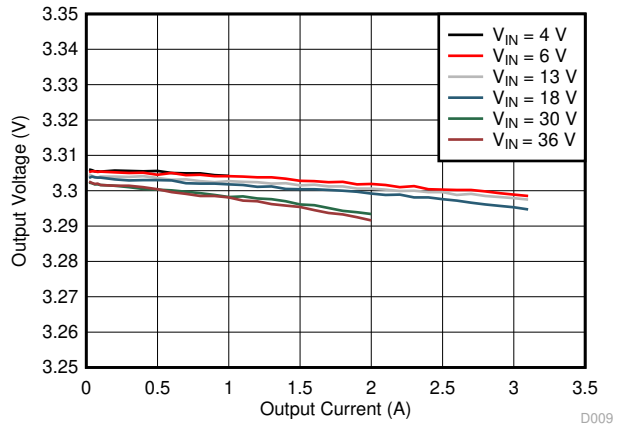
図 12-9. BOOST Efficiency



注

V_{BUCK1} = 3.3 V L_{OUT} = IHLP2525CZER1R5M5A

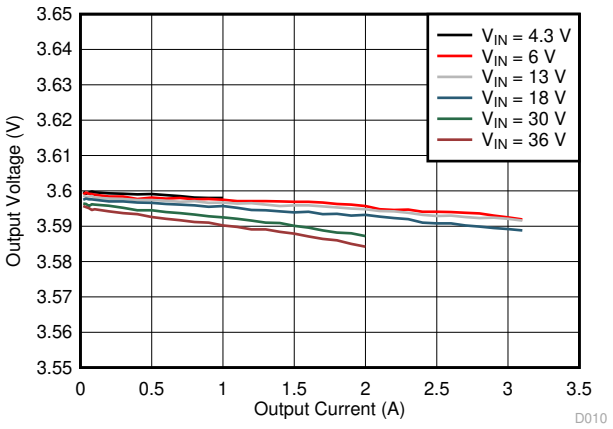
図 12-10. BOOST Efficiency



注

V_{BUCK1} = 3.3 V

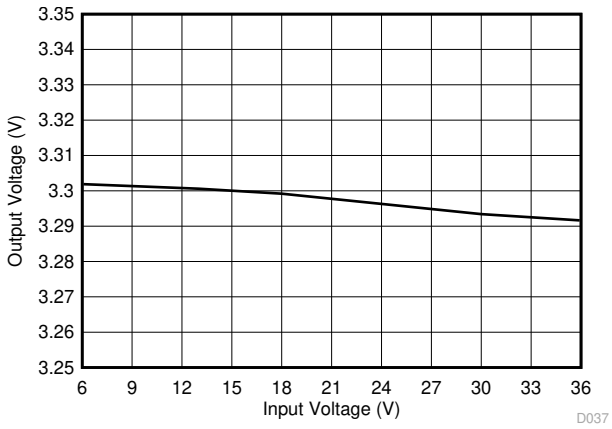
図 12-11. BUCK1 Load and Line Regulation



注

V_{BUCK1} = 3.6 V

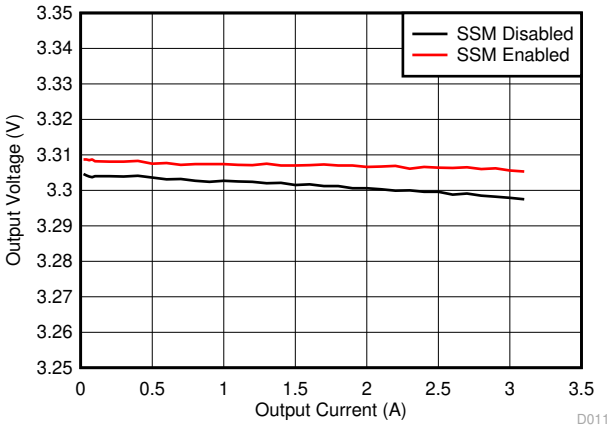
図 12-12. BUCK1 Load and Line Regulation



注

V_{BUCK1} = 3.3 V I_{OUT}= 2 A

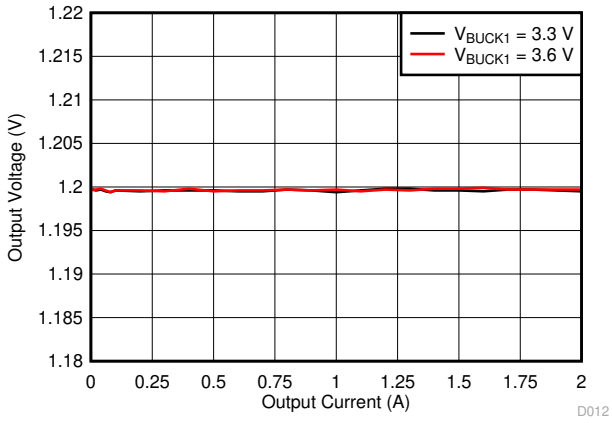
図 12-13. BUCK1 Line Regulation



注

V_{BUCK1} = 3.3 V

図 12-14. BUCK1 Load Regulation

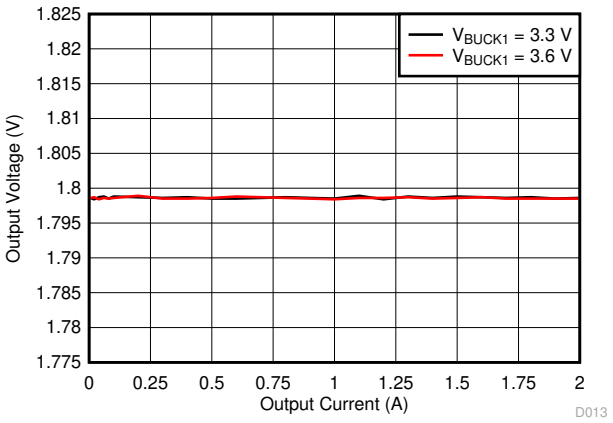


注

V_{BUCK2} = 1.2 V C_{OUT} = 22 µF + 10 µF

L_{OUT} = IHLP2525CZER1R0M5A

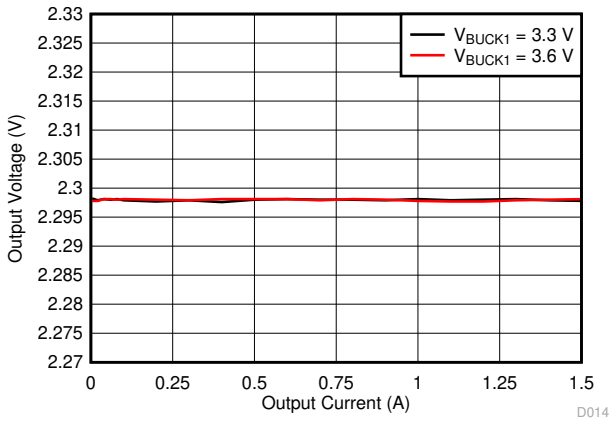
図 12-15. BUCK2 Load Regulation



注

V_{BUCK2} = 1.8 V　　C_{OUT} = 22 µF + 10 µF
L_{OUT} = IHLP2525CZER1R0M5A

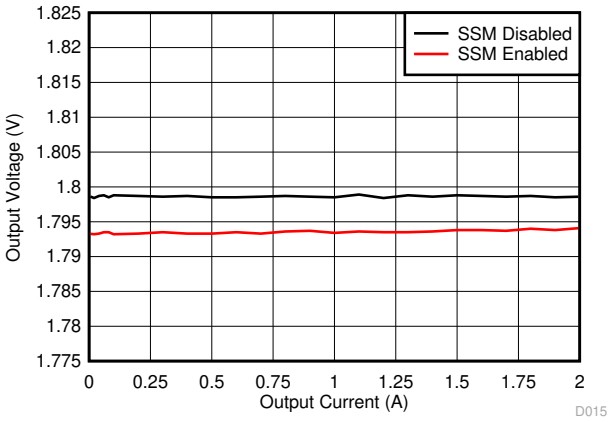
図 12-16. BUCK2 Load Regulation



注

V_{BUCK2} = 2.3 V　　C_{OUT} = 22 µF + 10 µF
L_{OUT} = IHLP2525CZER1R0M5A

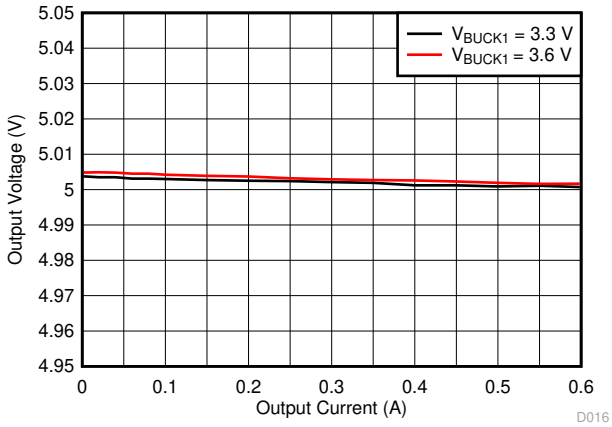
図 12-17. BUCK2 Load Regulation



注

V_{BUCK2} = 1.8 V　　C_{OUT} = 22 µF + 10 µF
V_{BUCK1} = 3.3 V　　L_{OUT} = IHLP2525CZER1R0M5A

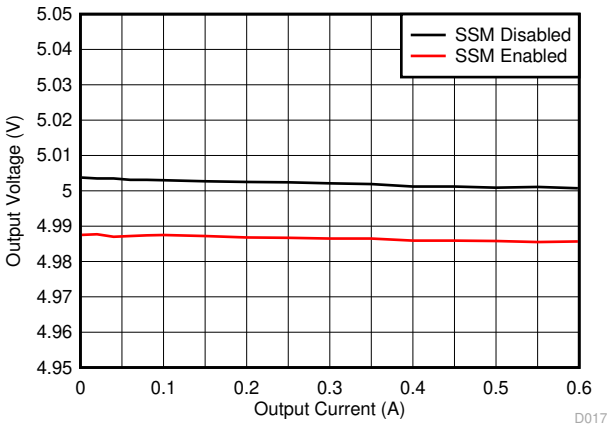
図 12-18. BUCK2 Load Regulation



注

C_{OUT} = 22 µF + 10 µF　　L_{OUT} = IHLP2525CZER1R5M5A

図 12-19. BOOST Load and Line Regulation



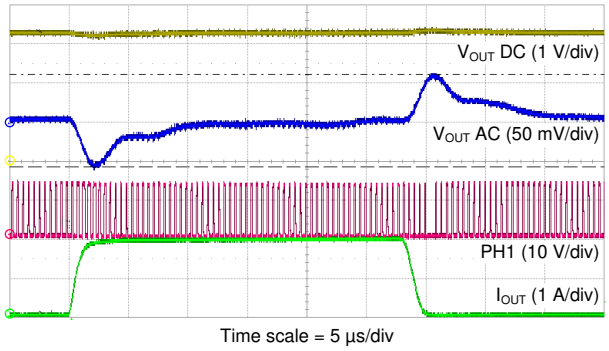
注

V_{BUCK1} = 3.3 V

C_{OUT} = 22 µF + 10 µF

L_{OUT} = IHLP2525CZER1R5M5A

図 12-20. BOOST Load Regulation



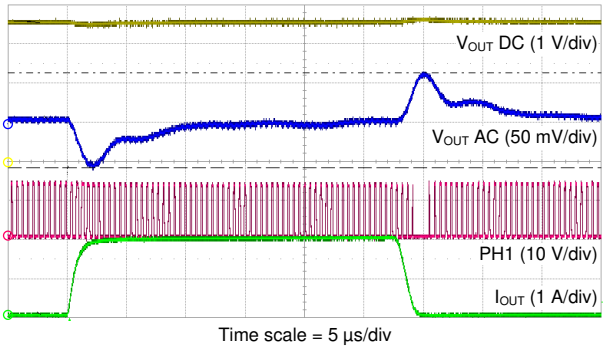
注

V_{OUT} (V_{BUCK1}) = 3.3 V

I_{OUT} = 0 A to 2 A

T_R = T_F = 1 µs

図 12-21. BUCK1 Load Transient



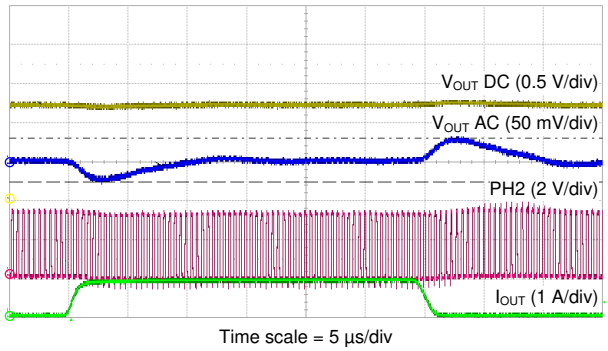
注

V_{OUT} (V_{BUCK1}) = 3.6 V

I_{OUT} = 0 A to 2 A

T_R = T_F = 1 µs

図 12-22. BUCK1 Load Transient



注

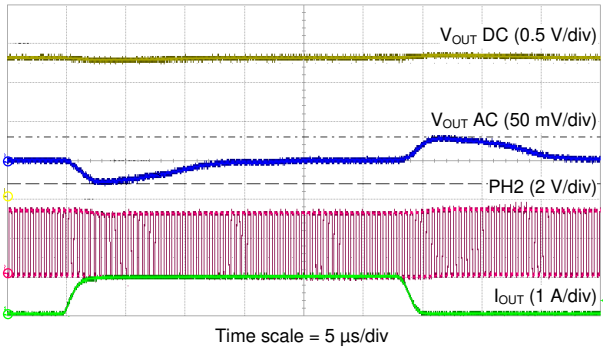
V_{OUT} (V_{BUCK2}) = 1.2 V

V_{BUCK1} = 3.3 V

T_R = T_F = 1 µs

I_{OUT} = 0 A to 1 A

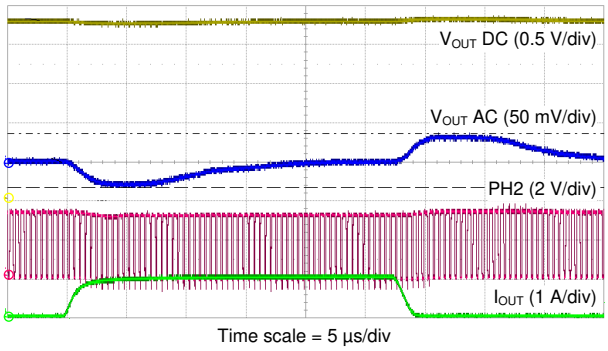
図 12-23. BUCK2 Load Transient



注

V_{OUT} (V_{BUCK2}) = 1.8 V
V_{BUCK1} = 3.3 V
T_R = T_F = 1 µs
I_{OUT} = 0 A to 1 A

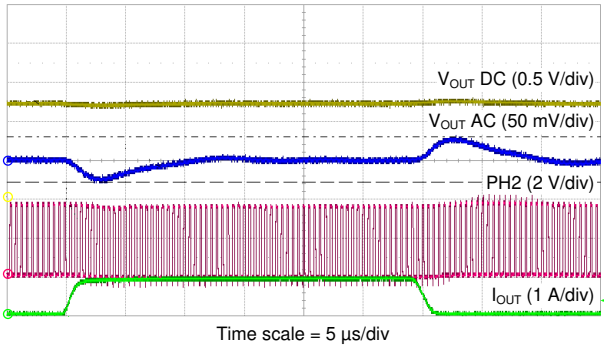
図 12-24. BUCK2 Load Transient



注

V_{OUT} (V_{BUCK2}) = 2.3 V
V_{BUCK1} = 3.3 V
T_R = T_F = 1 µs
I_{OUT} = 0 A to 1 A

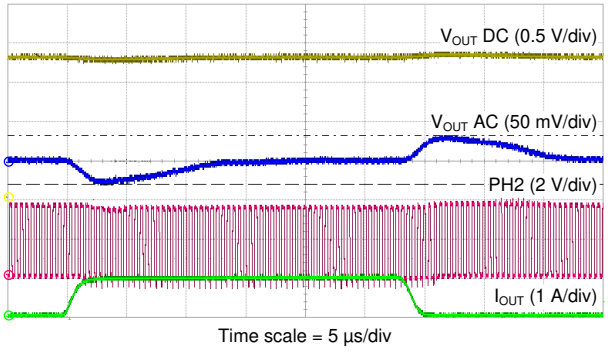
図 12-25. BUCK2 Load Transient



注

V_{OUT} (V_{BUCK2}) = 1.2 V
V_{BUCK1} = 3.6 V
T_R = T_F = 1 µs
I_{OUT} = 0 A to 1 A

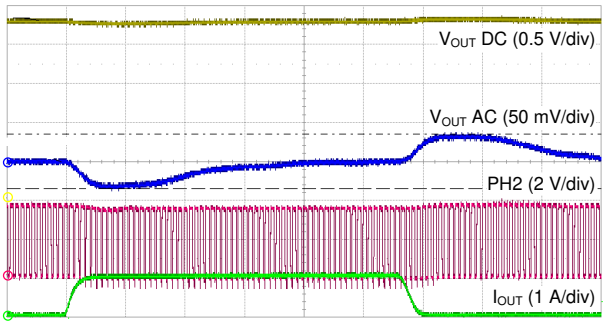
図 12-26. BUCK2 Load Transient



注

V_{OUT} (V_{BUCK2}) = 1.8 V
V_{BUCK1} = 3.6 V
T_R = T_F = 1 µs
I_{OUT} = 0 A to 1 A

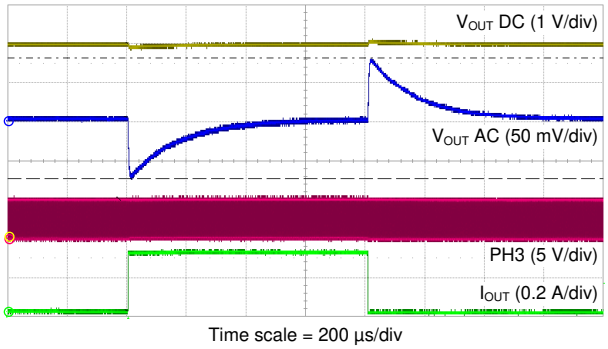
図 12-27. BUCK2 Load Transient



注

V_{OUT} (V_{BUCK2}) = 2.3 V
V_{BUCK1} = 3.6 V
T_R = T_F = 1 µs
I_{OUT} = 0 A to 1 A

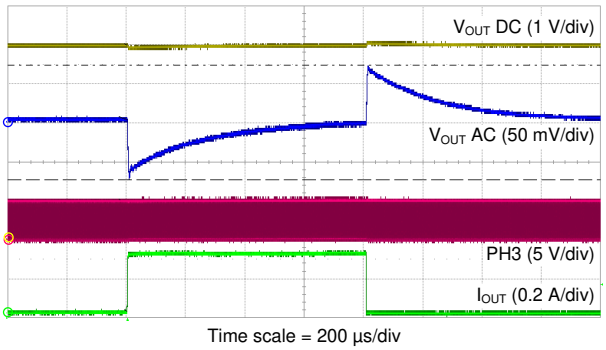
図 12-28. BUCK2 Load Transient



注

V_{OUT} (V_{BOOST}) = 5 V
V_{BUCK1} = 3.3 V
T_R = T_F = 1 µs
I_{OUT} = 0 A to 0.6 A

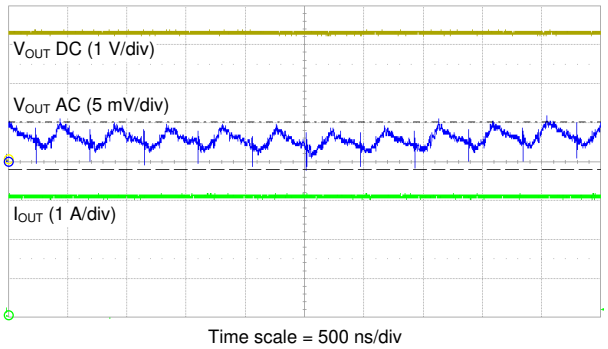
図 12-29. BOOST Load Transient



注

V_{OUT} (V_{BOOST}) = 5 V
V_{BUCK1} = 3.6 V
T_R = T_F = 1 µs
I_{OUT} = 0 A to 0.6 A

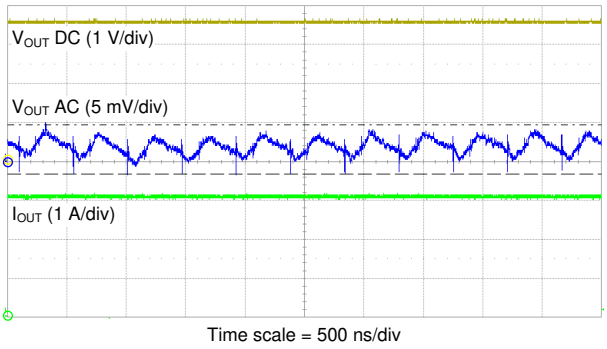
図 12-30. BOOST Load Transient



注

V_{OUT} (V_{BUCK1}) = 3.3 V
I_{OUT} = 3.1 A

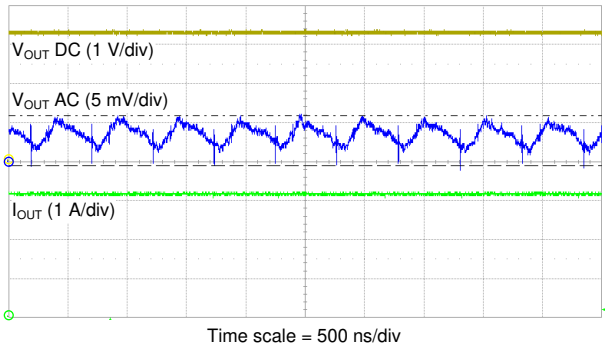
図 12-31. BUCK1 Output Voltage Ripple



注

VOUT (VBUCK1) = 3.6 V　　IOUT = 3.1 A

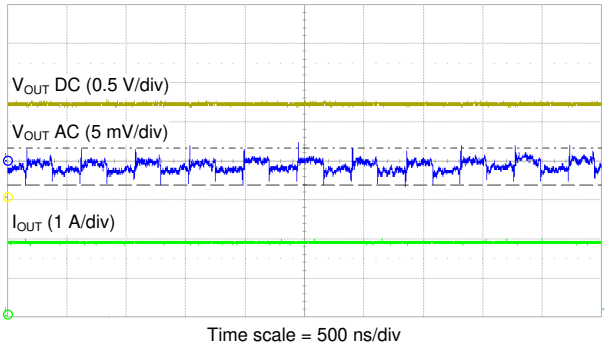
図 12-32. BUCK1 Output Voltage Ripple



注

VOUT (VBUCK1) = 3.3 V　SSM Enabled　IOUT = 3.1 A

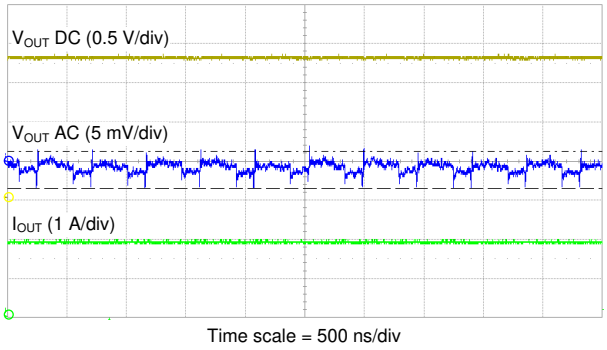
図 12-33. BUCK1 Output Voltage Ripple



注

VOUT (VBUCK2) = 1.2 V　VBUCK1 = 3.3 V　IOUT = 2 A

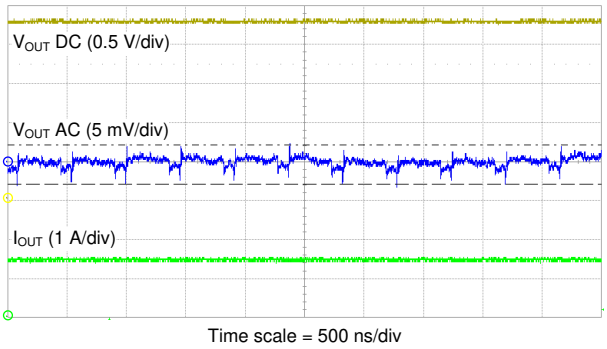
図 12-34. BUCK2 Output Voltage Ripple



注

VOUT (VBUCK2) = 1.8 V　VBUCK1 = 3.3 V　IOUT = 2 A

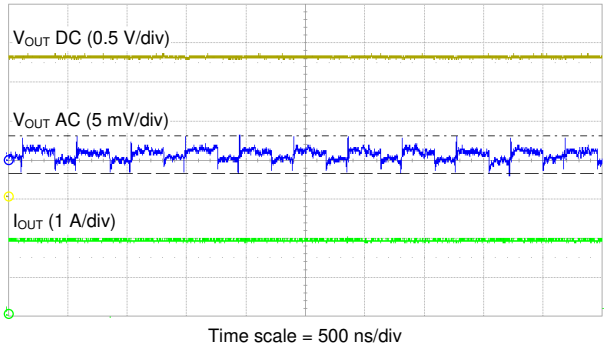
図 12-35. BUCK2 Output Voltage Ripple



注

VOUT (VBUCK2) = 2.3 V　VBUCK1 = 3.3 V　IOUT = 1.5 A

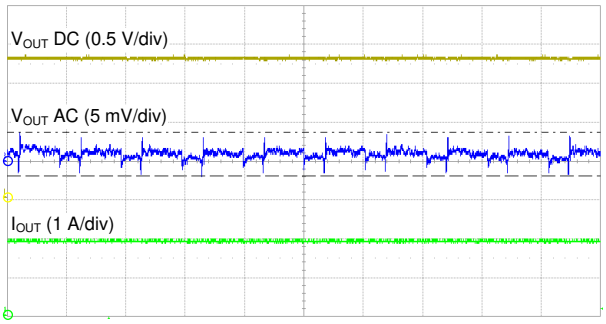
図 12-36. BUCK2 Output Voltage Ripple



注

VOUT (VBUCK2) = 1.8 V　VBUCK1 = 3.6 V　IOUT = 2 A

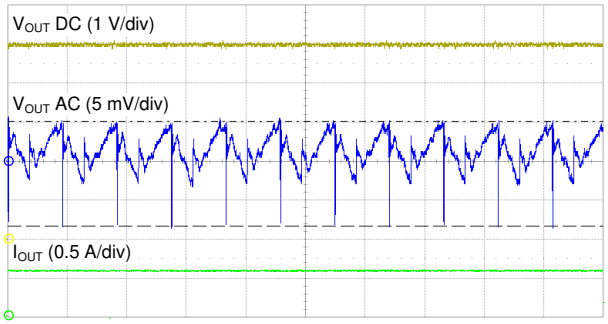
図 12-37. BUCK2 Output Voltage Ripple



注

V_{OUT} (V_{BUCK2}) = 1.8 V SSM Enabled I_{OUT} = 2 A
V_{BUCK1} = 3.3 V

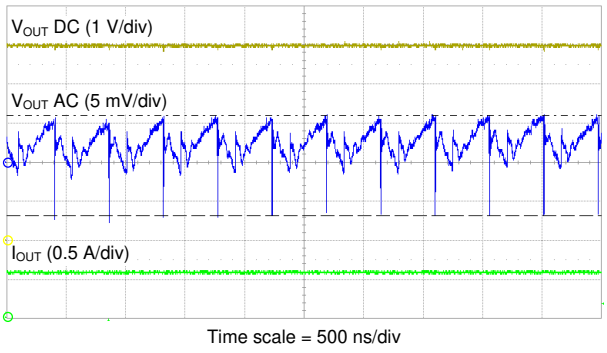
図 12-38. BUCK2 Output Voltage Ripple



注

V_{OUT} (V_{BOOST}) = 5 V V_{BUCK1} = 3.3 V I_{OUT} = 0.6 A

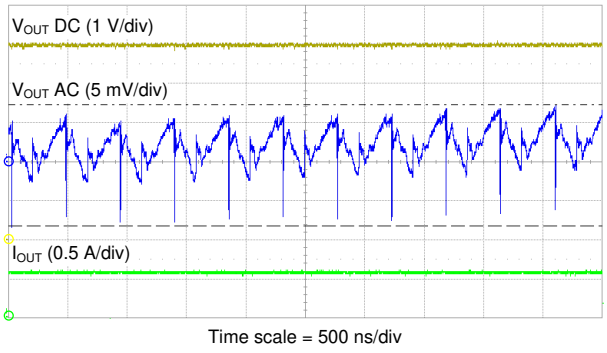
図 12-39. BOOST Output Voltage Ripple



注

V_{OUT} (V_{BOOST}) = 5 V V_{BUCK1} = 3.6 V I_{OUT} = 0.6 A

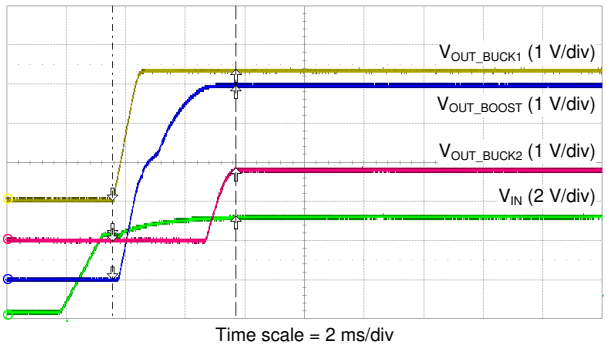
図 12-40. BOOST Output Voltage Ripple



注

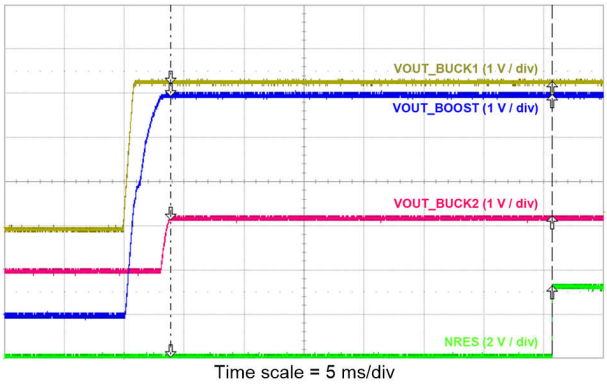
V_{OUT} (V_{BOOST}) = 5 V SSM Enabled I_{OUT} = 0.6 A
V_{BUCK1} = 3.3 V

図 12-41. BOOST Output Voltage Ripple



注

図 12-42. Start-up With V_{IN} and WAKE Connected Together



注

図 12-43. Start-up Showing NRES Output With Long NRES Extension Delay

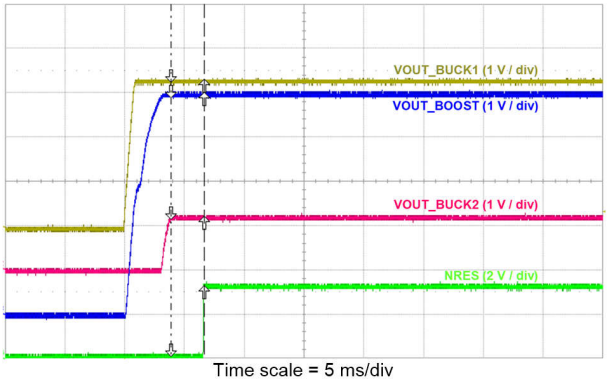
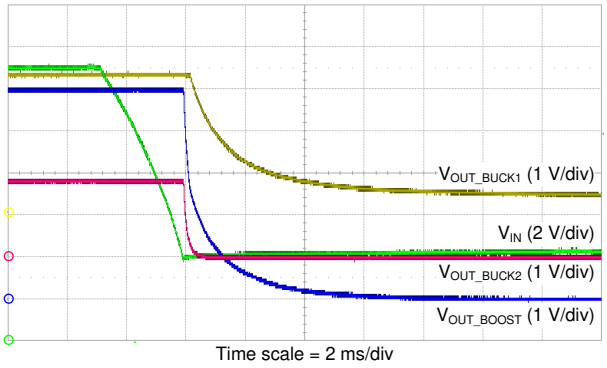


図 12-44. Start-up Showing NRES Output With Short NRES Extension Delay



注

図 12-45. Shutdown With V_{IN}

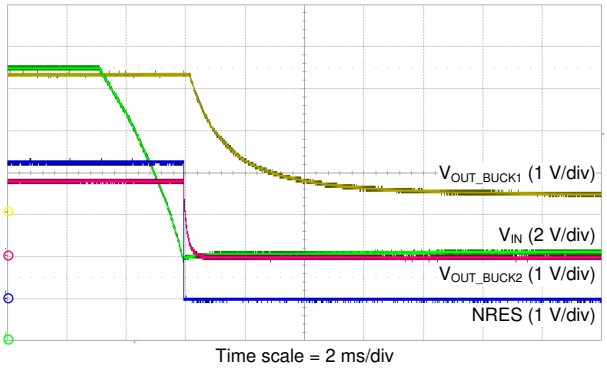


図 12-46. Shutdown Showing NRES Output

12.2.4 Layout

12.2.4.1 Layout Guidelines

Layout is a very important part of good power-supply design. Several signal paths conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. Layout Example shows the PCB layout example. Obtaining acceptable performance with alternate PCB layouts may be possible.

In Layout Example, layout was optimized with the guidelines that follow:

- Provide a low-inductance, low-impedance supply and ground path which are critical. Route the input supply line (VIN plane) with a wide trace to minimize the trace impedance.
- Place the VIN input filter capacitors (C5, C6, and C19) very close to the device. Place the high frequency capacitor (C19) as close to the device pin as possible. A large PGND plane minimizes the parasitics of the input capacitor ground connection. A solid PGND ground plane on the second layer further minimizes the PGND plane impedance.
- Place the AVIN pin filter capacitor (C1) very close to the pin with a short connection to the AGND pin.
- Place the BUCK1 output capacitors (C8 and C9) close to the input capacitors and device PGND pin. Connect these capacitors with a large ground plane through multiple vias to reduce the switching loop impedance.
- Route the PH1 signal in an inner layer to minimize the emission from the switching plane. Use multiple vias to minimize the impedance of the PH1 power path.
- Route the BUCK2 input supply line (VSUP2) with a wide trace to minimize the trace impedance.
- Place the VSUP2 input filter capacitors (C10 and C20) very close to the device. Place the high frequency capacitor (C20) as close to the device pin as possible. A large PGND plane minimizes the parasitics of the input capacitor ground connection.

- Place the BUCK2 output capacitors (C12 and C13) close to the input capacitors and device PGND pin. Connect these capacitors with a large ground plane through multiple vias to decrease the switching loop impedance.
- Route the PH2 signal in an inner layer to minimize the emission from the switching plane. Use multiple vias to minimize the impedance of the PH2 power path.
- Route the BOOST supply line with a wide trace to minimize the trace impedance.
- Place the BOOST input capacitors (C14 and C21) and output capacitors (C6 and C17) very close to each other with short ground connections to minimize loop impedance.
- Route the PGND3 connection with a wide trace and multiple vias to minimize the impedance between the ground of the BOOST input and BOOST output capacitors and the device PGND3 pin.
- Route the PH3 signal with minimal loop area to minimize the emission from the switching plane. Use a wide trace to minimize the impedance for the PH3 power path.
- Place the VREG pin capacitor (C4) as close as possible to the VREG pin. Connect the ground pad of the capacitor to a solid ground plane to minimize the loop impedance.
- Connect all PBKGx, AGND,DGND, and PGNDx pins together at the device thermal pad to make a star connection below the device thermal pad.
- Connect the device thermal pad to the solid ground plane through multiple thermal vias to improve the thermal conductivity.
- Place the BOOT1, BOOT2, and BOOT3 capacitors on the bottom layer with two vias on each pin to minimize the parasitic impedance in the BOOTx path.
- Route the VSENSEx signals away from the switching node with minimum interaction with any noise sources associated with the switching components.

12.2.4.2 Layout Example

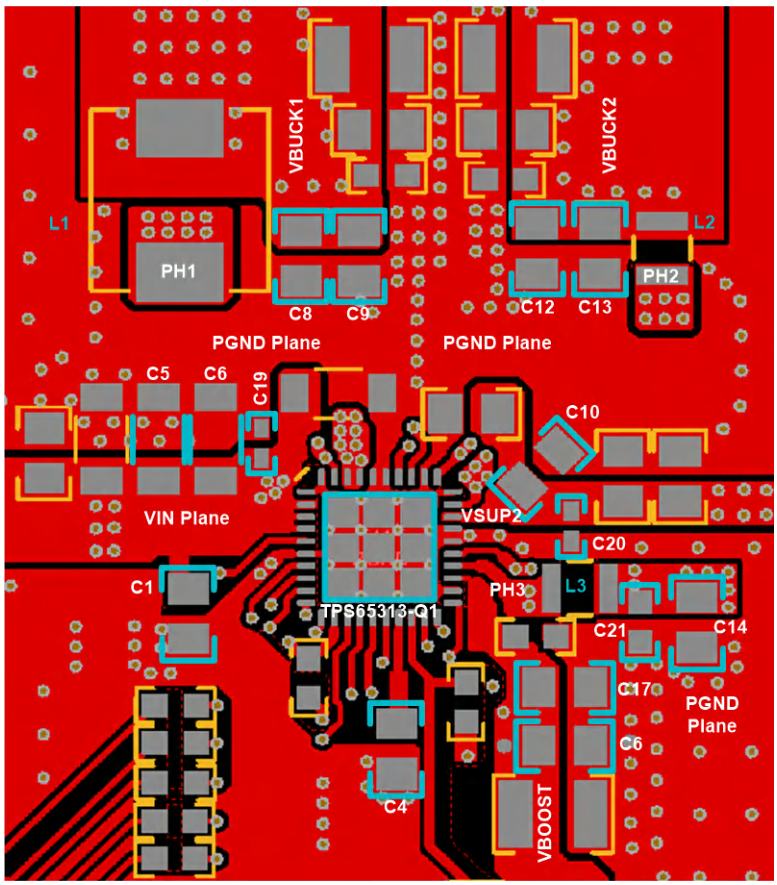


図 12-47. Layout Example

12.2.4.3 Considerations for Board-Level Reliability (BLR)

The TPS65313-Q1 device is packaged in a 40-pin, VQFN package with a higher coefficient of thermal expansion (CTE) mold compound to provide less CTE mismatch with the PCB, resulting in improved board level reliability (BLR) and thermal performance. PCB thickness, copper layer count, copper layer thickness, and area density are significant factors in solder joint reliability.

To achieve good performance, follow these precautions:

- Solder joints must have sufficient thickness for better solder joint reliability. TI recommends having at least 50 µm of thickness for the finished solder joint of this device.
- Avoid conformal coating under the device to avoid excessive solder joint stress caused by the expansion and contraction of these material across temperature and aging.
- Avoid use of solder-mask-defined (SMD) land pad designs. Always use non-solder-mask-defined (NSMD) land pad designs for leadless packages.
- Bonding the PCB to the Aluminium housing or back planes to act as a heat sink to the device can cause significant stress on the solder joint because of the CTE mismatch between the heat sink and the device mold compound.
- Avoid bonding heat sinks to top of QFN packages. The load imposed by the heat sink can have a negative effect on the creep performance of the solder joints. If heat sink cannot be avoided because of thermal reasons, a non-hardening, special thermal gel should be used to minimize the CTE mismatch between the device and the heat sink.
- PCB housing or connectors can cause stress on the device solder joints and solder joints of large package-size components (such as input capacitors, output capacitors, and inductors).Therefore, effects of housing and connectors on the PCB should be reduced.
- Temperature cycling test profiles with very a fast temperature ramp rate (for example, greater than 20°C/minute to 25°C/minute) leads to early solder joints failures and are not realistic or useful for acceleration-factor-based life calculations of solder joints. A temperature ramp rate of approximately 10°C/minute to 15°C/minute is more realistic. For more information, refer to the IPC-SM-785 guidelines.

注

Users should evaluate their application conditions and make sure that the device meets their BLR requirements.

12.3 Power Supply Coupling and Bulk Capacitors

The device is designed to operate from an input voltage supply range from 4 V to 36 V. This input supply must be well regulated. If the supply voltage in the application is likely to reach negative voltage (for example, reverse battery in automotive applications), a forward diode must be placed between the power supply and VIN pins. The BUCK1 output voltage is the recommended input supply for the BUCK2 regulator and BOOST converter. Select the input filter capacitors based on the recommendation in セクション 12.2.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS65313Q1E1 EVM User's Guide*
- Texas Instruments, *TPS65313-Q1 Functional Safety Manual*
- Texas Instruments, *TPS65313-Q1 EMC Evaluation Report*

13.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

13.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

13.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

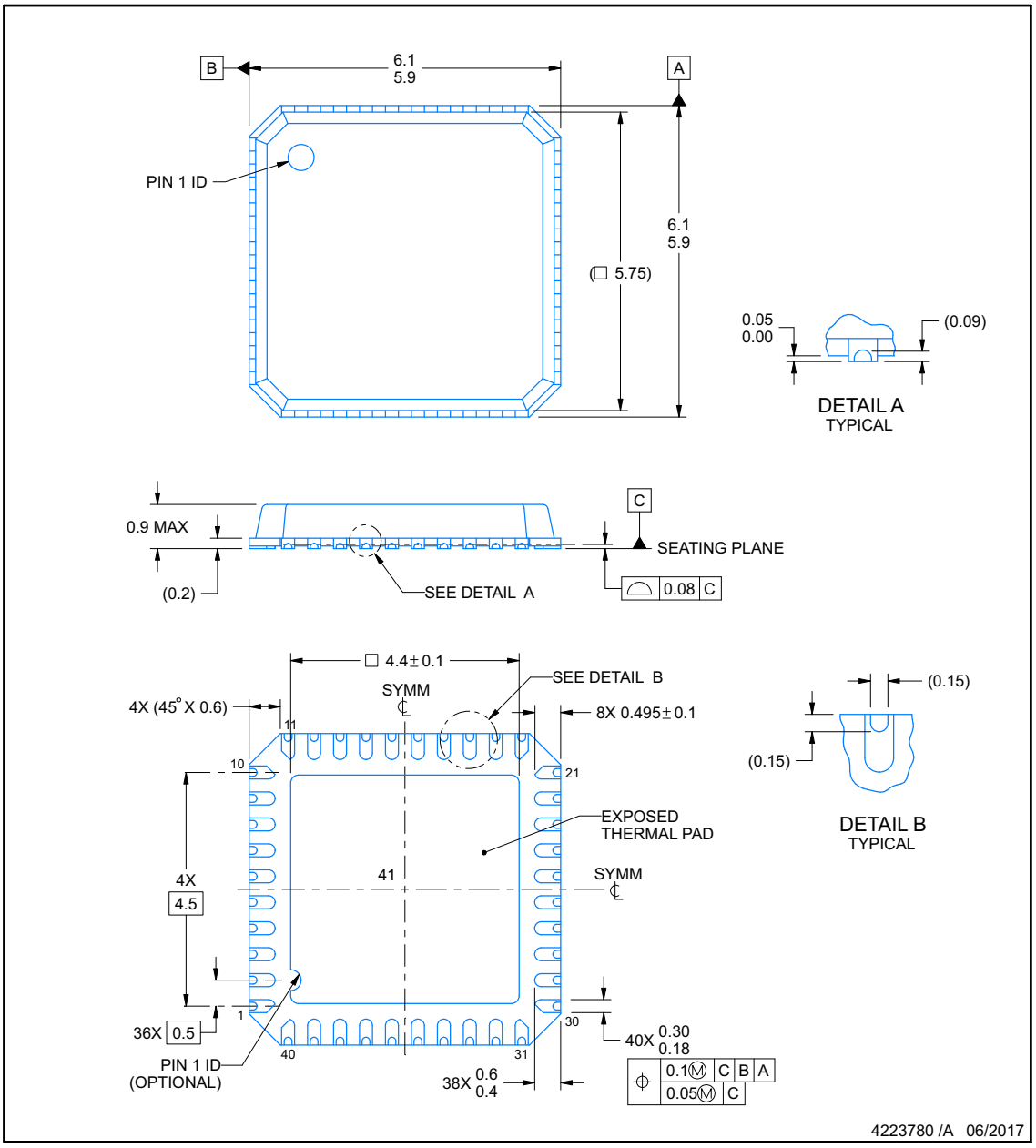
For the device mechanical, packaging, and orderable information, refer to the *Mechanical, Packaging, and Orderable Information* section of the data sheet available in the TPS65313-Q1 product folder.

PACKAGE OUTLINE

RWG0040B

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



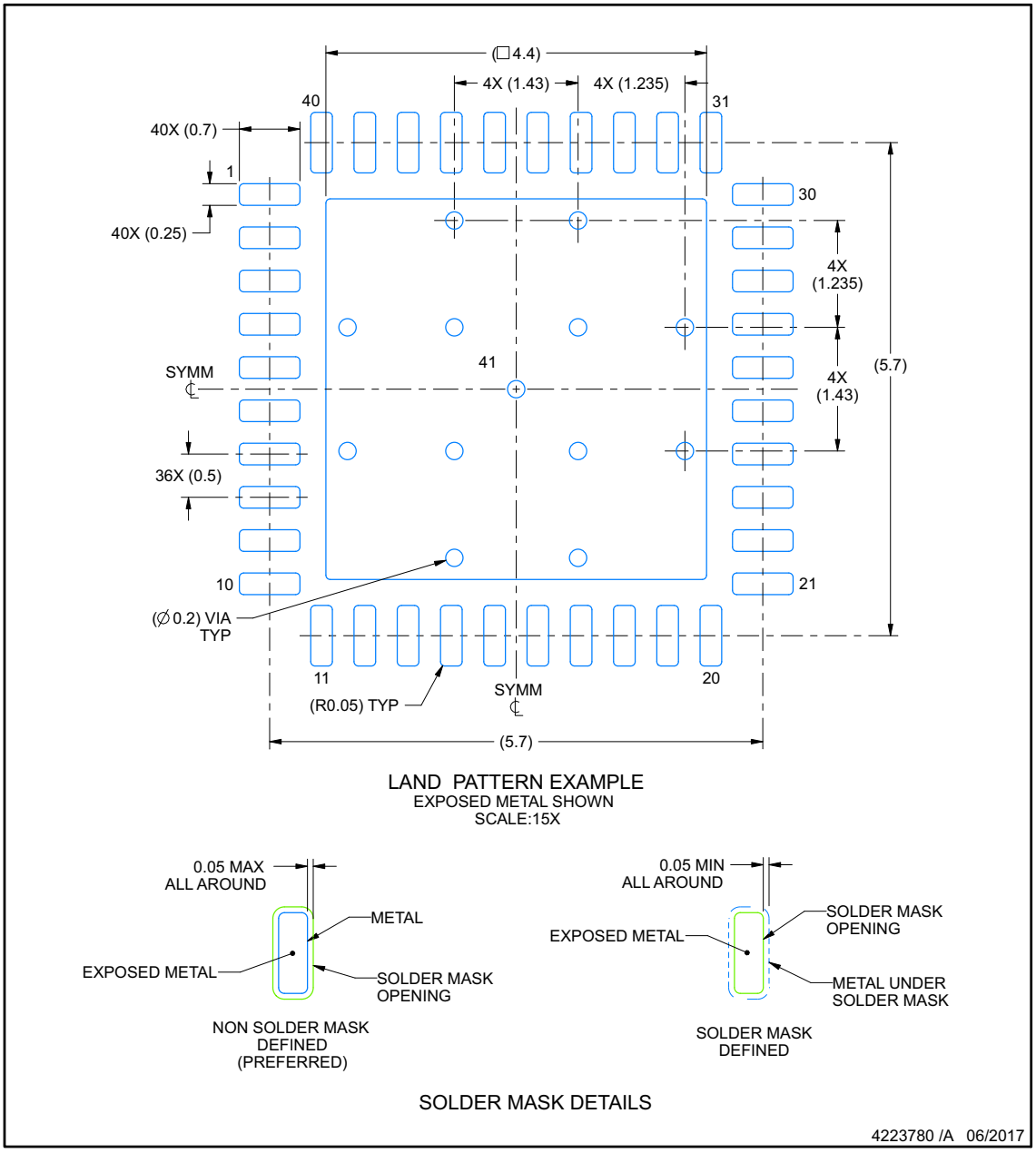
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RWG0040B — **VQFNP - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

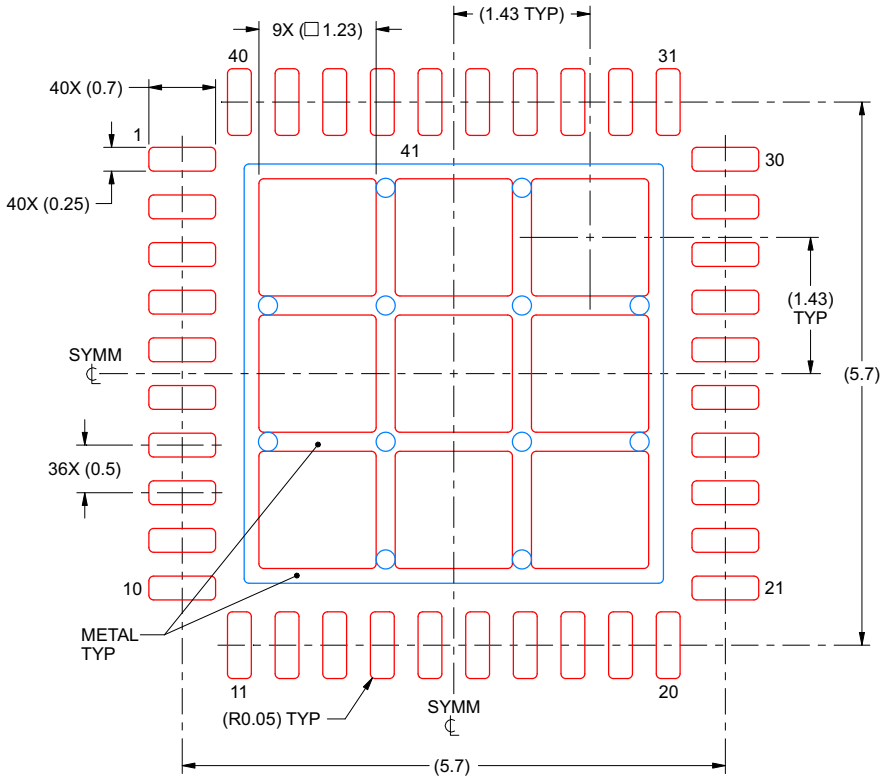
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RWG0040B

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 41: 70%
SCALE:15X

4223780 /A 06/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
O31310QRWGRQ1	Active	Production	VQFNP (RWG) | 40	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS653 1310
O31310QRWGRQ1.A	Active	Production	VQFNP (RWG) | 40	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS653 1310

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

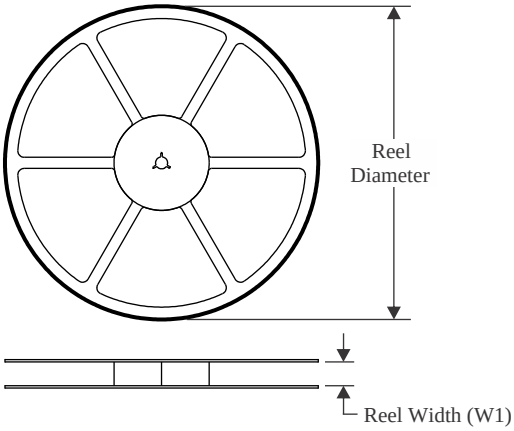
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

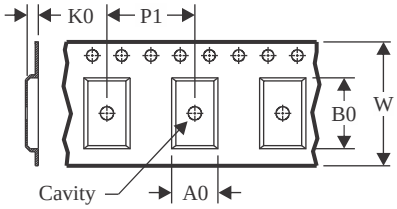
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

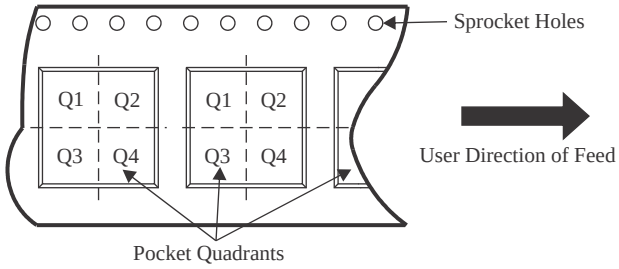


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

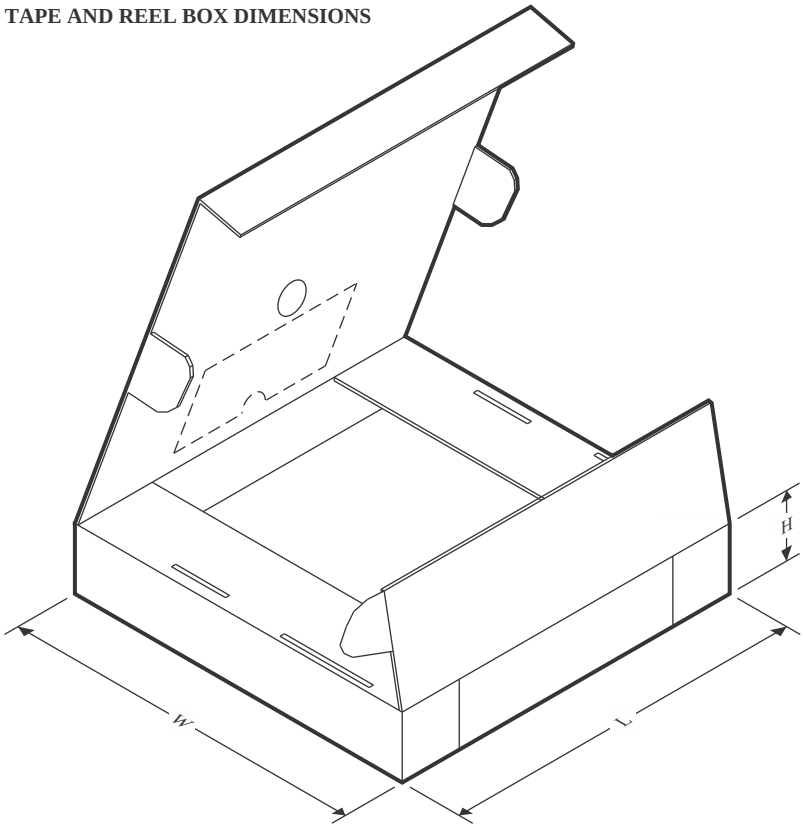
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
O31310QRWGRQ1	VQFNP	RWG	40	2000	330.0	16.4	6.3	6.3	1.3	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

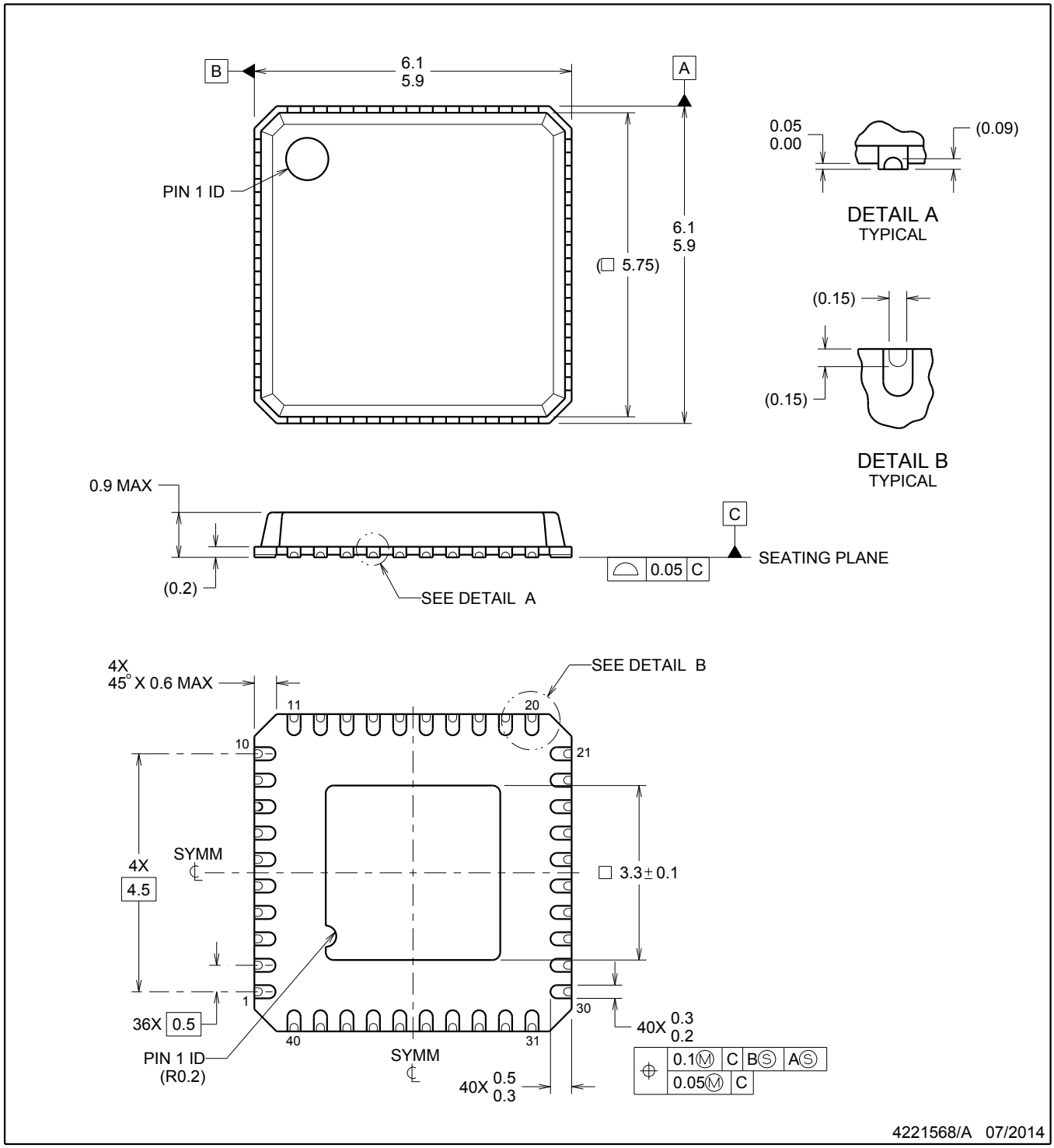
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
O31310QRWGRQ1	VQFNP	RWG	40	2000	350.0	350.0	43.0

PACKAGE OUTLINE

RWG0040A

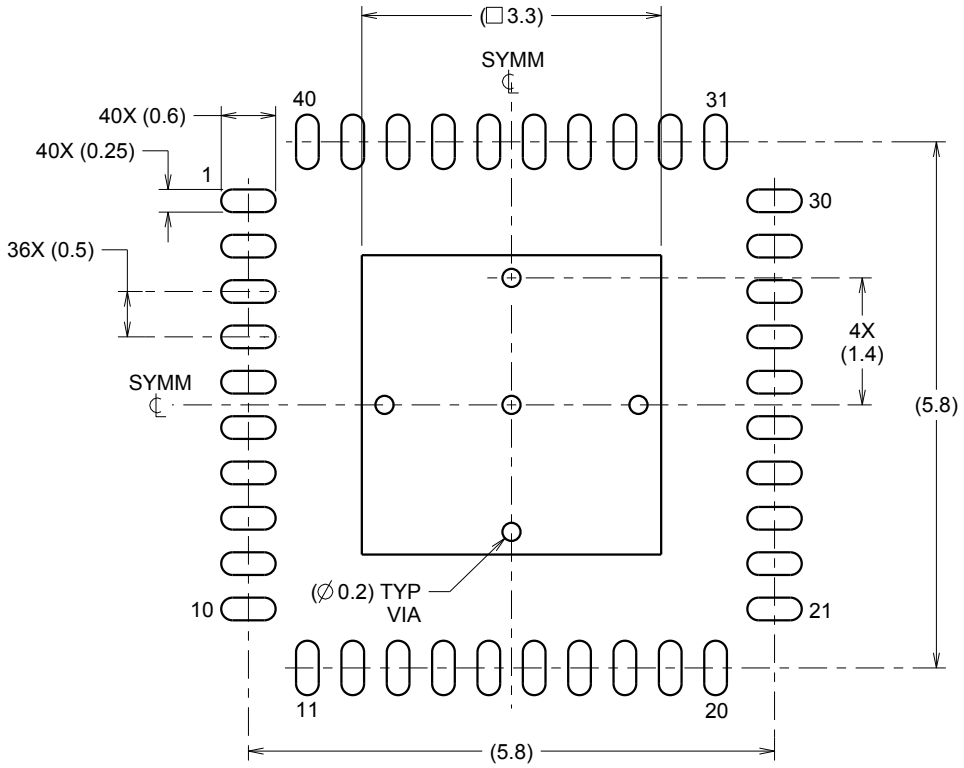
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

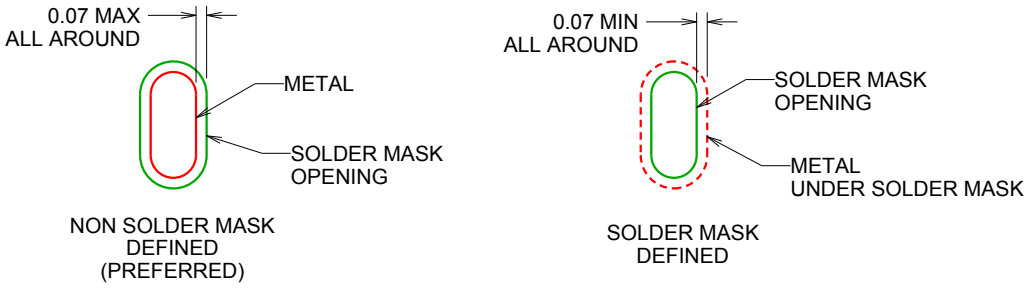


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

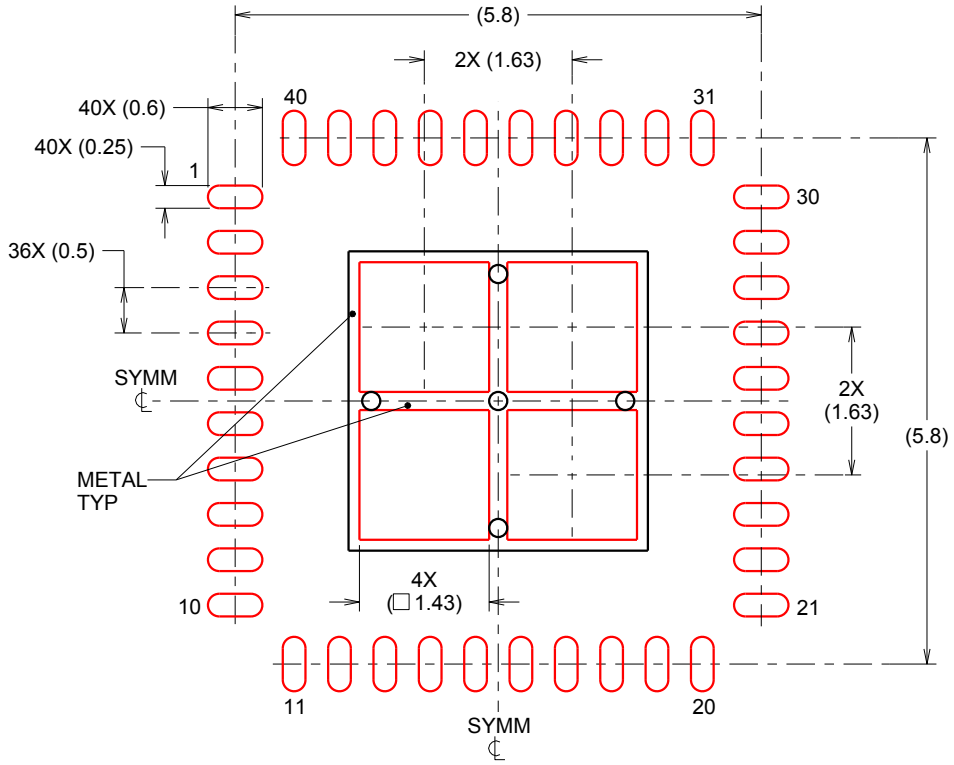


SOLDER MASK DETAILS

4221568/A 07/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

4221568/A 07/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月