AMD™ ファミリー 17h モデル 10h-1Fh プロセッサ向け TPS6508700 PMIC

1 特長

- 5.6V～21V の広い V_{IN} 範囲
- D-CAP2™ トポロジを採用した 3 つの可変出力電圧同期整流
  降圧型コントローラ
  - 外付け FET を使用して出力電流をスケーリング可能、電流制限を選択可能
  - IBUCK2 および BUCK6 向け I^2C 動的電圧スケーリング (DVS) 制御、BUCK1 向け外部フィードバック
- 出力電圧可変の 3 つの同期整流降圧型コンバータ (DCS-Control™トポロジ使用および I^2C DVS 機能搭載)
  - V_{IN} 範囲：4.5 V～5.5V
  - V_{OUT} 範囲：0.425 V～3.575V
  - 最大 3A の出力電流
- 出力電圧可変の 3 つの LDO レギュレータ
  - LDOA1：I^2C により、出力電圧を 1.35V～3.3V の範囲で選択可能、最大出力電流 200mA
  - LDOA2 および LDOA3：I^2C により、出力電圧を 0.7V～1.5V の範囲で選択可能、最大出力電流 600mA
- BUCK6 を入力電圧とする LDO
- スルー レート制御付きの 3 つの負荷スイッチ
  - 最大 300mA の出力電流、電圧降下は公称入力電圧の 1.5% 未満
  - 入力電圧 1.8V において R_{DSON} < 96mΩ
- 5V 固定出力電圧の LDO (LDO5)
  - SMPS のゲートドライバおよび LDOA1 用の電源
  - 5V 降圧への自動切り替えにより高効率を実現
- 工場出荷時の OTP プログラミングによる内蔵型シーケンシング
  - CTL1、CTL4、CTL5 を G3'、G3、S5、S0 状態の選択に使用
  - GPO1、GPO2 を PG_S0 および PG_S5 に使用
  - オープンドレインの割り込み出力ピン
- I^2C インターフェイスのサポート：
  - Standard mode (100 kHz)
  - Fast mode (400kHz)
  - Fast mode plus (1 MHz)

2 アプリケーション

- 2、3、4 直列セルのリチウムイオン バッテリ駆動製品 (NVDC または非 NVDC)
- 壁面電源を使用する設計、特に 12V 電源を使用する場合
- タブレット、ウルトラブック、ノートブック コンピュータ
- モバイル PC およびモバイル インターネット デバイス

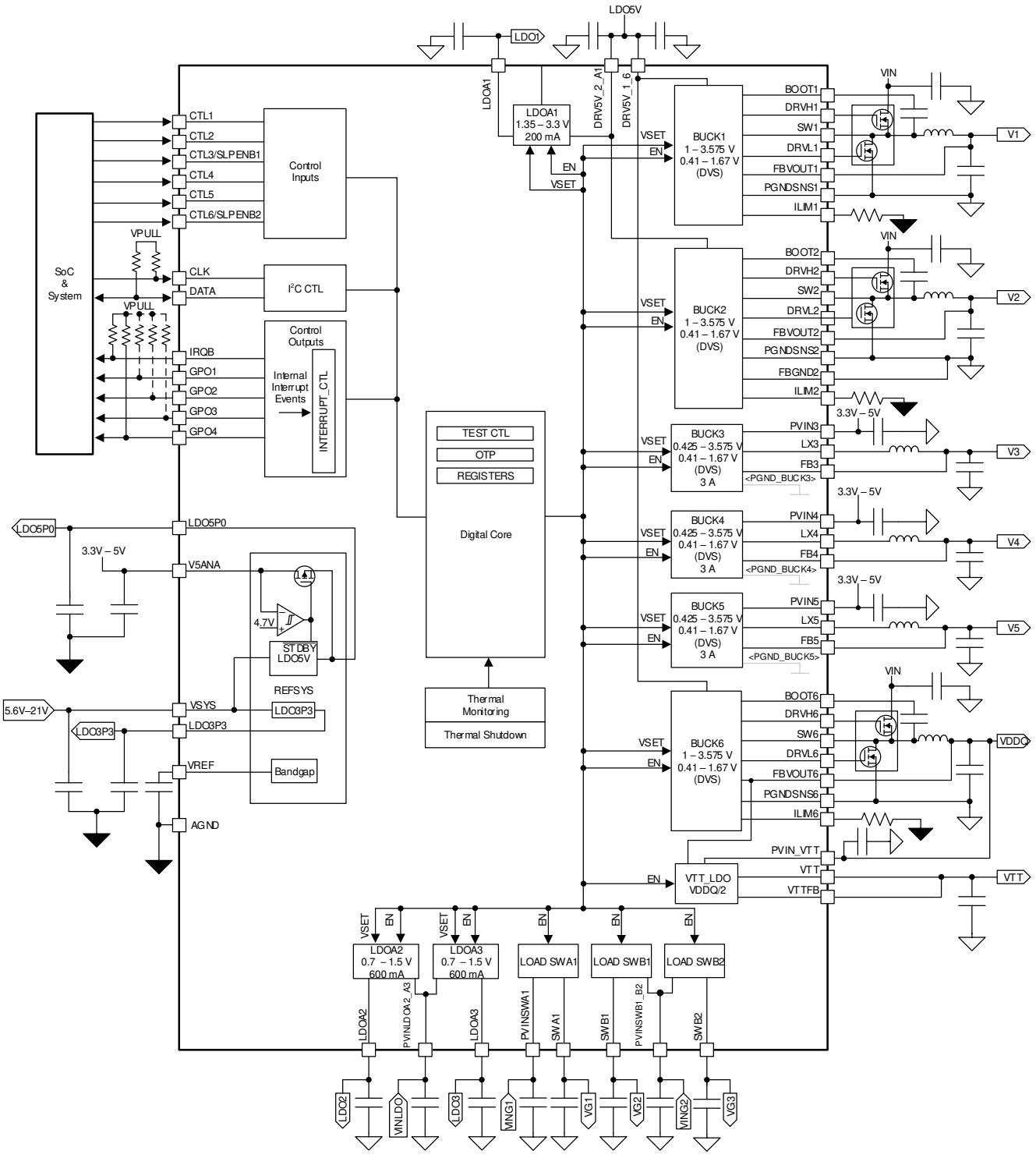
3 概要

TPS6508700 デバイスは、AMD™ファミリー 17h モデル 10h-1Fh プロセッサ用に設計されたシングルチップのパワー マネージメント IC (PMIC) で、ノート PC およびオールインワン デスクトップ PC を対象にしています。TPS6508700 デバイスは、5.6V～21V の入力範囲を提供し、広範なアプリケーションで使用可能です。このデバイスは、2S、3S、または 4S のリチウムイオン バッテリ パックを使用する、NVDC および非 NVDC 電源アーキテクチャに最適です。D-CAP2™ および DCS-Control™ の高周波電圧レギュレータは、小さなインダクタとコンデンサを使用できるため、ソリューションを小型化できます。D-CAP2 および DCS-Control トポロジは過渡応答性能が非常に優れており、高速な負荷切り替えが発生するプロセッサ コアおよびシステム メモリのレールに最適です。I^2C インターフェイスにより、組み込みコントローラ (EC) またはシステム オン チップ (SoC) を使用して簡単に制御できます。この PMIC は、8mm × 8mm、単一列の VQFN パッケージで供給され、放熱特性改善と基板配線の簡略化のためにサーマル パッドが付属します。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS6508700	VQFN (64)	8.00mm × 8.00mm

(1) 詳細については、*メカニカル、パッケージ、および注文情報*を参照してください。



PMIC の機能ブロック図

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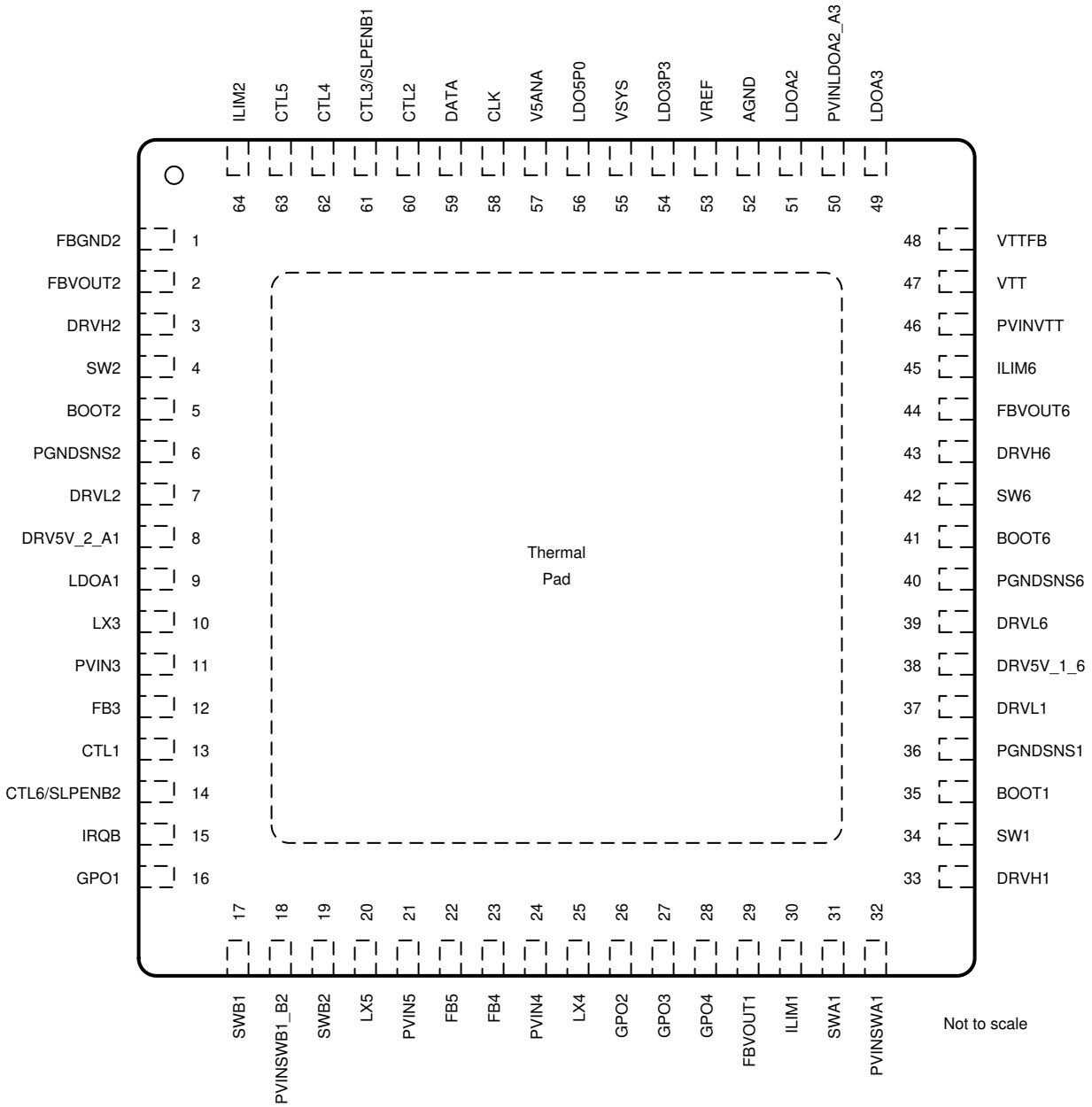
4 Pin Configuration and Functions

図 4-1 shows the 64-pin RSK plastic quad-flatpack no-lead package with exposed thermal pad.



The thermal pad must be connected to the system power ground plane.

図 4-1. 64-pin RSK VQFN (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
ANALOG			
Input voltage from battery, VSYS	–0.3	28	V
PVIN3, PVIN4, PVIN5, LDO5P0, DRV5V_1_6, DRV5V_2_A1, DRVL1, DRVL2, DRVL6	–0.3	7	V
V5ANA	–0.3	6	V
PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2	–0.3	0.3	V
DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6	–0.3	34	V
SW1, SW2, SW6, transient for less than 5ns.	–5	28	V
LX3, LX4, LX5	-0.3	7	V
LX3, LX4, LX5, transient for less than 20ns.	–2	9	V
Differential voltage, BOOTx to SWx	–0.3	5.5	V
VREF, LDO3P3, FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5, ILIM1, ILIM2, ILIM6, PVINVTT, VTT, VTTFB, PVINSWA1, SWA1, PVINSWB1_B2, SWB1, SWB2, LDOA1	–0.3	3.6	V
PVINLDOA2_A3, LDOA2, LDOA3	–0.3	3.3	V
DIGITAL IO			
DATA, CLK, GPO1-GPO3	–0.3	3.6	V
CTL1-CTL6, GPO4, IRQB	–0.3	7	V
CHIP			
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
ANALOG				
VSYS	5.6	13	21	V
VREF	–0.3		1.3	V
PVIN3, PVIN4, PVIN5, LDO5P0, V5ANA, DRV5V_1_6, DRV5V_2_A1	–0.3	5	5.5	V
PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2	–0.3		0.3	V
DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6	–0.3		26.5	v
DRVL1, DRVL2, DRVL6	–0.3		5.5	V
SW1, SW2, SW6	–1		21	V
LX3, LX4, LX5	–1		5.5	V
FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5	–0.3		3.6	V

5.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
LDO3P3, ILIM1, ILIM2, ILIM6, LDOA1	–0.3		3.3	V
PVINVTT	–0.3		FBVOUT6	V
VTT, VTTFB	–0.3		FBVOUT6 / 2	V
PVINSWA1, SWA1	–0.3	3.3	3.6	V
PVINSWB1_B2, PVINLDOA2_A3, SWB1, SWB2	–0.3		1.8	V
LDOA2, LDOA3	–0.3		1.5	V
DIGITAL IO				
DATA, CLK, CTL1–CTL6, GPO1–GPO4, IRQB	–0.3		3.3	V
CHIP				
Operating ambient temperature, T_A	–40	27	85	°C
Operating junction temperature, T_J	–40	27	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS6508700 RSK (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics: Total Current Consumption

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SD}	PMIC shutdown current that includes I_Q for references, LDO5, LDO3P3, and digital core	V_{SYS} = 13V, all functional output rails are disabled		65		µA

5.6 Electrical Characteristics: Reference and Monitoring System

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{REF}	Band-gap reference voltage			1.25		V
	Band-gap reference voltage accuracy		–0.5%		0.5%	
C_{VREF}	Band-gap output capacitor		0.047	0.1	0.22	µF
$V_{SYS\_UVLO\_5V}$	VSYS UVLO threshold for LDO5	V_{SYS} falling	5.24	5.4	5.56	V

5.6 Electrical Characteristics: Reference and Monitoring System (続き)

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SYS\_UVLO\_5V\_HYS}$	VSYS UVLO threshold hysteresis for LDO5	V_{SYS} rising above $V_{SYS\_UVLO\_5V}$		200		mV
$V_{SYS\_UVLO\_3V}$	VSYS UVLO threshold for LDO3P3	V_{SYS} falling	3.45	3.6	3.75	V
$V_{SYS\_UVLO\_3V\_HYS}$	VSYS UVLO threshold hysteresis for LDO3P3	V_{SYS} rising above $V_{SYS\_UVLO\_3V}$		150		mV
T_{CRIT}	Critical threshold of die temperature	T_J rising	130	145	160	°C
T_{CRIT_HYS}	Hysteresis of T_{CRIT}	T_J falling		10		°C
T_{HOT}	Hot threshold of die temperature	T_J rising	110	115	120	°C
T_{HOT_HYS}	Hysteresis of T_{HOT}	T_J falling		10		°C
LDO5						
V_{IN}	Input voltage at V_{SYS} pin		5.6	13	21	V
V_{OUT}	DC output voltage	I_{OUT} = 10mA	4.9	5	5.1	V
I_{OUT}	DC output current			100	180	mA
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	200			mA
V_{TH_PG}	Power good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		94%		
$V_{TH\_PG\_HYS}$	Power good deassertion hysteresis	V_{OUT} rising or falling		4%		
I_Q	Quiescent current	V_{IN} = 13V, I_{OUT} = 0A		20		µA
C_{OUT}	External output capacitance		2.7	4.7	10	µF
V5ANA-to-LDO5P0 LOAD SWITCH						
R_{DSON}	On resistance	V_{IN} = 5V, measured from V5ANA pin to LDO5P0 pin at I_{OUT} = 200mA			1	Ω
V_{TH_PG}	Power good threshold for external 5V supply	V_{V5ANA} rising		4.7		V
$V_{TH\_HYS\_PG}$	Power good threshold hysteresis for external 5V supply	V_{V5ANA} falling		100		mV
I_{LKG}	Leakage current	Switch disabled, V_{V5ANA} = 5V, V_{LDO5} = 0V			10	µA
LDO3P3						
V_{IN}	Input voltage at V_{SYS} pin		5.6	13	21	V
V_{OUT}	DC output voltage	I_{OUT} = 10mA		3.3		V
	DC output voltage accuracy	V_{IN} = 13V, I_{OUT} = 10mA	–3%		3%	
I_{OUT}	DC output current				40	mA
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	70			mA
V_{TH_PG}	Power good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		92%		
$V_{TH\_PG\_HYS}$	Power good deassertion hysteresis	V_{OUT} falling		3%		
I_Q	Quiescent current	V_{IN} = 13V, I_{OUT} = 0A		20		µA

5.6 Electrical Characteristics: Reference and Monitoring System (続き)

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	External output capacitance		2.2	4.7	10	µF

5.7 Electrical Characteristics: Buck Controllers

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK1						
V_{IN}	Power input voltage for external HSD FET		5.6	13	21	V
$V_{FBVOUT1}$	Internal reference regulation voltage	T_A = 25°C	0.392	0.4	0.408	V
I_{LIM_LSD}	Low-side output valley current limit accuracy (programmed by external resistor R_{LIM})		–15%		15%	
I_{LIMREF}	Source current out of ILIM1 pin	T_A = 25°C	45	50	55	µA
V_{LIM}	Voltage at ILIM1 pin	$V_{LIM} = R_{LIM} \times I_{LIMREF}$	0.2		2.25	V
V_{TH_PG}	Power good deassertion threshold in percentage of target V_{FB}	V_{OUT} rising	105.5%	108%	110.5%	
		V_{OUT} falling	89.5%	92%	94.5%	
R_{DSON_DRVH}	Driver DRVH resistance	Source, IDRVH = –50mA		3		Ω
		Sink, IDRVH = 50mA		2		Ω
R_{DSON_DRVL}	Driver DRVL resistance	Source, IDRVL = –50mA		3		Ω
		Sink, IDRVL = 50mA		0.4		Ω
C_{BOOT}	Bootstrap capacitance			100		nF
R_{ON_BOOT}	Bootstrap switch ON resistance				20	Ω
BUCK2, BUCK6						
V_{IN}	Power input voltage for external HSD FET		5.6	13	21	V
V_{OUT}	DC output voltage VID range and options	VID step size = 10mV, BUCKx_VID[6:0] progresses from 0000001b to 1111111b	0.41		1.67	V
		VID step size = 25mV, BUCKx_VID[6:0] progresses from 0000001b to 1111111b	1		3.575	V
	BUCK2 output voltage default	Set by BUCK2_VID[6:0], 10mV step size selected		0.8		V
	BUCK6 output voltage default	Set by BUCK6_VID[6:0], 25mV step size selected		3.3		V
	DC output voltage accuracy	V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3V I_{OUT} = 100mA to 7A	–2%		2%	
	Total output voltage accuracy (DC plus ripple) in DCM	I_{OUT} = 10mA, $V_{OUT} \le$ 1V	–30		40	mV
$SR(V_{OUT})$	Output DVS slew rate	Step size = 10mV	2.5	3.125		mV/µs
		Step size = 25mV	5	6.25		
I_{LIM_LSD}	Low-side output valley current limit accuracy (programmed by external resistor R_{LIM})		–15%		15%	
I_{LIMREF}	Source current out of ILIM1 pin	T_A = 25°C	45	50	55	µA
V_{LIM}	Voltage at ILIM1 pin	$V_{LIM} = R_{LIM} \times I_{LIMREF}$	0.2		2.25	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3V, I_{OUT} = 7A	–0.5%		0.5%	

5.7 Electrical Characteristics: Buck Controllers (続き)

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 13V, V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3V, I_{OUT} = 0A to 7A, referenced to V_{OUT} at I_{OUT} = I_{OUT_MAX}	0%		1%	
V_{TH_PG}	Power good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising	105.5%	108%	110.5%	
		V_{OUT} falling	89.5%	92%	94.5%	
R_{DSON_DRVH}	Driver DRVH resistance	Source, IDRVH = –50mA		3		Ω
		Sink, IDRVH = 50mA		2		Ω
R_{DSON_DRVL}	Driver DRVL resistance	Source, IDRVL = –50mA		3		Ω
		Sink, IDRVL = 50mA		0.4		Ω
R_{DIS}	Output auto-discharge resistance	BUCKx_DIS[1:0] = 01b		100		Ω
		BUCKx_DIS[1:0] = 10b		200		Ω
		BUCKx_DIS[1:0] = 11b		500		Ω
C_{BOOT}	Bootstrap capacitance			100		nF
R_{ON_BOOT}	Bootstrap switch ON resistance				20	Ω

5.8 Electrical Characteristics: Synchronous Buck Converters

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK3, BUCK4, BUCK5						
V_{IN}	Power input voltage		4.5	5	5.5	V
V_{OUT}	DC output voltage VID range and options	VID step size = 25mV, BUCKx_VID[6:0] progresses from 0000001b to 1111111b	0.425		3.575	V
	BUCK3 output voltage default	Set by BUCK3_VID[6:0], 25mV step size		1.8		V
	BUCK4 output voltage default	Set by BUCK4_VID[6:0], 25mV step size		0.8		V
	BUCK5 output voltage default	Set by BUCK5_VID[6:0], 25mV step size		1.8		V
	DC output voltage accuracy	V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3V, I_{OUT} = 1.5A	–2%		2%	
		V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, I_{OUT} = 100mA	–2.5%		2.5%	
	Total output voltage accuracy (DC plus ripple) in DCM	I_{OUT} = 10mA, V_{OUT} ≤ 1V	–30		40	mV
$SR(V_{OUT})$	Output DVS slew rate		5	6.25		mV/µs
I_{OUT}	Continuous DC output current				3	A
I_{IND_LIM}	HSD FET current limit		4.3		7	A
I_Q	Quiescent current	V_{IN} = 5V, V_{OUT} = 1V		35		µA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3V, I_{OUT} = 1.5A	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 5V, V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3V, I_{OUT} = 0A to 3A, referenced to V_{OUT} at I_{OUT} = 1.5A	–0.2%		2%	
V_{TH_PG}	Power good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		3%		

5.8 Electrical Characteristics: Synchronous Buck Converters (続き)

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DIS}	Output auto-discharge resistance	BUCKx_DIS[1:0] = 01b		100		Ω
		BUCKx_DIS[1:0] = 10b		200		
		BUCKx_DIS[1:0] = 11b		500		

5.9 Electrical Characteristics: LDOs

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDOA1						
V_{IN}	Input voltage		4.5	5	5.5	V
V_{OUT}	DC output voltage	Set by LDOA1_VID[3:0]		3.3		
	Accuracy	I_{OUT} = 0 to 200mA	–2%		2%	V
I_{OUT}	DC output current				200	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	I_{OUT} = 40mA	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	I_{OUT} = 10mA to 200mA	–2%		2%	
I_{OCP}	Overcurrent protection	V_{IN} = 5V, Measured with output shorted to ground	500			mA
V_{TH_PG}	Power good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$t_{STARTUP}$	Start-up time	Measured from EN = H to reach 95% of final value, C_{OUT} = 4.7µF			500	µs
I_Q	Quiescent current	I_{OUT} = 0A		23		µA
C_{OUT}	External output capacitance		2.7	4.7	10	µF
	ESR				100	mΩ
R_{DIS}	Output auto-discharge resistance	LDOA1_DIS[1:0] = 01b		100		Ω
		LDOA1_DIS[1:0] = 10b		190		Ω
		LDOA1_DIS[1:0] = 11b		450		Ω
LDOA2 and LDOA3						
V_{IN}	Power input voltage		V_{OUT} + V_{DROP} (1)	1.8	1.98	V
V_{OUT}	LDOA2 DC output voltage	Set by LDOA2_VID[3:0]		1.5		V
	LDOA3 DC output voltage	Set by LDOA3_VID[3:0]		1.2		V
	DC output voltage accuracy	I_{OUT} = 0 to 600mA	–2%		3%	
I_{OUT}	DC output current				600	mA
V_{DROP}	Dropout voltage	V_{OUT} = 0.99 × V_{OUT_NOM}, I_{OUT} = 600mA			350	mV
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	I_{OUT} = 300mA	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	I_{OUT} = 10mA to 600mA	–2%		2%	
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	0.65	1.25		A
V_{TH_PG}	Power good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$t_{STARTUP}$	Start-up time	Measured from EN = H to reach 95% of final value, C_{OUT} = 4.7µF			500	µs
I_Q	Quiescent current	I_{OUT} = 0A		20		µA
LDOA2 and LDOA3 (continued)						
PSRR	Power supply rejection ratio	f = 1kHz, V_{IN} = 1.8V, V_{OUT} = 1.2V, I_{OUT} = 300mA, C_{OUT} = 2.2µF – 4.7µF		48		dB
		f = 10kHz, V_{IN} = 1.8 V, V_{OUT} = 1.2V, I_{OUT} = 300mA, C_{OUT} = 2.2µF – 4.7µF		30		dB

5.9 Electrical Characteristics: LDOs (続き)

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	External output capacitance		2.2	4.7	10	µF
	ESR				100	mΩ
R_{DIS}	Output auto-discharge resistance	LDOAx_DIS[1:0] = 01b		80		Ω
		LDOAx_DIS[1:0] = 10b		180		
		LDOAx_DIS[1:0] = 11b		475		
VTT LDO						
V_{IN}	Power input voltage			1.2	3.3	V
V_{OUT}	DC output voltage	V_{IN} = 1.2V, Measured at VTTFB pin		V_{IN} / 2		V
	DC output voltage accuracy	Relative to V_{IN} / 2, I_{OUT} ≤ 10mA, 1.1V ≤ V_{IN} ≤ 1.35V	–10		10	mV
		Relative to V_{IN} / 2, I_{OUT} ≤ 500mA, 1.1V ≤ V_{IN} ≤ 1.35V	–25		25	
I_{OUT}	DC output current	sink(–) and source(+)	–500		500	mA
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	1.1 V ≤ V_{IN} ≤ 1.35V, I_{OUT} = –500mA to 500mA	–4%		4%	
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	0.95			A
V_{TH_PG}	Power good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		110%		
		V_{OUT} falling		95%		
$V_{TH\_HYS\_PG}$	Power good reassertion hysteresis entering back into V_{TH_PG}			5%		
I_Q	Total ground current	V_{IN} = 1.2V, I_{OUT} = 0A			240	µA
I_{LKG}	OFF leakage current	V_{IN} = 1.2V, disabled			1	µA
C_{IN}	External input capacitance		10			µF
C_{OUT}	External output capacitance		35			µF
R_{DIS}	Output auto-discharge resistance	VTT_DIS = 0b	1000			kΩ
		VTT_DIS = 1b	60	80	100	Ω

(1) It must be equal to or greater than 1.62V.

5.10 Electrical Characteristics: Load Switches

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWA1						
V_{IN}	Input voltage range		0.5	1.5	3.3	V
I_{OUT}	DC output current				300	mA
R_{DSON}	ON resistance	V_{IN} = 1.8V, measured from PVINSWA1 pin to SWA1 pin at I_{OUT} = $I_{OUT,MAX}$		60	93	mΩ
		V_{IN} = 3.3V, measured from PVINSWA1 pin to SWA1 pin at I_{OUT} = $I_{OUT,MAX}$		100	165	
V_{TH_PG}	Power good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		2%		
I_{INRUSH}	Inrush current upon turnon	V_{IN} = 3.3V, C_{OUT} = 0.1µF			10	mA
I_Q	Quiescent current	V_{IN} = 3.3V, I_{OUT} = 0 A		10.5		µA
		V_{IN} = 1.8V, I_{OUT} = 0A		9		

5.10 Electrical Characteristics: Load Switches (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LKG}	Leakage current	Switch disabled, V_{IN} = 1.8V		7	370	nA
		Switch disabled, V_{IN} = 3.3V		10	900	
C_{OUT}	External output capacitance			0.1		µF
R_{DIS}	Output auto-discharge resistance	SWA1_DIS[1:0] = 01		100		Ω
		SWA1_DIS[1:0] = 10		200		
		SWA1_DIS[1:0] = 11		500		
SWB1, SWB2						
V_{IN}	Input voltage range		0.5	1.5	3.3	V
I_{OUT}	DC current per channel				400	mA
R_{DSON}	ON resistance per channel	V_{IN} = 1.8V, measured from PVINSWB1_B2 pin to SWB1/SWB2 pin at I_{OUT} = $I_{OUT,MAX}$		68	92	mΩ
		V_{IN} = 3.3V, measured from PVINSWB1_B2 pin to SWB1/SWB2 pin at I_{OUT} = $I_{OUT,MAX}$		75	125	mΩ
V_{TH_PG}	Power good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		2%		
I_{INRUSH}	Inrush current upon turning on	V_{IN} = 3.3V, C_{OUT} = 0.1µF			10	mA
I_Q	Quiescent current	V_{IN} = 3.3V, I_{OUT} = 0A		10.5		µA
		V_{IN} = 1.8V, I_{OUT} = 0A		9		
I_{LKG}	Leakage current	Switch disabled, V_{IN} = 1.8V		7	460	nA
		Switch disabled, V_{IN} = 3.3V		10	1150	
C_{OUT}	External output capacitance			0.1		µF
R_{DIS}	Output auto-discharge resistance	SWBx_DIS[1:0] = 01		100		Ω
		SWBx_DIS[1:0] = 10		200		
		SWBx_DIS[1:0] = 11		500		

5.11 Digital Signals: I²C Interface

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	V_{PULL_UP} = 1.8V			0.4	V
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
I_{LKG}	Leakage current	V_{PULL_UP} = 1.8V		0.01	0.3	µA
$R_{PULL-UP}$	Pullup resistance	Standard mode			8.5	kΩ
		Fast mode			2.5	
		Fast mode plus			1	
C_{OUT}	Total load capacitance per pin				50	pF

5.12 Digital Input Signals (CTLx)

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.85			V
V_{IL}	Low-level input voltage				0.4	V

5.13 Digital Output Signals (IRQB, GPOx)

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} < 2mA			0.4	V
I_{LKG}	Leakage current	V_{PULL_UP} = 1.8V			0.35	µA

5.14 Timing Requirements

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I²C INTERFACE					
f_{CLK}	Clock frequency (standard mode)			100	kHz
	Clock frequency (fast mode)			400	kHz
	Clock frequency (fast mode plus)			1000	kHz
t_r	Rise time (standard mode)			1000	ns
	Rise time (fast mode)			300	ns
	Rise time (fast mode plus)			120	ns
t_f	Rise time (standard mode)			300	ns
	Rise time (fast mode)			300	ns
	Rise time (fast mode plus)			120	ns

5.15 Switching Characteristics

over operating free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK CONTROLLERS						
t_{PG}	Total turnon time	Measured from enable going high to when output reaches 90% of target value.		550	850	µs
$T_{ON,MIN}$	Minimum on-time of DRVH			50		ns
T_{DEAD}	Driver dead-time	DRVH off to DRVL on		15		ns
		DRVL off to DRVH on		30		ns
f_{SW}	Switching frequency	Continuous-conduction mode, V_{IN} = 13 V, V_{OUT} ≥ 1 V		1000		kHz
BUCK CONVERTERS						
t_{PG}	Total turnon time	Measured from enable going high to when output reaches 90% of target value.		250	1000	µs
f_{SW}	Switching frequency	Continuous-conduction mode, V_{OUT} = 1 V, I_{OUT} = 1 A		1.6		MHz
		Continuous-conduction mode, V_{OUT} = 1.05 V, I_{OUT} = 1 A		1.7		MHz
		Continuous-conduction mode, V_{OUT} = 1.24 V, I_{OUT} = 1 A		1.9		MHz
		Continuous-conduction mode, V_{OUT} = 1.35 V, I_{OUT} = 1 A		2		MHz
		Continuous-conduction mode, V_{OUT} = 1.8 V, I_{OUT} = 1 A		2.5		MHz
LDOAx						

5.15 Switching Characteristics (続き)

over operating free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{STARTUP}$ Start-up time	Measured from enable going high to when output reaches 95% of final value, V_{OUT} = 1.2 V, C_{OUT} = 4.7 µF		180		µs
VTT LDO					
$t_{STARTUP}$ Start-up time	Measured from enable going high to PG assertion, V_{OUT} = 0.675 V, C_{OUT} = 40 µF		22		µs
SWA1					
$t_{TURN-ON}$ Turnon time	Measured from enable going high to reach 95% of final value, V_{IN} = 3.3 V, C_{OUT} = 0.1 µF		0.85		ms
	Measured from enable going high to reach 95% of final value, V_{IN} = 1.8 V, C_{OUT} = 0.1 µF		0.63		ms
SWB1_2					
$t_{TURN-ON}$ Turnon time	Measured from enable going high to reach 95% of final value, V_{IN} = 3.3 V, C_{OUT} = 0.1 µF		1.1		ms
	Measured from enable going high to reach 95% of final value, V_{IN} = 1.8 V, C_{OUT} = 0.1 µF		0.82		ms

5.16 Typical Characteristics

Measurements done at 25°C.

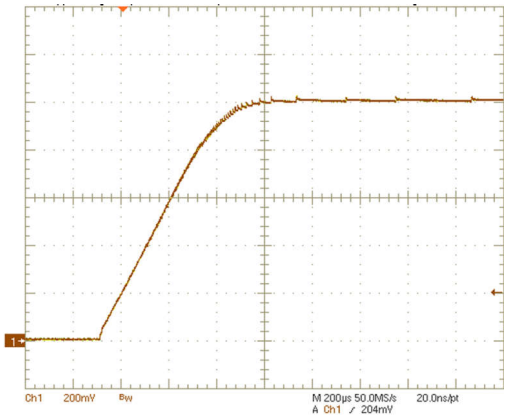


図 5-1. BUCK2 Controller Start Up to 1V by I²C

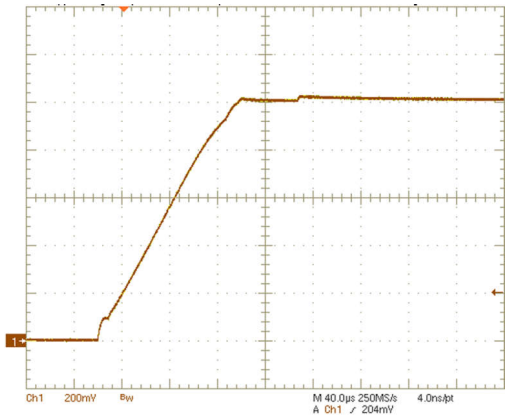


図 5-2. Converter Start Up to 1V by I²C

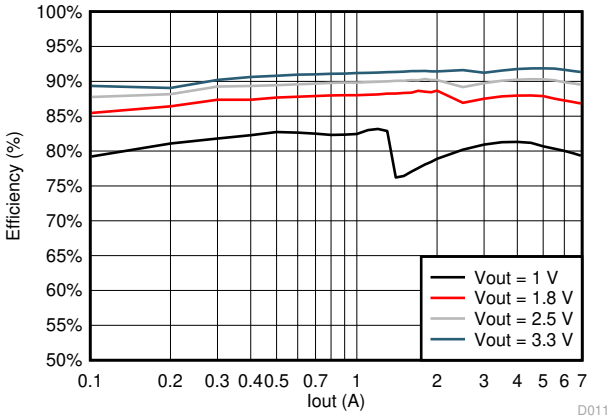


図 5-3. BUCK6 Efficiency at V_{IN} = 13V

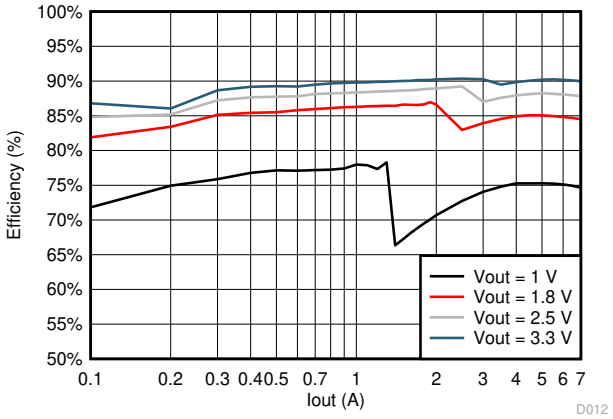


図 5-4. BUCK6 Efficiency at V_{IN} = 18V

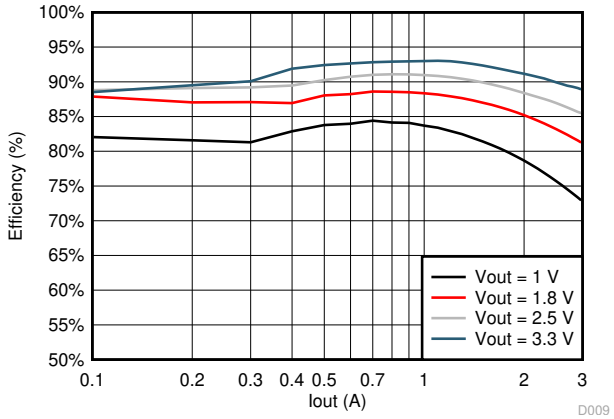


図 5-5. Converter Efficiency at V_{IN} = 5V

6 Detailed Description

6.1 Overview

The TPS6508700 power-management integrated circuit (PMIC) provides all the required power supplies for the AMD Family 17h Models 10h-1Fh Processors. The PMIC has the following integrated components: three step-down controllers (BUCK1, BUCK2, and BUCK6), three step-down converters (BUCK3, BUCK4, and BUCK5), a sink or source LDO (VTT LDO), three low-voltage V_{IN} LDOs (LDOA1–LDOA3), and three load switches (SWA1, SWB1, and SWB2). With on-chip, one-time programmable (OTP) memory, configuration of each rail for the default output value, power-up sequence, fault handling, and power good mapping into a GPO pin are all conveniently flexible. All voltage rails (VRs) have a built-in discharge resistor, and the value can be changed using the DISCHCNT1–DISCHCNT3 and LDOA1_CTRL registers. When enabling a VR, the PMIC automatically disconnects the discharge resistor for that rail without any I^2C command. 表 6-1 lists the key characteristics of the voltage rails.

表 6-1. Summary of Voltage Regulators

RAIL	TYPE	INPUT VOLTAGE (V)		OUTPUT VOLTAGE RANGE (V)			CURRENT (mA)
		MIN	MAX	MIN	TYP	MAX	
BUCK1	Step-down controller	4.5	21		5 V by external feedback		Scalable
BUCK2	Step-down controller	4.5	21	0.41	0.8	1.67	Scalable
BUCK3	Step-down converter	4.5	5.5	0.425	1.8	3.575	3000
BUCK4	Step-down converter	4.5	5.5	0.425	0.8	3.575	3000
BUCK5	Step-down converter	4.5	5.5	0.425	1.8	3.575	3000
BUCK6	Step-down controller	4.5	21	1	3.3	3.575	Scalable
LDOA1	LDO	4.5	5.5	1.35	3.3	3.3	200(1)
LDOA2	LDO	1.62	1.98	0.7	1.5	1.5	600
LDOA3	LDO	1.62	1.98	0.7	1.2	1.5	600
SWA1	Load switch	0.5	3.3		1.5		300
SWB1/SWB2	Load switch	0.5	3.3		1.5		300
VTT	Sink and Source LDO	BUCK6 output			V_{BUCK6} / 2		

(1) When powered from a 5-V supply through the DRV5V_2_A1 pin. Otherwise, max current is limited by max I_{OUT} of LDO5.

6.2 Functional Block Diagram

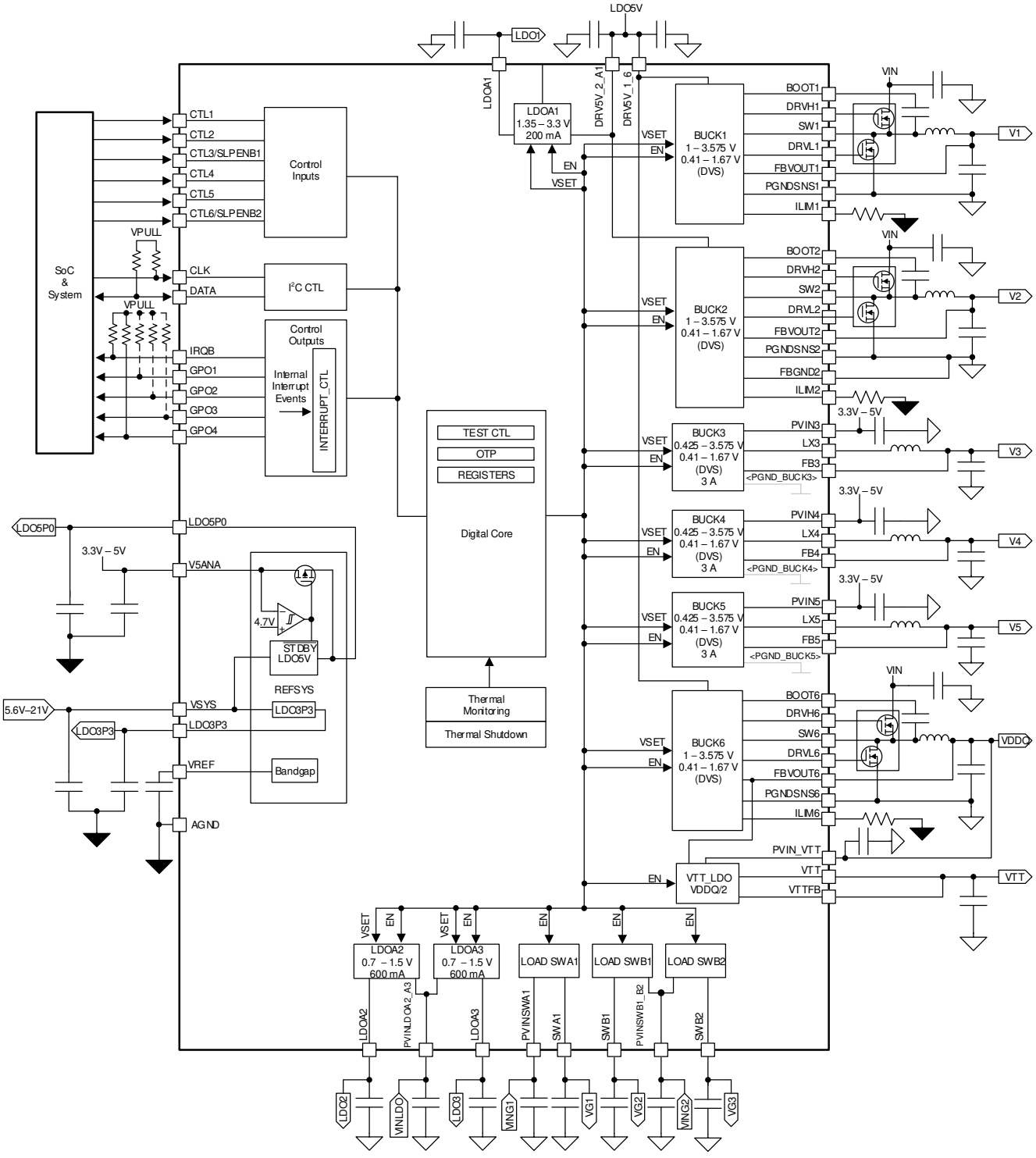


図 6-1. PMIC Functional Block Diagram

6.3 SMPS Voltage Regulators

The buck controllers integrate gate drivers for external power stages with a programmable current limit (set by an external resistor at ILIMx pin), which allows for optimal selection of external passive components based on the desired system load. The buck converters include an integrated power stage and require a minimum number of pins for power input, inductor, and output voltage feedback input. Combined with high-frequency switching, all these features allow the use of inductors in a small form factor, reducing total-system cost and size.

BUCK1–BUCK6 have selectable auto-PWM and forced-PWM mode through the BUCKx_MODE bit in the BUCKxCTRL register. In default auto-PWM mode, the VR automatically switches between pulse width modulation (PWM) and pulse frequency modulation (PFM) depending on the output load to maximize efficiency.

All controllers and converters can be set to the default output voltage (V_{OUT}) or dynamically voltage changing at any time. This feature means that the rails can be programmed for any V_{OUT} by the factory, therefore the device starts up with the default voltage, or during operation the rail can be programmed to another operating V_{OUT} while the rail is enable or disabled. Two step sizes, or ranges, are available for V_{OUT} selection: 10-mV steps and 25-mV steps. The step-size range must be selected prior to use and must be programmed by the factory. The step-size range is not subject to programming or change during operation.

表 6-2 lists the options for the 10-mV step-size range V_{OUT}. 表 6-3 lists the options for the 25-mV step-size range V_{OUT}.

表 6-2. 10-mV Step-Size V_{OUT} Range

VID BITS	V_{OUT}	VID BITS	V_{OUT}	VID BITS	V_{OUT}
0000000b	0	0101011b	0.83	1010110b	1.26
0000001b	0.41	0101100b	0.84	1010111b	1.27
0000010b	0.42	0101101b	0.85	1011000b	1.28
0000011b	0.43	0101110b	0.86	1011001b	1.29
0000100b	0.44	0101111b	0.87	1011010b	1.30
0000101b	0.45	0110000b	0.88	1011011b	1.31
0000110b	0.46	0110001b	0.89	1011100b	1.32
0000111b	0.47	0110010b	0.90	1011101b	1.33
0001000b	0.48	0110011b	0.91	1011110b	1.34
0001001b	0.49	0110100b	0.92	1011111b	1.35
0001010b	0.50	0110101b	0.93	1100000b	1.36
0001011b	0.51	0110110b	0.94	1100001b	1.37
0001100b	0.52	0110111b	0.95	1100010b	1.38
0001101b	0.53	0111000b	0.96	1100011b	1.39
0001110b	0.54	0111001b	0.97	1100100b	1.40
0001111b	0.55	0111010b	0.98	1100101b	1.41
0010000b	0.56	0111011b	0.99	1100110b	1.42
0010001b	0.57	0111100b	1.00	1100111b	1.43
0010010b	0.58	0111101b	1.01	1101000b	1.44
0010011b	0.59	0111110b	1.02	1101001b	1.45
0010100b	0.60	0111111b	1.03	1101010b	1.46
0010101b	0.61	1000000b	1.04	1101011b	1.47
0010110b	0.62	1000001b	1.05	1101100b	1.48
0010111b	0.63	1000010b	1.06	1101101b	1.49
0011000b	0.64	1000011b	1.07	1101110b	1.50
0011001b	0.65	1000100b	1.08	1101111b	1.51
0011010b	0.66	1000101b	1.09	1110000b	1.52
0011011b	0.67	1000110b	1.10	1110001b	1.53

表 6-2. 10-mV Step-Size V_{OUT} Range (続き)

VID BITS	V_{OUT}	VID BITS	V_{OUT}	VID BITS	V_{OUT}
0011100b	0.68	1000111b	1.11	1110010b	1.54
0011101b	0.69	1001000b	1.12	1110011b	1.55
0011110b	0.70	1001001b	1.13	1110100b	1.56
0011111b	0.71	1001010b	1.14	1110101b	1.57
0100000b	0.72	1001011b	1.15	1110110b	1.58
0100001b	0.73	1001100b	1.16	1110111b	1.59
0100010b	0.74	1001101b	1.17	1111000b	1.60
0100011b	0.75	1001110b	1.18	1111001b	1.61
0100100b	0.76	1001111b	1.19	1111010b	1.62
0100101b	0.77	1010000b	1.20	1111011b	1.63
0100110b	0.78	1010001b	1.21	1111100b	1.64
0100111b	0.79	1010010b	1.22	1111101b	1.65
0101000b	0.80	1010011b	1.23	1111110b	1.66
0101001b	0.81	1010100b	1.24	1111111b	1.67
0101010b	0.82	1010101b	1.25	—	—

表 6-3. 25-mV Step-Size V_{OUT} Range

VID BITS	V_{OUT} (Converters)	V_{OUT} (Controllers)	VID BITS	V_{OUT}	VID BITS	V_{OUT}
0000000b	0	1.000	0101011b	1.475	1010110b	2.550
0000001b	0.425	1.000	0101100b	1.500	1010111b	2.575
0000010b	0.450	1.000	0101101b	1.525	1011000b	2.600
0000011b	0.475	1.000	0101110b	1.550	1011001b	2.625
0000100b	0.500	1.000	0101111b	1.575	1011010b	2.650
0000101b	0.525	1.000	0110000b	1.600	1011011b	2.675
0000110b	0.550	1.000	0110001b	1.625	1011100b	2.700
0000111b	0.575	1.000	0110010b	1.650	1011101b	2.725
0001000b	0.600	1.000	0110011b	1.675	1011110b	2.750
0001001b	0.625	1.000	0110100b	1.700	1011111b	2.775
0001010b	0.650	1.000	0110101b	1.725	1100000b	2.800
0001011b	0.675	1.000	0110110b	1.750	1100001b	2.825
0001100b	0.700	1.000	0110111b	1.775	1100010b	2.850
0001101b	0.725	1.000	0111000b	1.800	1100011b	2.875
0001110b	0.750	1.000	0111001b	1.825	1100100b	2.900
0001111b	0.775	1.000	0111010b	1.850	1100101b	2.925
0010000b	0.800	1.000	0111011b	1.875	1100110b	2.950
0010001b	0.825	1.000	0111100b	1.900	1100111b	2.975
0010010b	0.850	1.000	0111101b	1.925	1101000b	3.000
0010011b	0.875	1.000	0111110b	1.950	1101001b	3.025
0010100b	0.900	1.000	0111111b	1.975	1101010b	3.050
0010101b	0.925	1.000	1000000b	2.000	1101011b	3.075
0010110b	0.950	1.000	1000001b	2.025	1101100b	3.100
0010111b	0.975	1.000	1000010b	2.050	1101101b	3.125
0011000b	1.000	1.000	1000011b	2.075	1101110b	3.150
0011001b	1.025	1.025	1000100b	2.100	1101111b	3.175

表 6-3. 25-mV Step-Size V_{OUT} Range (続き)

VID BITS	V_{OUT} (Converters)	V_{OUT} (Controllers)	VID BITS	V_{OUT}	VID BITS	V_{OUT}
0011010b	1.050	1.050	1000101b	2.125	1110000b	3.200
0011011b	1.075	1.075	1000110b	2.150	1110001b	3.225
0011100b	1.100	1.100	1000111b	2.175	1110010b	3.250
0011101b	1.125	1.125	1001000b	2.200	1110011b	3.275
0011110b	1.150	1.150	1001001b	2.225	1110100b	3.300
0011111b	1.175	1.175	1001010b	2.250	1110101b	3.325
0100000b	1.200	1.200	1001011b	2.275	1110110b	3.350
0100001b	1.225	1.225	1001100b	2.300	1110111b	3.375
0100010b	1.250	1.250	1001101b	2.325	1111000b	3.400
0100011b	1.275	1.275	1001110b	2.350	1111001b	3.425
0100100b	1.300	1.300	1001111b	2.375	1111010b	3.450
0100101b	1.325	1.325	1010000b	2.400	1111011b	3.475
0100110b	1.350	1.350	1010001b	2.425	1111100b	3.500
0100111b	1.375	1.375	1010010b	2.450	1111101b	3.525
0101000b	1.400	1.400	1010011b	2.475	1111110b	3.550
0101001b	1.425	1.425	1010100b	2.500	1111111b	3.575
0101010b	1.450	1.450	1010101b	2.525	—	—

6.3.1 Controller Overview

The controllers are fast-reacting, high-frequency, scalable output-power controllers capable of driving two external N-MOSFETs. The controllers use the D-CAP2 control scheme that optimizes transient responses at high load currents for such applications as CORE and DDR supplies. The output voltage is compared with and internal reference voltage after divider resistors. The PWM comparator determines the timing to turn on the high-side MOSFET. The PWM comparator response maintains a very small PWM output ripple voltage. Because the device does not have a dedicated oscillator for the on-board control loop, the switching cycle is controlled by the adaptive on-time circuit. The on-time is controlled to meet the target switching frequency by feed-forwarding the input and output voltage into the on-time one-shot timer.

The D-CAP2 control scheme has an injected ripple from the SW node that is added on to the reference voltage to simulate output ripple, which eliminates the need for ESR-induced output ripple from D-CAP mode control. Therefore, low-ESR output capacitors (such as low-cost ceramic MLCC capacitors) can be used with the controllers. 図 6-2 shows the block diagram for the controller

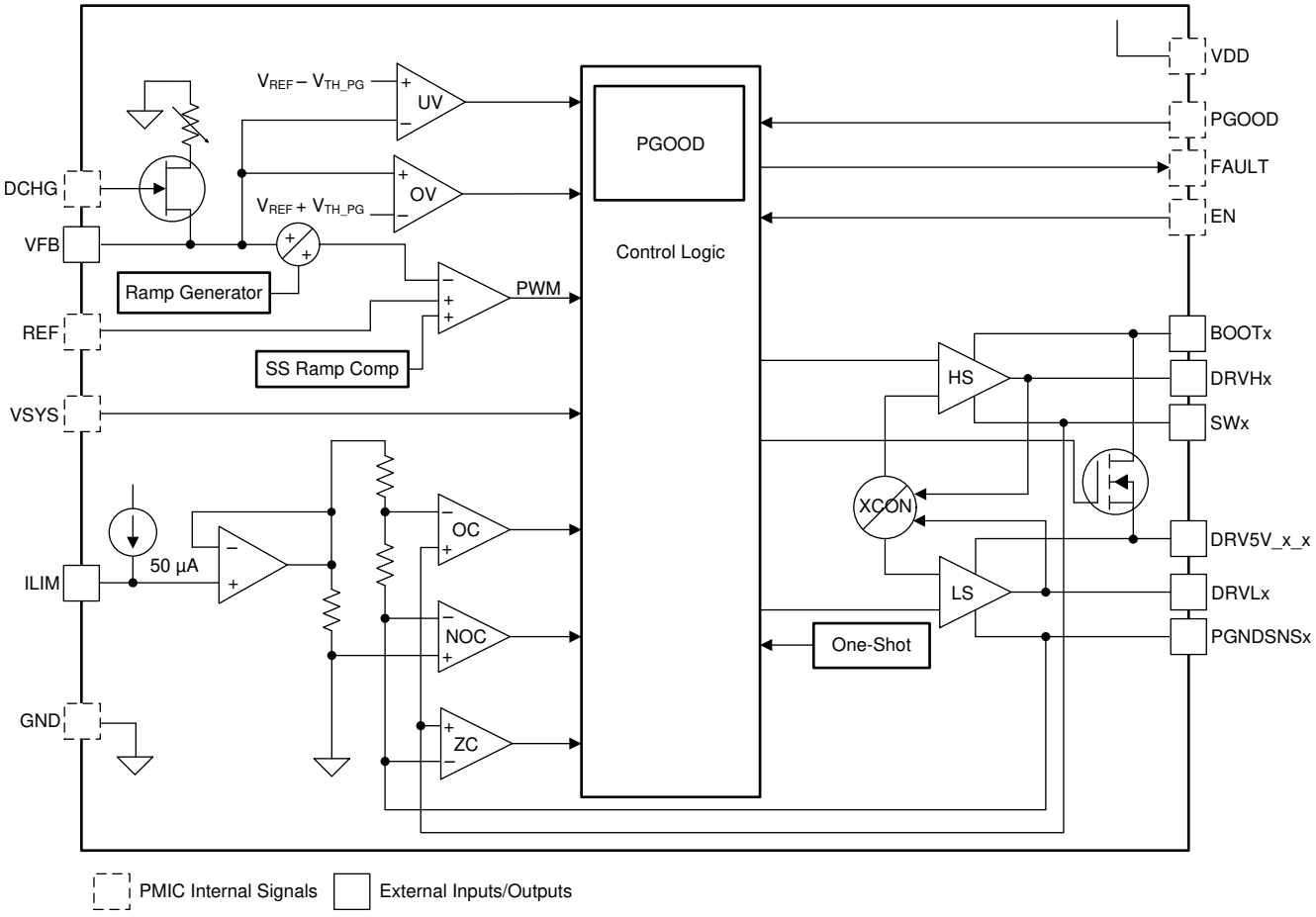


図 6-2. Controller Block Diagram

6.3.2 Converter Overview

The PMIC synchronous step-down DC-DC converters include a unique, hysteretic PWM-controller scheme which enables a high switching-frequency converter, excellent transient and AC load regulation as well as operation with cost-competitive external components. The controller topology supports forced PWM mode as well as power-save mode operation. Power-save mode operation, or PFM mode, reduces the quiescent current consumption and ensures high conversion efficiency at light loads by skipping switch pulses. In forced PWM mode, the device operates on a quasi-fixed frequency, avoids pulse skipping, and allows filtering of the switch noise by external filter components. The PMIC device offers fixed output voltage options featuring a small solution size by using only three external components per converter.

A significant advantage of a PMIC over other hysteretic PWM controller topologies is the excellent AC load transient regulation capability of PMICs. When the output voltage falls below the threshold of the error comparator, a switch pulse is initiated, and the high-side switch is turned on. The switch remains turned on until a minimum on-time (t_{ONmin}) expires and the output voltage trips the threshold of the error comparator, or until the inductor current reaches the current limit of the high-side switch. When the high-side switch turns off, the low-side switch rectifier is turned on and the inductor current ramps down until the high-side switch turns on again or the inductor current reaches zero. In forced PWM mode operation, negative inductor current is allowed to enable continuous conduction mode even at no load condition.

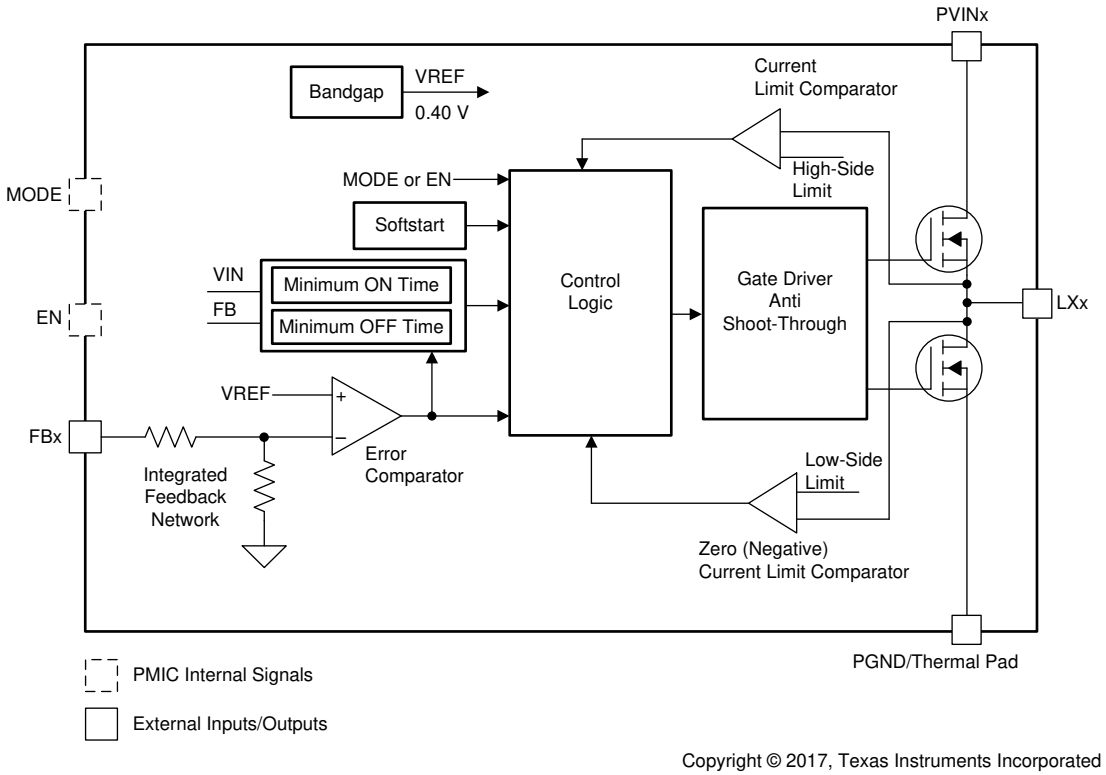


図 6-3. Converter Block Diagram

6.3.3 Dynamic Voltage Scaling

The buck regulators (BUCK1 through BUCK6) support dynamic voltage scaling (DVS) for maximum system efficiency. The VR outputs can slew up and slew down in either 10-mV or 25-mV steps using the 7-bit voltage ID (VID) defined in セクション 5.7 and セクション 5.8. The DVS slew rate is 2.5 mV/µs (minimum). To meet the minimum slew rate, VID progresses to the next code at 3-µs (nominal) interval per 10-mV or at 6-µs interval per 25-mV steps. When DVS is active, the VR is forced into PWM mode, unless the BUCKx_DECAY bit is 1b, to ensure the output keeps track of the VID code with minimal delay. Additionally, the PGOOD bits (in the PG_STATUS1 and PG_STATUS2 registers) are masked when DVS is in progress. 図 6-4 shows an example of slew down and slew up from one VID to another (step size of 10 mV).

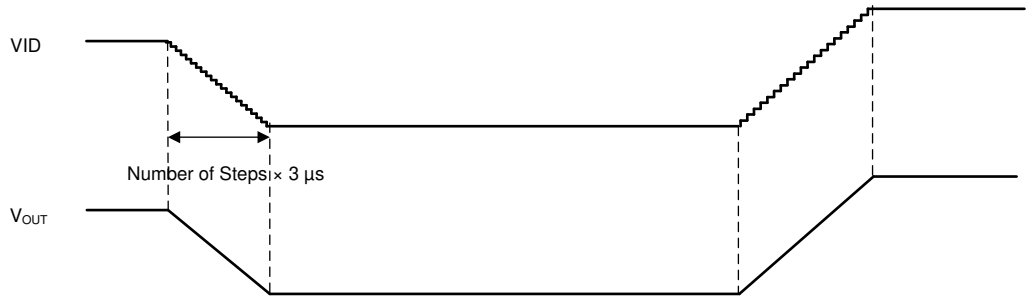


図 6-4. DVS Timing Diagram I (BUCKx_DECAY = 0b)

When DVS is enabled and the BUCKx_VID[6:0] bit is set to any setting except 0b or 1b, the slew rate of the voltage is as shown in 図 6-4.

As shown in 図 6-5, if a BUCKx_VID[6:0] bit is set to 0000000b, the output voltage of that buck slews down to 0.5 V first, and then drifts down to 0 V as the SMPS stops switching. Subsequently, if a BUCKx_VID[6:0] bit is set to a value (neither 0000000b nor 0000001b) when the output voltage of that buck is less than 0.5 V, the VR ramps up to 0.5 V first and the soft-start time begins. The output voltage then slews up to the target voltage of the previously mentioned slew rate.

注

A fixed 200 µs of soft-start time is reserved for the output voltage to reach 0.5 V. In this case, however, the SMPS is not forced into PWM mode as it otherwise could cause the output voltage to droop momentarily if the output voltage might have been drifting above 0.5 V for any reason.

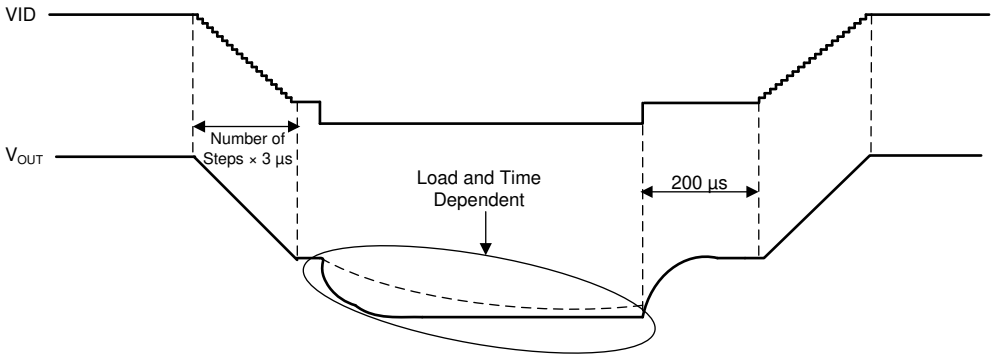


図 6-5. DVS Timing Diagram II (BUCKx_DECAY = 0b)

6.3.4 Current Limit

The buck controllers (BUCK1, BUCK2, and BUCK6) have inductor-valley current-limit architecture and the current limit is programmable by an external resistor at the ILIMx pin. 式 1 shows the calculation for a desired resistor value, depending on specific application conditions. The I_{LIMREF} current is the current source out of the ILIMx pin that is typically 50 µA, and R_{DSON} is the maximum channel resistance of the low-side FET. The scaling factor is 1.3 to consider all errors and temperature variations of R_{DSON}, I_{LIMREF}, and R_{ILIM}. Finally, 8 is another scaling factor associated with the I_{LIMREF} current.

$$R_{ILIM} = \frac{R_{DSON} \times 8 \times 1.3 \times \left(I_{LIM} - \frac{I_{ripple(min)}}{2} \right)}{I_{LIMREF}} \quad (1)$$

where

- I_{LIM} is the target current limit. An appropriate margin must be allowed when determining the value of I_{LIM} from the maximum DC load current of the output.
- $I_{ripple(min)}$ is the minimum peak-to-peak inductor ripple current for a given output voltage.

$$I_{ripple(min)} = \frac{V_{OUT} \left(V_{IN(MIN)} - V_{OUT} \right)}{L_{max} \times V_{IN(MIN)} \times f_{sw(max)}} \quad (2)$$

where

- L_{max} is the maximum inductance.
- $f_{sw(max)}$ is the maximum switching frequency.
- $V_{IN(MIN)}$ is the minimum input voltage to the external power stage.

The inductor of the buck converter limits the peak current. This current limiting is done on a cycle-by-cycle basis to the current limit (I_{IND_LIM}), which is specified in セクション 5.8.

6.4 LDO Regulators and Load Switches

6.4.1 VTT LDO

Powered from the BUCK6 output, the VTT LDO tracks the V_{BUCK6} voltage by regulating its output to a half of its input. The LDO current limit is OTP dependent, and it is designed specifically to power DDR memory. The LDO core is a transconductance amplifier with large gain, and it drives a current output stage that either sources or sinks current depending on the deviation of VTTFB pin voltage from the target regulation voltage.

6.4.2 LDOA1–LDOA3

The TPS6508700 device integrates three general-purpose LDOs. LDOA1 is powered from a 5-V supply through the DRV5V_2_A1 pin and it can be factory configured as an always-on rail as long as a valid power supply is available at the VSYS pin. For LDOA1 output voltage options, see 表 6-4. LDOA2 and LDOA3 share a power input pin (PVINLDOA2_A3). The output regulation voltages are set by writing to the LDOAx_VID[3:0] bits (registers 0x9A, 0x9B, and 0xAE). For LDOA2 and LDOA3 output voltage options, See 表 6-5.

表 6-4. LDOA1 Output Voltage Options

VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000b	1.35	0100b	1.8	1000b	2.3	1100b	2.85
0001b	1.5	0101b	1.9	1001b	2.4	1101b	3.0
0010b	1.6	0110b	2.0	1010b	2.5	1110b	3.3
0011b	1.7	0111b	2.1	1011b	2.6	1111b	Not Used

表 6-5. LDOA2 and LDOA3 Output Voltage Options

VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000b	0.70	0100b	0.90	1000b	1.10	1100b	1.30
0001b	0.75	0101b	0.95	1001b	1.15	1101b	1.35
0010b	0.80	0110b	1.00	1010b	1.20	1110b	1.40
0011b	0.85	0111b	1.05	1011b	1.25	1111b	1.50

6.4.3 Load Switches

The PMIC features three general-purpose load switches. The SWA1 switch has a dedicated power input pin (PVINSWA1). The SWB1 and SWB2 pins share one power input pin (PVINSWB1_B2). All switches have built-in slew-rate control during startup to limit the inrush current.

6.5 Power Good Information (PGOOD or PG) and GPO Pins

The device provides information on status of VRs through four GPO pins along with the power-good status registers defined in セクション 6.9.47 and セクション 6.9.48. Power good information of any individual VR and load switch can be assigned to be part of the PGOOD tree as defined from セクション 6.9.37 to セクション 6.9.44. PGOOD assertion delays are programmable from 0 ms to 15 ms for GPO1, 0 ms to 100 ms for GPO2 and GPO4, and 2.5 ms to 100 ms for GPO3 as defined in セクション 6.9.19 and セクション 6.9.31 (respectively).

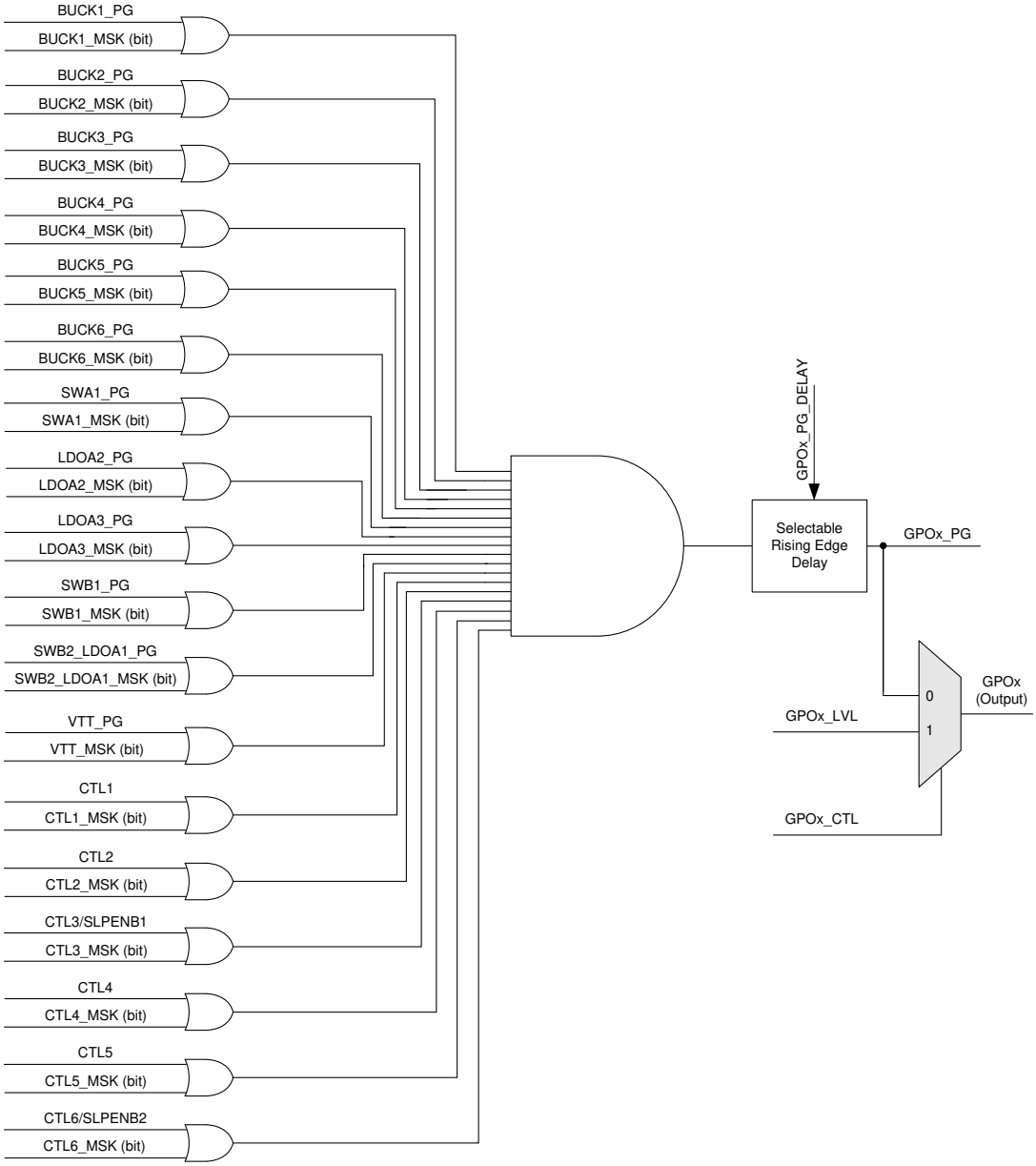


図 6-6. Power Good Tree

Alternatively, the GPOs can be used as general-purpose outputs controlled by the user through I^2C. For more information on controlling the GPOs in I^2C control mode, see セクション 6.9.34.

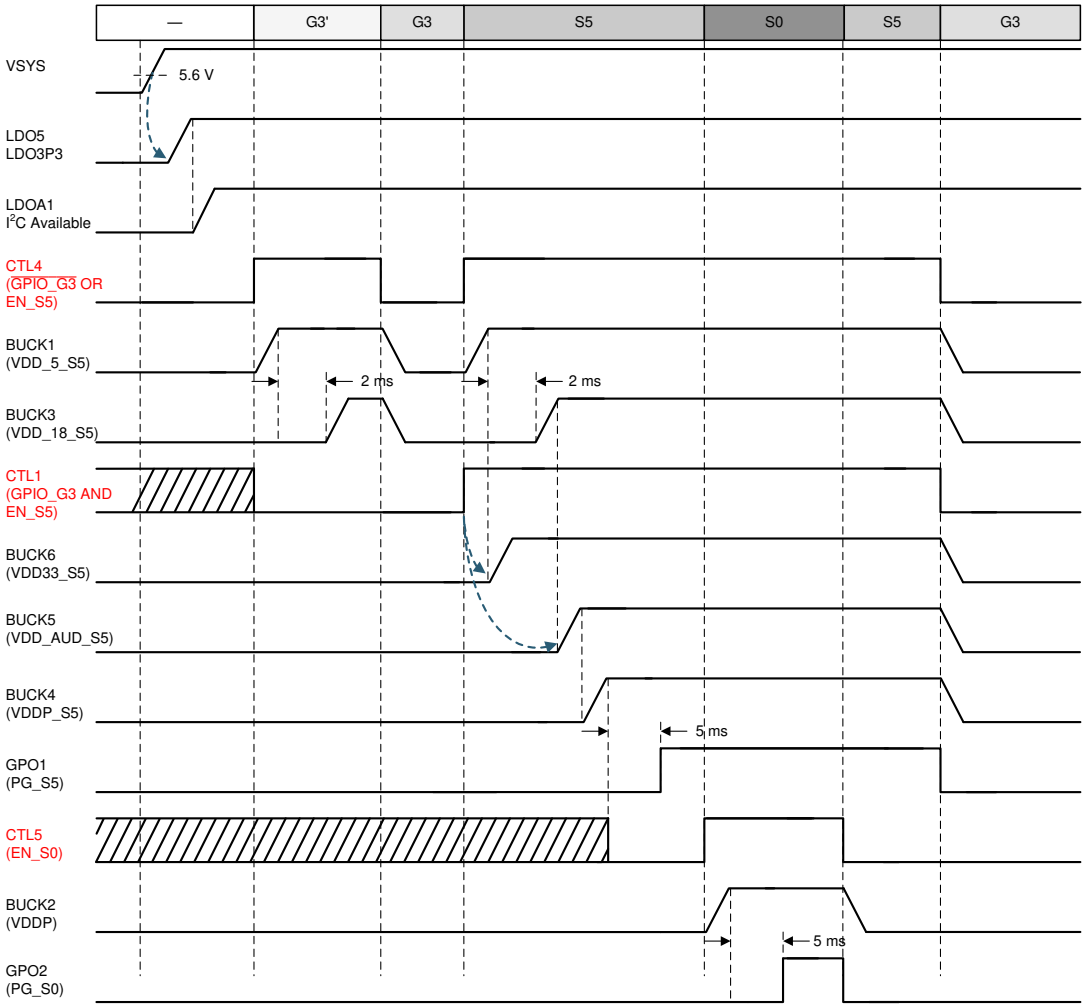
6.6 Power Sequencing and Voltage-Rail Control

When a valid power source is available at the VSYS pin (VSYS ≥ 5.6 V), the internal analog blocks, including LDO5 and LDO3P3, are enabled. The device then has three ways of sequencing the rails during power up and power down:

- Rail enabled by CTLx pin
- Rail enabled by power good, (PG) of the previously enabled rail
- Rail enabled by I^2C software command

6.6.1 Power-Up and Power-Down Sequencing

The power-up and power-down sequence uses the CTL1, CTL4, and CTL5 pins to enable and disable regulators as required by the system. 図 6-7 shows the sequencing of these enables in a typical power-up and power-down sequence.



A. CTLx are control signals from the discrete digital from the processor to enable the rails.
B. CTL2 enables SWA1, CTL3 enables SWB1, and CTL6 enables SWB2. The LDOA2 and LDOA3 enable bits are disabled by default. The LDOA2_Dis and LDOA3_Dis bits should be set to 1h to enable them.
C. The power fault is masked for 10 ms when the regulator is enabled.

図 6-7. Power-Up and Power-Down Sequence

表 6-6 lists the system power states.

表 6-6. System Power States

STATE	GPIO_G3	EN_S5	CTL4	CTL5
G3’	1	0	1	0
G3’	1	1	1	0
G3 state	0	0	0	0
S5 state	0	1	1	1

6.6.2 Emergency Shutdown

図 6-8 shows the emergency shutdown sequence.

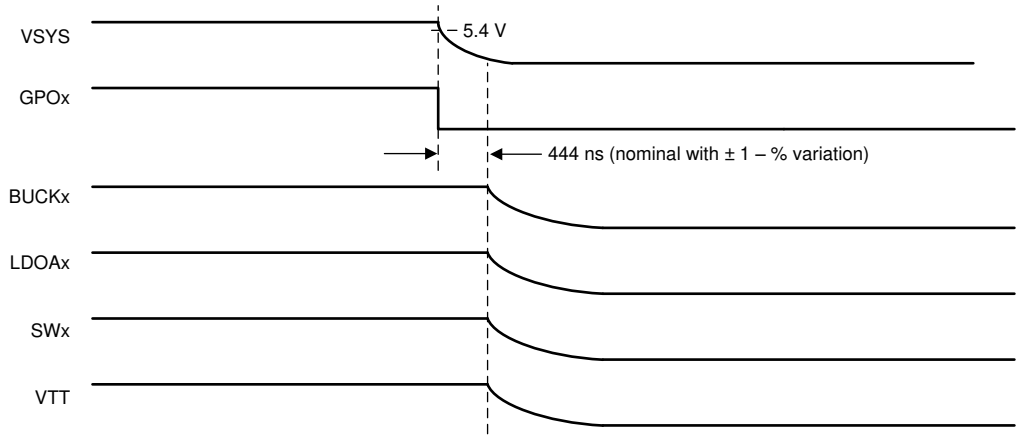


図 6-8. Emergency Shutdown Sequence

When the V_{SYS} voltage crosses below $V_{SYS\_UVLO\_5V}$, all power good pins are deasserted, and after 444 ns (nominal) of delay, all VRs shut down. Upon shutdown, all internal discharge resistors are set to 100 Ω to ensure timely decay of all VR outputs. Other conditions that cause emergency shutdown are the die temperature rising above the critical temperature threshold (T_{CRIT}), and deassertion of the power good of any rail (configurable).

6.7 Device Functional Modes

6.7.1 Off Mode

When the power supply at the VSYS pin is less than $V_{SYS\_UVLO\_5V}$ (5.4-V nominal) + $V_{SYS\_UVLO\_5V\_HYS}$ (0.2-V nominal), the device is in off mode, where all output rails are disabled. If the supply voltage is greater than $V_{SYS\_UVLO\_3V}$ (3.6-V nominal) + $V_{SYS\_UVLO\_3V\_HYS}$ (0.15-V nominal) while the supply voltage is still less than $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$, then the internal band-gap reference (VREF pin) along with LDO3P3 are enabled and regulated at target values.

6.7.2 Standby Mode

When the power supply at the VSYS pin rises above $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$, the device enters standby mode, where all internal reference and regulators (LDO3P3 and LDO5) are up and running, and I^2C interface and CTL pins are ready to respond. All default registers defined in セクション 6.9.1 should have been loaded from one-time programmable (OTP) memory by now. Quiescent current consumption in standby mode is specified in セクション 5.5.

6.7.3 Active Mode

The device proceeds to active mode when any output rail is enabled through an input pin as discussed in セクション 6.6 or by writing to EN bits through I^2C. The output regulation voltage can also be changed by writing to the VID bits defined in セクション 6.9.1.

6.8 I²C Interface

The I²C interface is a 2-wire serial interface. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, DATA, and CLK. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives data, transmits data, or both on the bus under control of the master device.

The TPS6508700 device works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode
(1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when the V_{SYS} voltage is higher than $V_{SYS\_UVLO\_5V}$ and is applied to the TPS6508700 device. The I²C interface is running from an internal oscillator that is automatically enabled when access to the interface is avaialble.

The data transfer protocol for fast and standard modes are exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as H/S-mode.

The TPS6508700 device supports 7-bit addressing; however, 10-bit addressing and a general call address are not supported. The default device address is 0x5E.

6.8.1 F/S-Mode Protocol

The master initiates a data transfer by generating a start condition. The start condition is a high-to-low transition that occurs on the SDA line while SCL is high (see 図 6-9). All I²C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read-write direction bit, R/W, on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see
図 6-10). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see 図 6-11) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master identifies that the communication link with a slave has been established.

The master generates additional SCL cycles to either transmit data to the slave (R/W bit is 0b) or receive data from the slave (R/W bit is 1b). In either case, the receiver must acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as required.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 6-9). This process releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the stop condition. Upon receiving a stop condition, all devices identify that the bus is released, and wait for a start condition followed by a matching address.

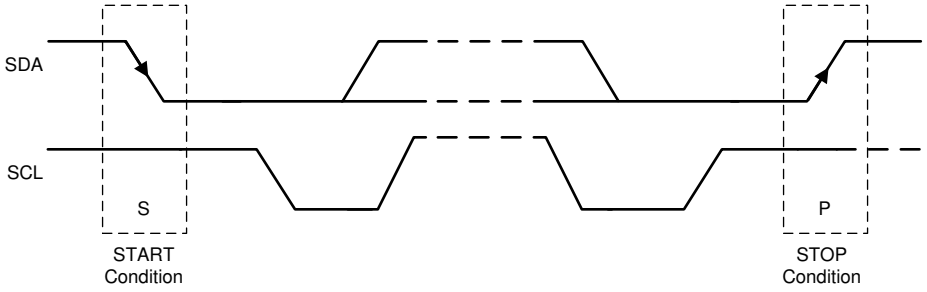


図 6-9. START and STOP Conditions

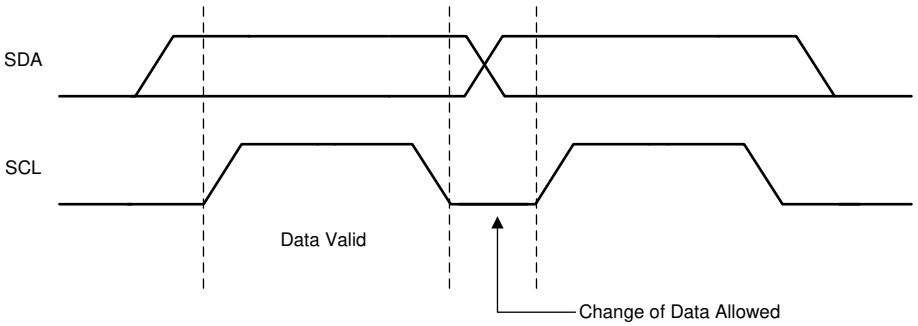


図 6-10. Bit Transfer on the I²C Bus

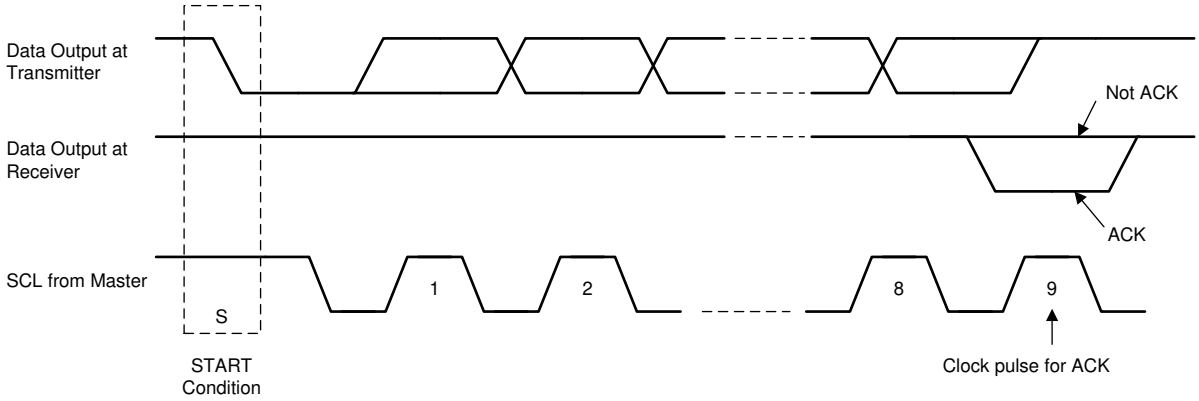


図 6-11. Acknowledge on the I²C Bus

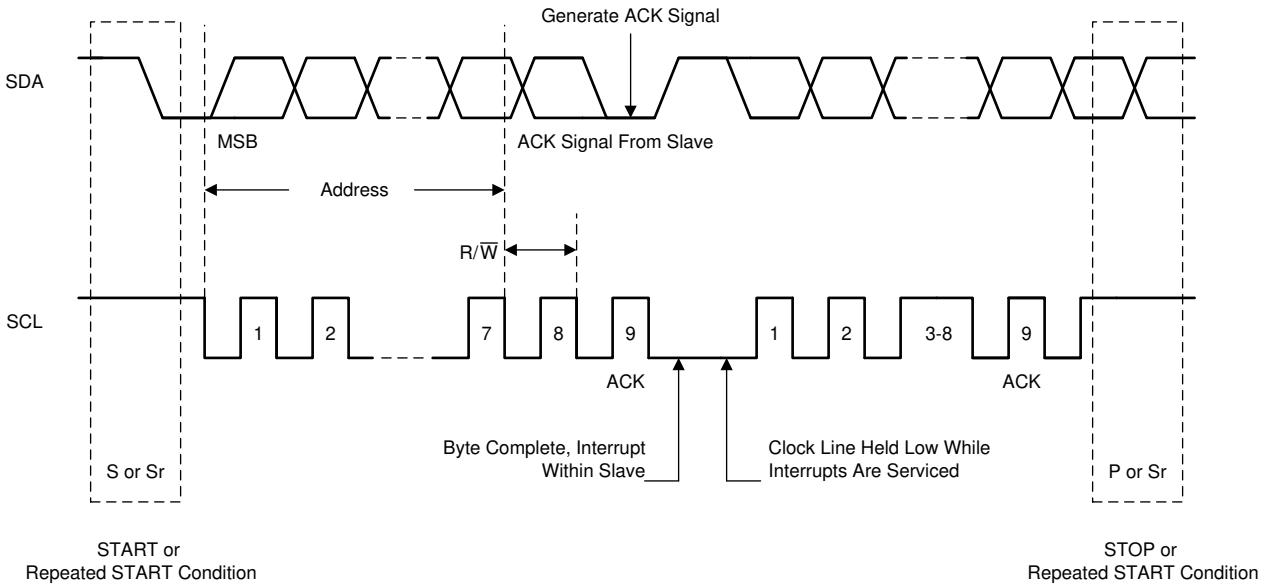


図 6-12. I²C Bus Protocol

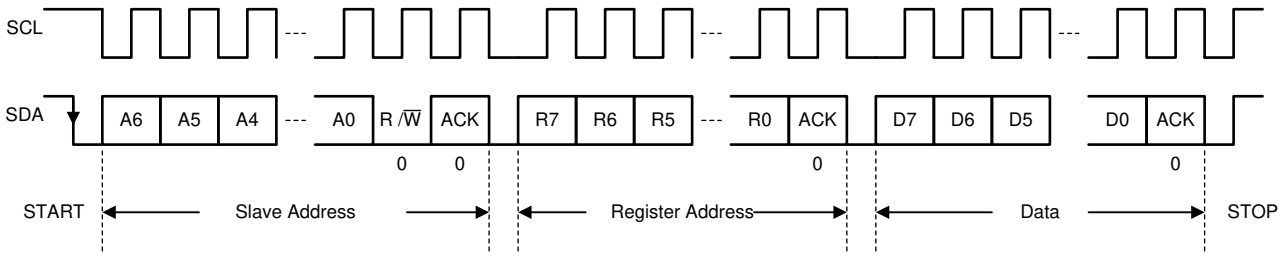


図 6-13. I²C Interface WRITE to TPS6508700 in F/S Mode

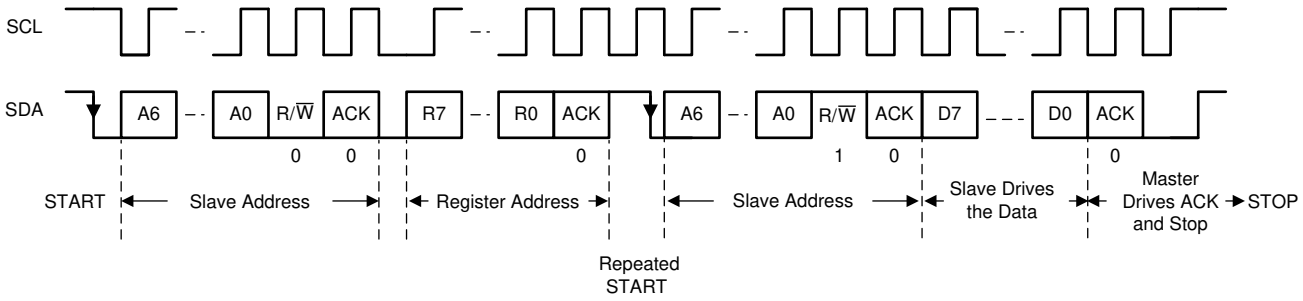


図 6-14. I²C Interface READ From TPS6508700 in F/S Mode (Only Repeated START is Supported)

6.9 Register Maps

6.9.1 Register Map Summary

表 6-7 lists the memory-mapped registers for the TPS6508700. All register offset addresses not listed in 表 6-7 should be considered as reserved locations and the register contents should not be modified.

表 6-7. Register Map Summary

Offset	Acronym	Short Description	Section
1h	DEVICEID	Device ID code indicating revision	Go
2h	IRQ	Interrupt statuses	Go
3h	IRQ_MASK	Interrupt masking	Go
4h	PMICSTAT	PMIC temperature indicator	Go
5h	SHUTDNSRC	Shutdown root cause indicator bits	Go
21h	BUCK2CTRL	BUCK2 decay control and voltage select	Go
22h	BUCK3DECAY	BUCK3 decay control	Go
23h	BUCK3VID	BUCK3 voltage select	Go
24h	BUCK3SLPCTRL	BUCK3 voltage select for SLEEP state	Go
25h	BUCK4CTRL	BUCK4 control	Go
26h	BUCK5CTRL	BUCK5 control	Go
27h	BUCK6CTRL	BUCK6 control	Go
28h	LDOA2CTRL	LDOA2 control	Go
29h	LDOA3CTRL	LDOA3 control	Go
40h	DISCHCTRL1	Discharge resistors for each rail control	Go
41h	DISCHCTRL2	Discharge resistors for each rail control	Go
42h	DISCHCTRL3	Discharge resistors for each rail control	Go
43h	PG_DELAY1	System Power Good on GPO3 (*if GPO3 is programmed to be system PG*)	Go
91h	FORCESHUTDN	Software force shutdown	Go
93h	BUCK2SLPCTRL	BUCK2 voltage select for SLEEP state	Go
94h	BUCK4VID	BUCK4 voltage select	Go
95h	BUCK4SLPVID	BUCK4 voltage select for SLEEP state	Go
96h	BUCK5VID	BUCK5 voltage select	Go
97h	BUCK5SLPVID	BUCK5 voltage select for SLEEP state	Go
98h	BUCK6VID	BUCK6 voltage select	Go
99h	BUCK6SLPVID	BUCK6 voltage select for SLEEP state	Go
9Ah	LDOA2VID	LDOA2 voltage select	Go
9Bh	LDOA3VID	LDOA3 voltage select	Go
9Ch	BUCK123CTRL	BUCK1, 2, and 3 disable and PFM/PWM mode control	Go
9Dh	PG_DELAY2	System Power Good on GPO1, 2, and 4 (*if GPOs are programmed to be system PG*)	Go
9Fh	SWVTT_DIS	SWs and VTT I^2C disable bits	Go
A0h	I2C_RAIL_EN1	I^2C enable control of individual rails	Go
A1h	I2C_RAIL_EN2/GPOCTRL	I^2C enable control of individual rails and I^2C controlled GPOs, high or low	Go
A2h	PWR_FAULT_MASK1	Power fault masking for individual rails	Go
A3h	PWR_FAULT_MASK2	Power fault masking for individual rails	Go
A4h	GPO1PG_CTRL1	Power good tree control for GPO1	Go
A5h	GPO1PG_CTRL2	Power good tree control for GPO1	Go
A6h	GPO4PG_CTRL1	Power good tree control for GPO4	Go

表 6-7. Register Map Summary (続き)

Offset	Acronym	Short Description	Section
A7h	GPO4PG_CTRL2	Power good tree control for GPO4	Go
A8h	GPO2PG_CTRL1	Power good tree control for GPO2	Go
A9h	GPO2PG_CTRL2	Power good tree control for GPO2	Go
AAh	GPO3PG_CTRL1	Power good tree control for GPO3	Go
ABh	GPO3PG_CTRL2	Power good tree control for GPO3	Go
ACh	MISCSYSPG	Power Good tree control with CTL3 and CTL6 for GPO	Go
AEh	LDOA1CTRL	LDOA1 control for discharge, voltage selection, and enable	Go
B0h	PG_STATUS1	Power Good statuses for individual rails	Go
B1h	PG_STATUS2	Power Good statuses for individual rails	Go
B2h	PWR_FAULT_STATUS1	Power fault statuses for individual rails	Go
B3h	PWR_FAULT_STATUS2	Power fault statuses for individual rails	Go
B4h	TEMPCRIT	Critical temperature indicators	Go
B5h	TEMPHOT	Hot temperature indicators	Go
B6h	OC_STATUS	Overcurrent fault status	Go

Complex bit access types are encoded to fit into small table cells. 表 6-8 shows the codes that are used for access types in this section.

表 6-8. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*h		Value after reset or the default value

6.9.2 DEVICEID: PMIC Device and Revision ID Register (offset = 1h) [reset = 10h]

DEVICEID is shown in 図 6-15 and described in 表 6-9.

Return to Summary Table.

図 6-15. DEVICEID Register

7	6	5	4	3	2	1	0
REVID[1:0]		OTP_VERSION[1:0]		PART_NUMBER[3:0]			
R-0h		R-1h		R-0h			

表 6-9. DEVICEID Field Descriptions

Bit	Field	Type	Reset	Description
7-6	REVID[1:0]	R	0h	Silicon revision ID
5-4	OTP_VERSION[1:0]	R	1h	OTP variation ID 0h = A 1h = B 2h = C 3h = D
3-0	PART_NUMBER[3:0]	R	0h	Device part number ID 0h = TPS6508700 1h = TPS6508701 Fh = TPS650870F

6.9.3 IRQ: PMIC Interrupt Register (offset = 2h) [reset = 0h]

IRQ is shown in 図 6-16 and described in 表 6-10.

Return to Summary Table.

図 6-16. IRQ Register

7	6	5	4	3	2	1	0
FAULT	RESERVED			SHUTDN	RESERVED		DIETEMP
R/W-0h	R-0h			R/W-0h	R-0h		R/W-0h

表 6-10. IRQ Field Descriptions

Bit	Field	Type	Reset	Description
7	FAULT	R/W	0h	Fault interrupt. Asserted when either condition occurs: SYS < UVLO, power fault of any rail, or die temperature crosses over the critical temperature threshold (T_{CRIT}). The user can read registers 0xB2 through 0xB6 to determine what has caused the interrupt. 0h = Not asserted 1h = Asserted. Host to write 1 to clear.
6-4	RESERVED	R	0h	
3	SHUTDN	R/W	0h	Asserted when PMIC shuts down. To clear indicator, SHUTDNSRC must be cleared first, see セクション 6.9.6 0h = Not asserted. 1h = Asserted. Host to write 1 to clear.
2-1	RESERVED	R	0h	
0	DIETEMP	R/W	0h	Die temp interrupt. Asserted when PMIC die temperature crosses above the hot temperature threshold (T_{HOT}). 0h = Not asserted. 1h = Asserted. Host to write 1 to clear.

6.9.4 IRQ_MASK: PMIC Interrupt Mask Register (offset = 3h) [reset = FFh]

IRQ_MASK is shown in 図 6-17 and described in 表 6-11.

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図 6-17. IRQ_MASK Register

7	6	5	4	3	2	1	0
MFAULT	RESERVED			MSHUTDN	RESERVED		MDIETEMP
R/W-1h	R-7h			R/W-1h	R-3h		R/W-1h

表 6-11. IRQ_MASK Field Descriptions

Bit	Field	Type	Reset	Description
7	MFAULT	R/W	1h	FAULT interrupt mask. 0h = Not masked. 1h = Masked.
6-4	RESERVED	R	7h	
3	MSHUTDN	R/W	1h	PMIC shutdown event interrupt mask 0h = Not masked. 1h = Masked.
2-1	RESERVED	R	3h	
0	MDIETEMP	R/W	1h	Die temp interrupt mask. 0h = Not masked. 1h = Masked.

6.9.5 PMICSTAT: PMIC Status Register (offset = 4h) [reset = 0h]

PMICSTAT is shown in 図 6-18 and described in 表 6-12.

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図 6-18. PMICSTAT Register

7	6	5	4	3	2	1	0
RESERVED							SDIETEMP
R-0h							R-0h

表 6-12. PMICSTAT Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	SDIETEMP	R	0h	PMIC die temperature status. 0h = PMIC die temperature is below T_{HOT}. 1h = PMIC die temperature is above T_{HOT}.

6.9.6 SHUTDNSRC: PMIC Shut-Down Event Register (offset = 5h) [reset = 0h]

SHUTDNSRC is shown in 図 6-19 and described in 表 6-13.

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図 6-19. SHUTDNSRC Register

7	6	5	4	3	2	1	0
RESERVED				COLDOFF	UVLO	PWRFLT	CRITTEMP
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-13. SHUTDNSRC Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	COLDOFF	R/W	0h	Set by PMIC cleared by host. Host to write 1 to clear. This bit is always 0h for TPS6508700. 0h = Cleared 1h = PMIC was shut down by pulling down ***CTL1*** pin.
2	UVLO	R/W	0h	Set by PMIC cleared by host. Host to write 1 to clear. 0h = Cleared 1h = PMIC was shut down due to a UVLO event (V_{SYS} crosses below 5.4 V). Assertion of this bit sets the SHUTDN bit in セクション 6.9.3.
1	PWRFLT	R/W	0h	Set by PMIC cleared by host. Host to write 1 to clear. 0h = Cleared 1h = PMIC was shut down due to a power fault on a rail with power fault not masked. Assertion of this bit sets the SHUTDN bit in セクション 6.9.3.
0	CRITTEMP	R/W	0h	Set by PMIC cleared by host. Host to write 1 to clear. 0h = Cleared 1h = PMIC was shut down due to the rise of PMIC die temperature above critical temperature threshold (T_{CRIT}). Assertion of this bit sets the SHUTDN bit in セクション 6.9.3.

6.9.7 BUCK2CTRL: BUCK2 Control Register (offset = 21h) [reset = 50h]

BUCK2CTRL is shown in 図 6-20 and described in 表 6-14.

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図 6-20. BUCK2CTRL Register

7	6	5	4	3	2	1	0
BUCK2_VID[6:0]							BUCK2_DECAY
R/W-28h							R/W-0h

表 6-14. BUCK2CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK2_VID[6:0]	R/W	28h	This field sets the BUCK2 regulator output regulation voltage in normal mode. See 表 6-2 and 表 6-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK2_DECAY	R/W	0h	Decay bit 0h = The output slews down to a lower voltage set by the VID bits. 1h = The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

6.9.8 BUCK3DECAY: BUCK3 Decay Control Register (offset = 22h) [reset = 70h]

BUCK3DECAY is shown in 図 6-21 and described in 表 6-15.

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図 6-21. BUCK3DECAY Register

7	6	5	4	3	2	1	0
RESERVED							BUCK3_DECAY
R/W-38h							R/W-0h

表 6-15. BUCK3DECAY Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	38h	Reserved bits are don't care bits, can be 1h or 0h.
0	BUCK3_DECAY	R/W	0h	Decay bit 0h = The output slews down to a lower voltage set by the VID bits. 1h = The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

6.9.9 BUCK3VID: BUCK3 VID Register (offset = 23h) [reset = 70h]

BUCK3VID is shown in 図 6-22 and described in 表 6-16.

Return to Summary Table.

図 6-22. BUCK3VID Register

7	6	5	4	3	2	1	0
BUCK3_VID[6:0]							RESERVED
R/W-38h							R/W-0h

表 6-16. BUCK3VID Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK3_VID[6:0]	R/W	38h	This field sets the BUCK3 regulator output regulation voltage in normal mode. See 表 6-2 and 表 6-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	RESERVED	R/W	0h	

6.9.10 BUCK3SLPCTRL: BUCK3 Sleep Control VID Register (offset = 24h) [reset = 70h]

BUCK3SLPCTRL is shown in 図 6-23 and described in 表 6-17.

Return to Summary Table.

図 6-23. BUCK3SLPCTRL Register

7	6	5	4	3	2	1	0
BUCK3_SLP_VID[6:0]							BUCK3_SLP_EN
R/W-38h							R/W-0h

表 6-17. BUCK3SLPCTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK3_SLP_VID[6:0]	R/W	38h	This field sets the BUCK3 regulator output regulation voltage in sleep mode. BUCK3_SLP_VID bits are copied to BUCK3_VID bits upon enters sleep mode. See 表 6-2 and 表 6-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK3_SLP_EN	R/W	0h	BUCK3 sleep mode enable. BUCK3 is factory configured to change to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0h = Disable. 1h = Enable.

6.9.11 BUCK4CTRL: BUCK4 Control Register (offset = 25h) [reset = Dh]

BUCK4CTRL is shown in 図 6-24 and described in 表 6-18.

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図 6-24. BUCK4CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BUCK4_SLP_EN[1:0]		RESERVED		BUCK4_MODE	BUCK4_DIS
R-0h		R/W-0h		R/W-3h		R/W-0h	R/W-1h

表 6-18. BUCK4CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	BUCK4_SLP_EN[1:0]	R/W	0h	BUCK4 sleep mode enable. BUCK4 is factory configured to change to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0h = Disable. 1h = Enable. 2h = Enable. 3h = Enable.
3-2	RESERVED	R/W	3h	Reserved as 3h. 0h, 1h, and 2h will result in BUCK4 regulation ignoring BUCK4_VID and BUCK4_SLP_VID values.
1	BUCK4_MODE	R/W	0h	This field sets the BUCK4 regulator operating mode. 0h = Automatic mode 1h = Forced PWM mode
0	BUCK4_DIS	R/W	1h	BUCK4 disable bit. Writing 0 to this bit forces BUCK4 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable 1h = Enable

6.9.12 BUCK5CTRL: BUCK5 Control Register (offset = 26h) [reset = Dh]

BUCK5CTRL is shown in 図 6-25 and described in 表 6-19.

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図 6-25. BUCK5CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BUCK5_SLP_EN[1:0]		RESERVED		BUCK5_MODE	BUCK5_DIS
R-0h		R/W-0h		R/W-3h		R/W-0h	R/W-1h

表 6-19. BUCK5CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	BUCK5_SLP_EN[1:0]	R/W	0h	BUCK5 sleep mode enable. BUCK5 is factory configured to change to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0h = Disable. 1h = Enable. 2h = Enable. 3h = Enable.
3-2	RESERVED	R/W	3h	Reserved as 3h. 0h, 1h, and 2h will result in BUCK5 regulation ignoring BUCK5_VID and BUCK5_SLP_VID values.
1	BUCK5_MODE	R/W	0h	This field sets the BUCK5 regulator operating mode. 0h = Automatic mode 1h = Forced PWM mode
0	BUCK5_DIS	R/W	1h	BUCK5 disable bit. Writing 0 to this bit forces BUCK5 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable. 1h = Enable.

6.9.13 BUCK6CTRL: BUCK6 Control Register (offset = 27h) [reset = Dh]

BUCK6CTRL is shown in 図 6-26 and described in 表 6-20.

Return to Summary Table.

図 6-26. BUCK6CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BUCK6_SLP_EN[1:0]		RESERVED		BUCK6_MODE	BUCK6_DIS
R-0h		R/W-0h		R/W-3h		R/W-0h	R/W-1h

表 6-20. BUCK6CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	BUCK6_SLP_EN[1:0]	R/W	0h	BUCK6 sleep mode enable. BUCK6 is factory configured to change to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0h = Disable. 1h = Enable. 2h = Enable. 3h = Enable.
3-2	RESERVED	R/W	3h	Reserved as 3h. 0h, 1h, and 2h will result in BUCK6 regulation ignoring BUCK6_VID and BUCK6_SLP_VID values.
1	BUCK6_MODE	R/W	0h	This field sets the BUCK6 regulator operating mode. 0h = Automatic mode 1h = Forced PWM mode
0	BUCK6_DIS	R/W	1h	BUCK6 disable bit. Writing 0 to this bit forces BUCK6 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable. 1h = Enable.

6.9.14 LDOA2CTRL: LDOA2 Control Register (offset = 28h) [reset = Ch]

LDOA2CTRL is shown in 図 6-27 and described in 表 6-21.

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図 6-27. LDOA2CTRL Register

7	6	5	4	3	2	1	0
RESERVED		LDOA2_SLP_EN[1:0]		RESERVED			LDOA2_DIS
R-0h		R/W-0h		R/W-6h			R/W-0h

表 6-21. LDOA2CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	LDOA2_SLP_EN[1:0]	R/W	0h	LDOA2 sleep mode enable. LDOA2 is factory configured to change to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0h = Disable. 1h = Enable. 2h = Enable. 3h = Enable.
3-1	RESERVED	R/W	6h	Reserved as 3h. 0h, 1h, and 2h will result in LDOA2 regulation ignoring LDOA2_VID and LDOA2_SLP_VID values.
0	LDOA2_DIS	R/W	0h	LDOA2 disable bit. Writing 0 to this bit forces LDOA2 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable. 1h = Enable.

6.9.15 LDOA3CTRL: LDOA3 Control Register (offset = 29h) [reset = 3Ch]

LDOA3CTRL is shown in 図 6-28 and described in 表 6-22.

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図 6-28. LDOA3CTRL Register

7	6	5	4	3	2	1	0
RESERVED		LDOA3_SLP_EN[1:0]		RESERVED			LDOA3_DIS
R-0h		R/W-3h		R/W-6h			R/W-0h

表 6-22. LDOA3CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	LDOA3_SLP_EN[1:0]	R/W	3h	LDOA3 sleep mode enable. LDOA3 is factory configured to change to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0h = Disable. 1h = Enable. 2h = Enable. 3h = Enable.
3-1	RESERVED	R/W	6h	Reserved as 3h. 0h, 1h, and 2h will result in LDOA3 regulation ignoring LDOA3_VID and LDOA3_SLP_VID values.
0	LDOA3_DIS	R/W	0h	LDOA3 disable bit. Writing 0h to this bit forces LDOA3 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable 1h = Enable

6.9.16 DISCHCTRL1: Discharge Control1 Register (offset = 40h) [reset = 55h]

DISCHCTRL1 is shown in 図 6-29 and described in 表 6-23.

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All xx_DISCHG[1:0] bits internally set to 0h whenever the corresponding VR is enabled.

図 6-29. DISCHCTRL1 Register

7	6	5	4	3	2	1	0
BUCK4_DISCHG[1:0]		BUCK3_DISCHG[1:0]		BUCK2_DISCHG[1:0]		BUCK1_DISCHG[1:0]	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	

表 6-23. DISCHCTRL1 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BUCK4_DISCHG[1:0]	R/W	1h	BUCK4 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω
5-4	BUCK3_DISCHG[1:0]	R/W	1h	BUCK3 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω
3-2	BUCK2_DISCHG[1:0]	R/W	1h	BUCK2 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω
1-0	BUCK1_DISCHG[1:0]	R/W	1h	BUCK1 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω

6.9.17 DISCHCTRL2: Discharge Control2 Register (offset = 41h) [reset = 55h]

DISCHCTRL2 is shown in 図 6-30 and described in 表 6-24.

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All xx_DISCHG[1:0] bits internally set to 0h whenever the corresponding VR is enabled.

図 6-30. DISCHCTRL2 Register

7	6	5	4	3	2	1	0
LDOA2_DISCHG[1:0]		SWA1_DISCHG[1:0]		BUCK6_DISCHG[1:0]		BUCK5_DISCHG[1:0]	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	

表 6-24. DISCHCTRL2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LDOA2_DISCHG[1:0]	R/W	1h	LDOA2 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω
5-4	SWA1_DISCHG[1:0]	R/W	1h	SWA1 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω
3-2	BUCK6_DISCHG[1:0]	R/W	1h	BUCK6 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω
1-0	BUCK5_DISCHG[1:0]	R/W	1h	BUCK5 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω

6.9.18 DISCHCTRL3: Discharge Control3 Register (offset = 42h) [reset = 15h]

DISCHCTRL3 is shown in 図 6-31 and described in 表 6-25.

Return to Summary Table.

All xx_DISCHG[1:0] bits internally set to 0h whenever the corresponding VR is enabled.

図 6-31. DISCHCTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		SWB2_DISCHG[1:0]		SWB1_DISCHG[1:0]		LDOA3_DISCHG[1:0]	
R-0h		R/W-1h		R/W-1h		R/W-1h	

表 6-25. DISCHCTRL3 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	SWB2_DISCHG[1:0]	R/W	1h	SWB2 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω
3-2	SWB1_DISCHG[1:0]	R/W	1h	SWB1 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω
1-0	LDOA3_DISCHG[1:0]	R/W	1h	LDOA3 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω

6.9.19 PG_DELAY1: Power Good Delay1 Register (offset = 43h) [reset = 0h]

PG_DELAY1 is shown in 図 6-32 and described in 表 6-26.

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Programmable power good delay for GPO3 pin, measured from the moment when all VRs assigned to GPO3 pin reach their regulation range to power good assertion. This register is optional as the PMIC can be programmed for system PG, level shifter or I^2C controller GPO.

図 6-32. PG_DELAY1 Register

7	6	5	4	3	2	1	0
RESERVED					GPO3_PG_DELAY[2:0]		
R-0h					R/W-0h		

表 6-26. PG_DELAY1 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2-0	GPO3_PG_DELAY[2:0]	R/W	0h	Programmable delay power good or level shifter for GPO3 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation. Register not used (GPO3 controlled by I^2C) 0h = 2.5 ms 1h = 5 ms 2h = 10 ms 3h = 15 ms 4h = 20 ms 5h = 50 ms 6h = 75 ms 7h = 100 ms

6.9.20 FORCESHUTDN: Force Emergency Shutdown Control Register (offset = 91h) [reset = 0h]

FORCESHUTDN is shown in 図 6-33 and described in 表 6-27.

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図 6-33. FORCESHUTDN Register

7	6	5	4	3	2	1	0
RESERVED							SDWN
R-0h							R/W-0h

表 6-27. FORCESHUTDN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	SDWN	R/W	0h	Forces reset of the PMIC and reset of all registers. The bit is self-clearing. 0h = No action. 1h = PMIC is forced to shut down.

6.9.21 BUCK2SLPCTRL: BUCK2 Sleep Control Register (offset = 93h) [reset = 50h]

BUCK2SLPCTRL is shown in 図 6-34 and described in 表 6-28.

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図 6-34. BUCK2SLPCTRL Register

7	6	5	4	3	2	1	0
BUCK2_SLP_VID[6:0]							BUCK2_SLP_EN
R/W-28h							R/W-0h

表 6-28. BUCK2SLPCTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK2_SLP_VID[6:0]	R/W	28h	This field sets the BUCK2 regulator output regulation voltage in sleep mode. Mapping between bits and output voltage is defined as in セクション 6.9.7.
0	BUCK2_SLP_EN	R/W	0h	BUCK2 sleep mode enable. BUCK2 is factory configured to change to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. 0h = Disable. 1h = Enable.

6.9.22 BUCK4VID: BUCK4 VID Register (offset = 94h) [reset = 20h]

BUCK4VID is shown in 図 6-35 and described in 表 6-29.

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図 6-35. BUCK4VID Register

7	6	5	4	3	2	1	0
BUCK4_VID[6:0]							BUCK4_DECAY
R/W-10h							R/W-0h

表 6-29. BUCK4VID Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK4_VID[6:0]	R/W	10h	This field sets the BUCK4 regulator output regulation voltage in normal mode. See 表 6-2 and 表 6-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK4_DECAY	R/W	0h	Decay bit 0h = The output slews down to a lower voltage set by the VID bits. 1h = The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

6.9.23 BUCK4SLPVID: BUCK4 Sleep VID Register (offset = 95h) [reset = 20h]

BUCK4SLPVID is shown in 図 6-36 and described in 表 6-30.

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図 6-36. BUCK4SLPVID Register

7	6	5	4	3	2	1	0
BUCK4_SLP_VID[6:0]							RESERVED
R/W-10h							R-0h

表 6-30. BUCK4SLPVID Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK4_SLP_VID[6:0]	R/W	10h	This field sets the BUCK4 regulator output regulation voltage in sleep mode. See 表 6-2 and 表 6-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	RESERVED	R	0h	

6.9.24 BUCK5VID: BUCK5 VID Register (offset = 96h) [reset = 70h]

BUCK5VID is shown in 図 6-37 and described in 表 6-31.

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図 6-37. BUCK5VID Register

7	6	5	4	3	2	1	0
BUCK5_VID[6:0]							BUCK5_DECAY
R/W-38h							R/W-0h

表 6-31. BUCK5VID Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK5_VID[6:0]	R/W	38h	This field sets the BUCK5 regulator output regulation voltage in normal mode. See 表 6-2 and 表 6-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK5_DECAY	R/W	0h	Decay bit 0h = The output slews down to a lower voltage set by the VID bits. 1h = The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

6.9.25 BUCK5SLPVID: BUCK5 Sleep VID Register (offset = 97h) [reset = E8h]

BUCK5SLPVID is shown in 図 6-38 and described in 表 6-32.

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図 6-38. BUCK5SLPVID Register

7	6	5	4	3	2	1	0
BUCK5_SLP_VID[6:0]							RESERVED
R/W-74h							R-0h

表 6-32. BUCK5SLPVID Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK5_SLP_VID[6:0]	R/W	74h	This field sets the BUCK5 regulator output regulation voltage in sleep mode. See 表 6-2 and 表 6-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	RESERVED	R	0h	

6.9.26 BUCK6VID: BUCK6 VID Register (offset = 98h) [reset = E8h]

BUCK6VID is shown in 図 6-39 and described in 表 6-33.

Return to Summary Table.

図 6-39. BUCK6VID Register

7	6	5	4	3	2	1	0
BUCK6_VID[6:0]							BUCK6_DECAY
R/W-74h							R/W-0h

表 6-33. BUCK6VID Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK6_VID[6:0]	R/W	74h	This field sets the BUCK6 regulator output regulation voltage in normal mode. See 表 6-2 and 表 6-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK6_DECAY	R/W	0h	Decay bit 0h = The output slews down to a lower voltage set by the VID bits. 1h = The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

6.9.27 BUCK6SLPVID: BUCK6 Sleep VID Register (offset = 99h) [reset = E8h]

BUCK6SLPVID is shown in 図 6-40 and described in 表 6-34.

Return to Summary Table.

図 6-40. BUCK6SLPVID Register

7	6	5	4	3	2	1	0
BUCK6_SLP_VID[6:0]							RESERVED
R/W-74h							R-0h

表 6-34. BUCK6SLPVID Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BUCK6_SLP_VID[6:0]	R/W	74h	This field sets the BUCK6 regulator output regulation voltage in normal mode. See 表 6-2 and 表 6-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	RESERVED	R	0h	

6.9.28 LDOA2VID: LDOA2 VID Register (offset = 9Ah) [reset = FFh]

LDOA2VID is shown in 図 6-41 and described in 表 6-35.

Return to Summary Table.

図 6-41. LDOA2VID Register

7	6	5	4	3	2	1	0
LDOA2_SLP_VID[3:0]				LDOA2_VID[3:0]			
R/W-Fh				R/W-Fh			

表 6-35. LDOA2VID Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LDOA2_SLP_VID[3:0]	R/W	Fh	This field sets the LDOA2 regulator output regulation voltage in sleep mode. See 表 6-5 for V_{OUT} options.
3-0	LDOA2_VID[3:0]	R/W	Fh	This field sets the LDOA2 regulator output regulation voltage in normal mode. See 表 6-5 for V_{OUT} options.

6.9.29 LDOA3VID: LDOA3 VID Register (offset = 9Bh) [reset = AAh]

LDOA3VID is shown in 図 6-42 and described in 表 6-36.

Return to Summary Table.

図 6-42. LDOA3VID Register

7	6	5	4	3	2	1	0
LDOA3_SLP_VID[3:0]				LDOA3_VID[3:0]			
R/W-Ah				R/W-Ah			

表 6-36. LDOA3VID Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LDOA3_SLP_VID[3:0]	R/W	Ah	This field sets the LDOA3 regulator output regulation voltage in sleep mode. See 表 6-5 for V_{OUT} options.
3-0	LDOA3_VID[3:0]	R/W	Ah	This field sets the LDOA3 regulator output regulation voltage in normal mode. See 表 6-5 for V_{OUT} options.

6.9.30 BUCK123CTRL: BUCK1-3 Control Register (offset = 9Ch) [reset = 7h]

BUCK123CTRL is shown in 図 6-43 and described in 表 6-37.

Return to Summary Table.

図 6-43. BUCK123CTRL Register

7	6	5	4	3	2	1	0
SPARE		BUCK3_MODE	BUCK2_MODE	BUCK1_MODE	BUCK3_DIS	BUCK2_DIS	BUCK1_DIS
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

表 6-37. BUCK123CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SPARE	R/W	0h	Spare bits.
5	BUCK3_MODE	R/W	0h	This field sets the BUCK3 regulator operating mode. 0h = Automatic mode 1h = Forced PWM mode
4	BUCK2_MODE	R/W	0h	This field sets the BUCK2 regulator operating mode. 0h = Automatic mode 1h = Forced PWM mode
3	BUCK1_MODE	R/W	0h	This field sets the BUCK1 regulator operating mode. 0h = Automatic mode 1h = Forced PWM mode
2	BUCK3_DIS	R/W	1h	BUCK3 disable bit. Writing 0 to this bit forces BUCK3 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable 1h = Enable
1	BUCK2_DIS	R/W	1h	BUCK2 disable bit. Writing 0 to this bit forces BUCK2 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable 1h = Enable
0	BUCK1_DIS	R/W	1h	BUCK1 disable bit. Writing 0 to this bit forces BUCK1 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable 1h = Enable

6.9.31 PG_DELAY2: Power Good Delay2 Register (offset = 9Dh) [reset = 21h]

PG_DELAY2 is shown in 図 6-44 and described in 表 6-38.

Return to Summary Table.

Programmable Power Good delay for GPO1, GPO2, and GPO4 pins, measured from the moment when all VRs assigned to respective GPO reach their regulation range to Power Good assertion. This is an optional register as the PMIC can be programmed for system PG, level shifter or I^2C controller GPO.

図 6-44. PG_DELAY2 Register

7	6	5	4	3	2	1	0
GPO2_PG_DELAY[2:0]			GPO4_PG_DELAY[2:0]			GPO1_PG_DELAY[1:0]	
R/W-1h			R/W-0h			R/W-1h	

表 6-38. PG_DELAY2 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPO2_PG_DELAY[2:0]	R/W	1h	Programmable delay power good or level shifter for GPO2 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation. 0h = 0 ms 1h = 5 ms 2h = 10 ms 3h = 15 ms 4h = 20 ms 5h = 50 ms 6h = 75 ms 7h = 100 ms
4-2	GPO4_PG_DELAY[2:0]	R/W	0h	Programmable delay power good or level shifter for GPO4 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation 0h = 0 ms 1h = 5 ms 2h = 10 ms 3h = 15 ms 4h = 20 ms 5h = 50 ms 6h = 75 ms 7h = 100 ms
1-0	GPO1_PG_DELAY[1:0]	R/W	1h	Programmable delay power good or level shifter for GPO1 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation 0h = 0 ms 1h = 5 ms 2h = 10 ms 3h = 15 ms

6.9.32 SWVTT_DIS: SWVTT Disable Register (offset = 9Fh) [reset = E0h]

SWVTT_DIS is shown in 図 6-45 and described in 表 6-39.

Return to Summary Table.

図 6-45. SWVTT_DIS Register

7	6	5	4	3	2	1	0
SWB2_DIS	SWB1_DIS	SWA1_DIS	VTT_DIS	RESERVED			
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h			

表 6-39. SWVTT_DIS Field Descriptions

Bit	Field	Type	Reset	Description
7	SWB2_DIS	R/W	1h	SWB2 disable bit. Writing 0h to this bit forces SWB2 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable. 1h = Enable.
6	SWB1_DIS	R/W	1h	SWB1 disable bit. Writing 0 to this bit forces SWB1 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable. 1h = Enable.
5	SWA1_DIS	R/W	1h	SWA1 disable bit. Writing 0 to this bit forces SWA1 to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable. 1h = Enable.
4	VTT_DIS	R/W	0h	VTT Disable Bit. Writing 0 to this bit forces VTT to turn off regardless of any control input pin (CTL1–CTL6) status. 0h = Disable. 1h = Enable.
3-0	Reserved	R/W	0h	Reserved, Keep bit set to 0h at all times. Do not write to 1h.

6.9.33 I2C_RAIL_EN1: VR Pin Enable Override1 Register (offset = A0h) [reset = 80h]

I2C_RAIL_EN1 is shown in 図 6-46 and described in 表 6-40.

Return to Summary Table.

図 6-46. I2C_RAIL_EN1 Register

7	6	5	4	3	2	1	0
LDOA2_EN	SWA1_EN	BUCK6_EN	BUCK5_EN	BUCK4_EN	BUCK3_EN	BUCK2_EN	BUCK1_EN
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-40. I2C_RAIL_EN1 Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_EN	R/W	1h	LDOA2 I²C enable 0h = LDOA2 is enabled or disabled by one of the control input pins or internal PG signal. 1h = LDOA2 is forced on unless LDOA2_DIS = 0.
6	SWA1_EN	R/W	0h	SWA1 I²C enable 0h = SWA1 is enabled or disabled by one of the control input pins or internal PG signal. 1h = SWA1 is forced on unless SWA1_DIS = 0.
5	BUCK6_EN	R/W	0h	BUCK6 I²C enable 0h = BUCK6 is enabled or disabled by one of the control input pins or internal PG signal. 1h = BUCK6 is forced on unless BUCK6_DIS = 0.
4	BUCK5_EN	R/W	0h	BUCK5 I²C enable 0h = BUCK5 is enabled or disabled by one of the control input pins or internal PG signal. 1h = BUCK5 is forced on unless BUCK5_DIS = 0.
3	BUCK4_EN	R/W	0h	BUCK4 I²C enable 0h = BUCK4 is enabled or disabled by one of the control input pins or internal PG signal. 1h = BUCK4 is forced on unless BUCK4_DIS = 0.
2	BUCK3_EN	R/W	0h	BUCK3 I²C enable 0h = BUCK3 is enabled or disabled by one of the control input pins or internal PG signal. 1h = BUCK3 is forced on unless BUCK3_DIS = 0.
1	BUCK2_EN	R/W	0h	BUCK2 I²C enable 0h = BUCK2 is enabled or disabled by one of the control input pins or internal PG signal. 1h = BUCK2 is forced on unless BUCK2_DIS = 0.
0	BUCK1_EN	R/W	0h	BUCK1 I²C enable 0h = BUCK1 is enabled or disabled by one of the control input pins or internal PG signal. 1h = BUCK1 is forced on unless BUCK1_DIS = 0.

6.9.34 I2C_RAIL_EN2/GPOCTRL: VR Pin Enable Override2/GPO Control Register (offset = A1h) [reset = 89h]

I2C_RAIL_EN2/GPOCTRL is shown in 図 6-47 and described in 表 6-41.

Return to Summary Table.

図 6-47. I2C_RAIL_EN2/GPOCTRL Register

7	6	5	4	3	2	1	0
GPO4_LVL	GPO3_LVL	GPO2_LVL	GPO1_LVL	VTT_EN	SWB2_EN	SWB1_EN	LDOA3_EN
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-1h

表 6-41. I2C_RAIL_EN2/GPOCTRL Field Descriptions

Bit	Field	Type	Reset	Description
7	GPO4_LVL	R/W	1h	The field is to set GPO4 pin output if the pin is factory-configured as an open-drain general-purpose output. 0h = The pin is driven to logic low. 1h = The pin is driven to logic high.
6	GPO3_LVL	R/W	0h	The field is to set GPO3 pin output if the pin is factory-configured as either an open-drain or a push-pull general-purpose output. 0h = The pin is driven to logic low. 1h = The pin is driven to logic high.
5	GPO2_LVL	R/W	0h	The field is to set GPO2 pin output if the pin is factory-configured as either an open-drain or a push-pull general-purpose output. 0h = The pin is driven to logic low. 1h = The pin is driven to logic high.
4	GPO1_LVL	R/W	0h	The field is to set GPO1 pin output if the pin is factory-configured as either an open-drain or a push-pull general-purpose output. 0h = The pin is driven to logic low. 1h = The pin is driven to logic high.
3	VTT_EN	R/W	1h	VTT LDO I^2C enable 0h = VTT LDO is enabled or disabled by one of the control input pins or internal PG signals. 1h = VTT LDO is forced on unless VTT_DIS = 0.
2	SWB2_EN	R/W	0h	SWB2 I^2C enable 0h = SWB2 is enabled or disabled by one of the control input pins or internal PG signals. 1h = SWB2 is forced on unless SWB2_DIS = 0.
1	SWB1_EN	R/W	0h	SWB1 I^2C enable 0h = SWB1 is enabled or disabled by one of the control input pins or internal PG signals. 1h = SWB1 is forced on unless SWB1_DIS = 0.
0	LDOA3_EN	R/W	1h	LDOA3 I^2C enable 0h = LDOA3 is enabled or disabled by one of the control input pins or internal PG signals. 1h = LDOA3 is forced on unless LDOA3_DIS = 0.

6.9.35 PWR_FAULT_MASK1: VR Power Fault Mask1 Register (offset = A2h) [reset = C0h]

PWR_FAULT_MASK1 is shown in 図 6-48 and described in 表 6-42.

Return to Summary Table.

図 6-48. PWR_FAULT_MASK1 Register

7	6	5	4	3	2	1	0
LDOA2_FLTMSK	SWA1_FLTMSK	BUCK6_FLTMSK	BUCK5_FLTMSK	BUCK4_FLTMSK	BUCK3_FLTMSK	BUCK2_FLTMSK	BUCK1_FLTMSK
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-42. PWR_FAULT_MASK1 Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_FLTMSK	R/W	1h	LDOA2 power fault mask. When masked, power fault from LDOA2 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
6	SWA1_FLTMSK	R/W	1h	SWA1 power fault mask. When masked, power fault from SWA1 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
5	BUCK6_FLTMSK	R/W	0h	BUCK6 power fault mask. When masked, power fault from BUCK6 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
4	BUCK5_FLTMSK	R/W	0h	BUCK5 power fault mask. When masked, power fault from BUCK5 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
3	BUCK4_FLTMSK	R/W	0h	BUCK4 power fault mask. When masked, power fault from BUCK4 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
2	BUCK3_FLTMSK	R/W	0h	BUCK3 power fault mask. When masked, power fault from BUCK3 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
1	BUCK2_FLTMSK	R/W	0h	BUCK2 power fault mask. When masked, power fault from BUCK2 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
0	BUCK1_FLTMSK	R/W	0h	BUCK1 power fault mask. When masked, power fault from BUCK1 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked

6.9.36 PWR_FAULT_MASK2: VR Power Fault Mask2 Register (offset = A3h) [reset = 3Fh]

PWR_FAULT_MASK2 is shown in 図 6-49 and described in 表 6-43.

Return to Summary Table.

図 6-49. PWR_FAULT_MASK2 Register

7	6	5	4	3	2	1	0
RESERVED			LDOA1_FLTMSK	VTT_FLTMSK	SWB2_FLTMSK	SWB1_FLTMSK	LDOA3_FLTMSK
R-1h			R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 6-43. PWR_FAULT_MASK2 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	1h	
4	LDOA1_FLTMSK	R/W	1h	LDOA1 power fault mask. When masked, power fault from LDOA1 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
3	VTT_FLTMSK	R/W	1h	VTT LDO Power Fault Mask. When masked, power fault from VTT LDO does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
2	SWB2_FLTMSK	R/W	1h	SWB2 power fault mask. When masked, power fault from SWB2 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
1	SWB1_FLTMSK	R/W	1h	SWB1 power fault mask. When masked, power fault from SWB1 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked
0	LDOA3_FLTMSK	R/W	1h	LDOA3 power fault mask. When masked, power fault from LDOA3 does not cause PMIC to shutdown. 0h = Not masked 1h = Masked

6.9.37 GPO1PG_CTRL1: GPO1 PG Control1 Register (offset = A4h) [reset = C2h]

GPO1PG_CTRL1 is shown in 図 6-50 and described in 表 6-44.

Return to Summary Table.

図 6-50. GPO1PG_CTRL1 Register

7	6	5	4	3	2	1	0
LDOA2_MSK	SWA1_MSK	BUCK6_MSK	BUCK5_MSK	BUCK4_MSK	BUCK3_MSK	BUCK2_MSK	BUCK1_MSK
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

表 6-44. GPO1PG_CTRL1 Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_MSK	R/W	1h	0h = LDOA2 PG is part of power good tree of GPO1 pin. 1h = LDOA2 PG is NOT part of power good tree of GPO1 pin and is ignored.
6	SWA1_MSK	R/W	1h	0h = SWA1 PG is part of power good tree of GPO1 pin. 1h = SWA1 PG is NOT part of power good tree of GPO1 pin and is ignored.
5	BUCK6_MSK	R/W	0h	0h = BUCK6 PG is part of power good tree of GPO1 pin. 1h = BUCK6 PG is NOT part of power good tree of GPO1 pin and is ignored.
4	BUCK5_MSK	R/W	0h	0h = BUCK5 PG is part of power good tree of GPO1 pin. 1h = BUCK5 PG is NOT part of power good tree of GPO1 pin and is ignored.
3	BUCK4_MSK	R/W	0h	0h = BUCK4 PG is part of power good tree of GPO1 pin. 1h = BUCK4 PG is NOT part of power good tree of GPO1 pin and is ignored.
2	BUCK3_MSK	R/W	0h	0h = BUCK3 PG is part of power good tree of GPO1 pin. 1h = BUCK3 PG is NOT part of power good tree of GPO1 pin and is ignored.
1	BUCK2_MSK	R/W	1h	0h = BUCK2 PG is part of power good tree of GPO1 pin. 1h = BUCK2 PG is NOT part of power good tree of GPO1 pin and is ignored.
0	BUCK1_MSK	R/W	0h	0h = BUCK1 PG is part of power good tree of GPO1 pin. 1h = BUCK1 PG is NOT part of power good tree of GPO1 pin and is ignored.

6.9.38 GPO1PG_CTRL2: GPO1 PG Control2 Register (offset = A5h) [reset = AFh]

GPO1PG_CTRL2 is shown in 図 6-51 and described in 表 6-45.

Return to Summary Table.

図 6-51. GPO1PG_CTRL2 Register

7	6	5	4	3	2	1	0
CTL5_MSK	CTL4_MSK	CTL2_MSK	CTL1_MSK	VTT_MSK	SWB2_MSK	SWB1_MSK	LDOA3_MSK
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 6-45. GPO1PG_CTRL2 Field Descriptions

Bit	Field	Type	Reset	Description
7	CTL5_MSK	R/W	1h	0h = CTL5 pin status is part of power good tree of GPO1 pin. 1h = CTL5 pin status is NOT part of power good tree of GPO1 pin and is ignored.
6	CTL4_MSK	R/W	0h	0h = CTL4 pin status is part of power good tree of GPO1 pin. 1h = CTL4 pin status is NOT part of power good tree of GPO1 pin and is ignored.
5	CTL2_MSK	R/W	1h	0h = CTL2 pin status is part of power good tree of GPO1 pin. 1h = CTL2 pin status is NOT part of power good tree of GPO1 pin and is ignored.
4	CTL1_MSK	R/W	0h	0h = CTL1 pin status is part of power good tree of GPO1 pin. 1h = CTL1 pin status is NOT part of power good tree of GPO1 pin and is ignored.
3	VTT_MSK	R/W	1h	0h = VTT LDO PG is part of power good tree of GPO1 pin. 1h = VTT LDO PG is NOT part of power good tree of GPO1 pin and is ignored.
2	SWB2_MSK	R/W	1h	0h = SWB2 pin status is part of power good tree of GPO1 pin. 1h = SWB2 pin status is NOT part of power good tree of GPO1 pin and is ignored.
1	SWB1_MSK	R/W	1h	0h = SWB1 PG is part of power good tree of GPO1 pin. 1h = SWB1 PG is NOT part of power good tree of GPO1 pin and is ignored.
0	LDOA3_MSK	R/W	1h	0h = LDOA3 PG is part of power good tree of GPO1 pin. 1h = LDOA3 PG is NOT part of power good tree of GPO1 pin and is ignored.

6.9.39 GPO4PG_CTRL1: GPO4 PG Control1 Register (offset = A6h) [reset = 0h]

GPO4PG_CTRL1is shown in 図 6-52 and described in 表 6-46.

Return to Summary Table.

図 6-52. GPO4PG_CTRL1 Register

7	6	5	4	3	2	1	0
LDOA2_MSK	SWA1_MSK	BUCK6_MSK	BUCK5_MSK	BUCK4_MSK	BUCK3_MSK	BUCK2_MSK	BUCK1_MSK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-46. GPO4PG_CTRL1 Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_MSK	R/W	0h	0h = LDOA2 PG is part of power good tree of GPO4 pin. 1h = LDOA2 PG is NOT part of power good tree of GPO4 pin and is ignored.
6	SWA1_MSK	R/W	0h	0h = SWA1 PG is part of power good tree of GPO4 pin. 1h = SWA1 PG is NOT part of power good tree of GPO4 pin and is ignored.
5	BUCK6_MSK	R/W	0h	0h = BUCK6 PG is part of power good tree of GPO4 pin. 1h = BUCK6 PG is NOT part of power good tree of GPO4 pin and is ignored.
4	BUCK5_MSK	R/W	0h	0h = BUCK5 PG is part of power good tree of GPO4 pin. 1h = BUCK5 PG is NOT part of power good tree of GPO4 pin and is ignored.
3	BUCK4_MSK	R/W	0h	0h = BUCK4 PG is part of power good tree of GPO4 pin. 1h = BUCK4 PG is NOT part of power good tree of GPO4 pin and is ignored.
2	BUCK3_MSK	R/W	0h	0h = BUCK3 PG is part of power good tree of GPO4 pin. 1h = BUCK3 PG is NOT part of power good tree of GPO4 pin and is ignored.
1	BUCK2_MSK	R/W	0h	0h = BUCK2 PG is part of power good tree of GPO4 pin. 1h = BUCK2 PG is NOT part of power good tree of GPO4 pin and is ignored.
0	BUCK1_MSK	R/W	0h	0h = BUCK1 PG is part of power good tree of GPO4 pin. 1h = BUCK1 PG is NOT part of power good tree of GPO4 pin and is ignored.

6.9.40 GPO4PG_CTRL2: GPO4 PG Control2 Register (offset = A7h) [reset = 0h]

GPO4PG_CTRL2 is shown in 図 6-53 and described in 表 6-47.

Return to Summary Table.

図 6-53. GPO4PG_CTRL2 Register

7	6	5	4	3	2	1	0
CTL5_MSK	CTL4_MSK	CTL2_MSK	CTL1_MSK	VTT_MSK	SWB2_MSK	SWB1_MSK	LDOA3_MSK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-47. GPO4PG_CTRL2 Field Descriptions

Bit	Field	Type	Reset	Description
7	CTL5_MSK	R/W	0h	0h = CTL5 pin status is part of power good tree of GPO4 pin. 1h = CTL5 pin status is NOT part of power good tree of GPO4 pin and is ignored.
6	CTL4_MSK	R/W	0h	0h = CTL4 pin status is part of power good tree of GPO4 pin. 1h = CTL4 pin status is NOT part of power good tree of GPO4 pin and is ignored.
5	CTL2_MSK	R/W	0h	0h = CTL2 pin status is part of power good tree of GPO4 pin. 1h = CTL2 pin status is NOT part of power good tree of GPO4 pin and is ignored.
4	CTL1_MSK	R/W	0h	0h = CTL1 pin status is part of power good tree of GPO4 pin. 1h = CTL1 pin status is NOT part of power good tree of GPO4 pin and is ignored.
3	VTT_MSK	R/W	0h	0h = VTT LDO PG is part of power good tree of GPO4 pin. 1h = VTT LDO PG is NOT part of power good tree of GPO4 pin and is ignored.
2	SWB2_MSK	R/W	0h	0h = SWB2 pin status is part of power good tree of GPO4 pin. 1h = SWB2 pin status is NOT part of power good tree of GPO4 pin and is ignored.
1	SWB1_MSK	R/W	0h	0h = SWB1 PG is part of power good tree of GPO4 pin. 1h = SWB1 PG is NOT part of power good tree of GPO4 pin and is ignored.
0	LDOA3_MSK	R/W	0h	0h = LDOA3 PG is part of power good tree of GPO4 pin. 1h = LDOA3 PG is NOT part of power good tree of GPO4 pin and is ignored.

6.9.41 GPO2PG_CTRL1: GPO2 PG Control1 Register (offset = A8h) [reset = C0h]

GPO2PG_CTRL1 is shown in 図 6-54 and described in 表 6-48.

Return to Summary Table.

図 6-54. GPO2PG_CTRL1 Register

7	6	5	4	3	2	1	0
LDOA2_MSK	SWA1_MSK	BUCK6_MSK	BUCK5_MSK	BUCK4_MSK	BUCK3_MSK	BUCK2_MSK	BUCK1_MSK
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-48. GPO2PG_CTRL1 Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_MSK	R/W	1h	0h = LDOA2 PG is part of power good tree of GPO2 pin. 1h = LDOA2 PG is NOT part of power good tree of GPO2 pin and is ignored.
6	SWA1_MSK	R/W	1h	0h = SWA1 PG is part of power good tree of GPO2 pin. 1h = SWA1 PG is NOT part of power good tree of GPO2 pin and is ignored.
5	BUCK6_MSK	R/W	0h	0h = BUCK6 PG is part of power good tree of GPO2 pin. 1h = BUCK6 PG is NOT part of power good tree of GPO2 pin and is ignored.
4	BUCK5_MSK	R/W	0h	0h = BUCK5 PG is part of power good tree of GPO2 pin. 1h = BUCK5 PG is NOT part of power good tree of GPO2 pin and is ignored.
3	BUCK4_MSK	R/W	0h	0h = BUCK4 PG is part of power good tree of GPO2 pin. 1h = BUCK4 PG is NOT part of power good tree of GPO2 pin and is ignored.
2	BUCK3_MSK	R/W	0h	0h = BUCK3 PG is part of power good tree of GPO2 pin. 1h = BUCK3 PG is NOT part of power good tree of GPO2 pin and is ignored.
1	BUCK2_MSK	R/W	0h	0h = BUCK2 PG is part of power good tree of GPO2 pin. 1h = BUCK2 PG is NOT part of power good tree of GPO2 pin and is ignored.
0	BUCK1_MSK	R/W	0h	0h = BUCK1 PG is part of power good tree of GPO2 pin. 1h = BUCK1 PG is NOT part of power good tree of GPO2 pin and is ignored.

6.9.42 GPO2PG_CTRL2: GPO2 PG Control2 Register (offset = A9h) [reset = 2Fh]

GPO2PG_CTRL2 is shown in 図 6-55 and described in 表 6-49.

Return to Summary Table.

図 6-55. GPO2PG_CTRL2 Register

7	6	5	4	3	2	1	0
CTL5_MSK	CTL4_MSK	CTL2_MSK	CTL1_MSK	VTT_MSK	SWB2_MSK	SWB1_MSK	LDOA3_ MSK
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 6-49. GPO2PG_CTRL2 Field Descriptions

Bit	Field	Type	Reset	Description
7	CTL5_MSK	R/W	0h	0h = CTL5 pin status is part of power good tree of GPO2 pin. 1h = CTL5 pin status is NOT part of power good tree of GPO2 pin and is ignored.
6	CTL4_MSK	R/W	0h	0h = CTL4 pin status is part of power good tree of GPO2 pin. 1h = CTL4 pin status is NOT part of power good tree of GPO2 pin and is ignored.
5	CTL2_MSK	R/W	1h	0h = CTL2 pin status is part of power good tree of GPO2 pin. 1h = CTL2 pin status is NOT part of power good tree of GPO2 pin and is ignored.
4	CTL1_MSK	R/W	0h	0h = CTL1 pin status is part of power good tree of GPO2 pin. 1h = CTL1 pin status is NOT part of power good tree of GPO2 pin and is ignored.
3	VTT_MSK	R/W	1h	0h = VTT LDO PG is part of power good tree of GPO2 pin. 1h = VTT LDO PG is NOT part of power good tree of GPO2 pin and is ignored.
2	SWB2_MSK	R/W	1h	0h = SWB2 pin status is part of power good tree of GPO2 pin. 1h = SWB2 pin status is NOT part of power good tree of GPO2 pin and is ignored.
1	SWB1_MSK	R/W	1h	0h = SWB1 PG is part of power good tree of GPO2 pin. 1h = SWB1 PG is NOT part of power good tree of GPO2 pin and is ignored.
0	LDOA3_MSK	R/W	1h	0h = LDOA3 PG is part of power good tree of GPO2 pin. 1h = LDOA3 PG is NOT part of power good tree of GPO2 pin and is ignored.

6.9.43 GPO3PG_CTRL1: GPO3 PG Control1 Register (offset = AAh) [reset = 0h]

GPO3PG_CTRL1 is shown in 図 6-56 and described in 表 6-50.

Return to Summary Table.

図 6-56. GPO3PG_CTRL1 Register

7	6	5	4	3	2	1	0
LDOA2_MSK	SWA1_MSK	BUCK6_MSK	BUCK5_MSK	BUCK4_MSK	BUCK3_MSK	BUCK2_MSK	BUCK1_MSK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-50. GPO3PG_CTRL1 Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_MSK	R/W	0h	0h = LDOA2 PG is part of power good tree of GPO3 pin. 1h = LDOA2 PG is NOT part of power good tree of GPO3 pin and is ignored.
6	SWA1_MSK	R/W	0h	0h = SWA1 PG is part of power good tree of GPO3 pin. 1h = SWA1 PG is NOT part of power good tree of GPO3 pin and is ignored.
5	BUCK6_MSK	R/W	0h	0h = BUCK6 PG is part of power good tree of GPO3 pin. 1h = BUCK6 PG is NOT part of power good tree of GPO3 pin and is ignored.
4	BUCK5_MSK	R/W	0h	0h = BUCK5 PG is part of power good tree of GPO3 pin. 1h = BUCK5 PG is NOT part of power good tree of GPO3 pin and is ignored.
3	BUCK4_MSK	R/W	0h	0h = BUCK4 PG is part of power good tree of GPO3 pin. 1h = BUCK4 PG is NOT part of power good tree of GPO3 pin and is ignored.
2	BUCK3_MSK	R/W	0h	0h = BUCK3 PG is part of power good tree of GPO3 pin. 1h = BUCK3 PG is NOT part of power good tree of GPO3 pin and is ignored.
1	BUCK2_MSK	R/W	0h	0h = BUCK2 PG is part of power good tree of GPO3 pin. 1h = BUCK2 PG is NOT part of power good tree of GPO3 pin and is ignored.
0	BUCK1_MSK	R/W	0h	0h = BUCK1 PG is part of power good tree of GPO3 pin. 1h = BUCK1 PG is NOT part of power good tree of GPO3 pin and is ignored.

6.9.44 GPO3PG_CTRL2: GPO3 PG Control2 Register (offset = ABh) [reset = 0h]

GPO3PG_CTRL2 is shown in 図 6-57 and described in 表 6-51.

Return to Summary Table.

図 6-57. GPO3PG_CTRL2 Register

7	6	5	4	3	2	1	0
CTL5_MSK	CTL4_MSK	CTL2_MSK	CTL1_MSK	VTT_MSK	SWB2_MSK	SWB1_MSK	LDOA3_MSK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-51. GPO3PG_CTRL2 Field Descriptions

Bit	Field	Type	Reset	Description
7	CTL5_MSK	R/W	0h	0h = CTL5 pin status is part of power good tree of GPO3 pin. 1h = CTL5 pin status is NOT part of power good tree of GPO3 pin and is ignored.
6	CTL4_MSK	R/W	0h	0h = CTL4 pin status is part of power good tree of GPO3 pin. 1h = CTL4 pin status is NOT part of power good tree of GPO3 pin and is ignored.
5	CTL2_MSK	R/W	0h	0h = CTL2 pin status is part of power good tree of GPO3 pin. 1h = CTL2 pin status is NOT part of power good tree of GPO3 pin and is ignored.
4	CTL1_MSK	R/W	0h	0h = CTL1 pin status is part of power good tree of GPO3 pin. 1h = CTL1 pin status is NOT part of power good tree of GPO3 pin and is ignored.
3	VTT_MSK	R/W	0h	0h = VTT LDO PG is part of power good tree of GPO3 pin. 1h = VTT LDO PG is NOT part of power good tree of GPO3 pin and is ignored.
2	SWB2_MSK	R/W	0h	0h = SWB2 pin status is part of power good tree of GPO3 pin. 1h = SWB2 pin status is NOT part of power good tree of GPO3 pin and is ignored.
1	SWB1_MSK	R/W	0h	0h = SWB1 PG is part of power good tree of GPO3 pin. 1h = SWB1 PG is NOT part of power good tree of GPO3 pin and is ignored.
0	LDOA3_MSK	R/W	0h	0h = LDOA3 PG is part of power good tree of GPO3 pin. 1h = LDOA3 PG is NOT part of power good tree of GPO3 pin and is ignored.

6.9.45 MISCSYSPG Register (offset = ACh) [reset = FFh]

MISCSYSPG is shown in 図 6-58 and described in 表 6-52.

Return to Summary Table.

図 6-58. MISCSYSPG Register

7	6	5	4	3	2	1	0
GPO3_CTL6_MSK	GPO3_CTL3_MSK	GPO2_CTL6_MSK	GPO2_CTL3_MSK	GPO4_CTL6_MSK	GPO4_CTL3_MSK	GPO1_CTL6_MSK	GPO1_CTL3_MSK
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 6-52. MISCSYSPG Field Descriptions

Bit	Field	Type	Reset	Description
7	GPO3_CTL6_MSK	R/W	1h	0h = CTL6 pin status is part of power good tree of GPO3 pin. 1h = CTL6 pin status is NOT part of power good tree of GPO3 pin.
6	GPO3_CTL3_MSK	R/W	1h	0h = CTL3 pin status is part of power good tree of GPO3 pin. 1h = CTL3 pin status is NOT part of power good tree of GPO3 pin.
5	GPO2_CTL6_MSK	R/W	1h	0h = CTL6 pin status is part of power good tree of GPO2 pin. 1h = CTL6 pin status is NOT part of power good tree of GPO2 pin.
4	GPO2_CTL3_MSK	R/W	1h	0h = CTL3 pin status is part of power good tree of GPO2 pin. 1h = CTL3 pin status is NOT part of power good tree of GPO2 pin.
3	GPO4_CTL6_MSK	R/W	1h	0h = CTL6 pin status is part of power good tree of GPO4 pin. 1h = CTL6 pin status is NOT part of power good tree of GPO4 pin.
2	GPO4_CTL3_MSK	R/W	1h	0h = CTL3 pin status is part of power good tree of GPO4 pin. 1h = CTL3 pin status is NOT part of power good tree of GPO4 pin.
1	GPO1_CTL6_MSK	R/W	1h	0h = CTL6 pin status is part of power good tree of GPO1 pin. 1h = CTL6 pin status is NOT part of power good tree of GPO1 pin.
0	GPO1_CTL3_MSK	R/W	1h	0h = CTL3 pin status is part of power good tree of GPO1 pin. 1h = CTL3 pin status is NOT part of power good tree of GPO1 pin.

6.9.46 LDOA1CTRL: LDOA1 Control Register (offset = AEh) [reset = 7Dh]

LDOA1CTRL is shown in 図 6-59 and described in 表 6-53.

Return to Summary Table.

図 6-59. LDOA1CTRL Register

7	6	5	4	3	2	1	0
LDOA1_DISCHG[1:0]		LDOA1_SDWN_CONFIG	LDOA1_VID[3:0]				LDOA1_EN
R/W-1h		R/W-1h	R/W-Eh				R/W-1h

表 6-53. LDOA1CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LDOA1_DISCHG[1:0]	R/W	1h	LDOA1 discharge resistance 0h = no discharge 1h = 100 Ω 2h = 200 Ω 3h = 500 Ω
5	LDOA1_SDWN_CONFIG	R/W	1h	Control for Disabling LDOA1 during Emergency Shutdown 0h = LDOA1 will turn off during Emergency Shutdown for factory-programmable duration of 1 ms, 5 ms, 10 ms, or 100 ms. 1h = LDOA1 is controlled by LDOA1_EN bit only.
4-1	LDOA1_VID[3:0]	R/W	Eh	This field sets the LDOA1 regulator output regulation voltage. See 表 6-4 for V_{OUT} options.
0	LDOA1_EN	R/W	1h	LDOA1 Enable Bit. 0h = Disable. 1h = Enable.

6.9.47 PG_STATUS1: Power Good Status1 Register (offset = B0h) [reset = 0h]

PG_STATUS1 is shown in 図 6-60 and described in 表 6-54.

Return to Summary Table.

図 6-60. PG_STATUS1 Register

7	6	5	4	3	2	1	0
LDOA2_PGOOD	SWA1_PGOOD	BUCK6_PGOOD	BUCK5_PGOOD	BUCK4_PGOOD	BUCK3_PGOOD	BUCK2_PGOOD	BUCK1_PGOOD
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 6-54. PG_STATUS1 Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_PGOOD	R	0h	LDOA2 power good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
6	SWA1_PGOOD	R	0h	SWA1 power good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
5	BUCK6_PGOOD	R	0h	BUCK6 power good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
4	BUCK5_PGOOD	R	0h	BUCK5 power good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
3	BUCK4_PGOOD	R	0h	BUCK4 power good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
2	BUCK3_PGOOD	R	0h	BUCK3 power good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
1	BUCK2_PGOOD	R	0h	BUCK2 power good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
0	BUCK1_PGOOD	R	0h	BUCK1 power good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.

6.9.48 PG_STATUS2: Power Good Status2 Register (offset = B1h) [reset = 0h]

PG_STATUS2 is shown in 図 6-61 and described in 表 6-55.

Return to Summary Table.

図 6-61. PG_STATUS2 Register

7	6	5	4	3	2	1	0
RESERVED		LDO5_PGOOD	LDOA1_PGOOD	VTT_PGOOD	SWB2_PGOOD	SWB1_PGOOD	LDOA3_PGOOD
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 6-55. PG_STATUS2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	LDO5_PGOOD	R	0h	LDO5 Power Good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
4	LDOA1_PGOOD	R	0h	LDOA1 Power Good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
3	VTT_PGOOD	R	0h	VTT LDO Power Good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
2	SWB2_PGOOD	R	0h	SWB2 Power Good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
1	SWB1_PGOOD	R	0h	SWB1 Power Good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.
0	LDOA3_PGOOD	R	0h	LDOA3 Power Good status. 0h = The output is not in target regulation range. 1h = The output is in target regulation range.

6.9.49 PWR_FAULT_STATUS1: Power Fault Status1 Register (offset = B2h) [reset = 0h]

PWR_FAULT_STATUS1 is shown in 図 6-62 and described in 表 6-56.

Return to Summary Table.

図 6-62. PWR_FAULT_STATUS1 Register

7	6	5	4	3	2	1	0
LDOA2_PWRFLT	SWA1_PWRFLT	BUCK6_PWRFLT	BUCK5_PWRFLT	BUCK4_PWRFLT	BUCK3_PWRFLT	BUCK2_PWRFLT	BUCK1_PWRFLT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-56. PWR_FAULT_STATUS1 Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_PWRFLT	R	0h	This fields indicates that LDOA2 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
6	SWA1_PWRFLT	R	0h	This fields indicates that SWA1 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
5	BUCK6_PWRFLT	R	0h	This fields indicates that BUCK6 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
4	BUCK5_PWRFLT	R	0h	This fields indicates that BUCK5 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
3	BUCK4_PWRFLT	R	0h	This fields indicates that BUCK4 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
2	BUCK3_PWRFLT	R	0h	This fields indicates that BUCK3 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
1	BUCK2_PWRFLT	R	0h	This fields indicates that BUCK2 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
0	BUCK1_PWRFLT	R	0h	This fields indicates that BUCK1 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.

6.9.50 PWR_FAULT_STATUS2: Power Fault Status2 Register (offset = B3h) [reset = 0h]

PWR_FAULT_STATUS2 is shown in 図 6-63 and described in 表 6-57.

Return to Summary Table.

図 6-63. PWR_FAULT_STATUS2 Register

7	6	5	4	3	2	1	0
RESERVED			LDOA1_PWRFLT	VTT_PWRFLT	SWB2_PWRFLT	SWB1_PWRFLT	LDOA3_PWRFLT
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-57. PWR_FAULT_STATUS2 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	LDOA1_PWRFLT	R/W	0h	This fields indicates that LDOA1 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
3	VTT_PWRFLT	R/W	0h	This fields indicates that VTT LDO has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
4	SWB2_PWRFLT	R/W	0h	This fields indicates that SWB2 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
3	SWB1_PWRFLT	R/W	0h	This fields indicates that SWB1 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.
0	LDOA3_PWRFLT	R/W	0h	This fields indicates that LDOA3 has lost its regulation. 0h = No Fault. 1h = Power fault has occurred. The host to write 1 to clear.

6.9.51 TEMPCRIT: Temperature Fault Status Register (offset = B4h) [reset = 0h]

TEMPCRIT is shown in 図 6-64 and described in 表 6-58.

Return to Summary Table.

Asserted when an internal temperature sensor detects rise of die temperature above the CRITICAL temperature threshold (T_{CRIT}). There are 5 temperature sensors across the die.

図 6-64. TEMPCRIT Register

7	6	5	4	3	2	1	0
RESERVED			DIE_CRIT	VTT_CRIT	TOP-RIGHT_CRIT	TOP-LEFT_CRIT	BOTTOM-RIGHT_CRIT
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-58. TEMPCRIT Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	DIE_CRIT	R/W	0h	Temperature of rest of die has exceeded T_{CRIT}. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
3	VTT_CRIT	R/W	0h	Temperature of VTT LDO has exceeded T_{CRIT}. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
2	TOP-RIGHT_CRIT	R/W	0h	Temperature of die Top-Right has exceeded T_{CRIT}. Top-Right corner of die from top view given pin1 is in Top-Left corner. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
1	TOP-LEFT_CRIT	R/W	0h	Temperature of die Top-Left has exceeded T_{CRIT}.Top-Left corner of die from top view given pin1 is in Top-Left corner. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
0	BOTTOM-RIGHT_CRIT	R/W	0h	Temperature of die Bottom-Right has exceeded T_{CRIT}. Bottom-Right corner of die from top view given pin1 is in Top-Left corner. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.

6.9.52 TEMPHOT: Temperature Hot Status Register (offset = B5h) [reset = 0h]

TEMPHOT is shown in 図 6-65 and described in 表 6-59.

Return to Summary Table.

Asserted when an internal temperature sensor detects rise of die temperature above the HOT temperature threshold (T_{HOT}). There are 5 temperature sensors across the die.

図 6-65. TEMPHOT Register

7	6	5	4	3	2	1	0
RESERVED			DIE_HOT	VTT_HOT	TOP-RIGHT_HOT	TOP-LEFT_HOT	BOTTOM-RIGHT_HOT
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-59. TEMPHOT Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	DIE_HOT	R/W	0h	Temperature of rest of die has exceeded T_{HOT}. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
3	VTT_HOT	R/W	0h	Temperature of VTT LDO has exceeded T_{HOT}. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
2	TOP-RIGHT_HOT	R/W	0h	Temperature of Top-Right has exceeded T_{HOT}. Top-Right corner of die from top view given pin1 is in Top-Left corner. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
1	TOP-LEFT_HOT	R/W	0h	Temperature of Top-Left has exceeded THOT. Top-Left corner of die from top view given pin1 is in Top-Left corner. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
0	BOTTOM-RIGHT_HOT	R/W	0h	Temperature of Bottom-Right has exceeded T_{HOT}. Bottom-Right corner of die from top view given pin1 is in Top-Left corner. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.

6.9.53 OC_STATUS: Overcurrent Fault Status Register (offset = B6h) [reset = 0h]

OC_STATUS is shown in 図 6-66 and described in 表 6-60.

Return to Summary Table.

Asserted when overcurrent condition is detected from a LSD FET.

図 6-66. OC_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					BUCK6_OC	BUCK2_OC	BUCK1_OC
R-0h					R/W-0h	R/W-0h	R/W-0h

表 6-60. OC_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	BUCK6_OC	R/W	0h	BUCK6 LSD FET overcurrent has been detected. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
1	BUCK2_OC	R/W	0h	BUCK2 LSD FET overcurrent has been detected. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.
0	BUCK1_OC	R/W	0h	BUCK1 LSD FET overcurrent has been detected. 0h = Not asserted. 1h = Asserted. The host to write 1 to clear.

7 Applications, Implementation, and Layout

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The TPS6508700 device can be used in several different applications from computing, industrial interfacing and much more. セクション 7.2 describes the general application information and provides a more detailed description on the TPS6508700 device that powers the AMD system. 図 7-2 shows the functional block diagram for the device, which outlines the typical external connections required for proper device functionality.

7.2 Typical Application

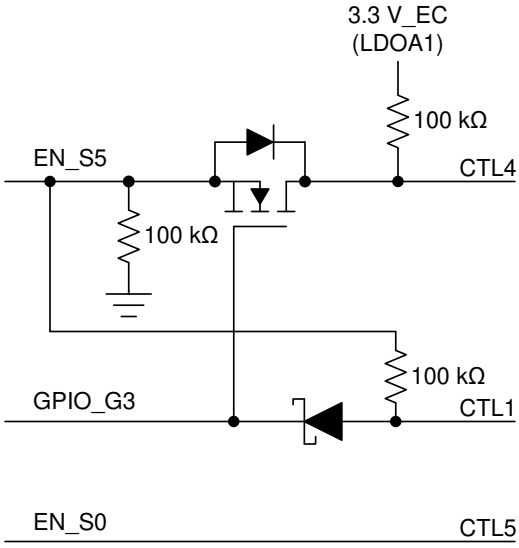

図 7-1. CTL Pin Implementation Option

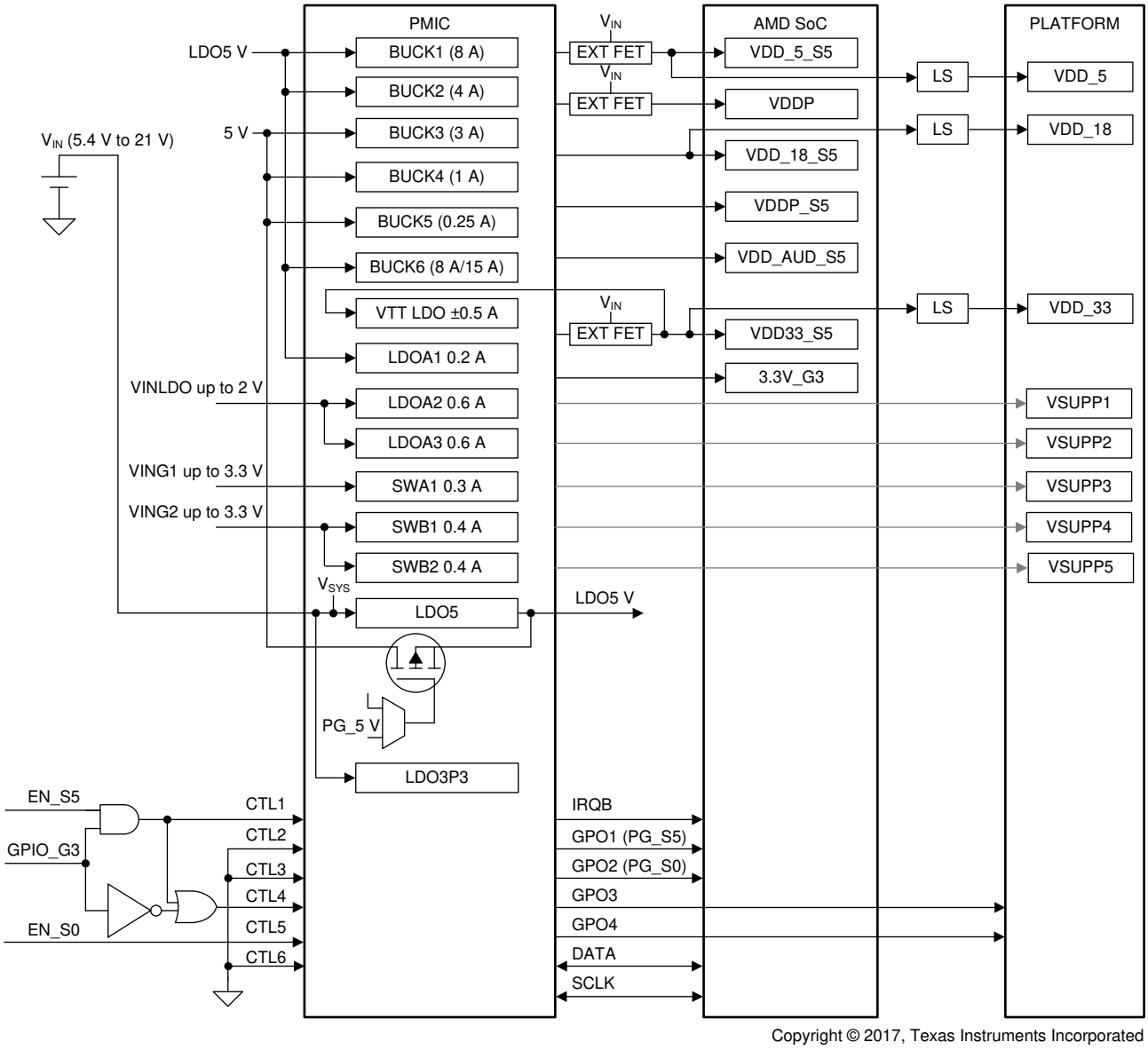

図 7-2. Typical Application Example

7.2.1 Design Requirements

The TPS6508700 device requires decoupling capacitors on the supply pins. Follow the values for recommended capacitance on these supplies given in セクション 5. The controllers, converter, LDOs, and some other features can be adjusted to meet specific application needs. セクション 7.2.2 describes how to design and adjust the external components to achieve the desired performance. In most cases, the controller and converter designs should be copied directly from the AMD reference design. If significant changes must be made, some guidelines are provided in セクション 7.2.2.

7.2.2 Detailed Design Procedure

7.2.2.1 Controller Design Procedure

Designing the controller can be broken down into the following steps:

1. Design the output filter
2. Select the FETs
3. Select the bootstrap capacitor
4. Select the input capacitors
5. Set the current limits

The BUCK1, BUCK2, and BUCK6 controllers require a 5-V supply and capacitors at their corresponding DRV5V_x_x pins. For most applications, the DRV5V_x_x input must come from the LDO5P0 pin to ensure uninterrupted supply voltage. A 2.2-µF, X5R, 20%, 10-V, or similar capacitor must be used for decoupling.

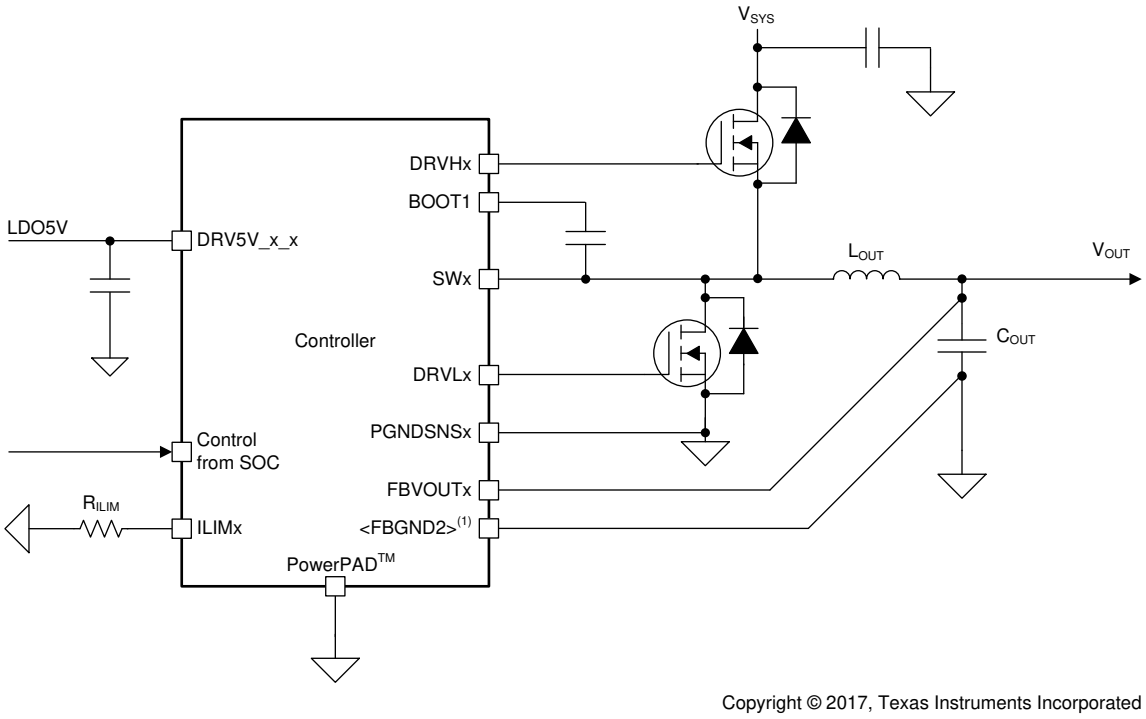

図 7-3. Controller Diagram

7.2.2.1.1 Controller With External Feedback Resistor

For BUCK1, the voltage can be set using external feedback resistor. For all other bucks, the voltage is set by the default OTP settings and no resistor divider is required. For BUCK1, The internal voltage reference is set to 0.4 V.The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using a 1% tolerance or better to get accurate number. Use 式 3 to calculate the value of R2.

$$R2 = R1 \, (0.4 / V_O - 0.4) \quad (3)$$

To set the output voltage to 5 V, use a value of 294 kΩ for R1 and 25.5 kΩ for R2.

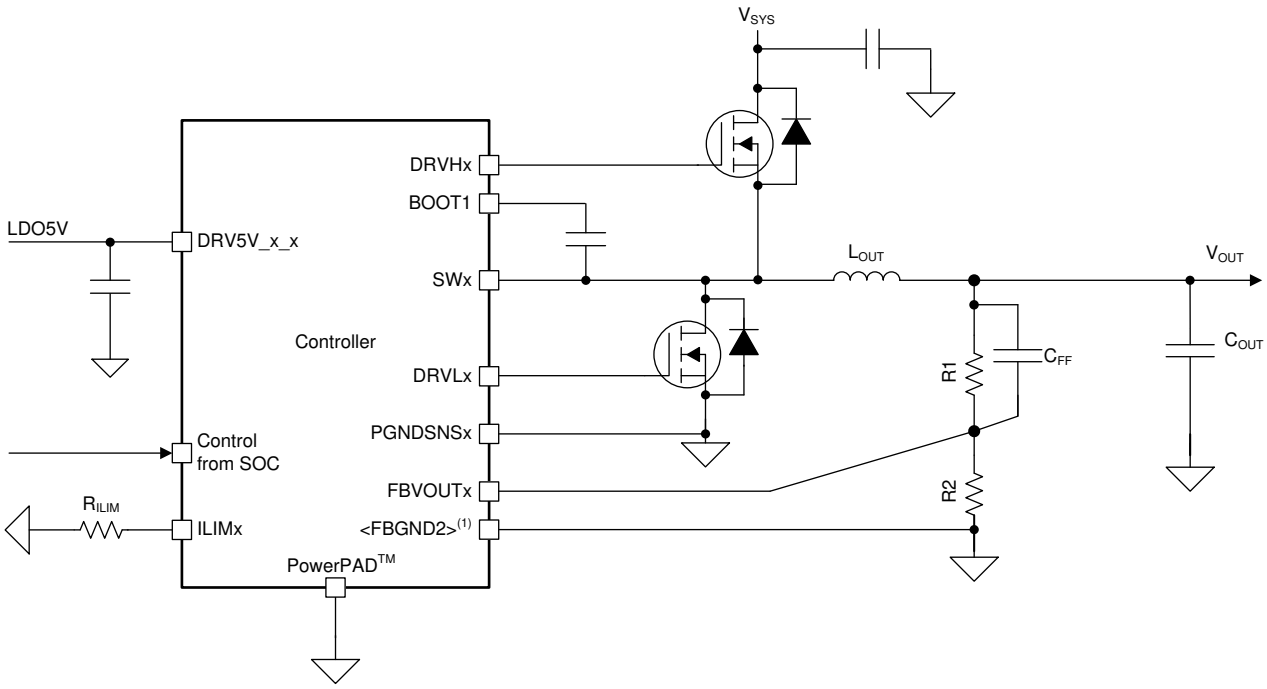

図 7-4. Controller Diagram With External Feedback Resistor

7.2.2.1.2 Selecting the Inductor

Placement of an inductor is required between the external FETs and the output capacitors. Together, the inductor and output capacitors make the double-pole that contributes to stability. Additionally, the inductor is directly responsible for the output ripple, efficiency, and transient performance. As the inductance used increases, the ripple current decreases, which typically results in increased efficiency. However, as the inductance used increases, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DC resistance (DCR).

Use 式 4 to calculate the recommended inductance for the controller.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{sw} \times I_{OUT(MAX)} \times K_{IND}} \tag{4}$$

where

- V_{OUT} is the typical output voltage.
- V_{IN} is the typical input voltage.
- f_{SW} is the typical switching frequency.
- $I_{OUT(MAX)}$ is the maximum load current.
- K_{IND} is the ratio of $I_{Lripple}$ to the $I_{OUT(MAX)}$. For this application, TI recommends that K_{IND} is set to a value from 0.2 to 0.4.

With the chosen inductance value, the peak current for the inductor in steady state operation, $I_{L(MAX)}$, can be calculated using 式 5. The rated saturation current of the inductor must be higher than the $I_{L(MAX)}$ current.

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{sw} \times L} \tag{5}$$

7.2.2.1.3 Selecting the Output Capacitors

TI recommends using ceramic capacitors with low ESR values to provide the lowest output voltage ripple. The output capacitor requires an X7R or an X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the controller operates in PFM mode, and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve the specified regulation performance and low output-voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

TI recommends using small ceramic capacitors placed between the inductor and load with many vias to the power ground (PGND) plane for the output capacitors of the buck controllers. This solution typically provides the smallest and lowest cost solution available for D-CAP2 controllers.

The selection of the output capacitor is typically driven by the output transient response. 式 6 provides a rough estimate of the minimum required capacitance to ensure proper transient response. Because the transient response is significantly affected by the board layout, some experimentation is expected to confirm that values derived in this section are applicable to any particular use case. 式 6 is not meant to be an absolute requirement, but rather a rough starting point. Alternatively, some known combination values from which to begin are provided in 表 7-1.

$$C_{OUT} > \frac{I_{TRAN(MAX)}{}^2 \times L}{(V_{IN} - V_{OUT}) \times V_{UNDER}} \quad (6)$$

where

- $I_{TRAN(MAX)}$ is the maximum load current step.
- L is the chosen inductance.
- V_{OUT} is the minimum programmed output voltage.
- V_{IN} is the maximum input voltage.
- V_{UNDER} is the minimum allowable undershoot from the programmable voltage.

In cases where the transient current change is very low, the DC stability may become important. Use 式 7 to calculate the approximate amount of capacitance required to maintain DC stability. Again, this equation is provided as a starting point; actual values will vary on a board-to-board case.

$$C_{OUT} > \frac{V_{OUT} \times 50\ \mu s}{V_{IN} \times f_{SW} \times L} \quad (7)$$

where

- V_{OUT} is the maximum programmed output voltage
- 50 µs is based on internal ramp setup
- V_{IN} is the minimum input voltage
- f_{SW} is the typical switching frequency
- L is the chosen inductance

The maximum valuable between 式 6 and 式 7 must be selected. 表 7-1 lists some known inductor-capacitor combinations.

表 7-1. Known LC Combinations

$I_{TRAN(max)}$ (A)	L (µH)	V_{OUT} (V)	V_{UNDER} (V)	C_{OUT}(µF)
3.5	0.47	1	0.05	110
4	0.47	1	0.05	220
5	0.47	1.35	0.068	220
8	0.33	1	0.06	440
20	0.22	1	0.16	550

7.2.2.1.4 Selecting the FETs

This controller is designed to drive two NMOS FETs. Typically, lower R_{DSON} values are better for improving the overall efficiency of the controller; however, higher gate-charge thresholds result in lower efficiency so the twovalues must be balanced for optimal performance. As the R_{DSON} for the low-side FET decreases, the minimum current limit increases; therefore, appropriately select the values for the FETs, inductor, output capacitors, and current limit resistor. TI's CSD87331Q3D, CSD87381P, and CSD87588N devices are recommended for the controllers, depending on the required maximum current.

7.2.2.1.5 Bootstrap Capacitor

To ensure the internal high-side gate drivers are supplied with a stable low-noise supply voltage, a capacitor must be connected between the SWx pins and the respective BOOTx pins. TI recommends placing ceramic capacitors with a value of 0.1 µF for the controllers. During testing, a 0.1-µF, size 0402, 10-V capacitor is used for the controllers.

TI recommends reserving a small resistor in series with the bootstrap capacitor in case the turnon and turnoff of the FETs must be slowed to reduce voltage ringing on the switch node, which is a common practice for controller design.

7.2.2.1.6 Setting the Current Limit

The current-limiting resistor value must be chosen based on 式 1.

7.2.2.1.7 Selecting the Input Capacitors

Because of the nature of the switching controller with a pulsating input current, a low-ESR input capacitor is required for best input-voltage filtering and also for minimizing the interference with other circuits caused by high input-voltage spikes. For the controller, a typical 2.2-µF capacitor can be used for the DRV5V_x_x pin to support the transients on the driver. For the FET input, 10 µF of input capacitance (after derating) is recommended for most applications. To achieve the low-ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. For better input-voltage filtering, the input capacitor can be increased without any limit.

注

Use the correct capacitance value for the ceramic capacitor after derating to achieve the recommended input capacitance.

TI recommends placing a ceramic capacitor as close as possible to the FET across the respective VSYS and PGND pins of the FETs. The preferred capacitors for the controllers are two Murata GRM21BR61E226ME44: 22-µF, 0805, 25-V, ±20%, or similar capacitors.

7.2.2.2 Converter Design Procedure

Designing the converter has only two steps: design the output filter and select the input capacitors.

The converter must be supplied by a 5V source. 図 7-5 shows a diagram of the converter.

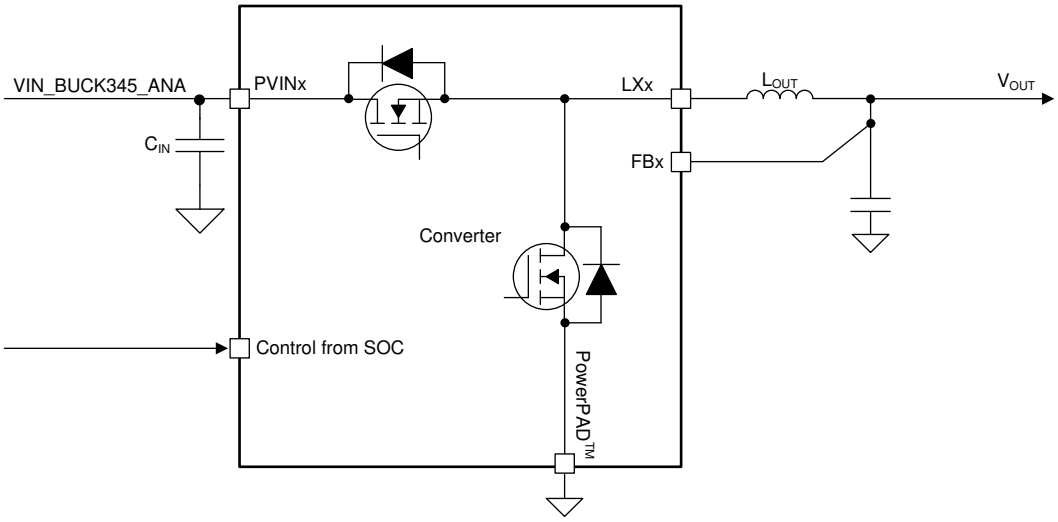

図 7-5. Converter Diagram

7.2.2.2.1 Selecting the Inductor

Placement of an inductor between the external FETs and the output capacitors is required. Together, the inductor and output capacitors form a double pole in the control loop that contributes to stability. Additionally, the inductor is directly responsible for the output ripple, efficiency, and transient performance. As the inductance used increases, the ripple current decreases, which typically results in an increase in efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DCR.

注

Internal parameters for the converters are optimized for a 0.47-µH inductor for BUCK3 and a 1-µH inductor for BUCK4 and BUCK5; however, using other inductor values is possible as long as they are chosen carefully and thoroughly tested.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{sw} \times I_{OUT(MAX)} \times K_{IND}} \quad (8)$$

With the chosen inductance value and the peak current for the inductor in steady state operation, $I_{L(MAX)}$ can be calculated using 式 9. The rated saturation current of the inductor must be higher than the $I_{L(MAX)}$ current.

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{sw} \times L} \quad (9)$$

7.2.2.2.2 Selecting the Output Capacitors

Ceramic capacitors with low ESR values are recommended because they provide the lowest output voltage ripple. The output capacitor requires either an X7R or X5R rating. Y5V and Z5U capacitors, aside from the wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operates in PFM mode and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve the specified regulation performance and low output-voltage ripple, the DC-bias

characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC-bias voltage.

For the output capacitors of the buck converters, TI recommends placing small ceramic capacitors between the inductor and load with many vias to the PGND plane. This solution typically provides the smallest and lowest-cost solution available for D-CAP2 controllers.

The output capacitance must equal or exceed the minimum capacitance listed for BUCK3, BUCK4, and BUCK5 (assuming quality layout techniques are followed).

7.2.2.2.3 Selecting the Input Capacitors

Because of the nature of the switching converter with a pulsating input current, a low-ESR input capacitor is required for the best input-voltage filtering and for minimizing the interference with other circuits caused by high input-voltage spikes. For the PVINx pin, 2.5 µF of input capacitance (after derating) is required for most applications. A ceramic capacitor is recommended to achieve the low-ESR requirement. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. The input capacitor can be increased without any limit for better input-voltage filtering.

注

Use the correct capacitance value for the ceramic capacitor after derating to achieve the recommended input capacitance.

The preferred capacitor for the converters is one Samsung CL05A106MP5NUNC: 10-µF, 0402, 10-V, ±20%, or similar capacitor.

7.2.2.3 LDO Design Procedure

The VTT LDO must support the fast load transients from the DDR memory for termination. Therefore, TI recommends using ceramic capacitors to maintain a high amount of capacitance with low ESR on the VTT LDO outputs and inputs. The preferred output capacitors for the VTT LDO are the GRM188R60J226MEA0 from Murata (22 µF, 0603, 6.3 V, ±20%, or similar capacitors). The preferred input capacitor for the VTT LDO is the CL05A106MP5NUNC from Samsung (10-µF, 0402, 10-V, ±20%, or similar capacitor).

The remaining LDOs must have input and output capacitors chosen based on the values in セクション 5.9.

7.2.3 Application Curves

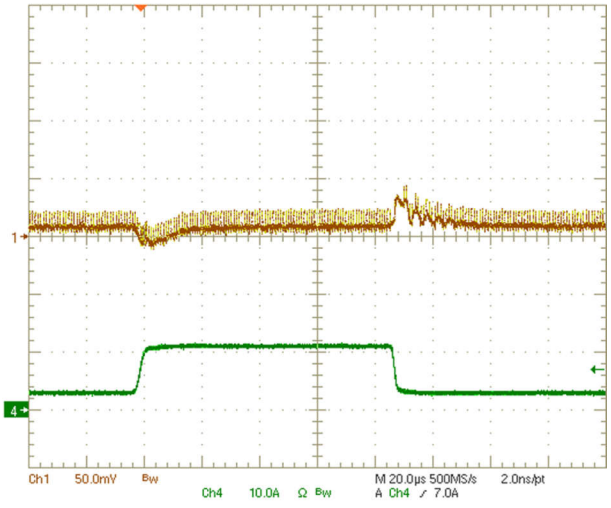

図 7-6. BUCK2 Load Transient

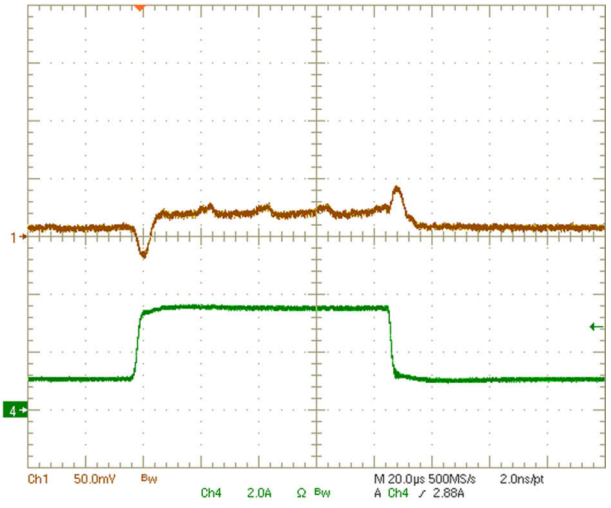

図 7-7. BUCK2 Load Transient

7.2.4 Layout

7.2.4.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can have stability problems and EMI issues. Therefore, use wide and short traces for the main current path and for the power ground (PGND) tracks. The input capacitors, output capacitors, and inductors must be placed as close as possible to the device. Use a common-ground node for the power ground and use a different, isolated node for the control ground to minimize the effects of ground noise. Connect these ground nodes close to the AGND pin by one or two vias. Use of the design guide is highly recommended in addition to following these other basic requirements:

- Do not allow the AGND, PGNDSNSx, or FBGND2 pin to connect to the thermal pad on the top layer.
- To ensure proper sensing based on the FET R_{DSON}, the PGNDSNSx pin must not connect to the board ground or to the PGND pin of the FET.
- All inductors, input and output capacitors, and FETs for the converters and controller must be on the same board layer as the device.
- To achieve the best regulation performance, place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible.
- Bootstrap capacitors must be placed close to the device.
- The internal reference regulators must have their input and output capacitors placed close to the device pins.
- Route the DRVHx and SWx pins as a differential pair. Ensure that a power-ground path is routed in parallel with the DRVLx pin, which provides optimal driver loops.

7.2.4.2 Layout Example

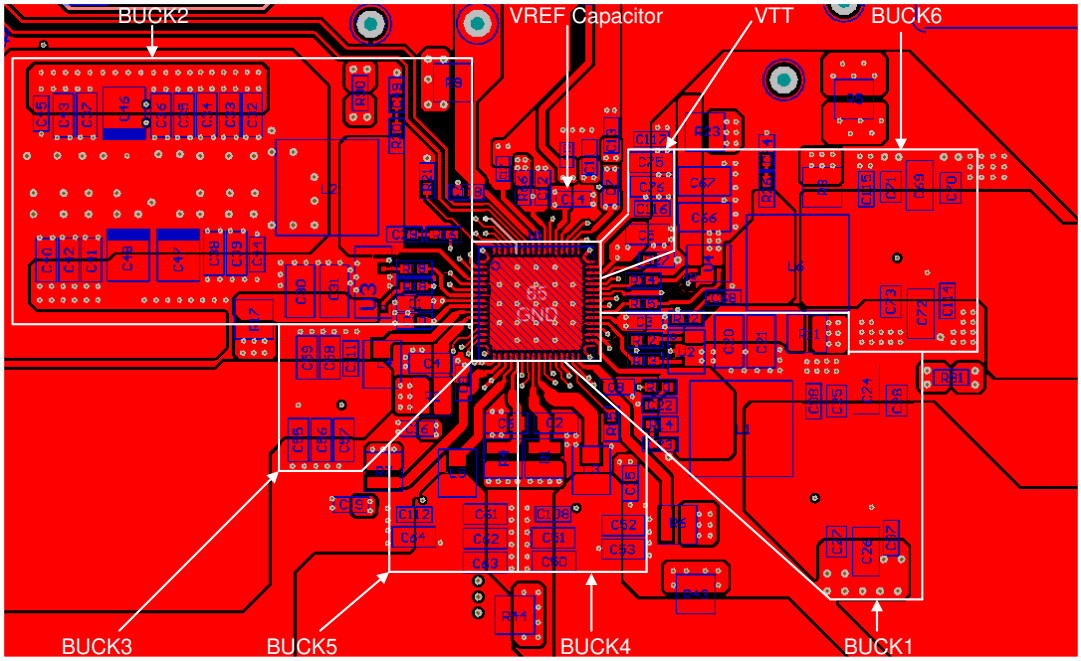

図 7-8. EVM Layout Example With All Components on the Top Layer

7.3 Power Supply Coupling and Bulk Capacitors

This device is designed to work with several different input voltages. The minimum voltage on the VSYS pin is 5.6 V for the device to start up; however, this is a low power rail. The input to the FETs must be from 4.5 V to 21 V as long as the proper bill of materials (BOM) choices are made. The input to the converters must be 5 V. For the device to output maximum power, the input power must be sufficient. For the controllers, V_{IN} must be able to supply sufficient input current for the output power of the application. For the converters, the PVINx converter must be able to supply 2 A (typical).

As a best practice, determine the power usage by the system and back-calculate the necessary power input based on the expected efficiency values.

7.4 Dos and Don'ts

- Connect the LDO5V output to the DRV5V_x_x inputs. This output initially supplies 5 V for the drivers from the VSYS pin and then switches to using the 5-V buck converter when available for optimal efficiency.
- Ensure that none of the control pins are potentially floating.
- Include 0-Ω resistors on the DRVH or BOOT pins of the controllers on prototype boards, which allows for slowing the controllers if the system is unable to handle the noise generated by the large switching or if switching voltage is too large because of layout.
- Do not connect the V5ANA power input to a different source other than PVINx. A mismatch here causes reference circuits to regulate incorrectly.
- Do not supply the V5ANA power input before the VSYS. Reference biasing of the internal FETs may turn on the HS FET passing the input to the output until VSYS is biased.

8 Device and Documentation Support

8.1 Device Support

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *CSD87331Q3D Synchronous Buck NexFET™ Power Block* data sheet
- Texas Instruments, *CSD87381P Synchronous Buck NexFET™ Power Block II* data sheet
- Texas Instruments, *CSD87588N Synchronous Buck NexFET™ Power Block II* data sheet

8.3 ドキュメントの更新通知を受け取る方法

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8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2017) to Revision A (February 2025)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Added note for switch control and bit enable to the *Power-Up and Power-Down Sequence* figure	28
• Changed the reset value for the SWBx_DIS and SWA1_DIS bits in the SWVTT_DIS: SWVTT Disable Register (offset = 9Fh)	58
• Changed the reset value for the SWA1_FLTMSK bit in the PWR_FAULT_MASK1: VR Power Fault Mask1 Register (offset = A2h)	61
• Changed order of bits in "MISCSYSPG" Register (offset = ACh)	71

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS6508700RSKR	Active	Production	VQFN (RSK) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T6508700 PG1.0
TPS6508700RSKR.A	Active	Production	VQFN (RSK) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T6508700 PG1.0
TPS6508700RSKT	Active	Production	VQFN (RSK) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T6508700 PG1.0
TPS6508700RSKT.A	Active	Production	VQFN (RSK) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T6508700 PG1.0

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

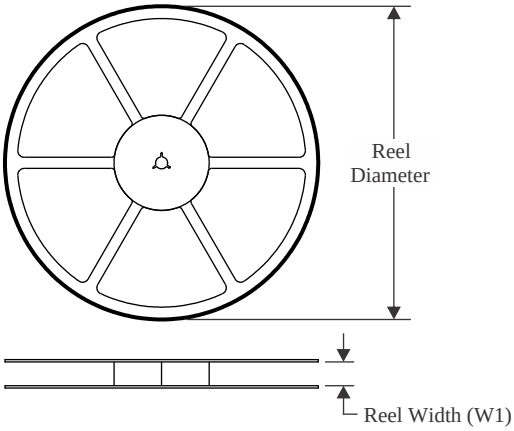
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

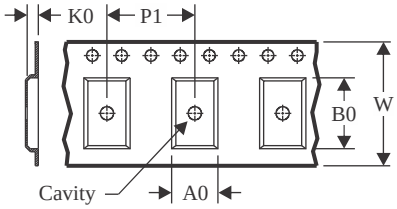
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

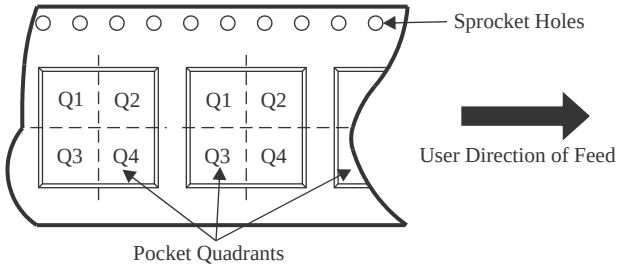


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

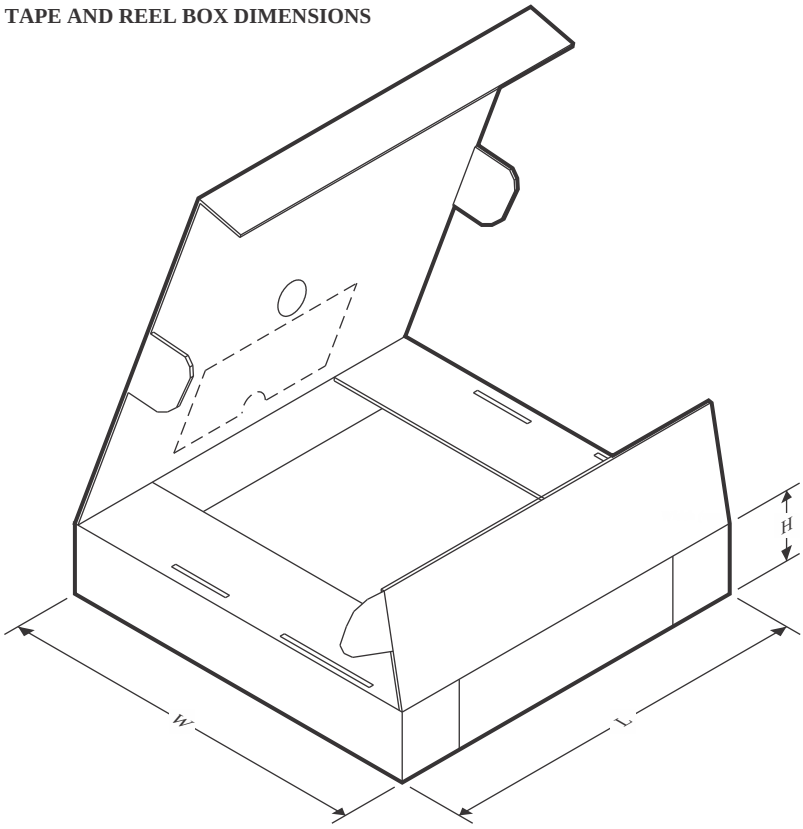
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6508700RSKR	VQFN	RSK	64	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS6508700RSKT	VQFN	RSK	64	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6508700RSKR	VQFN	RSK	64	2000	367.0	367.0	38.0
TPS6508700RSKT	VQFN	RSK	64	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

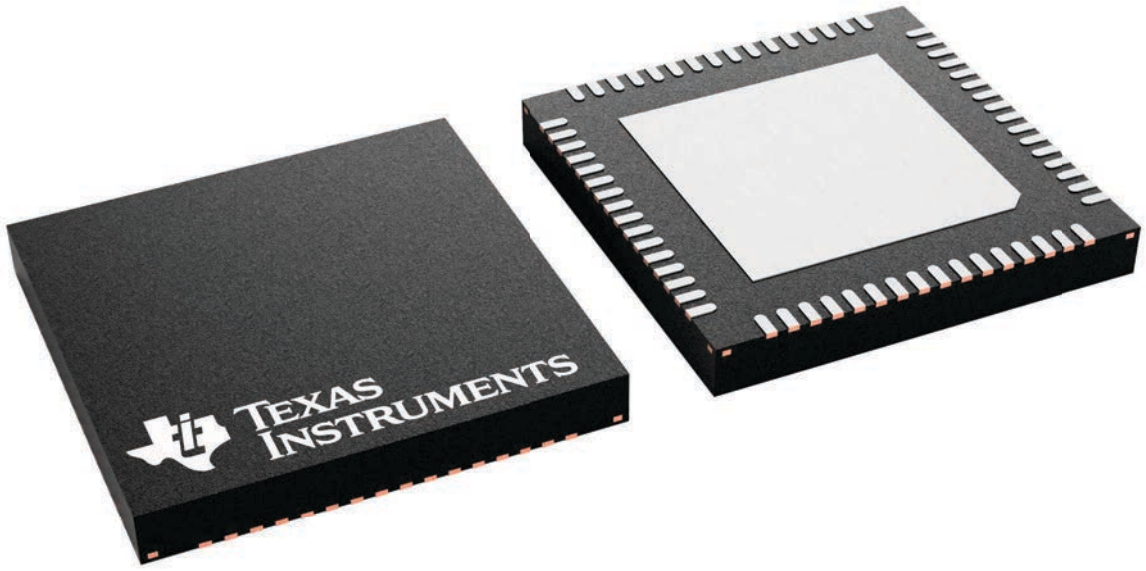
RSK 64

VQFN - 1 mm max height

8 x 8, 0.4 mm pitch

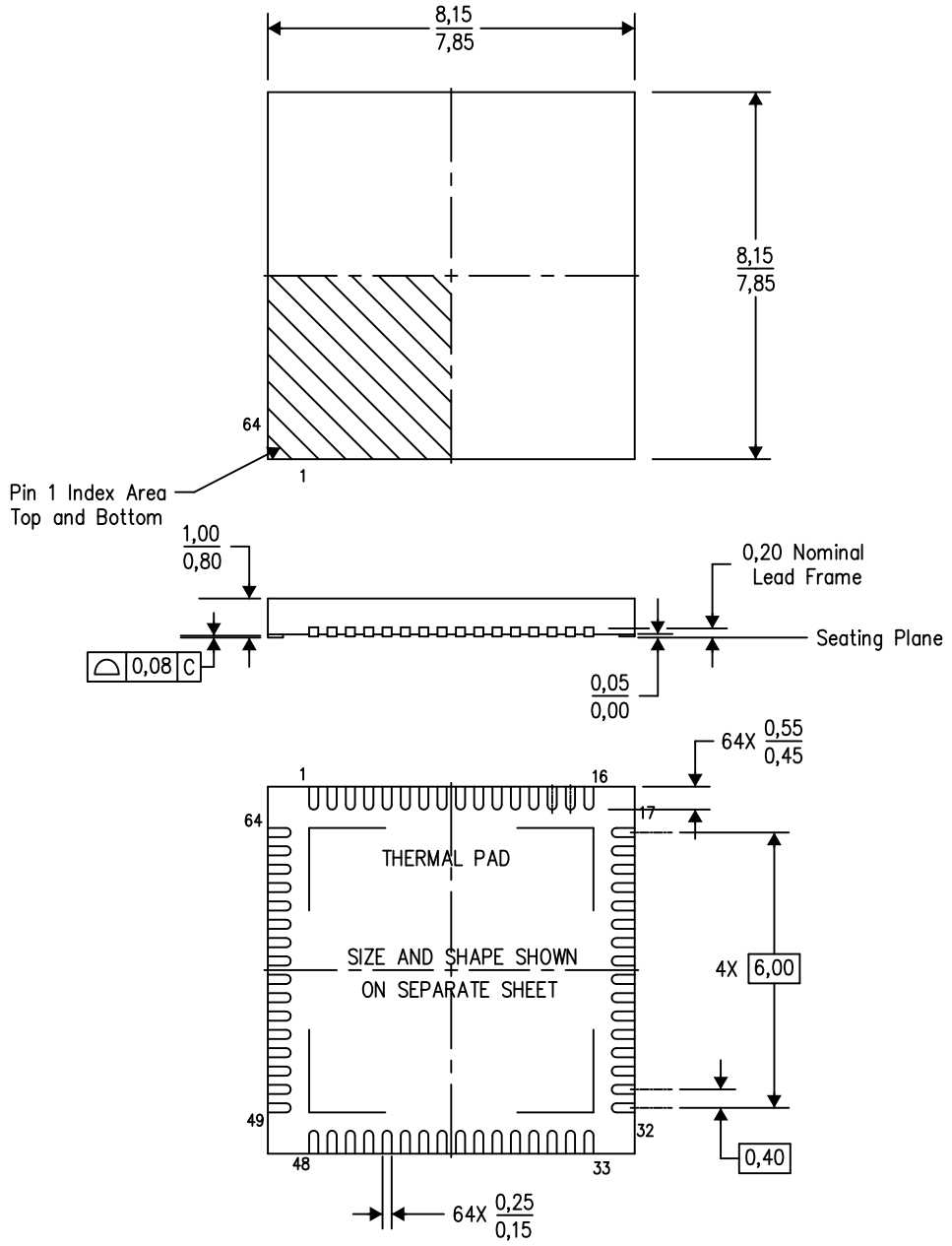
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231455/A

RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4207547/C 04/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

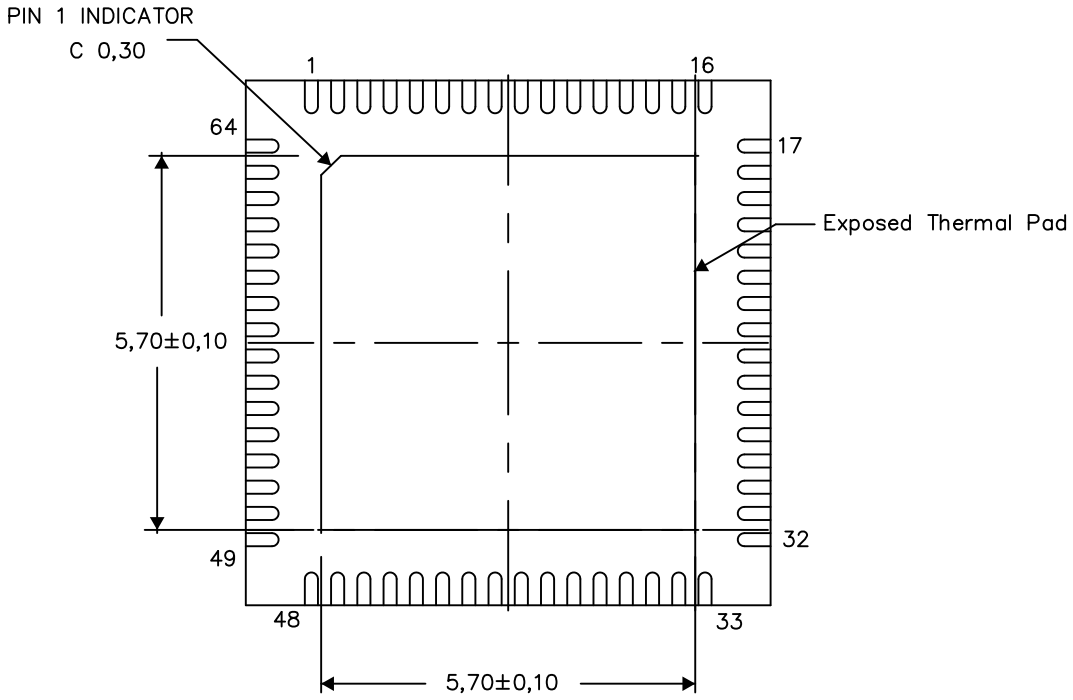
RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



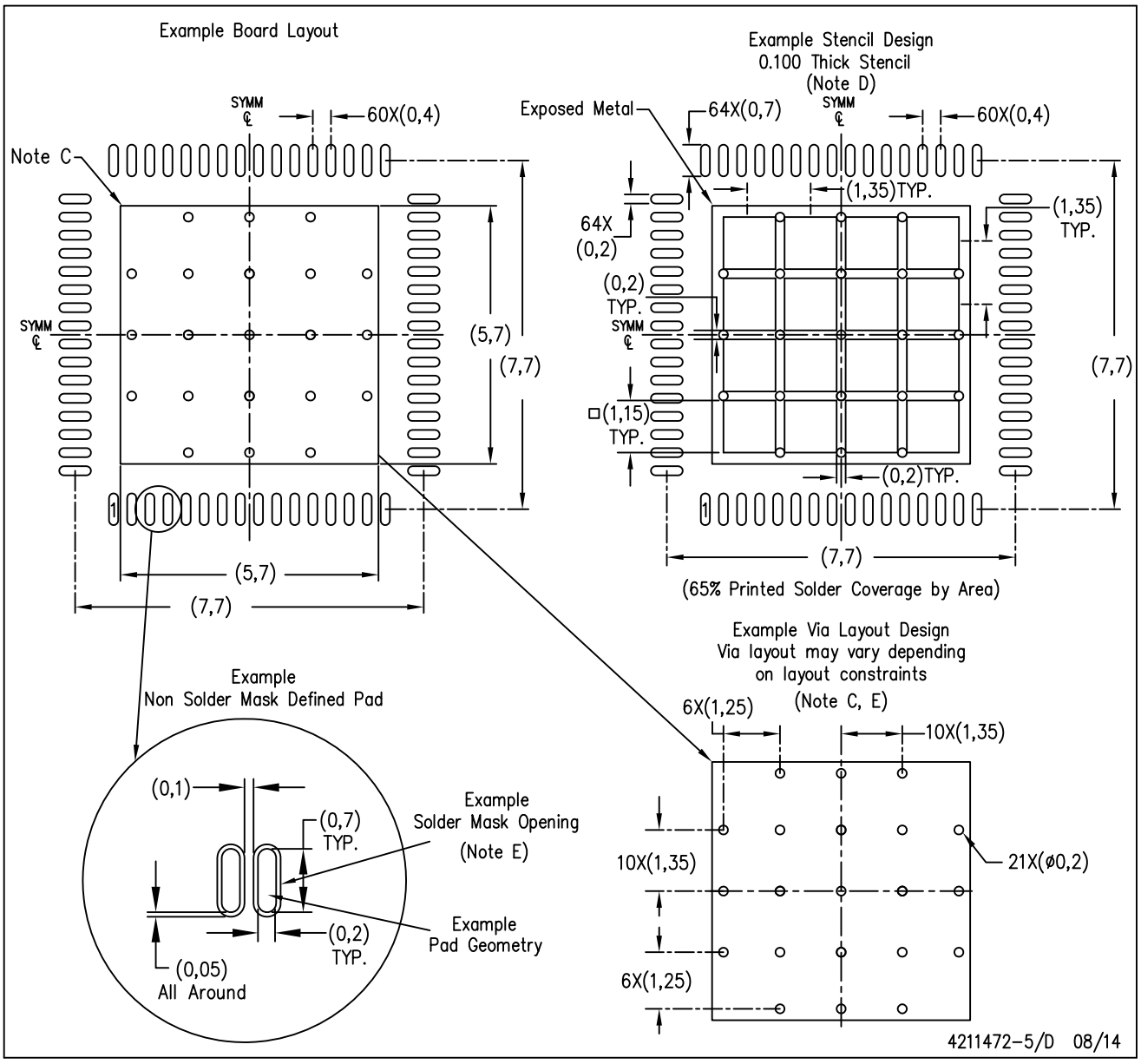
Bottom View

Exposed Thermal Pad Dimensions

4208001–5/H 08/14

NOTE: A. All linear dimensions are in millimeters

RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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最終更新日：2025 年 10 月