TPS63810 および TPS63811 - I²C インターフェイス付き 2.5A 昇降圧コンバータ

1 特長

- 入力電圧範囲：2.2V～5.5V
- 出力電圧範囲: 1.8V～5.2V
  - 動作中およびシャットダウン中に I²C で設定可能
  - VSEL ピンで 2 つのプリセット出力電圧を切り替え可能
- 出力電流
  - V_I ≥ 2.5V、V_O = 3.3V で最大 2.5A
  - V_I ≥ 2.8V、V_O = 3.5V で最大 2.5A
- 全負荷範囲にわたって高効率を実現
  - 低い動作時静止電流:13µA
  - 自動パワーセーブ・モードと強制 PWM モード (I²C で設定可能)
- ピーク電流モード昇降圧アーキテクチャ
  - 降圧、昇降圧、昇圧動作間の遷移を定義済み
  - 順方向および逆方向電流動作
  - あらかじめ出力にバイアスを印加した状態で起動
- 安全で堅牢な動作を実現する機能
  - ソフトスタート内蔵
  - 過熱保護および過電圧保護
  - シャットダウン時に負荷を完全に切断
  - 順方向および逆方向の電流制限
- 2 つのデバイス・オプション
  - TPS63810:出力電圧を事前設定済み (3.3V、3.45V)
  - TPS63811:起動前に出力電圧を設定
- 20mm² 未満のソリューション・サイズ、わずか 4 つの外付け部品

2 アプリケーション

- システム・プリレギュレータ (スマートフォン、タブレット、トラッキング / テレマティクス、EPOS、TWS イヤホン、医療用補聴器)
- ポイント・オブ・ロード・レギュレーション (TOF カメラ・センサ、ポート / ケーブル・アダプタおよびドングル)
- 熱電デバイスの電源 (TEC、光モジュール)
- ブロードバンド・ネットワーク無線または SoC 電源 (IoT、ホーム・オートメーション、EPOS)

3 概要

TPS63810 および TPS63811 は、I²C を介して完全にプログラム可能な高効率、大出力電流の昇降圧コンバータです。入力電圧に応じて自動的に昇圧モード、降圧モード、革新的な 4 サイクル昇降圧モード (入力電圧が出力電圧とほぼ等しい場合) で動作します。

モード間の遷移は定義されたスレッショルドで行い、出力電圧リップルを減らすためモード間の不要なトグルは行いません。

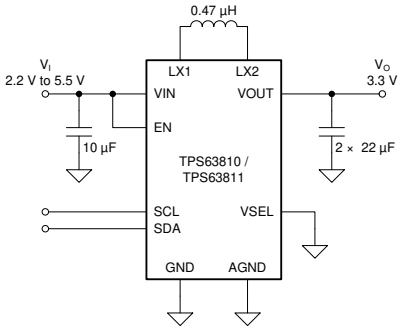
I²C を介して 2 つのレジスタで出力電圧を設定し、アクティブにする出力電圧レジスタを VSEL ピンで選択します。これにより、動的な電圧スケーリングをサポートできます。動作中に出力電圧レジスタを変更する (VSEL ピンを切り替える) と、定義されたプログラム可能なランプ・レートで遷移します。

製品情報(1)

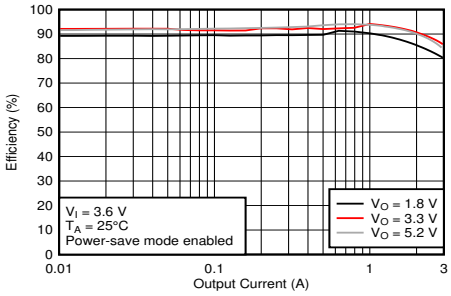
型番	パッケージ	本体サイズ(公称)
TPS63810	DSBGA (15)	2.3mm × 1.4mm
TPS63811		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



効率と出力電流との関係



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 デバイス比較表 ... 2
6 **Pin Configuration and Functions** ... 3
7 **Specifications** ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 5
7.5 Electrical Characteristics ... 5
7.6 Timing Requirements ... 6
7.7 Switching Characteristics ... 7
7.8 Typical Characteristics ... 7
8 **Detailed Description** ... 8
8.1 Overview ... 8
8.2 Functional Block Diagram ... 8
8.3 Feature Description ... 8
8.4 Device Functional Modes ... 17
8.5 Programming ... 17
8.6 Register Map ... 21
9 **Application and Implementation** ... 25
9.1 Application Information ... 25
9.2 Typical Applications ... 25
10 **Power Supply Recommendations** ... 34
11 **Layout** ... 34
11.1 Layout Guidelines ... 34
11.2 Layout Example ... 34
12 デバイスおよびドキュメントのサポート ... 35
12.1 デバイス・サポート ... 35
12.2 ドキュメントのサポート ... 35
12.3 関連リンク ... 35
12.4 ドキュメントの更新通知を受け取る方法 ... 35
12.5 サポート・リソース ... 35
12.6 商標 ... 35
12.7 用語集 ... 35
13 メカニカル、パッケージ、および注文情報 ... 36

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (November 2019) から Revision C に変更 **Page**

- Changed the unit in 図 2 ... 7
- Changed "Output Disabled (Hi-Z)" to "Output Discharge Active" in 表 2 ... 13
- Changed "EN pin is low" to "EN pin is low or the ENABLE bit is set to zero" in the *Output Discharge* section ... 17
- Changed "TPS63810" to "Start-up value for TPS63810" in bit 5 of Table 3 ... 22

Revision A (October 2019) から Revision B に変更 **Page**

- 製品ステータスを事前情報から量産データに変更 ... 1

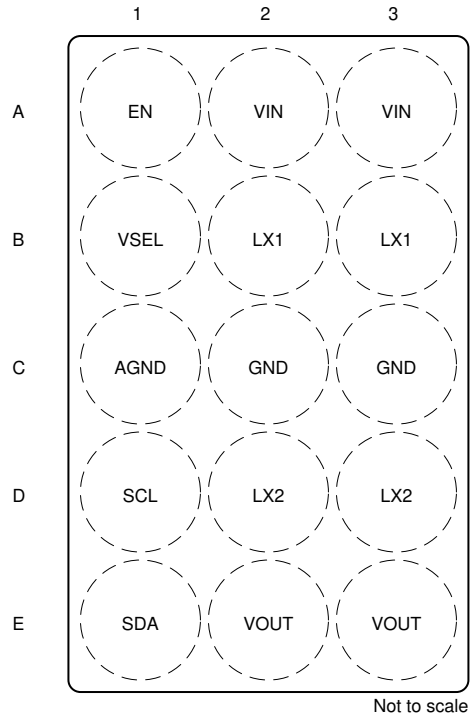
5 デバイス比較表

型番	起動時の出力の状態	出力電圧
TPS63810	イネーブル	VSEL = Low: 3.3V VSEL = High: 3.45V
TPS63811	ディセーブル	起動時に設定可能

Copyright © 2019–2020, Texas Instruments Incorporated

6 Pin Configuration and Functions

YFF Package
15-Ball DSBGA
Top View



BGA Package (YFF) Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	EN	I	Device enable. A high logic level on this pin enables the device; a low logic level on this pin disables the device.
A2	VIN	—	Supply voltage for power stage
A3	VIN	—	Supply voltage for power stage
B1	VSEL	I	This pin selects which VOUT register is active. When a low logic level is applied to this pin, the VOUT1 register sets the output voltage. When a high logic level is applied to this pin, the VOUT2 register sets the output voltage.
B2	LX1	—	Inductor connection
B3	LX1	—	Inductor connection
C1	AGND	—	Analog ground
C2	GND	—	Power ground
C3	GND	—	Power ground
D1	SCL	I/O	I^2C serial interface clock. Pull this pin up to the I^2C bus voltage with a resistor or a current source.
D2	LX2	—	Inductor connection
D3	LX2	—	Inductor connection
E1	SDA	I/O	I^2C serial interface data. Pull this pin up to the I^2C bus voltage with a resistor or a current source.
E2	VOUT	—	Converter output
E3	VOUT	—	Converter output

Copyright © 2019–2020, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_I	Input voltage (VIN, LX1, LX2, VOUT, SCL, SDA, EN, VSEL)[2]	–0.3	6	V
	Input voltage for less than 10 ns (LX1, LX2)[2]	–3	9	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		2.2		5.5	V
V_O	Output voltage	Low range	1.8		4.975	V
		High range	2.025		5.2	
V_{IH}	High-level input voltage	SCL, SDA, VSEL	1.3		V_I	V
V_{IL}	Low-level input voltage	SCL, SDA, VSEL	0		0.3	V
$V_{(EN)}$	Input voltage	EN	0		V_I	V
I_O	Output current[1]	V_O = 3.3 V, V_I ≥ 2.5 V			2.5	A
		V_O = 3.5 V, V_I ≥ 2.5 V			2	
		V_O = 3.5 V, V_I ≥ 2.8 V			2.5	
		V_O = 3.3 V, V_I ≥ 3 V			3	
C_I	Input capacitance[2]		5			µF
C_O	Output capacitance[2]		13	16		µF
L	Inductance		390	470	560	nH
T_A	Operating free-air temperature range		–40		85	°C
T_J	Operating junction temperature range		–40		125	°C

(1) The device can sustain the maximum recommended output current only for short durations before its junction temperature gets too hot. Users must verify that the thermal performance of the end application can support the maximum output current.
(2) Effective capacitance after DC bias effects have been considered.

Copyright © 2019–2020, Texas Instruments Incorporated

7.4 Thermal Information

THERMAL METRIC[1]		TPS63810, TPS63811 YFF (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 3.3 V and T_J = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
$I_{Q;VIN}$	Supply current into VIN		V_I = 3.6 V, V_O = 3.3 V, $V_{(EN)}$ = 3.6 V, not switching, T_J = 25°C		13		µA
	Supply current into VIN		V_I = 3.6 V, V_O = 0 V, $V_{(EN)}$ = 3.6 V, Output disabled with ENABLE bit in Control Register T_J = 25°C		15		µA
I_{SD}	Shutdown current into VIN		V_I = 3.6 V, V_O = 0 V, $V_{(EN)}$ = 0 V T_J = 25°C		0.35		µA
V_{IT+}	Positive-going UVLO threshold voltage			2	2.1	2.2	V
V_{hys}	UVLO threshold voltage hysteresis				200		mV
I/O SIGNALS							
V_{IT+}	Positive-going input threshold voltage	SCL, SDA, VSEL				1.2	V
		EN		1.07	1.1	1.13	
V_{IT-}	Negative-going input threshold voltage	SCL, SDA, VSEL		0.4			V
		EN		0.97	1	1.03	
V_{hys}	Hysteresis voltage	EN		40			mV
I_{IH}	High-level input current	SCL, SDA, VSEL	$V_{(SCL)}$ = $V_{(SDA)}$ = $V_{(VSEL)}$ = 1.8 V, no pullup resistor		±0.01	±0.1	µA
I_{IL}	Low-level input current	SCL, SDA, VSEL	$V_{(SCL)}$ = $V_{(SDA)}$ = $V_{(VSEL)}$ = 0 V, no pullup resistor		±0.01	±0.1	µA
I_{OL}	Low-level output current	SCL, SDA	V_{OL} = 0.4 V	20			mA
I_{IB}	Input bias current	EN	$V_{(EN)}$ = 0 V to 5.5 V		±0.01	±0.1	µA
POWER STAGE							
V_O	Output voltage range		Low range	1.8		4.975	V
			High range	2.025		5.2	
	Output voltage accuracy		PWM operation	–1.5		1.5	%
			PSM operation	–1.5		3.5	
	Default output voltage (RANGE = 0)		VSEL = low		3.3		V
			VSEL = high		3.45		
	Switch current limit		V_I = 2.9 V, V_O = 3.6 V, boost operation, output sourcing current	5.2		6.5	A
			V_I = 4.1 V, V_O = 3.3 V, buck operation, output sourcing current	3.8	4.3	5.2	
			V_I = 5 V, V_O = 3.3 V, reverse-boost operation, output sinking current	–1.3		–0.35	
$I_{T-(PSM)}$	PSM entry threshold (peak) current		V_I = 4.2 V; V_O = 3.3 V		0.85		A

Copyright © 2019–2020, Texas Instruments Incorporated

Electrical Characteristics (continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 3.3 V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output discharge current	V_I = 3.6 V, V_O ≥ 0.8 V	50			mA
$V_{T+(PG)}$	Positive-going power-good threshold voltage			95		%
$V_{T-(PG)}$	Negative-going power-good threshold voltage			90		%
	Positive-going input overvoltage threshold	Reverse current operation		5.7		V
I²C INTERFACE						
	7-Bit slave address			75h		
THERMAL SHUTDOWN						
	Thermal shutdown threshold temperature	T_J rising		150		°C
	Thermal shutdown hysteresis			20		°C

7.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus	0		1000	
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD;STA}$	Hold time (repeated) START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{SU;DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
$t_{HD;DAT}$	Data hold time	Standard mode	0			µs
		Fast mode	0			
		Fast mode plus	0			
t_r	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
t_f	Fall time of both SDA and SCL signals	Standard mode			300	ns
		Fast mode	$20 \times V_{DD}/5.5$		300	
		Fast mode plus	$20 \times V_{DD}/5.5$		120	
$t_{su;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			

Copyright © 2019–2020, Texas Instruments Incorporated

Timing Requirements (continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

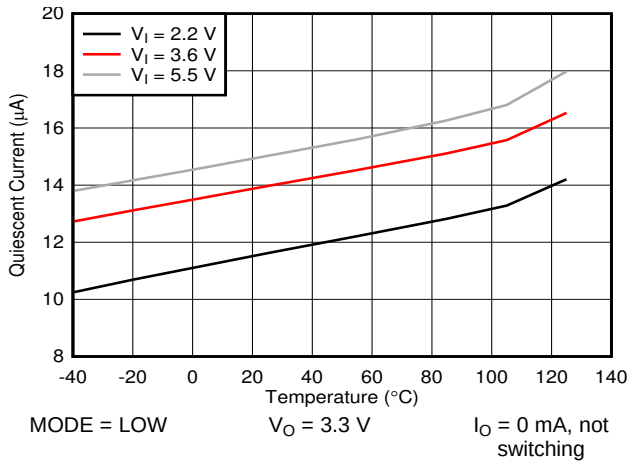
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VD;DAT}$	Data valid time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus			0.45	
$t_{VD;ACK}$	Data valid acknowledge time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus			0.45	
C_b	Capacitive load for each bus line	Standard mode			400	
		Fast mode			400	
		Fast mode plus			550	
$t_{w(VSEL)}$	VSEL pulse duration	VSEL = high or low	5			µs

7.7 Switching Characteristics

Over operating junction temperature range and recommended input voltage range (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 3.3 V, and T_J = 25°C (unless otherwise noted).

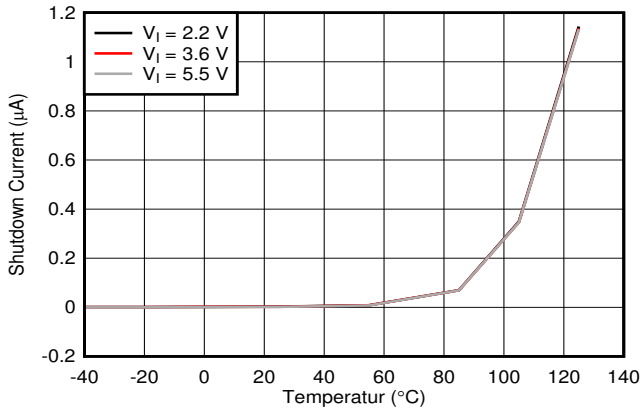
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of the output voltage ramp	T_J = 25°C, V_I = 3.6 V		229	440	µs
$t_{d(PG)}$	Power-good delay	V_O falling		50		µs
SR	Slew rate of internal ramp during dynamic voltage scaling	SLEW = 00b, forced-PWM operation		±1		V/ms
		SLEW = 01b, forced-PWM operation		±2.5		
		SLEW = 10b, forced-PWM operation		±5		
		SLEW = 11b, forced-PWM operation		±10		
f_{SW}	Inductor Switching Frequency, Boost Mode	V_I = 2.3 V, V_O = 3.3 V, no Load, PWM operation		2.6		MHz
	Inductor Switching Frequency, Buck-Boost Mode	V_I = 3.3 V, V_O = 3.3 V, no Load, PWM operation		1.6		MHz
	Inductor Switching Frequency, Buck Mode	V_I = 4.3 V, V_O = 3.3 V, no Load, PWM operation		2.0		MHz
$t_{d(VSEL)}$	Delay between rising edge of VSEL and start of DVS ramp	Measured from rising edge of VSEL to start of ramp.			5	µs

7.8 Typical Characteristics



MODE = LOW V_O = 3.3 V I_O = 0 mA, not switching

図 1. Quiescent Current versus Temperature



EN = LOW

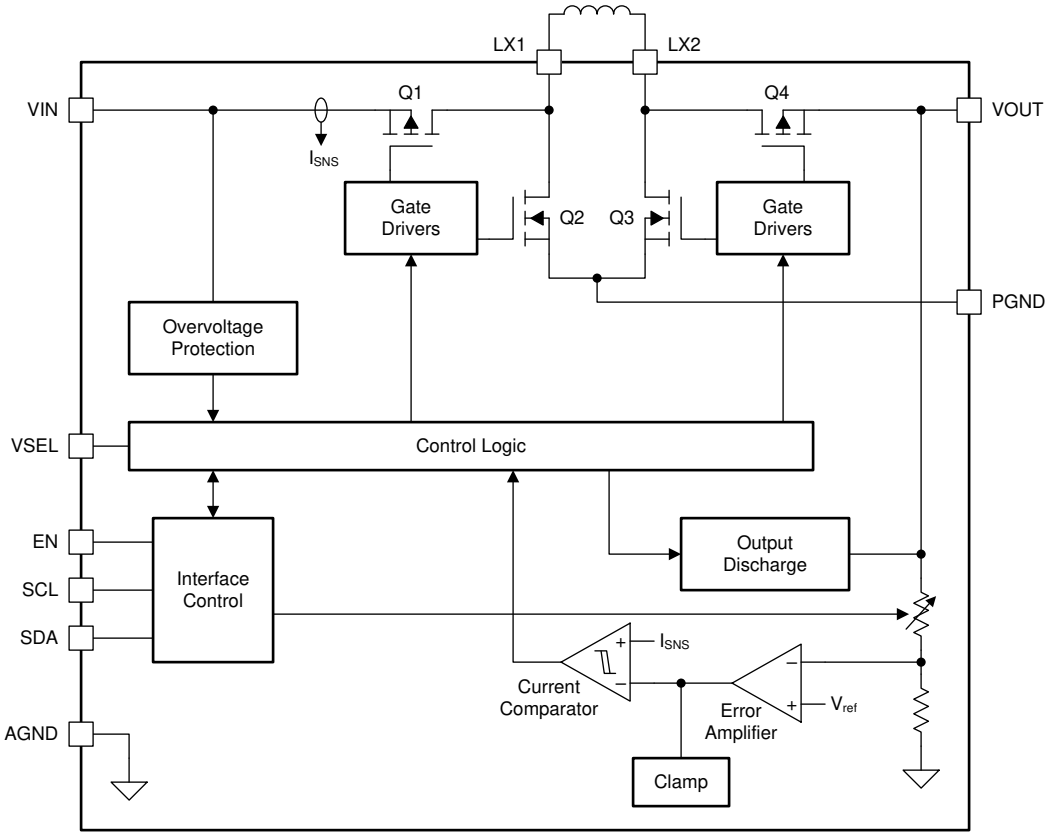
図 2. Shutdown Current versus Temperature

8 Detailed Description

8.1 Overview

The TPS63810 and TPS63811 devices are high-efficiency buck-boost converters. Each device uses four switches to maintain synchronous power conversion under all operating conditions, so that the device achieves high efficiency power conversion over a wide range of input voltages and output currents. The device automatically switches between buck, boost, and buck-boost operation as required by the operating conditions. The device operates as a true buck converter when $V_I > V_O$ and as a true boost converter when $V_I < V_O$. When $V_I \approx V_O$, the device operates in a 4-cycle buck-boost mode. The RMS current through the switches and the inductor is thus kept to a minimum, minimizing switching and conduction losses. Controlling the switches this way lets the converter achieve high efficiency over the whole input voltage range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Control Scheme

The device automatically selects the best switching scheme for the operating conditions. To make sure of stable operation, the selection logic includes hysteresis (see 図 3).

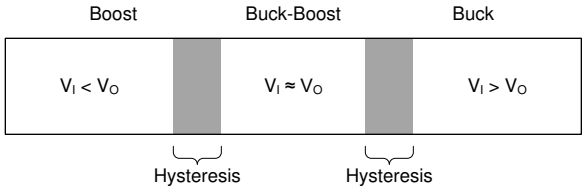


図 3. Switching Scheme Selection

Copyright © 2019–2020, Texas Instruments Incorporated

Feature Description (continued)

8.3.1.1 Buck Operation

When $V_I > V_O$, the device switches like a buck converter:

- Q1 is the switch.
- Q2 is the rectifier.
- Q3 is permanently off.
- Q4 is permanently on.

See 図 4. During buck operation, one switching cycle comprises two phases: on–off.

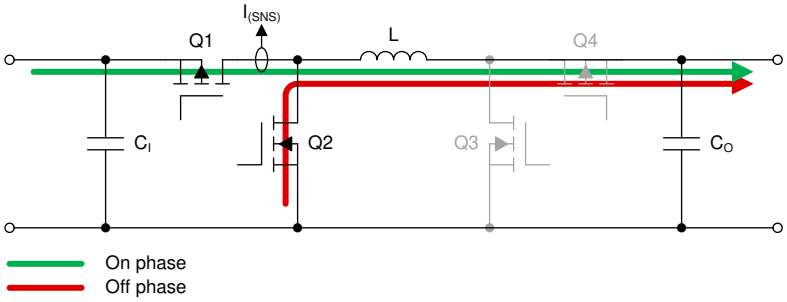


図 4. Buck Switch Configuration

8.3.1.2 Boost Operation

When $V_I < V_O$, the device switches like a boost converter:

- Q1 is permanently on.
- Q2 is permanently off.
- Q3 is the switch.
- Q4 is the rectifier.

See 図 5. During boost operation, one switching cycle comprises two phases: on–off.

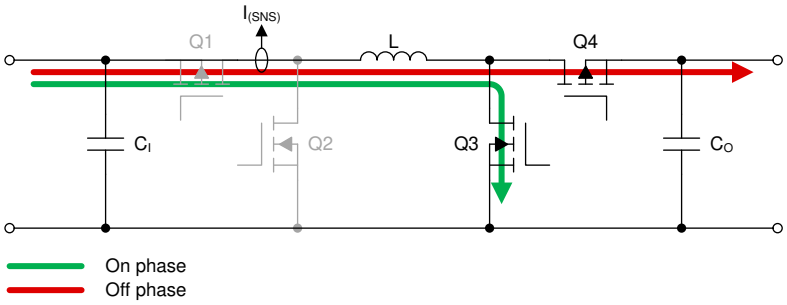


図 5. Boost Switch Configuration

8.3.1.3 Buck-Boost Operation

When $V_I \approx V_O$, all four transistors switch continuously (see 図 6). During buck-boost operation, one switching cycle comprises four phases: on–commutate–off–commutate.

Feature Description (continued)

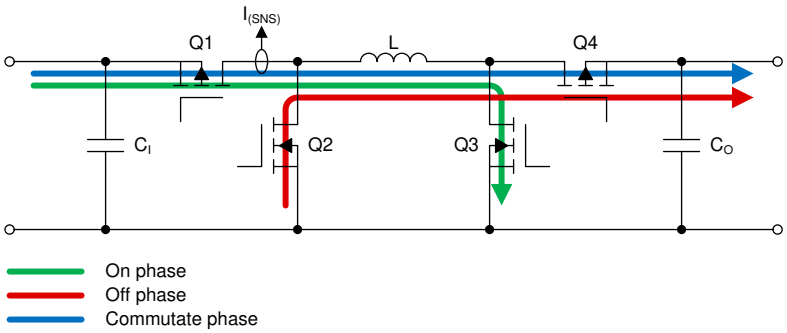


図 6. Buck-Boost Switch Configuration

8.3.2 Control Scheme

The device uses a constant off-time, peak-current-mode control scheme where an outer voltage control loop generates the demand signal for an inner current control loop. During the on-time, the inner current control loop monitors the inductor current, and when the inductor current equals the demand signal from the error amplifier, the on-time stops and the next part of the switching cycle starts.

The off-time is a function of V_I and V_O and the operating mode (buck, boost, or buck-boost) of the converter.

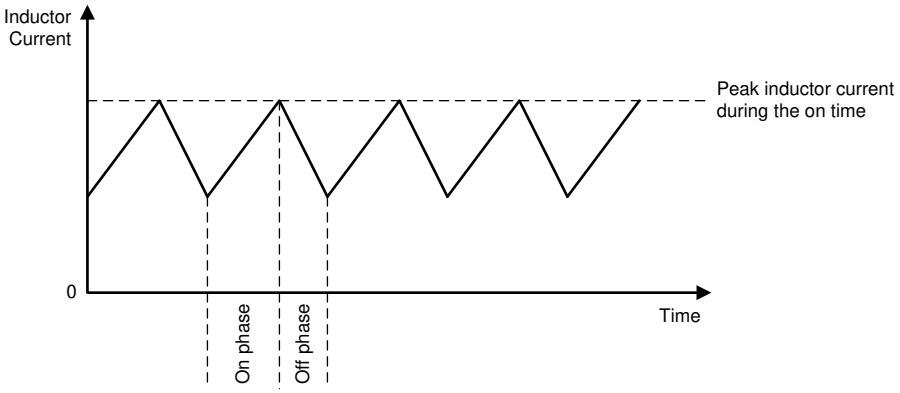


図 7. Peak Current Control (Buck and Boost Operation)

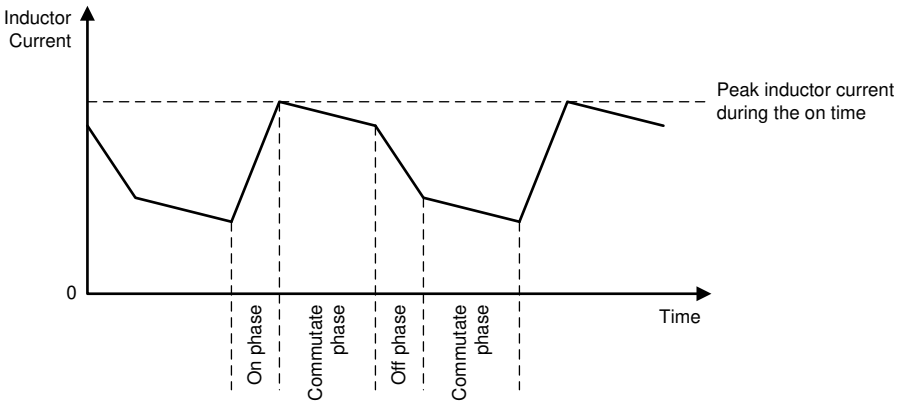


図 8. Peak Current Control – Buck-Boost Operation with $V_I < V_O$

Copyright © 2019–2020, Texas Instruments Incorporated

Feature Description (continued)

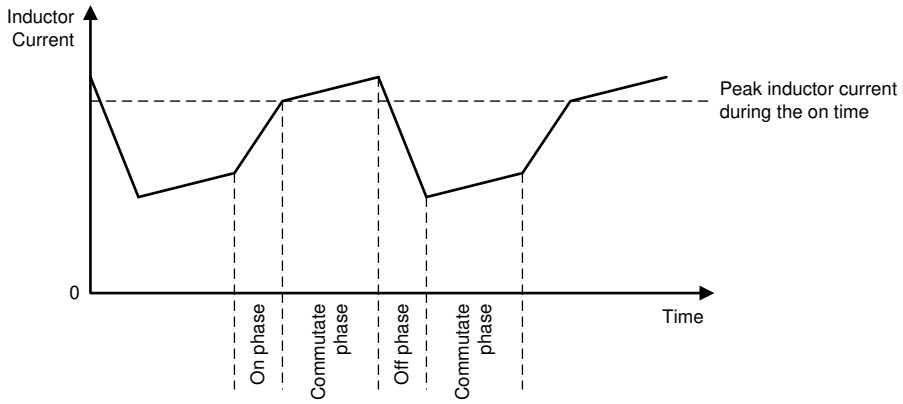


図 9. Peak Current Control – Buck-Boost Operation with $V_I > V_O$

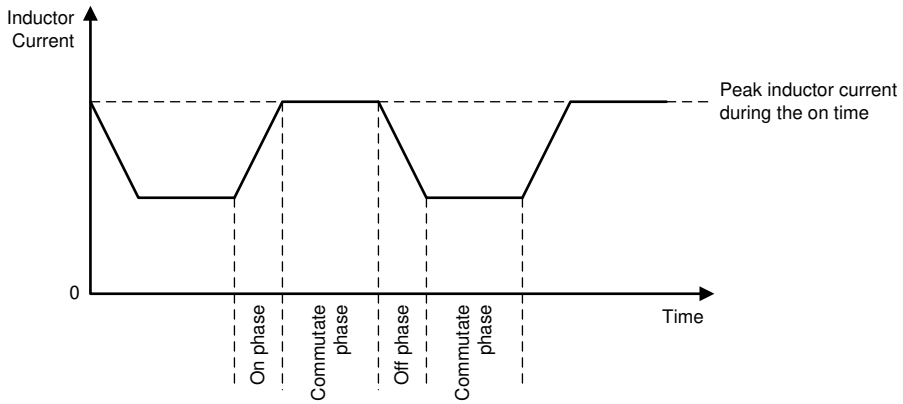


図 10. Peak Current Control – Buck-Boost Operation with $V_I = V_O$

During PWM operation, current can flow in the reverse direction (from output to input). In this case, the error amplifier provides a negative peak current target. Note that the average reverse current is greater (more negative) than the peak current (see 図 11 and 図 12).

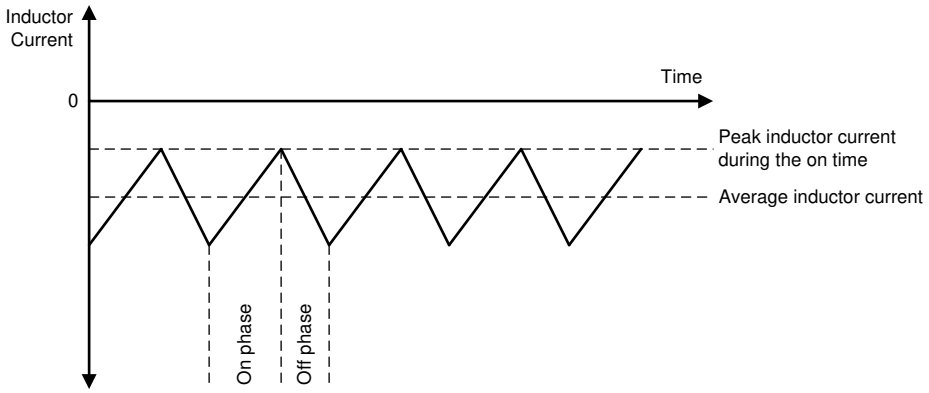


図 11. Reverse Peak Current Control – Buck and Boost Operation

Feature Description (continued)

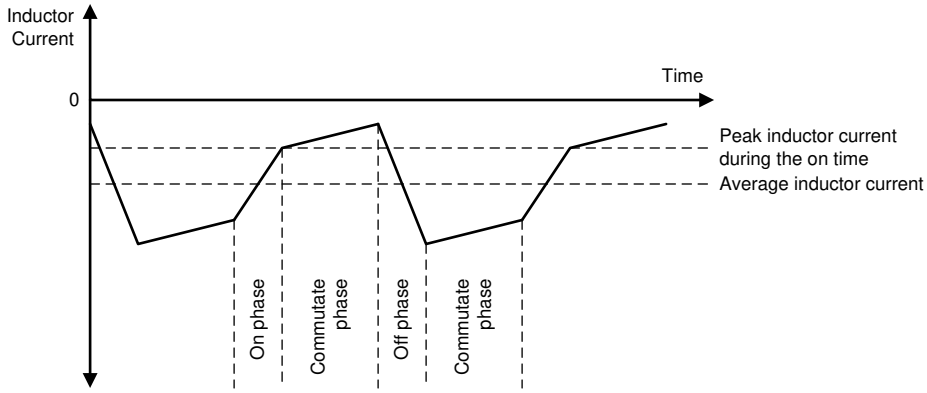


図 12. Reverse Peak Current Control – Buck-Boost Operation, with $V_I > V_O$

8.3.3 Power-Save Mode Operation (PSM)

To increase efficiency across a wide range of operating conditions, the device automatically changes from pulse-width modulation (PWM) at medium and high output currents to pulse-frequency modulation (PFM) at low output currents.

- During PWM operation, the device switches continuously and adjusts the duty cycle of each switching cycle to regulate the output voltage.
- During PFM operation, the device switches in bursts of a few switching cycles, separated by periods when the device does not switch (see 図 13). PFM operation increases efficiency at low output currents because when the device does not switch, there are no switching losses and most of the internal circuitry is disabled, which reduces quiescent power consumption. A comparator with hysteresis compares the output voltage of the error amplifier to a predefined PFM threshold voltage. When the output voltage of the error amplifier is greater than the burst threshold voltage, the device starts switching. When the output voltage of the error amplifier is less than the burst threshold voltage, the device stops switching. This scheme automatically adjusts the frequency and the duration of the switching bursts to regulate the output voltage. During PFM operation, the output voltage ripple can be higher and the transient response is not as good as during PWM operation (see 表 1).

To enable power-save mode, clear the FPWM bit in the Control register to 0.

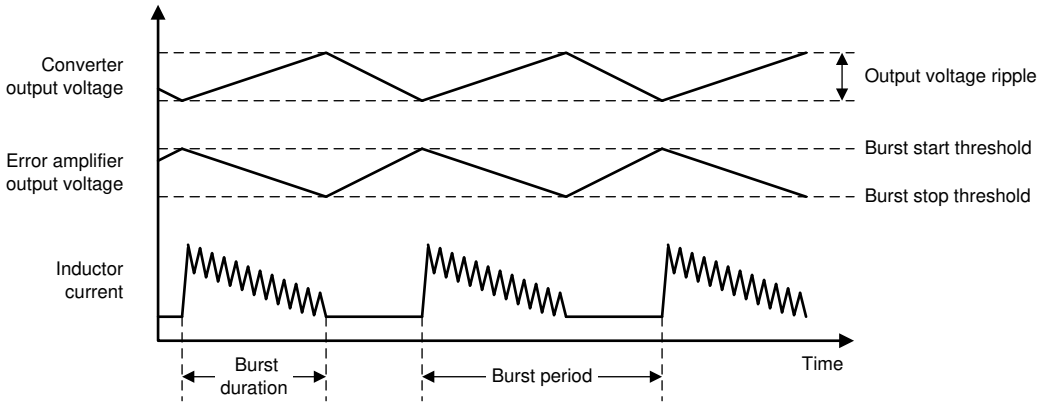


図 13. Pulse-Frequency Modulation

Copyright © 2019–2020, Texas Instruments Incorporated

表 1. Forced-PWM versus Power-Save Mode Performance Comparison

PERFORMANCE PARAMETER	BEST OPERATING MODE
Low-power efficiency	Power-Save Mode (PSM)
Medium- and high-power efficiency	No difference
DC Output voltage accuracy	Forced-PWM
Transient response	Forced-PWM
Output voltage ripple	Forced-PWM

8.3.4 Forced-PWM Operation (FPWM)

During forced-PWM operation, the device uses PWM for all operating conditions. Forced-PWM operation has lower output voltage ripple and better transient response than power-save mode operation, but lower efficiency at low output currents (see 表 1).

Note that the device inhibits forced-PWM operation during start-up (that is, until the converter output has reached power-good for the first time).

To enable forced-PWM operation, set the FPWM bit in the Control register to 1.

8.3.5 Ramp-PWM Operation (RPWM)

If Ramp-PWM operation is enabled, the device operates in forced-PWM when it ramps from one output voltage to another during dynamic voltage scaling. This function is useful if you want the device to operate in power-save mode, but you want to make sure that dynamic voltage scaling ramps the output voltage up and down in a controlled way. If the device operates in power-save mode and Ramp-PWM is disabled, the device cannot always control the ramp from a higher output voltage to a lower output voltage, because in power-save mode the device cannot sink current (see 図 14).

To enable Ramp-PWM operation, set the RAMP bit in the Control register to 1. To disable Ramp-PWM operation, clear the RAMP bit in the Control register to 0.

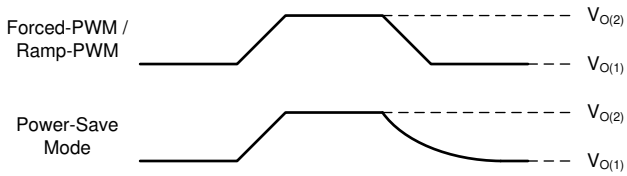


図 14. Ramp-PWM Operation

8.3.6 Device Enable (EN)

The EN pin enables and disables the device.

- When the EN pin is high, the device is enabled.
- When the EN pin is low, the device is disabled.

You can also use the ENABLE bit in the Control register to enable and disable the output of the converter (see the *Register Map*).

表 2. Device Enable Truth Table

ENABLE PIN (EN)	ENABLE BIT	DEVICE STATE	OUTPUT STATE
0	X	Device in Shutdown	Output Discharge Active
1	0	Programming Interface Active	Output Discharge Active
1	1	Device Active	Output Enabled

Copyright © 2019–2020, Texas Instruments Incorporated

8.3.7 Undervoltage Lockout (UVLO)

The device has an undervoltage lockout function that disables the device when the supply voltage is too low for correct operation.

8.3.8 Soft Start

To minimize inrush current and output voltage overshoot during start-up, the device has a soft-start function. At turn on, the switch current limit ramps gradually to its maximum value and the device starts up in a controlled way. The gradual increase of the current limit generates the smallest inrush current for no-load conditions. It is also possible to start into a high load as long as the load does not exceed the device current limit.

The rise time of the output voltage changes with the application circuit and the operating conditions. The output voltage rise time increases if the following occurs:

- The output capacitance is large.
- The load current is large.
- The device operates in boost mode.

See the *Application and Implementation* section for output voltage rise times in a typical application.

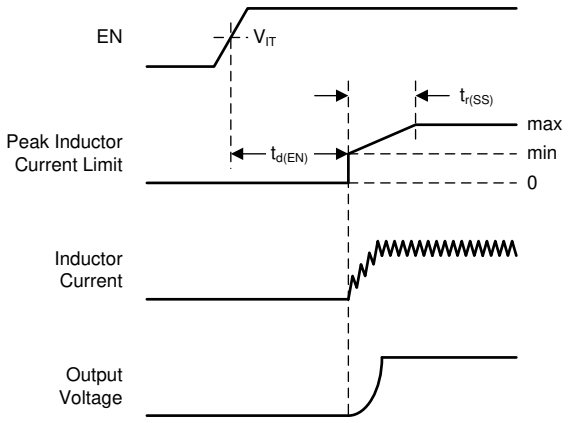


図 15. Device Start-Up

8.3.9 Output Voltage Control

The device can generate output voltages from 1.8 V to 5.2 V with a resolution of 25 mV. To set the output voltage, you must first program the RANGE bit in the Control register to select the output voltage range:

- When RANGE = 0, you can program the output voltage from 1.8 V to 4.975 V.
- When RANGE = 1, you can program the output voltage from 2.025 V to 5.2 V.

When you have selected the output voltage range, you can program the VOUT1 register and VOUT2 register to set the output voltage:

- When RANGE = 0, V_O = (VOUT[6:0] × 0.025) + 1.8 V
- When RANGE = 1, V_O = (VOUT[6:0] × 0.025) + 2.025 V

VOUT[6:0] is the 7-bit value in the VOUT1 register or VOUT2 register, whichever is active.

The VSEL pin selects which VOUT register is active:

- When VSEL = low, the VOUT1 register sets the output voltage.
- When VSEL = high, the VOUT2 register sets the output voltage.

Copyright © 2019–2020, Texas Instruments Incorporated

注

To prevent output voltage transients, TI recommends that you do not change the output voltage range while the converter is in operation. Instead, clear the ENABLE bit in the Control register to 0 to disable the DC/DC converter before you change the RANGE bit.

8.3.9.1 Dynamic Voltage Scaling

The device has a dynamic voltage scaling (DVS) function which lets you change the output voltage in a controlled way during operation. 図 16 shows a simplified block diagram of the DVS function. The VSEL pin controls a multiplexer which selects either the VOUT1 register or the VOUT2 register to control the set voltage. The ramp control block detects when the target output voltage is different from the actual output voltage and ramps the output voltage to the target voltage in 25-mV steps. You can use the 2-bit SLEW parameter in the Control register to select one of four slew rates from 0.5 V/ms to 10 V/ms.

The device starts a DVS ramp when you change the logic level on the VSEL pin or program to a new value in the active VOUT register.

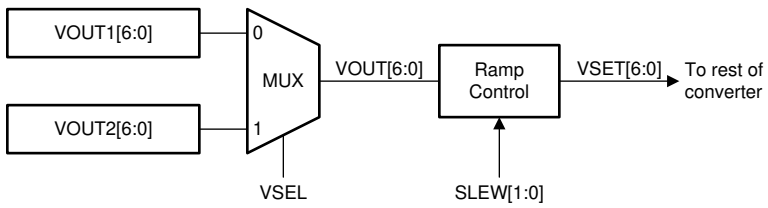
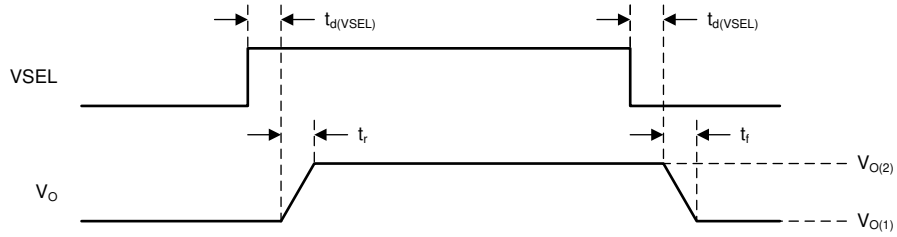


図 16. Dynamic Voltage Scaling Block Diagram

Note that if you change the contents of the active VOUT register or change the state of the VSEL pin during start-up (that is, before the end of the soft start), the converter uses the new value immediately and does not ramp gradually to the final value.

図 17 shows the timing diagram when you use the VSEL pin to change between the output voltage values in the VOUT1 and VOUT2 registers.



$$t_r = t_f = \frac{|V_{O(1)} - V_{O(2)}|}{SR}$$

Where

- $V_{O(1)}$ is the output voltage set by the VOUT1 register
- $V_{O(2)}$ is the output voltage set by the VOUT2 register
- SR is the slew rate set by the SLEW bits in the CONTROL register

図 17. DVS Timing Diagram Using the VSEL Pin

図 18 shows the timing diagram when you use the I^2C interface to change the output voltage value in one of the VOUT registers.

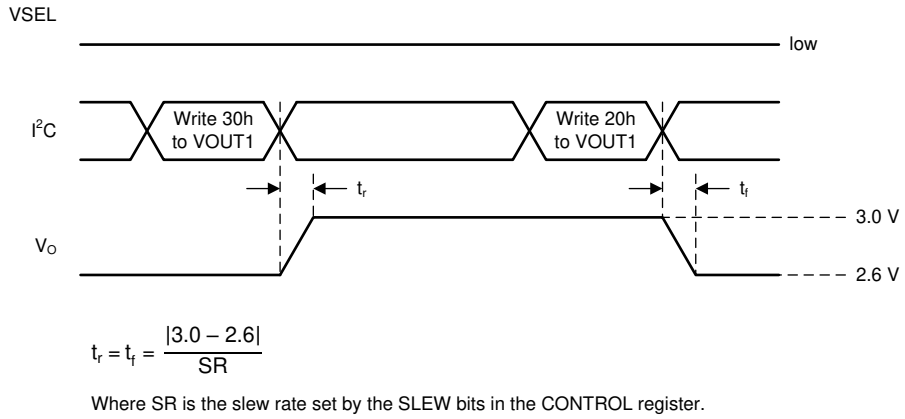


図 18. DVS Timing Using the I²C Interface

8.3.10 Protection Functions

8.3.10.1 Input Voltage Protection (IVP)

Under certain operating conditions, current can flow from the output of the device to the input. For example, this can occur during dynamic voltage scaling when the output ramps down to a lower voltage and the VOUT pin sinks current from the output capacitor. Under such conditions, if the voltage source supplying the device cannot sink current, the voltage on the VIN pin can rise uncontrollably.

To make sure the input voltage stays within the permitted range, the device stops switching if the voltage on the VIN pin is greater than 5.7 V. The device automatically starts to switch again when the voltage on the VIN pin is less than 5.7 V.

The device sets the $\overline{PG}$ bit in the Status register when an input overvoltage event occurs. The device clears the $\overline{PG}$ bit if the Status register is read when the power-not-good condition no longer exists.

8.3.10.2 Current Limit Mode and Overcurrent Protection

The device has a clamp circuit which limits the peak inductor current in the event of an overload. The exact value of the output current during an overload changes with the operating conditions (V_I and V_O) and the switching mode (buck, buck-boost, or boost) – see 図 52.

Overloads increase the power dissipation in the device, which increases its temperature. If the device becomes too hot, the thermal shutdown function turns off the converter. When the device cools down, the thermal shutdown function automatically turns on the converter again. Thus, under a permanent overload condition, the device can periodically turn on and off, as it cools down and then heats up.

8.3.10.3 Thermal Shutdown

The device has a thermal shutdown function which turns off the converter if the junction temperature is greater than 150°C. The device automatically turns on the converter again when the junction temperature is less than 130°C. You can still use the I²C interface to read and write to the registers when the device is in an overtemperature condition.

When the device detects an overtemperature condition, it sets the TSD bit in the Status register to 1. The device clears the TSD bit to 0 if you read the Status register when the junction temperature of the device is less than 130°C.

8.3.11 Power Good

The device has a power-good function which indicates if the output of the DC/DC converter is in regulation or not. The device detects a power-good condition when the output voltage is greater than 95% of its nominal value and detects a power-not-good condition when the output voltage is less than 90% of its nominal value.

When a power-not-good condition occurs, the device sets the $\overline{PG}$ bit in the Status register to 1. The device clears the $\overline{PG}$ bit to 0 if you read the Status register when a power-good condition exists.

Copyright © 2019–2020, Texas Instruments Incorporated

8.3.12 Load Disconnect

During device shutdown, the input is disconnected from the output. This prevents any current flow from the output to the input or from the input to the output.

8.3.13 Output Discharge

The device actively discharges the output when the EN pin is low or the ENABLE bit is set to zero.

8.4 Device Functional Modes

The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

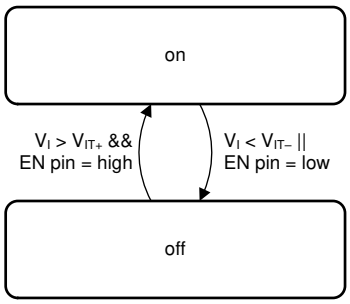


図 19. Device Functional Modes

8.5 Programming

8.5.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see *NXP Semiconductors, UM10204 – I^2C-Bus Specification and User Manual*). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through open-drain I/O pins, SDA, and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and transmits data on the bus under control of the master device.

The device works as a slave and supports the following data transfer modes, as defined in the I^2C-Bus Specification:

- Standard-mode (100 kbps)
- Fast-mode (400 kbps)
- Fast-mode Plus (1 Mbps)

The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values, depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.1 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, it is referred to as F/S-mode in this document. The device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is 75h (1110101b).

To make sure that the I^2C function in the device is correctly reset, it is recommended that the I^2C master initiates a STOP condition on the I^2C bus after the initial power up of SDA and SCL pullup voltages.

Programming (continued)

8.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The master initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 図 20. All I^{2}C-compatible devices recognize a start condition.

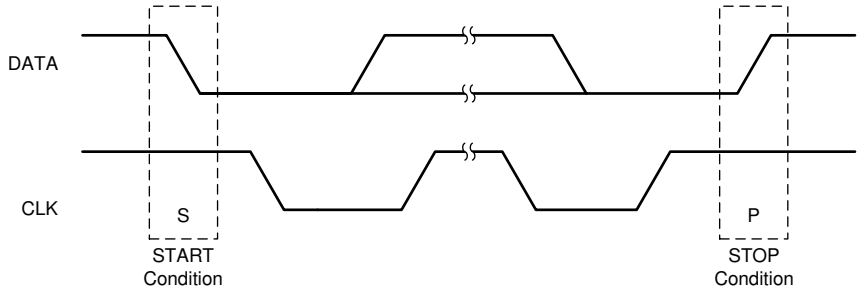


図 20. START and STOP Conditions

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit, R/W, on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 図 21). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see 図 22) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

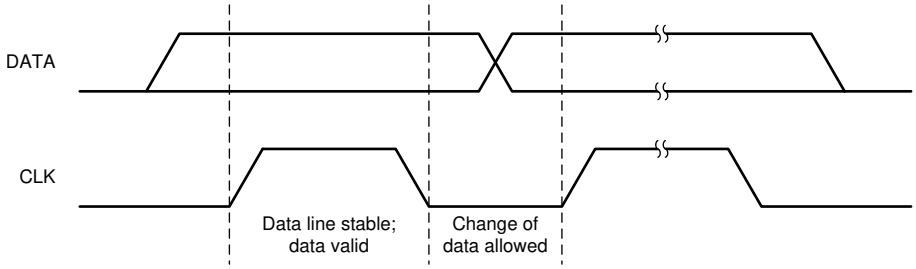


図 21. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 20). This releases the bus and stops the communication link with the addressed slave. All I^{2}C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

Copyright © 2019–2020, Texas Instruments Incorporated

Programming (continued)

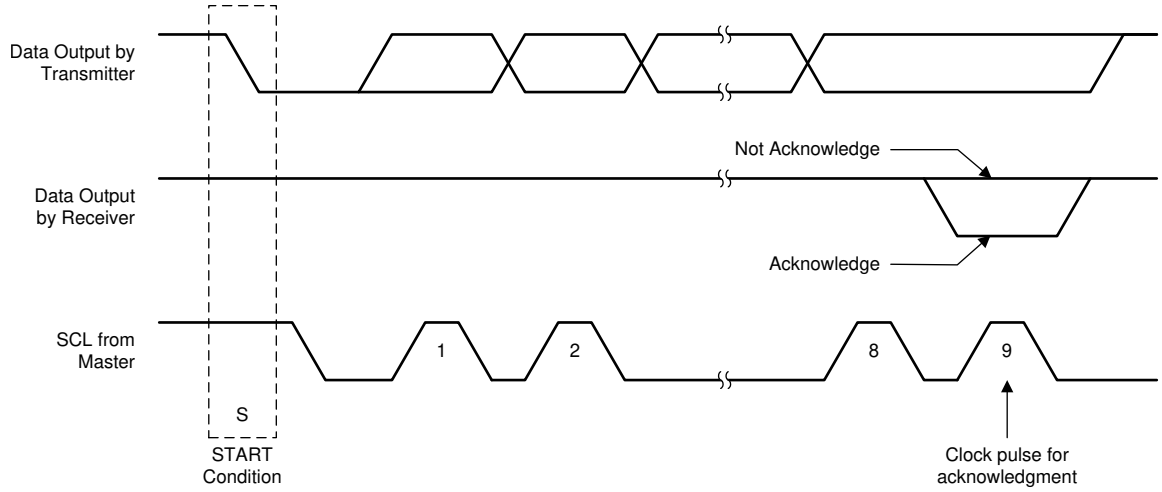


図 22. Acknowledge on the I²C Bus

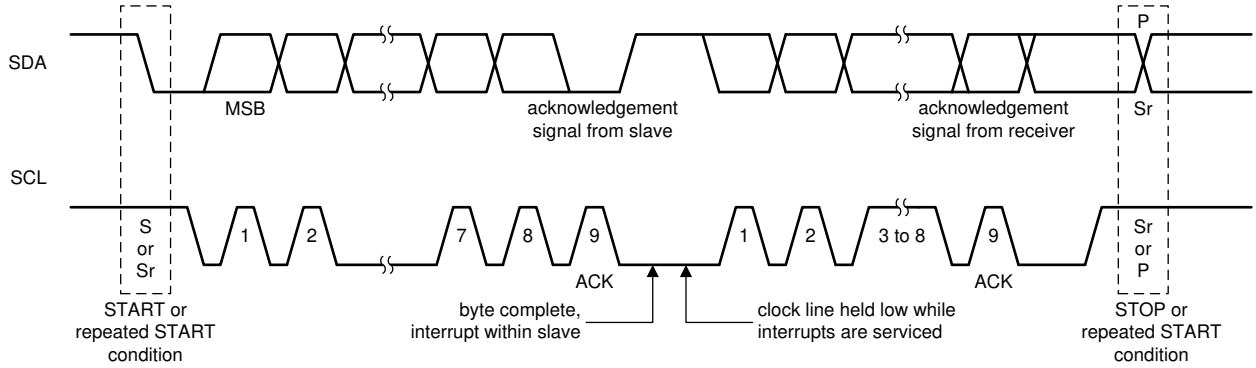


図 23. Bus Protocol

8.5.3 I²C Update Sequence

A single update requires the following:

- A start condition
- A valid I²C slave address
- A register address
- A data byte

To acknowledge the receipt of each byte, the device pulls the SDA line low during the high period of a single clock pulse. The device performs an update on the falling edge of the acknowledge signal that follows the last byte.

Programming (continued)

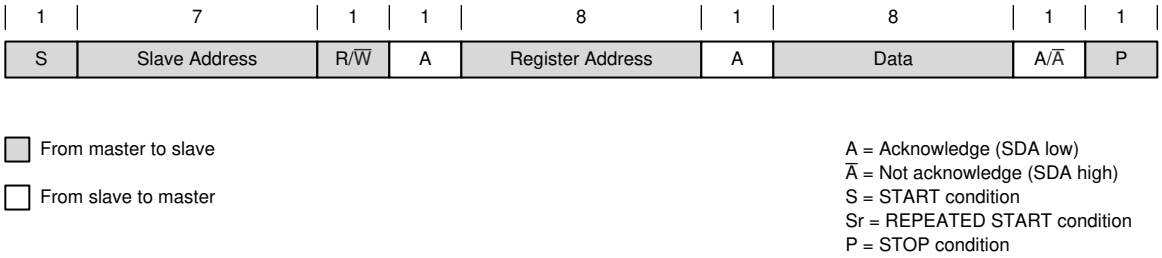


図 24. “Write” Data Transfer Format in Standard, Fast, and Fast-Plus Modes

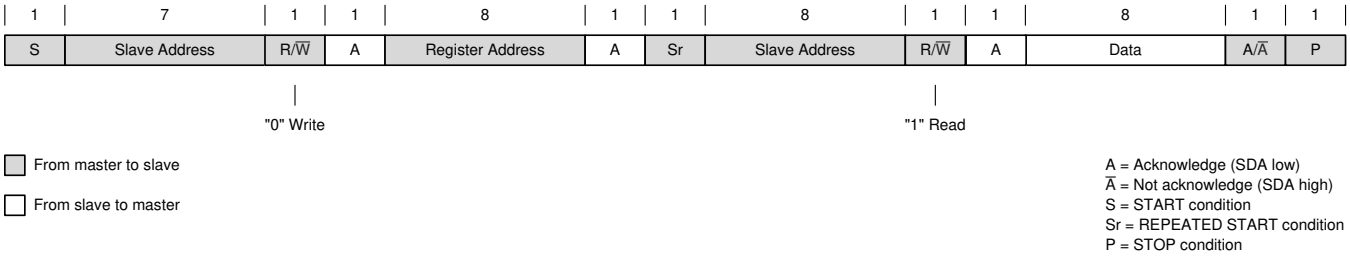


図 25. “Read” Data Transfer Format in Standard, Fast, and Fast-Plus Modes

Copyright © 2019–2020, Texas Instruments Incorporated

8.6 Register Map

8.6.1 Register Description

8.6.1.1 Register Map

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0x01	CONTROL	Control Register	Go
0x02	STATUS	Status Register	Go
0x03	DEVID	DEVID Register	Go
0x04	VOUT1	VOUT1 Register	Go
0x05	VOUT2	VOUT2 Register	Go

8.6.1.2 Register CONTROL (Slave address: 0b1110101; Register address: 0x01; Default: 0x00 or 0x20)

Return to Register Map.

Figure 26. Register CONTROL Format

7	6	5	4	3	2	1	0
RESERVED	RANGE	ENABLE	RESERVED	FPWM	RPWM	SLEW[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only

Table 3. Register CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	Reserved for future use. This bit can be written to and read from but it has no function. For compatibility with possible future device variants, it is recommended to program this bit to 0.
6	RANGE	R/W	0	This bit selects the output voltage range. **0: Low range (1.800 V to 4.975 V)** 1 : High range (2.025 V to 5.200 V)
5	ENABLE	R/W	X	This bit controls operation of the converter. 0 : Converter operation disabled (Start-up value for TPS63811) 1 : Converter operation enabled (Start-up value for TPS63810)
4	RESERVED	R/W	0	Reserved for future use. This bit can be written to and read from but it has no function. For compatibility with possible future device variants, it is recommended to program this bit to 0.
3	FPWM	R/W	0	This bit controls the forced-PWM function. **0: Forced-PWM operation disabled** 1 : Forced-PWM operation enabled
2	RPWM	R/W	0	This bit controls the ramp-PWM function. **0: Ramp-PWM operation disabled** 1 : Ramp-PWM operation enabled
1:0	SLEW[1:0]	R/W	00	These bits control the slew rate of the DVS function. **00: 1.0 V/ms** 01: 2.5 V/ms 10: 5.0 V/ms 11: 10.0 V/ms

8.6.1.3 Register STATUS (Slave address: 0b1110101; Register address: 0x02; Default: 0x00)

Return to Register Map.

Figure 27. Register STATUS Format

7	6	5	4	3	2	1	0
NIL[5:0]						TSD	PGn
R						R	R

LEGEND: R/W = Read/Write; R = Read only

Table 4. Register STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7:2	NIL[5:0]	R	000000	Not used. These bits always return 0 when read.
1	TSD	R	0	This bit shows the status of the thermal shutdown function. This bit is cleared if the STATUS register is read when the overtemperature condition no longer exists. **0: Temperature good** 1 : An overtemperature event was detected.
0	PGn	R	0	This bit shows the status of the power-good comparator. This bit is cleared if the STATUS register is read when the power-not-good condition no longer exists. **0: Power-good** 1 : A power-not-good event was detected.

Copyright © 2019–2020, Texas Instruments Incorporated

8.6.1.4 Register DEVID (Slave address: 0b1110101; Register address: 0x03; Default: 0x04)

Return to *Register Map*.

Figure 28. Register DEVID Format

7	6	5	4	3	2	1	0
MANUFACTURER[3:0]				MAJOR[1:0]		MINOR[1:0]	
R				R		R	

LEGEND: R/W = Read/Write; R = Read only

Table 5. Register DEVID Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MANUFACTURER[3:0]	R	0000	These bits identify the device manufacturer. **0000: Texas Instruments**
3:2	MAJOR[1:0]	R	01	These bits identify the major silicon revision. 00: A (initial silicon) **01: B (first major revision)** 10: C (second major revision) 11: D (third major revision)
1:0	MINOR[1:0]	R	00	These bits identify the minor silicon revision. **00: 0 (initial silicon)** 01: 1 (first minor revision) 10: 2 (second minor revision) 11: 3 (third minor revision)

8.6.1.5 Register VOUT1 (Slave address: 0b1110101; Register address: 0x04; Default: 0x3C)

Return to *Register Map*.

Figure 29. Register VOUT1 Format

7	6	5	4	3	2	1	0
NIL	VOUT1[6:0]						
R	R/W						

LEGEND: R/W = Read/Write; R = Read only

Table 6. Register VOUT1 Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0	Not used This bit always returns 0 when read.
6:0	VOUT1[6:0]	R/W	0111100	These bits set the output voltage when the VSEL pin is low. Output voltage = 1.800 + (VOUT1[6 :0] × 0.025) V (low range) (default = 3.3 V) Output voltage = 2.025 + (VOUT1[6 :0] × 0.025) V (high range) (default = 3.525 V)

8.6.1.6 Register VOUT2 (Slave address: 0b1110101; Register address: 0x05; Default: 0x42)

Back to *Register Map*.

Figure 30. Register VOUT2 Format

7	6	5	4	3	2	1	0
NIL	VOUT2[6:0]						
R	R/W						

LEGEND: R/W = Read/Write; R = Read only

Table 7. Register VOUT2 Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0	Not used This bit always returns 0 when read.

Table 7. Register VOUT2 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	VOUT2[6:0]	R/W	1000010	These bits set the output voltage when the VSEL pin is high. Output voltage = 1.800 + (VOUT2[6 :0] × 0.025) V (low range) (default = 3.45 V) Output voltage = 2.025 + (VOUT2[6 :0] × 0.025) V (high range) (default = 3.675 V)

Copyright © 2019–2020, Texas Instruments Incorporated

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS63810 and TPS63811 devices are high efficiency, high current buck-boost converters, suitable for applications where the input voltage is higher, lower, or equal to the output voltage. The maximum peak current in the switches is limited to a typical value of 6 A.

9.2 Typical Applications

9.2.1 1.8-V to 5.2-V Output Smartphone Power Supply

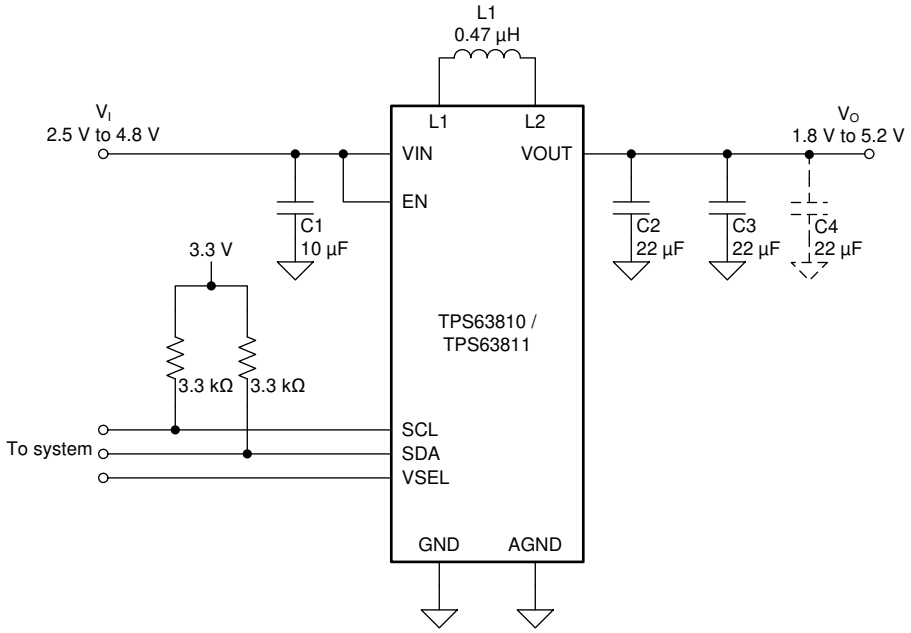


図 31. Typical Application Schematic

9.2.1.1 Design Requirements

This example uses the design parameters listed in 表 8.

表 8. Design Parameters

DESIGN PARAMETER	SYMBOL	EXAMPLE VALUE
Input voltage	V_I	2.5 V to 4.8 V
Output voltage	V_O	1.8 V to 5.2 V
Output current	I_O	2 A
I^2C bus voltage	V_{BUS}	3.3 V
I^2C bus capacitance	C_b	100 pF
I^2C bus speed		Fast-mode (400 kHz)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Input Capacitor Selection

TI recommends a minimum input capacitance (including DC bias effects) of 5 µF. A 10-µF, 10-V ceramic capacitor is suitable for typical applications. If the input supply is located more than a few centimeters from the converter, you may need to add additional bulk capacitance (a 47-µF electrolytic or tantalum capacitor is a typical choice).

The output capacitance does not have an upper limit; you can make it as big as you want.

9.2.1.2.2 Inductor Selection

TI recommends you use the TPS63810 device with 0.47-µH inductors. For high efficiencies, use an inductor with a low DC resistance (DCR) and low core losses.

The saturation current of the inductor must be greater than the maximum inductor current in your application. To include sufficient margin for worst-case and transient operating conditions, TI recommends you use an inductor with saturation current that is at least 20% higher than the maximum inductor current in your application. The maximum current in the inductor occurs when the device operates in boost mode and the following is true:

- The input voltage is at its minimum value.
- The output voltage is at its maximum value.
- The output current is at its maximum value.

To calculate the maximum inductor current, first use 式 1 to calculate the maximum duty cycle during boost operation (which is when the maximum inductor current occurs).

$$D = \frac{V_O - V_I}{V_O}$$

where

- D is the duty cycle
- V_I is the input voltage
- V_O is the output voltage (1)

$$D = \frac{5\ V - 2.5\ V}{5\ V} = 0.5$$

Next, use 式 2 to calculate the maximum inductor current.

$$I_{LM} = \frac{I_O}{\eta(1 - D)} + \frac{DV_I}{2fL}$$

where

- I_{LM} is the peak inductor current
- I_O is the output current
- η is the converter efficiency (use the value from the application curves or assume 90%)
- D is the duty cycle (calculated with 式 1)
- V_I is the input voltage
- f is the switching frequency (assume 2 MHz)
- L is the inductance (use 0.47 µH) (2)

$$I_{LM} = \frac{2\ A}{(0.9)(1 - 0.5)} + \frac{(0.5)(2.5\ V)}{(2)(2\ MHz)(0.47\ \mu H)} = 5.1\ A$$

Copyright © 2019–2020, Texas Instruments Incorporated

To include enough margin for transient conditions, TI recommends you use an inductor with a saturation current rating at least 20% higher than the calculated maximum current. In this example, TI recommends an inductor with a saturation current of at least 6.1 A.

9.2.1.2.3 *Output Capacitor Selection*

TI recommends a minimum output capacitance (including DC bias effects) of 16 µF. Two 22-µF, 10-V ceramic capacitors are suitable for typical applications with $V_O \leq 3.6$ V. For $V_O > 3.6$ V, three 22-µF or two 47-µF ceramic capacitors are suitable. If you want to minimize switching noise on the output, connect a small ceramic capacitor (100 nF is a typical value) in parallel to the two main output capacitors and place it closest to the VOUT pin. Smaller capacitors have lower parasitic inductance and are more effective at filtering high frequencies than the two main output capacitors.

The output capacitance does not have an upper limit, however, very large values of output capacitance make the transient response of the converter slower.

It is important that the effective capacitance is given according to the recommended value in Recommended Operating Conditions. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a trade-off between size and transient behavior as higher capacitance reduces transient response overshoot and undershoot and increases transient response time. 表 9 lists possible output capacitors.

表 9. List of Recommended Capacitors(1)

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
22	6.3	10	GRM187R60J226ME15	Murata	0603 (1608)
22	10	40	GRM187R61A226ME15	Murata	0603 (1608)
47	6.3	43	GRM188R60J476ME15	Murata	0603 (1608)
47	6.3	43	GRM219R60J476ME44	Murata	0805 (2012)

(1) See *Third-party Products Disclaimer*.

9.2.1.2.4 I²C Pullup Resistor Selection

Refer to the *NXP Semiconductors, UM10204 – I²C-Bus Specification and User Manual* for the specifications relevant to your application.

Use 式 3 to calculate the maximum permitted pullup resistor value for the bus speed used in the application.

$$R_P(\max) = \frac{t_r}{0.8473 \times C_b}$$

where

- t_r is the maximum permitted rise time (300 ns for Fast-mode)
- C_b is the capacitive load on each bus line (3)

$$R_P(\max) = \frac{300\ \text{ns}}{0.8473 \times 100\ \text{pF}} = 3.541\ \text{k}\Omega$$

If you do not know what the bus capacitance is in your application, start with a 1-kΩ pullup resistor and measure the rise time with an oscilloscope. Use 式 3 to calculate the bus capacitance and thus the maximum permitted pullup resistor.

Use 式 4 to calculate the minimum permitted pullup resistor value for different bus speeds.

$$R_P(\min) = \frac{V_{BUS} - V_{OL}}{I_{OL}}$$

where

- V_{BUS} is the I^2C bus pullup voltage
- V_{OL} is the low-level output voltage (0.4 V)
- I_{OL} is the low-level output current (3 mA for Fast-mode) (4)

$$R_P(\text{min}) = \frac{3.3\ \text{V} - 0.4\ \text{V}}{3\ \text{mA}} = 967\ \Omega$$

A pullup resistor value of 3.3 kΩ meets both of these requirements.

Copyright © 2019–2020, Texas Instruments Incorporated

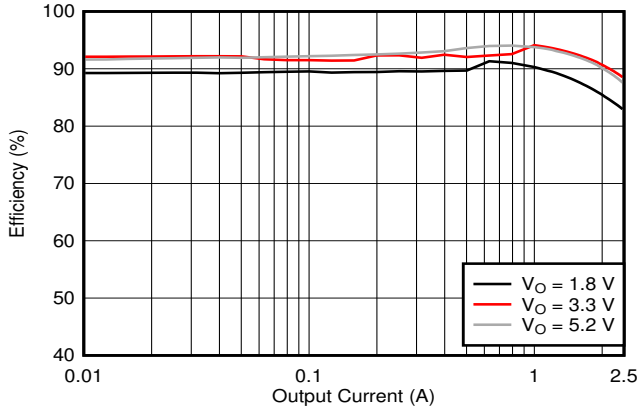
9.2.1.3 Application Curves

表 10 lists the components that were used for the measurements contained in the following pages.

表 10. Components for Application Characteristic Curves

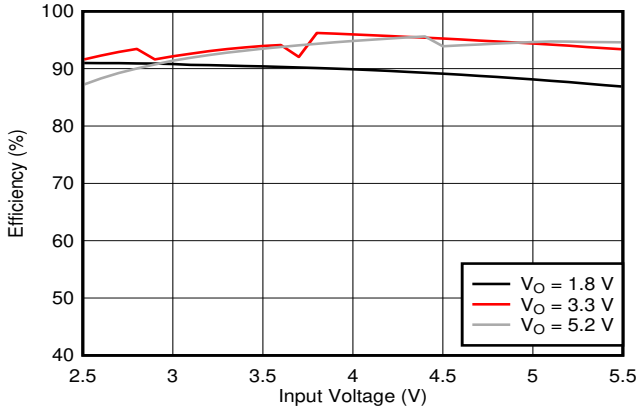
REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER
C1	Capacitor, 10 µF, 10 V, 0603, ceramic	GRM188R61A106ME69	Murata
C2, C3	Capacitor, 22 µF, 10 V, 0603, ceramic	GRM187R61A226ME15	Murata
L1	Inductor, 0.47 µH	XFL4015-471MEC	Coilcraft
U1	Integrated circuit	TPS63810YFF	Texas Instruments

Copyright © 2019–2020, Texas Instruments Incorporated



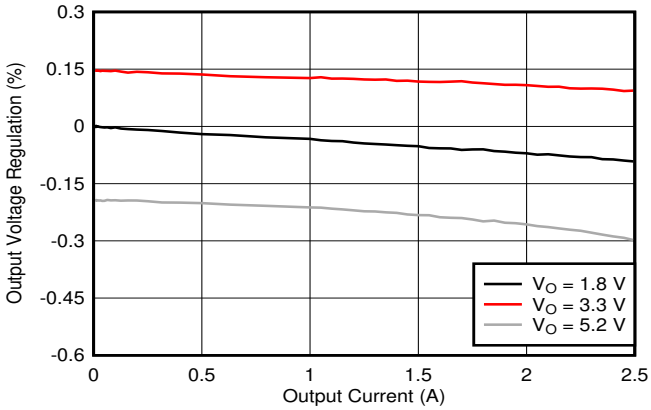
V_I = 3.6 V PSM T_A = 25°C

図 32. Efficiency versus Output Current



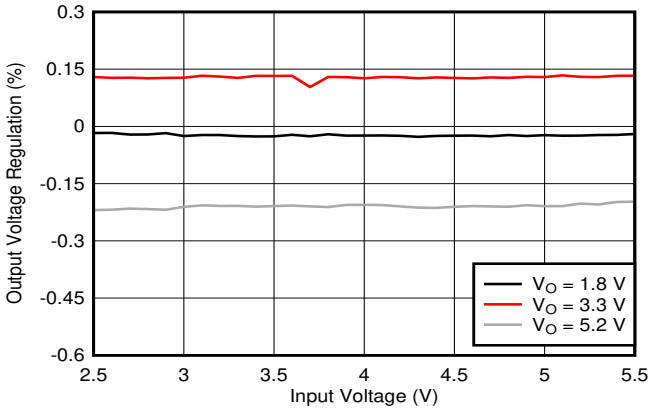
I_O = 1 A PSM T_A = 25°C

図 33. Efficiency versus Input Voltage



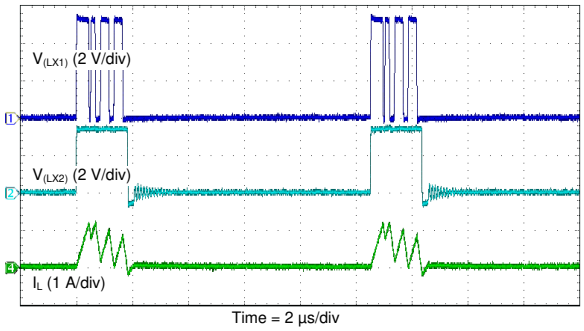
V_I = 3.6 V FPWM T_A = 25°C

図 34. Load Regulation



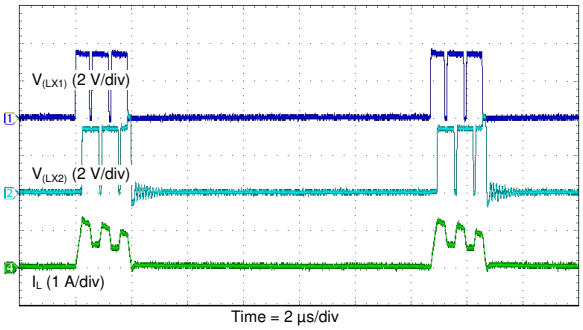
I_O = 1 A FPWM T_A = 25°C

図 35. Line Regulation



V_I = 5 V PSM T_A = 25°C
V_O = 3.3 V I_O = 100 mA

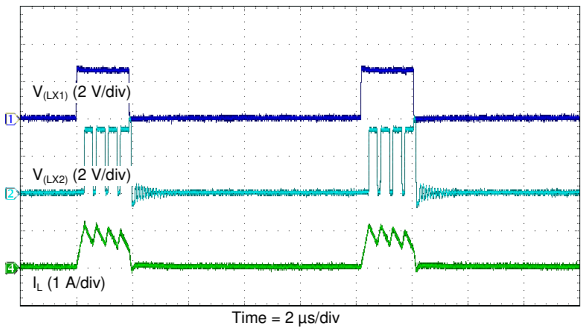
図 36. PFM Switching Waveforms (Buck Operation)



V_I = 3.3 V PSM T_A = 25°C
V_O = 3.3 V I_O = 100 mA

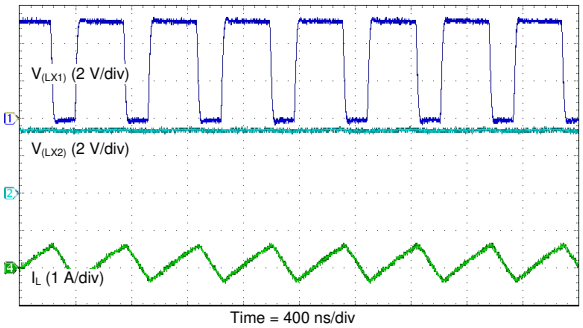
図 37. PFM Switching Waveforms (Buck-Boost Operation)

Copyright © 2019–2020, Texas Instruments Incorporated



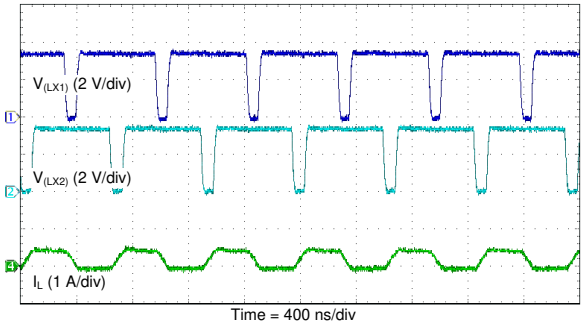
V_I = 2.5 V　PSM　T_A = 25°C
V_O = 3.3 V　I_O = 100 mA

図 38. PFM Switching Waveforms (Boost Operation)



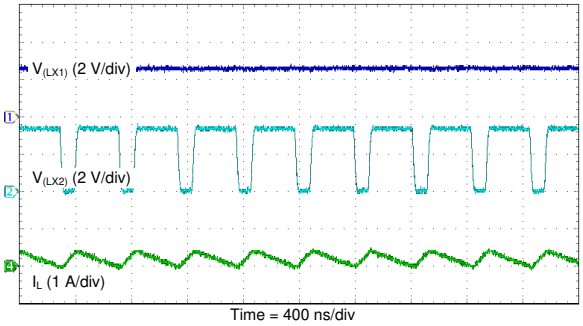
V_I = 5 V　FPWM　T_A = 25°C
V_O = 3.3 V　I_O = 100 mA

図 39. PWM Switching Waveforms (Buck Operation)



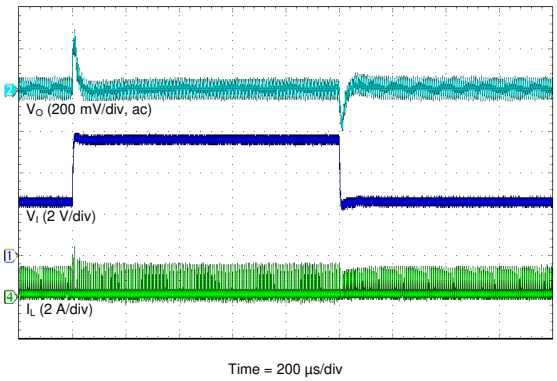
V_I = 3.3 V　FPWM　T_A = 25°C
V_O = 3.3 V　I_O = 100 mA

図 40. PWM Switching Waveforms (Buck-Boost Operation)



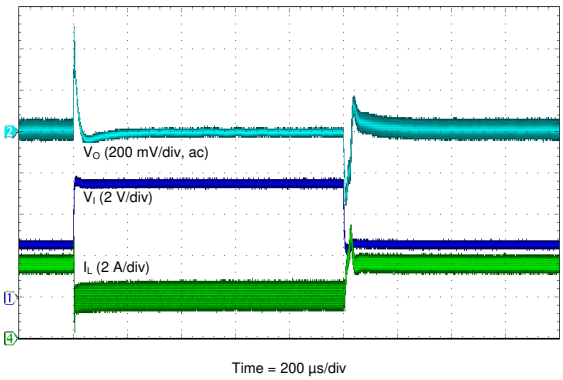
V_I = 2.5 V　FPWM　T_A = 25°C
V_O = 3.3 V　I_O = 100 mA

図 41. PWM Switching Waveforms (Boost Operation)



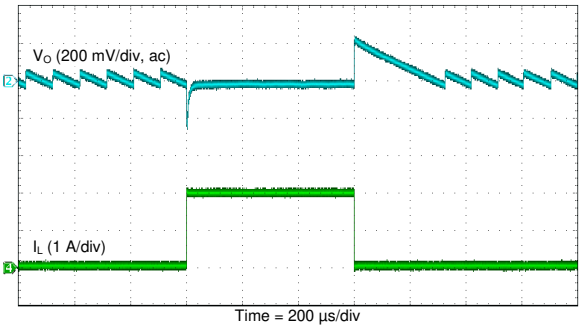
V_I = 2.5 V to 5.5 V　PSM　T_A = 25°C
V_O = 3.3 V　I_O = 200 mA

図 42. Line Transient Response



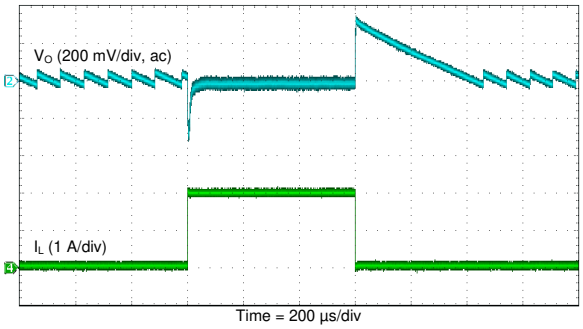
V_I = 2.5 V to 5.5 V　PSM　T_A = 25°C
V_O = 3.3 V　I_O = 2 A

図 43. Line Transient Response



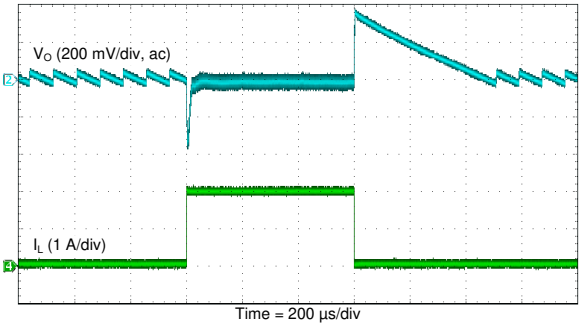
V_I = 4.2 V　PSM　T_A = 25°C
V_O = 3.3 V　I_O = 10 mA to 2 A

図 44. Load Transient Response (Buck)



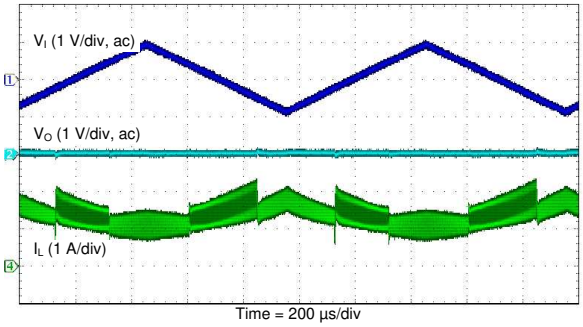
V_I = 3.3 V　PSM　T_A = 25°C
V_O = 3.3 V　I_O = 10 mA to 2 A

図 45. Load Transient Response (Buck-Boost)



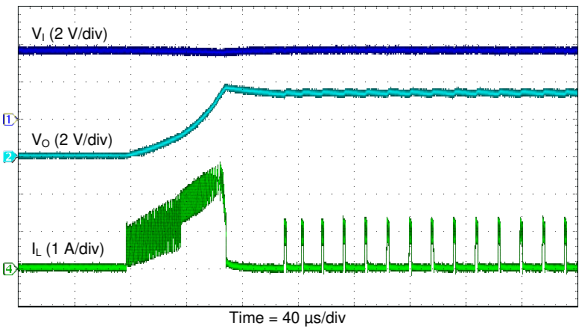
V_I = 2.6 V　PSM　T_A = 25°C
V_O = 3.3 V　I_O = 10 mA to 2 A

図 46. Load Transient Response (Boost)



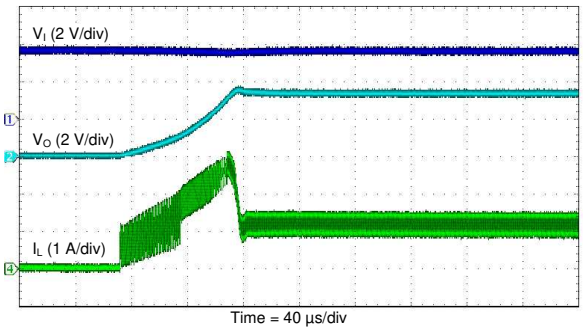
V_I = 3.3 V ±0.9 V　FPWM　T_A = 25°C
V_O = 3.3 V　R_L = 3 Ω

図 47. Line Sweep (PWM)



V_I = 3.6 V　PSM　T_A = 25°C
V_O = 3.3 V　R_L = 33 Ω

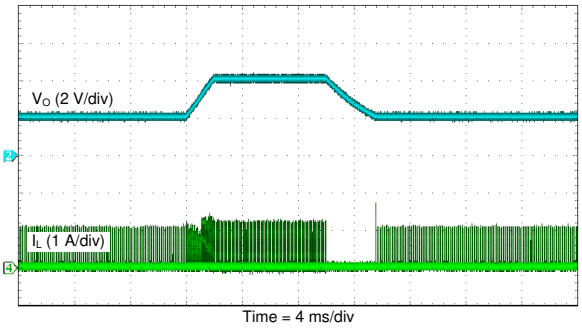
図 48. Start-Up Waveforms (Light Load)



V_I = 3.6 V　PSM　T_A = 25°C
V_O = 3.3 V　R_L = 3.3 Ω

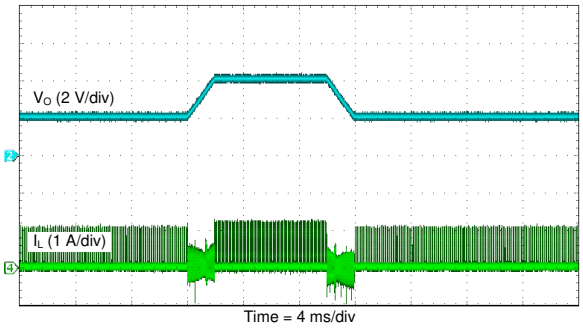
図 49. Start-Up Waveforms (Heavy Load)

Copyright © 2019–2020, Texas Instruments Incorporated



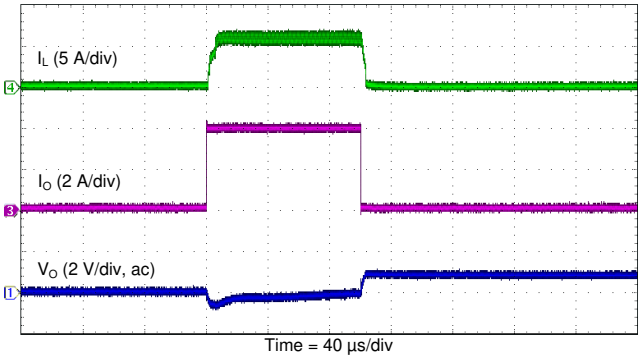
V_I = 3.6 V PSM T_A = 25°C
V_O = 2 V to 4 V R_L = 330 Ω

図 50. Dynamic Voltage Scaling (PFM)



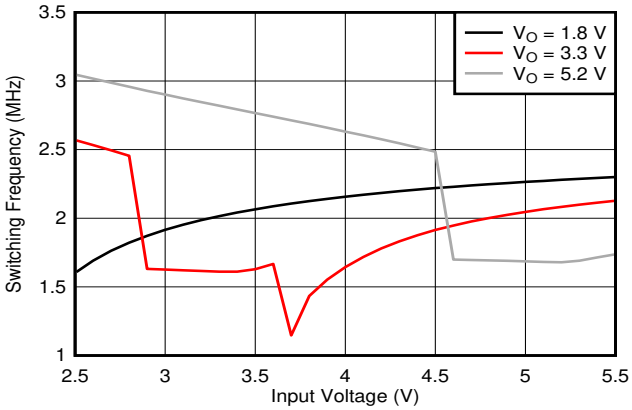
V_I = 3.6 V PSM T_A = 25°C
V_O = 2 V to 4 V RPWM R_L = 330 Ω

図 51. Dynamic Voltage Scaling (RPWM)



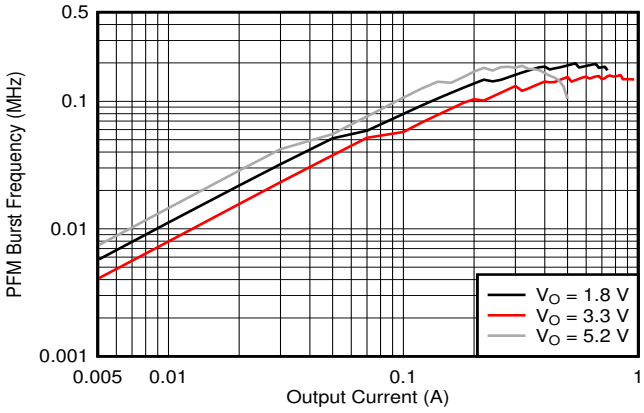
V_I = 3.6 V PSM T_A = 25°C
V_O = 3.3 V

図 52. Overcurrent Protection



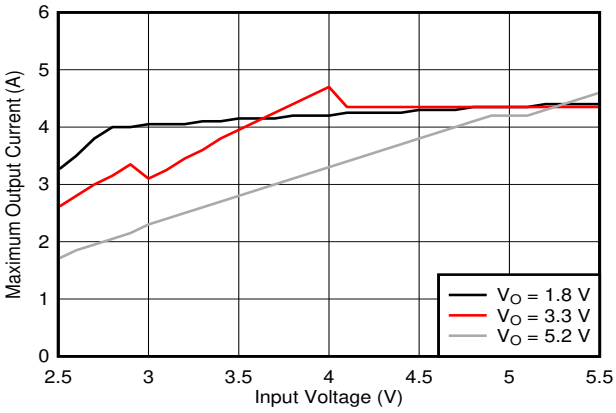
I_O = 1 A FPWM T_A = 25°C
V_I rising

図 53. Switching Frequency versus Input Voltage



V_I = 3.6 V PSM T_A = 25°C

図 54. Burst Switching Frequency versus Output Current



PSM T_A = 25°C

図 55. Maximum Output Current versus Input Voltage

10 Power Supply Recommendations

The device is designed to operate with a DC supply voltage in the range 2.2 V to 5.5 V. If the input supply is more than a few centimeters from the device, TI recommends adding some bulk capacitance to the ceramic bypass capacitors. A 47-µF electrolytic capacitor is a typical selection for the bulk capacitance.

11 Layout

11.1 Layout Guidelines

Correct PCB layout is necessary to obtain the full performance from the device. TI recommends to follow these basic principles:

- Place input and output capacitors close to the device to minimize the input and output loop areas.
- If you combine different-sized capacitors to make up the total input capacitance, place the smallest capacitor closest to the device. The same applies to the output capacitance.
- Keep PCB traces short and wide to minimize parasitic resistance and inductance.
- Use the following PCB layer stack (or something similar):
  - Layer 1 (top): All components and all power traces
  - Layer 2 (inner): Signals
  - Layer 3 (inner): Signals
  - Layer 4 (bottom): Ground plane

図 56 shows an example of the PCB layout used for all of the measurement data in *Application Curves*.

11.2 Layout Example

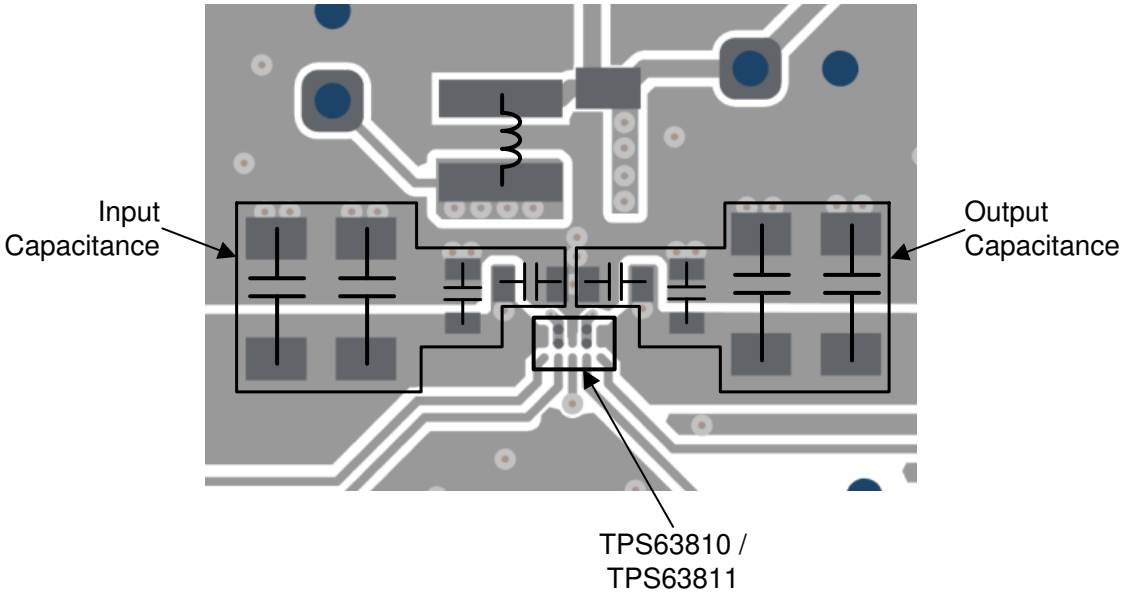


図 56. Recommended PCB Layout for the TPS63810 Device

Copyright © 2019–2020, Texas Instruments Incorporated

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- *NXP Semiconductors、『UM10204 – I²C-bus specification and user manual』* (英語)
- テキサス・インスツルメンツ、*『TPS6381xEVM』ユーザー・ガイド* (英語)

12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 11. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS63810	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS63811	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.5 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.6 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 用語集

SLYZ022 - *TI 用語集*

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

Copyright © 2019–2020, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS63810YFFR	Active	Production	DSBGA (YFF) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63810
TPS63810YFFR.A	Active	Production	DSBGA (YFF) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63810
TPS63811YFFR	Active	Production	DSBGA (YFF) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63811
TPS63811YFFR.A	Active	Production	DSBGA (YFF) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63811

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

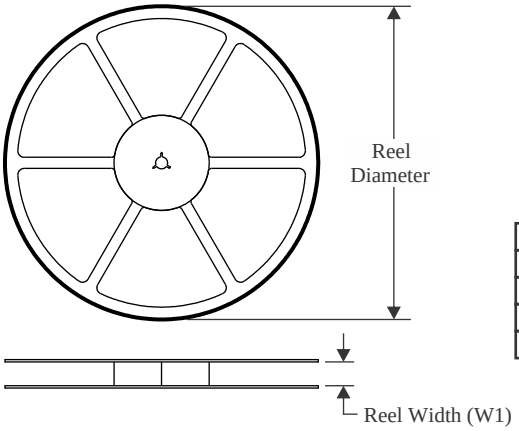
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

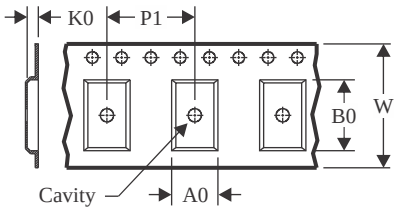
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

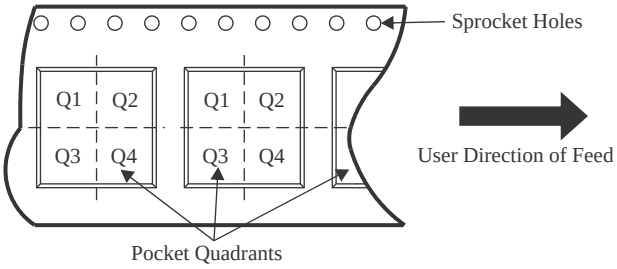


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

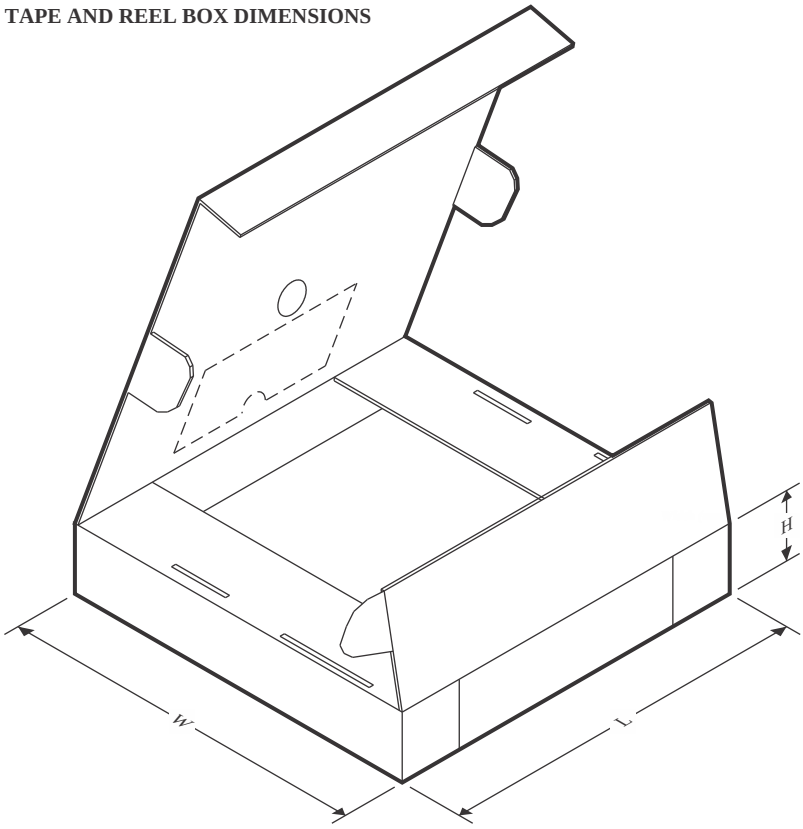
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

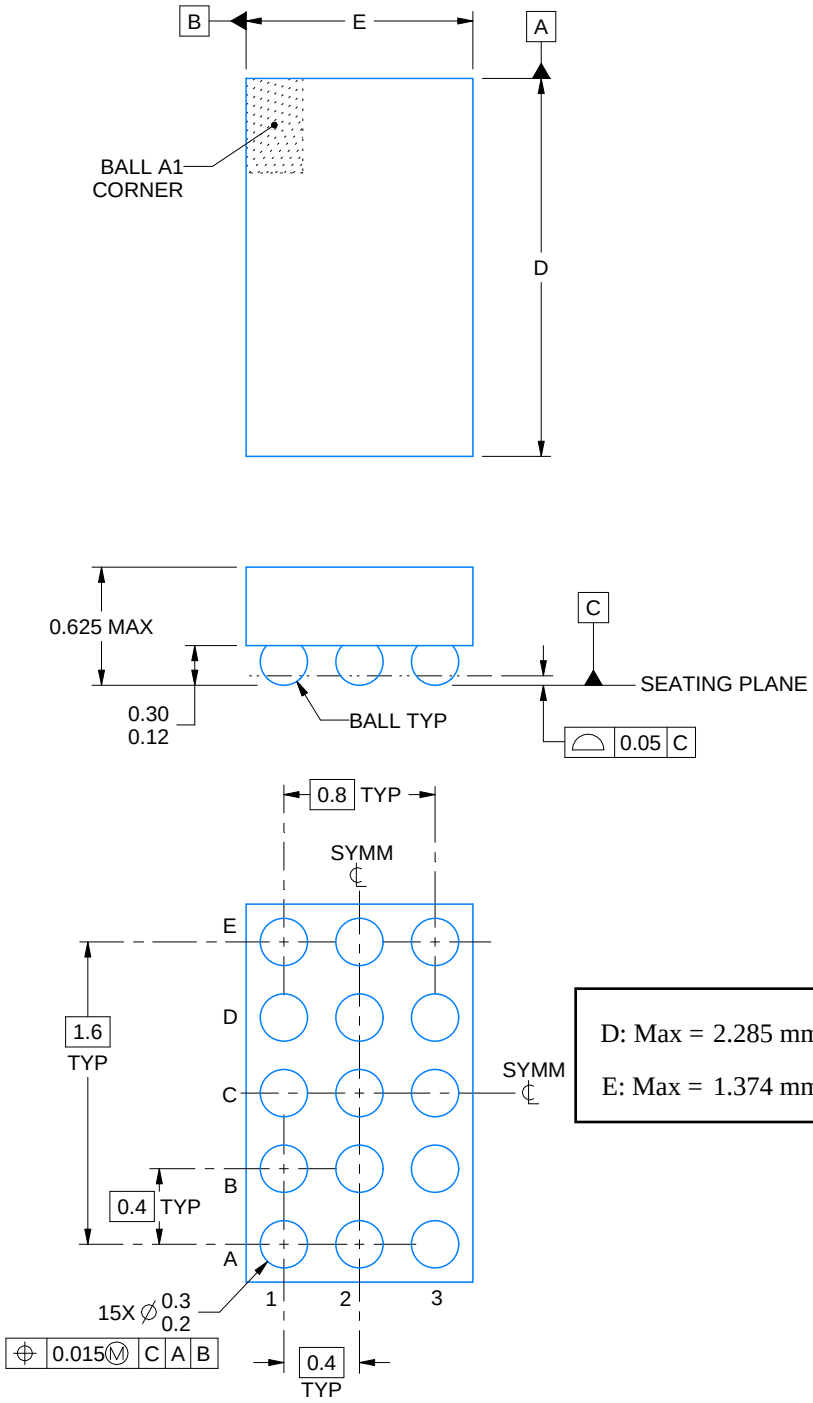
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63810YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1
TPS63811YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63810YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0
TPS63811YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0



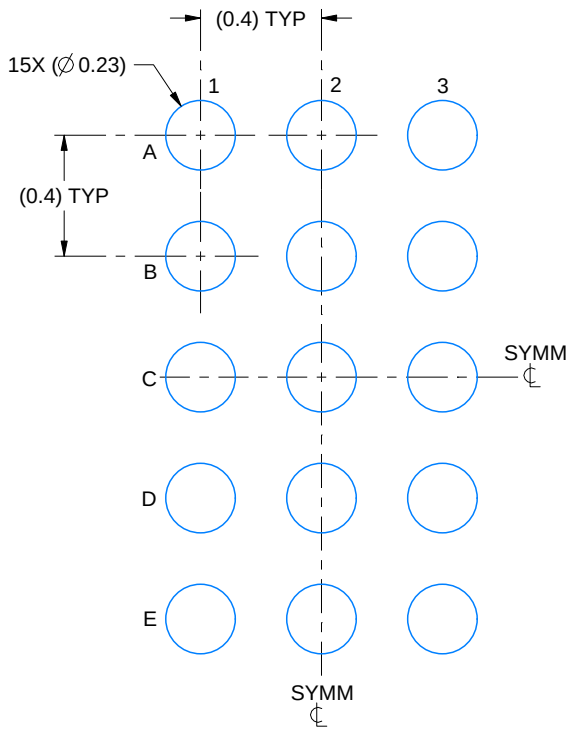
D: Max = 2.285 mm, Min =2.225 mm

E: Max = 1.374 mm, Min =1.314 mm

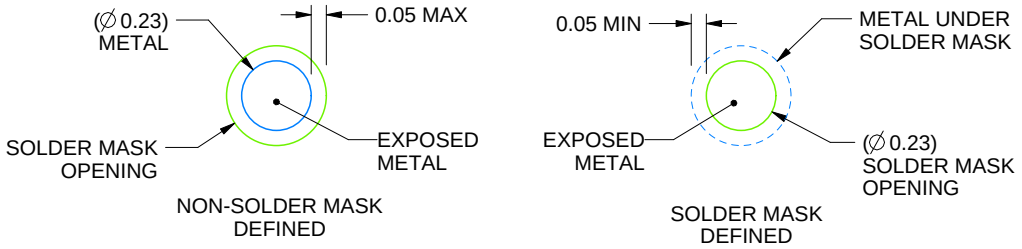
4219378/B 05/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X

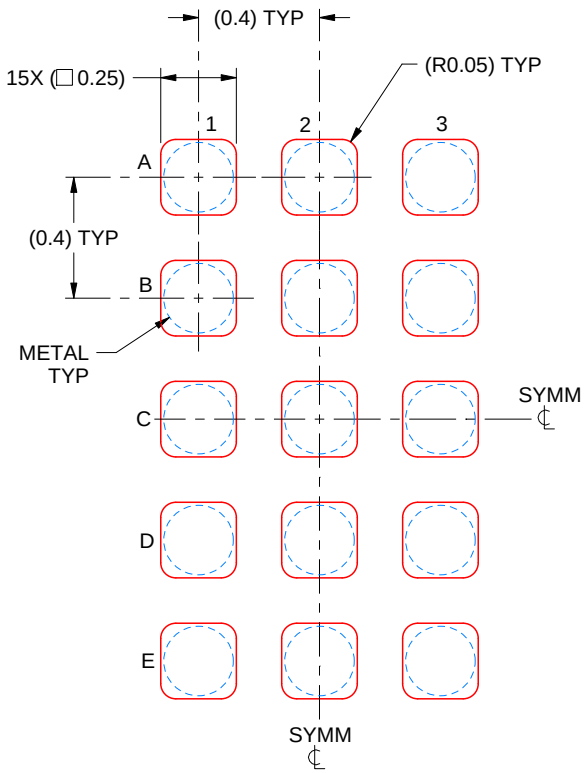


SOLDER MASK DETAILS
NOT TO SCALE

4219378/B 05/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219378/B 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

テキサス· インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス· インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス· インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス· インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス· インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス· インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス· インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス· インスツルメンツは一切の責任を拒否します。

テキサス· インスツルメンツの製品は、 テキサス· インスツルメンツの販売条件、または ti.com やかかる テキサス· インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス· インスツルメンツがこれらのリソースを提供することは、適用される テキサス· インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス· インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated