



TPS63710 低ノイズ同期整流、反転降圧コンバータ

1 特長

- 入力電圧範囲: 3.1V~14V
- 出力電流: 1A
- 最高91%の効率
- 出力電圧精度: $\pm 1.5\%$
- 同期整流
- 低1/fノイズのリファレンス・システム
- ノイズ: $22\mu V_{RMS}$ (10Hz~100kHz)
- 出力電圧: -1V~-5.5V
- $|V_{OUT}| < 0.7 \times V_{IN}$
- 1.5MHz固定周波数のPWMモード
- サーマル・シャットダウン
- シャットダウン電流 $5\mu A$
- 3mm×3mmのWSONパッケージ
- **WEBENCH® Power Designer**により、TPS63710を使用するカスタム設計を作成

2 アプリケーション

- 汎用の負電圧電源
- テレコム・システムのADCおよびDAC電源
- GaNトランジスタ用のバイアス
- 光学モジュールのレーザー・ダイオードのバイアス
- 負の電源電圧を必要とし、ノイズに敏感またはスペースが限られたアプリケーション

3 概要

TPS63710は反転降圧型のDC/DCコンバータであり、最低で-5.5Vまでの負の出力電圧を生成します。入力電圧と出力電圧の比率に応じて、最大1Aの出力電流を供給できます。フィルタ処理されるリファレンス電圧システムにより、高性能のテレコミュニケーション・システムで要求される低1/fノイズを実現します。

TPS63710は固定周波数のPWM制御トポロジで動作します。内部的な電流制限とサーマル・シャットダウンを備えています。TPS63710の入力電圧範囲は3.1V~14Vであり、絶対値が高い正の入力電圧から負の出力電圧を生成する各種アプリケーションに使用できます。

同期整流により、高性能DACおよびADCの負の電源電圧として一般的に使用される、-1.8Vなどの小さい出力電圧で特に高い効率が得られます。スイッチング周波数は1.5MHz固定で、小型の外付け部品を使用でき、ソリューション全体のサイズも小さくなります。

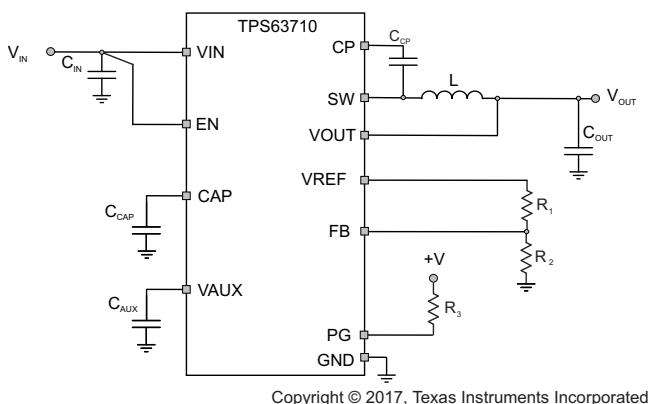
TPS63710は3mm×3mmのWSONパッケージで供給され、周囲温度が高い環境で実行されるアプリケーションにおいて、優れた熱性能を実現します。

製品情報⁽¹⁾

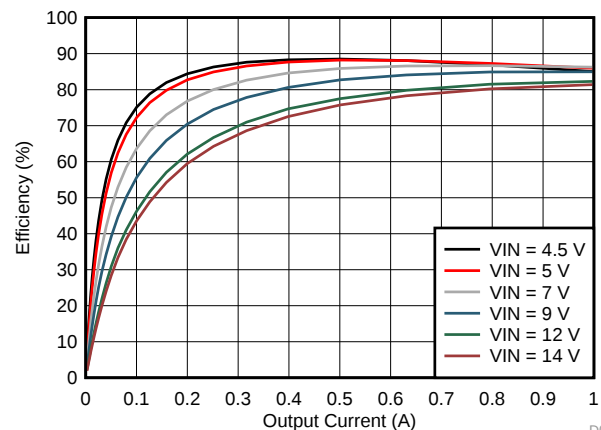
型番	パッケージ	本体サイズ(公称)
TPS63710	WSON	3mm×3mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

標準アプリケーション



$V_{OUT} = -1.8V$ 時の効率と出力電流との関係



D004



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4 改訂履歴

20179	Page
• 「特長」に「ノイズ: 22μV _{RMS} (10Hz~100kHz)」を追加.....	1
• Changed 図 31 to 図 34	18
• Added 図 35 and 図 36	19
• Changed 図 41	20

5 Pin Configuration and Functions

**DRR Package
12-Pin WSON
Top View**

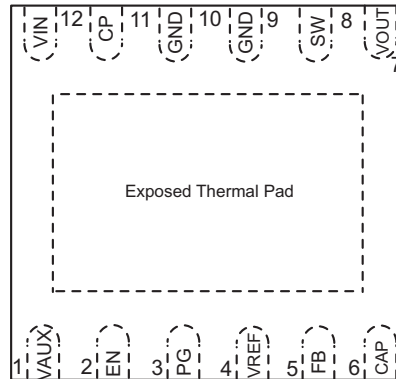


Table 1. Pin Functions

Pin		I/O	Description
Name	No.		
VIN	12	I	Power supply Input. Connect the input capacitor from this pin to GND and place it as close as possible to the device pins.
VAUX	1	O	Connect the output capacitor of the internal voltage regulator from this pin to GND. VAUX can be loaded externally with up to 100uA. Do not use this pin for any pulsed load to not couple noise into the internal supply.
GND	10, 9		Ground Connection. Voltages and signals are referenced to this pin.
CP	11	O	Connect a capacitor from this pin to SW.
SW	8	O	Connect a capacitor from this pin to CP and the inductor from this pin to the output.
FB	5	I	Feedback pin for the voltage divider.
VOUT	7	I	Output voltage sense pin.
CAP	6	O	Reference system bypass capacitor connection. Do not tie anything other than a capacitor to GND to this pin. Keep any noise sources away from this pin. The capacitor connected to this pin forms a low-pass filter with an internal filter resistor and also defines the soft-start time.
VREF	4	O	Reference voltage output. Connect a voltage divider between this pin, FB and GND to set the output voltage. Do not connect any other circuitry to this pin.
EN	2	I	Enable pin. The device is enabled when the pin is connected to a logic high level e.g. VIN. The device is disabled when the pin is connected to a logic low level. The logic levels are referenced to the IC's GND pin.
PG	3	O	Open drain power good output. Connect with a pull-up resistor to a positive voltage up to 5.5 V. If not used, leave open or connect to GND.
Exposed Thermal Pad	-	-	The thermal pad must be tied to GND. The pad must be soldered to a GND plane to achieve an appropriate thermal resistance and for mechanical reliability.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

	PIN	MIN	MAX	UNIT
Voltage ⁽²⁾	VIN, EN	-0.3	15	V
	CP (DC)	-0.5	15	V
	CP (AC, less than 10ns) ⁽³⁾	-3	17	V
	SW (DC)	-16	0.3	V
	SW (AC, less than 10ns) ⁽³⁾	-20	1	V
	VAUX, PG	-0.3	5.5	V
	FB	-3.6	0.3	V
	VOUT	-6	0.3	V
	VREF, CAP	-5.5	0.3	V
Sink Current	PG		5	mA
Operating junction temperature, T _J		-40	150	°C
Storage temperature, T _{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND pin.

(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply Voltage Range	3.1		14	V
	Supply voltage slew rate for a V_{IN} step of less than 1V	-1		1	V/ μ s
	Supply voltage slew rate for a V_{IN} step of greater or equal than 1V	-0.1		0.1	V/ μ s
I_{OUT}	Output Current	-1		0	A
L	Effective Inductance	1.5	2.2	6.2	μ H
C_{OUT}	Effective Output Capacitance ⁽¹⁾ for $T_j = -20^\circ\text{C}$ to 125°C	15	44	100	μ F
C_{OUT}	Effective Output Capacitance ⁽¹⁾ for $T_j = -40^\circ\text{C}$ to 125°C	22	44	100	μ F
C_{IN}	Effective Input Capacitance ⁽¹⁾	2 x C_{CP}			μ F
C_{CP}	Effective Capacitance on the CP pin required for full output current at $\leq 70\%$ duty cycle ⁽¹⁾ ⁽²⁾	4	4.7	20 ⁽³⁾	μ F
C_{AUX}	Effective Capacitance from VAUX pin to GND ⁽¹⁾	0.08	0.22	1	μ F
C_{CAP}	Effective Capacitance from CAP pin to GND ⁽¹⁾	0.01		10	μ F
R	Total resistance for R1 + R2 from VREF to GND	100		500	k Ω
T_j	Operating Junction Temperature	-40		125	$^\circ\text{C}$

- (1) The values given for all the capacitors are effective capacitance, which includes the dc bias effect. Especially the input capacitor C_{IN} and the C_{CP} capacitor, which are charged to the input voltage, are strongly effected. Their effective capacitance is much lower based on the dc voltage applied. Therefore, the nominal capacitor value needs to be larger than the minimum values given in the table. Please check the manufacturer's dc bias curves for the effective capacitance vs dc voltage applied.
- (2) If a maximum output current below 1A is required, the capacitance can be reduced accordingly. See the application section for details.
- (3) The maximum value also includes dc bias at the nominal operating voltage. During start-up when the voltage is 0 V, the effective capacitance can be higher. Please see the application section for details.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS63710	UNIT
		DRR (WSON)	
		12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.3	$^\circ\text{C/W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.7	$^\circ\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	18.9	$^\circ\text{C/W}$
ψ_{JT}	Junction-to-top characterization parameter	0.4	$^\circ\text{C/W}$
ψ_{JB}	Junction-to-board characterization parameter	19.1	$^\circ\text{C/W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	$^\circ\text{C/W}$

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to 125°C , over recommended input voltage range. Typical values are at $V_{IN} = 5\text{ V}$ and $T_J = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{(Q)}$	Quiescent supply current	$I_{OUT} = 0\text{mA}$, EN = high		15		mA
I_{SD}	Shutdown supply current	EN = low, $T_J = -40^{\circ}\text{C}$ to 85°C ⁽¹⁾		5	25	μA
I_{SD}	Shutdown supply current	EN = low, $T_J = -40^{\circ}\text{C}$ to 125°C ⁽¹⁾			55	μA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling, detected at VAUX	2.55	2.6	2.7	V
	Undervoltage lockout hysteresis	V_{IN} rising, detected at VAUX	250		350	mV
T_{SD}	Thermal shutdown temperature	Junction temperature rising		160		$^{\circ}\text{C}$
	Thermal shutdown hysteresis	Junction temperature falling		20		$^{\circ}\text{C}$
CONTROL (EN, PG)						
V_{IH}	High level input voltage for EN		1		14	V
V_{IL}	Low level input voltage for EN				0.4	V
I_{IN}	Input current for EN	EN = high		0.01	0.1	μA
R_{IN}	Input resistance for EN	EN = low		400		k Ω
	PG de-glitch time	rising or falling		10		μs
V_{OL_PG}	PG output low voltage	$I_{PG} = 1\text{ mA}$		0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	$V_{PG} = 5\text{ V}$			100	nA
V_{VAUX}	Voltage at VAUX	$V_{IN} \geq 5\text{ V}$, $I_{VAUX} = 100\text{ }\mu\text{A}$		4.6		V
I_{VAUX}	Current drawn from VAUX		0		100	μA
POWER SWITCH						
I_{LIM}	Switch current limit (LSD)	$4\text{ V} \leq V_{IN} < 14\text{ V}$, duty cycle $\leq 70\%$	1.4	2.1	3	A
I_{LIM}	Switch current limit (LSD)	$3.1\text{ V} < V_{IN} < 4\text{ V}$, duty cycle $\leq 70\%$	0.8			A
$R_{DS(ON)}$	Switch on-resistance	HSD switch, $V_{IN} \geq 5\text{ V}$		80	130	m Ω
		LSD switch, $V_{IN} \geq 5\text{ V}$		120	190	
		RECT switch, $V_{IN} \geq 5\text{ V}$		40	80	
D_{MAX}	Maximum duty cycle	at SW pin		70%		
$t_{on,min}$	Minimum on-time			130		ns
f_S	Switching frequency		1400	1500	1600	kHz
OUTPUT						
V_{OUT}	Output voltage range	$ V_{OUT} < 0.7 \times V_{IN}$	-5.5		-1	V
V_{FB}	FB regulation voltage			-0.7 ⁽²⁾		V
	Output voltage tolerance ⁽³⁾	for $V_{OUT} \leq -1.8\text{ V}$	-1.5%		1.5%	
	Output voltage tolerance ⁽³⁾	for $-1.8\text{ V} < V_{OUT} \leq -1\text{ V}$	-2%		1.5%	
I_{FB}	Feedback input bias current	$V_{FB} = -0.7\text{ V}$		2	100	nA
R_{DIS}	Discharge resistance from pin VOUT to GND	EN = low		100		Ω
	Line regulation			0.05		%/A
	Load regulation			0.02		%/V
t_{delay}	Start-up delay time from EN = high to start switching	with $C_{CP} = 10\text{ }\mu\text{F}$		5		ms
t_{ramp}	Ramp time from start switching until device has reached 95% of its nominal output voltage	$C_{CAP} = 47\text{ nF}$, $V_{OUT} = -1.8\text{ V}$, device not in current limit during start-up		1		ms
I_{ramp}	Soft-start current into C_{CAP}		55	100	145	μA

(1) This specification applies after there has been a high to low transition on EN. If EN is low while the supply voltage is applied, the shutdown current can be up to 90 μA .

(2) Please see the application section for how to set the output voltage.

(3) Tolerance of V_{FB} voltage and error of gain stage - see also "Low Noise Reference System"

6.6 Typical Characteristics

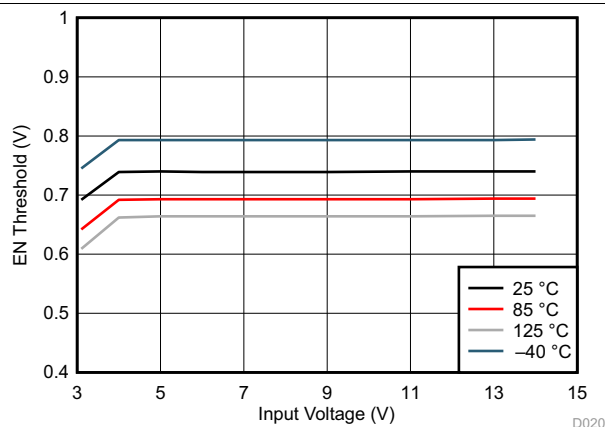


图 2. EN Threshold, rising V_{IN}

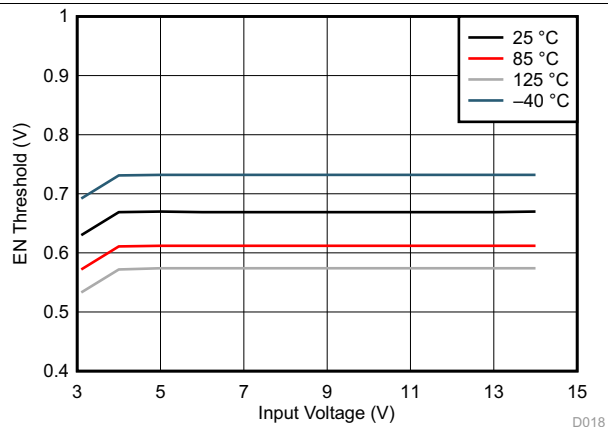


图 3. EN Threshold, falling V_{IN}

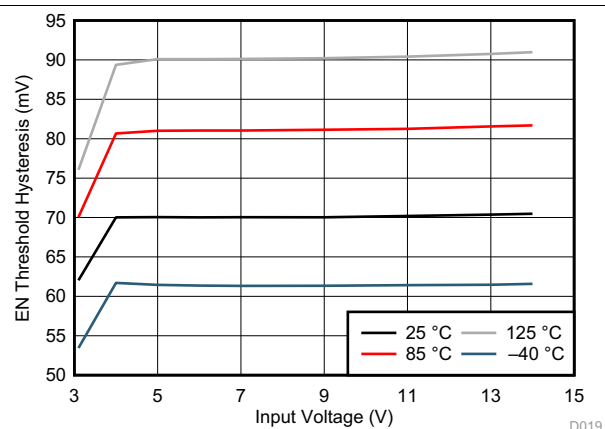


图 4. EN Threshold Hysteresis

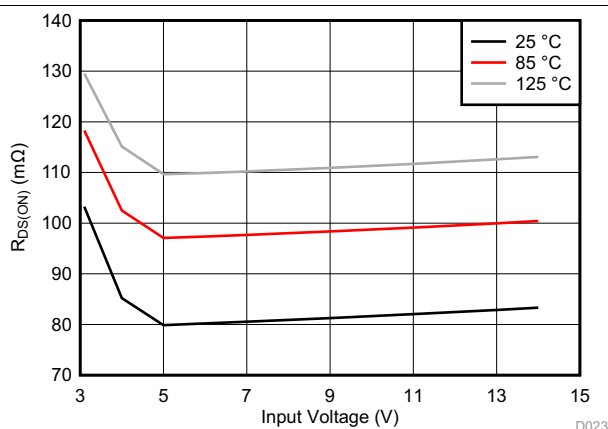


图 5. Resistance of HSD

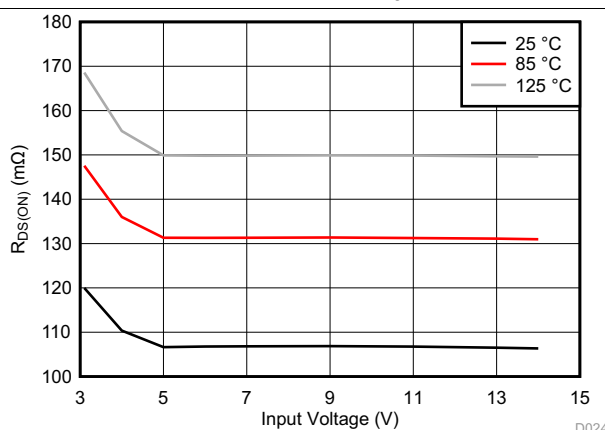


图 6. Resistance of LSD

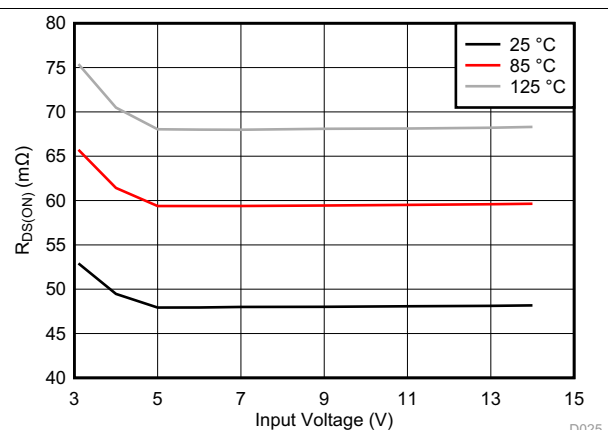


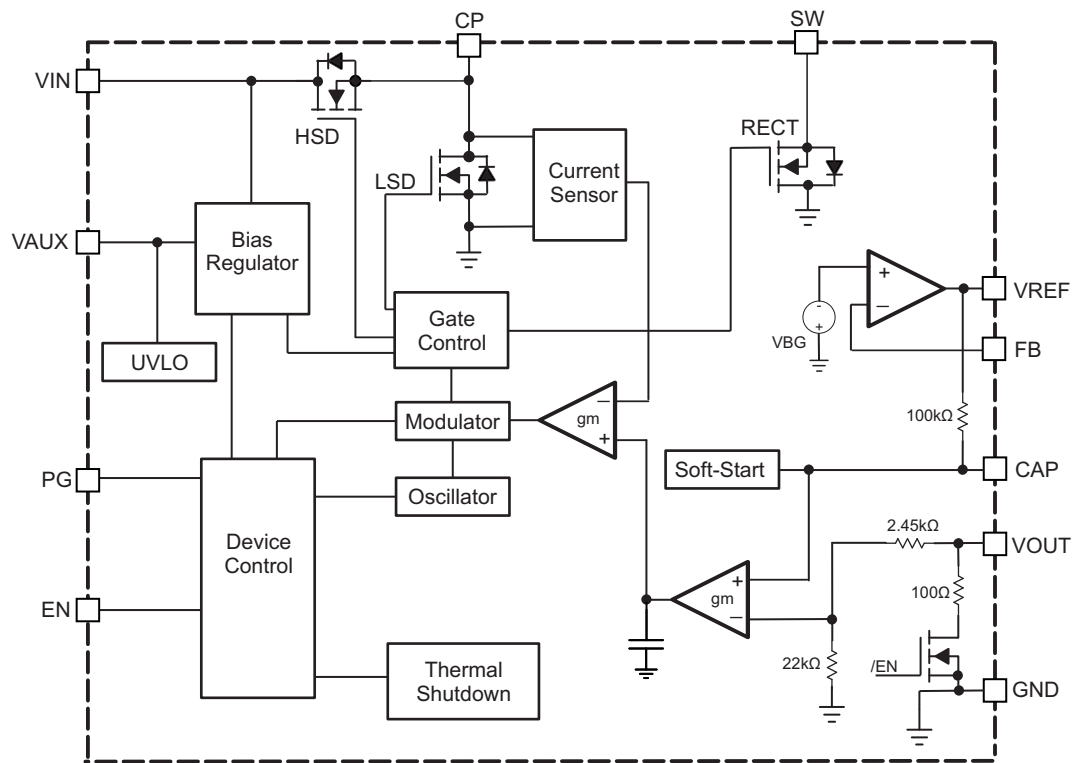
图 7. Resistance of RECT

7 Detailed Description

7.1 Overview

The TPS63710 is a dc-dc converter that generates a negative output voltage using an inverting buck topology. It operates with an input voltage range of 3.1 V to 14 V and generates a negative output voltage down to -5.5 V. As it is based on a step-down topology, the input voltage needs to be larger than the negative voltage, in absolute value, that is generated. The output is controlled by a fixed-frequency, pulse-width-modulated (PWM) regulator. As there is an inductor in the output path, similar to a step-down converter, the output current is continuous and the output voltage ripple is low. This makes this topology a perfect solution for noise sensitive applications.

7.2 Functional Block Diagram



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图 8. Block Diagram

7.3 Feature Description

7.3.1 Low Noise Reference System

The reference system in the TPS63710 uses an external filter capacitor on the CAP pin. This reduces the low-frequency (1/f) noise in a range from a lower limit up to around 100kHz. The lower limit is defined by the corner frequency of the RC filter from the internal 100-kΩ resistor and an external capacitor on the CAP pin. The corner frequency is defined by [Equation 1](#).

$$f_c = \frac{1}{2\pi \times R \times C} = \frac{1}{2\pi \times 100k\Omega \times C_{CAP}} \quad (1)$$

In order to minimize the noise on the output voltage, the TPS63710 uses an architecture where the output voltage setting is done by changing the reference voltage which then is filtered. The gain stage therefore does not have to have a large gain in order to not increase the noise level. VBG is the internal bandgap reference voltage, optimized for low noise. Its output voltage is amplified and inverted and then filtered. The voltage on the CAP pin is the reference for the gain stage. The connection from CAP to the external capacitor should be as short as possible and be kept away from noisy traces. The gain stage has a small gain of 1/0.9. The voltage at VREF is negative and lower than the output voltage by the gain factor of the gain stage. Please also see [Setting the Output Voltage](#). [Figure 9](#) shows the low noise architecture.

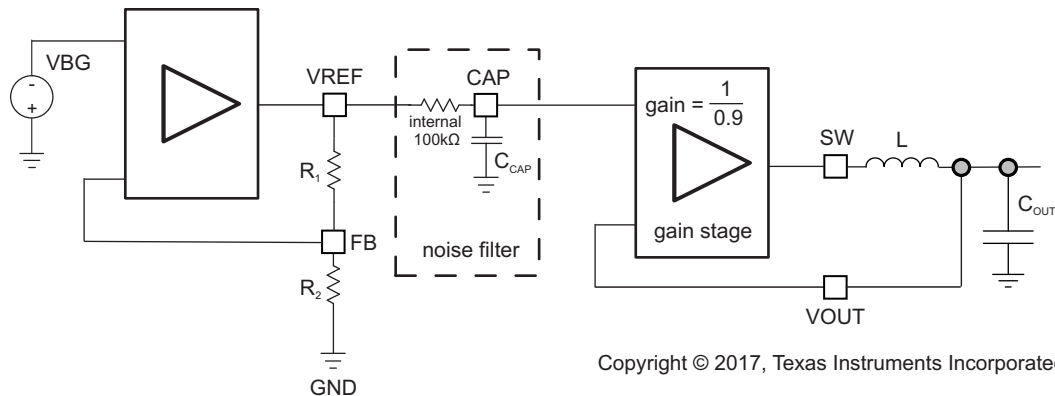


Figure 9. Low Noise Architecture

7.3.2 Duty Cycle

The duty cycle referred to in this data sheet is the duty cycle at the SW pin. By definition, from the PWM operation, the CP pin has the inverse duty cycle of 1-D. As a first approximation, the duty cycle is defined as $|V_{OUT}| / V_{IN}$. However, the actual duty cycle is larger, due to losses, and must remain below 70% for a robust design.

7.3.3 Enable

The device is enabled when the EN pin is set to high. With EN set to low, the device shuts down. After EN is set high, the capacitor C_{CP} (from CP to SW) is pre-charged with about 50mA. After the start-up delay time t_{delay} , the device starts switching and ramps the output voltage to its target value. See [Soft-Start](#).

The EN pin must be set externally to high or low. An internal pull-down resistor of about 400 kΩ is connected and keeps EN low, if a low is detected internally and afterwards the pin is floating. When a high level is detected, the internal resistor is disconnected. The logic levels are referenced to the IC's GND pin.

7.3.4 Undervoltage Lockout

An undervoltage lockout circuit prevents the device from starting up and operating, if the supply voltage is too low. The device automatically shuts down the converter when the V_{AUX} voltage falls below the V_{UVLO} threshold. There is hysteresis to prevent oscillation with high impedance supply voltage sources. Once the threshold plus hysteresis is exceeded, the device enters soft-start. Undervoltage lockout is sensed on the V_{AUX} voltage, as this is the internal supply for the control loop and logic.

Feature Description (continued)

When V_{IN} ramps down to a voltage too low to maintain the desired output voltage, the absolute value of the output voltage drops and the power good output goes low. When the output voltage level reaches the voltage on C_{CAP} , at about 90% of the target output voltage, the device shuts down and initiates a re-start cycle. The TPS63710 then stays in the start-up state, until the input voltage is high enough to reach the desired output voltage.

7.3.5 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds the thermal shutdown temperature T_{SD} , the device turns off the internal power FETs, discharges the output capacitor and the power good output goes low. It starts operation again when the junction temperature has decreased by the thermal shutdown hysteresis.

7.3.6 Power Good Output

The TPS63710 has a built-in power good (PG) output to indicate whether or not the output voltage is in regulation. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor to any positive voltage up to 5.5 V. It can sink 1 mA of current and maintain its specified logic low level. PG is low when the device is turned off due to $EN = \text{low}$, undervoltage lockout, or thermal shutdown. There is a typical de-glitch time of 10 μs on the power good output. The minimum V_{IN} to drive the PG pin properly is typically 2 V. If not used, the PG pin may be left floating or connected to GND.

V_{AUX} may be used to pull-up the PG pin, but the pull-up resistor must be chosen such that the maximum load of 100 μA on V_{AUX} is not exceeded.

During start-up, the power good signal is gated by the soft-start circuit such that the output is held low as long as the soft-start is ongoing.

表 2. Power Good Pin Logic Table

EN	device status	PG state
X	$V_{IN} < 2 \text{ V}$	high impedance
low	$V_{IN} \geq 2 \text{ V}$	low
high	$2 \text{ V} \leq V_{IN} < \text{UVLO}$ OR in thermal shutdown OR V_{OUT} not in regulation	low
high	V_{OUT} in regulation	high impedance

7.4 Device Functional Modes

7.4.1 Soft-Start

The discharge circuit keeps the output voltage at 0 V when the TPS63710 is disabled. The TPS63710 only begins the start-up cycle when the output voltage is between +300 mV to -300 mV to ensure a proper start-up. When the output voltage is not in this range, the device keeps the discharge switch on and waits until the voltage is within the window.

When the device is enabled, the internal reference is powered up. After the startup delay time when the C_{CP} capacitor is pre-charged, the device enters soft-start, starts switching and ramps down the output voltage. Soft-start is achieved by ramping the reference voltage, hence the output voltage, to its nominal value. This ramp time is defined by an external capacitor connected to the CAP pin. The capacitor is charged with typically 100 μA by an internal current source. The ramp time is defined in [Equation 2](#).

$$t_{\text{ramp}} = \frac{C_{\text{CAP}} \times V_{\text{REF}}}{I_{\text{ramp}}} = \frac{C_{\text{CAP}} \times 0.9 \times V_{\text{OUT}}}{I_{\text{ramp}}} \quad (2)$$

7.4.2 VOUT Discharge

The V_{OUT} pin has a discharge circuit to connect the output to GND, once the device is disabled. This feature prevents residual voltages on the output capacitor. The discharge circuit becomes active when V_{IN} drops below V_{UVLO} , $EN = \text{low}$, or thermal shutdown occurs. The minimum supply voltage required to drive the discharge switch is typically 2 V.

Device Functional Modes (continued)

7.4.3 Current Limit

A current limit protects the device against short circuits at the output. The current limit is scaled down from its nominal value for input voltages below 4 V. The current limit monitors the peak current in the LSD during the ON-time. If this current is reached during the ON-time, the LSD is turned off and the HSD and RECT turned on to decrease the current. The next ON-time begins at the next switching cycle.

A short circuit from VIN to GND during operation should be avoided as this leads to a high current discharging the C_{CP} capacitor through the back-gate diode of the high side switch to GND. When there is an overload on the output and the output voltage drops below 0.9 times the target output voltage, the device re-starts.

7.4.4 C_{CP} Capacitor Precharge

The C_{CP} capacitor is pre-charged during the start-up delay phase by a current that increases up to 50 mA based on the voltage of V_{IN} - V_{CP}. When the voltage on C_{CP} reaches approximately the V_{IN} level, the device starts switching.

7.4.5 PWM Operation

The converter operates with a fixed-frequency, pulse-width-modulated control. In the OFF-time, the rectifier switch (RECT) and the high-side switch (HSD) are turned on to charge C_{CP} to the input voltage. As well, the inductor current ramps down, continuing to charge the output capacitor. During the ON-time, the low-side switch (LSD) is closed and HSD and RECT are opened. C_{CP} inverts the supply voltage onto SW, and the inductor current is ramped up. The LC output filter filters the SW voltage, just like in a step-down converter. Charging the C_{CP} capacitor during the OFF-time limits the maximum duty cycle. The upper limit of the duty cycle is 70% to allow charging the C_{CP} capacitor in the remaining 30%.

Lower negative voltages require higher positive supply voltages. For an output voltage of -1.8 V, a minimum input voltage of 4.5 V is sufficient while for an output voltage of -3.3 V, the input voltage has to be above 6 V. See [Figure 37](#) to [Figure 39](#) for the relation of input voltage, output voltage and temperature vs output current.

For high input voltages and, in absolute value, small output voltages, the device operates with its minimum on-time (t_{on,min}) to generate the duty cycle required for this V_{IN} and V_{OUT} ratio. This means that, for such cases, the switching frequency is lower than f_S.

8 Application and Implementation

注

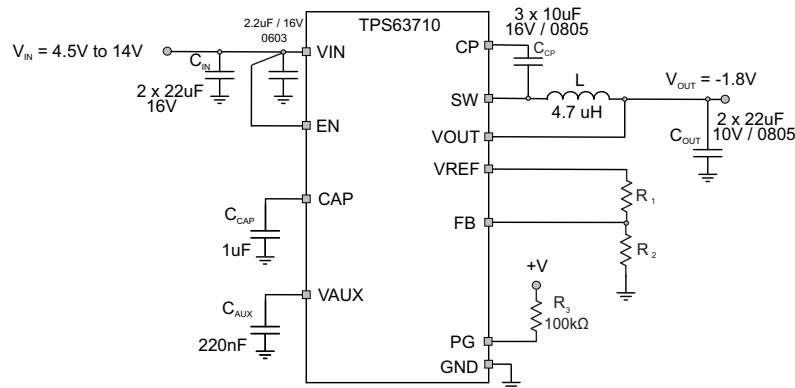
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS63710 is intended for systems typically powered by a pre-regulated power supply but can also run on a battery with a supply voltage range between 3.1 V and 14 V.

8.2 Typical Application

The application covers the input voltage range from 4.5 V to 14 V at the full 1-A output current. The output capacitors are designed for an output voltage of -1.8 V. With output voltages below -1.8 V (larger negative voltages), the output capacitance has to be increased as described in the [Detailed Design Procedure](#). The minimum supply voltage is defined by the 70% duty cycle limit, output current and the output voltage. Please see [Figure 37](#) to [Figure 39](#) for the recommended input voltage levels to generate a specific output voltage.



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Figure 10. Typical Application for an Input Voltage up to 14V

8.2.1 Design Requirements

The design of the inverter can be adapted to different output voltages and load currents. The following components cover an input voltage range up to 9 V. For C_{IN} , a 0603 capacitor close to the device pins is required in addition to the larger capacitor. As the C_{CP} capacitor has the same voltage across it, its dc bias effect is similar to C_{IN} . [Table 3](#) gives examples for the schematics optimized for different input and output voltage ranges.

Table 3. Bill of Materials

Reference	Part Number	Value	Manufacturer ⁽¹⁾
IC	TPS63710DRR		Texas Instruments
C_{IN}	EMK107BB7225KA-T EMK316BB7226ML-T	2.2 µF / 16 V + 2 x 22 µF / 16 V	Taiyo Yuden
C_{CP}	EMK212BB7106MG-T	3 x 10 µF / 16V	Taiyo Yuden
C_{OUT}	C2012X7S1A226M125AC	2 x 22 µF / 10 V	TDK
L	XFL4020-222	2.2 µH	Coilcraft
C_{CAP}	885012206026	1 µF / 10 V	Würth
C_{AUX}	885012206022	220 nF / 10 V	Würth
R_1		196 kΩ	

(1) See [Third-party Products Disclaimer](#)

Typical Application (continued)

表 3. Bill of Materials (continued)

Reference	Part Number	Value	Manufacturer ⁽¹⁾
R ₂		150 kΩ	
R ₃		100 kΩ	

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS63710 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting the Output Voltage

The output voltage of the TPS63710 converter is adjusted with an external resistor divider connected to the FB pin. The voltage at the feedback pin is negative and is regulated to -0.7 V. The gain stage adds a gain factor of 1/0.9 such that the output voltage is -0.778 V for -0.7 V of FB voltage. See [Low Noise Reference System](#) for details.

The value of the output voltage is set by the selection of the resistive divider using [Equation 3](#) and V_{FB_SET} = -0.778 V. Both V_{OUT} and V_{FB_SET} are negative, so the ratio is positive again.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB_SET}} - 1 \right) \quad (3)$$

It is recommended to choose resistor values such that R₁ + R₂ are in a range from 100 kΩ to 500 kΩ. For example, if an output voltage of -1.8 V is needed and a resistor of 150-kΩ has been chosen for R₂, a 196-kΩ resistor on R₁ is required to program the desired output voltage.

表 4. Recommended Resistor Values

Output Voltage	R ₁	R ₂
-1 V	51.1 kΩ	180 kΩ
-1.8 V	196 kΩ	150 kΩ
-2.5 V	287 kΩ	130 kΩ
-5 V	130 kΩ	24 kΩ

For proper regulation, the minimum input voltage should remain at least above the output voltage, per [Equation 4](#):

$$V_{IN} \geq \frac{1}{0.7} \times |V_{OUT}| \quad (4)$$

See [Figure 37](#) to [Figure 39](#) for the recommended input voltage levels to generate a specific output voltage.

8.2.2.3 Inductor Selection

The basic parameters for choosing an appropriate inductor is saturation current, as well as the dc resistance of the inductor. The TPS63710 is designed such that it operates with an inductance as given in the recommended operating conditions. For best performance, a nominal inductance of 2.2 μH should be used for input voltages below 9 V. For input voltages above 9 V, a nominal inductance of 4.7 μH is preferred to keep the inductor current ripple at a reasonable level.

Similar to a step-down converter, the inductor along with the output capacitor forms a LC filter. For noise-sensitive applications, larger values for the inductance and output capacitance are preferred to get the noise level at the output to very low values.

The peak inductor current depends on the output load, the input voltage V_{IN} , and the output voltage V_{OUT} . The average inductor current equals the load current.

The topology can be simplified to an inverter stage followed by a step-down converter. The equations for calculating the inductor current of a step-down converter therefore also apply. The worst case inductor ripple current occurs at 50% duty cycle which is when $V_{\text{IN}} = 2 \times |V_{\text{OUT}}|$. The voltage across the inductor is $V_{\text{IN}} - |V_{\text{OUT}}|$, which is $0.5 \times V_{\text{IN}}$ at 50% duty cycle. With this, Equation 5 and $dt = 0.5 \times 1/f_s$, the peak to peak inductor ripple current is defined by Equation 6. The inductor's saturation current must remain above its peak current which is calculated in Equation 7. 表 5 shows a list of recommended inductors.

$$V = L \times \frac{dI}{dt} \quad (5)$$

$$\Delta I_{pp} = \frac{V_{\text{IN}} \times 0.5}{L} \times \frac{1}{f_s} \times 0.5 = \frac{|V_{\text{OUT}}|}{L} \times \frac{1}{f_s} \times 0.5 \quad (6)$$

$$I_{L_{\text{peak}}} = I_{\text{OUT}} + \frac{1}{2} \Delta I_{pp} \quad (7)$$

表 5. List of Inductors

Input Voltage	Vendor	comment	Suggested Inductor ⁽¹⁾
3.1 V to 9 V	Coilcraft		XFL3012-222ME
3.1 V to 9 V	Coilcraft	best performance for low input voltage	XFL4020-222ME
3.1 V to 9 V	Toko	low cost; small size	DFE252012F-2R2M
3.1 V to 14 V	Coilcraft		XFL4020-472ME
3.1 V to 14 V	Würth		744 383 570 47

(1) See [Third-party Products Disclaimer](#)

8.2.2.4 Capacitor Selection

8.2.2.4.1 C_{CP} Capacitor

The capacitance of C_{CP} determines the maximum output current of TPS63710. Therefore it is selected at first. A minimum 4- μF of effective capacitance is required to support the full output current of 1 A. Only ceramic capacitors like X7R, X5R or equivalent are recommended. For applications that require a lower maximum output current, its value can be reduced linearly. As the voltage at the C_{CP} capacitor is equal to the input voltage V_{IN} , the dc bias effect has to be taken into account based on the maximum input voltage. 表 6 shows recommended C_{CP} capacitors.

表 6. C_{CP} Capacitor Selection

input voltage range; V_{IN}	nominal value	voltage rating	package size	number of capacitors required for 1A of output current based on dc bias effect	Suggested Capacitors ⁽¹⁾
3.1 V to 6 V	10 μF	$> V_{\text{IN}}$	0805	2	EMK212BB7106MG-T
3.1 V to 14 V	10 μF	$> V_{\text{IN}}$	0805	3	EMK212BB7106MG-T

(1) See [Third-party Products Disclaimer](#)

8.2.2.4.2 Input Capacitor

The capacitance of the input capacitor should be at least twice the capacitance of C_{CP} . At least a 22- μ F ceramic input capacitor is recommended for a good transient behavior of the regulator and EMI behavior of the total power supply circuit. The capacitor must be located as close to the VIN and GND pins as possible. Only ceramic capacitors like X7R, X5R or equivalent are recommended. A 0603 size 2.2- μ F ceramic capacitor in parallel to the main input capacitor is recommended to reduce high frequency noise. The input capacitance can be increased without limit. 表 7 shows recommended capacitors.

表 7. Input Capacitor Selection

input voltage range; V_{IN}	nominal value	voltage rating	package size	number of capacitors required for 1A of output current based on dc bias effect	Suggested Capacitors ⁽¹⁾
3.1 V to 6 V	2 x capacitance of C_{CP}	$> V_{IN}$	1206	2	EMK316BB7226ML-T
3.1 V to 14 V	2 x capacitance of C_{CP}	$> V_{IN}$	1206	3	EMK316BB7226ML-T

(1) See [Third-party Products Disclaimer](#)

8.2.2.4.3 Output Capacitor

One of the major parameters necessary to define the capacitance value of the output capacitor is the maximum allowed output voltage ripple of the converter and device stability. Internal device compensation defines the limits for the capacitance on the output. Only ceramic capacitors like X7R, X5R or equivalent are recommended. Table 表 8 gives the minimum amount of capacitors required for a given output voltage based on the dc bias effect. For lowest output voltage ripple, more capacitance can be added up to the maximum value as defined in the recommended operating conditions.

表 8. Output Capacitor Selection

output voltage range; V_{OUT}	nominal value	voltage rating	package size	number of capacitors required based on dc bias effect	Suggested Capacitors ⁽¹⁾
-1 V to -3.3 V	22 μ F	≥ 6.3 V	0805	2	C2012X7S1A226M125AC
- 1 V to -5.5 V	22 μ F	≥ 10 V	0805	3	C2012X7S1A226M125AC

(1) See [Third-party Products Disclaimer](#)

8.2.3 Application Curves

8.2.3.1 Parameter Measurement Information

The application curves have been taken using the schematic in 图 10 and BOM according 表 3. Based on the output voltage, the components given in 表 9 have been changed. The resistor divider is based on 表 4.

表 9. Component Selection for V_{OUT} Options

V_{OUT}	C_{CP}	L	C_{OUT}
-1 V and -1.8 V	2 x EMK212BB7106MG-T	XFL4020-222ME	2 x C2012X7S1A226M125AC
-3.3 V and -5 V	3 x EMK212BB7106MG-T	XFL4020-472ME	3 x C2012X7S1A226M125AC

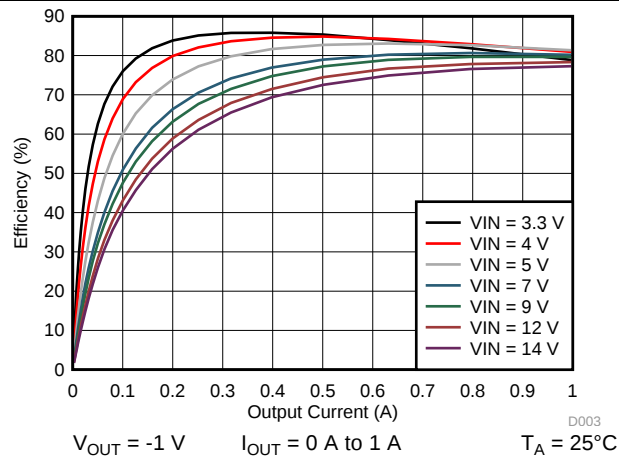


图 11. Efficiency vs Output Current

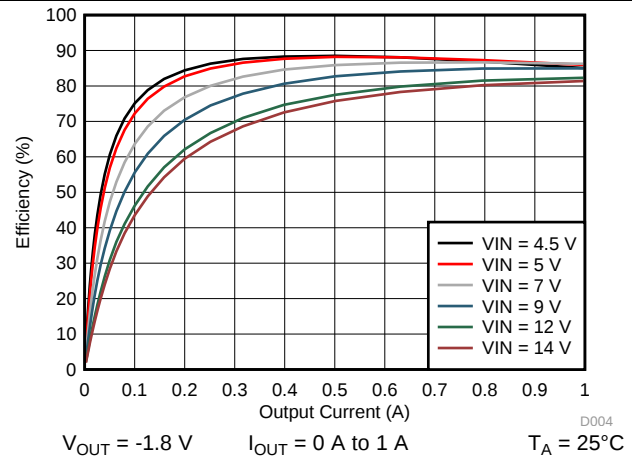


图 12. Efficiency vs Output Current

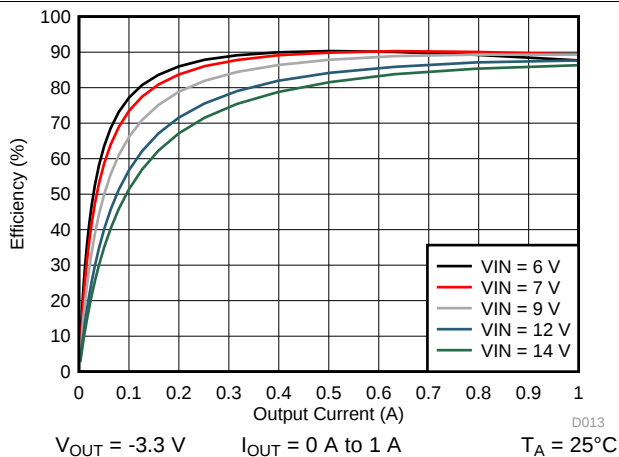


图 13. Efficiency vs Output Current

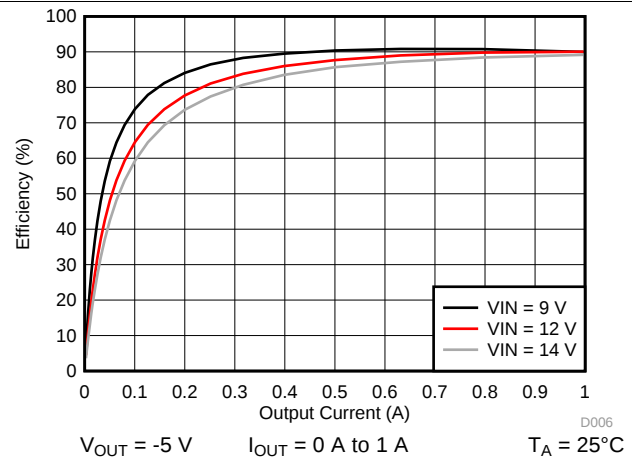


图 14. Efficiency vs Output Current

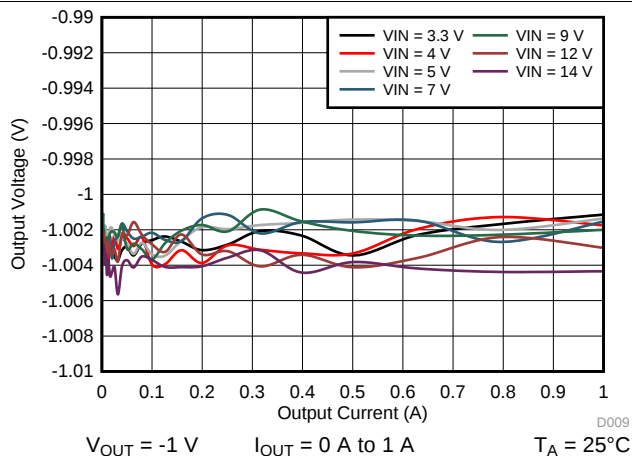


图 15. Output Voltage vs Output Current

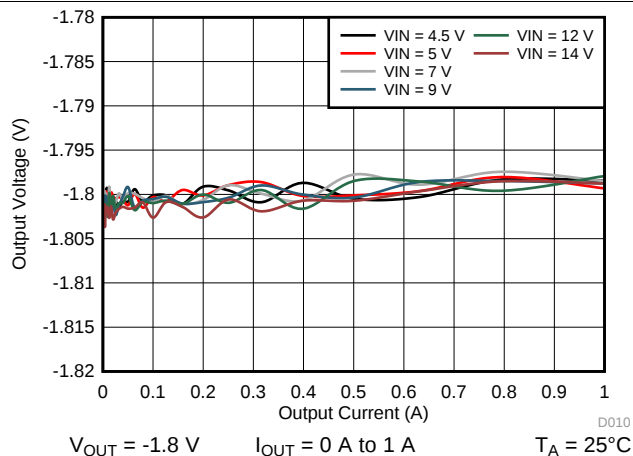


图 16. Output Voltage vs Output Current

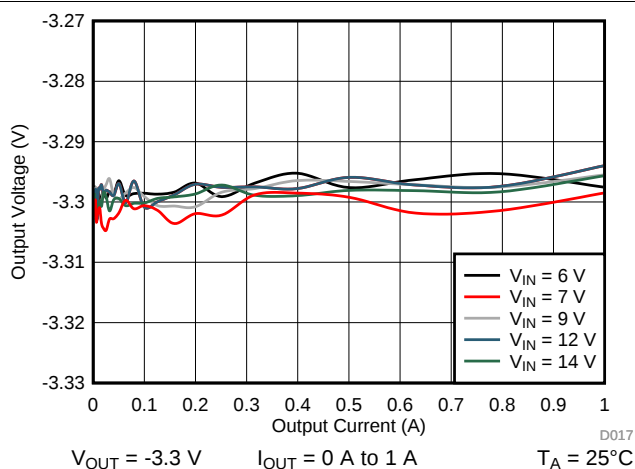


图 17. Output Voltage vs Output Current

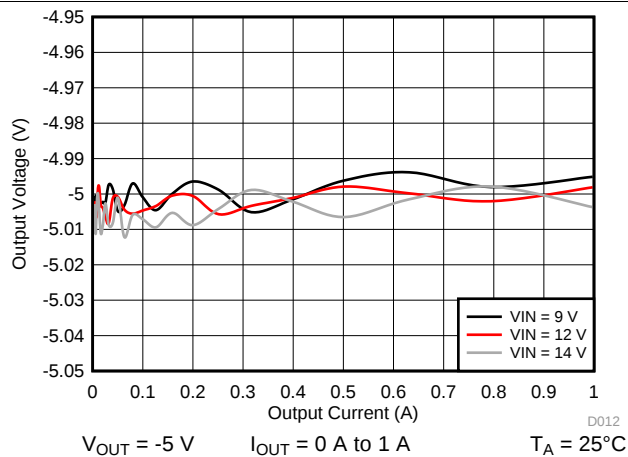


图 18. Output Voltage vs Output Current

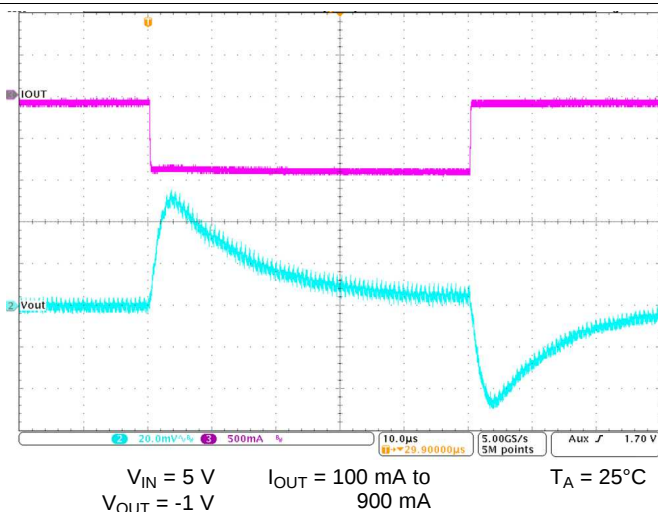


图 19. Load Transient Response

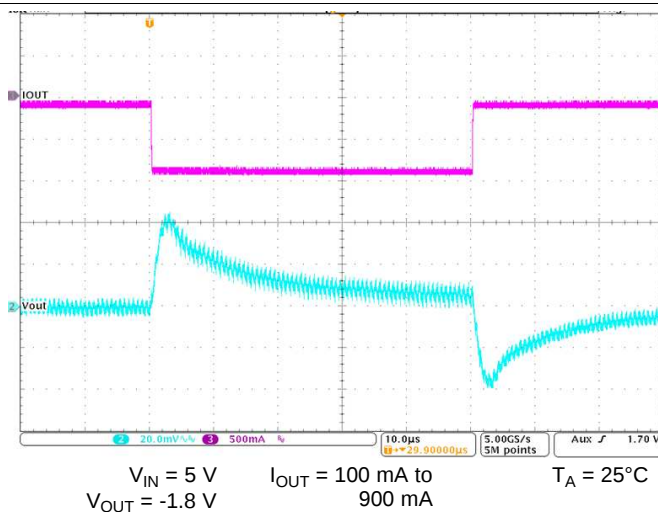


图 20. Load Transient Response

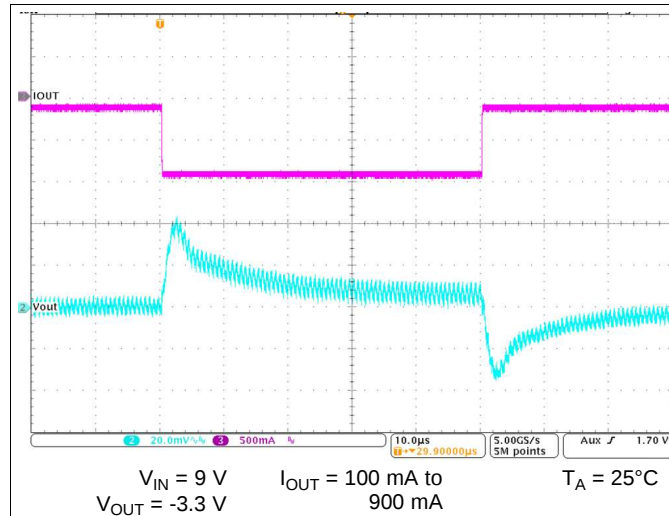


图 21. Load Transient Response

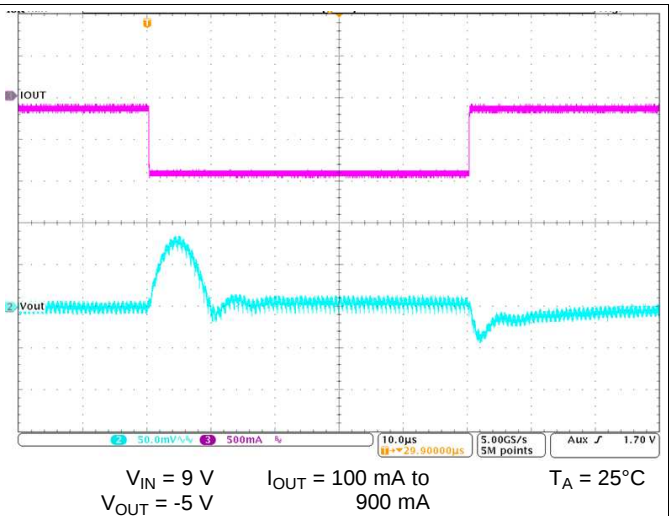


图 22. Load Transient Response

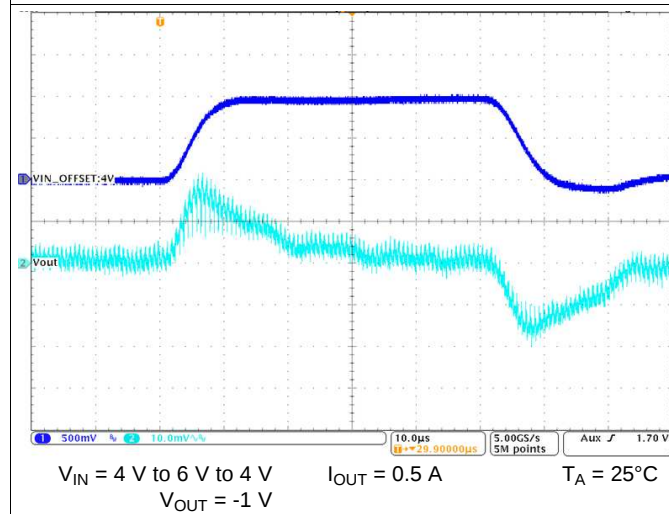


图 23. Line Transient Response

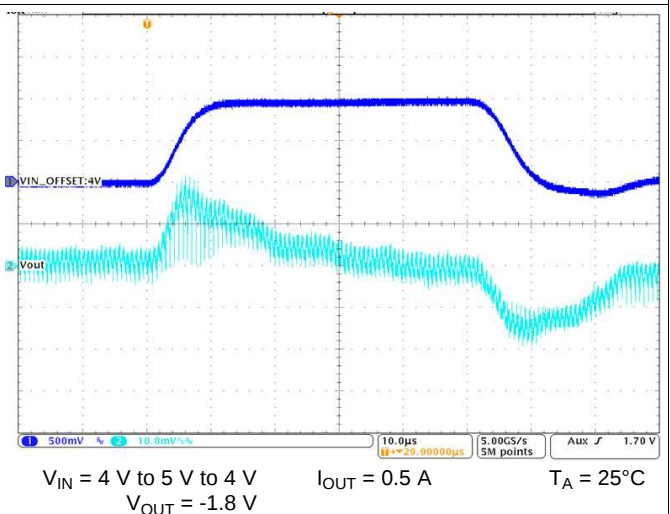


图 24. Line Transient Response

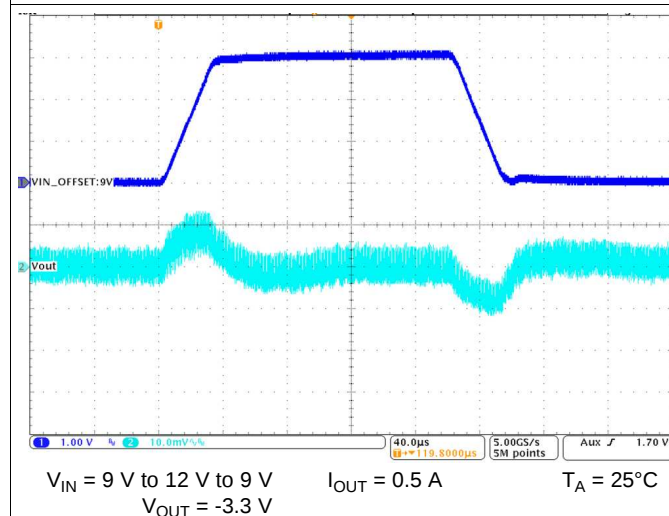


图 25. Line Transient Response

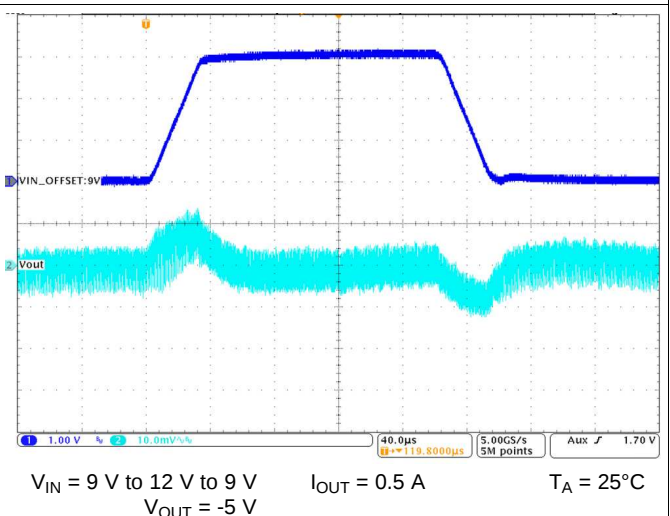


图 26. Line Transient Response

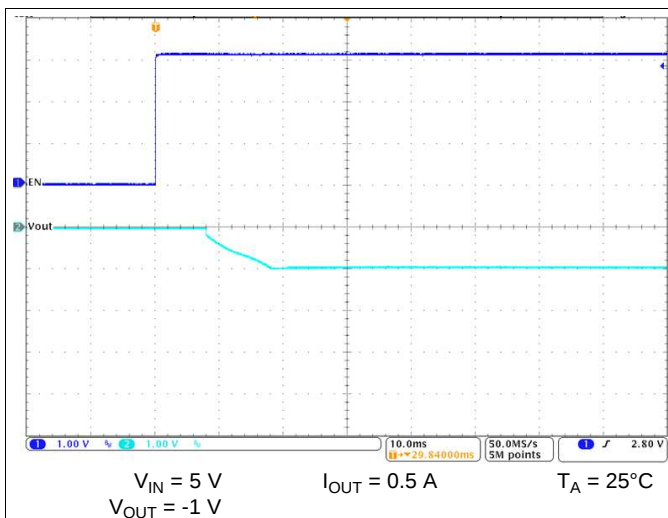


图 27. Start-Up Timing

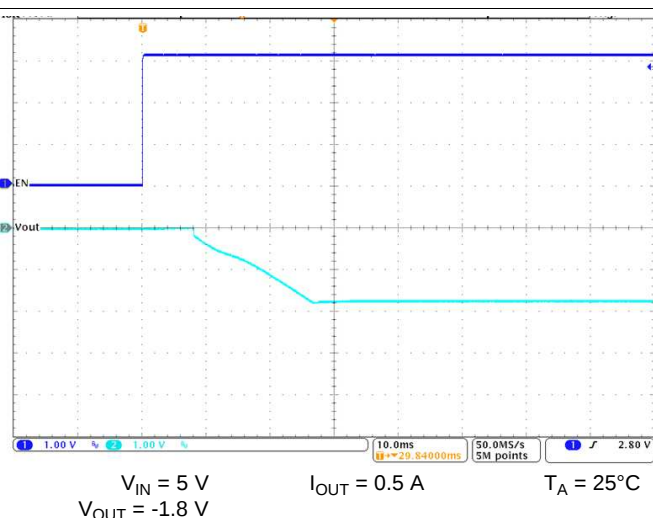


图 28. Start-Up Timing

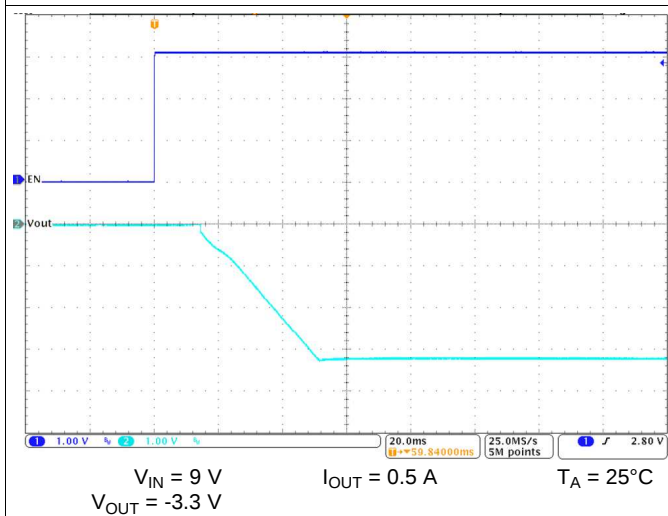


图 29. Start-Up Timing

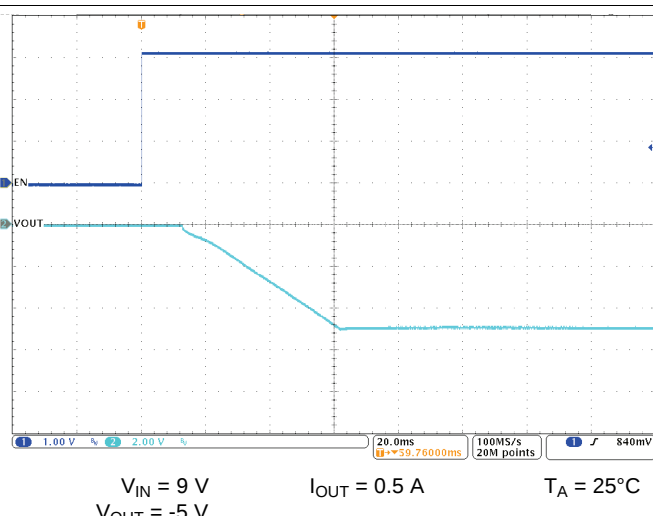


图 30. Start-Up Timing

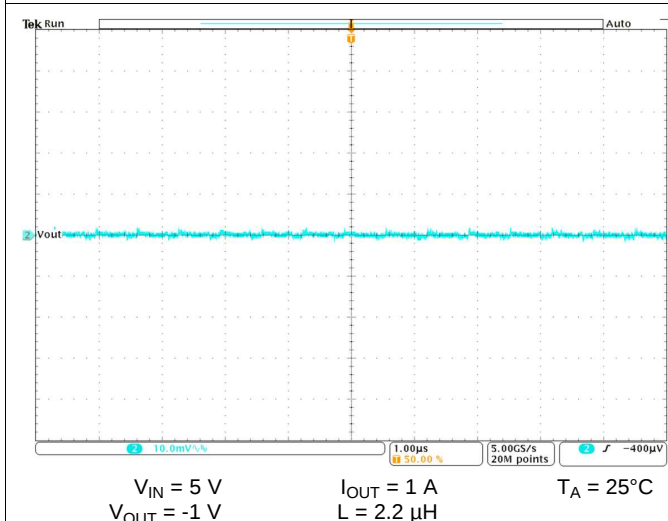


图 31. Output Voltage Ripple

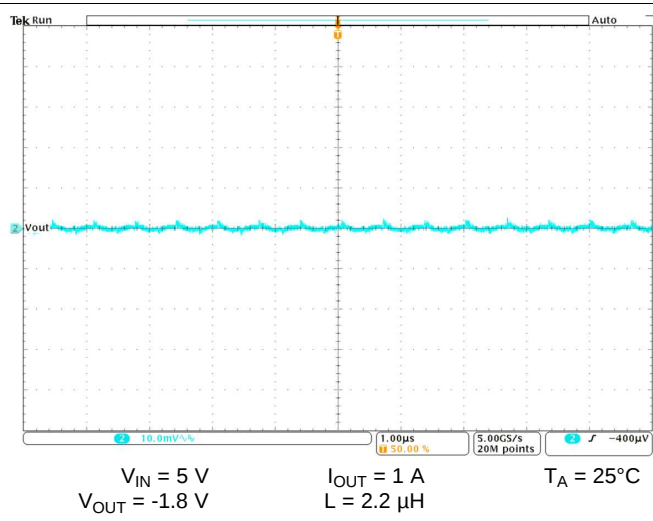


图 32. Output Voltage Ripple

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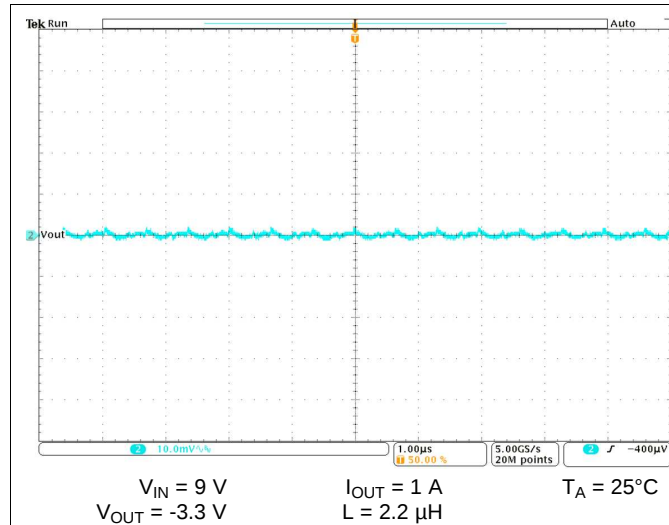


Figure 33. Output Voltage Ripple

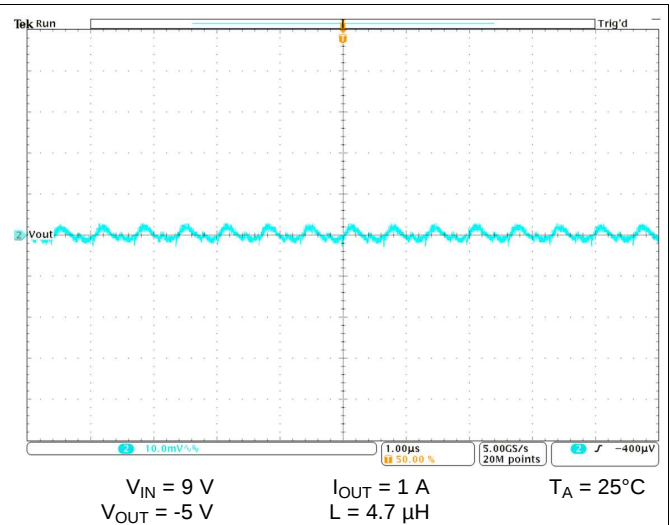


Figure 34. Output Voltage Ripple

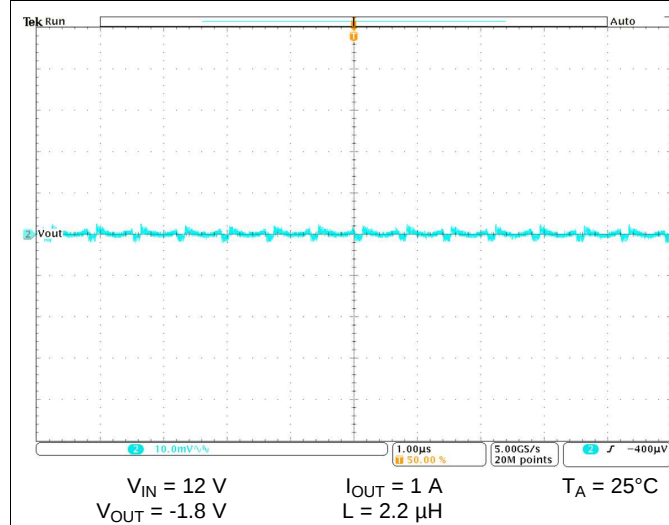


Figure 35. Output Voltage Ripple

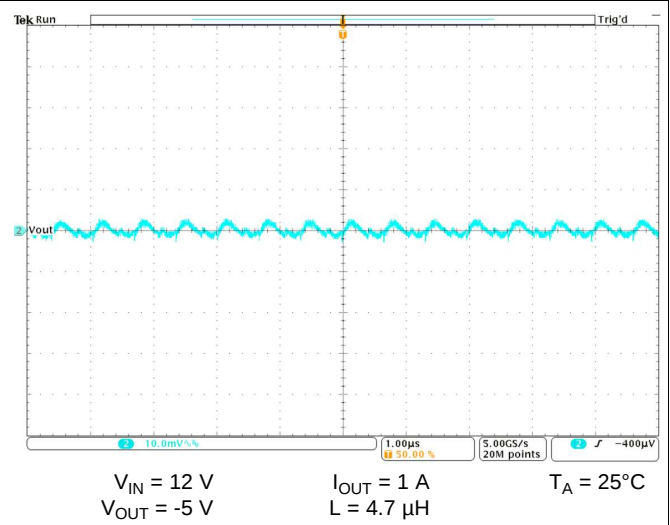


Figure 36. Output Voltage Ripple

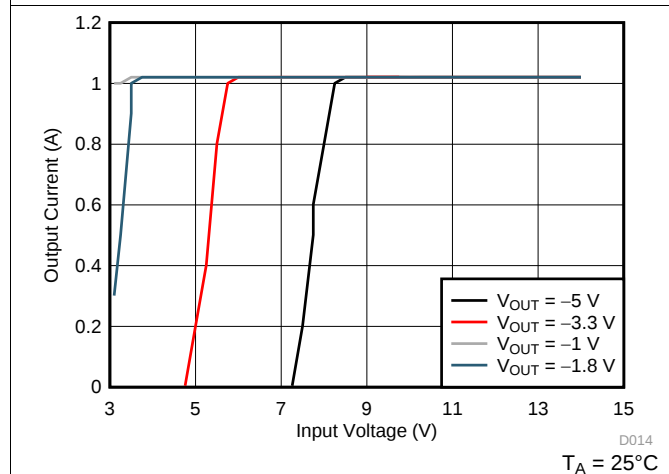


Figure 37. Maximum Output Current vs Input Voltage

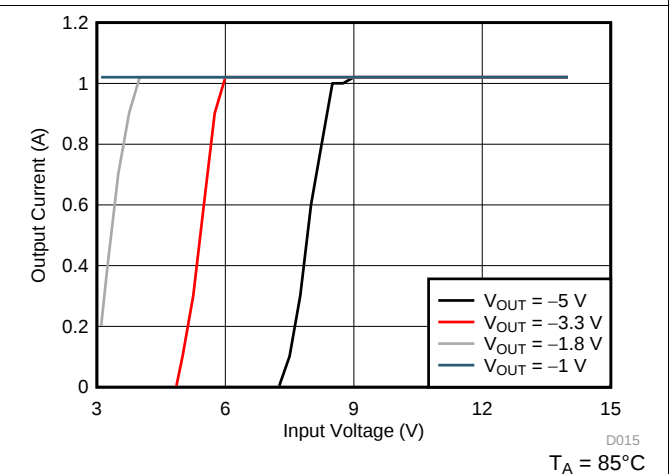


Figure 38. Maximum Output Current vs Input Voltage

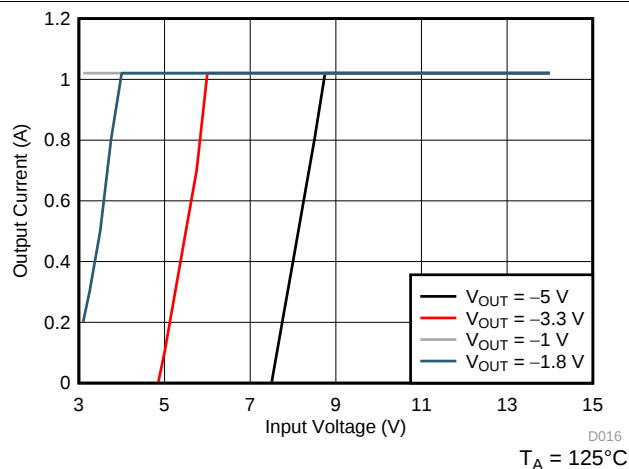


Figure 39. Maximum Output Current vs Input Voltage

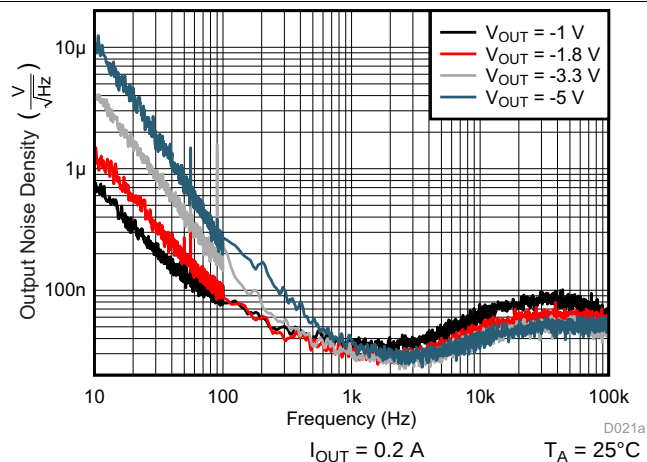


Figure 40. Output Noise Density

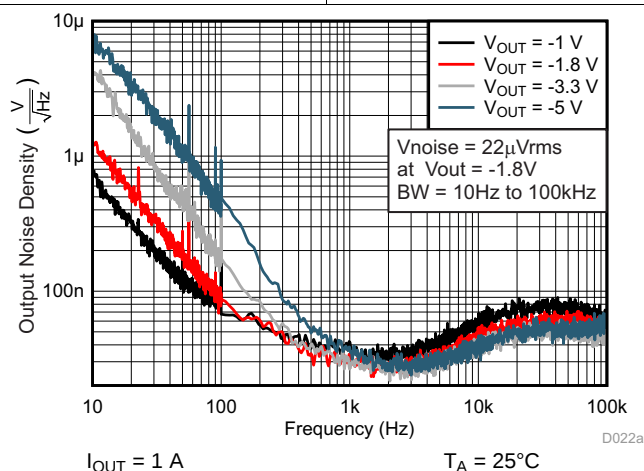
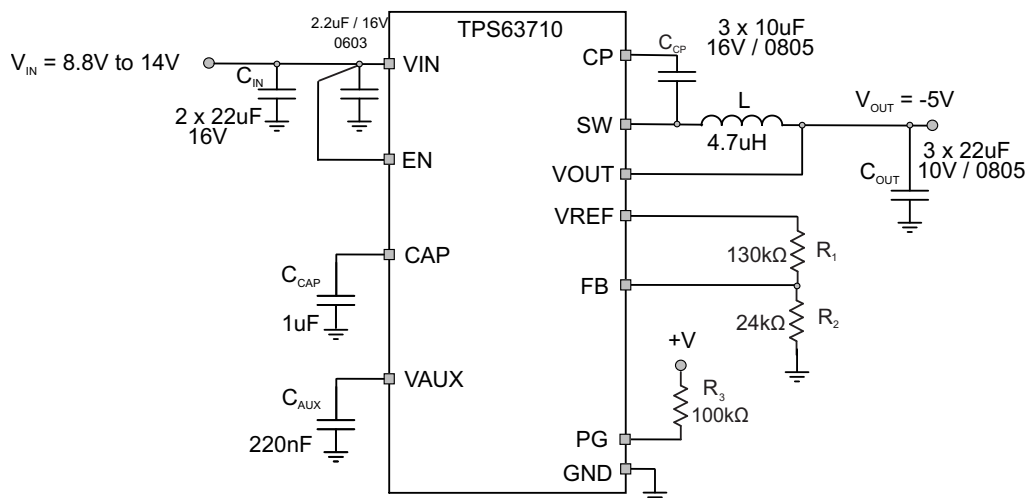


Figure 41. Output Noise Density

8.3 System Examples

8.3.1 Typical Application for Powering the Negative Rail of a Gallium Nitride (GaN) Power Amplifier

The TPS63710 requires a supply voltage in the range of 8.8 V to 14 V in order to generate an output voltage of -5 V. The circuit therefore was optimized for this input voltage range. The number of the input, output and C_{CP} capacitors have been adjusted to compensate for the higher dc bias effect with large input and output voltages. In addition, the inductor has been changed to 4.7 μ H for low inductor current ripple at an input voltage up to 14 V.



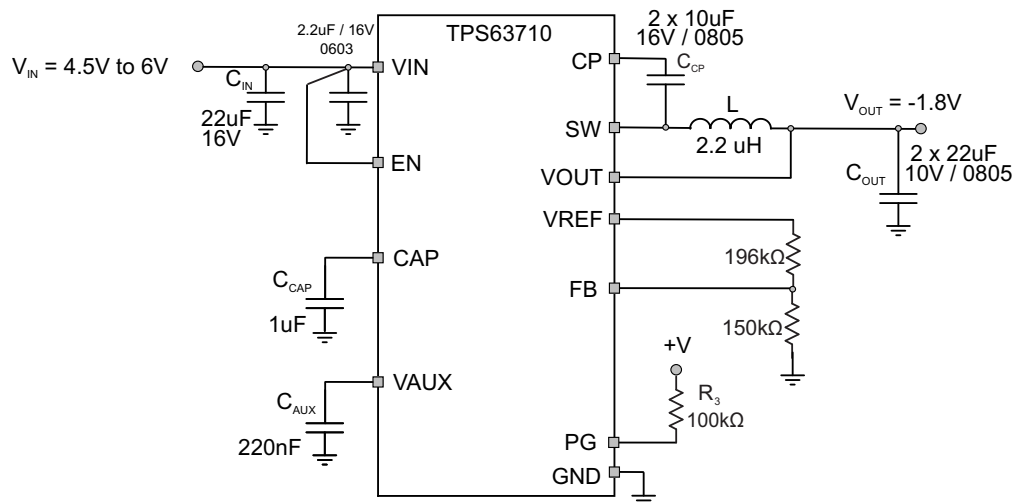
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✎ 42. Typical Application for an Output Voltage of -5 V

8.3.2 Typical Application for Powering the Negative Rail of an ADC or DAC

Typically, the input voltage to the inverter in applications powering the negative supply of an ADC or DAC is about 5 V. The circuit therefore was optimized for this input voltage range, because the size and amount of capacitors depends on the voltage applied to the capacitors. In order not to over-design, the input voltage range was set to the range required to set a limit for the dc bias of the capacitors. ✎ 43 shows a, for an input voltage of 5-V, optimized design. The minimum input voltage to support the full output current is 4.5 V. The maximum input voltage is defined by the dc bias characteristic of the input and C_{CP} capacitors. If a higher input voltage is required, these capacitors have to be adjusted accordingly.

System Examples (continued)

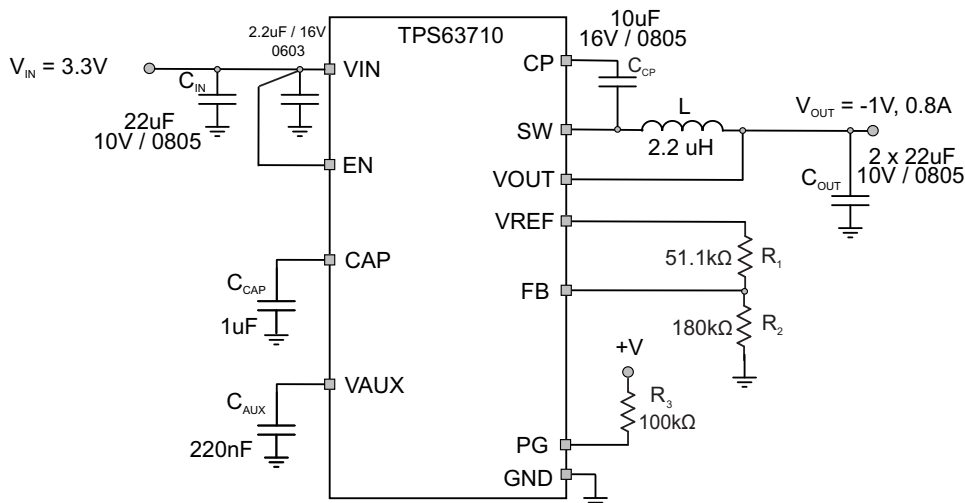


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Figure 43. Typical Application for $V_{IN} \approx 5\text{ V}$

8.3.3 Typical Application for Laser Diode Bias

Laser diode bias typically requires a voltage of about -1 V from a 3.3 V supply. The TPS63710 was optimized for these operating conditions. The passive components have been chosen for a fixed supply voltage of 3.3 V. The number of the input, output and C_{CP} capacitors have been adjusted for the input and output voltage in this application.



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Figure 44. Typical Application for an Output Voltage of -1 V

9 Power Supply Recommendations

The power supply to the TPS63710 needs to have a current rating according to the input supply voltage, output voltage and output current of the TPS63710. The peak current requirement on the input depends on the duty cycle, as C_{CP} is charged during the off-time. Worst case is for the maximum duty cycle of 70% when the OFF-time is at its shortest value of 30%. The peak current on the input can be up to 5 times of the average output current. A proper input capacitor needs to be placed directly at the VIN and GND pins to supply the peak current demand of the converter. Slew rates faster than 1 V/ μ s for a V_{IN} step of less than 1 V and 0.1 V/ μ s for a V_{IN} step over the full input voltage range up to 14 V should be avoided, as this leads to a large inrush current through the C_{CP} capacitor and HSD.

When the input supply of TPS63710 is shorted while the device is enabled, the charge stored on the C_{CP} capacitor is transferred to the output. This may cause an output voltage undershoot. It is recommended to disable the TPS63710 by setting the EN pin to low while the supply voltage is within the recommended input voltage range. This ensures a proper shutdown.

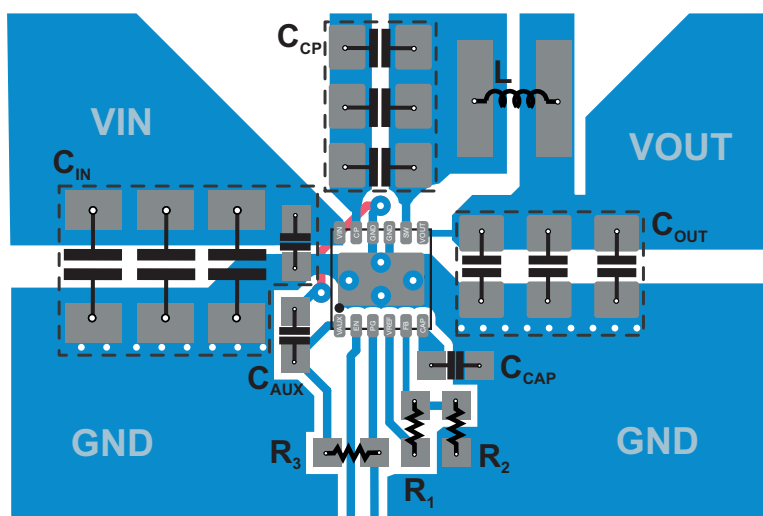
10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths, and for the power-ground tracks. The input, output and CP capacitors should be placed as close as possible to the IC. Because C_{VAUX} carries the peak currents of the gate control block, it should have a compact and direct routing to the VAUX and GND pin 10, staying away from sensitive signals. The CAP, FB, and VREF pins should all be routed close to the IC in order to keep them away from external noise. The total resistance of the voltage divider $R_1 + R_2$ must be kept in the range as defined in the Recommended Operating Conditions.

The pinout of the device has been defined such that the external components can be placed directly at the pins to allow for a simplified external layout and good performance. Thermal and electrical vias should be used under the exposed thermal pad to the GND plane.

10.2 Layout Example



✕ 45. Recommended Layout

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TPS63710デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電氣的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WBENCHでご覧になれます。

11.1.2 デベロッパー・ネットワークの製品に関する免責事項

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11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.3 Trademarks

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WEBENCH is a registered trademark of Texas Instruments.

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11.4 Electrostatic Discharge Caution



これらのデバイスは、限定的なESD (静電破壊) 保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS63710DRRR	Active	Production	WSON (DRR) 12	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	63710
TPS63710DRRR.A	Active	Production	WSON (DRR) 12	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	63710
TPS63710DRRT	Active	Production	WSON (DRR) 12	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	63710
TPS63710DRRT.A	Active	Production	WSON (DRR) 12	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	63710
TPS63710DRRTG4	Active	Production	WSON (DRR) 12	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	63710
TPS63710DRRTG4.A	Active	Production	WSON (DRR) 12	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	63710

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63710DRRR	WSO	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63710DRRT	WSO	DRR	12	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63710DRRTG4	WSO	DRR	12	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63710DRRR	WSN	DRR	12	3000	367.0	367.0	35.0
TPS63710DRRT	WSN	DRR	12	250	210.0	185.0	35.0
TPS63710DRRTG4	WSN	DRR	12	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

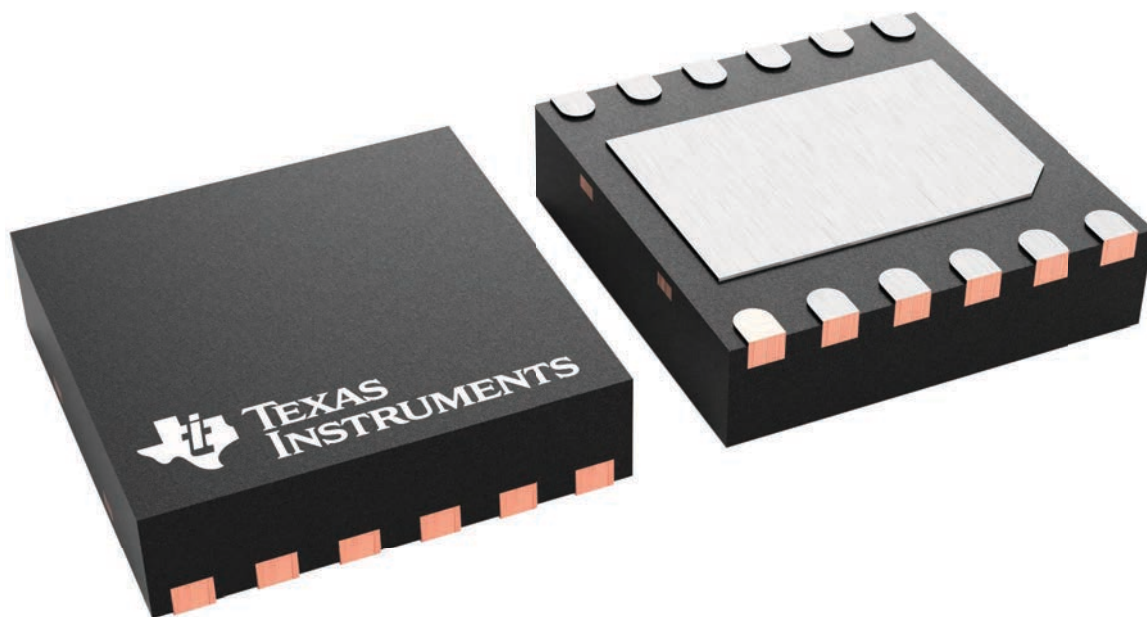
DRR 12

WSON - 0.8 mm max height

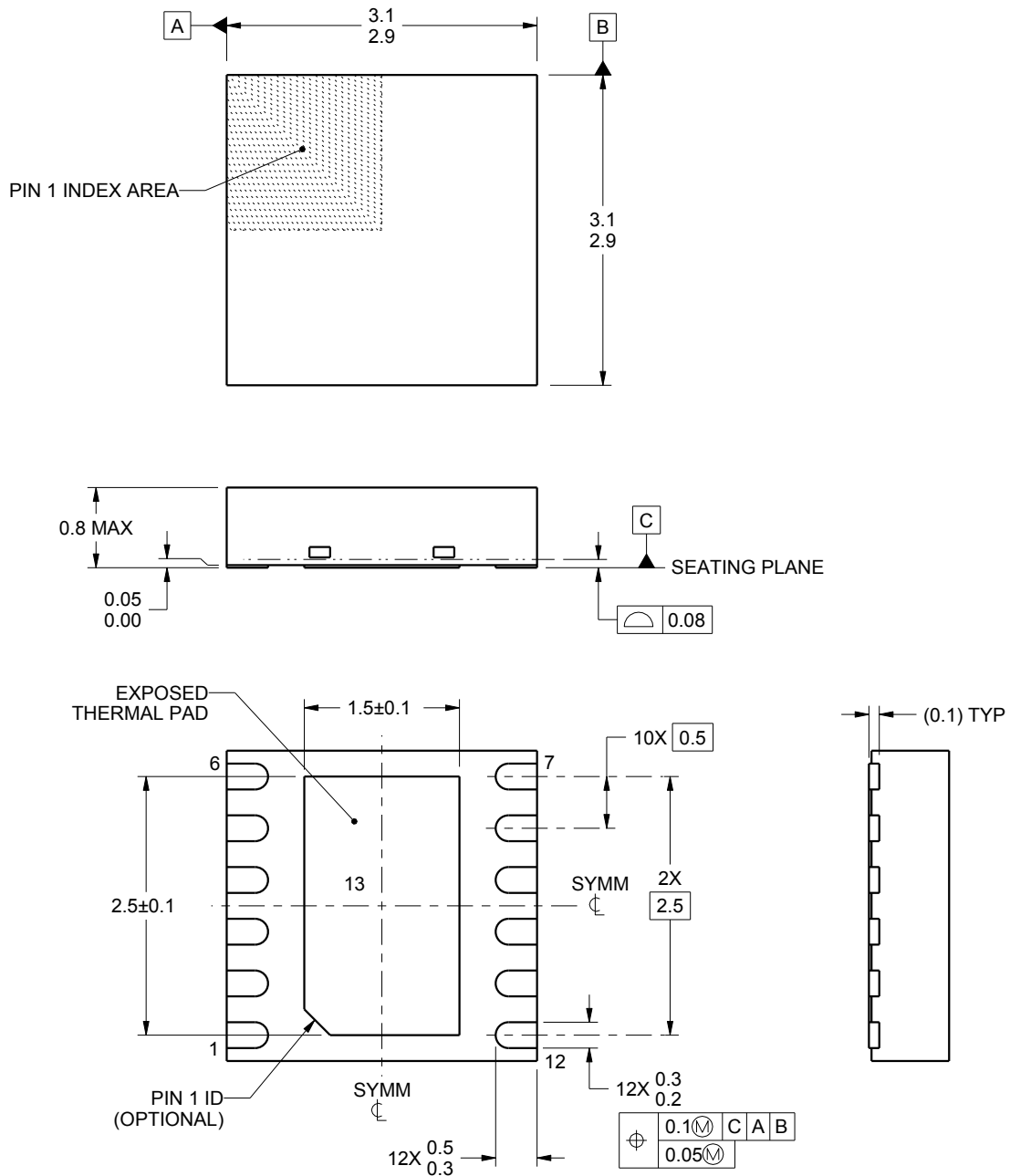
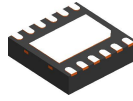
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4223490/B



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NOTES:

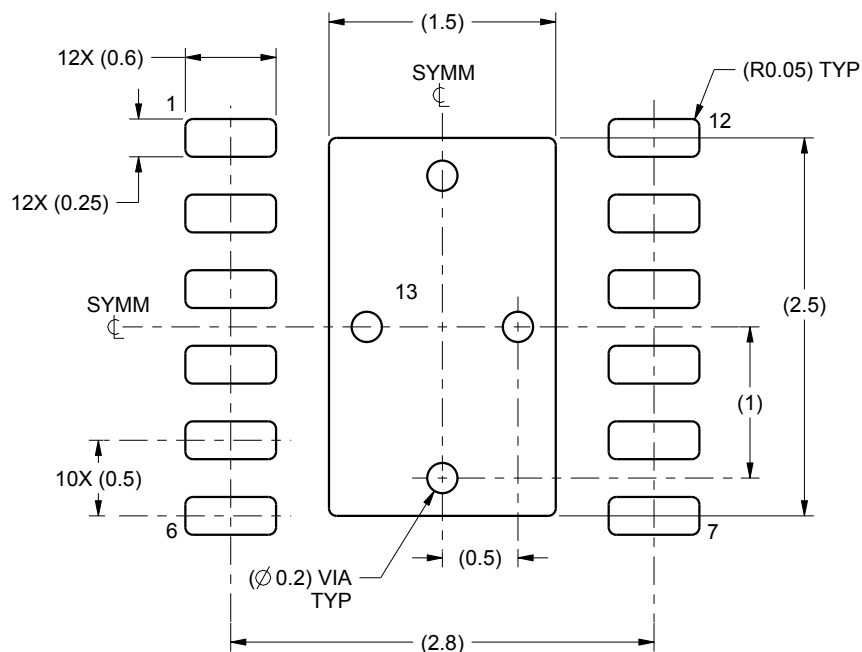
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

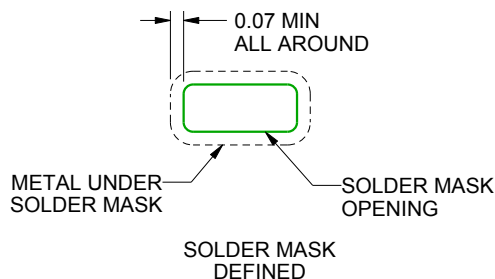
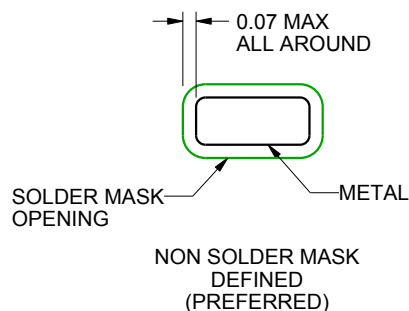
DRR0012C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

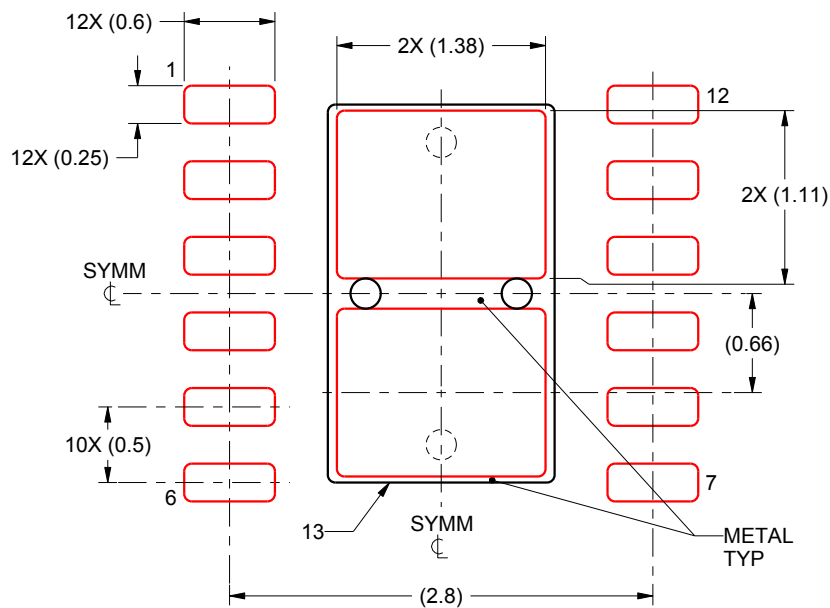
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRR0012C

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13
81.7% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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