



TPS63036 超小型 WCSP に搭載した高効率昇降圧コンバータ

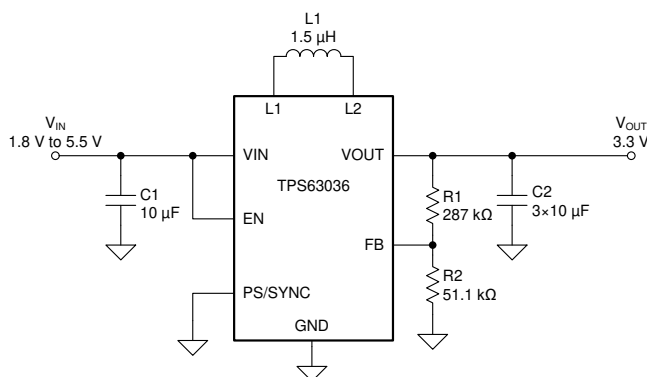
1 特長

- 入力電圧範囲：1.8V～5.5V
(デバイスの起動時は 2V より高いこと)
- 可変出力電圧範囲：1.2V～5.5V
- 全負荷範囲にわたって高効率を実現
 - 動作時静止電流：25μA
 - パワー・セーブ・モードへのシームレスな遷移
- 平均電流モード昇降圧アーキテクチャ
 - モード間の自動遷移
 - 2.4MHz の固定周波数で動作
 - 外部クロックへの同期が可能
- 安全で堅牢な動作を実現する機能
 - 過熱、過電圧保護
 - シャットダウン中の負荷切断
- 超小型の 8 ピン、ウェハー・チップ・スケール・パッケージ (WCSP)：1.814mm × 1.076mm

2 アプリケーション

- バッテリー電圧レギュレーション (ヘッドセットおよびイヤホン、カメラ、AR (拡張現実) メガネ、電子およびロボット玩具、個人用医療関連製品)
- Wi-Fi®または Bluetooth®モジュールの電源 (IP ネットワーク・カメラ、ワイヤレス・アクセス・ポイント、シングル・ボード・コンピュータ、携帯型 POS、ワイヤレス・センサ)
- LED/レーザーの電源 (バーコード・スキャナ、レーザー距離計)

代表的なアプリケーションの回路図



3 概要

TPS63036 は、出力電圧より高い入力電源または低い入力電源からレギュレートされた出力電圧を生成できる非反転昇降圧コンバータです。この昇降圧コンバータは、固定周波数のパルス幅変調(PWM)コントローラを基礎とし、同期整流を使用して最大の効率を実現しています。負荷電流が低い時にはコンバータがパワー・セーブ・モードに移行し、広い負荷電流範囲にわたって高効率を維持します。パワー・セーブ・モードを無効にし、コンバータを常に固定スイッチング周波数で動作させることもできます。

スイッチの最大平均電流は 1000mA (標準値) に制限されています。出力電圧は外付けの抵抗分圧器でプログラムできます。

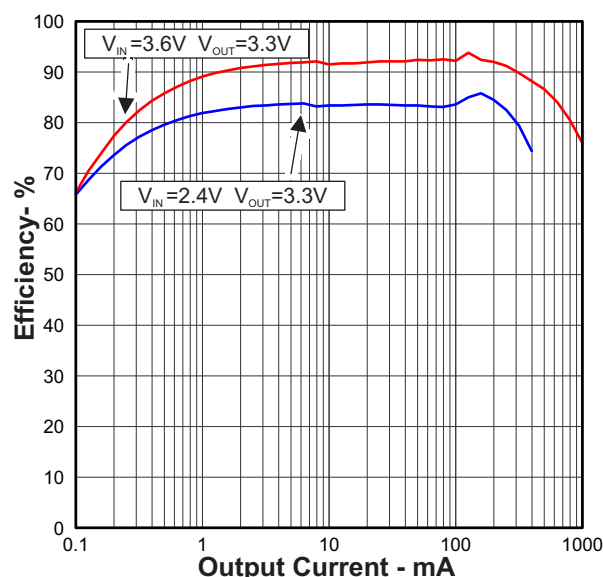
バッテリーの消耗を最小限に抑えるために、コンバータをディセーブルできます。シャットダウン中、負荷は電源から切り離されます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS63036	WCSP (8)	1.814mm × 1.076mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

効率と出力電流との関係



目次

1	特長	1	7.4	Device Functional Modes.....	7
2	アプリケーション	1	8	Application and Implementation	10
3	概要	1	8.1	Application Information.....	10
4	改訂履歴.....	2	8.2	Typical Application	10
5	Pin Configuration and Functions	3	9	Power Supply Recommendations	17
6	Specifications.....	3	10	Layout.....	17
6.1	Absolute Maximum Ratings	3	10.1	Layout Guidelines	17
6.2	ESD Ratings.....	3	10.2	Layout Example	17
6.3	Recommended Operating Conditions.....	3	10.3	Thermal Considerations.....	17
6.4	Thermal Information	4	11	デバイスおよびドキュメントのサポート	18
6.5	Electrical Characteristics.....	4	11.1	デバイス・サポート	18
6.6	Typical Characteristics	5	11.2	コミュニティ・リソース	18
7	Detailed Description	6	11.3	商標	18
7.1	Overview	6	11.4	静電気放電に関する注意事項	18
7.2	Functional Block Diagram	6	11.5	Glossary	18
7.3	Feature Description.....	6	12	メカニカル、パッケージ、および注文情報	18

4 改訂履歴

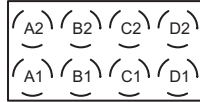
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (August 2015) から Revision B に変更	Page
• 特長 および アプリケーション を更新	1
• 「 特長 」と「製品情報」表の本体サイズを訂正.....	1
• 効率グラフを訂正	1
• Removed hints to fixed output voltage versions (for example, in the <i>Pin Functions</i> table).....	3

2012年8月発行のものから更新	Page
• 「 ESD 定格 」表、「 機能説明 」セクション、「 デバイスの機能モード 」セクション、「 アプリケーションと実装 」セクション、「 電源に関する推奨事項 」セクション、「 レイアウト 」セクション、「 デバイスおよびドキュメントのサポート 」セクション、「 メカニカル、パッケージ、および注文情報 」セクション 追加	1
• Removed <i>Available Output Voltage Options</i> table	3
• Removed <i>Packaging Information</i> section	17

5 Pin Configuration and Functions

**YFG Package
8-Pin WCSP
Top View**



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	A2	Input	Enable input (1 enabled, 0 disabled)
FB	D2	Input	Voltage feedback pin
GND	C2	—	Control/logic ground
PS/SYNC	B2	Input	Enable/disable power-save mode (1 disabled, 0 enabled, clock signal for synchronization)
L1	B1	Input	Connection for inductor
L2	C1	Input	Connection for inductor
VIN	A1	Input	Supply voltage for power stage
VOUT	D1	Output	Buck-boost converter output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Input voltage on VIN, L1, L2, VOUT, PS/SYNC, EN, FB	−0.3	7	V
Operating virtual junction temperature, T _J	−40	150	°C
Storage temperature, T _{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage at VIN	1.8	5.5	V
Operating free air temperature, T _A	−40	85	°C
Operating virtual junction temperature, T _J	−40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS63036	UNIT
		YFG (WCSP)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	84	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	43.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage range		1.8 ⁽¹⁾		5.5	V
V _{OUT}	Output voltage range		1.2		5.5	V
	Duty cycle in step-down conversion		20%			
V _{FB}	Feedback voltage	PS/SYNC = V _{IN} I _{OUT} < 5 mA	495	500	505	mV
V _{FB}	Feedback voltage	PS/SYNC = GND referenced to 500 mV I _{OUT} < 5 mA	-3%		+6%	
	Load regulation	PS/SYNC = GND		0.008		%/mA
f	Oscillator frequency		1800	2000	2200	kHz
	Frequency range for synchronization		2200	2400	2600	kHz
I _{SW}	Average input current limit	V _{IN} = 3.6 V, T _A = 25°C ⁽²⁾		1000		mA
	High-side switch ON-resistance	V _{IN} = 3.6 V		200		mΩ
	Low-side switch ON-resistance	V _{IN} = 3.6 V		200		mΩ
	Line regulation			0.5%		
I _q	Quiescent current	V _{IN}		25	35	μA
		V _{OUT}		4	6	μA
I _S	Shutdown current	V _{EN} = 0 V, V _{IN} = 3.6 V		0.1	0.9	μA
CONTROL STAGE						
V _{UVLO}	Undervoltage lockout threshold falling		1.4	1.5	1.6	V
	Undervoltage lockout threshold raising		1.6	1.8	2.0	V
V _{IL}	EN, PS/SYNC input low voltage				0.4	V
V _{IH}	EN, PS/SYNC input high voltage		1.2			V
	EN, PS/SYNC input current	Clamped on GND or V _{IN}		0.01	0.1	μA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C

(1) The typical required supply voltage for start-up is 2 V. The part is functional down to 1.8 V.

(2) For the minimum specified average input current limit at V_{OUT} = 2.5 V, 3.3 V and 4.5 V refer to curve in [Figure 1](#). For the maximum specified average input current limit at V_{OUT} = 2.5 V, 3.3 V and 4.5 V refer to curve in [Figure 2](#).

6.6 Typical Characteristics

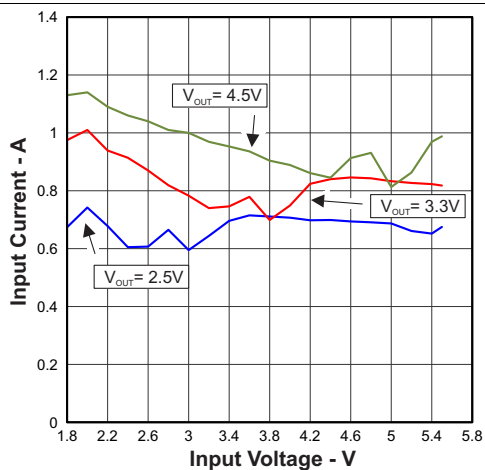


Figure 1. Minimum Input Current vs Input Voltage

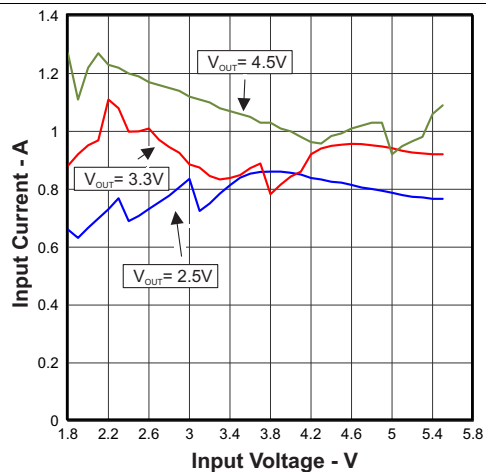


Figure 2. Maximum Input Current vs Input Voltage

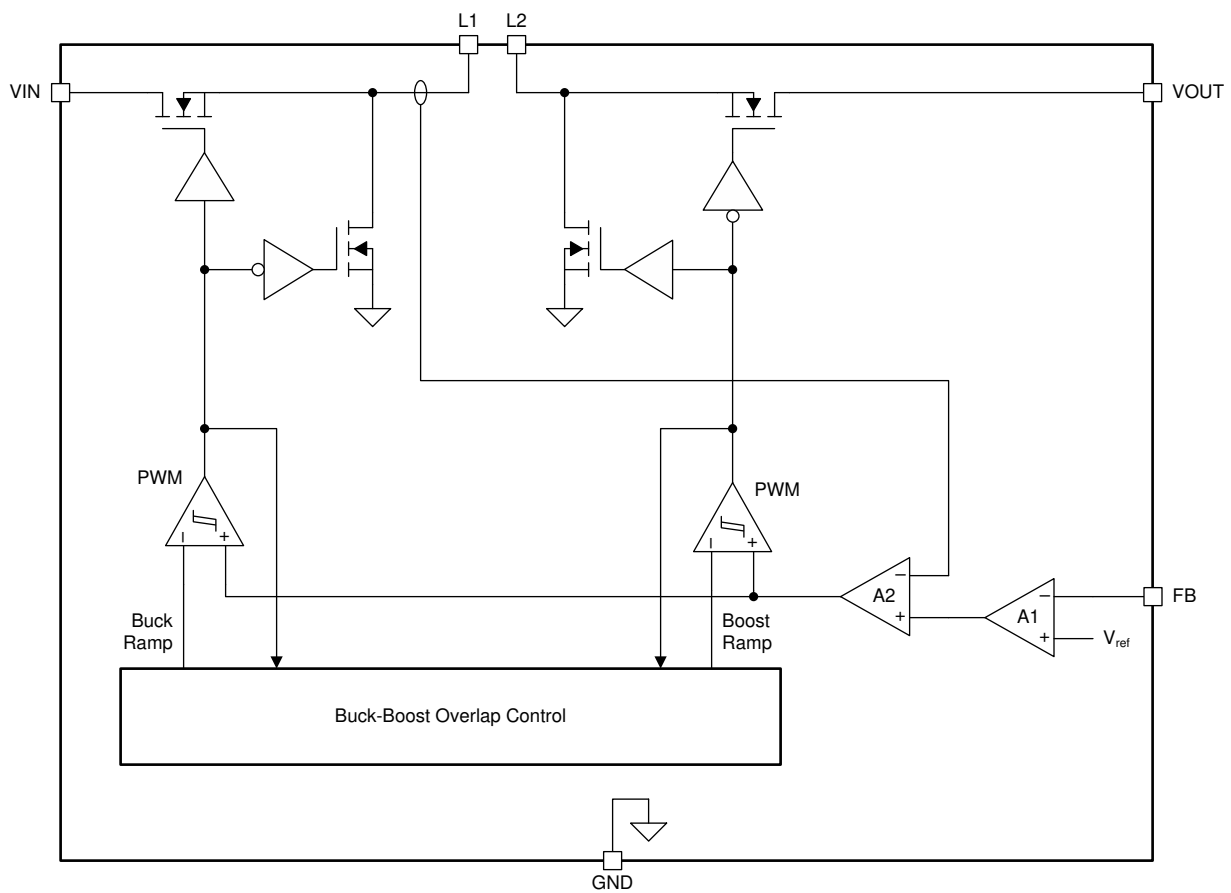
7 Detailed Description

7.1 Overview

The controller circuit of the device is based on an average current mode topology. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately can change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. A resistive voltage divider must be connected to that pin. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The device uses 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter. To protect the device from overheating an internal temperature sensor is implemented.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

Feature Description (continued)

7.3.2 Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. The implemented overvoltage protection circuit monitors the output voltage internally as well. In case it reaches the overvoltage threshold the voltage amplifier regulates the output voltage to this value.

7.3.3 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage at VIN is lower than approximately its threshold (see [Electrical Characteristics](#) table). When in operation, the device automatically enters the shutdown mode if the voltage at VIN drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

7.3.4 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see [Electrical Characteristics](#) table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

7.4 Device Functional Modes

7.4.1 Soft-Start and Short Circuit Protection

After being enabled, the device starts operating. The average input current limit ramps up from an initial 400 mA following the output voltage increasing. At an output voltage of about 1.2 V, the current limit is at its nominal value. If the output voltage does not increase, the current limit will also not increase. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. When the output voltage does not increase above 1.2 V, the device assumes a short circuit at the output, and keeps the current limit low to protect itself and the application. At a short on the output during operation, the current limit also is decreased accordingly.

7.4.2 Buck-Boost Operation

To regulate the output voltage at all possible input voltage conditions, the device automatically switches from step-down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step-down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. For the remaining 2 switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

7.4.3 Control Loop

The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. [Figure 3](#) shows the control loop.

The noninverting input of the trans-conductance amplifier Gmv can be assumed to be constant. The output of Gmv defines the average inductor current. The inductor current is reconstructed measuring the current through the high-side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode the current is measured during the ON-time of the same MOSFET. During the OFF-time the current is reconstructed internally starting from the peak value reached at the end of the ON-time cycle. The average current is then compared to the desired value and the difference, or current error, is amplified and compared to the sawtooth ramp of either the buck or the boost.

Device Functional Modes (continued)

The Buck-Boost Overlap Control makes sure that the classical buck-boost function, which would cause two switches to be on every half a cycle, is avoided. Thanks to this block whenever all switches becomes active during one clock cycle, the two ramps are shifted away from each other, on the other hand when there is no switching activities because there is a gap between the ramps, the ramps are moved closer together. As a result the number of classical buck-boost cycles or no switching is reduced to a minimum and high-efficiency values have been achieved.

Slope compensation is not required to avoid subharmonic oscillation which are otherwise observed when working with peak current mode control with $D > 0.5$.

Nevertheless the amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input. This purpose is reached limiting the gain of the current amplifier.

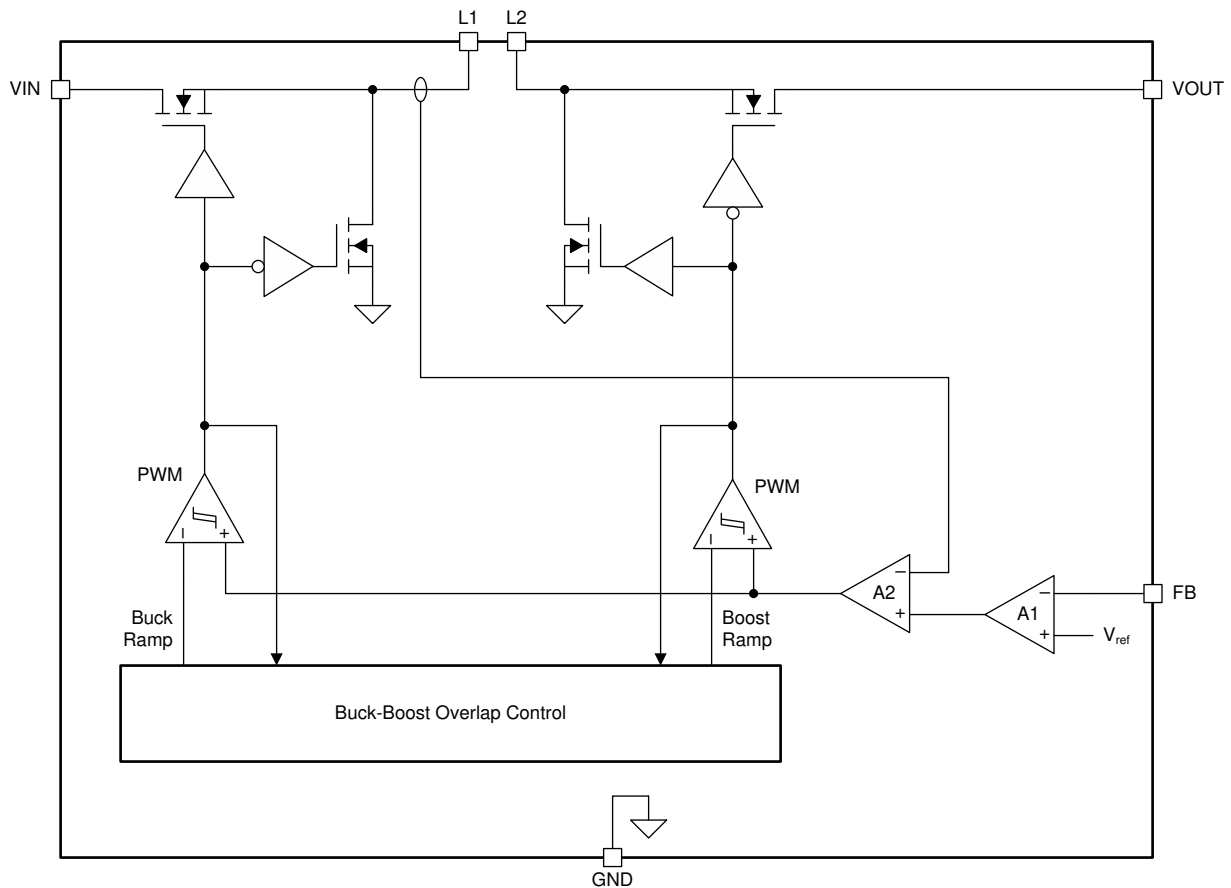


Figure 3. Average Current Mode Control

7.4.4 Power-Save Mode and Synchronization

The PS/SYNC pin can be used to select different operation modes. Power-save mode is used to improve efficiency at light load. To enable power-save mode, PS/SYNC must be set low. If PS/SYNC is set low then power-save mode is entered when the average inductor current gets lower than about 100 mA. At this point the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency.

Device Functional Modes (continued)

During the power-save mode, the output voltage is monitored with a comparator by the threshold comp low and comp high. When the device enters power-save mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. As the output voltage falls below the comp low threshold, the device ramps up the output voltage again, by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last one or several pulses. The converter continues these pulses until the comp high threshold is reached and the average inductance current gets lower than about 100 mA. When the load increases above the minimum forced inductor current of about 100 mA, the device will automatically switch to PWM mode.

The power-save mode can be disabled by programming high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency.

Synchronization is done by a phase-locked loop (PLL), so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS63036 device is a noninverting buck-boost converter that is suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage. The device supports regulated output voltages from 1.2 V to 5.5 V.

8.2 Typical Application

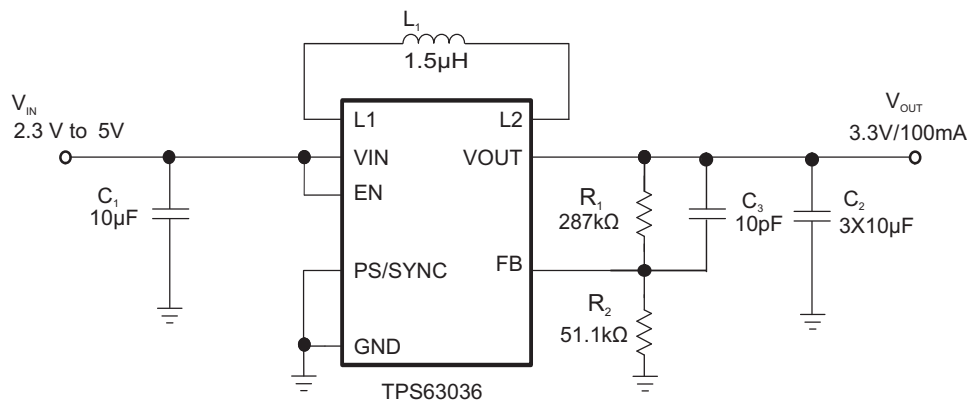


Figure 4. Typical Operating Circuit

8.2.1 Design Requirements

The design guidelines provide a component selection to operate the adjustable device within the [Recommended Operating Conditions](#).

8.2.2 Detailed Design Procedure

The design guideline provides a component selection to operate the device within the recommended operating conditions.

[Table 1](#) shows the list of components for the [Application Curves](#).

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63036	Texas Instruments
L1	1.5 µH, 3 mm x 3 mm x 1.5 mm	Coilcraft, LPS3015-152MLC
C1	10 µF 6.3V, 0603, X7R ceramic	GRM188R60J106KME8 4D, Murata
C2	3 × 10 µF 6.3V, 0603, X7R ceramic	GRM188R60J106KME8 4D, Murata
R1, R2	Depending on the output voltage at TPS63036	

The TPS63036 buck-boost converter has internal loop compensation. Therefore, the external L-C filter has to be selected to work with the internal compensation. As a general rule of thumb, the product $L \times C$ should not move over a wide range when selecting a different output filter. However, when selecting the output filter a low limit for the inductor value exists to avoid sub-harmonic oscillation which could be caused by a far too fast ramp up of the amplified inductor current. For the TPS63036 the minimum inductor value should be kept at 1 μH . To simplify this process [Table 1](#) outlines possible inductor and capacitor value combinations.

Table 2. Output Filter Selection (Average Inductance Current up to 1 A)

INDUCTOR VALUE [μH] ⁽¹⁾	OUTPUT CAPACITOR VALUE [μF] ⁽²⁾		
	30	44	66
1.0	√	√	√
1.5	√ ⁽³⁾	√	√
2.2			√

- (1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and –30%.
- (2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and –50%.
- (3) Typical application. Other check mark indicates recommended filter combinations

8.2.2.1 Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, with the chosen inductance value, the peak current for the inductor in steady-state operation can be calculated. Only the equation which defines the switch current in boost mode is reported because this is providing the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \quad D = \frac{V_{\text{out}} - V_{\text{in}}}{V_{\text{out}}} \quad (1)$$

$$I_{\text{PEAK}} = I_{\text{SW_MAX}} + \frac{V_{\text{in}} \times D}{2 \times f \times L}$$

where

- D = Duty cycle in boost mode
 - f = Converter switching frequency (typical 2 MHz)
 - L = Selected inductor value
 - η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)
 - $I_{\text{SW_MAX}}$ = Maximum average input current ([Figure 6](#))
- (2)

NOTE

The calculation must be done for the minimum input voltage which is possible to have in boost mode.

Consider the load transients and error conditions that can cause higher inductor currents. Consider when selecting an appropriate inductor. Please refer to [Table 3](#) for typical inductors.

The size of the inductor can also affect the stability of the feedback loop. In particular the boost transfer function exhibits a right half-plane zero, whose frequency is inverse proportional to the inductor value and the load current. This means as higher the value of inductance and load current is the more possibilities has the right plane zero to be moved at lower frequency. This could degrade the phase margin of the feedback loop. TI recommends to choose the value of the inductor in order to have the frequency of the right half plane zero >400 kHz. The frequency of the RHPZ can be calculated using equation [Equation 2](#).

$$f_{\text{RHPZ}} = \frac{(1 - D)^2 \times V_{\text{out}}}{2\pi \times I_{\text{out}} \times L}$$

where

- D =Duty cycle in boost mode

(3)

NOTE

The calculation must be done for the minimum input voltage which is possible to have in boost mode.

Table 3. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
1 μH	TOKO 1286AS-H-1R0M	2x1.6x1.2	2.3A/78mΩ
1 μH	Coilcraft XFL4020-102	4 x 4 x 2.1	5.1A/10.8 mΩ
1 μH	Coilcraft XFL3012-102	3 x 3 x 1.2	2.2 A/35 mΩ
1.5μH	TOKO, 1286AS-H-1R5M	2 x 1.6 x 1.2	4.4A/ 14.40mΩ
1.5μH	Coilcraft, LPS3015-152MLC	3 x 3 x 1.5	2.1A/100mΩ
1.5μH	TOKO, 1269AS-H-1R5M	2.5 x 2 x 1	2.1A/108mΩ
2.2μH	TOKO D1286AS-H-2R2M	2 x 1.6 x 1.2	1.6A/192mΩ

8.2.2.2 Capacitor Selection

8.2.2.2.1 Input Capacitor

At least a 10-μF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

8.2.2.2.2 Output Capacitor

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and GND pins of the IC. The recommended typical output capacitor value is 30 μF.

There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

When choosing input and output capacitors, it needs to be kept in mind, that the value of capacitance experiences significant losses from their rated value depending on the operating temperature and the operating DC voltage. It is not uncommon for a small surface mount ceramic capacitor to lose 50% and more of its rated capacitance. For this reason it could be important to use a larger value of capacitance or a capacitor with higher voltage rating in order to ensure the required capacitance at the full operating voltage.

8.2.2.3 Setting the Output Voltage

The output voltage of the TPS63036 is set by an external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The typical current into the FB pin is 0.01 μA, and the voltage across the resistor between FB and GND, R2, is typically 500 mV. Based on these two values, the recommended value for R2 should be lower than 100 kΩ, in order to set the divider current at 5 μA or higher. From that, the value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using [Equation 4](#):

$$R1 = R2 \times \left(\frac{V_{\text{OUT}}}{V_{\text{FB}}} - 1 \right) \quad (4)$$

A small capacitor C3 = 10 pF, in parallel with R1 needs to be placed when using the power-save mode, to improve considerably the output voltage ripple.

8.2.2.4 Current Limit

To protect the device and the application, the average input current is limited internally on the IC. At nominal operating conditions, this current limit is constant. The current limit value can be found in the [Electrical Characteristics](#) table. The current limit varies depending on the input voltage. A curve of the input current varying with the input voltage is shown in [Figure 5](#) and [Figure 6](#) respectively showing the minimum and the maximum current limit expected depending on input and output voltage.

Given the average input current in [Figure 5](#) is then possible to calculate the output current reached in boost mode using [Equation 5](#) and [Equation 6](#) and in buck mode using [Equation 7](#) and [Equation 8](#).

$$\text{Duty Cycle Boost} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (5)$$

$$\text{Maximum Output Current Boost} \quad I_{OUT} = \eta \times I_{SW} \times (1 - D) \quad (6)$$

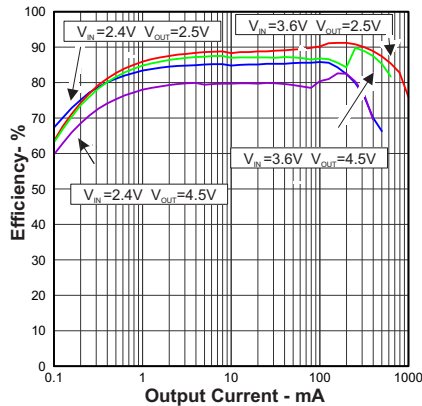
$$\text{Duty Cycle Buck} \quad D = \frac{V_{OUT}}{V_{IN}} \quad (7)$$

$$\text{Maximum Output Current Buck} \quad I_{out} = \frac{\eta \times I_{sw}}{D}$$

where

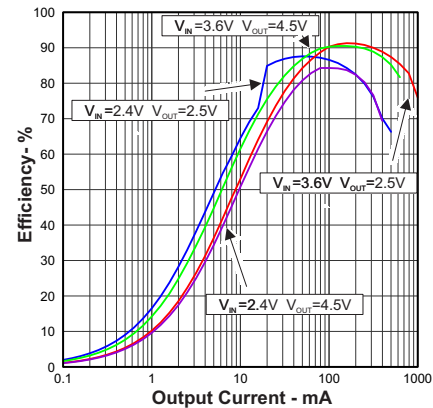
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)
 - f = Converter switching frequency (typical 2 MHz)
 - L = Selected inductor value
 - I_{SW} = Minimum average input current ([Figure 5](#))
- (8)

8.2.3 Application Curves



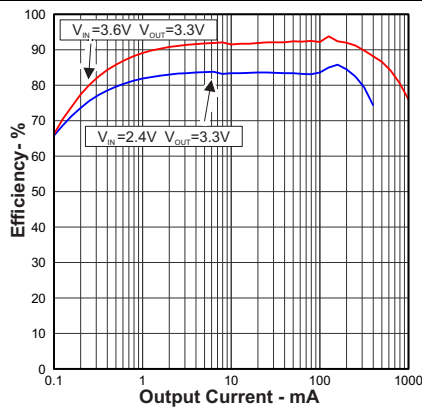
$V_{OUT} = 2.5\text{ V} / 4.5\text{ V}$

Figure 5. Efficiency vs Output Current – Power-Save Mode Enabled



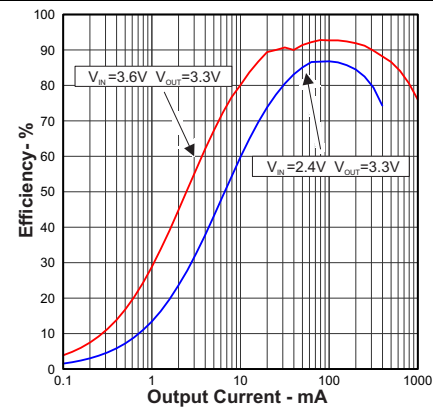
$V_{OUT} = 2.5\text{ V} / 4.5\text{ V}$

Figure 6. Efficiency vs Output Current – Power-Save Mode Disabled



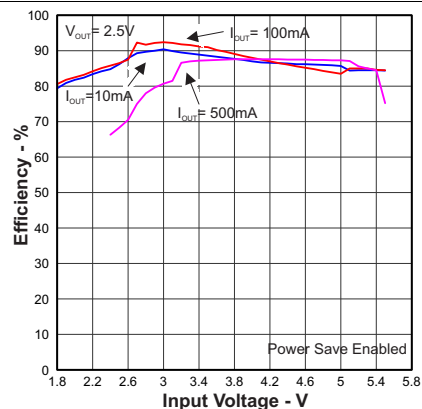
$V_{OUT} = 3.3\text{ V}$

Figure 7. Efficiency vs Output Current – Power-Save Mode Enabled



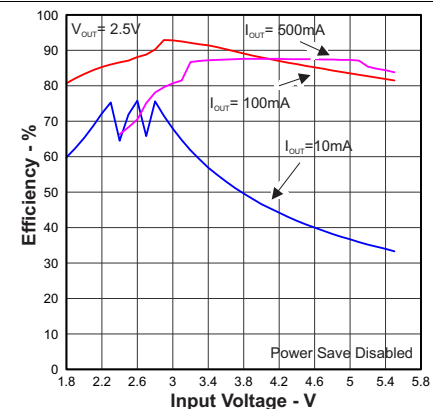
$V_{OUT} = 3.3\text{ V}$

Figure 8. Efficiency vs Output Current – Power-Save Mode Disabled



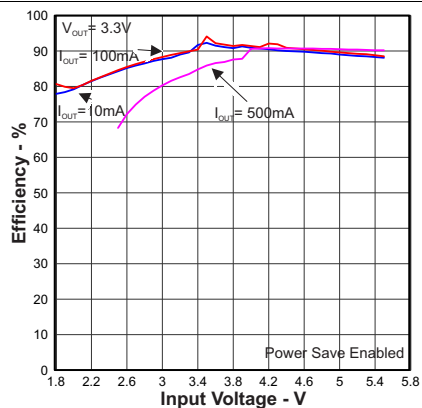
$V_{OUT} = 2.5\text{ V}, I_{OUT} = 10\text{ mA}/100\text{ mA}/500\text{ mA}$

Figure 9. Efficiency vs Input Voltage – Power-Save Mode Enabled



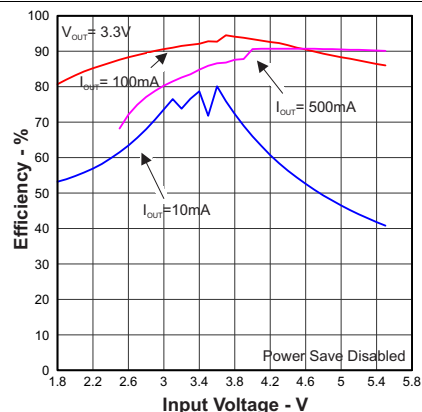
$V_{OUT} = 2.5\text{ V}, I_{OUT} = 10\text{ mA}/100\text{ mA}/500\text{ mA}$

Figure 10. Efficiency vs Input Voltage – Power-Save Mode Disabled



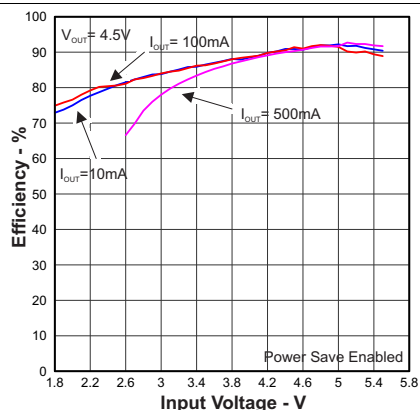
$V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 10\text{ mA}/100\text{ mA}/500\text{ mA}$

Figure 11. Efficiency vs Input Voltage – Power-Save Mode Enabled



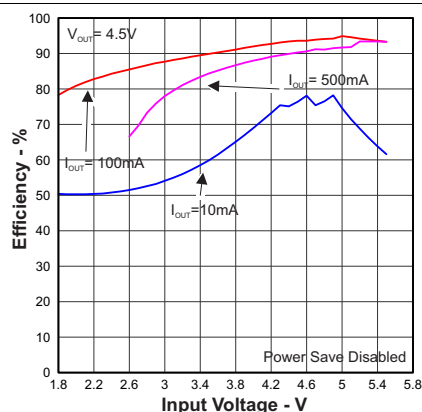
$V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 10\text{ mA}/100\text{ mA}/500\text{ mA}$

Figure 12. Efficiency vs Input Voltage – Power-Save Mode Disabled



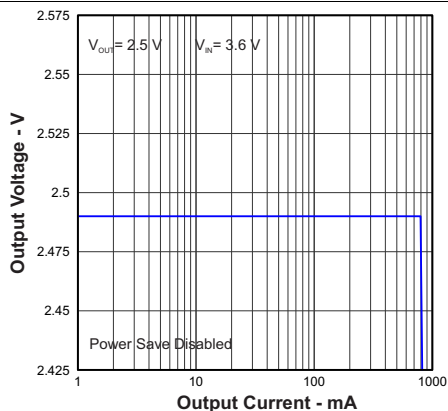
$V_{OUT} = 4.5\text{ V}$, $I_{OUT} = 10\text{ mA}/100\text{ mA}/500\text{ mA}$

Figure 13. Efficiency vs Input Voltage – Power-Save Mode Enabled



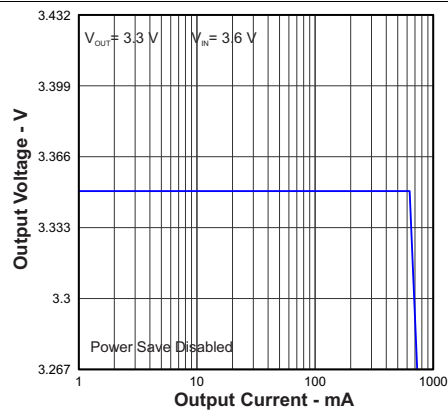
$V_{OUT} = 4.5\text{ V}$, $I_{OUT} = 10\text{ mA}/100\text{ mA}/500\text{ mA}$

Figure 14. Efficiency vs Input Voltage – Power-Save Mode Disabled



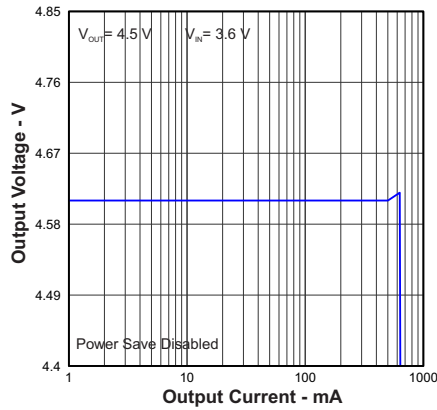
$V_{OUT} = 2.5\text{ V}$

Figure 15. Output Voltage vs Output Current



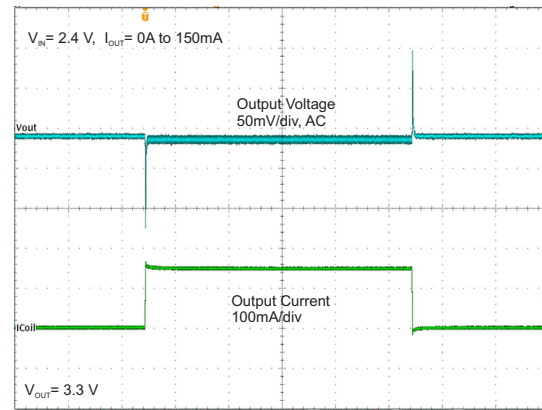
$V_{OUT} = 3.3\text{ V}$

Figure 16. Output Voltage vs Output Current



$V_{OUT} = 4.5\text{ V}$

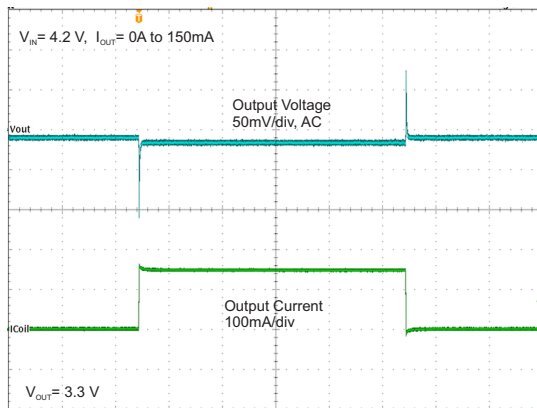
Figure 17. Output Voltage vs Output Current



Time 1ms/Div

$V_{IN} < V_{OUT}$, Load Change from 0 mA to 150 mA

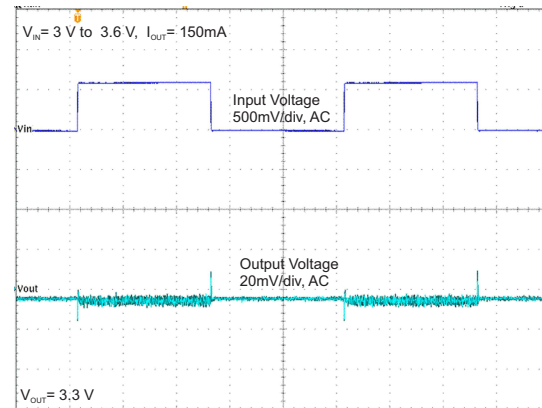
Figure 18. Load Transient Response



Time 1ms/Div

$V_{IN} > V_{OUT}$, Load Change from 0 mA to 150 mA

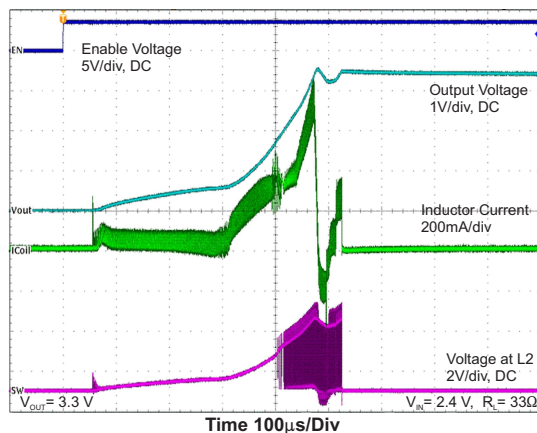
Figure 19. Load Transient Response



Time 2ms/Div

$V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 150\text{ mA}$

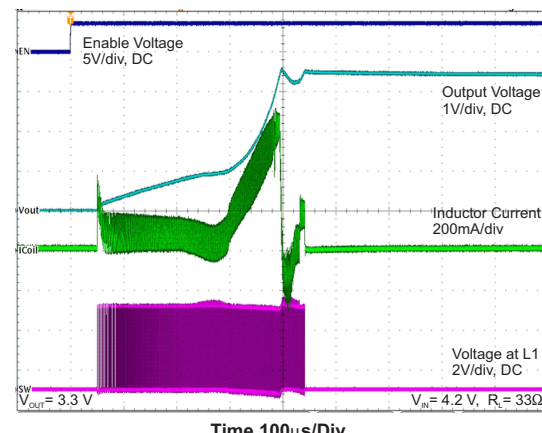
Figure 20. Line Transient Response



Time 100μs/Div

$V_{OUT} = 3.3\text{ V}$, $V_{IN} = 2.4\text{ V}$, $R_L = 33\Omega$

Figure 21. Start-Up After Enable



Time 100μs/Div

$V_{OUT} = 3.3\text{ V}$, $V_{IN} = 4.2\text{ V}$, $R_L = 33\Omega$

Figure 22. Start-Up After Enable

9 Power Supply Recommendations

The TPS63036 device has no special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage and output current of the TPS63036.

10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC.

The feedback divider should be placed as close as possible to the ground pin of the IC.

10.2 Layout Example

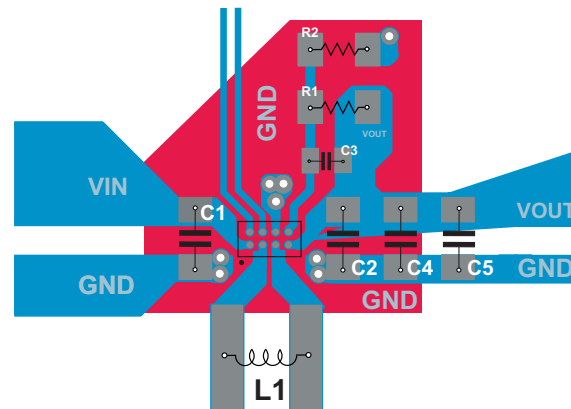


Figure 23. Layout Recommendation

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB by soldering all pins to traces as wide as possible.
3. Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS63036 device is 125°C. The thermal resistance of this 8-pin chip-scale package (YFG) is $R_{\theta JA} = 84^\circ\text{C/W}$, if all pins are soldered. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 476 mW, as calculated in Equation 9. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125^\circ\text{C} - 85^\circ\text{C}}{84^\circ\text{C/W}} = 476 \text{ mW} \quad (9)$$

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商標

E2E is a trademark of Texas Instruments.

Bluetooth is a registered trademark of Bluetooth SIG.

Wi-Fi is a registered trademark of Wi-Fi Alliance.

11.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD（静電破壊）保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS63036YFGR	Active	Production	DSBGA (YFG) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S63036
TPS63036YFGR.A	Active	Production	DSBGA (YFG) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S63036
TPS63036YFGT	Active	Production	DSBGA (YFG) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S63036
TPS63036YFGT.A	Active	Production	DSBGA (YFG) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S63036

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63036YFGR	DSBGA	YFG	8	3000	180.0	8.4	1.2	2.0	0.7	4.0	8.0	Q1
TPS63036YFGT	DSBGA	YFG	8	250	180.0	8.4	1.2	2.0	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

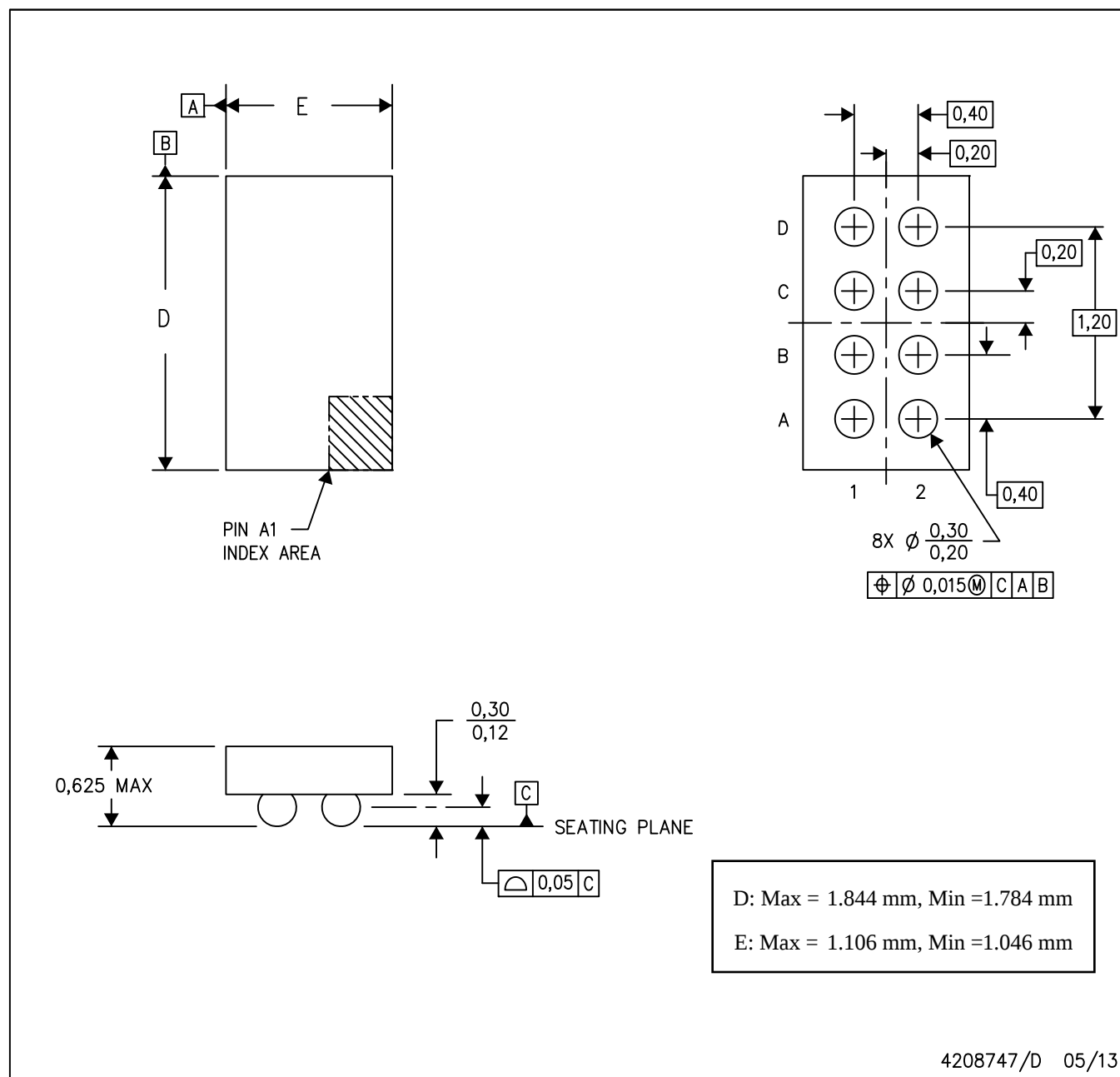


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63036YFGR	DSBGA	YFG	8	3000	182.0	182.0	20.0
TPS63036YFGT	DSBGA	YFG	8	250	182.0	182.0	20.0

YFG (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Die size package configuration.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月