

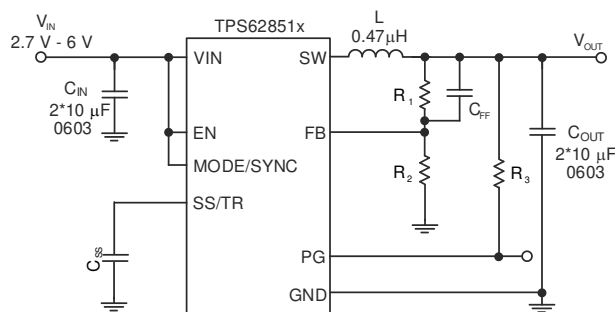
# TPS62851x 2.7V~6V、0.5A/1A/2A/3A 降圧コンバータ、SOT583 パッケージ

## 1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 入力電圧範囲: 2.7V~6V
- 出力電圧: 0.6V~5.5V
- 1% の帰還電圧精度 (全温度範囲)
- $T_J = -40^{\circ}\text{C} \sim +150^{\circ}\text{C}$
- 0.5A、1A、2A (連続)、3A (ピーク) のコンバータ・ファミリ
- スイッチング周波数 (PWM): 2.25MHz
- 同期周波数: 1.8MHz~4MHz
- 強制 PWM または PWM/PFM 動作
- 静止電流: 17 $\mu\text{A}$  (標準値)
- 最大 10ms の可変ソフト・スタート
- 高精度の ENABLE 入力:
  - ユーザー定義の低電圧誤動作防止機能
  - 正確なシーケンシング
- 100% デューティ・サイクル・モード
- アクティブ出力放電
- ウィンドウ・コンパレータを使用したパワー・グッド出力
- 選択可能な補償機能を備えたデバイスについては、[TPS628501](#) をご覧ください。

## 2 アプリケーション

- モーター・ドライブ
- ファクトリ・オートメーション / 制御
- ビル・オートメーション
- 試験 / 測定機器
- マルチファンクション・プリンタ (MFP)
- 汎用 POL



概略回路図

## 3 説明

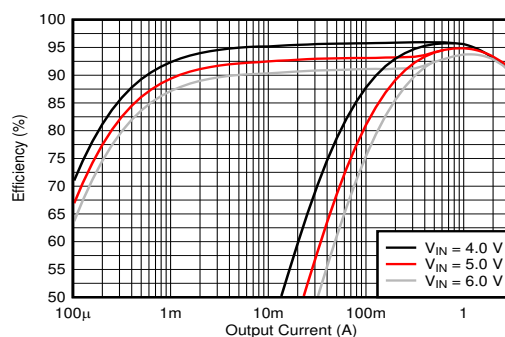
TPS62851x はピン互換で 0.5A、1A、2A (連続) および 3A (ピーク) の高効率で使いやすい同期整流降圧 DC/DC コンバータ・ファミリです。これらのデバイスは、ピーク電流モードの制御トポロジを基礎としています。低抵抗のスイッチにより、最大 2A の連続出力電流、3A のピーク電流を供給できます。スイッチング周波数は内部で 2.25MHz に固定されており、1.8MHz~4MHz の範囲の外部クロックに同期することもできます。PWM/PFM モードでは、TPS62851x は負荷が軽いときに自動的にパワーセーブ・モードへ移行するため、負荷範囲全体にわたって高い効率が維持されます。TPS62851x は PWM モードで 1% の出力電圧精度を実現しているため、出力電圧精度の高い電源の設計に役立ちます。SS/TR ピンを使用すると、起動時間を設定し、または出力電圧が外部電圧源に追従するように構成できるため、各種電源レールを外部からシーケンシングし、起動時の突入電流を制限できます。

TPS62851x は 8 ピンの 1.60mm x 2.10mm SOT583 パッケージで供給され、高電力密度のソリューションを実現できます。

### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
TPS628510	SOT583	1.60mm × 2.10mm (ピンを含む)
TPS628511		
TPS628512		
TPS628513		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と  $I_{OUT}$  との関係、 $V_{OUT} = 3.3\text{V}$



## Table of Contents

<b>1 特長</b> .....	<b>1</b>	9.4 Device Functional Modes.....	<b>11</b>
<b>2 アプリケーション</b> .....	<b>1</b>	<b>10 Application and Implementation</b> .....	<b>14</b>
<b>3 説明</b> .....	<b>1</b>	10.1 Application Information.....	14
<b>4 Revision History</b> .....	<b>2</b>	10.2 Typical Application.....	15
<b>5 Device Comparison Table</b> .....	<b>3</b>	10.3 System Examples.....	26
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	<b>11 Power Supply Recommendations</b> .....	<b>28</b>
<b>7 Specifications</b> .....	<b>5</b>	<b>12 Layout</b> .....	<b>29</b>
7.1 Absolute Maximum Ratings.....	5	12.1 Layout Guidelines.....	29
7.2 ESD Ratings.....	5	12.2 Layout Example.....	29
7.3 Recommended Operating Conditions.....	5	<b>13 Device and Documentation Support</b> .....	<b>30</b>
7.4 Thermal Information.....	6	13.1 Device Support.....	30
7.5 Electrical Characteristics.....	6	13.2 Receiving Notification of Documentation Updates.....	30
7.6 Typical Characteristics.....	8	13.3 サポート・リソース.....	30
<b>8 Parameter Measurement Information</b> .....	<b>9</b>	13.4 Trademarks.....	30
8.1 Schematic.....	9	13.5 Electrostatic Discharge Caution.....	30
<b>9 Detailed Description</b> .....	<b>10</b>	13.6 Glossary.....	30
9.1 Overview.....	10	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>31</b>
9.2 Functional Block Diagram.....	10		
9.3 Feature Description.....	10		

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision A (March 2021) to Revision B (June 2022)</b>	<b>Page</b>
• TPS628513 を追加.....	<b>1</b>
<b>Changes from Revision * (August 2020) to Revision A (March 2021)</b>	<b>Page</b>
• デバイス・ステータスを「事前情報」から「量産データ」に変更.....	<b>1</b>

## 5 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	V <sub>OUT</sub> DISCHARGE	FOLDBACK CURRENT LIMIT	TYPICAL OUTPUT CAPACITOR	SOFT START	OUTPUT VOLTAGE	PACKAGE TYPE
TPS628510DRLR	0.5 A	ON	OFF	2 × 10 µF	External capacitor on the SS/TR pin	Adjustable	DRL
TPS628511DRLR	1 A	ON	OFF	2 × 10 µF	External capacitor on the SS/TR pin	Adjustable	DRL
TPS628512DRLR	2 A	ON	OFF	2 × 10 µF	External capacitor on the SS/TR pin	Adjustable	DRL
TPS628513DRLR	3 A	ON	OFF	2 × 10 µF	External capacitor on the SS/TR pin	Adjustable	DRL
TPS6285010MQDYCRQ1 <sup>(1)</sup>	1A	ON	OFF	2 × 10 µF	Internal 1 ms	Fixed 1.8 V	DYC
TPS62850140QDYCRQ1 <sup>(1)</sup>	1A	ON	ON	2 × 10 µF	Internal 1 ms	Adjustable	DYC
TPS62850240QDYCRQ1 <sup>(1)</sup>	2A	ON	ON	2 × 10 µF	Internal 1 ms	Adjustable	DYC

(1) Preview

## 6 Pin Configuration and Functions

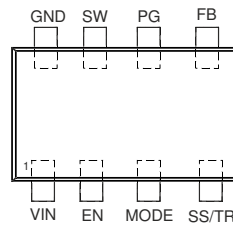


図 6-1. 8-Pin SOT583 DRL Package (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	This is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB	5	I	Voltage feedback input. Connect the resistive output voltage divider to this pin.
GND	8		Ground pin
MODE/SYNC	3	I	The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external frequency. See <a href="#">セクション 7.5</a> for the detailed specification for the digital signal applied to this pin for external synchronization.
PG	6	O	Open-drain power-good output
SS/TR	4	I	Soft-Start / Tracking pin. An external capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing - see <a href="#">セクション 10.3.1</a> in this data sheet.
SW	7		This is the switch pin of the converter and is connected to the internal power MOSFETs.
VIN	1		Power supply input. Make sure the input capacitor is connected as close as possible between the VIN pin and GND.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Pin voltage <sup>(2)</sup>	V <sub>IN</sub>	−0.3	6.5	V
	SW (DC)	−0.3	V <sub>IN</sub> + 0.3	
	SW (AC, less than 10 ns) <sup>(3)</sup>	−3	10	
	SS/TR, PG	−0.3	V <sub>IN</sub> + 0.3	
	EN, MODE/SYNC, FB	−0.3	6.5	
T <sub>stg</sub>	Storage temperature	−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to the network ground terminal.
- (3) While switching

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage range	2.7		6	V
V <sub>OUT</sub>	Output voltage range	0.6		5.5	V
L	Effective inductance	0.32	0.47	1.2	μH
C <sub>OUT</sub>	Effective output capacitance <sup>(1)</sup>	8	10	200	μF
C <sub>IN</sub>	Effective input capacitance <sup>(1)</sup>	5	10		μF
I <sub>SINK_PG</sub>	Sink current at the PG pin	0		2	mA
I <sub>OUT</sub>	Output current, TPS628513 <sup>(2)</sup>	0		3	A
T <sub>J</sub>	Junction temperature	−40		150	°C

- (1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer's DC bias curves for the effective capacitance vs DC voltage applied.
- (2) This part is designed for a 2-A continuous output current at a junction temperature of 105°C or 3-A continuous output current at a junction temperature of 85°C; exceeding the output current or the junction temperature can significantly reduce lifetime.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DRL (JEDEC) <sup>(2)</sup>	DRL (EVM)	UNIT
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.3	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	n/a	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.8	n/a	°C/W
$Y_{JB}$	Junction-to-board characterization parameter	20	n/a	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) JEDEC standard PCB with four layers, no thermal vias

## 7.5 Electrical Characteristics

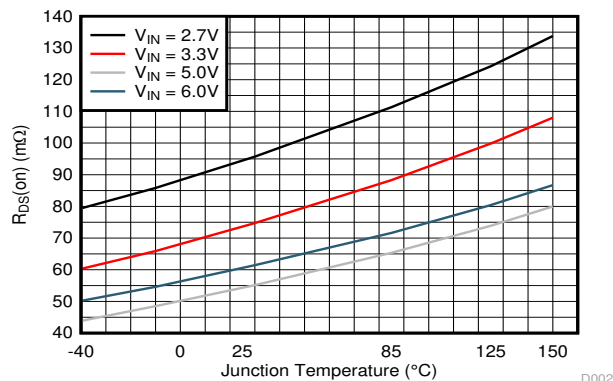
Over operating junction temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ) and  $V_{IN} = 2.7\text{ V}$  to  $6\text{ V}$ . Typical values at  $V_{IN} = 5\text{ V}$  and  $T_J = 25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$I_Q$	Quiescent current	EN = $V_{IN}$ , no load, device not switching, MODE = GND, $V_{OUT} = 0.6\text{ V}$		17	36	$\mu\text{A}$
$I_{SD}$	Shutdown current	EN = GND, nominal value at $T_J = 25^{\circ}\text{C}$ , maximum value at $T_J = 150^{\circ}\text{C}$		1.5	48	$\mu\text{A}$
$V_{UVLO}$	Undervoltage lockout threshold	$V_{IN}$ rising	2.45	2.6	2.7	V
		$V_{IN}$ falling	2.1	2.5	2.6	V
$T_{JSD}$	Thermal shutdown threshold	$T_J$ rising		170		°C
	Thermal shutdown hysteresis	$T_J$ falling		15		°C
<b>CONTROL AND INTERFACE</b>						
$V_{EN,IH}$	Input threshold voltage at EN, rising edge		1.05	1.1	1.15	V
$V_{EN,IL}$	Input threshold voltage at EN, falling edge		0.96	1.0	1.05	V
$V_{IH}$	High-level input-threshold voltage at MODE/SYNC		1.1			V
$I_{EN,LKG}$	Input leakage current into EN	$V_{IH} = V_{IN}$ or $V_{IL} = \text{GND}$			125	nA
$V_{IL}$	Low-level input-threshold voltage at MODE/SYNC				0.3	V
$I_{LKG}$	Input leakage current into MODE/SYNC				100	nA
$t_{Delay}$	Enable delay time	Time from EN high to device starts switching; $V_{IN}$ applied already	85	150	470	$\mu\text{s}$
$t_{Ramp}$	Output voltage ramp time	Time from device starts switching to power good; device not in current limit	0.8	1.3	1.8	ms
$t_{Ramp}$	Output voltage ramp time, SS/TR pin open	Time from device starts switching to power good; device not in current limit	90	150	210	$\mu\text{s}$
$I_{SS/TR}$	SS/TR source current		2	2.5	2.8	$\mu\text{A}$
	Tracking gain	$V_{FB} / V_{SS/TR}$		1		
	Tracking offset	$V_{FB}$ when $V_{SS/TR} = 0\text{ V}$		$\pm 1$		mV
$f_{SYNC}$	Frequency range on MODE/SYNC pin for synchronization		1.8		4	MHz
	Duty cycle of synchronization signal at MODE/SYNC		20%		80%	
	Time to lock to external frequency			50		$\mu\text{s}$
$V_{TH\_PG}$	UVP power-good threshold voltage; DC level	Rising ( $\%V_{FB}$ )	92%	95%	98%	

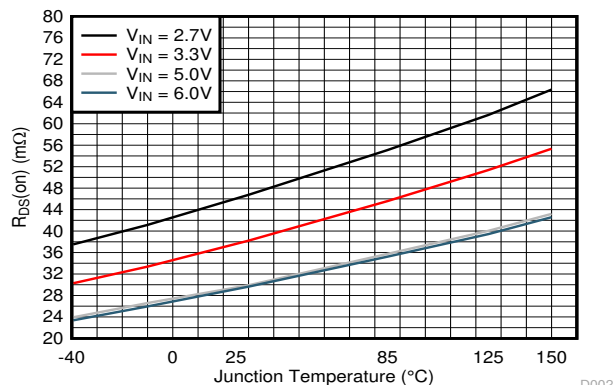
Over operating junction temperature range ( $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ) and  $V_{IN} = 2.7\text{ V}$  to  $6\text{ V}$ . Typical values at  $V_{IN} = 5\text{ V}$  and  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TH\_PG}$	UVP power-good threshold voltage; DC level	Falling ( $\%V_{FB}$ )	87%	90%	93%	
$V_{TH\_PG}$	OVP power-good threshold voltage; DC level	Rising ( $\%V_{FB}$ )	107%	110%	113%	
	OVP power-good threshold voltage; DC level	Falling ( $\%V_{FB}$ )	104%	107%	111%	
$V_{PG\_OL}$	Low-level output voltage at PG	$I_{SINK\_PG} = 2\text{ mA}$		0.07	0.3	V
$I_{PG\_LKG}$	Input leakage current into PG	$V_{PG} = 5\text{ V}$			100	nA
$t_{PG}$	PG deglitch time	For a high level to low level transition on the power-good output		40		$\mu\text{s}$
<b>OUTPUT</b>						
$V_{FB}$	Feedback voltage, adjustable version			0.6		V
$I_{FB\_LKG}$	Input leakage current into FB, adjustable version	$V_{FB} = 0.6\text{ V}$		1	70	nA
$V_{FB}$	Feedback voltage accuracy	PWM, $V_{IN} \geq V_{OUT} + 1\text{ V}$	-1%		1%	
$V_{FB}$	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT} + 1\text{ V}$ , $V_{OUT} \geq 1.0\text{ V}$ , $C_{o,eff} \geq 10\text{ }\mu\text{F}$ , $L = 0.47\text{ }\mu\text{H}$	-1%		2%	
$V_{FB}$	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT} + 1\text{ V}$ , $V_{OUT} < 1.0\text{ V}$ , $C_{o,eff} \geq 15\text{ }\mu\text{F}$ , $L = 0.47\text{ }\mu\text{H}$	-1%		3%	
$V_{FB}$	Feedback voltage accuracy with voltage tracking	$V_{IN} \geq V_{OUT} + 1\text{ V}$ , $V_{SS/TR} = 0.3\text{ V}$	-4%		4%	
	Load regulation	PWM		0.05		%/A
	Line regulation	PWM, $I_{OUT} = 1\text{ A}$ , $V_{IN} \geq V_{OUT} + 1\text{ V}$		0.02		%/V
$R_{DIS}$	Output discharge resistance				100	$\Omega$
$f_{SW}$	PWM switching frequency		2.025	2.25	2.475	MHz
$t_{on,min}$	Minimum on time of high-side FET	$V_{IN} = 3.3\text{ V}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$		35	52	ns
$t_{on,min}$	Minimum on time of low-side FET			10		ns
$R_{DS(ON)}$	High-side FET on-resistance	$V_{IN} \geq 5\text{ V}$		65	120	m $\Omega$
	Low-side FET on-resistance	$V_{IN} \geq 5\text{ V}$		33	70	m $\Omega$
	High-side MOSFET leakage current			0.01	44	$\mu\text{A}$
	Low-side MOSFET leakage current			0.01	70	$\mu\text{A}$
	SW leakage	$V(SW) = 0.6\text{ V}$ , current into SW	-0.05		11	$\mu\text{A}$
$I_{LIMH}$	High-side FET switch current limit	DC value, for TPS628513; $V_{IN} = 3\text{ V}$ to $6\text{ V}$	3.45	4.5	5.1	A
$I_{LIMH}$	High-side FET switch current limit	DC value, for TPS628512; $V_{IN} = 3\text{ V}$ to $6\text{ V}$	2.85	3.4	3.9	A
$I_{LIMH}$	High-side FET switch current limit	DC value, for TPS628511; $V_{IN} = 3\text{ V}$ to $6\text{ V}$	2.1	2.6	3.0	A
$I_{LIMH}$	High-side FET switch current limit	DC value, for TPS628510; $V_{IN} = 3\text{ V}$ to $6\text{ V}$	1.6	2.1	2.5	A
$I_{LIMNEG}$	Low-side FET negative current limit	DC value		-1.8		A

## 7.6 Typical Characteristics



7-1.  $R_{DS(on)}$  of High-Side Switch



7-2.  $R_{DS(on)}$  of Low-Side Switch



## 8 Parameter Measurement Information

### 8.1 Schematic

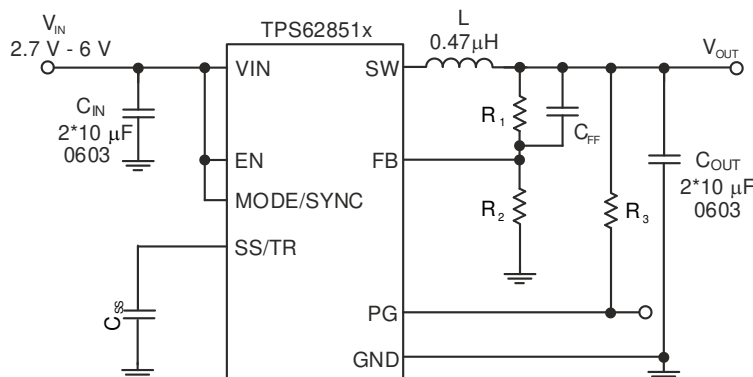


图 8-1. Measurement Setup

表 8-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER <sup>(1)</sup>
IC	TPS628512	Texas Instruments
L	0.47-μH inductor DFE201210U	Murata
C <sub>IN</sub>	2 × 10 μF / 6.3 V GRM188D70J106MA73	Murata
C <sub>OUT</sub>	2 × 10 μF / 6.3 V GRM188D70J106MA73 for V <sub>OUT</sub> ≥ 1 V	Murata
C <sub>OUT</sub>	3 × 10 μF / 6.3 V GRM188D70J106MA73 for V <sub>OUT</sub> < 1 V	Murata
C <sub>SS</sub>	4.7 nF (equal to 1-ms start-up ramp); GCM188R72A472KA37	Any
C <sub>FF</sub>	10 pF	Any
R <sub>1</sub>	Depending on V <sub>OUT</sub>	Any
R <sub>2</sub>	Depending on V <sub>OUT</sub>	Any
R <sub>3</sub>	100 kΩ	Any

(1) See the [Third-Party Products Disclaimer](#).

## 9 Detailed Description

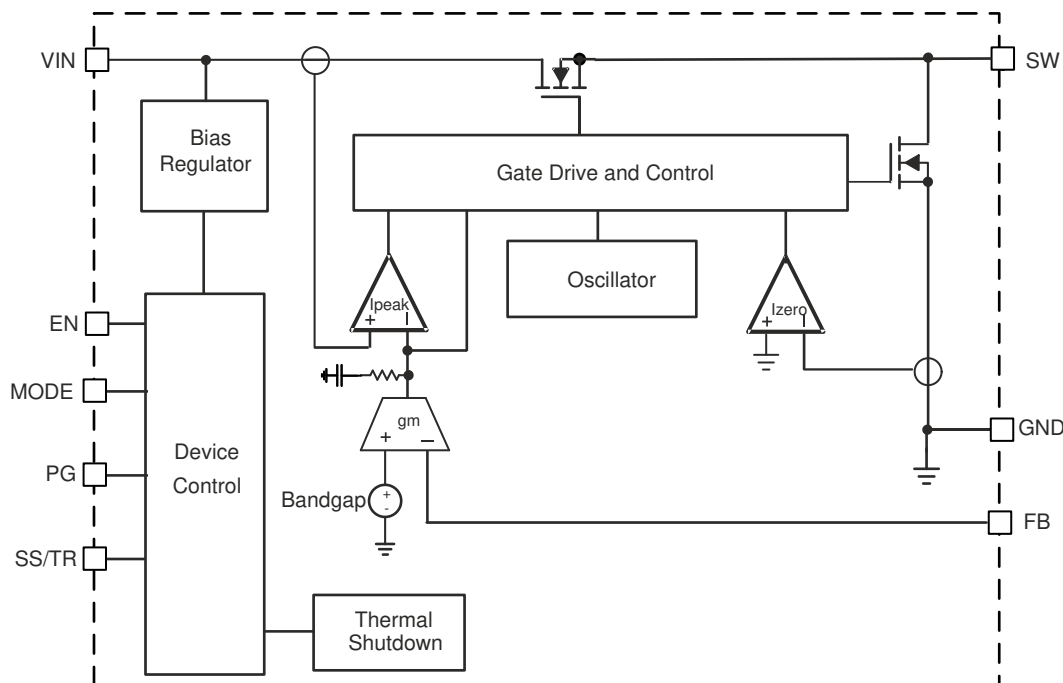
### 9.1 Overview

The TPS62851x synchronous switch mode power converters are based on a peak current mode control topology. The control loop is internally compensated.

The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors. The devices can be operated without a feedforward capacitor on the output voltage divider, however, using a typically 10-pF feedforward capacitor improves transient response.

The devices support forced fixed frequency PWM operation with the MODE pin tied to a logic high level. The frequency is defined as 2.25 MHz internally fixed. Alternatively, the devices can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz, applied to the MODE pin with no need for additional passive components. An internal PLL allows you to change from internal clock to external clock during operation. The synchronization to the external clock is done on a falling edge of the clock applied at MODE to the rising edge on the SW pin. This allows a roughly 180° phase shift when the SW pin is used to generate the synchronization signal for a second converter. When the MODE pin is set to a logic low level, the device operates in power save mode (PFM) at low output current and automatically transfers to fixed frequency PWM mode at higher output current. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Precise Enable (EN)

The voltage applied at the enable pin of the TPS62851x is compared to a fixed threshold of 1.1 V for a rising voltage. This allows you to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS62851x starts operation when the rising threshold is exceeded. For proper operation, the enable (EN) pin must be terminated and must not be left floating. Pulling the enable pin low forces the device into shutdown, with

a shutdown current of typically 1  $\mu$ A. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

### 9.3.2 MODE / SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin allows you to force PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. The specifications for the minimum on-time and minimum off-time have to be observed when setting the external frequency. The external clock must be set to about 2.25 MHz initially and then increased or decreased to the desired frequency. This ensures a low distortion of the output voltage when the external frequency is applied.

### 9.3.3 Spread Spectrum Clocking (SSC)

If interested in this option, please contact Texas Instruments. The device offers spread spectrum clocking as an option. When SSC is enabled, the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288 kHz above the nominal switching frequency. When the device is externally synchronized by applying a clock signal to the MODE/SYNC pin, the TPS62851x follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

### 9.3.4 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents misoperation of the device by switching off both the power FETs. When enabled, the device is fully operational for input voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

### 9.3.5 Power Good Output (PG)

Power good is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. It is driven by a window comparator. PG is held low when the device is disabled, in undervoltage lockout in thermal shutdown, and not in soft start. When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the output is high impedance.

$V_{IN}$  must remain present for the PG pin to stay low. If the power good output is not used, it is recommended to tie to GND or leave open. The PG indicator features a de-glitch, as specified in the electrical characteristics, for the transition from "high impedance" to "low" of its output.

**表 9-1. PG Status**

EN	DEVICE STATUS	PG STATE
X	$V_{IN} < 2\text{ V}$	undefined
low	$V_{IN} \geq 2\text{ V}$	low
high	$2\text{ V} \leq V_{IN} \leq \text{UVLO}$ OR in thermal shutdown OR $V_{OUT}$ not in regulation OR device in soft start	low
high	$V_{OUT}$ in regulation	high impedance

### 9.3.6 Thermal Shutdown

The junction temperature ( $T_J$ ) of the device is monitored by an internal temperature sensor. If  $T_J$  exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When  $T_J$  decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During a PFM pause, the thermal shutdown is not active. After a PFM pause, the device needs up to 9  $\mu$ s to detect a junction temperature that is too high. If the PFM burst is shorter than this delay, the device does not detect a junction temperature that is too high.

## 9.4 Device Functional Modes

### 9.4.1 Pulse Width Modulation (PWM) Operation

The TPS62851x has two operating modes: forced PWM mode, which is discussed in this section, and PWM/PFM as discussed in [セクション 9.4.2](#).

With the MODE/SYNC pin set to high, the TPS62851x operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is 2.25 MHz or defined by an external clock signal applied to the MODE/SYNC pin. With an external clock applied to MODE/SYNC, the TPS62851x follow the frequency applied to the pin. In general, the frequency range in forced PWM mode is 1.8 MHz to 4 MHz. However, the frequency needs to be in a range the TPS62851x can operate at, taking the minimum on-time into account.

#### 9.4.2 Power Save Mode Operation (PWM/PFM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 0.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency.

#### 9.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as  $D = V_{OUT} / V_{IN}$ . The duty cycle increases as the input voltage comes close to the output voltage and the off-time gets smaller. When the minimum off-time of typically 10 ns is reached, the TPS62851x skips switching cycles while it approaches 100% mode. In 100% mode, it keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. In 100% mode, the low-side switch is turned off. The maximum dropout voltage in 100% mode is the product of the on-resistance of the high-side switch plus the series resistance of the inductor and the load current.

#### 9.4.4 Current Limit and Short Circuit Protection

The TPS62851x is protected against overload and short circuit events. If the inductor current exceeds the current limit  $I_{LIMH}$ , the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side switch turns on again only if the current in the low side-switch has decreased below the low side current limit. Due to internal propagation delay, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \cdot t_{PD} \quad (1)$$

where

- $I_{LIMH}$  is the static current limit as specified in the electrical characteristics
- $L$  is the effective inductance at the peak current
- $V_L$  is the voltage across the inductor ( $V_{IN} - V_{OUT}$ )
- $t_{PD}$  is the internal propagation delay of typically 50 ns

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \cdot 50ns \quad (2)$$

#### 9.4.5 Foldback Current Limit and Short Circuit Protection

This is valid for devices where foldback current limit is enabled. If interested in this option, please contact Texas Instruments.

When the device detects current limit for more than 1024 subsequent switching cycles, it reduces the current limit from its nominal value to typically 1.3 A. Foldback current limit is left when the current limit indication goes away. If device operation continues in current limit, it would, after 3072 switching cycles, try for full current limit again for 1024 switching cycles.

#### 9.4.6 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled and to keep the output voltage close to 0 V when the device is off. The output discharge feature

is only active once the TPS62851x have been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V. Output discharge is not activated during a current limit or foldback current limit event.

#### 9.4.7 Soft Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay of about 200 µs, then the internal reference and hence  $V_{OUT}$  rises with a slope controlled by an external capacitor connected to the SS/TR pin.

Leaving the SS/TR pin un-connected provides the fastest start-up ramp with 160 µs typically. A capacitor connected from SS/TR to GND is charged with 2.5 µA by an internal current source during soft start until it reaches the reference voltage of 0.6 V. The capacitance required to set a certain ramp-time ( $t_{ramp}$ ) therefore is:

$$C_{SS}[nF] = \frac{2.5\mu A \cdot t_{ramp}[ms]}{0.6V} \quad (3)$$

If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin to GND to ensure a proper low level. Returning from those states causes a new start-up sequence.

A voltage applied at SS/TR can be used to track a master voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current. The SS/TR pin must not be connected to the SS/TR pin of other devices. The maximum value for  $C_{SS}$  is 47 nF to ensure proper discharge before the device starts to ramp the output voltage.

#### 9.4.8 Input Overvoltage Protection

When the input voltage exceeds the absolute maximum rating, the device is set to PFM mode so it cannot transfer energy from the output to the input.

## 10 Application and Implementation

### Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 10.1 Application Information

#### 10.1.1 Programming the Output Voltage

The output voltage of the TPS62851x is adjustable. It can be programmed for output voltages from 0.6 V to 5.5 V using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from [Equation 6](#). It is recommended to choose resistor values that allow a current of at least 2 µA, meaning the value of R<sub>2</sub> must not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2 \cdot \left( \frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (4)$$

#### 10.1.2 Inductor Selection

The TPS62851x is designed for a nominal 0.47-µH inductor with a switching frequency of typically 2.25 MHz. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 0.47 µH cause a larger inductor current ripple which causes larger negative inductor current in forced PWM mode at low or no output current. For a higher or lower nominal switching frequency, the inductance must be changed accordingly. See [セクション 7.3](#) for details.

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PFM transition point, and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). [式 5](#) calculates the maximum inductor current.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (5)$$

$$\Delta I_{L(max)} = \frac{V_{OUT} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}{L_{min}} \cdot \frac{1}{f_{SW}} \quad (6)$$

where

- I<sub>L(max)</sub> is the maximum inductor current
- ΔI<sub>L(max)</sub> is the peak-to-peak inductor ripple current
- L<sub>min</sub> is the minimum inductance at the operating point

**表 10-1. Typical Inductors**

TYPE	INDUCTANCE [μH]	CURRENT [A] (1)	FOR DEVICE	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [LxBxH] mm	MANUFACTURER <sup>(2)</sup>
DFE201210U-R47M	0.47 μH, ±20%	see data sheet	TPS628510/511 / 512	2.25 MHz	2.0 x 1.2 x 1.0	Murata
DFE201210U-1R0M	1 μH, ±20%	see data sheet	TPS628510/511 / 512	2.25 MHz	2.0x 1.2 x 1.0	Murata
DFE201210U-R68	0.68 μH, ±20%	see data sheet	TPS628510/511 / 512	2.25 MHz	2.0x 1.2 x 1.0	Murata
XEL3515-561ME	0.56 μH, ±20%	4.5	TPS628510/511 / 512	2.25 MHz	3.5 x 3.2 x 1.5	Coilcraft
XFL4015-701ME	0.70 μH, ±20%	3.3	TPS628510/511 / 512	2.25 MHz	4.0 x 4.0 x 1.6	Coilcraft
XFL4015-471ME	0.47 μH, ±20%	3.5	TPS628510/511 / 512	2.25 MHz	4.0 x 4.0 x 1.6	Coilcraft

(1) Lower of  $I_{RMS}$  at 20°C rise or  $I_{SAT}$  at 20% drop.

(2) See the [Third-Party Products Disclaimer](#).

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well.

### 10.1.3 Capacitor Selection

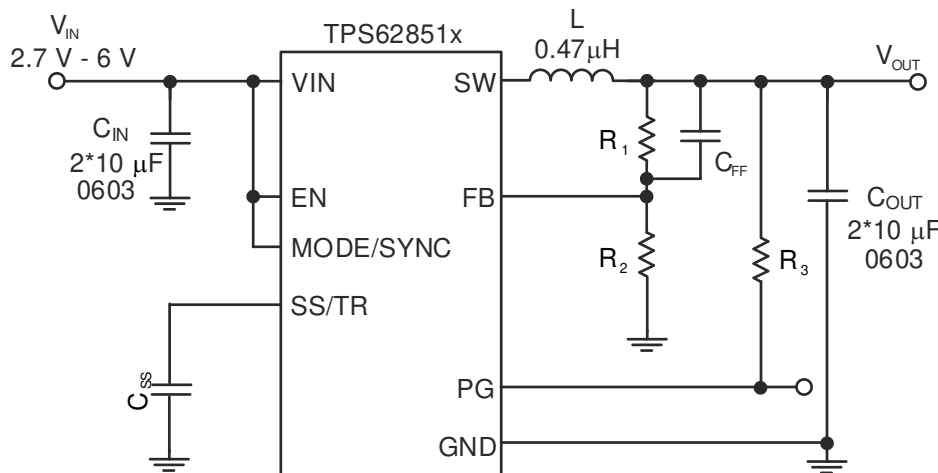
#### 10.1.3.1 Input Capacitor

For most applications, 10-μF nominal is sufficient and is recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins.

#### 10.1.3.2 Output Capacitor

The architecture of the TPS62851x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode.

## 10.2 Typical Application



**图 10-1. Typical Application for Indy**

### 10.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

## 10.2.2 Detailed Design Procedure

$$R_1 = R_2 \cdot \left( \frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (7)$$

With  $V_{FB} = 0.6 \text{ V}$ :

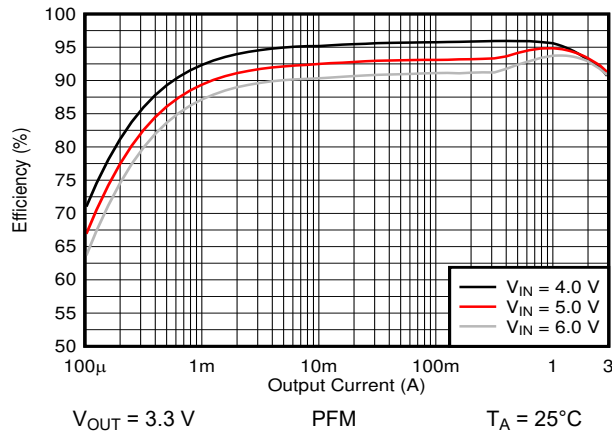
**表 10-2. Setting the Output Voltage**

NOMINAL OUTPUT VOLTAGE $V_{OUT}$	$R_1$	$R_2$	$C_{FF}$	EXACT OUTPUT VOLTAGE
0.8 V	16.9 k $\Omega$	51 k $\Omega$	10 pF	0.7988 V
1.0 V	20 k $\Omega$	30 k $\Omega$	10 pF	1.0 V
1.1 V	39.2 k $\Omega$	47 k $\Omega$	10 pF	1.101 V
1.2 V	68 k $\Omega$	68 k $\Omega$	10 pF	1.2 V
1.5 V	76.8 k $\Omega$	51 k $\Omega$	10 pF	1.5 V
1.8 V	80.6 k $\Omega$	40.2 k $\Omega$	10 pF	1.803 V
2.5 V	47.5 k $\Omega$	15 k $\Omega$	10 pF	2.5 V
3.3 V	88.7 k $\Omega$	19.6 k $\Omega$	10 pF	3.315 V

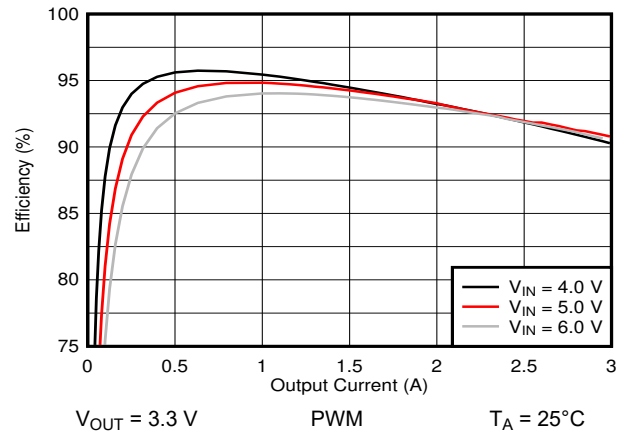


### 10.2.3 Application Curves

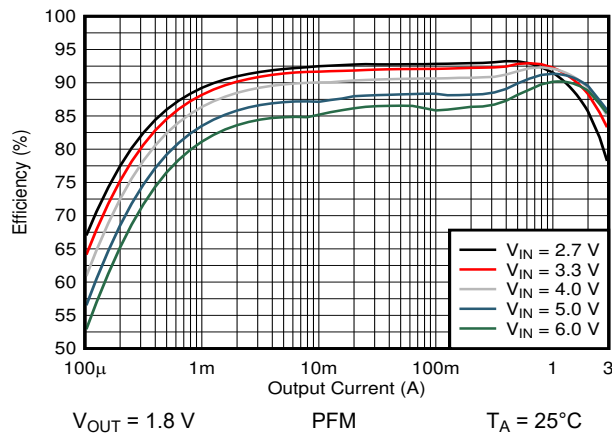
All plots have been taken with a nominal switching frequency of 2.25 MHz when set to PWM mode, unless otherwise noted. The BOM is according to [8-1](#).



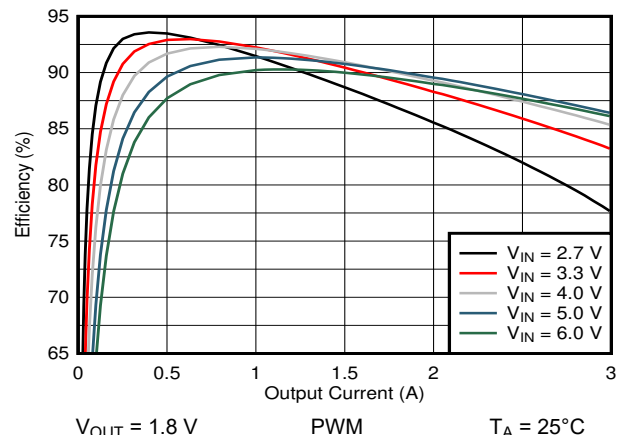
**10-2. Efficiency Versus Output Current**



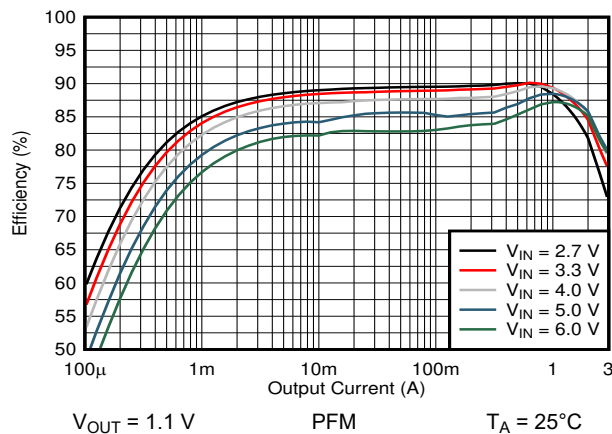
**10-3. Efficiency Versus Output Current**



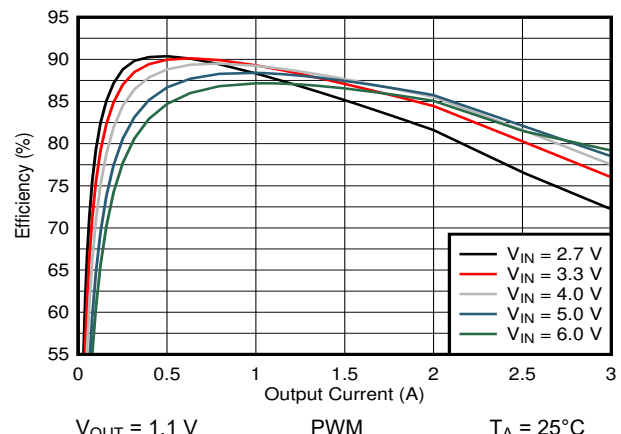
**10-4. Efficiency Versus Output Current**



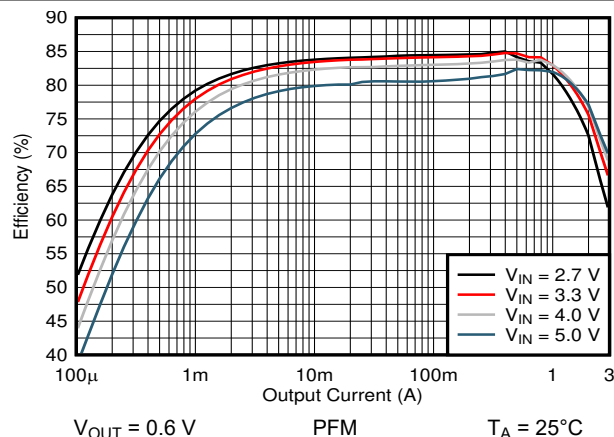
**10-5. Efficiency Versus Output Current**



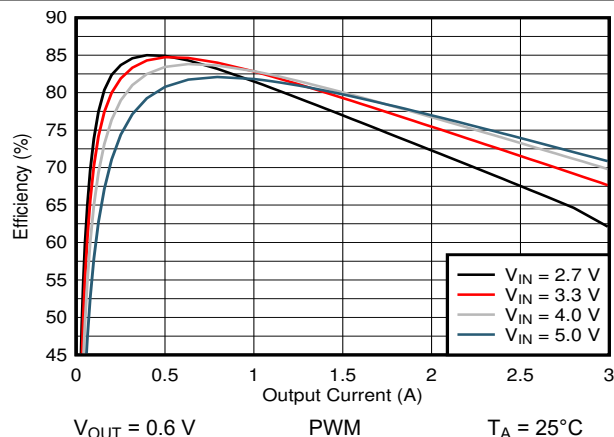
**10-6. Efficiency Versus Output Current**



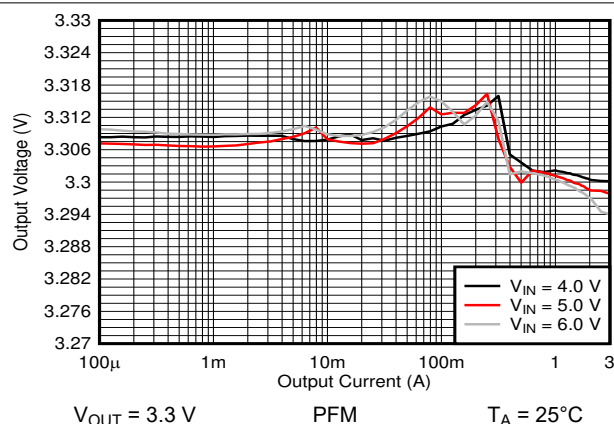
**10-7. Efficiency Versus Output Current**



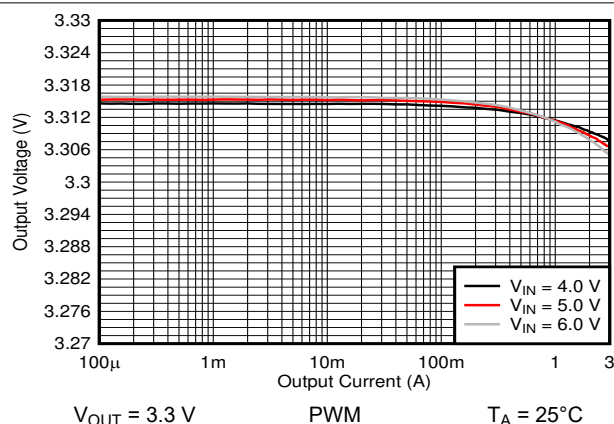
**10-8. Efficiency Versus Output Current**



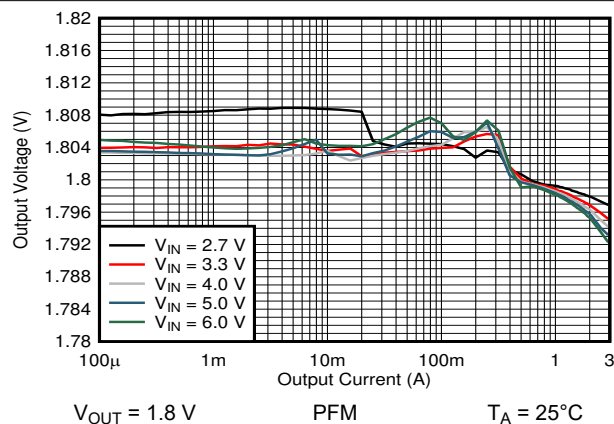
**10-9. Efficiency Versus Output Current**



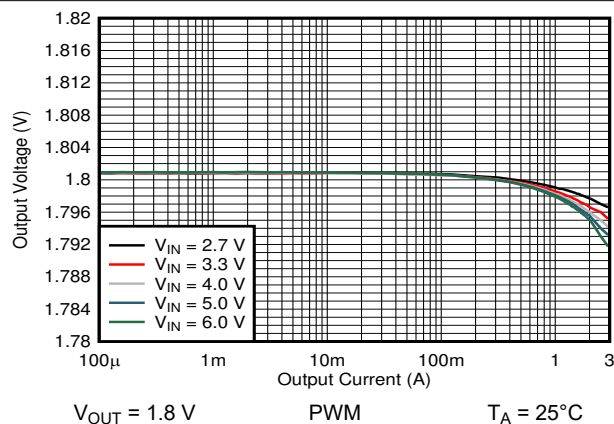
**10-10. Output Voltage Versus Output Current**



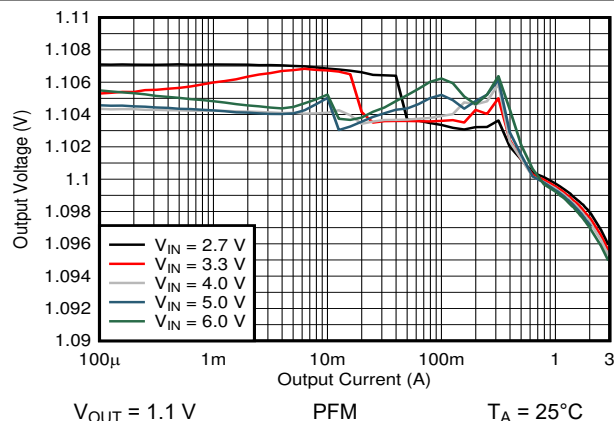
**10-11. Output Voltage Versus Output Current**



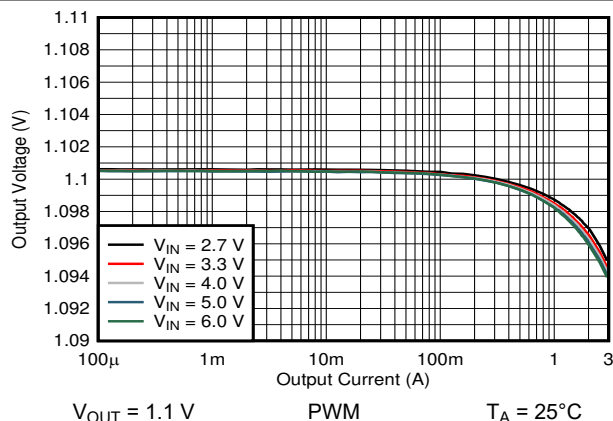
**10-12. Output Voltage Versus Output Current**



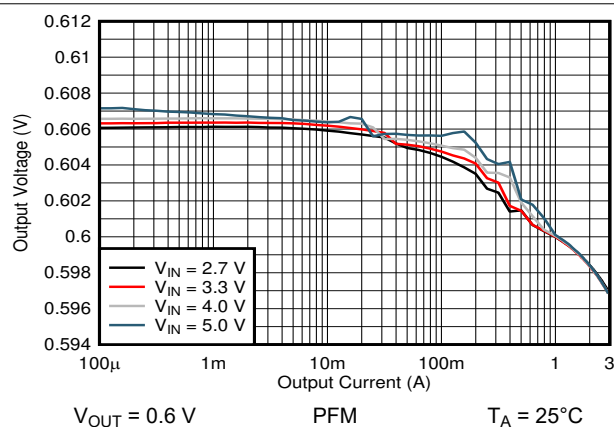
**10-13. Output Voltage Versus Output Current**



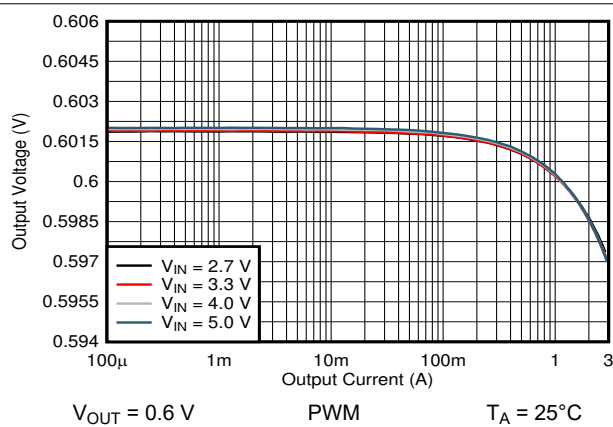
10-14. Output Voltage Versus Output Current



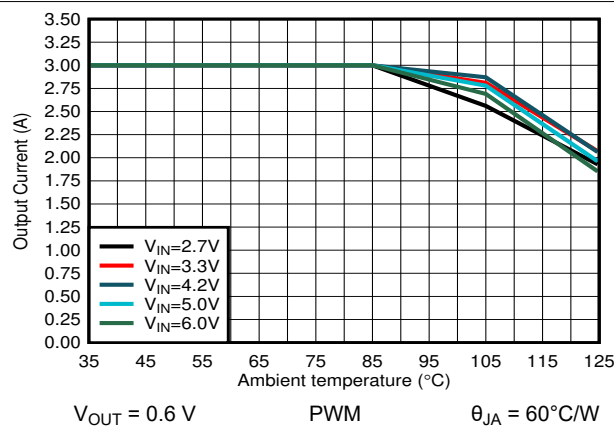
10-15. Output Voltage Versus Output Current



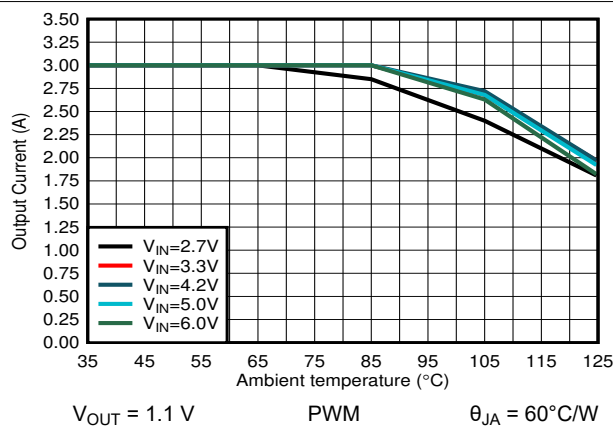
10-16. Output Voltage Versus Output Current



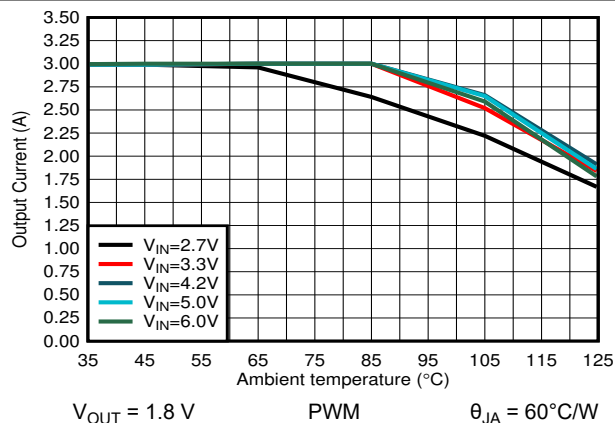
10-17. Output Voltage Versus Output Current



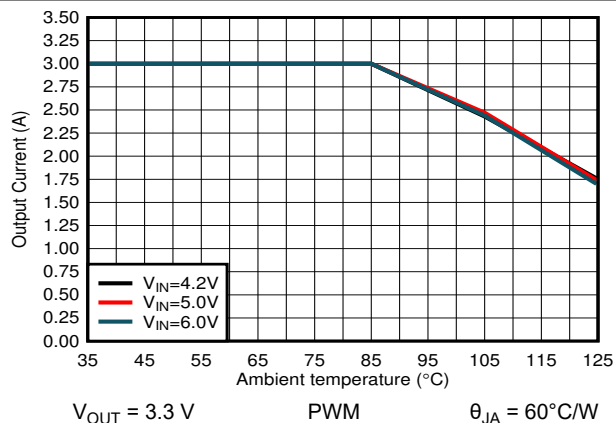
10-18. Output Current Versus Ambient Temperature



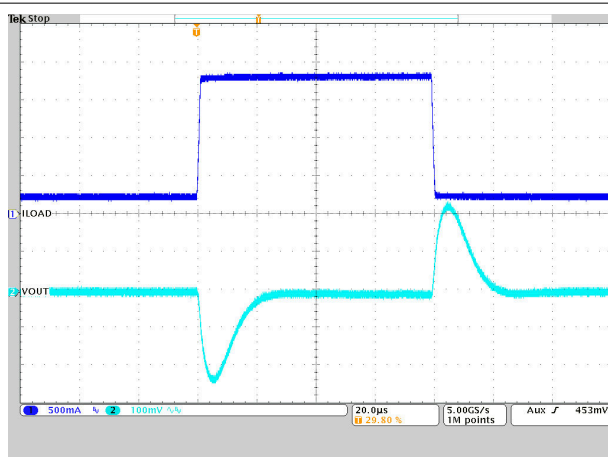
10-19. Output Current Versus Ambient Temperature



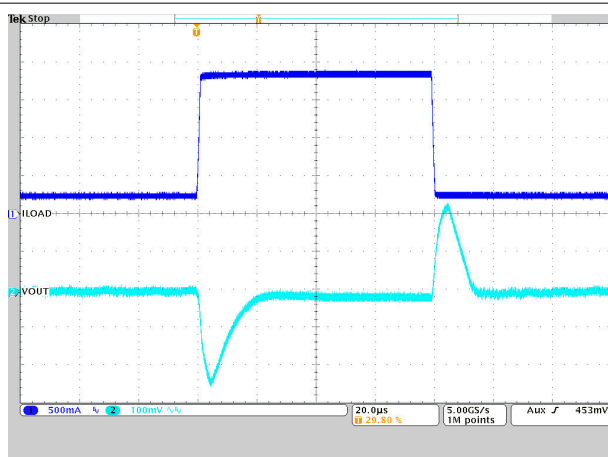
10-20. Output Current Versus Ambient Temperature



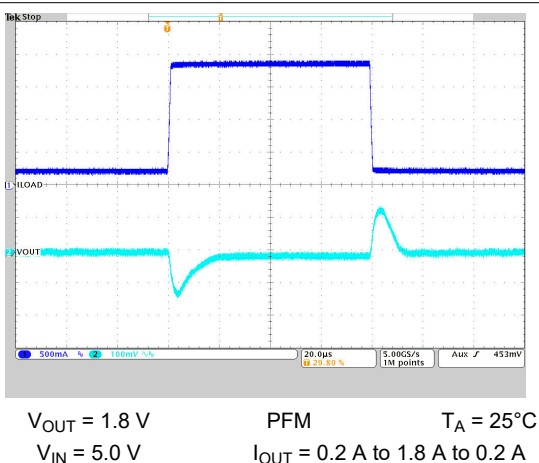
10-21. Output Current Versus Ambient Temperature



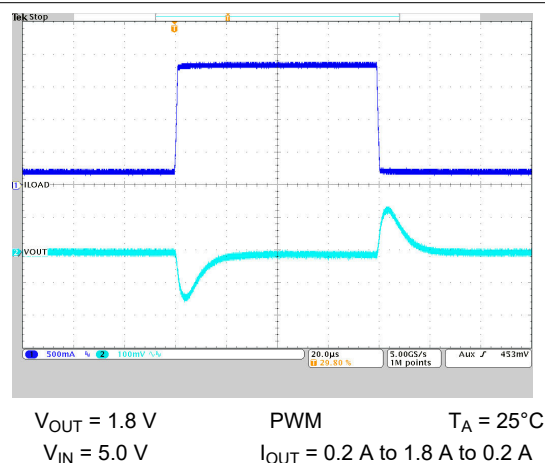
10-22. Load Transient Response



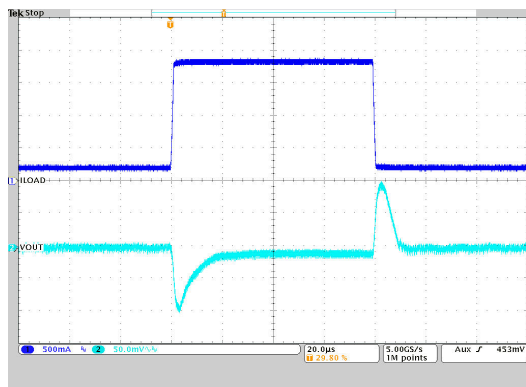
10-23. Load Transient Response



10-24. Load Transient Response

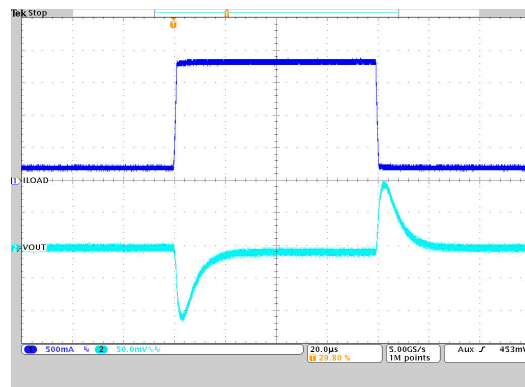


10-25. Load Transient Response



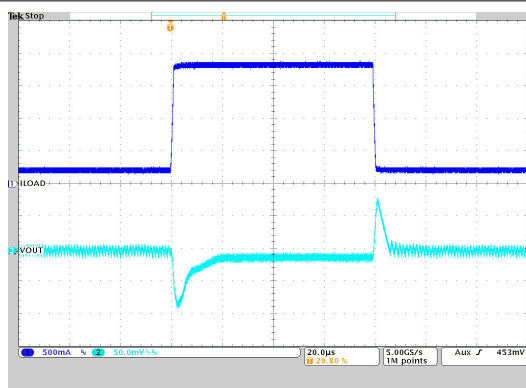
$V_{OUT} = 1.2\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5.0\text{ V}$        $I_{OUT} = 0.2\text{ A to } 1.8\text{ A to } 0.2\text{ A}$

**10-26. Load Transient Response**



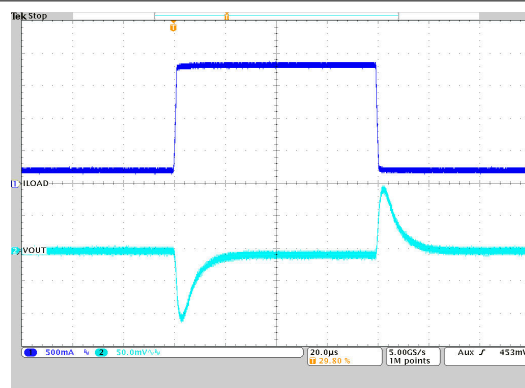
$V_{OUT} = 1.2\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5.0\text{ V}$        $I_{OUT} = 0.2\text{ A to } 1.8\text{ A to } 0.2\text{ A}$

**10-27. Load Transient Response**



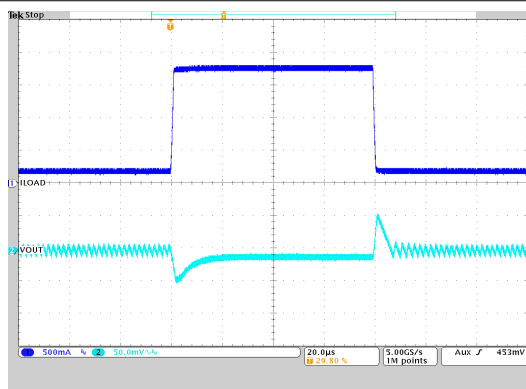
$V_{OUT} = 1.0\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5.0\text{ V}$        $I_{OUT} = 0.2\text{ A to } 1.8\text{ A to } 0.2\text{ A}$

**10-28. Load Transient Response**



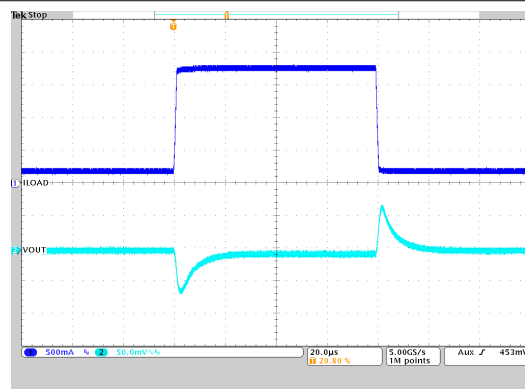
$V_{OUT} = 1.0\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5.0\text{ V}$        $I_{OUT} = 0.2\text{ A to } 1.8\text{ A to } 0.2\text{ A}$

**10-29. Load Transient Response**



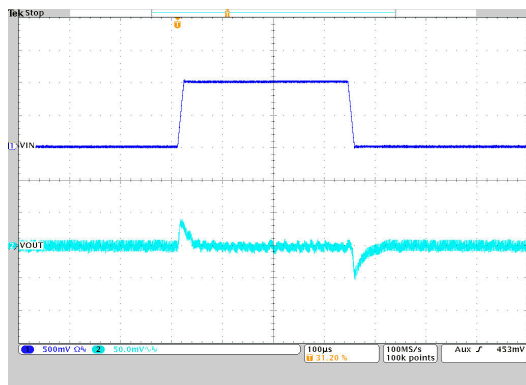
$V_{OUT} = 0.6\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 3.3\text{ V}$        $I_{OUT} = 0.2\text{ A to } 1.8\text{ A to } 0.2\text{ A}$

**10-30. Load Transient Response**



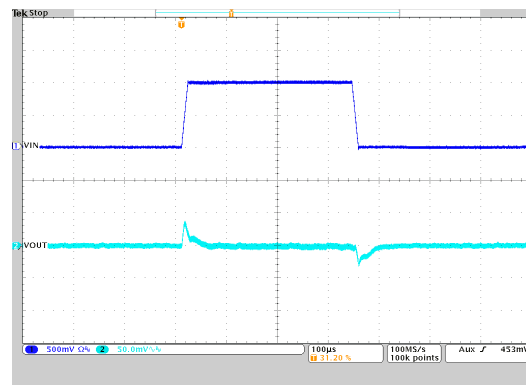
$V_{OUT} = 0.6\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 3.3\text{ V}$        $I_{OUT} = 0.2\text{ A to } 1.8\text{ A to } 0.2\text{ A}$

**10-31. Load Transient Response**



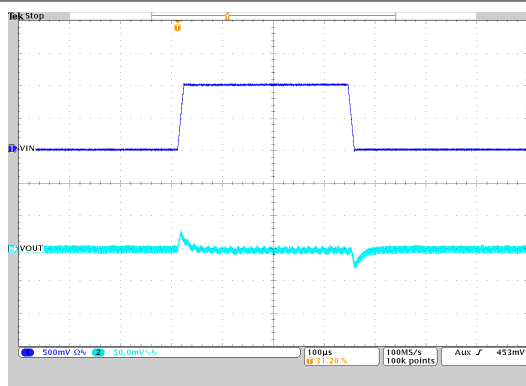
$V_{OUT} = 3.3\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.2\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

 **10-32. Line Transient Response**



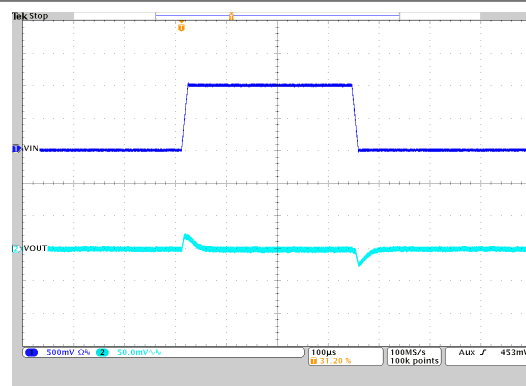
$V_{OUT} = 3.3\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 2\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

 **10-33. Line Transient Response**



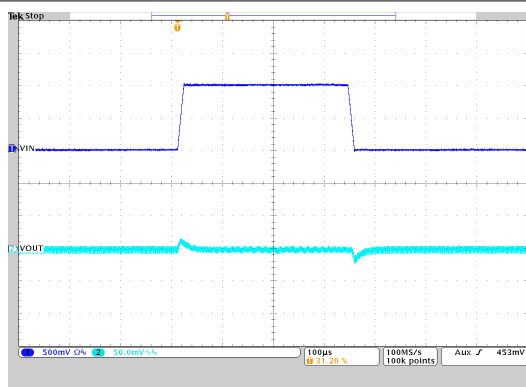
$V_{OUT} = 1.8\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.2\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

 **10-34. Line Transient Response**



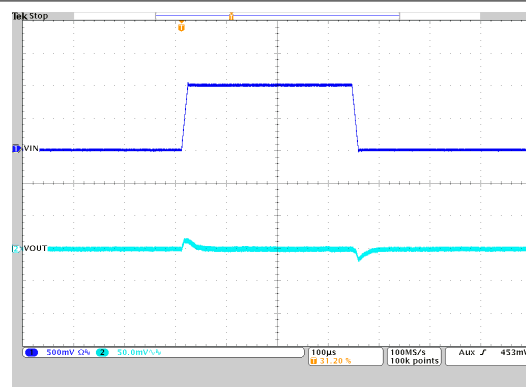
$V_{OUT} = 1.8\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 2\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

 **10-35. Line Transient Response**



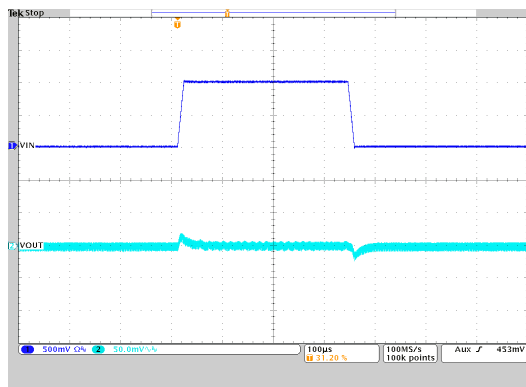
$V_{OUT} = 1.2\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.2\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

 **10-36. Line Transient Response**



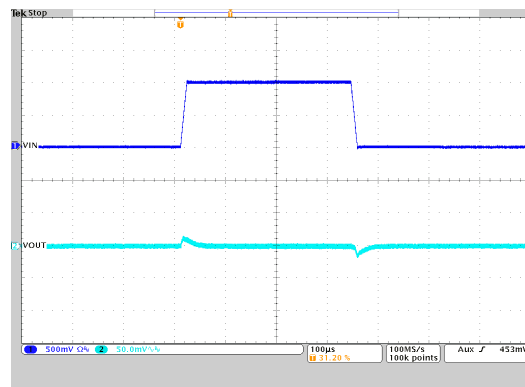
$V_{OUT} = 1.2\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 2\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

 **10-37. Line Transient Response**



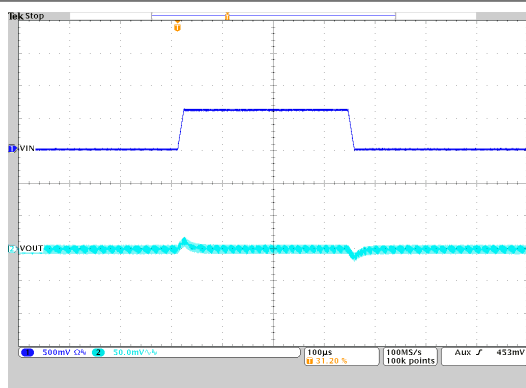
$V_{OUT} = 1.0\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.2\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**FIG 10-38. Line Transient Response**



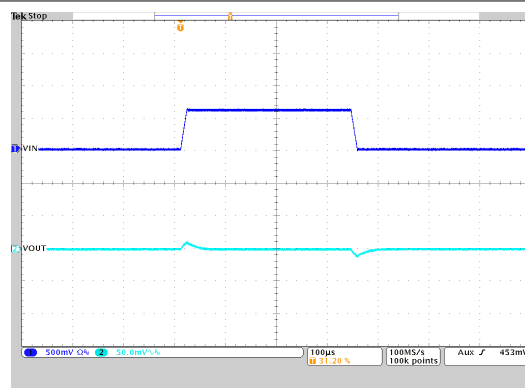
$V_{OUT} = 1.0\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 2\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**FIG 10-39. Line Transient Response**



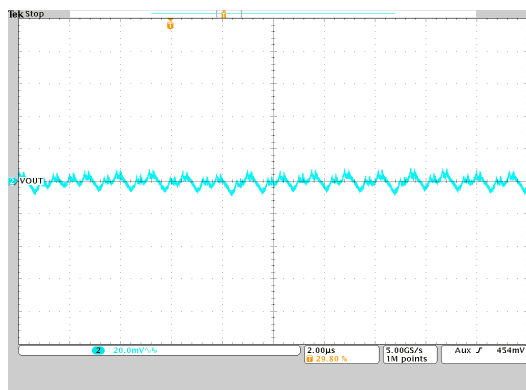
$V_{OUT} = 0.6\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.2\text{ A}$        $V_{IN} = 3.0\text{ V to } 3.6\text{ V to } 3.0\text{ V}$

**FIG 10-40. Line Transient Response**



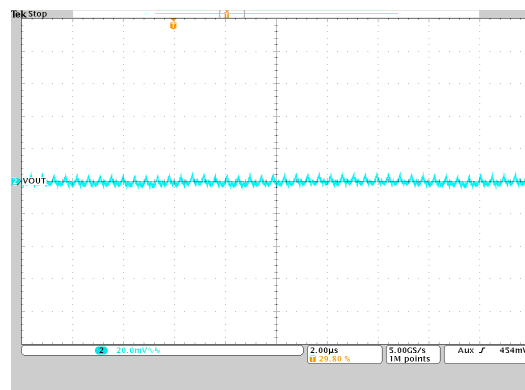
$V_{OUT} = 0.6\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 2\text{ A}$        $V_{IN} = 3.0\text{ V to } 3.6\text{ V to } 3.0\text{ V}$

**FIG 10-41. Line Transient Response**



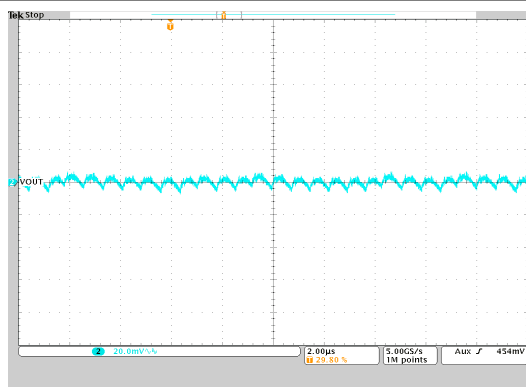
$V_{OUT} = 3.3\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$        $I_{OUT} = 0.2\text{ A}$

**FIG 10-42. Output Voltage Ripple**



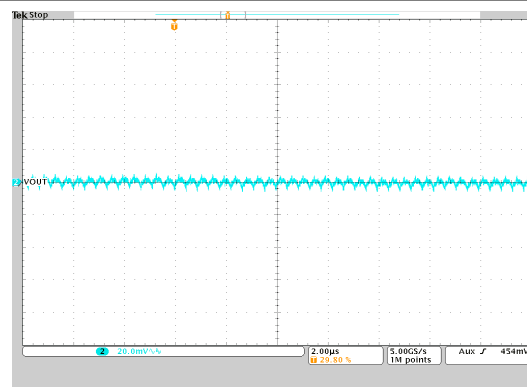
$V_{OUT} = 3.3\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$        $I_{OUT} = 2\text{ A}$

**FIG 10-43. Output Voltage Ripple**



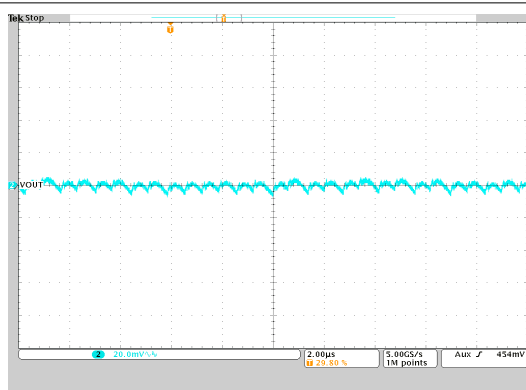
$V_{OUT} = 1.8\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$        $I_{OUT} = 0.2\text{ A}$

**10-44. Output Voltage Ripple**



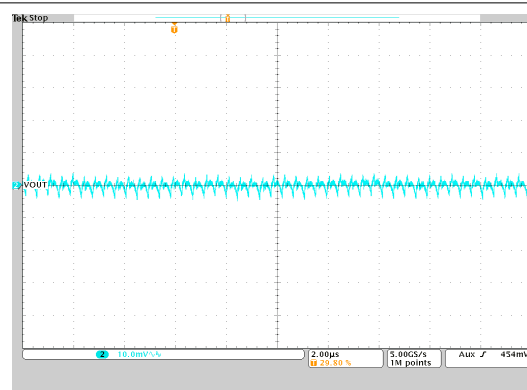
$V_{OUT} = 1.8\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$        $I_{OUT} = 2\text{ A}$

**10-45. Output Voltage Ripple**



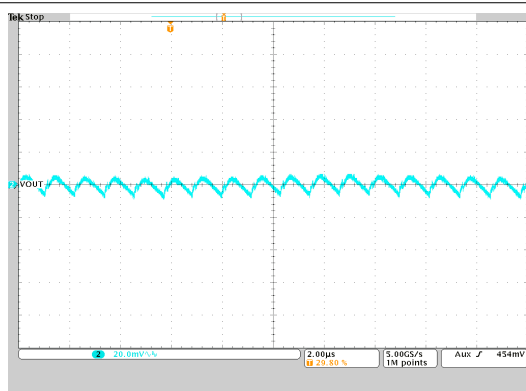
$V_{OUT} = 1.2\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$        $I_{OUT} = 0.2\text{ A}$

**10-46. Output Voltage Ripple**



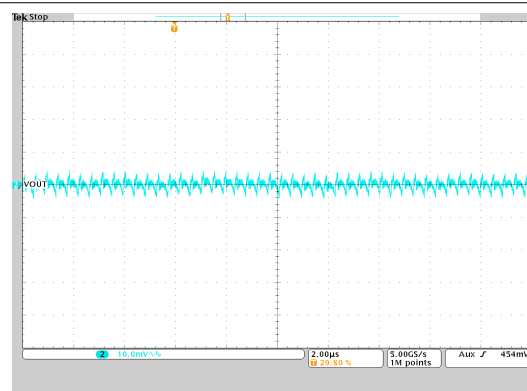
$V_{OUT} = 1.2\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$        $I_{OUT} = 2\text{ A}$

**10-47. Output Voltage Ripple**



$V_{OUT} = 1.0\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$        $I_{OUT} = 0.2\text{ A}$

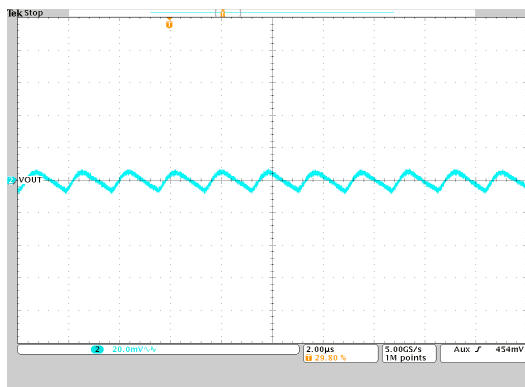
**10-48. Output Voltage Ripple**



$V_{OUT} = 1.0\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$        $I_{OUT} = 2\text{ A}$

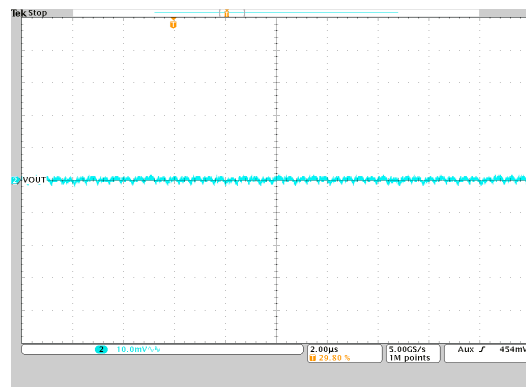
**10-49. Output Voltage Ripple**





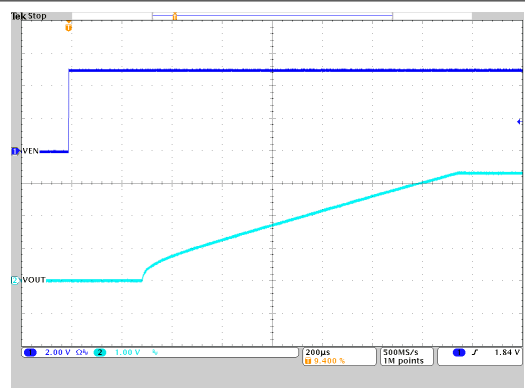
$V_{OUT} = 0.6\text{ V}$  PFM  $T_A = 25^\circ\text{C}$   
 $V_{IN} = 3.3\text{ V}$   $I_{OUT} = 0.2\text{ A}$

**10-50. Output Voltage Ripple**



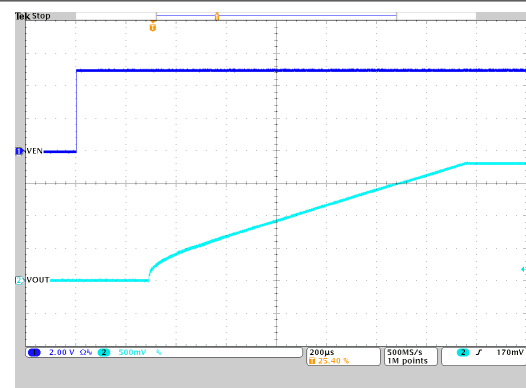
$V_{OUT} = 0.6\text{ V}$  PWM  $T_A = 25^\circ\text{C}$   
 $V_{IN} = 3.3\text{ V}$   $I_{OUT} = 2\text{ A}$

**10-51. Output Voltage Ripple**



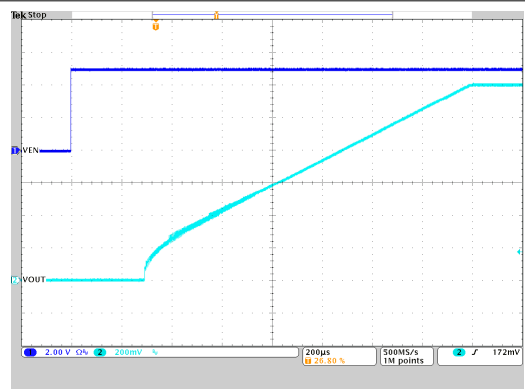
$V_{OUT} = 3.3\text{ V}$  PWM or PFM  $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$   $C_{SS} = 4.7\text{ nF}$   $I_{OUT} = 2\text{ A}$

**10-52. Start-Up Timing**



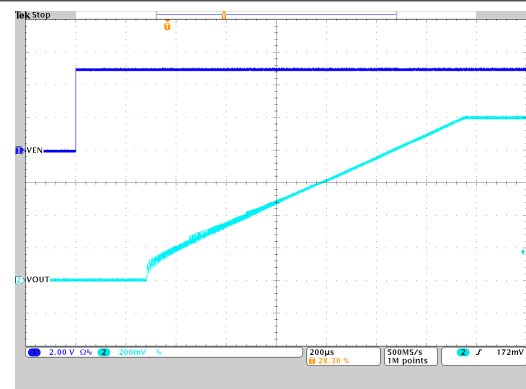
$V_{OUT} = 1.8\text{ V}$  PWM or PFM  $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$   $C_{SS} = 4.7\text{ nF}$   $I_{OUT} = 2\text{ A}$

**10-53. Start-Up Timing**



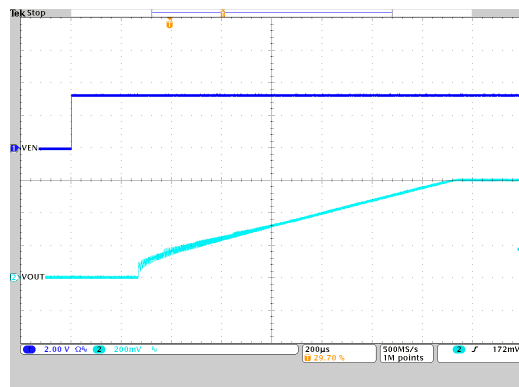
$V_{OUT} = 1.2\text{ V}$  PWM or PFM  $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$   $C_{SS} = 4.7\text{ nF}$   $I_{OUT} = 2\text{ A}$

**10-54. Start-Up Timing**



$V_{OUT} = 1.0\text{ V}$  PWM or PFM  $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5\text{ V}$   $C_{SS} = 4.7\text{ nF}$   $I_{OUT} = 2\text{ A}$

**10-55. Start-Up Timing**

 $V_{OUT} = 0.6\text{ V}$ 

PWM or PFM

 $T_A = 25^\circ\text{C}$  $V_{IN} = 3.3\text{ V}$  $C_{SS} = 4.7\text{ nF}$  $I_{OUT} = 2\text{ A}$ **FIG 10-56. Start-Up Timing**

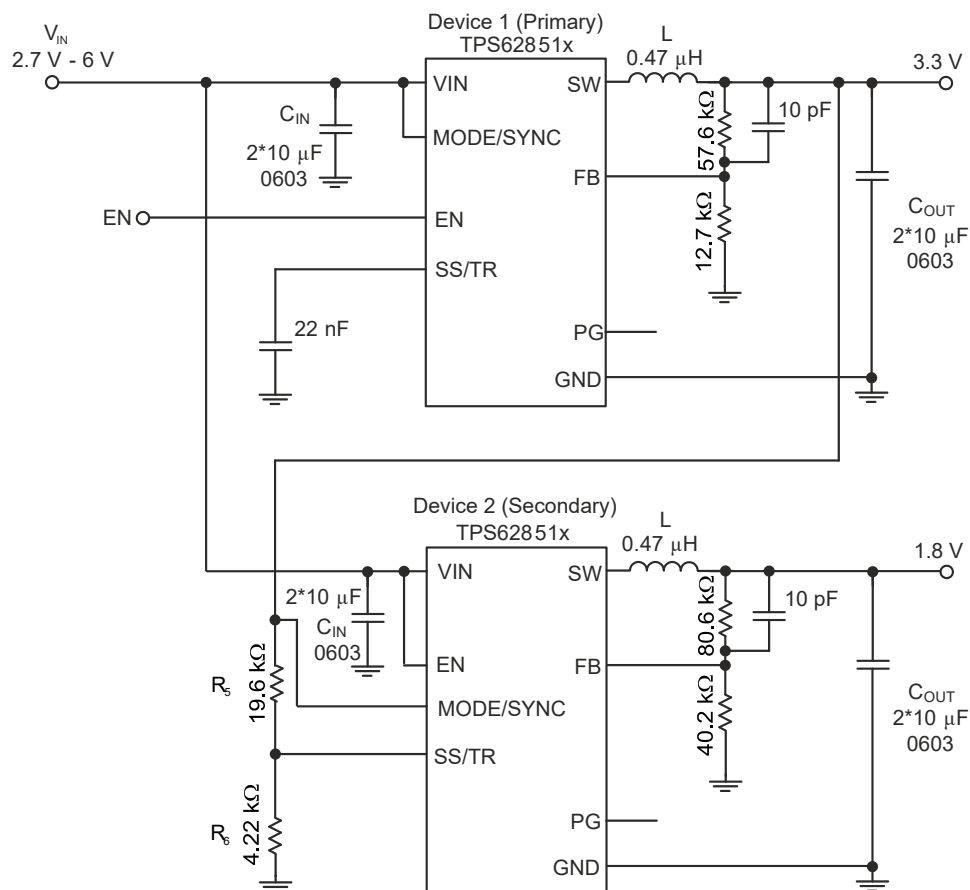
## 10.3 System Examples

### 10.3.1 Voltage Tracking

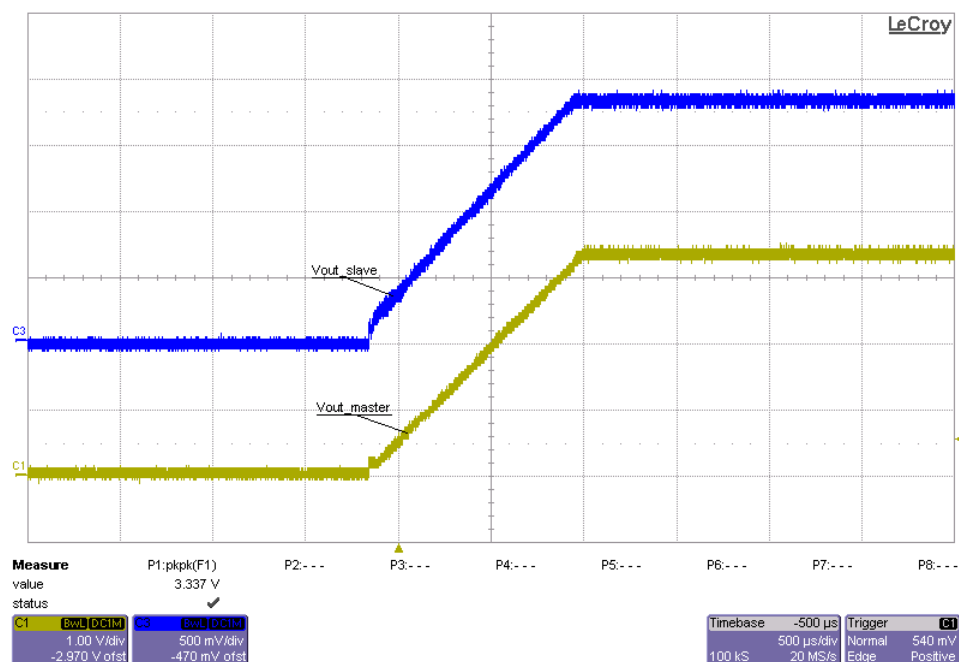
The TPS62851x follows the voltage applied to the SS/TR pin. A voltage ramp on SS/TR to 0.6 V ramps the output voltage according to the 0.6-V feedback voltage.

Tracking the 3.3 V of device 1, so that both rails reach their target voltage at the same time, requires a resistor divider on SS/TR of device 2 equal to the output voltage divider of device 1. The output current of 2.5  $\mu\text{A}$  on the SS/TR pin causes an offset voltage on the resistor divider formed by  $R_5$  and  $R_6$ . The equivalent resistance of  $R_5 \parallel R_6$  must be kept below 15 k $\Omega$ . The current from SS/TR causes a slightly higher voltage across  $R_6$  than 0.6 V, which is desired because device 2 switches to its internal reference as soon as the voltage at SS/TR is higher than 0.6 V.

In case both devices need to run in forced PWM mode, it is recommended to tie the MODE pin of device 2 to the output voltage or the power good signal of device 1, the master device. The TPS6281x does have a duty cycle limitation defined by the minimum on-time. For tracking down to low output voltages, device 2 cannot follow once the minimum duty cycle is reached. Enabling PFM mode while tracking is in progress allows the user to ramp down the output voltage close to 0 V.



**10-57. Schematic for Output Voltage Tracking**



**10-58. Scope Plot for Output Voltage Tracking**

### 10.3.2 Synchronizing to an External Clock

The TPS62851x can be externally synchronized by applying an external clock on the MODE/SYNC pin. There is no need for any additional circuitry as long as the input signal meets the requirements given in the electrical specifications. The clock can be applied / removed during operation, allowing you to switch from an externally defined fixed frequency to power-save mode or to internal fixed frequency operation.

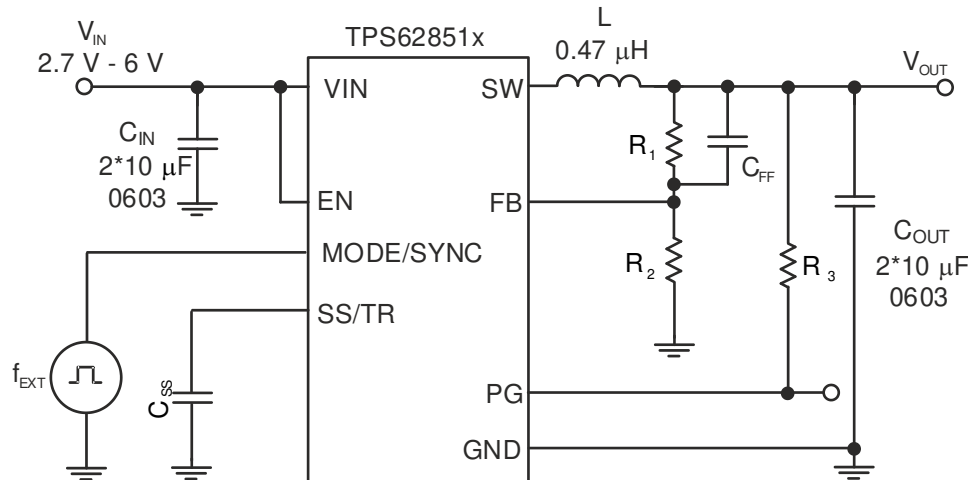
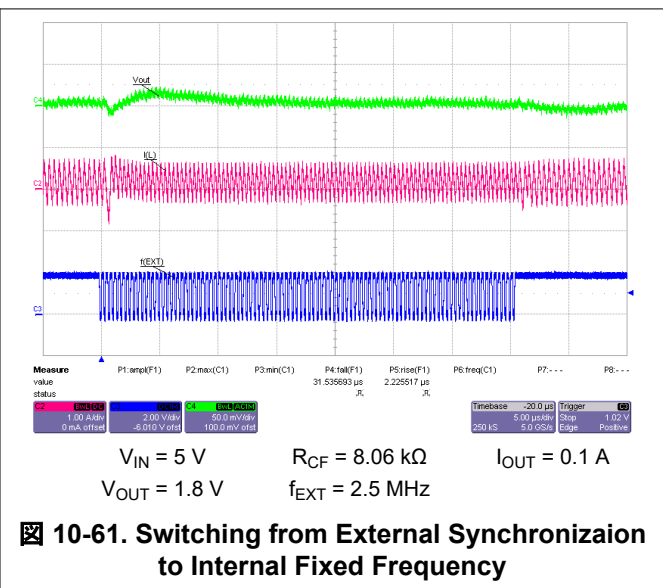
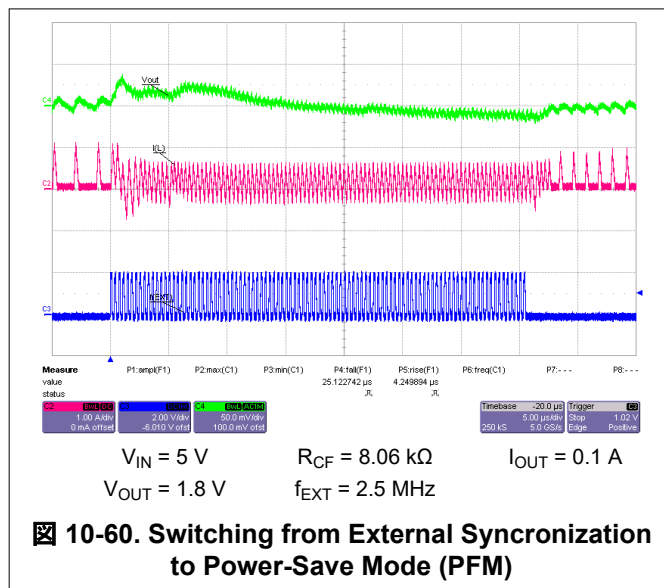


FIG 10-59. Schematic using External Synchronization



## 11 Power Supply Recommendations

The TPS62851x device family does not have special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPS62851x.

## 12 Layout

### 12.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS62851x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like the following:

- Poor regulation (both in [セクション 12.2](#) and load)
- Stability and accuracy weaknesses
- Increased EMI radiation
- Noise sensitivity

See [図 12-1](#) for the recommended layout of the TPS62851x, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances and narrow traces must be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB need to be connected with short wires and not nearby high dv/dt signals (for example, SW). As they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin as well as the FB resistors, R<sub>1</sub> and R<sub>2</sub>, must be kept close to the IC and be connected directly to the pin and the system ground plane.

The package uses the pins for power dissipation. Thermal vias on the VIN and GND pins help to spread the heat into the PCB.

The recommended layout is implemented on the EVM and shown in the [TPS62851xEVM-139 Evaluation Module User's Guide](#).

### 12.2 Layout Example

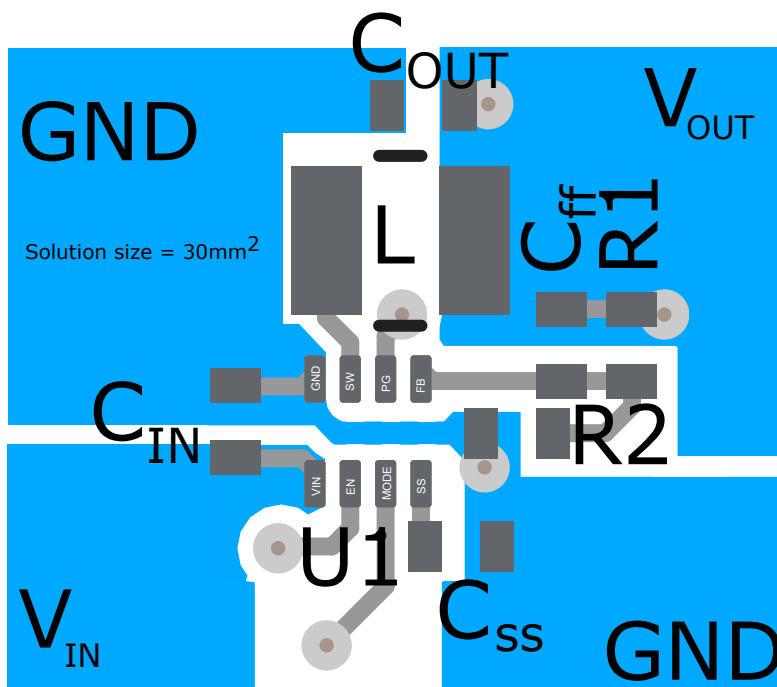


図 12-1. Example Layout

## 13 Device and Documentation Support

### 13.1 Device Support

#### 13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 13.3 サポート・リソース

**TI E2E™ サポート・フォーラム**は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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#### 13.4 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

#### 13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 13.6 Glossary

##### TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS628510DRLR</a>	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 150	1000
TPS628510DRLR.A	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	1000
TPS628510DRLR.B	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 150	1000
<a href="#">TPS628511DRLR</a>	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 150	1100
TPS628511DRLR.A	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	1100
TPS628511DRLR.B	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 150	1100
<a href="#">TPS628512DRLR</a>	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 150	1200
TPS628512DRLR.A	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	1200
TPS628512DRLR.B	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 150	1200
<a href="#">TPS628513DRLR</a>	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 150	1300
TPS628513DRLR.A	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	1300
TPS628513DRLR.B	Active	Production	SOT-5X3 (DRL)   8	4000   LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 150	1300

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

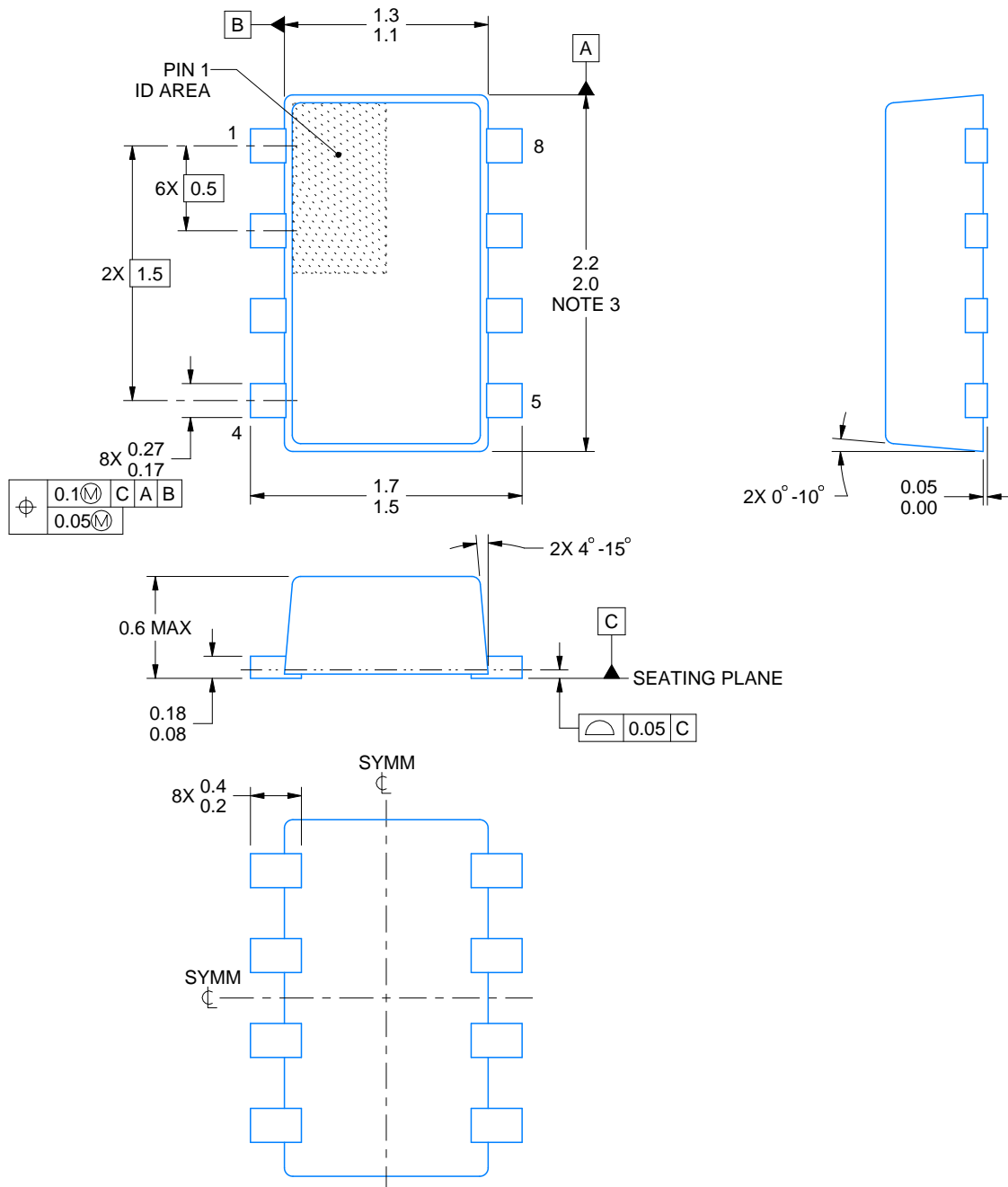
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628510DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS628511DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS628512DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS628513DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS628510DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS628511DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS628512DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS628513DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0



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## NOTES:

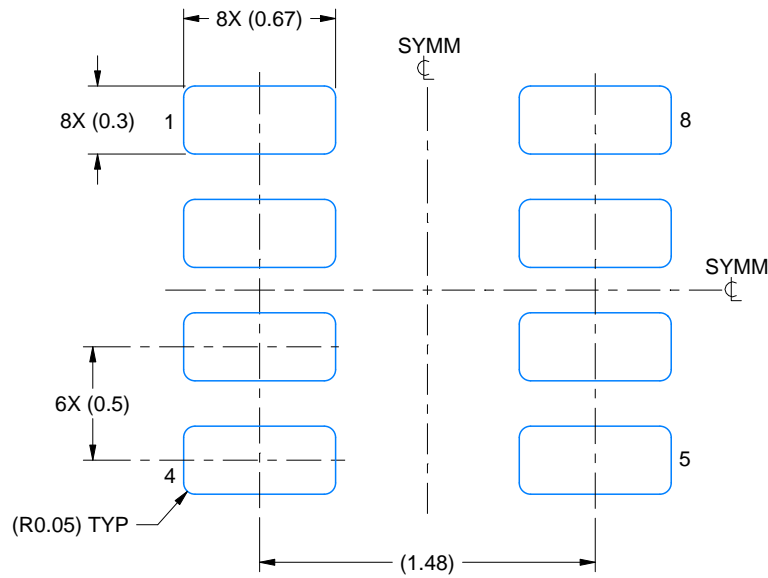
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

# EXAMPLE BOARD LAYOUT

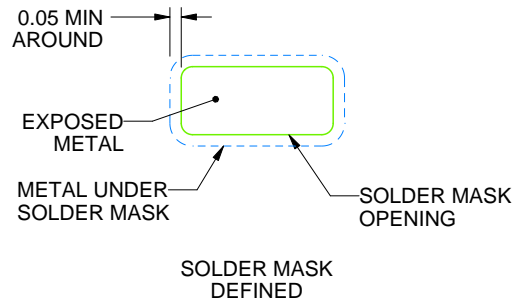
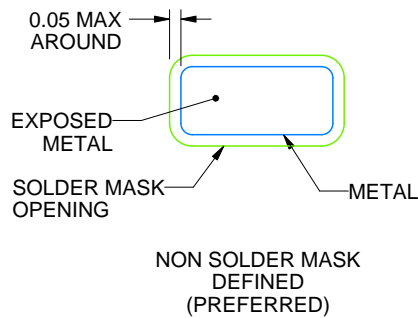
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDERMASK DETAILS

4224486/G 11/2024

NOTES: (continued)

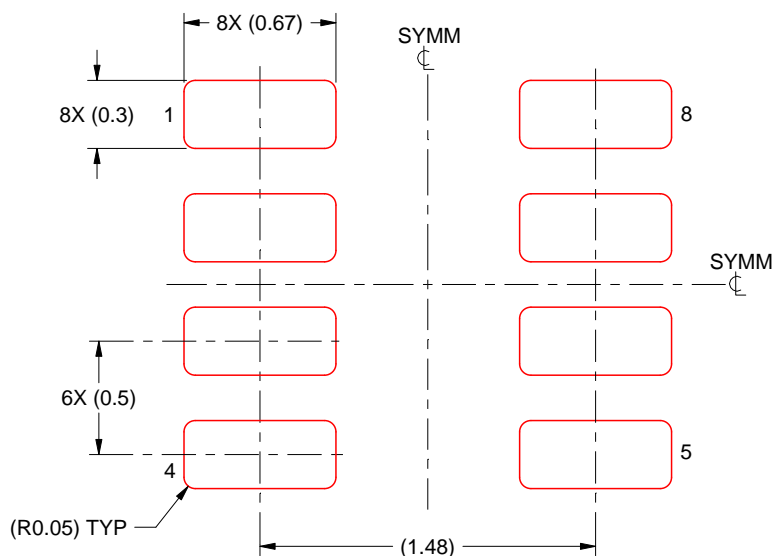
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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