TEXAS INSTRUMENTS
TPS62821, TPS62822, TPS62823
JAJSEU1B – NOVEMBER 2017 – REVISED MAY 2018

TPS6282x 5.5V、1/2/3Aで1%精度の降圧コンバータ・ファミリ

1 特長

- DCS-Control™トポロジ
- 26/25mΩの内部パワー・スイッチ(TPS62823)
- 最大3Vの出力電流(TPS62823)
- 非常に低い静止電流: 4µA
- 標準2.2MHzのスイッチング周波数
- 1%の帰還電圧精度(全温度範囲)
- イネーブル(EN)およびパワー・グッド(PG)
- 出力電圧を0.6V～4Vの範囲で調整可能
- 100%デューティ・サイクル・モード
- 内部ソフト・スタート回路
- シームレスなパワーセーブ・モード移行
- 低電圧誤動作防止
- アクティブ出力放電
- サイクルごとの電流制限
- ヒカップ短絡保護機能
- 過熱保護機能
- WEBENCH® Power Designerにより、TPS62822を使用するカスタム設計を作成

2 アプリケーション

- 携帯型/バッテリ駆動デバイス用のPOL電源
- ファクトリ/ビルディング・オートメーション
- モバイル・コンピューティング、ネットワーキング・カード
- ソリッド・ステート・ドライブ
- データ端末、POS
- サーバー、プロジェクタ、プリンタ

3 概要

TPS6282xは、汎用で使いやすい同期整流降圧DC-DCコンバータで、静止電流がわずか4µAと非常に低いのが特長です。2.4V～5.5Vの入力電圧から、最大3Aの出力電流(TPS62823)を供給できます。また、DCS-Control™トポロジにより高速な過渡応答を実現しています。

内部基準電圧により、最低0.6Vまで出力電圧をレギュレートでき、接合部温度が-40℃～125℃の範囲で、1%の高い帰還電圧精度を維持します。1、2、3Aを選択可能なピン互換でBOM互換のデバイス・ファミリを、小さな470nHのインダクタで使用できます。

TPS6282xにはパワー・セーブ・モードがあり、自動的にこのモードに移行して、非常に軽い負荷までの範囲で高い効率を維持します。

このデバイスにはパワー・グッド信号と、内部のソフトスタート回路があります。100%モードで動作可能です。フォルト保護のため、ヒカップ電流制限と、サーマル・シャットダウンが内蔵されています。

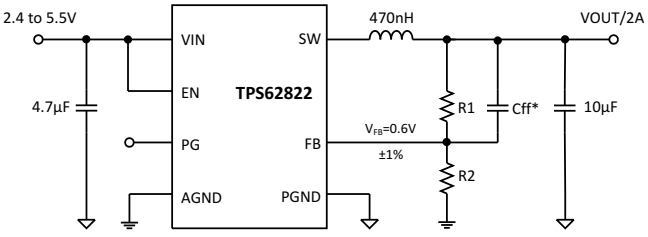
TPS6282xは、2×1.5mmのQFN-8パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS62821DLC	QFN (8)	2.00×1.50mm
TPS62822DLC		
TPS62823DLC		

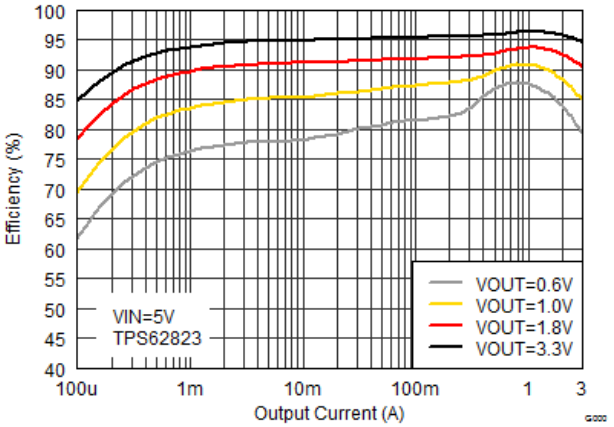
(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



* optional

効率と出力電流との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (February 2018) から Revision B に変更 **Page**

- 変更 TPS62822およびTPS62823のステータスを量産データ・デバイスに ... 22

2017年11月発行のものから更新 **Page**

- 変更 TPS62821のステータスを量産データ・デバイスに ... 22

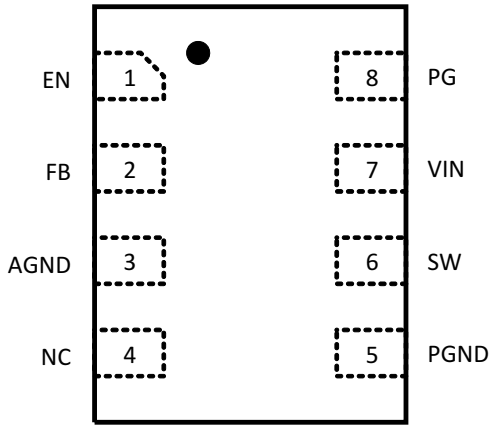
5 Device Comparison Table

Part Number	Output Current	Output Voltage (1)
TPS62821DLC	1 A	Adjustable
TPS62822DLC	2 A	Adjustable
TPS62823DLC	3 A	Adjustable

(1) For fixed output voltage versions please contact your TI sales representative.

6 Pin Configuration and Functions

DLC Package
8 Pin (VQFN)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable input (High=Enabled, Low=Disabled). Do not leave floating.
FB	2	I	Output voltage feedback. Connect resistive voltage divider to this pin.
AGND	3		Signal ground. Internally connected to the PGND pin. Can be left floating.
NC	4		Internally not connected. Can be connected to VOUT, GND or left floating.
PGND	5	Power	Power ground
SW	6	Power	Switch node, connected to the internal MOSFET switches.
VIN	7	Power	Supply voltage
PG	8	O	Power good output. If unused, leave floating or connect to GND.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Pin Voltage Range	VIN, FB, EN, PG, NC	-0.3	6	V
	SW (DC)	-0.3	V_{IN} + 0.3	
	SW (DC, in current limit)	-1.0		
	SW (AC), less than 10ns(2)	-2.5	10	
Power Good Sink Current			1	mA
Operating Junction Temperature Range, T_J		-40	150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) While switching.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply Voltage Range, V_{IN}		2.4		5.5	V
Output Voltage Range, V_{OUT}		0.6		4	V
Maximum Output Current, I_{OUT}	TPS62821			1	A
	TPS62822			2	
	TPS62823			3	
Operating Junction Temperature, T_J		-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6282x DLC (VQFN) 8 PINS		UNIT
		JEDEC PCB	TPS6282xEVM-005	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.1	69.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.2	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.4	n/a(2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	4.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.7	44.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM.

7.5 Electrical Characteristics

over operating junction temperature range (T_J=-40°C to 125°C) and V_{IN}=2.4V to 5.5V. Typical values at V_{IN}=5V and T_J=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input Voltage range		2.4		5.5	V
I_Q	Operating Quiescent Current	EN=High, I_{OUT}=0A, device not switching		4	10	µA
I_{SD}	Shutdown Current	EN=Low, T_J = -40°C to 85°C		0.05	0.5	µA
V_{UVLO}	Undervoltage Threshold	Falling Input Voltage	2.1	2.2	2.3	V
	Undervoltage Hysteresis			160		mV
T_{SD}	Thermal Shutdown Threshold	Rising Junction Temperature		150		°C
	Thermal Shutdown Hysteresis			20		
CONTROL (EN, PG)						
V_H	High-Level Threshold Voltage (EN)		1.0			V
V_L	Low-Level Threshold Voltage (EN)				0.4	V
I_{LKG}	Input Leakage Current (EN, PG)	EN = High, V_{PG} = 5V		10	100	nA
t_{SS}	Soft-Start Time	Time from EN=High to 95% of V_{OUT} nominal		1.25		ms
V_{PGTL}	Power Good Lower Threshold Voltage	Rising (V_{FB} vs regulation target)	94%	96%	98%	
		Falling (V_{FB} vs regulation target)	90%	92%	94%	
V_{PGTH}	Power Good Upper Threshold Voltage	Rising (V_{FB} vs regulation target)	108%	110%	112%	
		Falling (V_{FB} vs regulation target)	103%	105%	107%	
V_{PGL}	Power Good Logic Low Level Output Voltage	I_{PG} = -1mA			0.4	V
t_{PGD}	Power Good delay	rising		100		µs
		falling		20		
POWER SWITCH						
F_{SW}	Switching Frequency	PWM Mode Operation		2.2		MHz
$R_{DS(on)}$	High-Side FET ON-Resistance	TPS62821		35		mΩ
		TPS62822		35		
		TPS62823		26		
	Low-Side FET ON-Resistance	TPS62821,2,3		25		
I_{LIM}	High-Side FET Current Limit	TPS62821	1.7	2.1	2.4	A
		TPS62822	2.7	3.3	3.7	
		TPS62823	3.7	4.3	5.0	
OUTPUT						
I_{LKG_FB}	Input Leakage Current (FB)	EN=High, V_{FB}=0.6V		10	50	nA
V_{FB}	Feedback Voltage Accuracy	PWM Mode	594	600	606	mV
I_{DIS}	Output Discharge Current	EN=Low, V_{SW} = 0.4V	75	400		mA
	DC Load Regulation	PWM Mode Operation		0.2		%/A
	DC Line Regulation	PWM Mode Operation		0.05		%/V

.0

7.6 Typical Characteristics

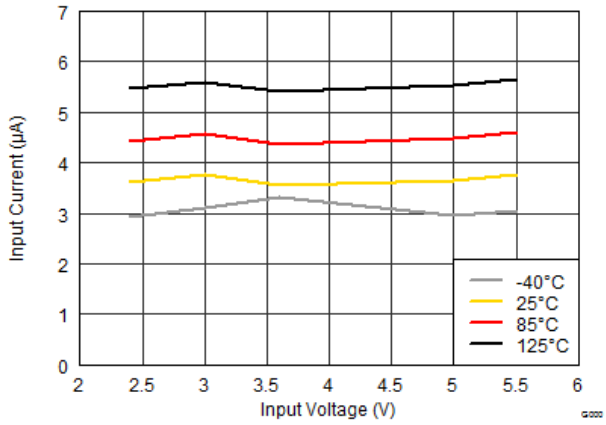


図 1. Quiescent Current

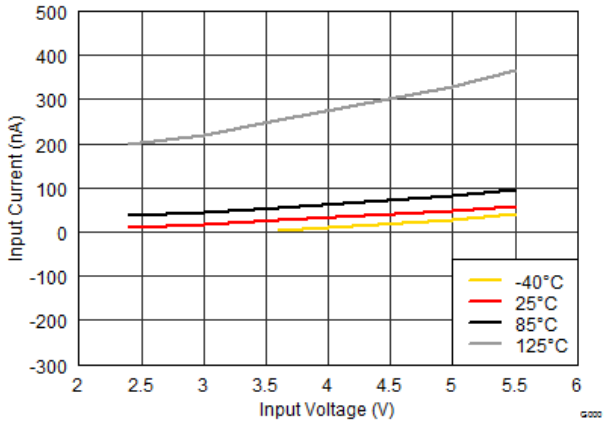


図 2. Shutdown Current

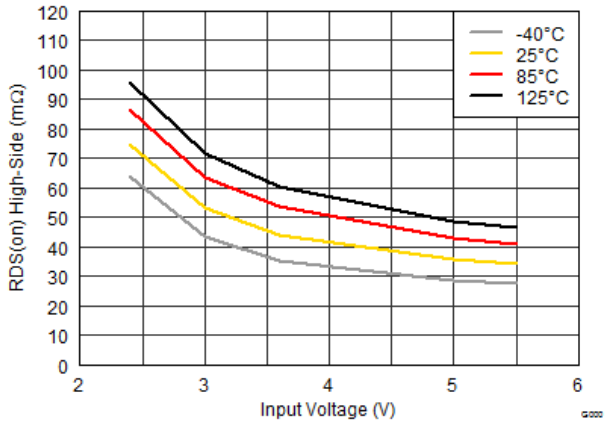


図 3. High-Side Switch Resistance (TPS62821/2)

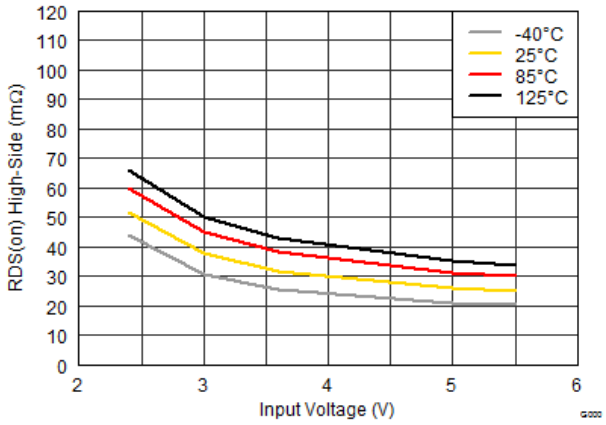


図 4. High-Side Switch Resistance (TPS62823)

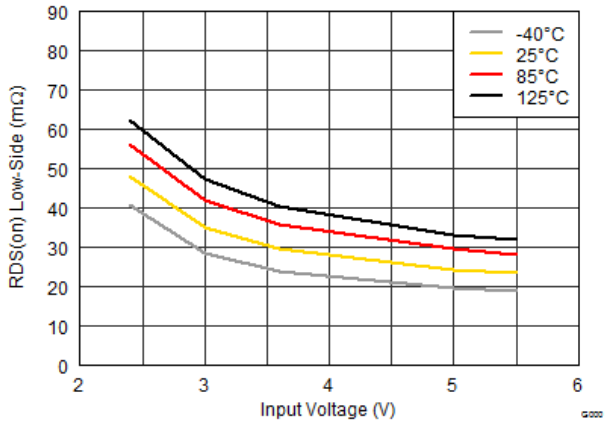


図 5. Low-Side Switch Resistance (TPS62821/2/3)

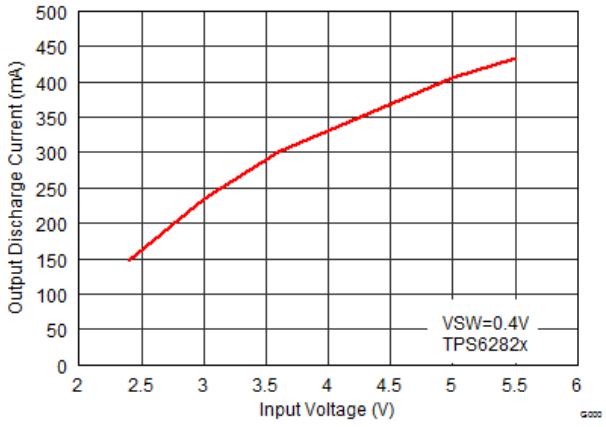


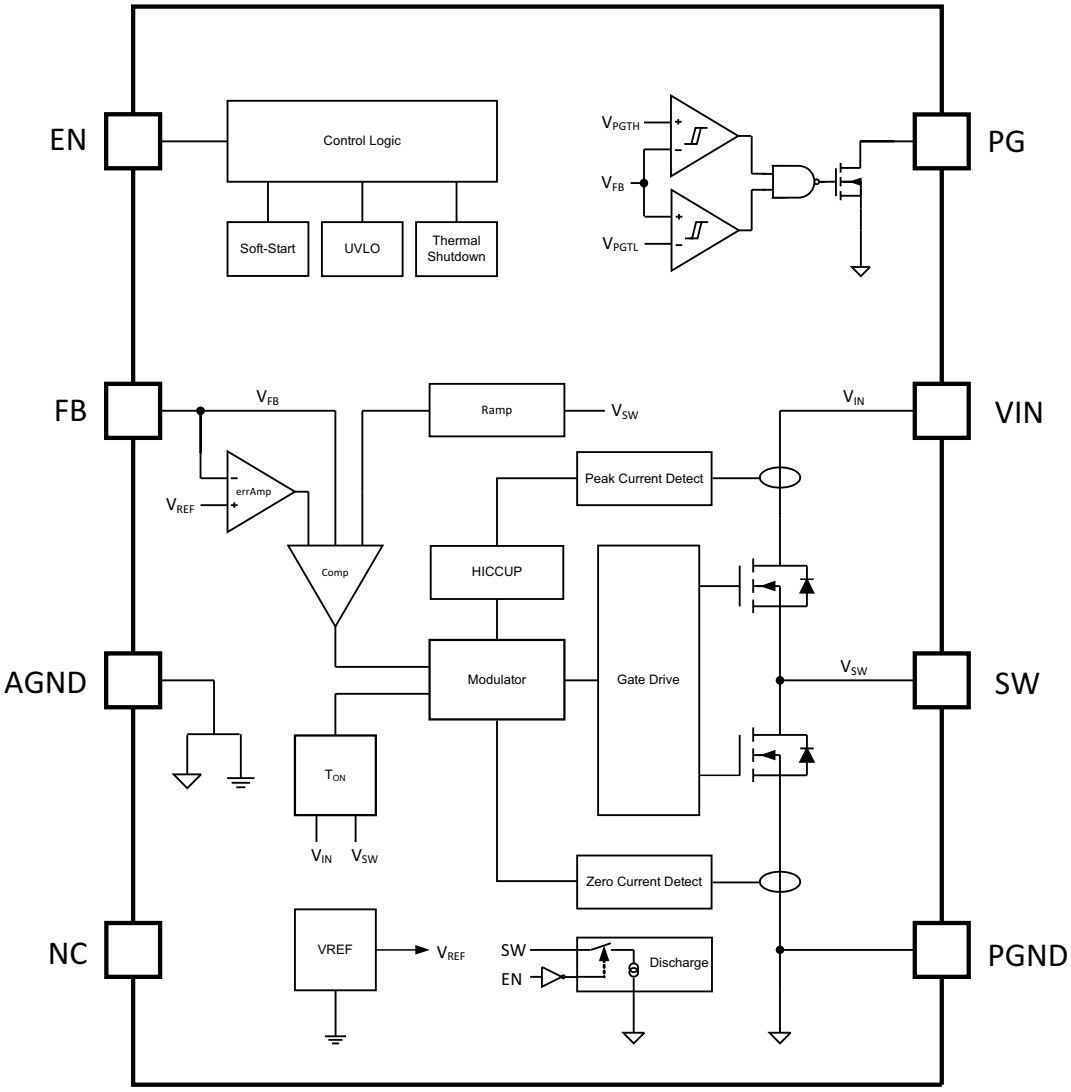
図 6. Active Output Discharge Current (EN=Low)

8 Detailed Description

8.1 Overview

The TPS6282x are synchronous step-down converters based on the DCS-Control™ topology with an adaptive constant on-time control and a stabilized switching frequency. It operates in PWM (pulse width modulation) mode for medium to heavy loads and in PSM (power save mode) at light load conditions, keeping the output voltage ripple small. The nominal switching frequency is about 2.2MHz with a small and controlled variation over the input voltage range. As the load current decreases, the converter enters PSM, reducing the switching frequency to keep efficiency high over the entire load current range. Since combining both PWM and PSM within a single building block, the transition between modes is seamless and without effect on the output voltage. The devices offer both excellent dc voltage and fast load transient regulation, combined with a very low output voltage ripple.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable / Shutdown and Output Discharge

The device starts operation, when Enable (EN) is set High. The input threshold levels are typically 0.9V for rising and 0.7V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled Low with a shutdown current of typically 50nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore, V_{IN} must remain present for the discharge to function.

8.3.2 Soft-Start

About 250µs after EN goes High, the internal soft-start circuitry controls the output voltage during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time of about 1ms. It also prevents unwanted voltage drops from high-impedance power sources or batteries. TPS6282x can start into a pre-biased output.

8.3.3 Power Good (PG)

The TPS6282x has a built in power good (PG) function. The PG pin goes high impedance, when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low (see 表 1). The PG function is formed with a window comparator, which has an upper and lower voltage threshold (see *Electrical Characteristics*). The PG pin is an open drain output that requires a pull-up resistor and can sink up to 1mA. If not used, the PG pin can be left floating or connected to GND.

表 1. Power Good Pin Logic

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{PGTL}$ and $V_{FB} \leq V_{PGTH}$	√	
	$V_{FB} \leq V_{PGTL}$ or $V_{FB} \geq V_{PGTH}$		√
Shutdown (EN=Low)			√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

At startup, PG transitions from low to floating about 100µs after the output voltage has reached regulation. Once in operation, PG has a deglitch delay of about 20µs before going low. When the output voltage returns to regulation, the same 100µs delay occurs.

8.3.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) function prevents misoperation of the device, if the input voltage drops below the UVLO threshold. It is set to about 2.2V with a hysteresis of typically 160mV.

8.3.5 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typ.), the device goes in thermal shutdown with a hysteresis of typically 20°C. Once the T_J has decreased enough, the device resumes normal operation.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

At load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM).

The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

Device Functional Modes (continued)

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 450ns \tag{1}$$

With that, the typical switching frequency is about 2.2MHz.

8.4.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This happens when the output current becomes smaller than half of the inductor's ripple current. The device operates now with a fixed on-time and the switching frequency further decreases proportional to the load current. It can be calculated as:

$$f_{PSM} = \frac{2 \cdot I_{OUT}}{T_{ON}^2 \cdot \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \tag{2}$$

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device may not enter PSM. The device maintains output regulation in PWM mode.

8.4.3 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles, since even at very low duty cycles the switching frequency is reduced as needed to always ensure a proper regulation.

If the output voltage level comes close to the input voltage, the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. The difference between V_{IN} and V_{OUT} is determined by the voltage drop across the high-side FET and the dc resistance of the inductor. The minimum V_{IN} that is needed to maintain a specific V_{OUT} value is estimated as:

$$V_{IN(\min)} = V_{OUT} + I_{OUT} \left(R_{DS(on)} + R_{DC(L)} \right) \tag{3}$$

8.4.4 Current Limit and Short Circuit Protection

The peak switch current of TPS6282x is internally limited, cycle by cycle, to a maximum dc value as specified in *Electrical Characteristics*. This prevents the device from drawing excessive current in case of externally caused over current or short circuit condition. Due to an internal propagation delay of about 60ns, the actual ac peak current can exceed the static current limit during that time.

If the current limit threshold is reached, the device delivers its maximum output current. Detecting this condition for 32 switching cycles (about 13µs), the device turns off the high-side MOSFET for about 100µs which allows the inductor current to decrease through the low-side MOSFET's body diode and then restarts again with a soft start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6282x is a switched mode step-down converter, able to convert a 2.4-V to 5.5-V input voltage into a lower 0.6-V to 4-V output voltage, providing up to 3A continuous output current (TPS62823). It needs a very low amount of external components. Apart from the inductor and the output and input capacitors, additional parts are only needed to set the output voltage and to enable the Power Good (PG) feature.

9.2 Typical Application

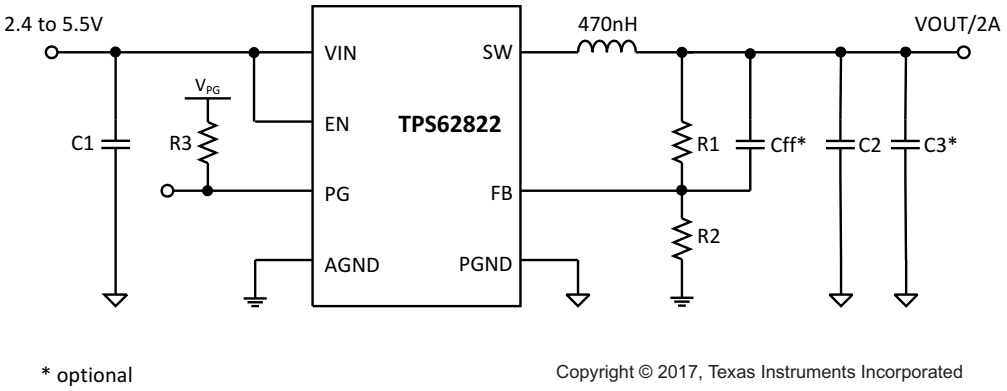


図 7. A typical 2.4 to 5.5-V, 2-A Power Supply

9.2.1 Design Requirements

The following design guideline provides a range for the component selection to operate within the recommended operating conditions. 表 2 shows the components selection that was used for the measurements shown in the *Application Curves*.

表 2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	5.5-V, step-down converter	TPS6282xDLC, Texas Instruments
L1	470 nH ±20%, 7.6mΩ DCR, 6.6A I_{SAT}	XFL4015-471MEB, Coilcraft
C1	4.7 µF ±20%, 6.3V, ceramic, 0603, X7R	JMK107BB7475MA-T, Taiyo Yuden
C2, C3	10 µF ±20%, 10V, ceramic, 0603, X7R	GRM188Z71A106MA73D, MuRata
Cff	120pF ±5%, 50V, 0603	GRM1885C1H121JA01D, MuRata
R1, R2	Depending on VOUT, chip, 0603	Standard
R3	100-kΩ, chip, 0603, 0.1W, 1%	Standard

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62822 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting the Adjustable Output Voltage

While the device regulates the feedback voltage to 0.6V, the output voltage is specified from 0.6 to 4V. A resistive divider (from VOUT to FB to AGND) sets the actual output voltage of the TPS6282x. 式 4 and 式 5 calculate the values of the resistors. I_{FB} is recommended to be in the range of 5µA, but can differ if needed.

$$R_2 = \frac{0.6V}{I_{FB}} \tag{4}$$

$$R_1 = \frac{V_{OUT}}{I_{FB}} - R_2 \tag{5}$$

表 3 shows standard resistor values for typical output voltages.

表 3. Feedback Resistor Values for Typical Output Voltages

VOUT (V)	R1 (kΩ)	R2 (kΩ)
1.0	100	150
1.2	100	100
1.8	200	100
2.5	475	150
3.3	732	162

9.2.2.3 Output Filter Selection

The TPS6282x is internally compensated and optimized for a range of output filter component values, which is specified in 表 4. Using these values simplifies the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations are possible, but should be checked for each individual application.

表 4. Recommended LC Output Filter Combinations(1)

	4.7 µF	10 µF	22 µF	47 µF	100 µF	150 µF
0.33 µH						
0.47 µH		√	√ (2)	√	√(3)	
1.0 µH		√	√	√ (3)	√(3)	
1.5 µH						

(1) The values in the table are the nominal values of inductors and ceramic capacitors. The effective capacitance can vary depending on package size, voltage rating and dielectric material (typical variations are from +20% to -50%).
(2) This combination is recommended as the standard value for most of all applications.
(3) C_{ff} is recommended for large C_{OUT} values.

9.2.2.4 Inductor Selection

The TPS6282x is designed to work with inductors of 470nH nominal and can be used with 1µH inductors as well. The inductor has to be selected for adequate saturation current and a low dc resistance (DCR). The minimum inductor current rating, that is needed under static load conditions is calculated using 式 6 and 式 7.

$$I_{peak(\max)} = I_{L(\min)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{6}$$

$$\Delta I_{L(\max)} = V_{OUT} \left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{L_{(\min)} \cdot f_{SW}} \right) \tag{7}$$

This calculation gives the minimum saturation current of the inductor needed and an additional margin is recommended to cover dynamic overshoot due to startup or load transients. Inductors are available in different dimensions. Choosing the smallest size might result in less efficiency due to larger DCR and ac losses. The following inductors have been tested with the TPS6282x:

表 5. List of Recommended Inductors

TYPE	Nominal INDUCTANCE (1)	Saturation Current and DC Resistance		Dimensions [mm]	Manufacturer(2)
		max. I_{SAT} [A](3)	max. R_{DC} [mΩ]		
HTEN20161T-R47MDR	0.47	4.8	32	2.0 x 1.6 x 1.0	Cyntec
HTEH20121T-R47MSR	0.47	4.6	25	2.0 x 1.2 x 1.0	Cyntec
DFE201610E - R47M	0.47	4.8	32	2.0 x 1.6 x 1.0	muRata
DFE201210S - R47M	0.47	4.8	32	2.0 x 1.2 x 1.0	muRata
TFM201610ALM-R47MTAA	0.47	5.1	34	2.0 x 1.6 x 1.0	TDK
TFM201610ALC-R47MTAA	0.47	5.2	25	2.0 x 1.6 x 1.0	TDK
XFL4015-471ME	0.47	6.6	8.36	4.0 x 4.0 x 1.6	Coilcraft

(1) Inductance Tolerance ±20%
(2) See *Third-party Products* disclaimer.
(3) ΔL/L≈30%

9.2.2.5 Output Capacitor Selection

The output voltage range of TPS6282x is 0.6V to 4V. While stability is a first criteria for the output filter selection (L and C_{OUT}), the output capacitor value also determines transient response behavior and ripple of V_{OUT}. The recommended typical value for the output capacitor is 2x10µF (or 1x 22µF) and can be small ceramic capacitors with low equivalent series resistance (ESR). For lower V_{OUT} (V_{OUT} ≤ 2V) and where only moderate load transients are present, 10µF can be sufficient. In either case a minimum effective output capacitance of 5µF should be present.

To keep low resistance and to get a narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using an even higher value has advantages like smaller voltage ripple and tighter output voltage accuracy in PSM.

9.2.2.6 Input Capacitor Selection

For typical application, an input capacitor of 4.7µF is sufficient and recommended. A larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR ceramic capacitor is recommended for best filtering and should be placed between VIN and PGND as close as possible to those pins. In either case a minimum effective input capacitance of 3µF should be present.

9.2.2.7 Feed-forward Capacitor Selection

To improve regulation speed, TPS6282x preferably operates with a feed-forward capacitor, connected between V_{OUT} and FB. The appropriate value is calculated using 式 8.

$$C_{ff} = \frac{12\mu s}{R_2} \tag{8}$$

Therewith, for typical values of feedback resistors (R2=100kΩ), the feed-forward capacitance is 120pF.

図 44 and 図 45 show the results of a frequency domain analysis for both use cases, with and without a feed-forward capacitor. The larger unity gain frequency, caused by the feed forward capacitor, results in a significant improvement of the transient response.

9.2.3 Application Curves

V_{IN}=5V, V_{OUT}=1.8V, T_A=25°C, BOM = 表 2, (unless otherwise noted)

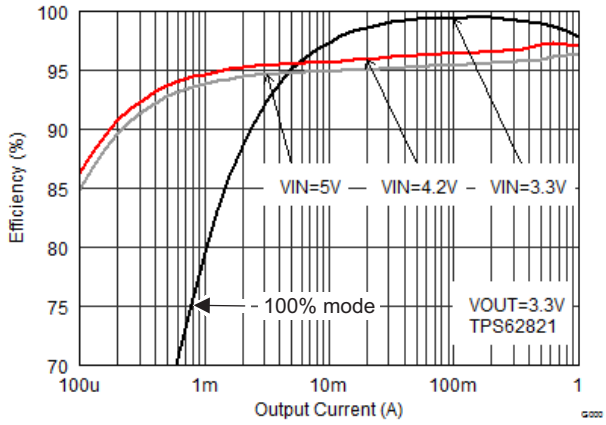


図 8. Efficiency TPS62821 at VOUT=3.3V

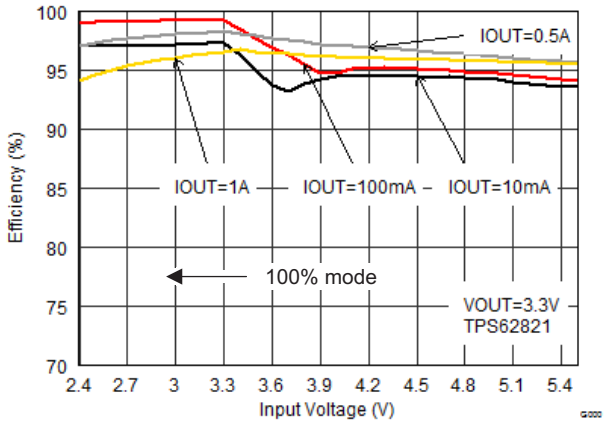


図 9. Efficiency TPS62821 at VOUT=3.3V

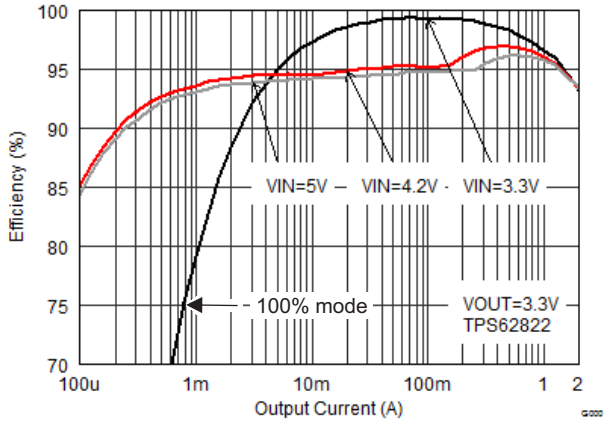


図 10. Efficiency TPS62822 at VOUT=3.3V

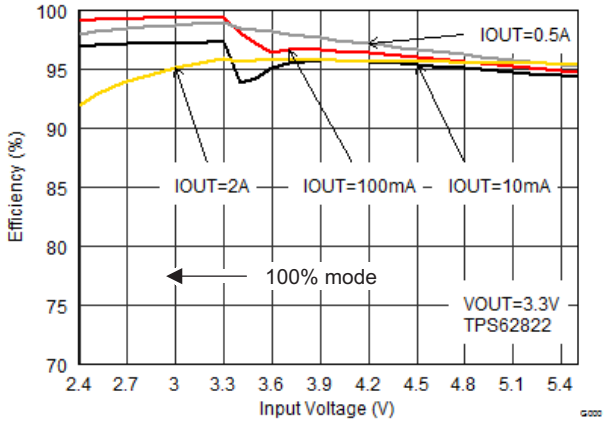


図 11. Efficiency TPS62822 at VOUT=3.3V

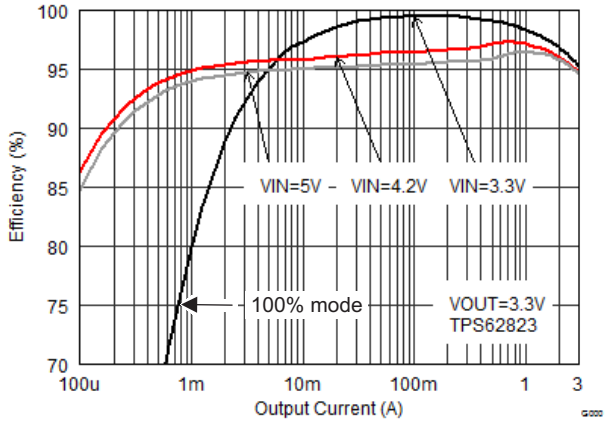


図 12. Efficiency TPS62823 at VOUT=3.3V

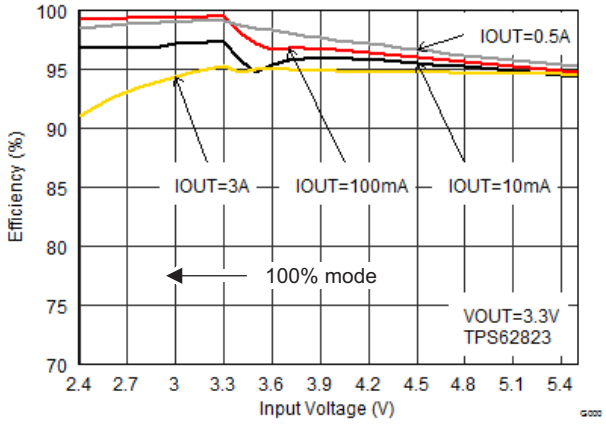


図 13. Efficiency TPS62823 at VOUT=3.3V

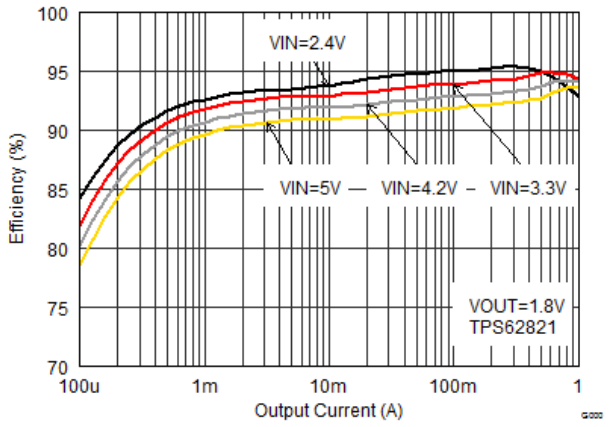


図 14. Efficiency TPS62821 at VOUT=1.8V

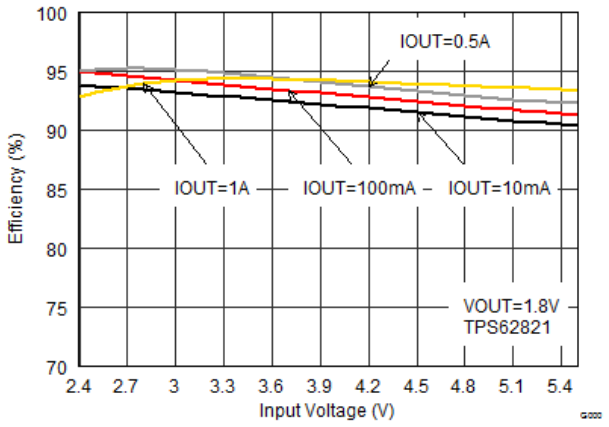


図 15. Efficiency TPS62821 at VOUT=1.8V

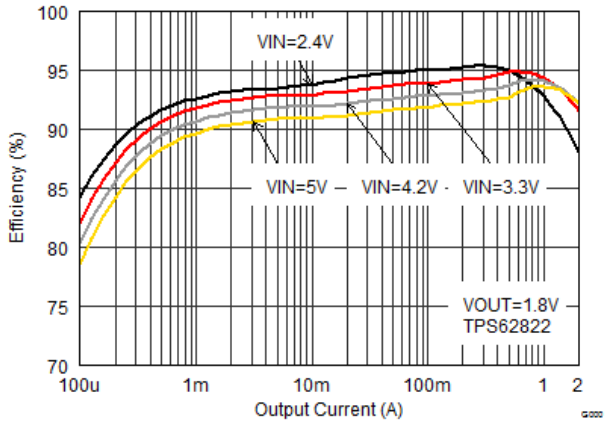


図 16. Efficiency TPS62822 at VOUT=1.8V

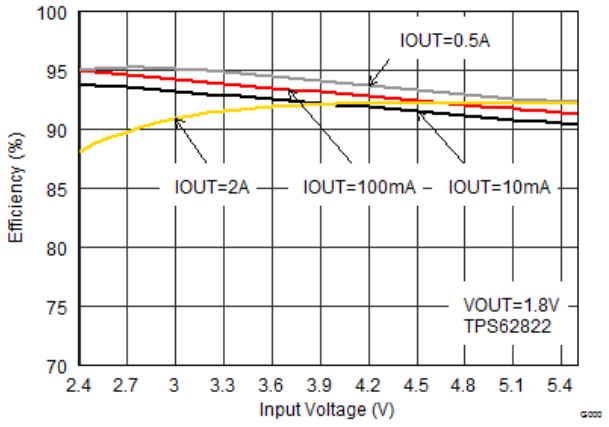


図 17. Efficiency TPS62822 at VOUT=1.8V

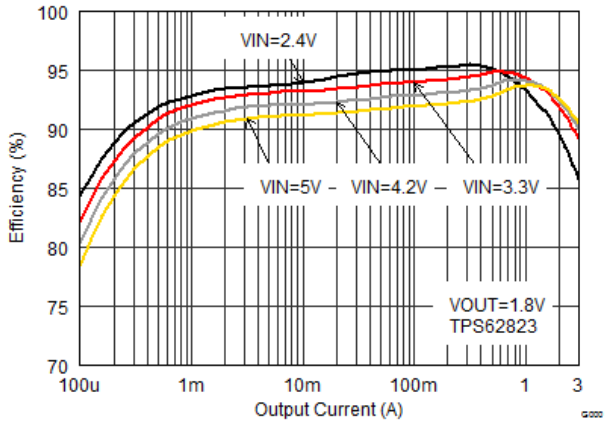


図 18. Efficiency TPS62823 at VOUT=1.8V

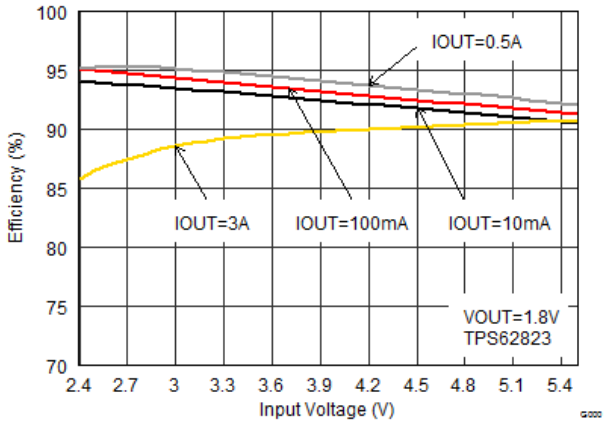


図 19. Efficiency TPS62823 at VOUT=1.8V

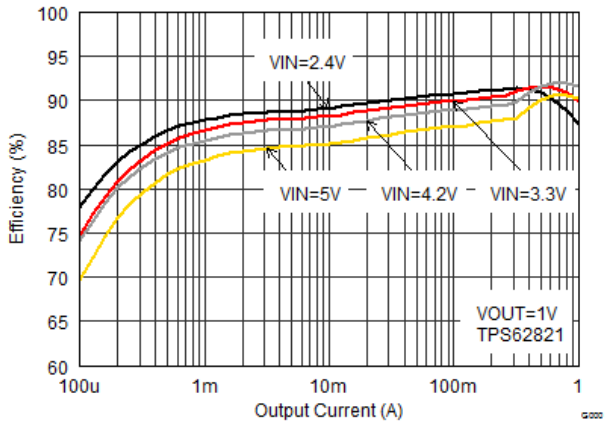


図 20. Efficiency TPS62821 at VOUT=1V

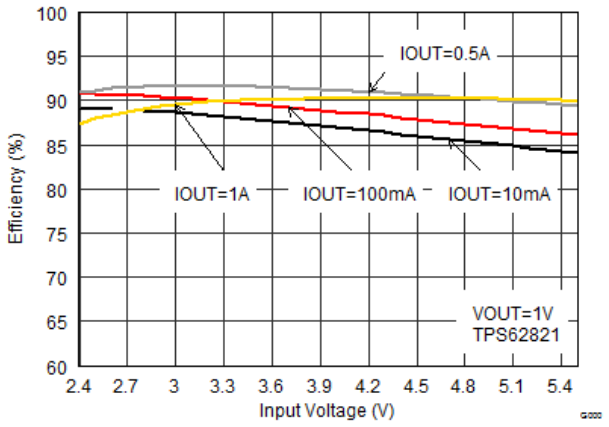


図 21. Efficiency TPS62821 at VOUT=1V

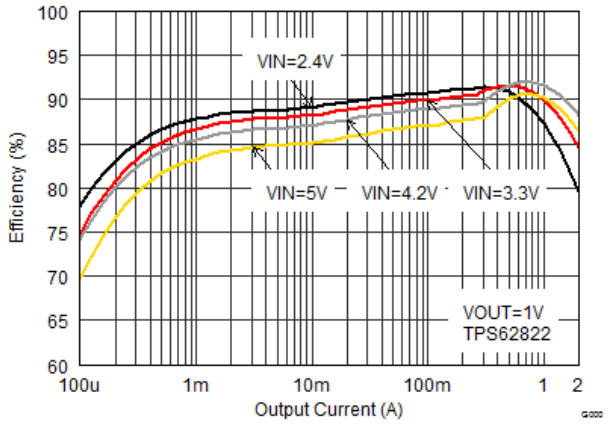


図 22. Efficiency TPS62822 at VOUT=1V

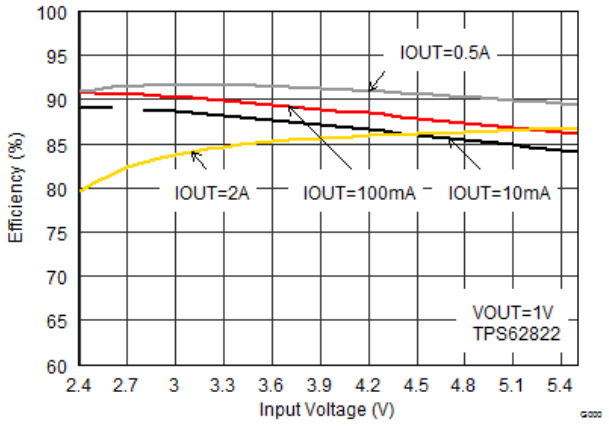


図 23. Efficiency TPS62822 at VOUT=1V

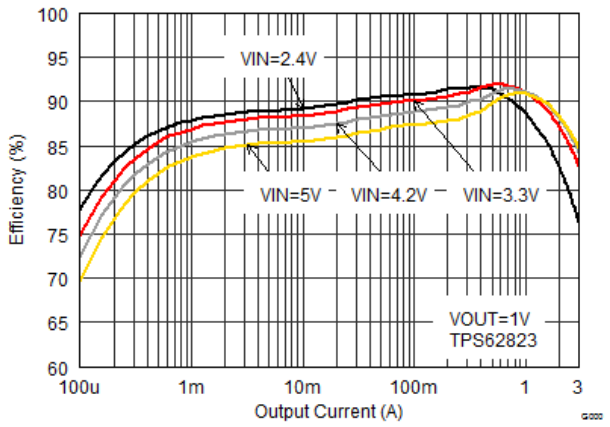


図 24. Efficiency TPS62823 at VOUT=1V

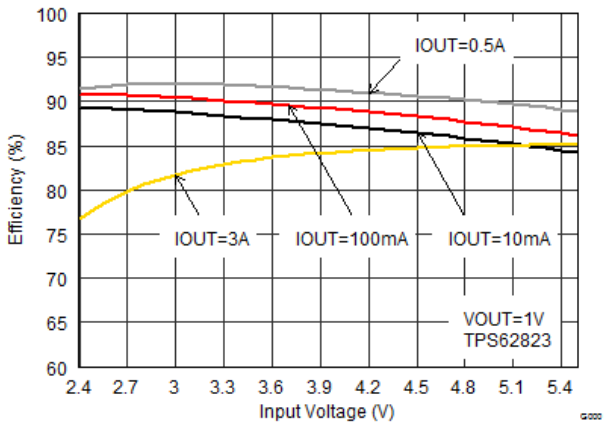


図 25. Efficiency TPS62823 at VOUT=1V

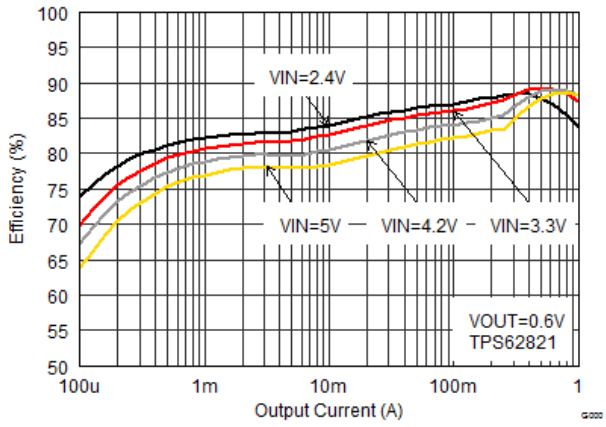


図 26. Efficiency TPS62821 at VOUT=0.6V

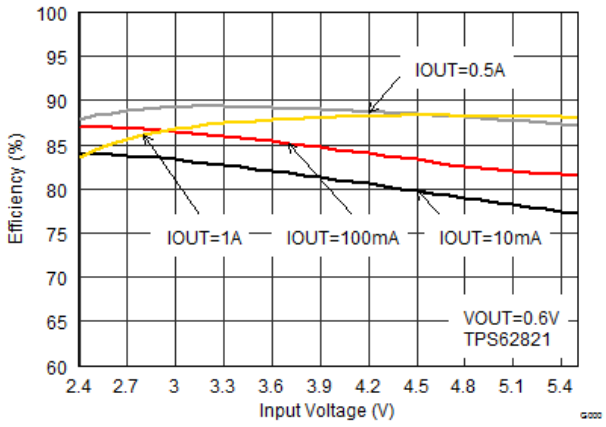


図 27. Efficiency TPS62821 at VOUT=0.6V

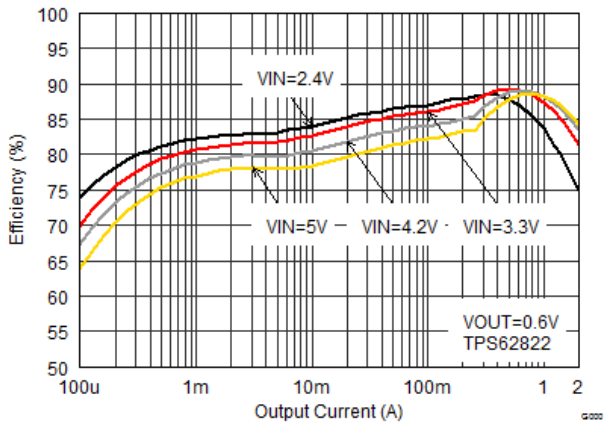


図 28. Efficiency TPS62822 at VOUT=0.6V

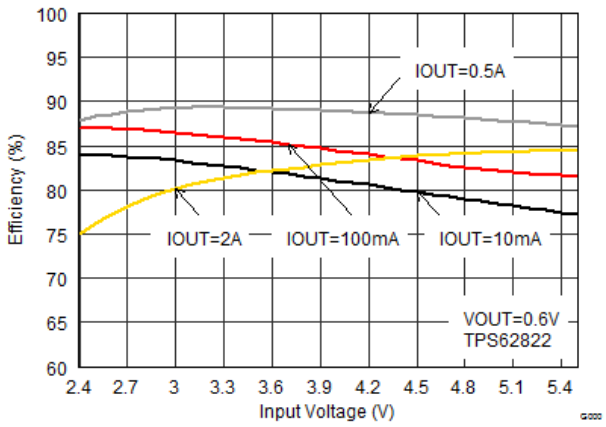


図 29. Efficiency TPS62822 at VOUT=0.6V

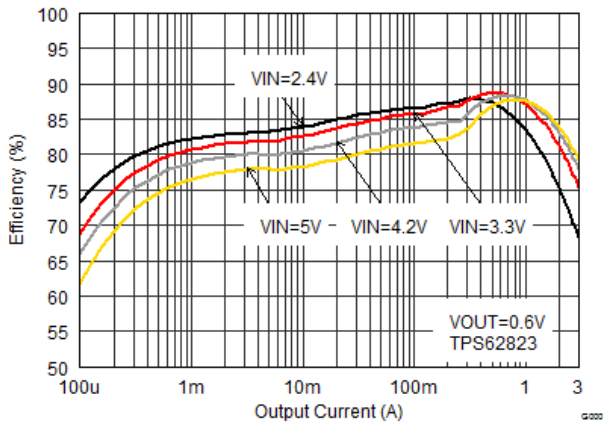


図 30. Efficiency TPS62823 at VOUT=0.6V

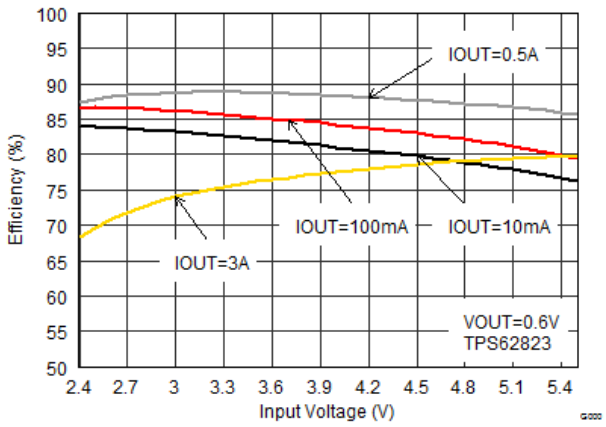


図 31. Efficiency TPS62823 at VOUT=0.6V

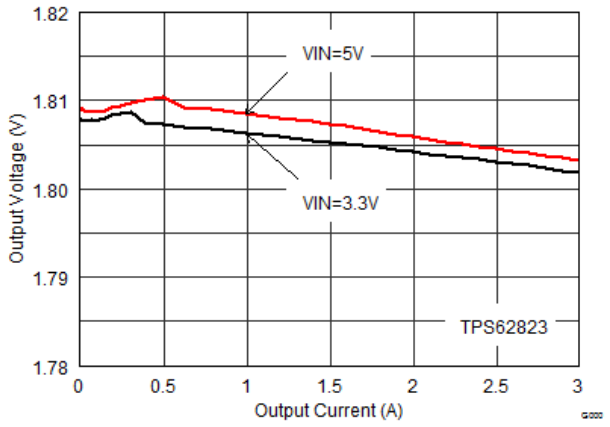


図 32. Output Voltage Accuracy (Load Regulation)

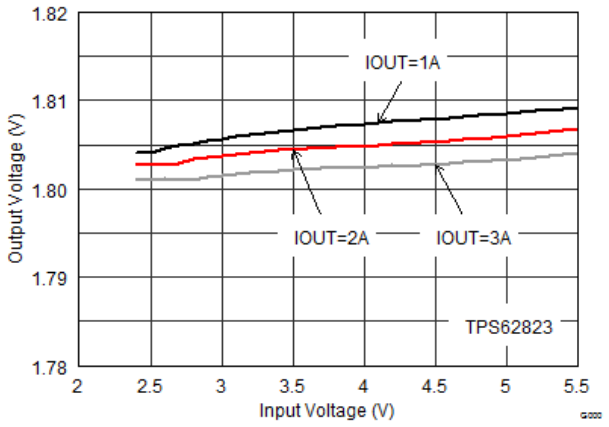


図 33. Output Voltage Accuracy (Line Regulation)

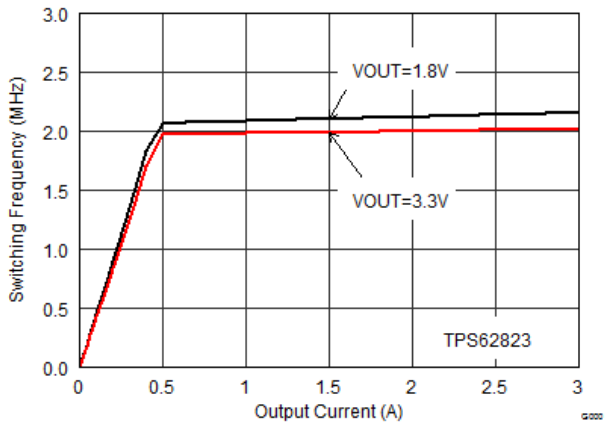


図 34. Switching Frequency vs Output Current

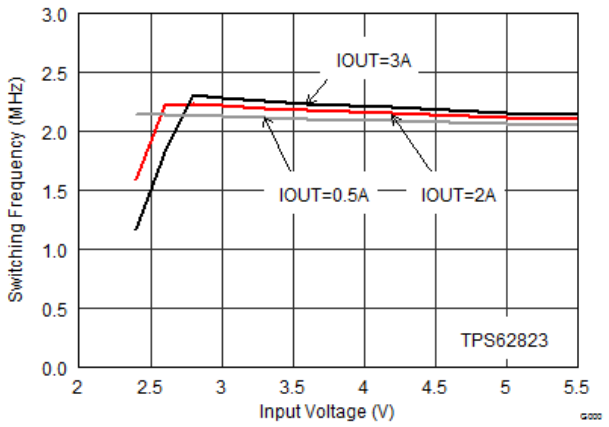
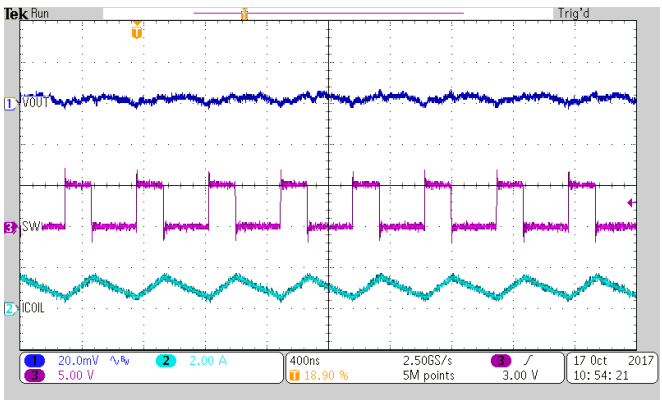
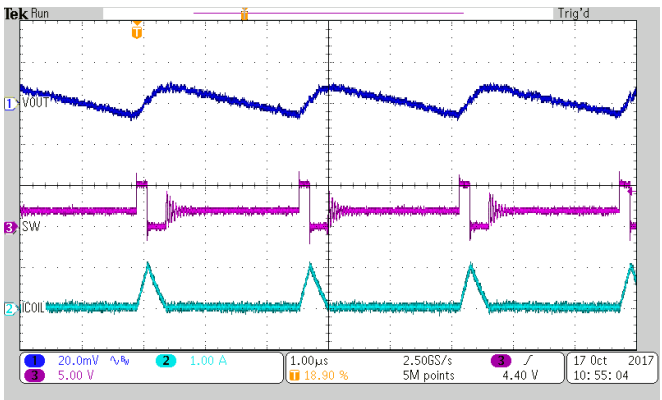


図 35. Switching Frequency vs Input Voltage



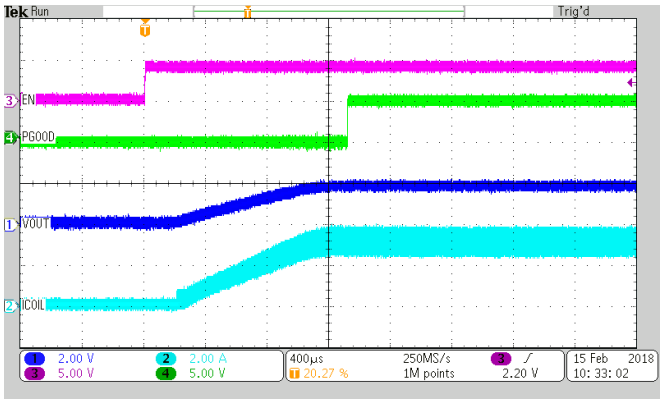
C_{OUT}=2x10µF I_{OUT}=1A

図 36. Typical Operation PWM



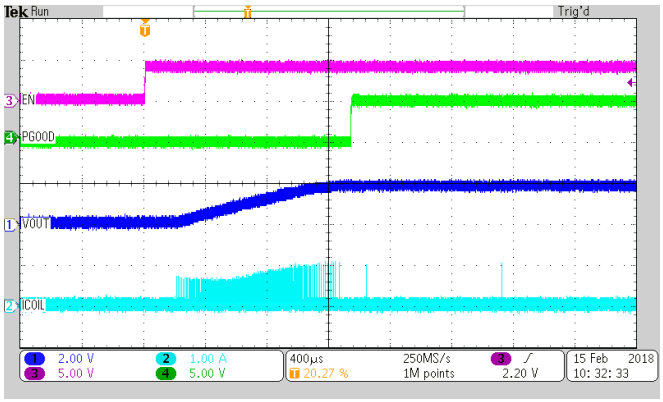
C_{OUT}=2x10µF I_{OUT}=0.1A

図 37. Typical Operation PSM



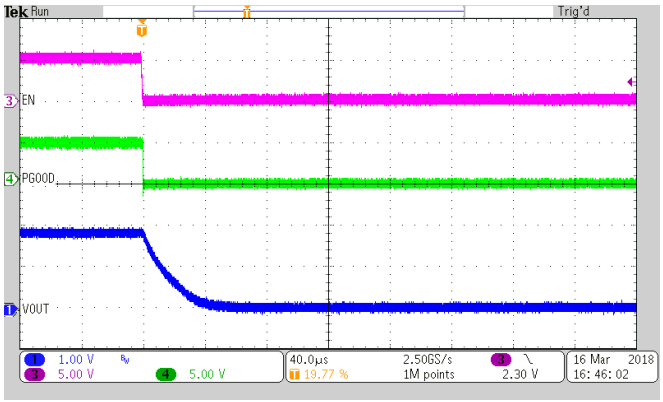
C_{OUT}=2x10µF

図 38. Startup into 0.6-Ohm (TPS62823)



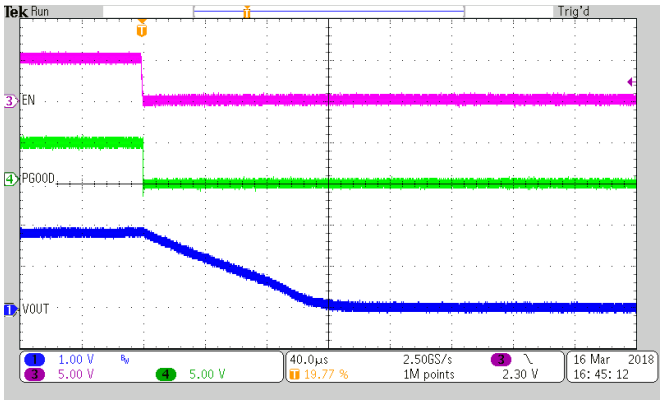
C_{OUT}=2x10µF

図 39. Startup at No Load



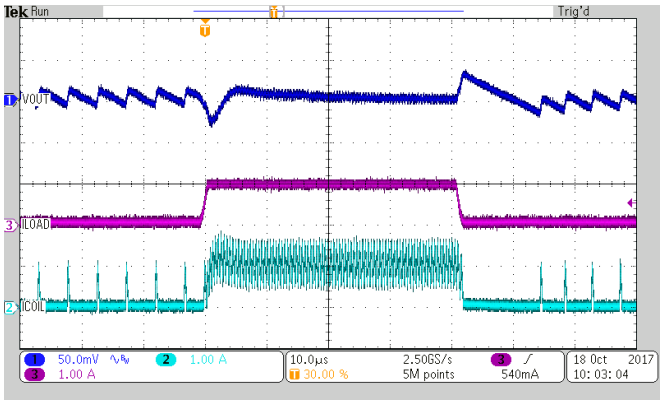
C_{OUT}=2x10µF

図 40. Active Output Discharge at load 1.8-Ohm



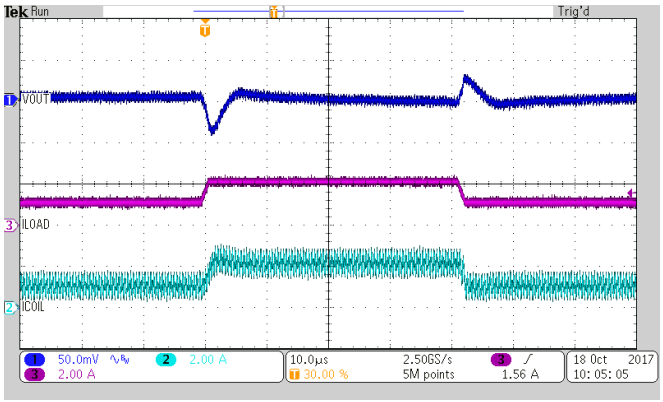
C_{OUT}=2x10µF

図 41. Active Output Discharge at No Load



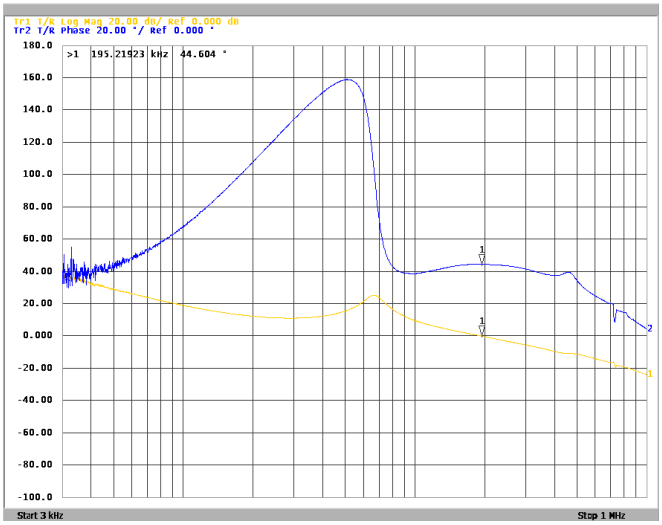
C_{OUT}=2x10µF C_{ff}=120pF

図 42. Load Transient Response, 50mA to 1A, TPS62822



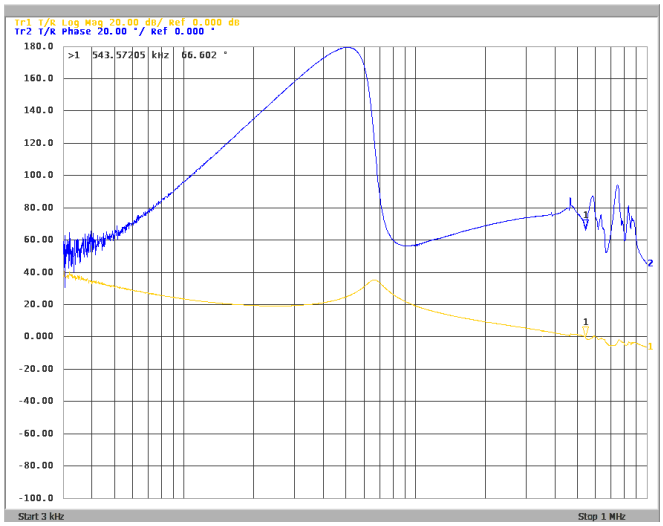
C_{OUT}=2x10µF C_{ff}=120pF

図 43. Load Transient Response, 1A to 2A, TPS62822



C_{OUT}=2x10µF　　no C_{FF}

図 44. Frequency Response (TPS62823), IOUT=3A



C_{OUT}=2x10µF　　C_{FF}=120pF

図 45. Frequency Response (TPS62823), IOUT=3A

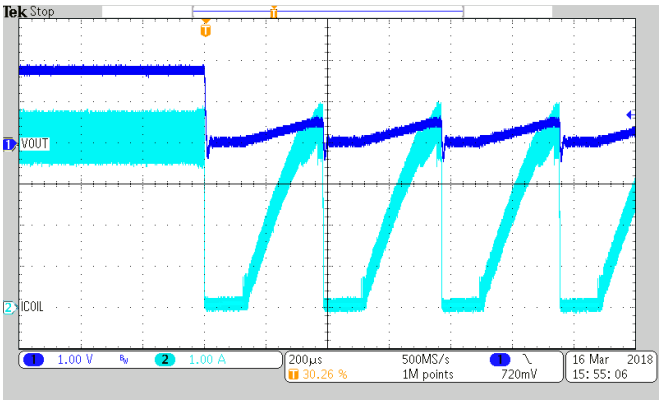


図 46. Overload Response of TPS62823

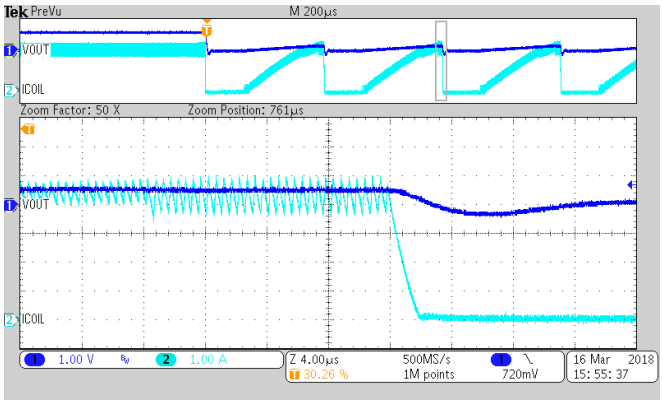


図 47. Overload Response of TPS62823 (Hiccup cycle)

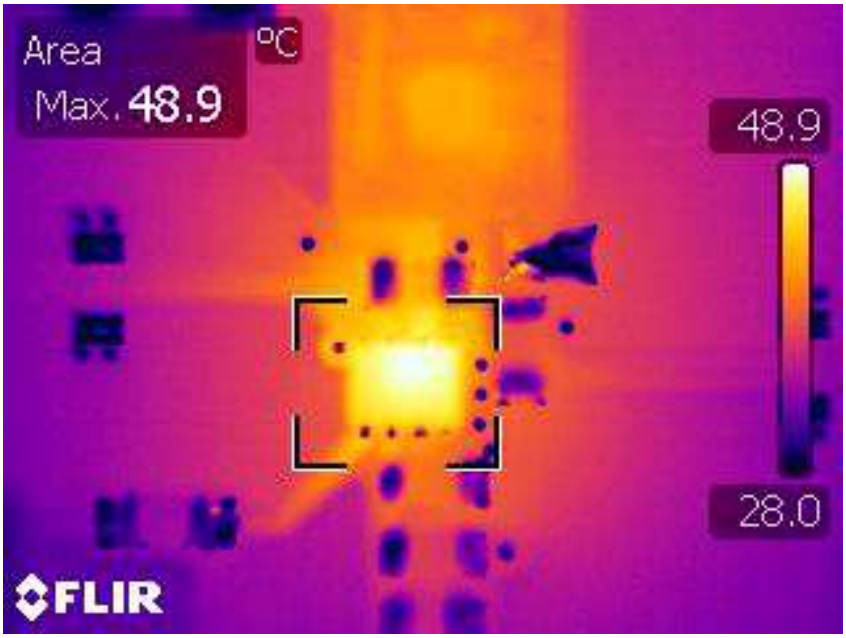


図 48. Device Temperature Rise on TPS62823 EVM at IOUT=3A

10 Power Supply Recommendations

The TPS6282x is designed to operate from a 2.4-V to 5.5-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

11 Layout

11.1 Layout Guidelines

The recommended PCB layout for the TPS6282x is shown below. It ensures best electrical and optimized thermal performance considering the following important topics:

- The input capacitor(s) must be placed as close as possible to the VIN and PGND pins of the device. This provides low resistive and inductive paths for the high di/dt input current.

- The SW node connection from the IC to the inductor conducts alternating high currents. It should be kept short.

- The V_{OUT} regulation loop is closed with COUT and its ground connection. To avoid load regulation and EMI noise, the loop should be kept short.

- The FB node is sensitive to dv/dt signals. Therefore the resistive divider should be placed close to the FB and AGND pins.

For more detailed information about the actual EVM solution, see the EVM users guide.

11.2 Layout Example

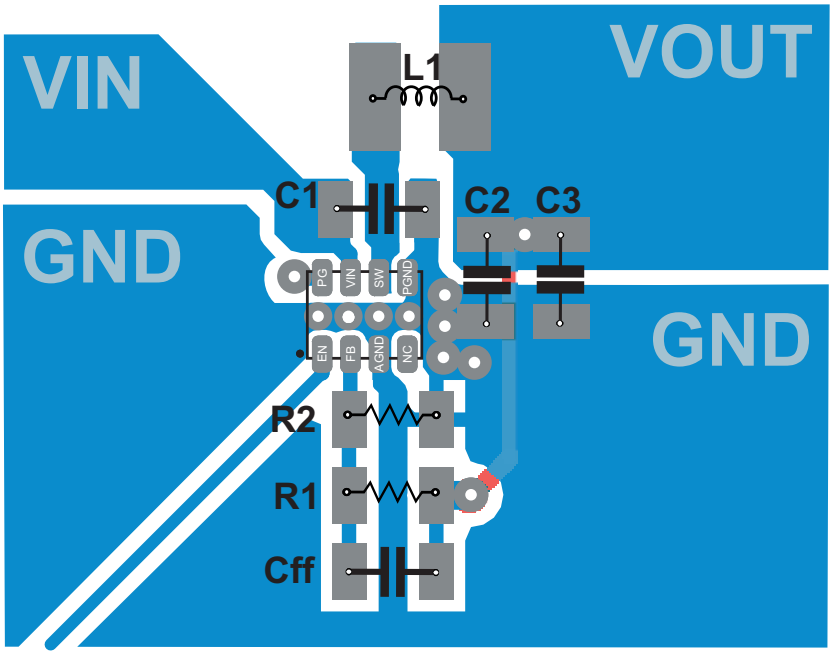


図 49. TPS6282x Board Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 6. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS62821	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62822	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62823	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。***

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.5 商標

DCS-Control, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62821DLCR	Active	Production	VSON-HR (DLC) | 8	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A1
TPS62821DLCR.A	Active	Production	VSON-HR (DLC) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A1
TPS62821DLCT	Active	Production	VSON-HR (DLC) | 8	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A1
TPS62821DLCT.A	Active	Production	VSON-HR (DLC) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A1
TPS62822DLCR	Active	Production	VSON-HR (DLC) | 8	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A2
TPS62822DLCR.A	Active	Production	VSON-HR (DLC) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A2
TPS62822DLCT	Active	Production	VSON-HR (DLC) | 8	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A2
TPS62822DLCT.A	Active	Production	VSON-HR (DLC) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A2
TPS62823DLCR	Active	Production	VSON-HR (DLC) | 8	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A3
TPS62823DLCR.A	Active	Production	VSON-HR (DLC) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A3
TPS62823DLCT	Active	Production	VSON-HR (DLC) | 8	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	A3
TPS62823DLCT.A	Active	Production	VSON-HR (DLC) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A3

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

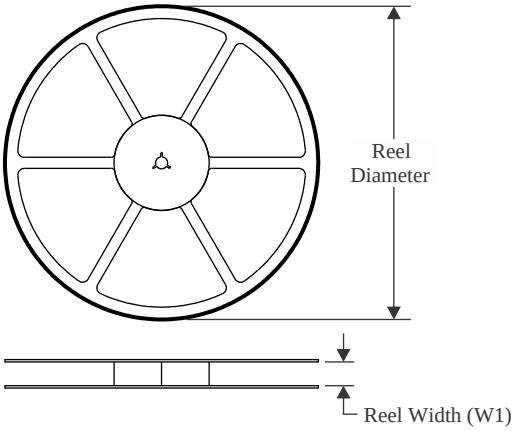
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

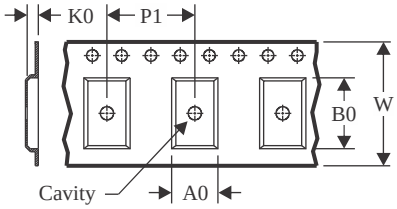
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

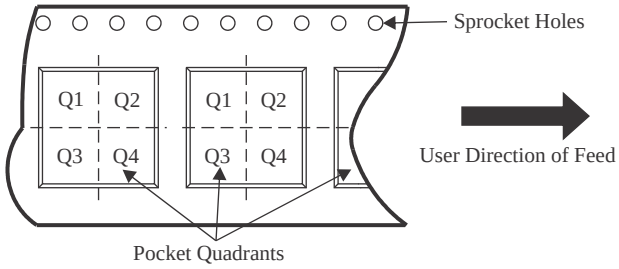


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

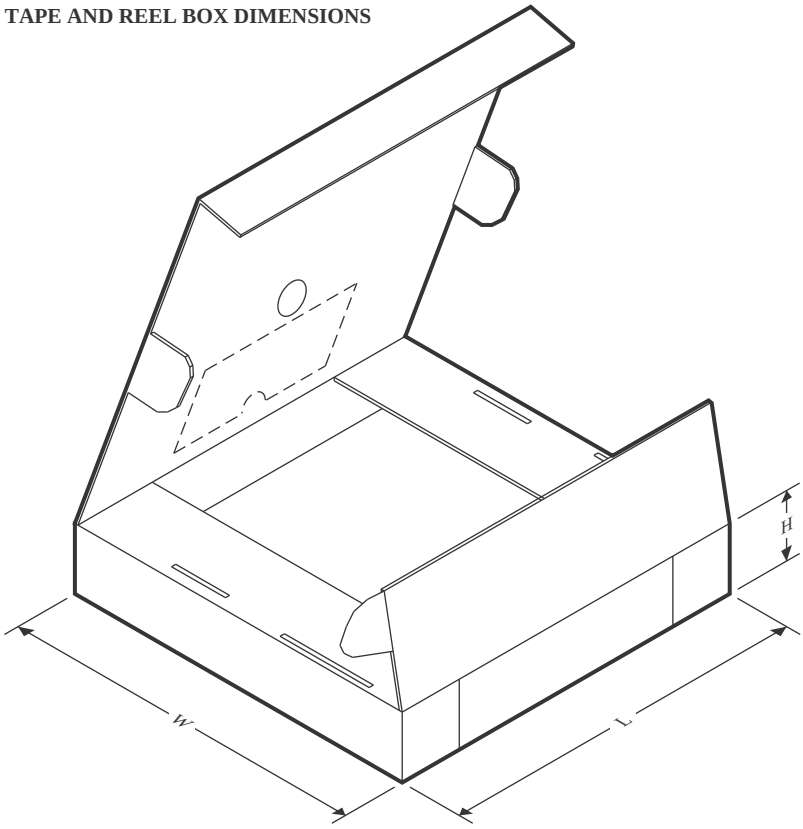
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62821DLCT	VSON-HR	DLC	8	250	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



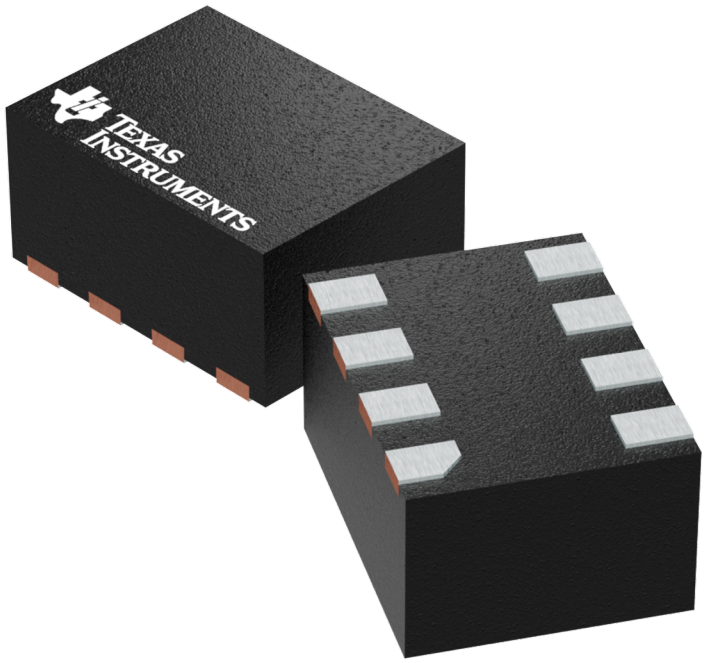
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62821DLCT	VSON-HR	DLC	8	250	341.0	182.0	80.0

DLC 8 VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

2.0 x 1.5 mm, 0.5 mm pitch



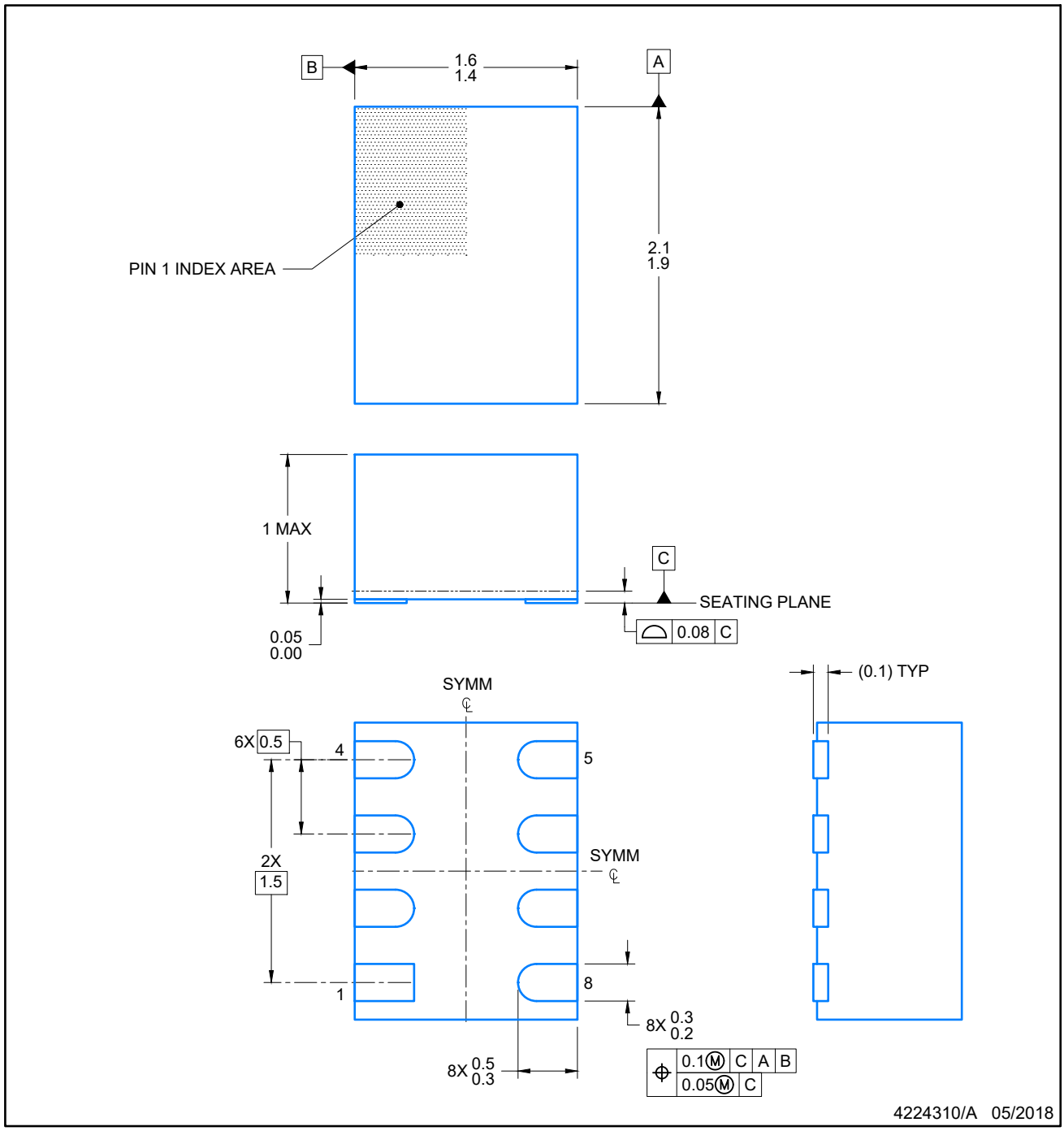
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DLC0008B

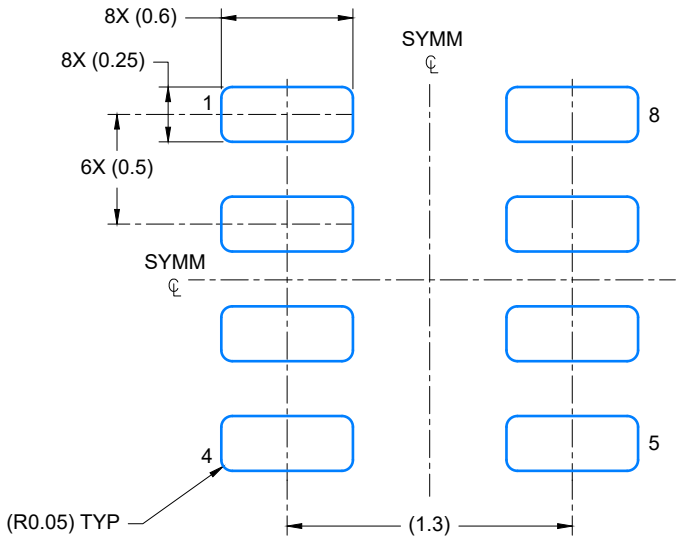
VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE- NO LEAD

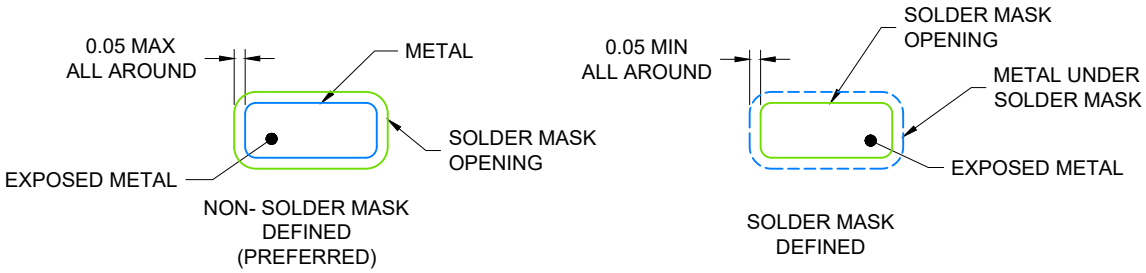


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

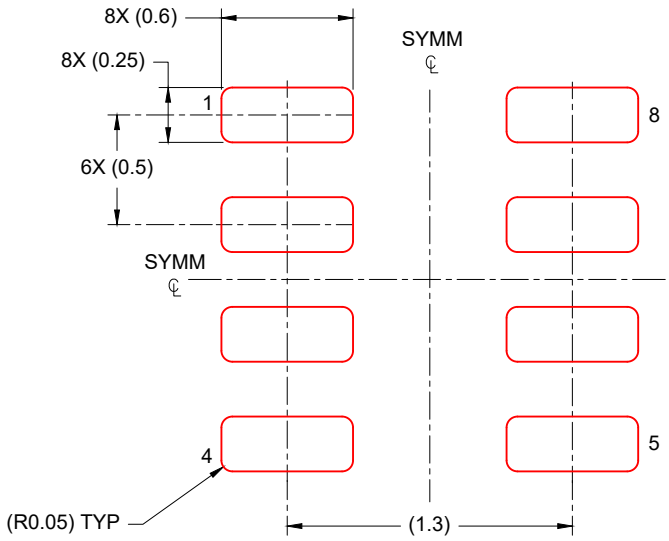


SOLDER MASK DETAILS

4224310/A 05/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224310/A 05/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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