

TPS62748 300/400mA 超低静止電流高効率降圧型コンバータ、負荷スイッチ付き

1 特長

- 入力電圧範囲 V_{IN} : 2.15V~5.5V
- 一度起動した後の入力電圧範囲は最低 2.0V
- 出力電流: 300mA
- 動作時静止電流: 360nA
- 10 μ A 出力電流時に最高 90% の効率
- パワーセーブ・モード動作
- 出力電圧を選択可能
 - 1.2V、1.8V
- 出力電圧放電
- 100mA/2.2 Ω 内蔵負荷スイッチ
- 低出力電圧リップル
- リップルなし 100% モードへの自動遷移
- RF 対応 DCS-Control™
- 基板占有面積 < 10mm²
- 小型の 1.6mm × 0.9mm 8 ボール WCSP パッケージ

2 アプリケーション

- ウェアラブル
- フィットネス・トラッカー
- スマートウォッチ
- 健康状態モニタ
- Bluetooth® Low Energy、RF4CE、Zigbee
- 高効率、超低消費電力のアプリケーション
- エネルギー・ハーベスト

3 概要

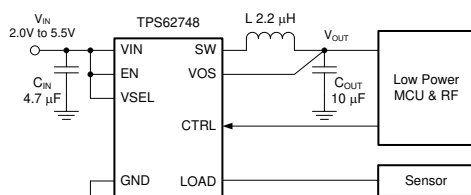
TPS62748 は、静止電流が 360nA (標準値) ときわめて小さい、高効率の降圧型コンバータです。このデバイスは、2.2 μ H のインダクタと 10 μ F の出力コンデンサで動作するよう最適化されています。本デバイスは、DCS-Control™ を使用しており、1.2MHz (標準値) のスイッチング周波数で動作します。パワーセーブ・モードでは、10 μ A 以下の負荷電流範囲まで軽負荷時効率を維持できます。TPS62748 は 300mA の電流を出力します。本デバイスは一度起動すると、最低 2.0V の入力電圧範囲まで動作します。そのため、1 個の Li-MnO₂ ボタン型電池で直接動作させることができます。

TPS62748 は、1 本の電圧選択ピンで選択可能な 2 つのプログラマブルな出力電圧 (1.2V と 1.8V) を備えています。TPS62748 は小さな出力コンデンサだけで、低い出力電圧リップルと低ノイズを実現するよう最適化されています。入力電圧が出力電圧に近づく、デバイスはリップルなしの 100% モードに移行し、出力リップル電圧の増加を防止します。この動作モードでは、デバイスはスイッチングを停止し、ハイサイドの MOSFET スイッチがオンになります。

TPS62748 は、VOS ピンと LOAD ピンの間にオン抵抗 0.6 Ω (標準値) の 100mA 負荷スイッチを備えています。この負荷スイッチは通常、降圧型コンバータの出力電圧をサブシステムに分配するために使用されます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS62748	DSBGA (8)	1.6mm × 0.9mm



代表的なアプリケーション

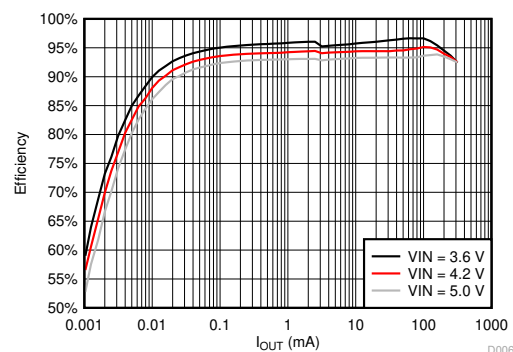


Table of Contents

1 特長	1	8.4 Device Functional Modes.....	10
2 アプリケーション	1	9 Application and Implementation	11
3 概要	1	9.1 Application Information.....	11
4 Revision History	2	9.2 Typical Application.....	11
5 Device Comparison Table	3	10 Power Supply Recommendations	18
6 Pin Configuration and Functions	3	11 Layout	19
7 Specifications	4	11.1 Layout Guidelines.....	19
7.1 Absolute Maximum Ratings.....	4	11.2 Layout Example.....	19
7.2 ESD Ratings.....	4	12 Device and Documentation Support	20
7.3 Recommended Operating Conditions.....	4	12.1 Device Support.....	20
7.4 Thermal Information.....	5	12.2 ドキュメントの更新通知を受け取る方法.....	20
7.5 Electrical Characteristics.....	5	12.3 サポート・リソース.....	20
7.6 Timing Requirements.....	6	12.4 Trademarks.....	20
7.7 Typical Characteristics.....	7	12.5 静電気放電に関する注意事項.....	20
8 Detailed Description	8	12.6 用語集.....	20
8.1 Overview.....	8	13 Mechanical, Packaging, and Orderable Information	20
8.2 Functional Block Diagram.....	8		
8.3 Feature Description.....	8		

4 Revision History

Changes from Revision A (October 2015) to Revision B (March 2021) Page

- 文書全体にわたって表、図、相互参照の採番方法を更新..... **1**

Changes from Revision * (September 2015) to Revision A (October 2015) Page

- 「特長」の箇条書き項目を「動作時静止電流:60nA」から「動作時静止電流:360nA」に変更..... **1**

5 Device Comparison Table

T _A	PART NUMBER	OUTPUT VOLTAGE SETTINGS (VSEL 1 - 3)	OUTPUT CURRENT	PACKAGE MARKING
–40°C to 85°C	TPS62748	1.2 V and 1.8 V (VSEL)	300 mA	TPS748

6 Pin Configuration and Functions

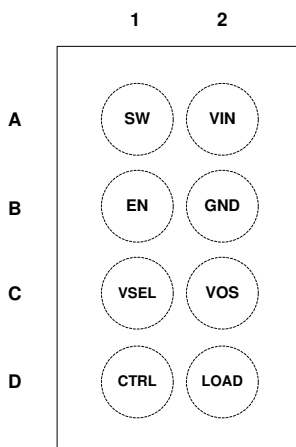


图 6-1. YFP Package 8-Pin DSBGA Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO		
VIN	A2	PWR	V _{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor of 4.7 µF is required.
SW	A1	OUT	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
GND	B2	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VOS	C2	IN	Feedback pin for the internal feedback divider network and regulation loop. An internal load switch is connected between VOUT pin and LOAD pin. Connect this pin directly to the output capacitor with a short trace. Discharges V _{OUT} when the converter is disabled.
VSEL	C1	IN	Output voltage selection pin. See for V _{OUT} selection. This pin must be terminated. The pin can be dynamically changed during operation.
EN	B1	IN	High level enables the devices, low level turns the device into shutdown mode. The pin must be terminated.
CTRL	D1	IN	This pin controls the load switch between VOS and LOAD. With CTRL = low, the LOAD switch is disabled. This pin must be terminated.
LOAD	D2	OUT	Output terminal of the internal load switch. With CTRL = high, the internal load switch connects VOS to the LOAD pin. This pin is pulled to GND with the CTRL = low. If not used, leave the pin open.

表 6-2. Output Voltage Setting TPS62748

DEVICE	V _{OUT}	VSEL
TPS62748	1.2	0
	1.8	1

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Pin voltage ⁽²⁾	VIN	−0.3	6	V
	SW, VSEL, LOAD, CTRL	−0.3	VIN + 0.3V	V
	EN	−0.3	VIN + 0.3V	V
	VOS	−0.3	3.7	V
Operating junction temperature, TJ		−40	125	°C
Storage temperature, Tstg		−65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal GND.

7.2 ESD Ratings

			VALUE	UNIT
V(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
VIN	Supply voltage VIN		2.15		5.5	V
VIN	Supply voltage VIN, once started		2.0		5.5	V
IOUT	Device output current	TPS62743 / TPS627431 5.5V ≥ VIN ≥ (VOUTnom + 0.7V) ≥ 2.15V			300	mA
		5.5V ≥ VIN ≥ (VOUTnom + 0.7V) ≥ 3V			400	
ILOAD	Load switch current				100	mA
TJ	Operating junction temperature range		−40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS62748	UNIT
		YFP	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	103	°C/W
R _{θJCTop}	Junction-to-case (top) thermal resistance	1.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	20	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	20	°C/W
R _{θJCbot}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

V_{IN} = 3.6V, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I _Q	Operating quiescent current	EN = V _{IN} , CTRL = GND, I _{OUT} = 0μA, V _{OUT} = 1.8V, device not switching	360	1800	nA	
		EN = V _{IN} , I _{OUT} = 0mA, CTRL = GND, V _{OUT} = 1.8V , device switching	460			
I _{SD}	Shutdown current	EN = GND, shutdown current into V _{IN}	70	1000	nA	
V _{TH_UVLO+}	Undervoltage	Rising V _{IN}	2.075	2.15	V	
V _{TH_UVLO-}	lockout threshold	Falling V _{IN}	1.925	2		
INPUTS (EN, VSEL, CTRL)						
V _{IH TH}	High level input threshold	2.2V ≤ V _{IN} ≤ 5.5V			1.1	V
V _{IL TH}	Low level input threshold	2.2V ≤ V _{IN} ≤ 5.5V	0.4			V
I _{IN}	Input bias Current			10	25	nA
POWER SWITCHES						
R _{DS(ON)}	High side MOSFET on-resistance	I _{OUT} = 50mA	0.45	1.12	Ω	
	Low Side MOSFET on-resistance		0.22	0.65		
I _{LIMF}	High side MOSFET switch current limit		480	600	720	mA
			590	650	800	
	Low side MOSFET switch current limit	TPS62743	600			
		TPS627431	650			
OUTPUT VOLTAGE DISCHARGE						
R _{DSCH_VOS}	MOSFET on-resistance	EN = GND, I _{VOS} = -10mA into VOS pin	30	65		Ω
I _{IN_VOS}	Bias current into VOS pin	EN = V _{IN} , V _{OUT} = 2V	40	1010		nA
LOAD Switch						
R _{LOAD}	MOSFET on-resistance	I _{LOAD} = 50mA, CTRL = V _{IN} , V _{OUT} = 1.8V, 2.2V ≤ V _{IN} ≤ 5.5V	0.6	1.27		Ω
R _{DCHRG}	MOSFET on-resistance	2.2V ≤ V _{IN} ≤ 5.5V; CTRL=GND	30	65		Ω

$V_{IN} = 3.6V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ typical values are at $T_A = 25^{\circ}C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUTO 100% MODE TRANSITION						
V _{TH_100+}	Auto 100% Mode leave detection threshold ⁽¹⁾	Rising V _{IN} , 100% Mode is left with V _{IN} = V _{OUT} + V _{TH_100+}	150	250	350	mV
V _{TH_100-}	Auto 100% Mode enter detection threshold ⁽¹⁾	Falling V _{IN} , 100% Mode is entered with V _{IN} = V _{OUT} + V _{TH_100-}	85	200	290	
OUTPUT						
I _{LIM_softstart}	High side softstart switch current limit	EN=low to high	80	150	200	mA
	Low side softstart switch current limit		150			
V _{OUT}	Output voltage range	Output voltages are selected with pins VSEL	1.2		1.8	V
	Output voltage accuracy	I _{OUT} = 10mA, V _{OUT} = 1.8V	-2.5	0%	2.5	
		I _{OUT} = 100mA, V _{OUT} = 1.8V	-2	0%	2	
	DC output voltage load regulation	V _{OUT} = 1.8V	0.001			%/mA
	DC output voltage line regulation	V _{OUT} = 1.8V, I _{OUT} = 100mA, 2.2V ≤ V _{IN} ≤ 5.0V	0			%/V

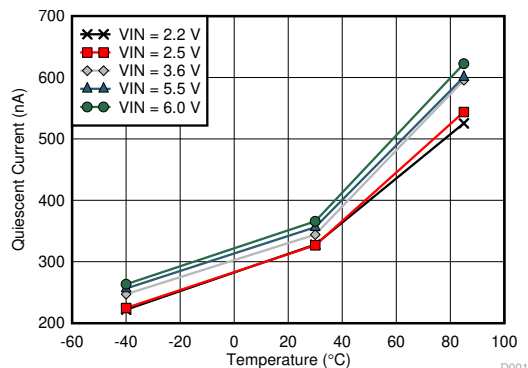
- (1) V_{IN} is compared to the programmed output voltage (V_{OUT}). When $V_{IN}-V_{OUT}$ falls below V_{TH_100-} , the device enters 100% Mode by turning the high side MOSFET on. The 100% Mode is exited when $V_{IN}-V_{OUT}$ exceeds V_{TH_100+} and the device starts switching. The hysteresis for the 100% Mode detection threshold $V_{TH_100+} - V_{TH_100-}$ will always be positive and will be approximately 50 mV(typ)

7.6 Timing Requirements

$V_{IN} = 3.6V$, $T_J = -40^{\circ}C$ to $85^{\circ}C$ typical values are at $T_A = 25^{\circ}C$ (unless otherwise noted)

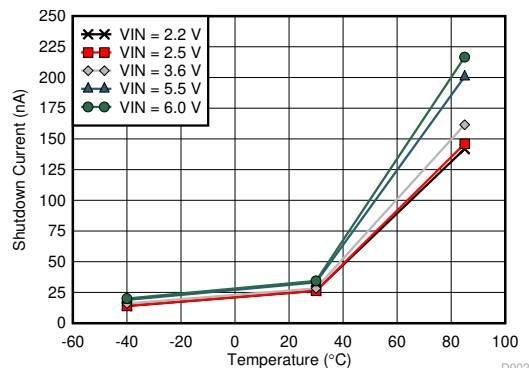
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOAD Switch						
t_{rise_LOAD}	V_{LOAD} rise time	CTRL= low to high, $V_{OUT} = 1.8V$, $2.2V \leq V_{IN} \leq 5.5V$, $I_{LOAD} = 20mA$	315	800		μs
OUTPUT						
t_{ONmin}	Minimum ON time	$V_{OUT} = 2.0V$, $I_{OUT} = 0 mA$	225			ns
t_{OFFmin}	Minimum OFF time	$V_{IN} = 2.3V$	50			ns
$t_{Startup_delay}$	Regulator start up delay time	From transition EN = low to high until device starts switching	10			ms
$t_{Softstart}$	Softstart time	$2.2V \leq V_{IN} \leq 5.5V$, EN = V_{IN}	700	1200		μs

7.7 Typical Characteristics



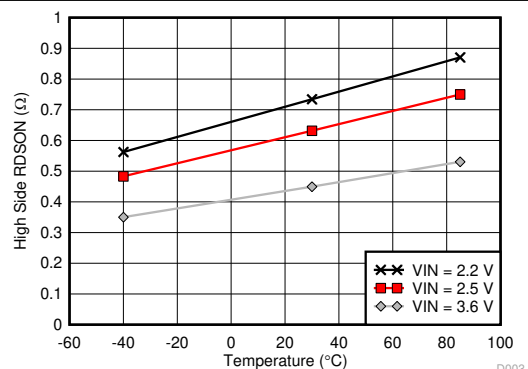
EN = VIN, $V_{OUT} = 1.8V$ Device Not Switching

7-1. Quiescent Current vs Temperature

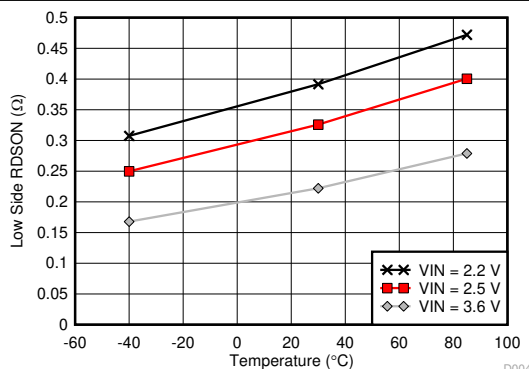


EN = GND

7-2. Shutdown Current I_{SD} vs Temperature



7-3. High Side $R_{DS(on)}$ vs Temperature



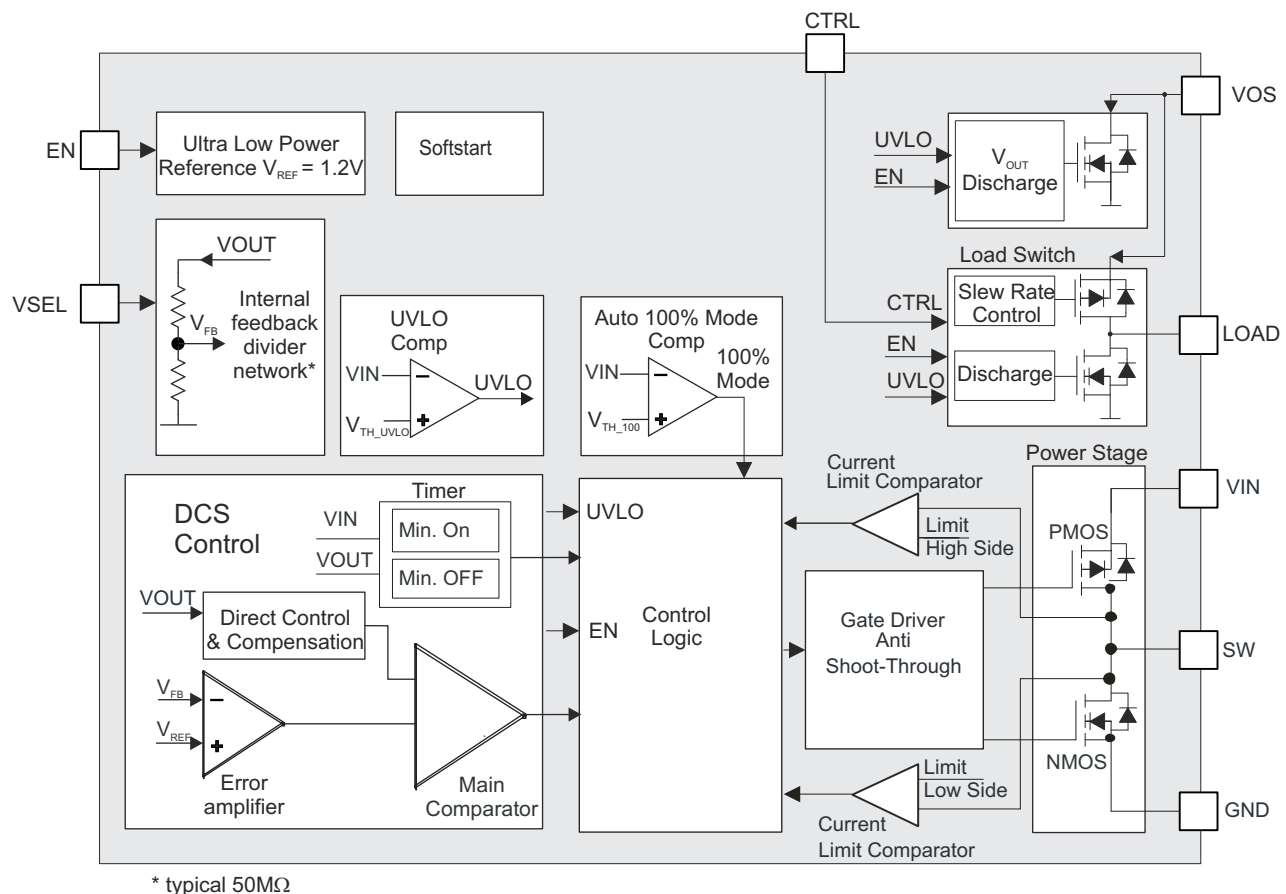
7-4. Low-side $R_{DS(on)}$ vs Temperature

8 Detailed Description

8.1 Overview

The TPS62748 is a high frequency step down converter with ultra low quiescent current. The device operates with a quasi fixed switching frequency typically at 1.2 MHz. Using TI's DCS-Control™ topology the device extends the high efficiency operation area down to a few microamperes of load current during Power Save Mode Operation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DCS-Control™

TI's DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and high load conditions and a Power Save Mode at light loads. During PWM mode, it operates in continuous conduction mode. The switching frequency is typically 1.2 MHz with a controlled frequency variation depending on the input voltage and load current. If the load current decreases, the converter seamlessly enters Power Save Mode to

maintain high efficiency down to very light loads. In Power Save Mode, the switching frequency varies linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless with minimum output voltage ripple. The TPS62748 offers both excellent DC voltage and superior load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

8.3.2 Power Save Mode Operation

In Power Save Mode the device operates in PFM (Pulse Frequency Modulation) that generates a single switching pulse to ramp up the inductor current and recharges the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption of TPS62748 is reduced to 360 nA. This low quiescent current consumption is achieved by an ultra low power voltage reference, an integrated high impedance feedback divider network and an optimized Power Save Mode operation.

8.3.3 100mA Load Switch

The load switch connects VOS pin to the LOAD pin and is able to support 100 mA. The on-resistance depends on the output voltage. At 1.2 V Vout the on-resistance is maximum 2.2 Ω and at 1.8 V Vout the on-resistance is maximum 1.2 Ω . The load switch can be used to power a sub system. With CTRL=high the load switch is turned on. To avoid a voltage drop at the output of the buck converter the load switch has a internal softstart. With CTRL=low the load switch is turned off and the LOAD pin is internally discharged to GND by typically 30 Ω . This makes sure the output of the load switch is always discharged to GND before the load switch is turned on again.

8.3.4 Output Voltage Selection

The TPS62748 doesn't require an external resistor divider network to program the output voltage. The device integrates a high impedance feedback resistor divider network which is programmed by the pin VSEL. TPS62748 supports two output voltage options: 1.2 V and 1.8 V. The output voltage is programmed according to [表 6-2](#). The output voltage can be changed during operation and supports a simple dynamic output voltage scaling.

8.3.5 Output Voltage Discharge of the Buck Converter

The device provides automatic output voltage discharge when EN is pulled low or the UVLO is triggered. The output of the buck converter is discharged over VOS. Because of this the output voltage will ramp up from zero once the device is enabled again. This is very helpful for accurate start-up sequencing.

8.3.6 Undervoltage Lockout UVLO

To avoid misoperation of the device at low input voltages, an undervoltage lockout is used. The UVLO shuts down the device at a maximum voltage level of 2.0 V. The device will start at a UVLO level of 2.15 V.

8.3.7 Short circuit protection

The TPS6274x integrates a current limit on the high side, as well on the low side MOSFETs to protect the device against overload or short circuit conditions. The peak current in the switches is monitored cycle by cycle. If the high side MOSFET current limit is reached, the high side MOSFET is turned off and the low side MOSFET is turned on until the switch current decreases below the low side MOSFET current limit. Once the low side MOSFET current limit trips, the low side MOSFET is turned off and the high side MOSFET turns on again.

8.4 Device Functional Modes

8.4.1 Enable and Shutdown

The device is turned on with EN=high. With EN=low the device enters shutdown and turns off the load switch. This pin must be terminated.

8.4.2 Device Start-up and Softstart

The device has an internal softstart to minimize input voltage drop during start-up. This allows the operation from high impedance battery cells. Once the device is enabled the device starts switching after a typical delay time of 10ms. Then the softstart time of typical 700 μ s begins with a reduced current limit of typical 150 mA. When this time passed by the device enters full current limit operation. This allows a smooth start-up and the device can start into full load current. Furthermore, larger output capacitors impact the start-up behaviour of the DC/DC converter. Especially when the output voltage does not reach its nominal value after the typical soft-start time of 700 μ s, has passed.

8.4.3 Automatic Transition Into No Ripple 100% Mode

Once the input voltage comes close to the output voltage, the DC/DC converter stops switching and enters 100% duty cycle operation. It connects the output V_{OUT} via the inductor and the internal high side MOSFET switch to the input V_{IN} , once the input voltage V_{IN} falls below the 100% mode enter threshold, V_{TH_100-} . The DC/DC regulator is turned off, switching stops and therefore no output voltage ripple is generated. Since the output is connected to the input, the output voltage follows the input voltage minus the voltage drop across the internal high side switch and the inductor. Once the input voltage increases and trips the 100% mode exit threshold, V_{TH_100+} , the DC/DC regulator turns on and starts switching again. See [Figure 8-1](#) and [Figure 9-20](#).

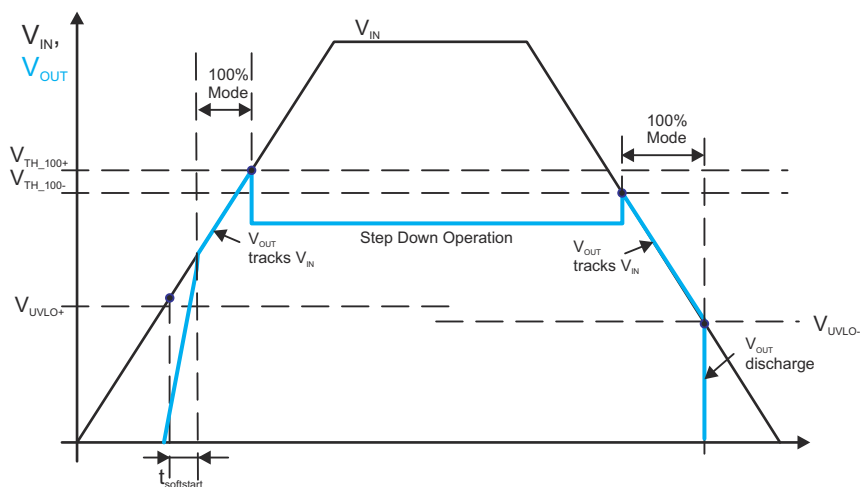


Figure 8-1. Automatic Transition into 100% Mode

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TPS62748 is a high efficiency step down converter with ultra low quiescent current of typically 360 nA. The device operates with a tiny 2.2- μ H inductor and 10- μ F output capacitor over the entire recommended operation range. A dedicated measurement set-up is required for the light load efficiency measurement and device quiescent current due to the operation in the sub microampere range. In this range any leakage current in the measurement set-up will impact the measurement results.

9.2 Typical Application

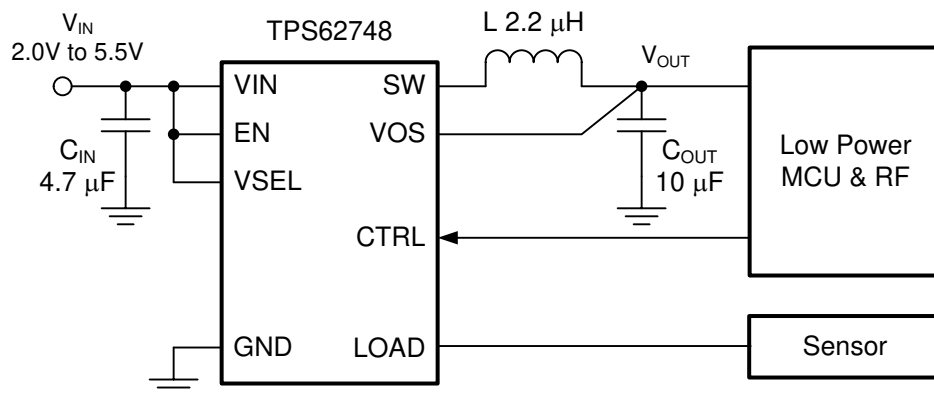


図 9-1. TPS62748 Typical Application Circuit

9.2.1 Design Requirements

The TPS62748 is a highly integrated DC/DC converter. The output voltage is set via a VSEL pin interface. The design guideline provides a component selection to operate the device within the recommended operating conditions.

表 9-1 shows the list of components for the Application Characteristic Curves.

表 9-1. Components for Application Characteristic Curves

Reference	Description	Value	Manufacturer
TPS62748	360nA Iq step down converter		Texas Instruments
CIN	Ceramic capacitor, GRM155R61C475ME15	4.7 μF	Murata
COUT	Ceramic capacitor, GRM155R60J106ME11	10 μF	Murata
L	Inductor DFE201610C	2.2 μH	Toko

9.2.2 Detailed Design Procedure

The first step in the design procedure is the selection of the output filter components. To simplify this process, [表 9-2](#) outlines possible inductor and capacitor value combinations.

表 9-2. Recommended LC Output Filter Combinations

Inductor Value [μH] ⁽²⁾	Output Capacitor Value [μF] ⁽¹⁾				
	4.7μF	10μF	22μF	47μF	100μF
2.2	√	√ ⁽³⁾	√	√	

(1) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and –50%.

(2) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -30%.

(3) Typical application configuration. Other check marks indicate alternative filter combinations.

9.2.2.1 Inductor Selection

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to [式 1](#).

[式 2](#) calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with equation 2. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit, I_{LIMF} .

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- f = Switching Frequency
- L = Inductor Value
- ΔI_L = Peak to Peak inductor ripple current
- I_{Lmax} = Maximum Inductor current

[表 9-3](#) shows a list of possible inductors.

表 9-3. List of Possible Inductors⁽¹⁾

INDUCTANCE [μH]	DIMENSIONS [mm ³]	INDUCTOR TYPE	Isat/DCR	SUPPLIER	Comment
2.2	2.0 x 1.6 x 1.0	DFE201610C	1.4 A/170 mΩ	TOKO	Efficiency plot  9-8
2.2	2.0 x 1.25 x 1.0	MIPSZ2012D 2R2	0.7 A/230 mΩ	FDK	
2.2	2.0 x 1.2 x 1.0	744 797 752 22	0.7 A/200 mΩ	Würth Elektronik	
2.2	1.6 x 0.8 x 0.8	MDT1608-CH2R2M	0.7 A/300 mΩ	TOKO	

(1) See [Third-party Products Disclaimer](#)

9.2.2.2 Output Capacitor Selection

The DCS-Control™ scheme of the TPS62748 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple. The leakage current of the output capacitor adds to the overall quiescent current.

9.2.2.3 Input Capacitor Selection

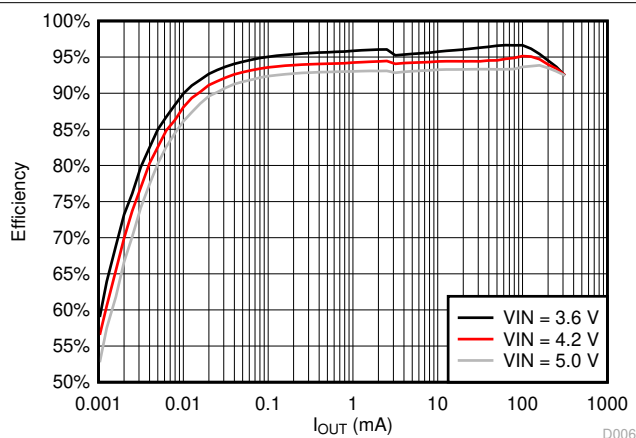
Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications a 4.7-μF input capacitor is sufficient. When operating from a high impedance source, like a coin cell a larger input buffer capacitor ≥10μF is recommended avoiding voltage drops during start-up and load transients. The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall quiescent current. [表 9-4](#) shows a selection of input and output capacitors.

表 9-4. List of Possible Capacitors⁽¹⁾

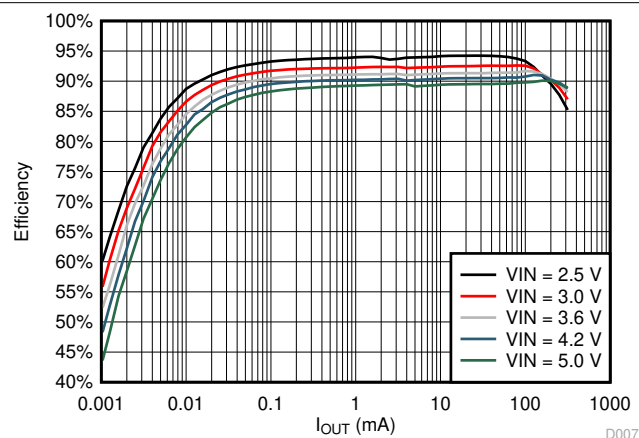
CAPACITANCE [μF]	SIZE	CAPACITOR TYPE	SUPPLIER
4.7	0402	GRM155R61C475ME15	Murata
10	0402	GRM155R60J106ME11	Murata

(1) See [Third-party Products Disclaimer](#)

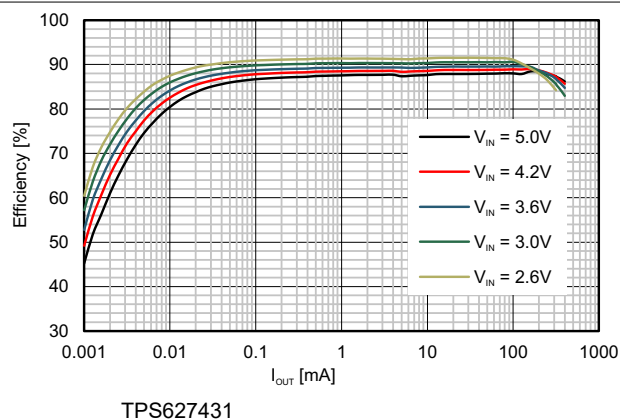
9.2.3 Application Curves



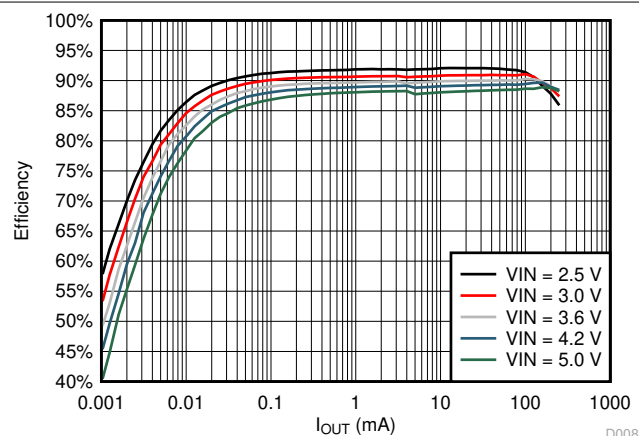
9-2. Efficiency vs Load Current, $V_{OUT} = 3.3\text{ V}$



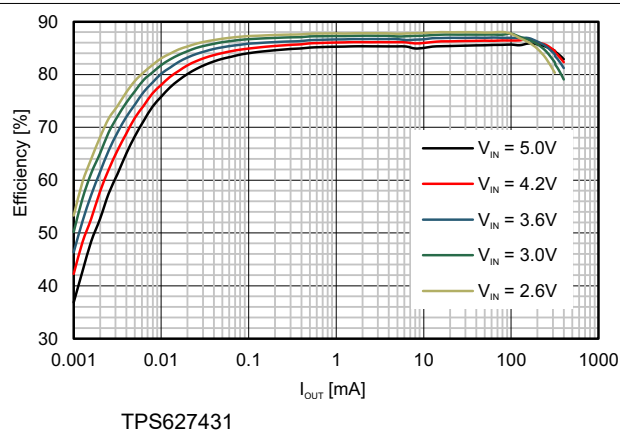
9-3. Efficiency vs Load Current; $V_{OUT} = 2.1\text{ V}$



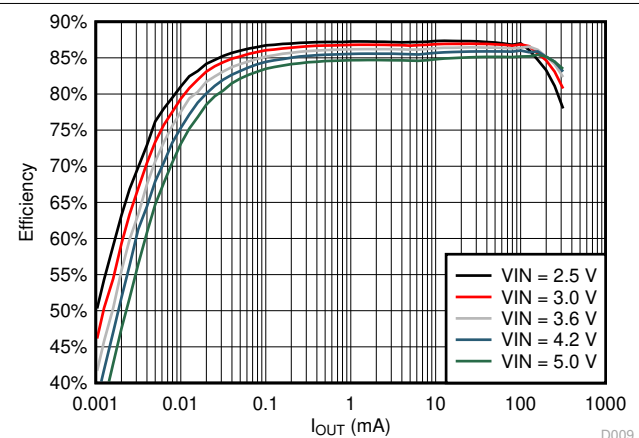
9-4. Efficiency vs Load Current; $V_{OUT} = 1.9\text{ V}$



9-5. Efficiency vs Load Current; $V_{OUT} = 1.8\text{ V}$

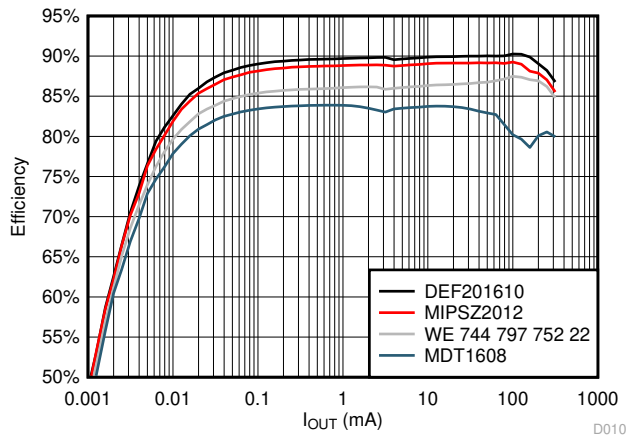


9-6. Efficiency vs Load Current; $V_{OUT} = 1.4\text{ V}$

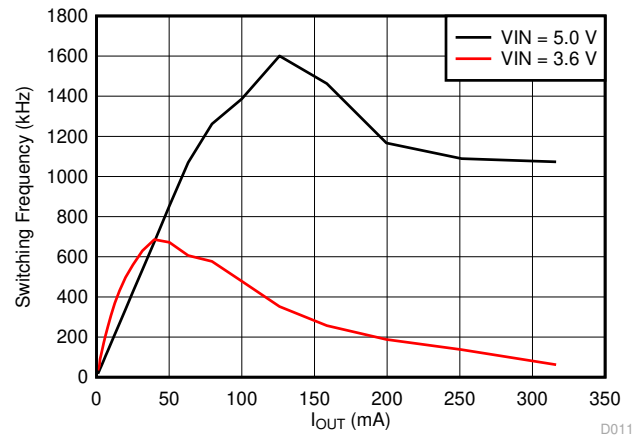


9-7. Efficiency vs Load Current; $V_{OUT} = 1.2\text{ V}$

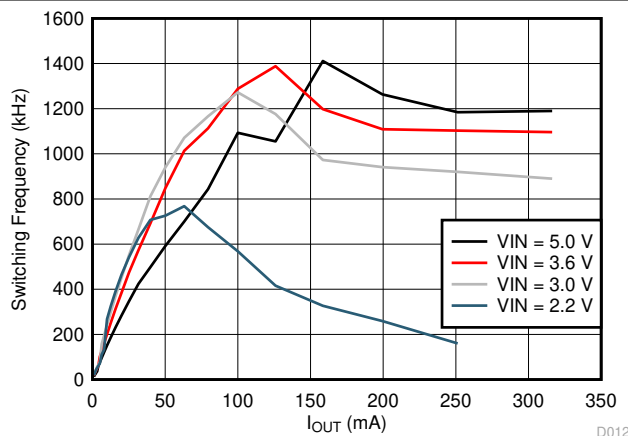
9.2.3 Application Curves (continued)



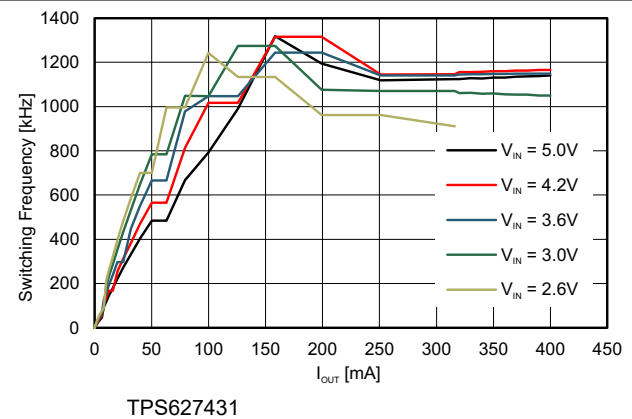
9-8. Efficiency vs Load Current; $V_{OUT} = 1.8\text{ V}$



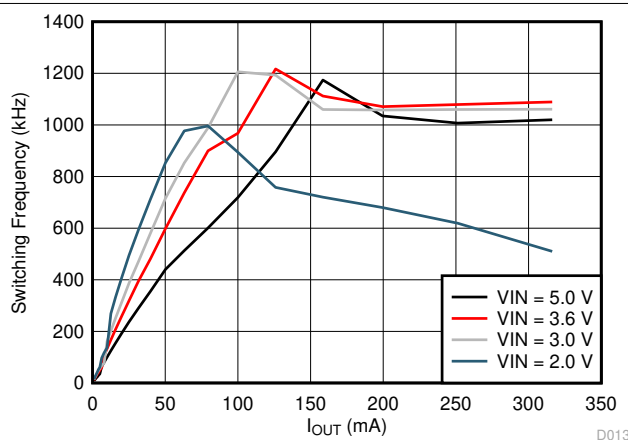
9-9. Switching Frequency vs Load Current $V_{OUT} = 3.3\text{ V}$



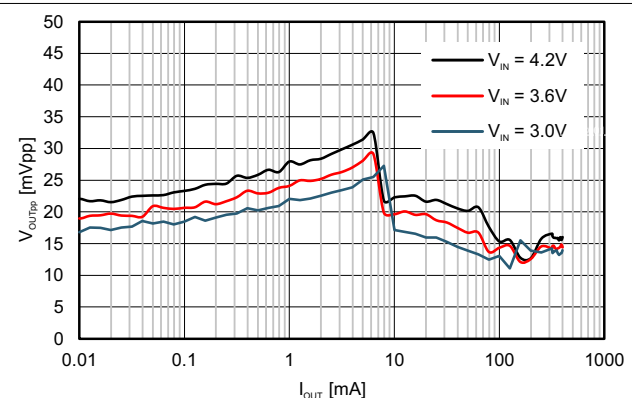
9-10. Switching Frequency vs Load Current $V_{OUT} = 1.8\text{ V}$



9-11. Switching Frequency vs Load Current $V_{OUT} = 1.4\text{ V}$



9-12. Switching Frequency vs Load Current $V_{OUT} = 1.2\text{ V}$



9-13. Typical Output Ripple Voltage $V_{OUT} = 1.4\text{ V}$

9.2.3 Application Curves (continued)



FIG 9-14. PFM (Power Save Mode) Mode Operation

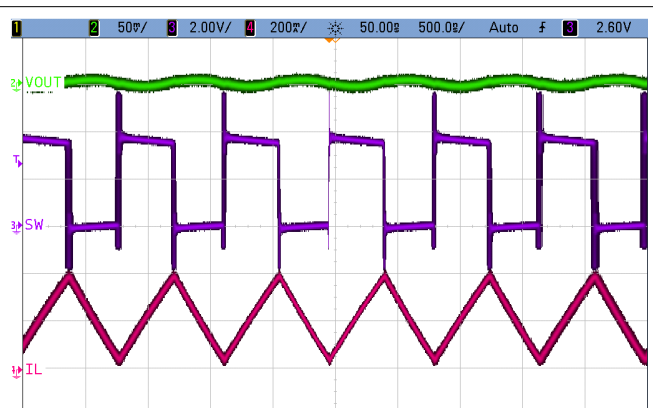


FIG 9-15. PWM Mode Operation

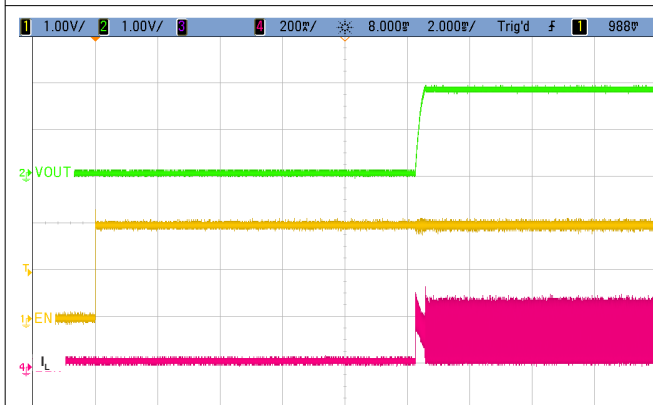


FIG 9-16. Startup Into 100 mA Electronic Load EN Delay + Soft-Start Delay

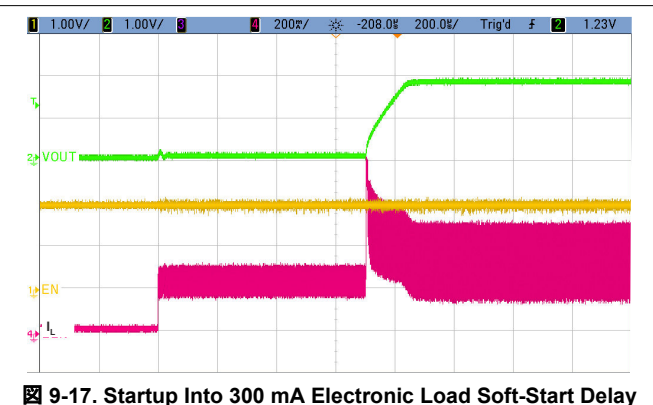


FIG 9-17. Startup Into 300 mA Electronic Load Soft-Start Delay

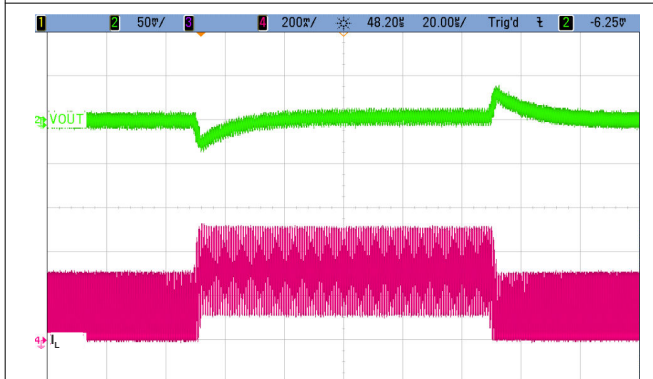


FIG 9-18. Load Transient Response; 100 mA to 290 mA

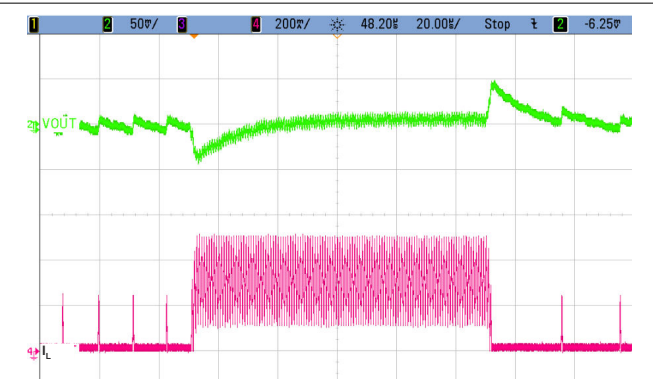
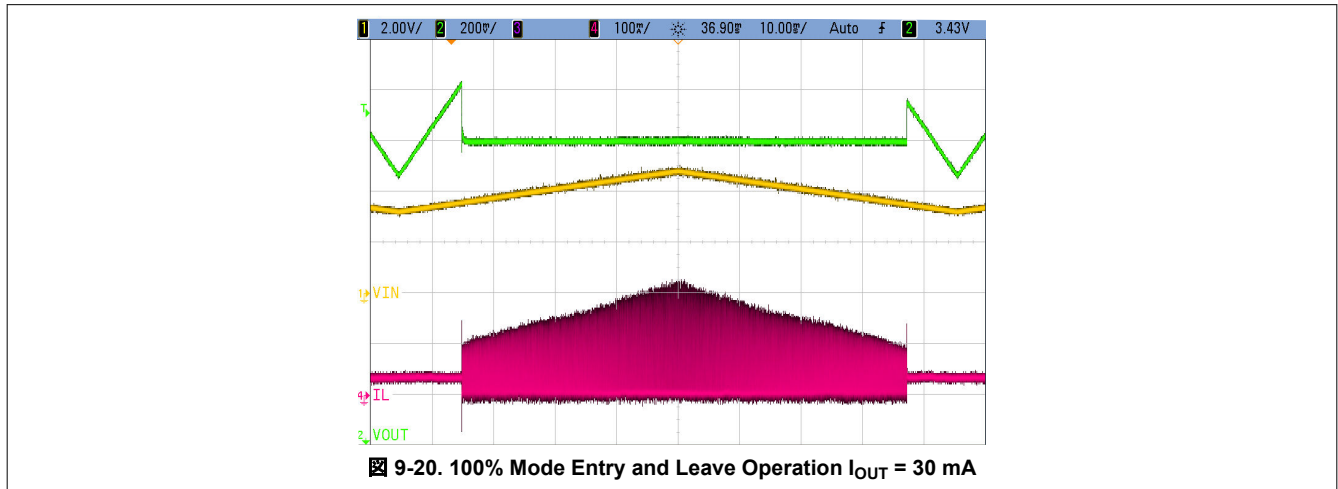


FIG 9-19. Load Transient Response; 5 mA to 290 mA

9.2.3 Application Curves (continued)



10 Power Supply Recommendations

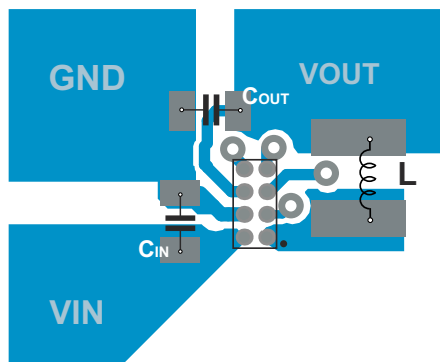
The power supply must provide a current rating according to the supply voltage, output voltage and output current of the TPS62748.

11 Layout

11.1 Layout Guidelines

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor should be placed as close as possible to the IC pins VIN and GND. This is the most critical component placement.
- The V_{OS} line is a sensitive high impedance line and should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line) or other noise sources.

11.2 Layout Example



11-1. Recommended PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

12.4 Trademarks

DCS-Control™ and TI E2E™ are trademarks of Texas Instruments.

Bluetooth® is a registered trademark of Bluetooth SIG, Inc.

すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

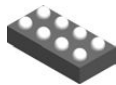
ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

[TI 用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

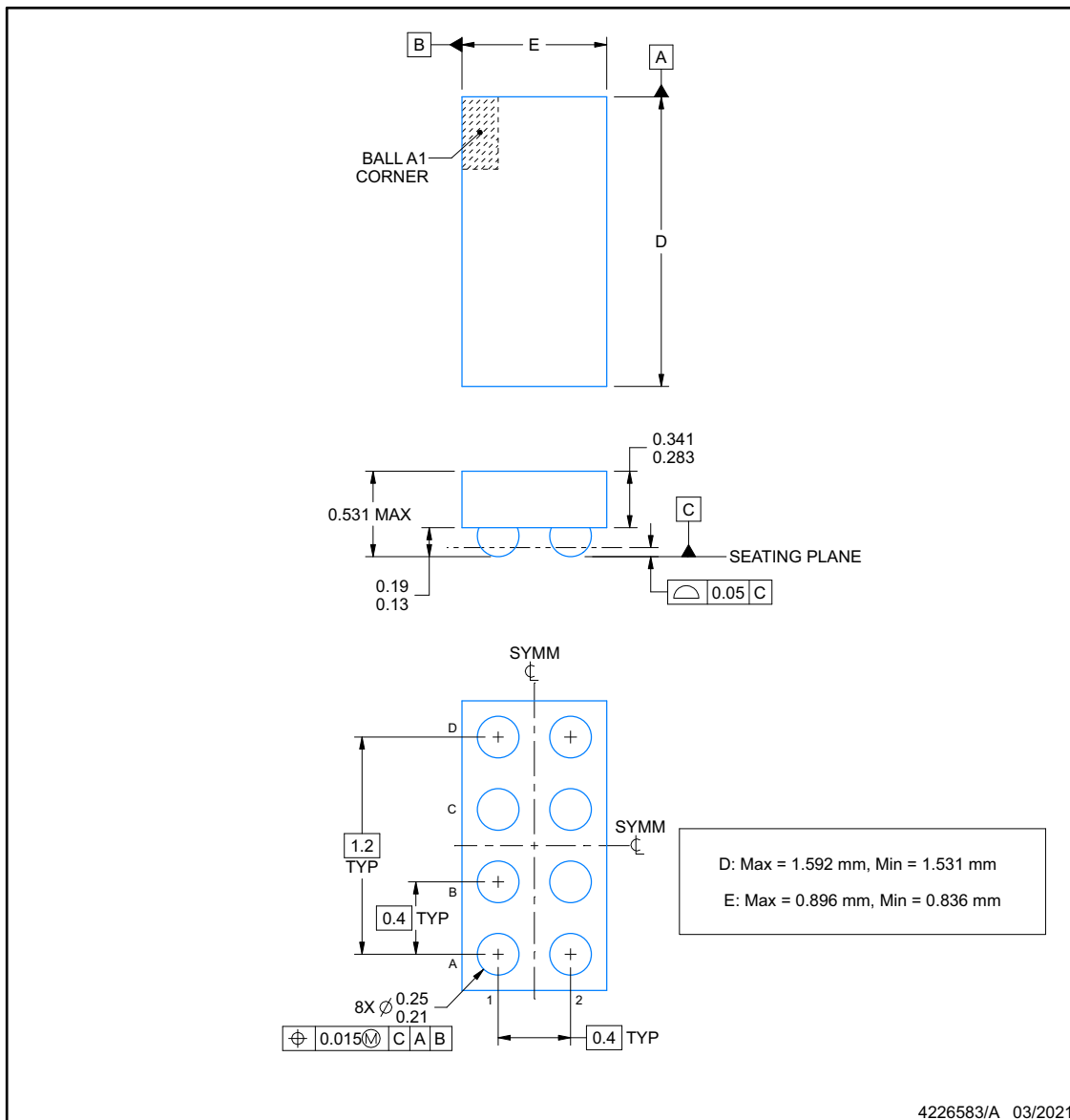


PACKAGE OUTLINE

YFP0008-C01

DSBGA - 0.531 mm max height

DIE SIZE BALL GRID ARRAY

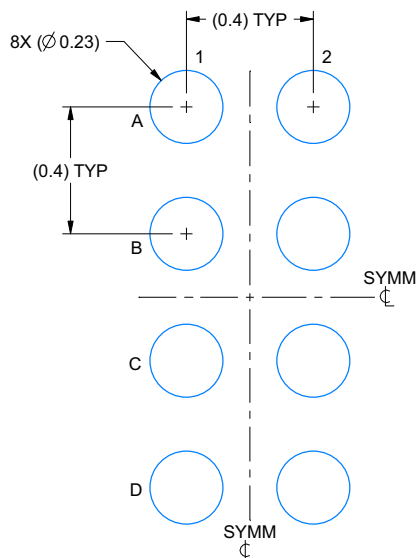


NOTES:

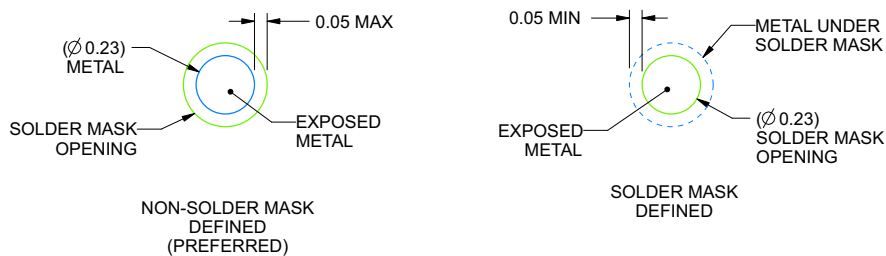
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT**YFP0008-C01****DSBGA - 0.531 mm max height**

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE: 50X



SOLDER MASK DETAILS
 NOT TO SCALE

4226583/A 03/2021

NOTES: (continued)

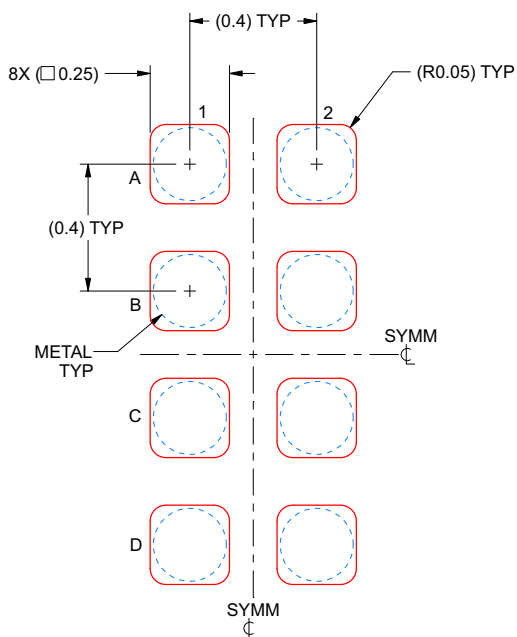
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
 See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0008-C01

DSBGA - 0.531 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4226583/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62748YFPR	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS748
TPS62748YFPR.B	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS748
TPS62748YFPT	Active	Production	DSBGA (YFP) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS748
TPS62748YFPT.B	Active	Production	DSBGA (YFP) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS748

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

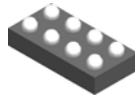
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

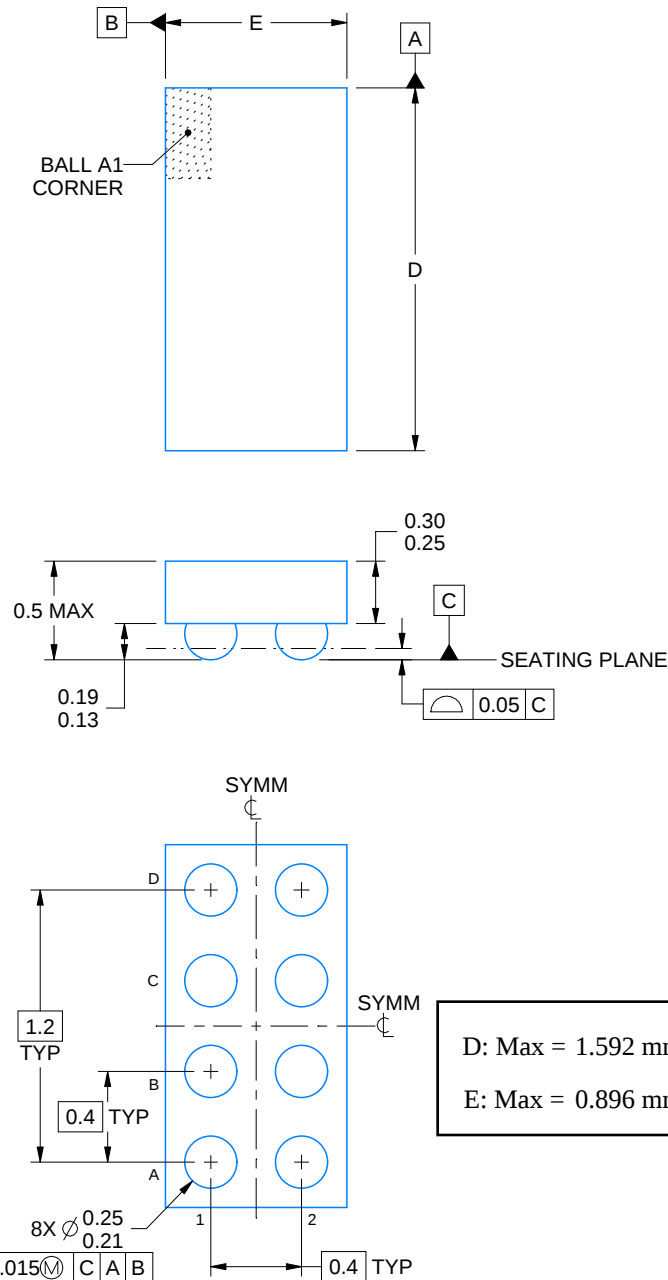
YFP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4225242/A 08/2019

NOTES:

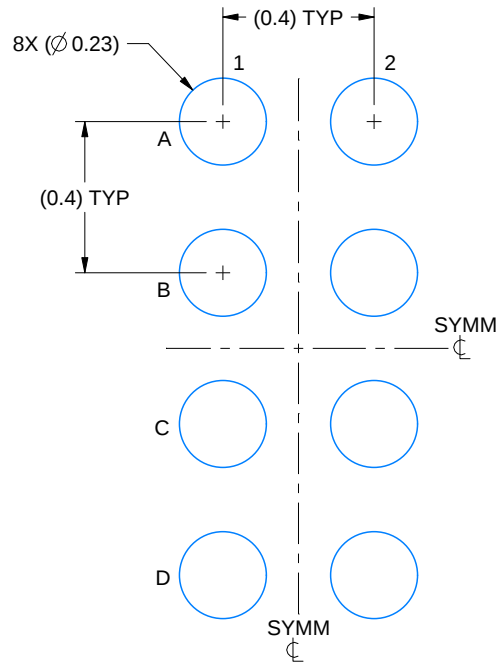
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

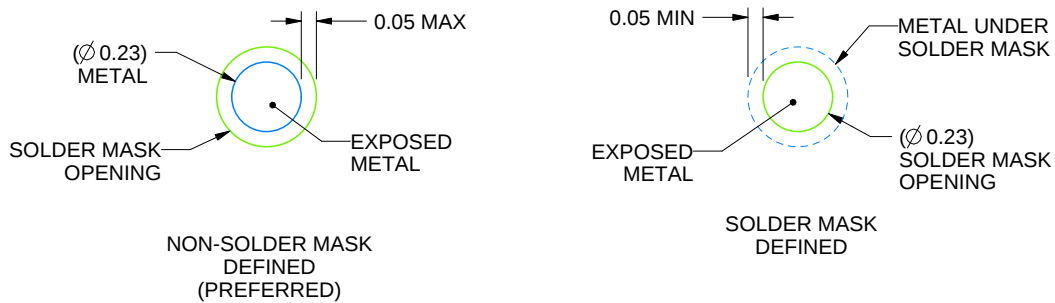
YFP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

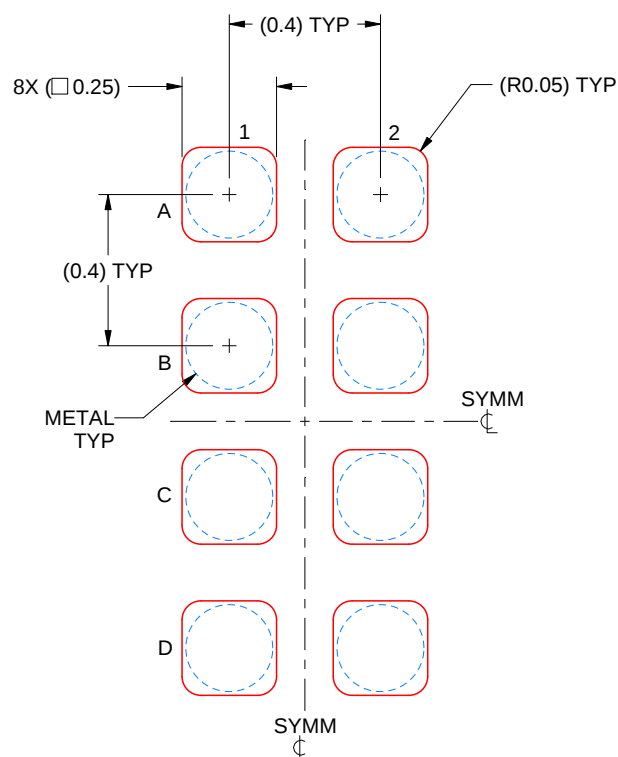


SOLDER MASK DETAILS
NOT TO SCALE

4225242/A 08/2019

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
 BASED ON 0.1 mm THICK STENCIL
 SCALE: 50X

4225242/A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月