# TPS6274x 360nA $I_Q$ Step Down Converter For Low Power Applications

## 1 Features

- Input Voltage Range $V_{IN}$ from 2.2V to 5.5
- Typ. 360nA Quiescent Current
- Up to 90% Efficiency at 10µA Output Current
- Up to 300mA / 400mA Output Current (TPS62740/TPS62742)
- RF Friendly DCS-Control ™
- Up to 2 MHz Switching Frequency
- Low Output Ripple Voltage
- 16 Selectable Output Voltages in 100mV Steps between 1.8V to 3.3V
- Automatic Transition to No Ripple 100% Mode
- Slew Rate Controlled Load Switch
- Discharge Function on VOUT / LOAD
- Power Good Output
- Optimized for Operation with a Tiny 2.2µH Inductor and 10µF $C_{OUT}$
- Total Solution Size <31mm$^2$
- Small 2 x 3 mm$^2$ WSON Package

## 2 Applications

- *Bluetooth*® Low Energy, RF4CE, Zigbee
- Industrial Metering
- Energy Harvesting

## 3 Description

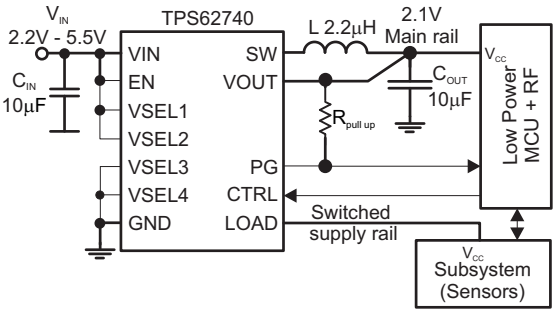
The TPS6274x is industry's first step down converter featuring typ. 360nA quiescent current and operating with a tiny 2.2µH inductor and 10µF output capacitor. This new DCS-Control™ based device extends the light load efficiency range below 10µA load currents. TPS62740 supports output currents up to 300mA, TPS62742 up to 400mA. The device operates from rechargeable Li-Ion batteries, Li-primary battery chemistries such as Li-SOCl2, Li-MnO2 and two or three cell alkaline batteries. The input voltage range up to 5.5V allows also operation from a USB port and thin-film solar modules. The output voltage is user selectable by four VSEL pins within a range from 1.8V to 3.3V in 100mV steps. TPS6274x features low output ripple voltage and low noise with a small output capacitor. Once the battery voltage comes close to the output voltage (close to 100% duty cycle) the device enters no ripple 100% mode operation to prevent an increase of output ripple voltage. The device then stops switching and the output is connected to the input voltage. The integrated slew rate controlled load switch provides typ. 0.6Ω on-resistance and can distribute the selected output voltage to a temporarily used sub-system. The TPS6274x is available in a small 12 pin 2 × 3mm$^2$ WSON package and supports a total solutions size of 31mm$^2$.

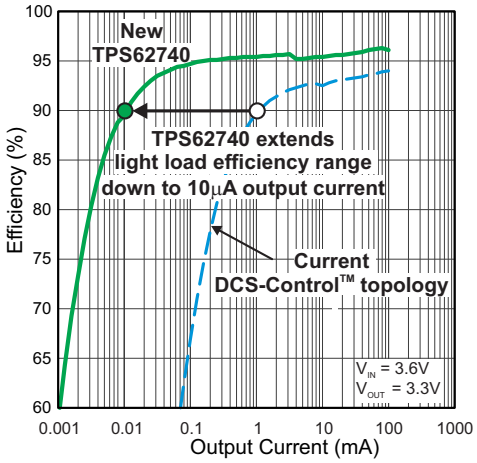
**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS62740 | WSON | 3.00 mm × 2.00 mm |
| TPS62742 | | |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Typical Application



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## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (November 2013) to Revision B | Page |
|---|---|
| • Added TPS62742 device | 1 |
| • Added efficiency graph, Figure 11 | 15 |

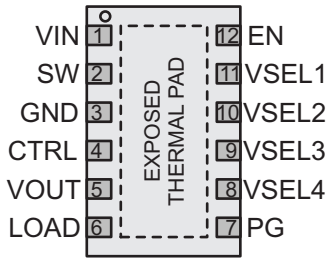
# 6 Device Comparison Table

| $T_A$ | PART NUMBER | OUTPUT VOLTAGE SETTING VSEL 1 - 4 | OUTPUT CURRENT [mA] | PACKAGE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | TPS62740 | 1.8V to 3.3V in 100mV steps | 300mA | 62740 |
| | TPS62741 (1) | 1.3V to 2.8V in 100mV steps | 300mA | -/- |
| | TPS62742 | 1.8V to 3.3V in 100mV steps | 400mA | 62742 |

(1) Device option, contact TI for more details

# 7 Pin Configuration and Functions

**WSON PACKAGE**
**12-Pin**
DSS PACKAGE
(TOP VIEW)




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO | | |
| VIN | 1 | PWR | $V_{IN}$ power supply pin. Connect this pin close to the VIN terminal of the input capacitor. A ceramic capacitor of 4.7µF is required. |
| SW | 2 | OUT | This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal. |
| GND | 3 | PWR | GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor. |
| CTRL | 4 | IN | This pin controls the output LOAD pin. With CTRL = low, the output LOAD is disabled. This pin must be terminated. |
| VOUT | 5 | IN | Feedback pin for the internal feedback divider network and regulation loop. An internal load switch is connected between this pin and the LOAD pin. Connect this pin directly to the output capacitor with a short trace. |
| LOAD | 6 | OUT | This output is controlled by the CTRL Pin. With CTRL high, an internal load switch connects the LOAD pin to the VOUT pin. The LOAD pin allows to connect / disconnect other system components to the output of the DC/DC converter. This pin is pulled to GND with CTRL pin = low. The LOAD pin features a soft switching. If not used, leave the pin open. |
| PG | 7 | OUT | Power good open drain output. This pin is high impedance to indicate "Power Good". Connect a external pull up resistor to generate a "high" level. If not used, this pin can be left open. |
| VSEL4 | 8 | IN | Output voltage selection pins. See Table 1 for $V_{OUT}$ selection. These pins must be terminated and can be changed during operation. |
| VSEL3 | 9 | IN | |
| VSEL2 | 10 | IN | |
| VSEL1 | 11 | IN | |
| EN | 12 | IN | High level enables the devices, low level turns the device into shutdown mode. This pin must be terminated. |
| EXPOSED THERMAL PAD | | NC | Not electrically connected to the IC, but must be soldered. Connect this pad to GND and use it as a central GND plane. |

**Table 1. Output Voltage Setting**

| Device | VOUT | VSEL 4 | VSEL 3 | VSEL 2 | VSEL 1 |
|---|---|---|---|---|---|
| TPS62740 / 42 | 1.8 | 0 | 0 | 0 | 0 |
| | 1.9 | 0 | 0 | 0 | 1 |
| | 2.0 | 0 | 0 | 1 | 0 |
| | 2.1 | 0 | 0 | 1 | 1 |
| | 2.2 | 0 | 1 | 0 | 0 |
| | 2.3 | 0 | 1 | 0 | 1 |
| | 2.4 | 0 | 1 | 1 | 0 |
| | 2.5 | 0 | 1 | 1 | 1 |
| | 2.6 | 1 | 0 | 0 | 0 |
| | 2.7 | 1 | 0 | 0 | 1 |
| | 2.8 | 1 | 0 | 1 | 0 |
| | 2.9 | 1 | 0 | 1 | 1 |
| | 3.0 | 1 | 1 | 0 | 0 |
| | 3.1 | 1 | 1 | 0 | 1 |
| | 3.2 | 1 | 1 | 1 | 0 |
| | 3.3 | 1 | 1 | 1 | 1 |

# 8 Specifications

## 8.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Pin voltage(2) | VIN | | –0.3 | 6 | V |
| | SW (3) | | –0.3 | $V_{IN}$ +0.3V | V |
| | EN, CTRL, VSEL1-4 | | –0.3 | $V_{IN}$ +0.3V | V |
| | PG | | –0.3 | $V_{IN}$ +0.3V | V |
| | VOUT, LOAD | | –0.3 | 3.7 | V |
| PG pin | $I_{PG}$ | sink current | | 10 | mA |
| Maximum operating junction temperature, $T_J$ | | | –40 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) The MAX value $V_{IN}$ +0.3V applies for applicative operation (device switching), DC voltage applied to this pin may not exceed 4V

## 8.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Supply voltage $V_{IN}$ (1) | | | 2.2 | | 5.5 | V |
| $I_{OUT}$ + $I_{LOAD}$ | Device output current (sum of $I_{OUT}$ and $I_{LOAD}$) | $V_{OUTnom}$ + 0.7V ≤ $V_{IN}$ ≤ 5.5V | TPS62740 | | | 300 | mA |
| | | 3V ≤ $V_{IN}$, $V_{OUTnom}$ + 0.7V ≤ $V_{IN}$ ≤ 5.5V | TPS62742 | | | 400 | |
| | | $V_{OUTnom}$ ≤ $V_{IN}$ ≤ $V_{OUTnom}$ +0.7V | | | | 100 | |
| $I_{LOAD}$ | Load current (current from LOAD pin) | | | | | 100 | |
| L | Inductance | | | 1.5 | 2.2 | 3.3 | µH |
| $C_{OUT}$ | Output capacitance connected to VOUT pin (not including LOAD pin) | | | | | 22 | µF |
| $C_{LOAD}$ | Capacitance connected to LOAD pin | | | | | 10 | |
| $T_J$ | Operating junction temperature range | | | -40 | | 125 | °C |
| $T_A$ | Ambient temperature range | | | -40 | | 85 | |

(1) The minimum required supply voltage for startup is 2.15V (undervoltage lockout threshold $V_{TH\_UVLO+}$) . The device is functional down to 2V supply voltage (falling undervoltage lockout threshold $V_{TH\_UVLO-}$).

## 8.4 Thermal Information

| THERMAL METRIC | | DSS / 12 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 61.8 | °C/W |
| $R_{\theta JCtop}$ | Junction-to-case (top) thermal resistance | 70.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 25.7 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 25.7 | |
| $R_{\theta JCbot}$ | Junction-to-case (bottom) thermal resistance | 7.2 | |

## 8.5 Electrical Characteristics

$V_{IN}$ = 3.6V, $T_A$ = –40°C to 85°C typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $V_{IN}$ | Input voltage range | | 2.2 | | 5.5 | V |
| $I_Q$ | Operating quiescent current | EN = $V_{IN}$, CTRL = GND, $I_{OUT}$ = 0µA, $V_{OUT}$ = 1.8V, device not switching, | | 360 | 1800 | nA |
| | | EN = $V_{IN}$, $I_{OUT}$ = 0mA, CTRL = GND, $V_{OUT}$ = 1.8V , device switching | | 460 | | |
| | | EN = $V_{IN}$, $I_{OUT}$ = 0mA., CTRL = $V_{IN}$, $V_{OUT}$ = 1.8V, device not switching | | 12.5 | | µA |
| $I_{SD}$ | Shutdown current | EN = GND, shutdown current into $V_{IN}$ | | 70 | 1000 | nA |
| | | EN = GND, shutdown current into $V_{IN}$, $T_A$ = 60°C | | 150 | 450 | |
| $V_{TH\_UVLO+}$ | Undervoltage lockout threshold | Rising $V_{IN}$ | | 2.075 | 2.15 | V |
| $V_{TH\_UVLO-}$ | | Falling $V_{IN}$ | | 1.925 | 2 | |
| **INPUTS EN, CTRL, VSEL 1-4** | | | | | | |
| $V_{IH\ TH}$ | High level input threshold | 2.2V ≤ $V_{IN}$ ≤ 5.5V | | | 1.1 | V |
| $V_{IL\ TH}$ | Low level input threshold | 2.2V ≤ $V_{IN}$ ≤ 5.5V | 0.4 | | | V |
| $I_{IN}$ | Input bias Current | $T_A$ = 25°C | | | 10 | nA |
| | | $T_A$ = –40°C to 85°C | | | 25 | |
| **POWER SWITCHES** | | | | | | |
| $R_{DS(ON)}$ | High side MOSFET on-resistance | $V_{IN}$ = 3.6V, $I_{OUT}$ = 50mA | | 0.6 | 0.85 | Ω |
| | Low Side MOSFET on-resistance | | | 0.36 | 0.5 | |

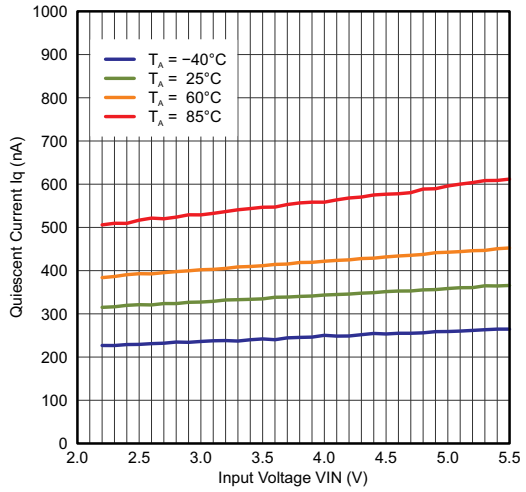
## Electrical Characteristics (continued)

$V_{IN}$ = 3.6V, $T_A$ = –40°C to 85°C typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{LIMF}$ | High side MOSFET switch current limit | 2.2V ≤ $V_{IN}$ ≤ 5.5V, TPS62740 | | 480 | 600 | 720 | mA |
| | | 3.0V ≤ $V_{IN}$ ≤ 5.5V, TPS62742 | | 590 | 650 | 740 | |
| | Low side MOSFET switch current limit | TPS62740 | | | 600 | | mA |
| | | TPS62742 | | | 650 | | |
| **OUTPUT DISCHARGE SWITCH (VOUT)** | | | | | | | |
| $R_{DSCH\_VOUT}$ | MOSFET on-resistance | $V_{IN}$ = 3.6V, EN = GND, $I_{OUT}$ = -10mA into VOUT pin | | | 30 | 65 | Ω |
| $I_{IN\_VOUT}$ | Bias current into VOUT pin | $V_{IN}$ = 3.6V, EN = $V_{IN}$, VOUT = 2V, CTRL = GND | $T_A$ = 25°C | | 40 | 100 | nA |
| | | | $T_A$ = –40°C to 85°C | | | 1010 | |
| **LOAD OUTPUT (LOAD)** | | | | | | | |
| $R_{LOAD}$ | High side MOSFET on-resistance | $I_{LOAD}$ = 50mA, CTRL = $V_{IN}$, VOUT = 2.0V, 2.2 V ≤ $V_{IN}$ ≤ 5.5V | | | 0.6 | 1.25 | Ω |
| $R_{DSCH\_LOAD}$ | Low side MOSFET on-resistance | CTRL = GND, 2.2V ≤ $V_{IN}$ ≤ 5.5V, $I_{LOAD}$ = - 10mA | | | 30 | 65 | |
| $t_{Rise\_LOAD}$ | $V_{LOAD}$ rise time | Starting with CTRL low to high transition, time to ramp $V_{LOAD}$ from 0V to 95% VOUT = 1.8V, 2.2V ≤ $V_{IN}$ ≤ 5.5V, $I_{LOAD}$ = 1mA | | | 315 | 800 | µs |
| **AUTO 100% MODE TRANSITION** | | | | | | | |
| $V_{TH\_100+}$ | Auto 100% Mode leave detection threshold (1) | Rising $V_{IN}$,100% Mode is left with $V_{IN}$ = $V_{OUT}$ + $V_{TH\_100+}$ , max value at $T_J$ = 85°C | | 170 | 250 | 340 | mV |
| $V_{TH\_100-}$ | Auto 100% Mode enter detection threshold (1) | Falling $V_{IN}$, 100% Mode is entered with $V_{IN}$ = $V_{OUT}$ + $V_{TH\_100-}$, max value at $T_J$ = 85°C | | 110 | 200 | 280 | |
| **POWER GOOD OUTPUT (PG, OPEN DRAIN)** | | | | | | | |
| $V_{TH\_PG+}$ | Power good threshold voltage | Rising output voltage on VOUT pin, referred to $V_{VOUT}$ | | | 97.5% | | |
| $V_{PG\_Hys}$ | | Hysteresis | | | -3% | | |
| $V_{OL}$ | Low level output voltage | 2.2V ≤ $V_{IN}$ ≤ 5.5V, EN = GND, current into PG pin $I_{PG}$ = 4mA | | | | 0.3 | V |
| $I_{IN\_PG}$ | Bias current into PG pin | PG pin is high impedance, VOUT = 2V, EN = $V_{IN}$, CTRL = GND, $I_{OUT}$ = 0mA | $T_A$ = 25°C | | 0 | 10 | nA |
| | | | $T_A$ = –40°C to 85°C | | | 25 | |
| **OUTPUT** | | | | | | | |
| $t_{ONmin}$ | Minimum ON time | $V_{IN}$ = 3.6V, $V_{OUT}$ = 2.0V, $I_{OUT}$ = 0 mA | | | 225 | | ns |
| $t_{OFFmin}$ | Minimum OFF time | $V_{IN}$ = 2.3V | | | 50 | | ns |
| $t_{Startup\_delay}$ | Regulator start up delay time | $V_{IN}$ = 3.6V, from transition EN = low to high until device starts switching | | | 10 | 25 | ms |
| $t_{Softstart}$ | Softstart time with reduced switch current limit | 2.2V ≤ $V_{IN}$ ≤ 5.5V, EN = $V_{IN}$ | | | 700 | 1200 | µs |
| $I_{LIM\_softstart}$ | High side MOSFET switch current limit | Reduced switch current limit during softstart | TPS62740 | 80 | 150 | 200 | mA |
| | | | TPS62742 | | 150 | | |
| | Low side MOSFET switch current limit | | | | 150 | | |
| $V_{VOUT}$ | Output voltage range | Output voltages are selected with pins VSEL 1 - 4 | | 1.8 | | 3.3 | V |
| | Output voltage accuracy | $V_{IN}$ = 3.6V, $I_{OUT}$ = 10mA, $V_{OUT}$ = 1.8V | | -2.5 | 0% | 2.5 | |
| | | $V_{IN}$ = 3.6V, $I_{OUT}$ = 100mA, $V_{OUT}$ = 1.8V | | –2 | 0% | 2 | |
| | DC output voltage load regulation | $V_{OUT}$ = 1.8V, $V_{IN}$ = 3.6V, CTRL = $V_{IN}$ | | | 0.001 | | %/mA |
| | DC output voltage line regulation | $V_{OUT}$ = 1.8V, CTRL = $V_{IN}$, $I_{OUT}$ = 10 mA, 2.5V ≤ $V_{IN}$ ≤ 5.5V | | | 0 | | %/V |

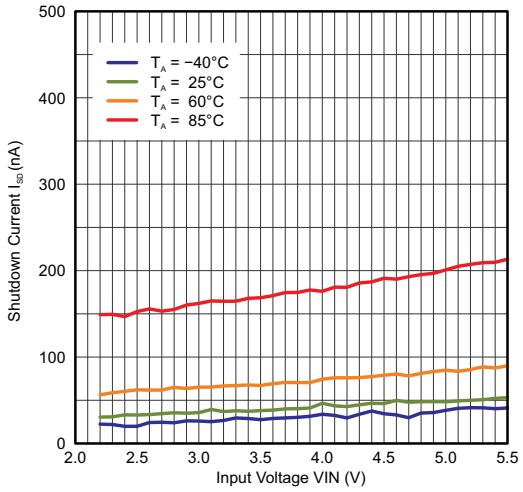
(1) $V_{IN}$ is compared to the programmed output voltage ($V_{OUT}$). When $V_{IN}$–$V_{OUT}$ falls below $V_{TH\_100-}$ the device enters 100% Mode by turning the high side MOSFET on. The 100% Mode is exited when $V_{IN}$–$V_{OUT}$ exceeds $V_{TH\_100+}$ and the device starts switching. The hysteresis for the 100% Mode detection threshold $V_{TH\_100+}$ - $V_{TH\_100-}$ will always be positive and will be approximately 50 mV(typ.)

## 8.6 Typical Characteristics




EN = VIN, $V_{OUT}$ = 1.8V, CTRL = GND  Device Not Switching

**Figure 1. Quiescent Current**




EN = GND

**Figure 2. Shutdown Current $I_{SD}$**

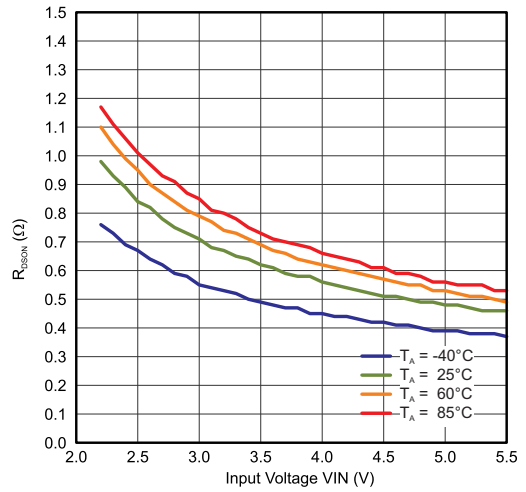



**Figure 3. $R_{DSON}$ High Side Mosfet**

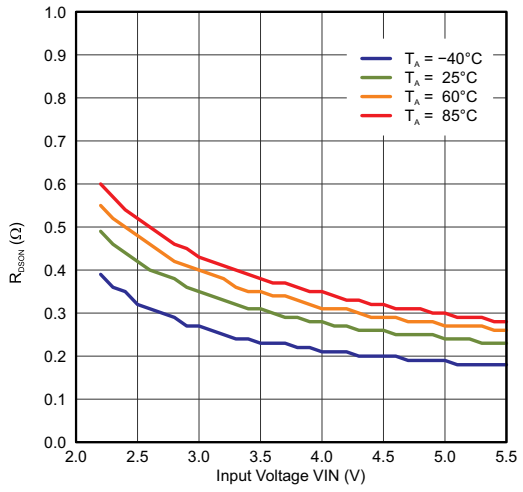



**Figure 4. $R_{DSON}$ Low Side Mosfet**

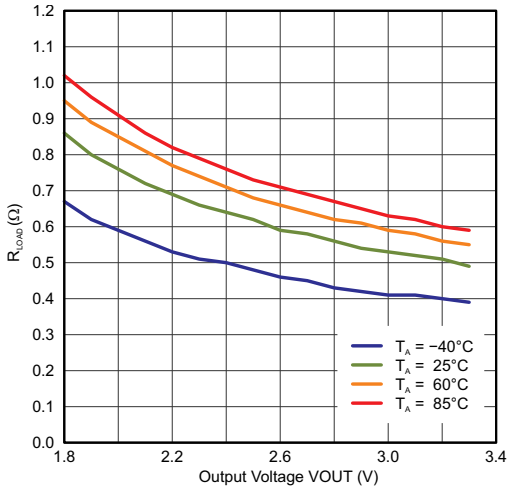


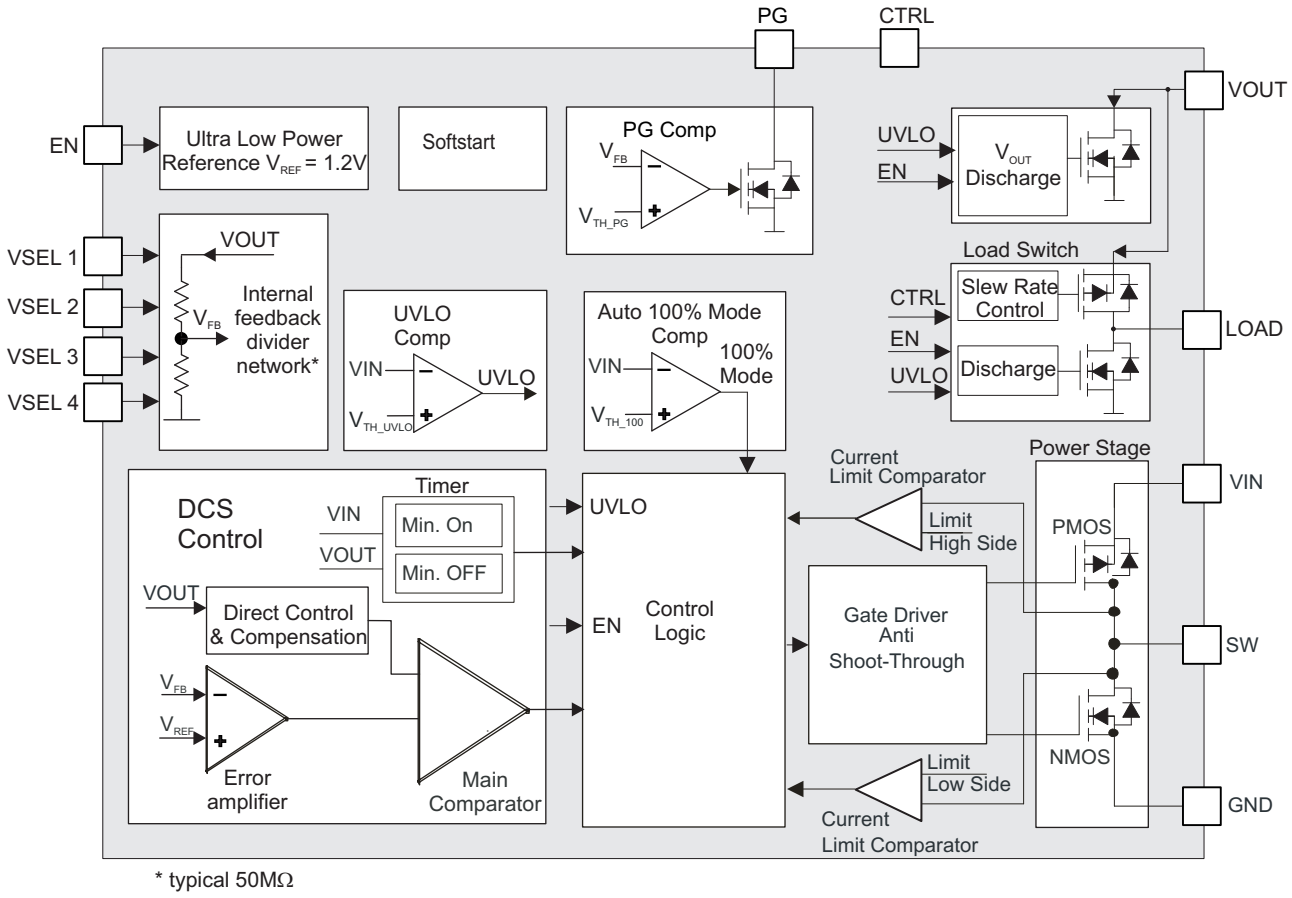

**Figure 5. Load Switch Resistance $R_{LOAD}$**

# 9 Detailed Description

## 9.1 Overview

The TPS6274x is the first step down converter with an ultra low quiescent current consumption (360nA typ.) and featuring TI's DCS-Control™ topology while maintaining a regulated output voltage. The device extends high efficiency operation to output currents down to a few micro amperes.

## 9.2 Functional Block Diagram




* typical 50MΩ

## 9.3 Feature Description

### 9.3.1 DCS-Control™

TI's DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOUT pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

## Feature Description (continued)

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and high load conditions and a Power Save Mode at light loads. During PWM mode, it operates in continuous conduction. The switching frequency is up to 2MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter seamlessly enters Power Save Mode to maintain high efficiency down to very light loads. In Power Save Mode the switching frequency varies nearly linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage. The TPS6274x offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits. At high load currents, the converter operates in quasi fixed frequency PWM mode operation and at light loads, in PFM (Pulse Frequency Modulation) mode to maintain highest efficiency over the full load current range. In PFM Mode, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve a lowest quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

During the sleep periods, the current consumption of TPS6274x is reduced to 360nA. This low quiescent current consumption is achieved by an ultra low power voltage reference, an integrated high impedance (typ. 50MΩ) feedback divider network and an optimized DCS-Control™ block.

### 9.3.2 CTRL / Output Load

With the CTRL pin set to high, the LOAD pin is connected to the VOUT pin via an load switch and can power up an additional, temporarily used sub-system. The load switch is slew rate controlled to support soft switching and not to impact the regulated output VOUT. If CTRL pin is pulled to GND, the LOAD pin is disconnected from the VOUT pin and internally connected to GND by an internal discharge switch. When CTRL pin is set to high, the Quiescent current of the DCS control block is increased to typ. 12.5µA. This ensures excellent transient response on both outputs VOUT and LOAD in case of a sudden load step at the LOAD output. The CTRL pin can be controlled by a micro controller.

### 9.3.3 Enable / Shutdown

The DC/DC converter is activated when the EN pin is set to high. For proper operation, the pin must be terminated and must not be left floating. With the EN pin set to low, the device enters shutdown mode with less than typ. 70nA current consumption.

### 9.3.4 Power Good Output (PG)

The Power Good comparator features an open drain output. The PG comparator is active with EN pin set to high and $V_{IN}$ is above the threshold $V_{TH\_UVLO+}$. It is driven to high impedance once $V_{OUT}$ trips the threshold $V_{TH\_PG+}$ for rising $V_{OUT}$. The output is pulled to low level once $V_{OUT}$ falls below the PG hysteresis, $V_{PG\_hys}$. The output is also pulled to low level in case the input voltage $V_{IN}$ falls below the undervoltage lockout threshold $V_{TH\_UVLO-}$ or the device is disabled with EN = low. The power good output (PG) can be used as an indicator for the system to signal that the converter has started up and the output voltage is in regulation.

### 9.3.5 Output Voltage Selection (VSEL1 – 4)

The TPS6274x doesn't require an external resistor divider network to program the output voltage. The device integrates a high impedance (typ. 50MΩ) feedback resistor divider network which is programmed by the pins VSEL 1-4. TPS6274x supports an output voltage range of 1.8V to 3.3V in 100mV steps. The output voltage can be changed during operation and supports a simple dynamic output voltage scaling, shown in Figure 47. The output voltage is programmed according to table Table 1.

### 9.3.6 Softstart

When the device is enabled, the internal reference is powered up and after the startup delay time $t_{Startup\_delay}$ has expired, the device enters softstart, starts switching and ramps up the output voltage. During softstart the device operates with a reduced current limit, $I_{LIM\_softstart}$, of typ. 1/4 of the nominal current limit. This reduced current limit is active during the softstart time $t_{Softstart}$. The current limit is increased to its nominal value, $I_{LIMF}$, once the softstart time has expired.

## Feature Description (continued)

### 9.3.7 Undervoltage Lockout UVLO

The device includes an under-voltage lockout (UVLO) comparator which prevents the device from misoperation at too low input voltages. The UVLO comparator becomes active once the device is enabled with EN set to high. Once the input voltage trips the UVLO threshold $V_{TH\_UVLO+}$ (typically 2.075V) for rising $V_{IN}$, the UVLO comparator releases the device for start up and operation. With a falling input voltage, the device operates down to the UVLO threshold level $V_{TH\_UVLO-}$ (typically 1.925V). Once this threshold is tripped, the device stops switching, the load switch at pin LOAD is disabled and both rails, VOUT and LOAD are discharged. The converter starts operation again once the input voltage trips the rising UVLO threshold level $V_{TH\_UVLO+}$.

## 9.4 Device Functional Modes

### 9.4.1 VOUT And LOAD Output Discharge

Both the VOUT pin and the LOAD pin feature a discharge circuit to connect each rail to GND, once they are disabled. This feature prevents residual charge voltages on capacitors connected to these pins, which may impact proper power up of the main- and sub-system. With CTRL pin pulled to low, the discharge circuit at the LOAD pin becomes active. With the EN pin pulled to low, the discharge circuits at both pins VOUT and Load are active. The discharge circuits of both rails VOUT and LOAD are associated with the UVLO comparator as well. Both discharge circuits become active once the UVLO comparator triggers and the input voltage $V_{IN}$ has dropped below the UVLO comparator threshold $V_{TH\_UVLO-}$ (typ. 1.925V).

### 9.4.2 Automatic Transition Into 100% Mode

Once the input voltage comes close to the output voltage, the DC/DC converter stops switching and enters 100% duty cycle operation. It connects the output VOUT via the inductor and the internal high side MOSFET switch to the input VIN, once the input voltage $V_{IN}$ falls below the 100% mode enter threshold, $V_{TH\_100-}$. The DC/DC regulator is turned off, not switching and therefore it generates no output ripple voltage. Because the output is connected to the input, the output voltage tracks the input voltage minus the voltage drop across the internal high side switch and the inductor caused by the output current. Once the input voltage increases and trips the 100% mode leave threshold, $V_{TH\_100+}$ , the DC/DC regulator turns on and starts switching again. See Figure 6, Figure 49, Figure 50, Figure 51.

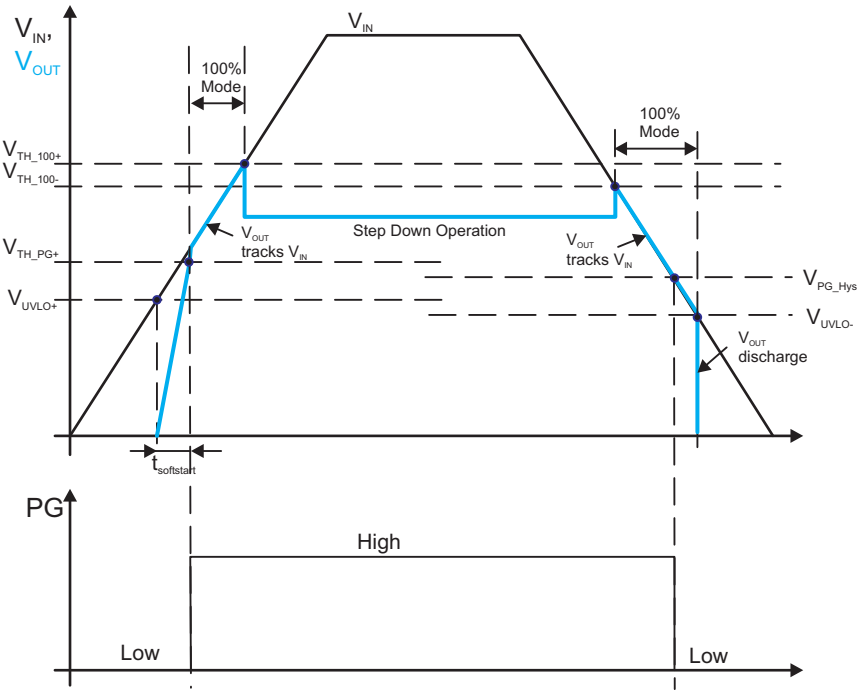



**Figure 6. Automatic 100% Mode Transition**

## Device Functional Modes (continued)

### 9.4.3 Internal Current Limit

The TPS6274x integrates a current limit on the high side, as well the low side MOSFETs to protect the device against overload or short circuit conditions. The peak current in the switches is monitored cycle by cycle. If the high side MOSFET current limit is reached, the high side MOSFET is turned off and the low side MOSFET is turned on until the current decreases below the low side MOSFET current limit.

### 9.4.4 Dynamic Voltage Scaling with VSEL Interface

During operation, the output voltage of the device can be changed, see Figure 47. The device will not actively ramp down the output voltage from a higher to a lower level.

# 10 Application and Implementation

## 10.1 Application Information

The TPS6274x devices are a step down converter family featuring typ. 360nA quiescent current and operating with a tiny 2.2µH inductor and 10µF output capacitor. This new DCS-Control™ based devices extend the light load efficiency range below 10µA load currents. TPS62740 supports output currents up to 300mA, TPS62742 up to 400mA. The devices operate from rechargeable Li-Ion batteries, Li-primary battery chemistries such as Li-SOCl2, Li-MnO2 and two or three cell alkaline batteries.

## 10.2 Typical Application

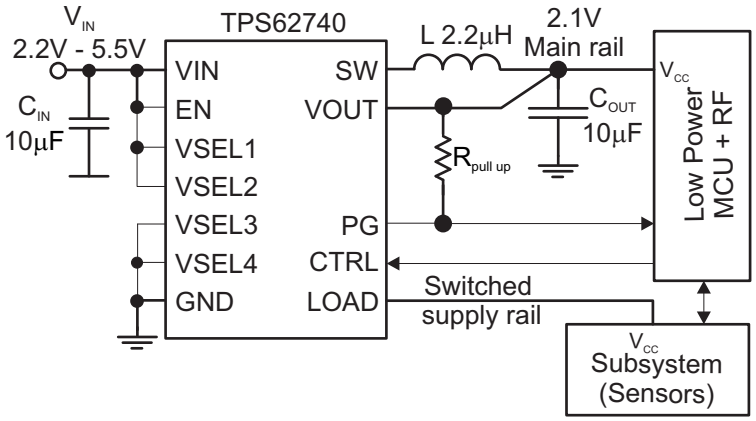



**Figure 7. TPS62740 Typical Application Circuit**

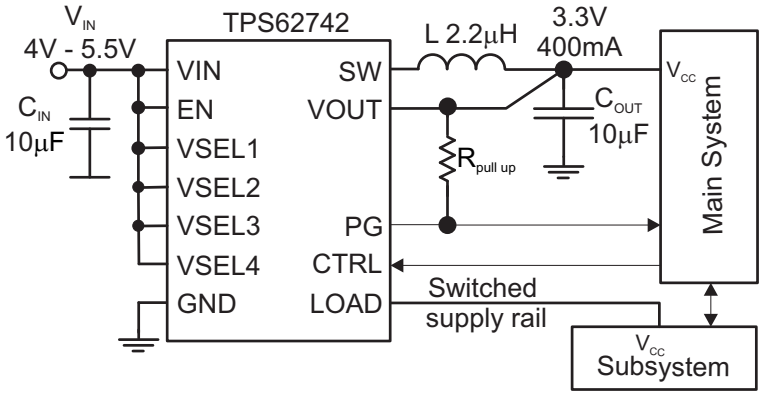



**Figure 8. TPS62742 Typical Application Circuit**

### 10.2.1 Design Requirements

The TPS6274x is a highly integrated DC/DC converter. The output voltage is set via a VSEL pin interface without any additional external components. For proper operation only a input- and output capacitor and an inductor is required. The integrated load switch doesn't require a capacitor on its LOAD pin. Table 2 shows the components used for the application characteristic curves.

**Table 2. Components for Application Characteristic Curves**

| Reference | Description | Value | Manufacturer |
|---|---|---|---|
| TPS62740/42 | 360nA Iq step down converter | | Texas Instruments |
| CIN, COUT, CLOAD | Ceramic capacitor GRM188R60J106M | 10µF | Murata |
| L | Inductor LPS3314 | 2.2µH | Coilcraft |

### 10.2.2 Detailed Design Procedure

Table 3 shows the recommended output filter components. The TPS6274x is optimized for operation with a 2.2µH inductor and with 10µF output capacitor.

**Table 3. Recommended LC Output Filter Combinations**

| Inductor Value [µH](1) | Output Capacitor Value [µF](2) | | |
|---|---|---|---|
| | 4.7µF | 10µF | 22µF |
| 2.2 | √ | √(3) | √ |

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

#### *10.2.2.1 Inductor Selection*

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current ($\Delta I_L$) decreases with higher inductance and increases with higher $V_{IN}$ or $V_{OUT}$ and can be estimated according to Equation 1.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with Equation 2. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current above the high-side MOSFET switch current limit, $I_{LIMF}$.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

With:

f = Switching Frequency
L = Inductor Value
$\Delta I_L$= Peak to Peak inductor ripple current
$I_{Lmax}$ = Maximum Inductor current

In DC/DC converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and by the inductor DCR value. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance ($R_{DC}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used:

**Table 4. List Of Inductors(1)**

| INDUCTANCE [µH] | DIMENSIONS [mm³] | INDUCTOR TYPE | SUPPLIER |
|---|---|---|---|
| 2.2 | 3.3 x 3.3 x 1.4 | LPS3314 | Coilcraft |
| 2.2 | 2.5 x 3.0 x 1.5 | VLF302515MT | TDK |
| 2.2 | 2.0 × 1.2 × 1.0 | MIPSZ2012 2R2 | FDK |
| 2.2 | 2.5 x 2.0 x 1.2 | MIPSA2520 2R2 | FDK |
| 2.2 | 2.0 x 1.2 x 1.0 | MDT2012CH2R2 | TOKO |

(1) See Third-party Products Disclaimer

#### *10.2.2.2 DC/DC Output Capacitor Selection*

The DCS-Control™ scheme of the TPS6274x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. A larger output capacitors can be used, but it should be considered that larger output capacitors lead to an increased leakage current in the capacitor and may reduce overall conversion efficiency. Furthermore, larger output capacitors impact the start up behavior of the DC/DC converter.

#### *10.2.2.3 Input Capacitor Selection*

Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to ensure proper function of the device and to minimize input voltage spikes. For most applications a 10µF is sufficient. The input capacitor can be increased without any limit for better input voltage filtering.

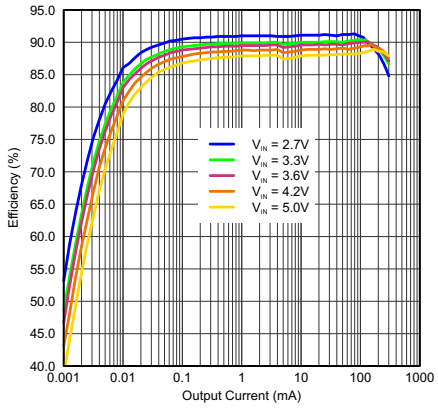
Table 5 shows a list of tested input/output capacitors.

**Table 5. List Of Capacitors(1)**

| CAPACITANCE [µF] | SIZE | CAPACITOR TYPE | SUPPLIER |
|---|---|---|---|
| 10 | 0603 | GRM188R60J106ME84 | Murata |

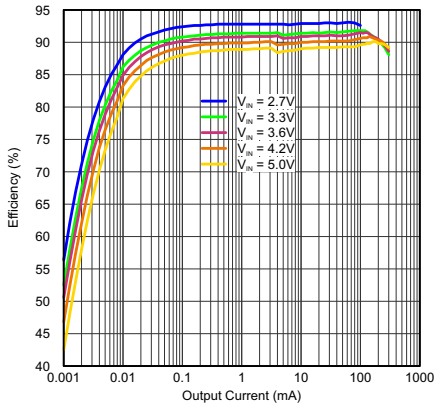
(1) See Third-party Products Disclaimer

### 10.2.3 Application Curves



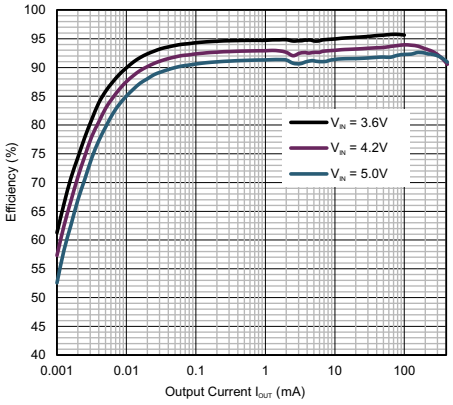

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 9. Efficiency $V_{OUT}$ = 1.8V**



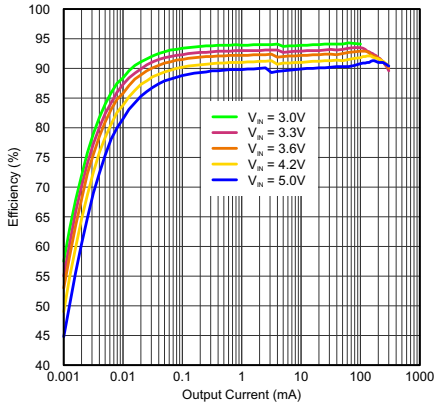

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 10. Efficiency $V_{OUT}$ = 2.1V**



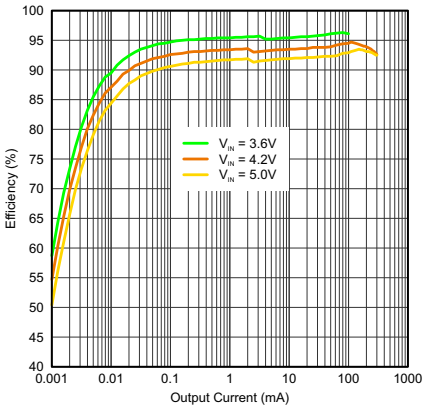

$C_{OUT}$ = 10 µF, CTRL = GND.
L = 2.2 µH (VLF302515)

**Figure 11. Efficiency VOUT = 3.3V TPS62742**



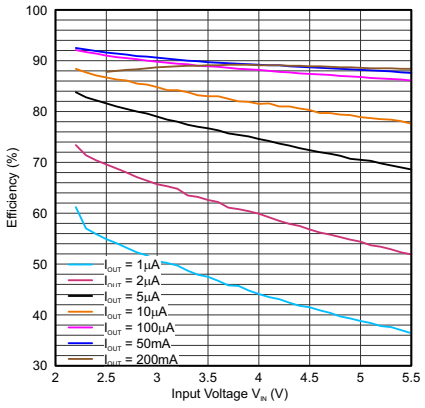

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 12. Efficiency $V_{OUT}$ = 2.5V**



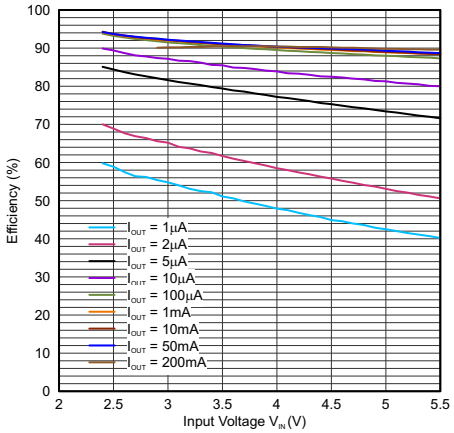

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 13. Efficiency $V_{OUT}$ = 3.3V**



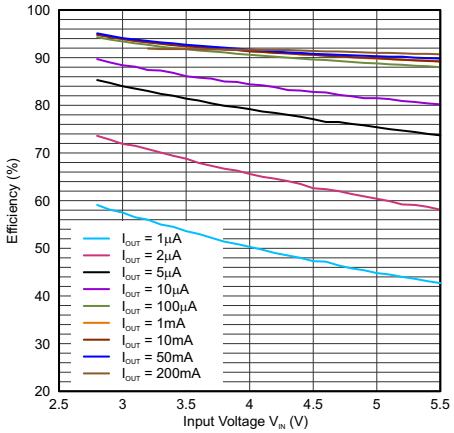

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 14. Efficiency $V_{OUT}$ = 1.8V**



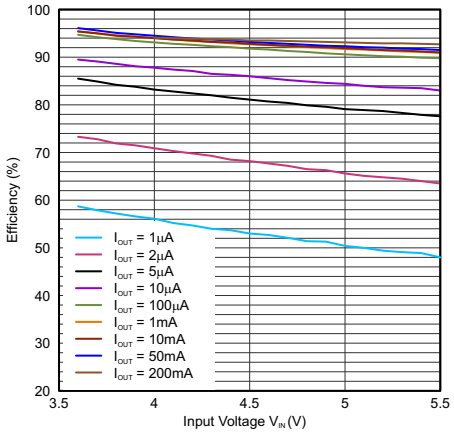

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 15. Efficiency $V_{OUT}$ = 2.1V**



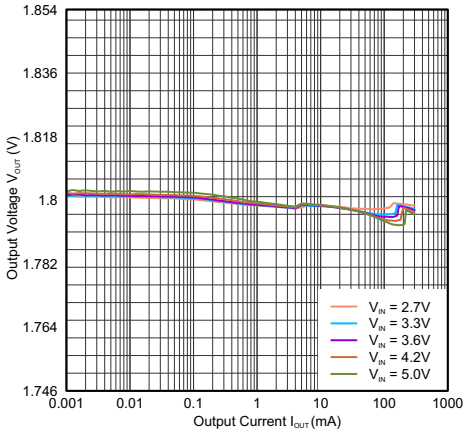

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 16. Efficiency $V_{OUT}$ = 2.5V**



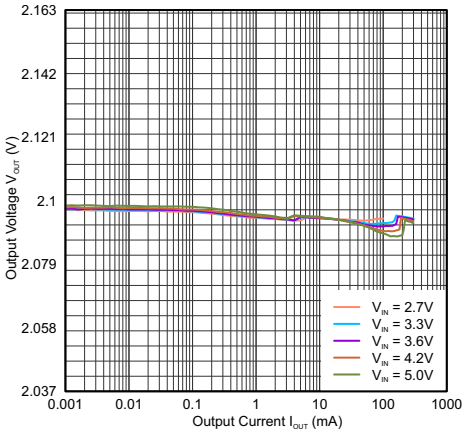

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 17. Efficiency $V_{OUT}$ = 3.3V**



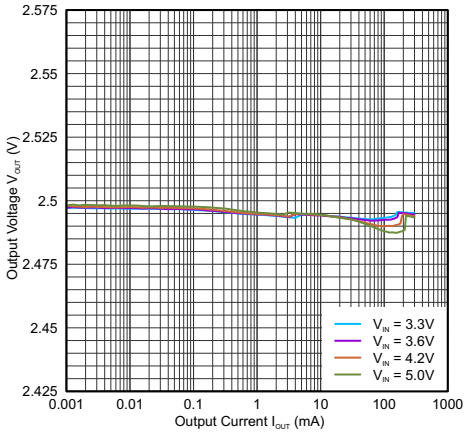

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 18. Output Voltage $V_{OUT}$ = 1.8V**



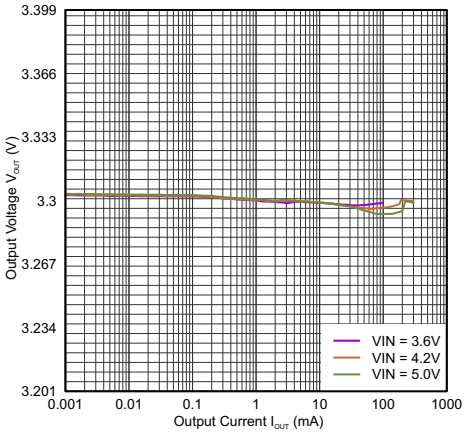

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

**Figure 19. Output Voltage $V_{OUT}$ = 2.1V**




$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH (LPS3314 2R2)

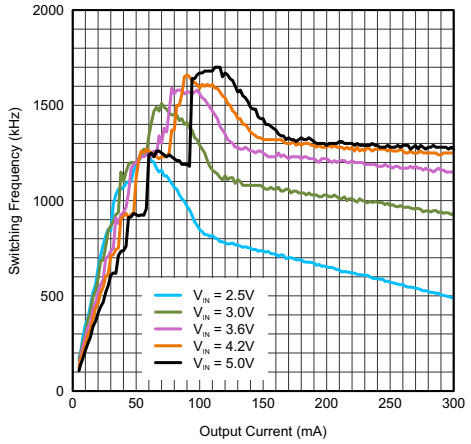
**Figure 20. Output Voltage $V_{OUT}$ = 2.5V**




$C_{OUT}$ = 10 µF (0603) CTRL = GND

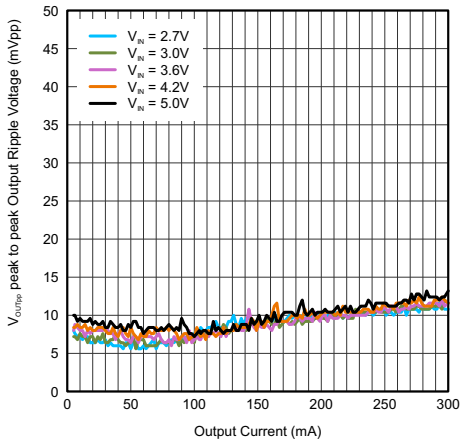
L = 2.2 µH (LPS3314 2R2)

**Figure 21. Output Voltage $V_{OUT}$ = 3.3V**




$C_{OUT}$ = 10 µF L = 2.2 µH

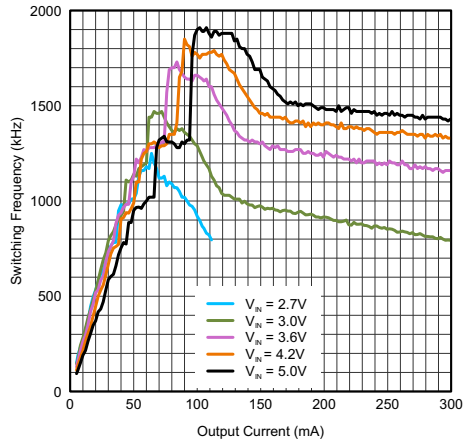
**Figure 22. Typical Switching Frequency $V_{OUT}$ = 1.8V**




$C_{OUT}$ = 10 µF (0603) CTRL = GND

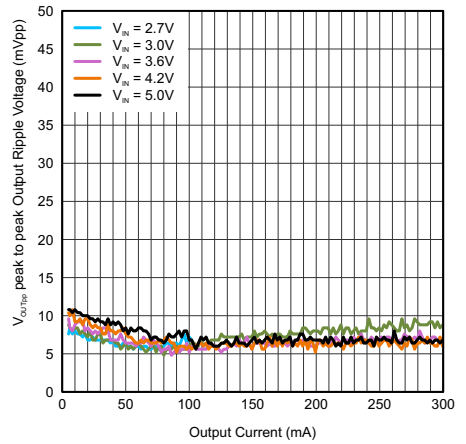
L = 2.2 µH

**Figure 23. Typical Output Ripple Voltage $V_{OUT}$ = 1.8V**




$C_{OUT}$ = 10 µF L = 2.2 µH

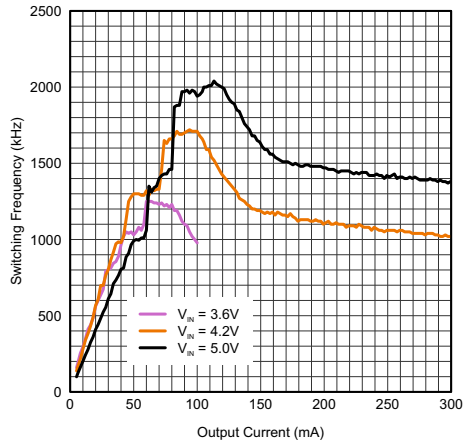
**Figure 24. Typical Switching Frequency $V_{OUT}$ = 2.1V**




$C_{OUT}$ = 10 µF (0603) CTRL = GND

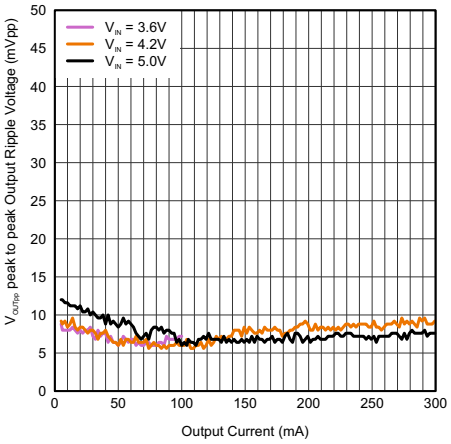
L = 2.2 µH

**Figure 25. Typical Output Ripple Voltage $V_{OUT}$ = 2.1V**



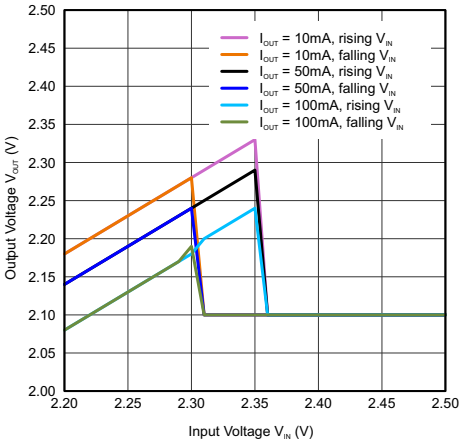

$C_{OUT}$ = 10 µF L = 2.2 µH

**Figure 26. Typical Switching Frequency $V_{OUT}$ = 3.0V**



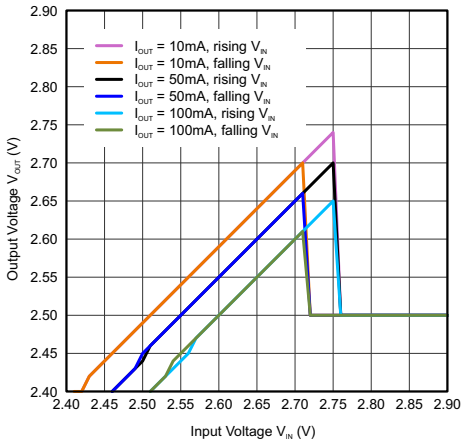

$C_{OUT}$ = 10 µF (0603) CTRL = GND
L = 2.2 µH

**Figure 27. Typical Output Ripple Voltage $V_{OUT}$ = 3.0V**



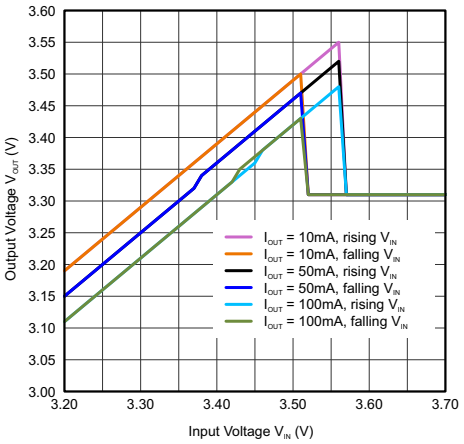

L = 2.2 µH (LPS3314)

**Figure 28. 100% Mode Transition $V_{OUT}$ 2.1V**



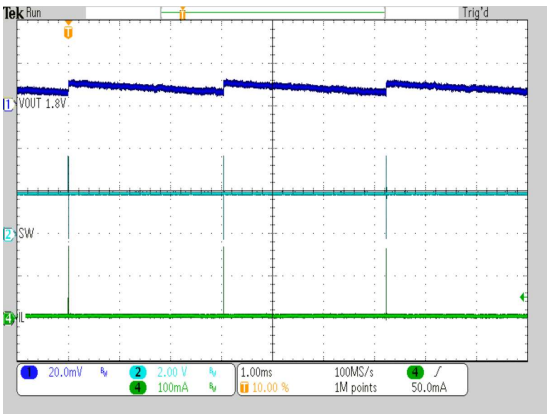

L = 2.2 µH (LPS3314)

**Figure 29. 100% Mode Transition $V_{OUT}$ 2.5V**



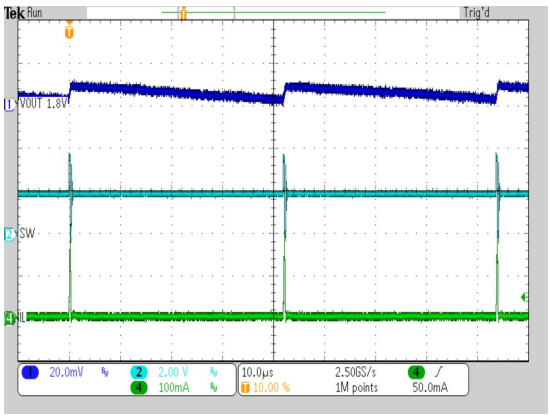

L = 2.2 µH (LPS3314)

**Figure 30. 100% Mode Transition $V_{OUT}$ 3.3V**



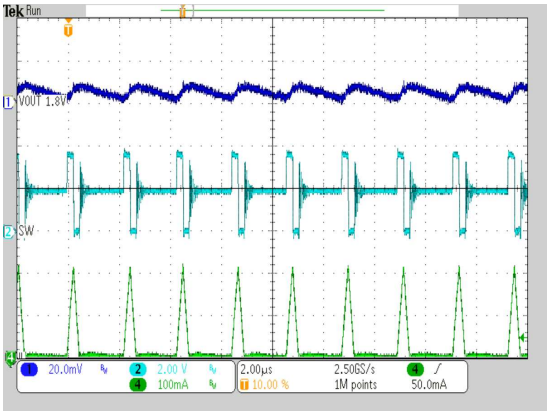

$V_{IN}$ = 3.6 V $I_{OUT}$ = 10 µA L = 2.2 µH
$C_{OUT}$ = 10 µF CTRL = GND

**Figure 31. Typical Operation $I_{Load}$ = 10µA $V_{OUT}$ = 1.8V**



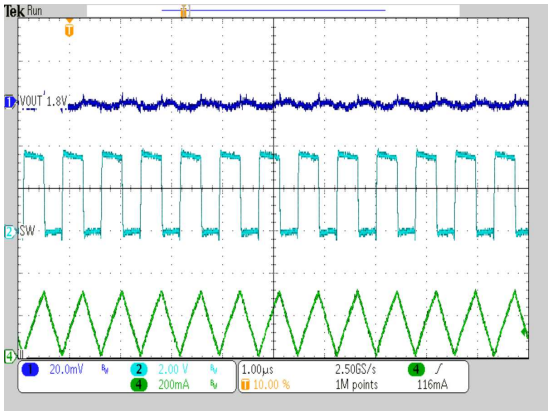

$V_{IN}$ = 3.6 V $I_{OUT}$ = 1 mA L = 2.2 µH
$C_{OUT}$ = 10 µF CTRL = GND

**Figure 32. Typical Operation $I_{Load}$ = 1ma, $V_{OUT}$ = 1.8V**



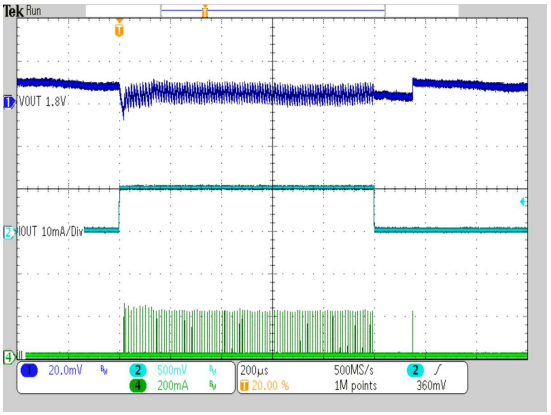

$V_{IN}$ = 3.6 V $I_{OUT}$ = 25 mA L = 2.2 µH
$C_{OUT}$ = 10 µF CTRL = GND

**Figure 33. Typical Operation $I_{Load}$ = 25mA, $V_{OUT}$ = 1.8V**



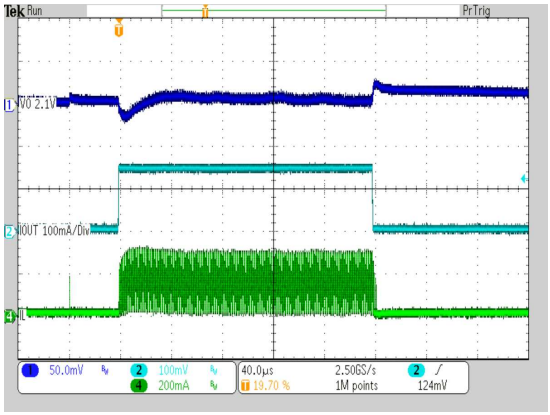

$V_{IN}$ = 3.6 V $I_{OUT}$ = 150 mA L = 2.2 µH
$C_{OUT}$ = 10 µF CTRL = GND

**Figure 34. Typical Operation $I_{Load}$ = 150ma, $V_{OUT}$ = 1.8V**



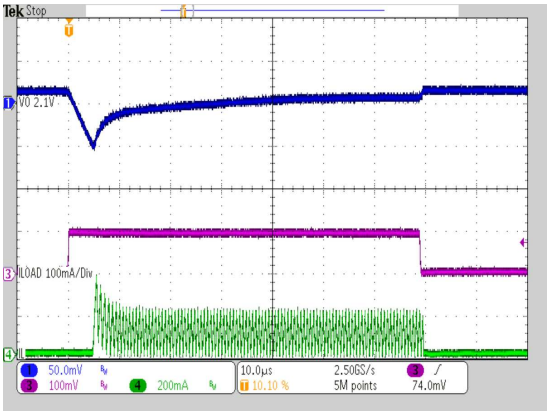

$V_{IN}$ = 3.6 V $I_{OUT}$ = 50 µA to 10 mA L = 2.2 µH
$C_{OUT}$ = 10 µF CTRL = GND

**Figure 35. Load Transient Response $V_{OUT}$ = 1.8V**



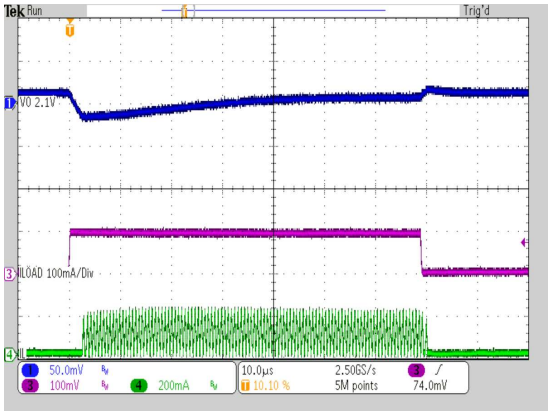

$V_{IN}$ = 3.6 V $I_{OUT}$ = 0.5 mA to 150 mA L = 2.2 µH
$C_{OUT}$ = 10 µF CTRL = $V_{IN}$

**Figure 36. Load Transient Response $V_{OUT}$ = 2.1V**



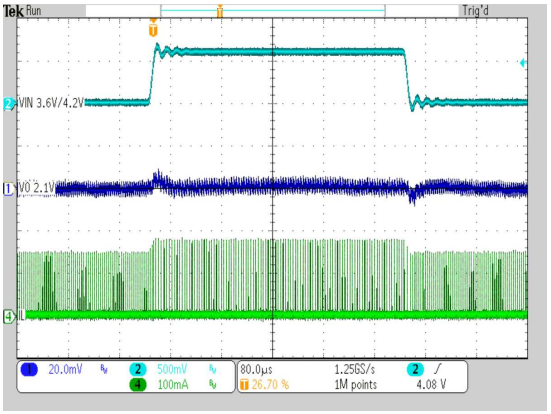

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 2.1 V L = 2.2 µH $C_{OUT}$ = 10 µF
Loadstep at $V_{OUT}$ 0 mA to 100 mA,
1 µs rise/ fall time, 70 µs / 7 ms

**Figure 37. Load Transient Response CTRL = GND**



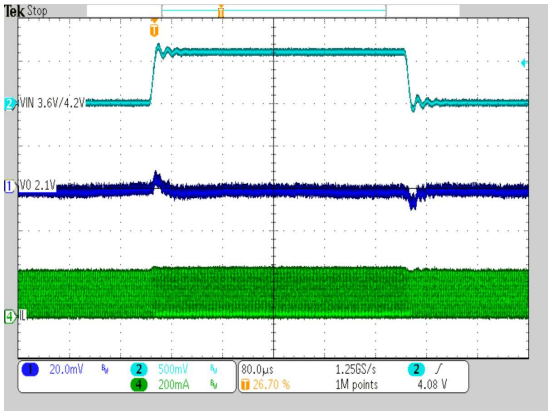

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 2.1 V L = 2.2 µH, $C_{OUT}$ = 10 µF
Loadstep at $V_{OUT}$ 0 mA to 100 mA,
1 µs rise/fall time; 70 µs / 7 ms

**Figure 38. Load Transient Response CTRL = VIN**



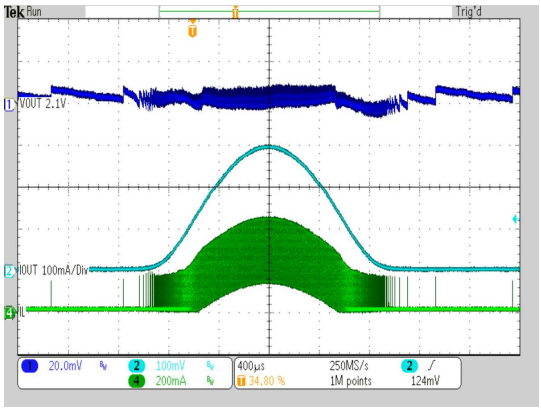

$V_{IN}$ = 3.6 V / 4.2 V $V_{OUT}$ = 2.1 V $C_{OUT}$ = 10 µF L = 2.2 µH CTRL = GND

**Figure 39. Line Transient Response $I_{OUT}$=10mA**



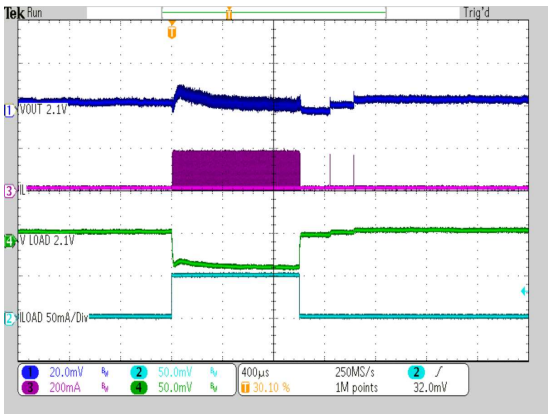

$V_{IN}$ = 3.6 V / 4.2 V $V_{OUT}$ = 2.1 V $C_{OUT}$ = 10 µF L = 2.2 µH CTRL = GND

**Figure 40. Line Transient Response $I_{OUT}$ = 100mA**



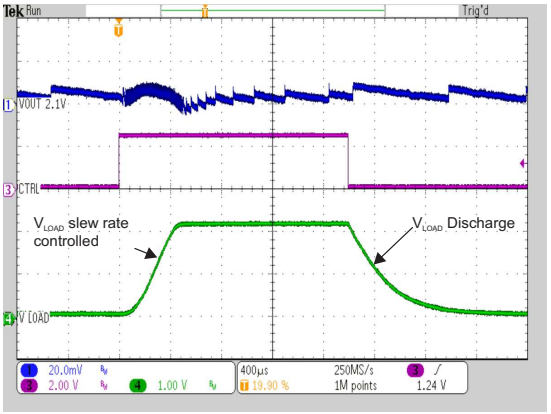

$V_{IN}$ = 3.6 V $I_{OUT}$ = 50 µA to 300 mA $C_{OUT}$ = 10 µF L = 2.2 µH CTRL = GND

**Figure 41. AC Load Sweep $V_{OUT}$ = 2.1V**



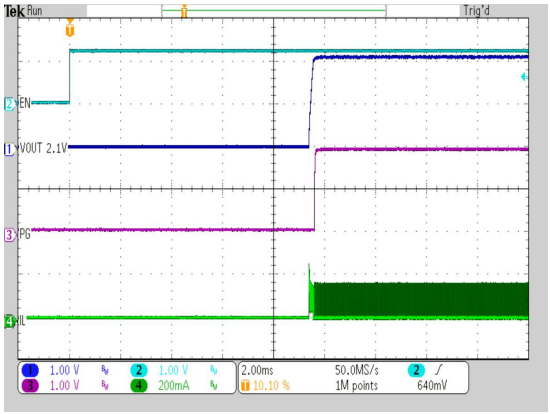

$V_{IN}$ = 3.6 V, $I_{OUT}$ = 0 mA $C_{OUT}$ = 10 µF $V_{OUT}$ = $V_{LOAD}$= 2.1 V $C_{LOAD}$ = 10 µF CTRL = $V_{IN}$ L = 2.2 µH $I_{LOAD}$ = 0 to 50 mA to 0 mA

**Figure 42. Load Step At Load Output**



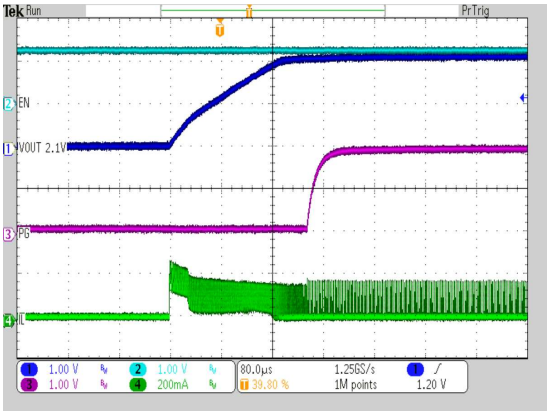

$V_{IN}$ = 3.6 V $I_{OUT}$ = 0 mA $V_{OUT}$ = 2.1 V $C_{OUT}$ = 10 µF $I_{LOAD}$ = 0 mA $C_{LOAD}$ = 10 µF L = 2.2 µH

**Figure 43. Load Output On / Off**



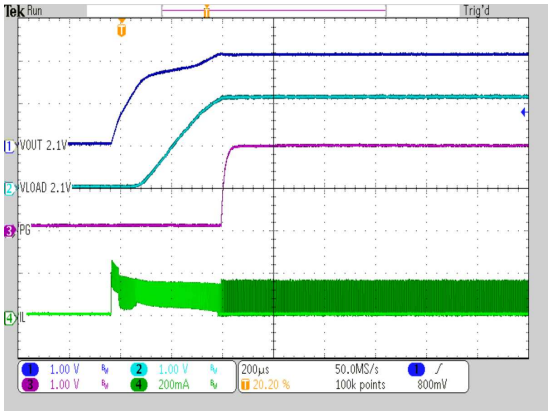

$V_{IN}$ = 3.6 V $R_{OUT}$ = 100 Ω $V_{OUT}$ = 2.1 V $C_{OUT}$ = 10 µF CTRL = GND L = 2.2 µH

**Figure 44. Device Enable And Start Up**



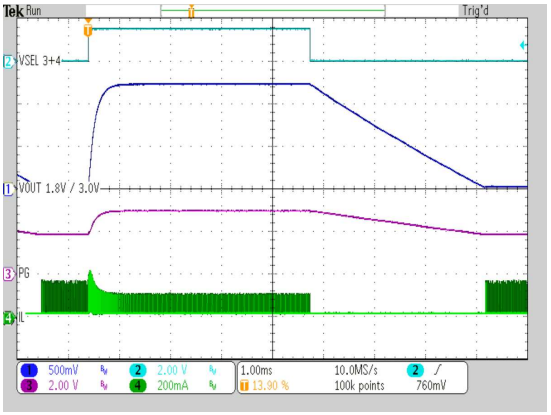

$V_{IN}$ = 3.6 V $V_{OUT}$ = 2.1 V CTRL = GND
$R_{OUT}$ = 100 Ω $C_{OUT}$ = 10 µF L = 2.2 µH

**Figure 45. $V_{OUT}$ Ramp Up After Enable**



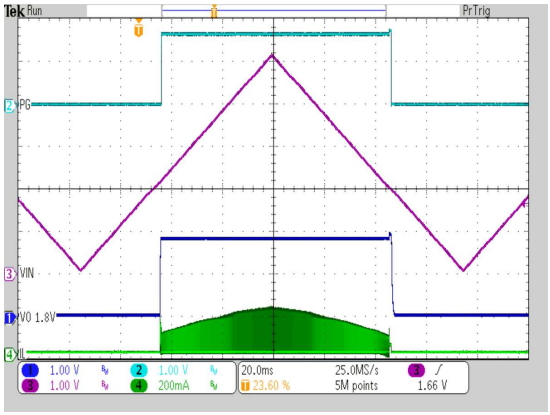

$V_{IN}$ = 3.6 V $V_{OUT}$ = $V_{LOAD}$ = 2.1 V CTRL = $V_{IN}$
$R_{OUT}$ = 100 Ω, $C_{OUT}$ = $C_{LOAD}$ = 10 µF L = 2.2 µH
$I_{LOAD}$ = 0 mA

**Figure 46. $V_{OUT}$ Ramp Up With Activated Load Switch**



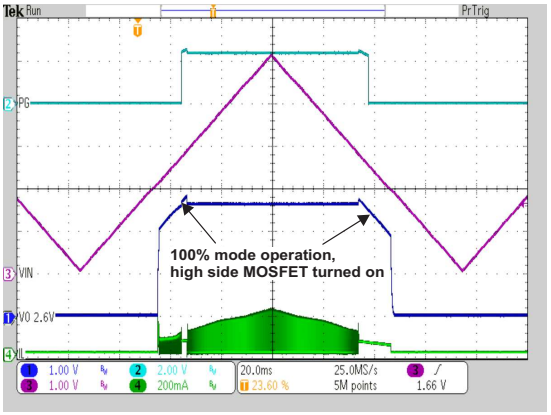

$V_{IN}$ = 3.6 V Ramp up / Down
$C_{OUT}$ = 10 µF CTRL = GND VSEL 3+4 toggled
$I_{OUT}$ = 5 mA L = 2.2 µH VSEL 1+2 = GND

**Figure 47. Dynamic Output Voltage Scaling $V_{OUT}$ = 1.8V/3.0V**



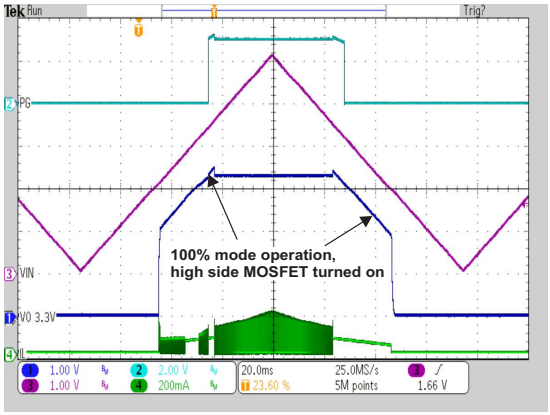

$C_{OUT}$ = 10 µF L = 2.2 µH CTRL = GND
$V_{IN}$ = ramp up/down 0 V to 5 V, 150 ms,
Output resistance 50 Ω

**Figure 48. Input Voltage Ramp Up/Down $V_{OUT}$ = 1.8V**



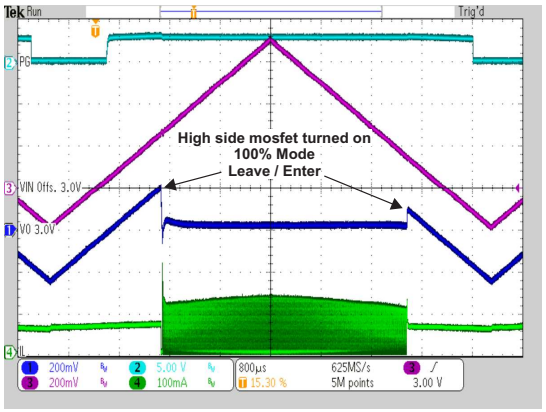

$C_{OUT}$ = 10 µF L = 2.2 µH CTRL = GND
$V_{IN}$ = ramp up/down 0 V to 5 V, 150 ms,
Output resistance 50 Ω

**Figure 49. Input Voltage Ramp Up/Down $V_{OUT}$ = 2.6V**




$C_{OUT}$ = 10 µF L = 2.2 µH CTRL = GND
$V_{IN}$ = ramp up/down 0 V to 5 V, 150 ms,
Output resistance 50 Ω

**Figure 50. Input Voltage Ramp Up/Down $V_{OUT}$ = 3.3V**




$V_{OUT}$ = 3.0 V $C_{OUT}$ = 10 µF L = 2.2 µH, CTRL = GND
$V_{IN}$ = ramp up /down 2.8 V to 3.7 V,
Output resistance 50 Ω

**Figure 51. Enter/Leave 100% Mode Operation**

## 10.3 System Example

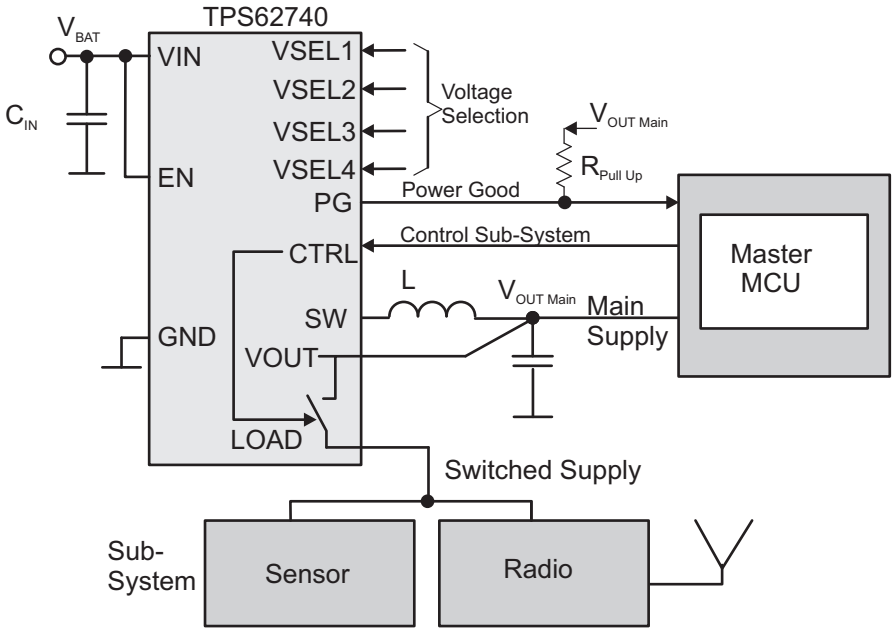



**Figure 52. Example Of Implementation In A Master MCU Based System**

# 11 Power Supply Recommendations

The power supply to the TPS6274x needs to have a current rating according to the supply voltage, output voltage and output current of the TPS6274x.

# 12 Layout

## 12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems and interference with RF circuits. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins VIN and GND. The output capacitor should be placed close between VOUT and GND pins. The VOUT line should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line) or other noise sources. The exposed thermal pad of the package and the GND pin should be connected. See Figure 53 for the recommended PCB layout.

## 12.2 Layout Example

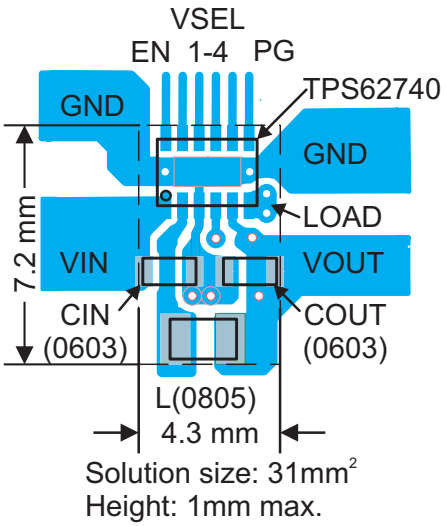



**Figure 53. Recommended PCB Layout**

# 13 Device and Documentation Support

## 13.1 Device Support

### 13.1.1 Third-Party Products Disclaimer

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## 13.2 Documentation Support

### 13.2.1 Related Documentation

See also *TPS62740EVM-186 Evaluation Module User's Guide*, SLVU949; and application note *Accurately measuring efficiency of ultralow-IQ devices,* SLYT558 for accurate efficiency measurements in PFM mode operation.

## 13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 6. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS62740 | Click here | Click here | Click here | Click here | Click here |
| TPS62742 | Click here | Click here | Click here | Click here | Click here |

## 13.4 Trademarks

DCS-Control is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.

## 13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS62740DSSR | Active | Production | WSON (DSS) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62740 |
| TPS62740DSSR.B | Active | Production | WSON (DSS) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62740 |
| TPS62740DSSRG4 | Active | Production | WSON (DSS) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62740 |
| TPS62740DSSRG4.B | Active | Production | WSON (DSS) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62740 |
| TPS62740DSST | Active | Production | WSON (DSS) \| 12 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62740 |
| TPS62740DSST.B | Active | Production | WSON (DSS) \| 12 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62740 |
| TPS62742DSSR | Active | Production | WSON (DSS) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62742 |
| TPS62742DSSR.B | Active | Production | WSON (DSS) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62742 |
| TPS62742DSSRG4 | Active | Production | WSON (DSS) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62742 |
| TPS62742DSSRG4.B | Active | Production | WSON (DSS) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62742 |
| TPS62742DSST | Active | Production | WSON (DSS) \| 12 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62742 |
| TPS62742DSST.B | Active | Production | WSON (DSS) \| 12 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 62742 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

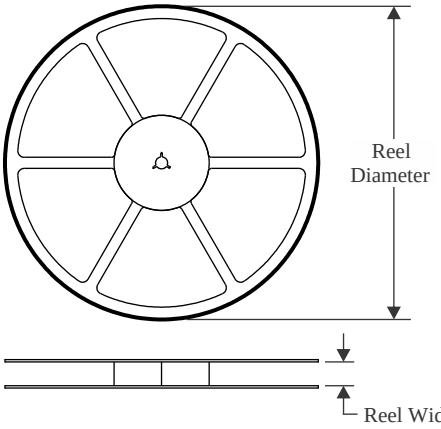
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

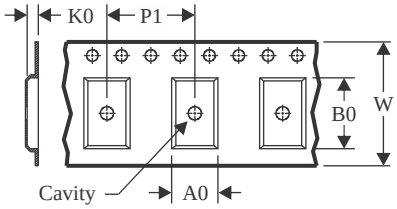
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

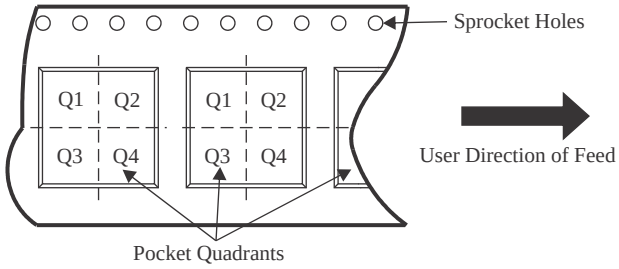



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

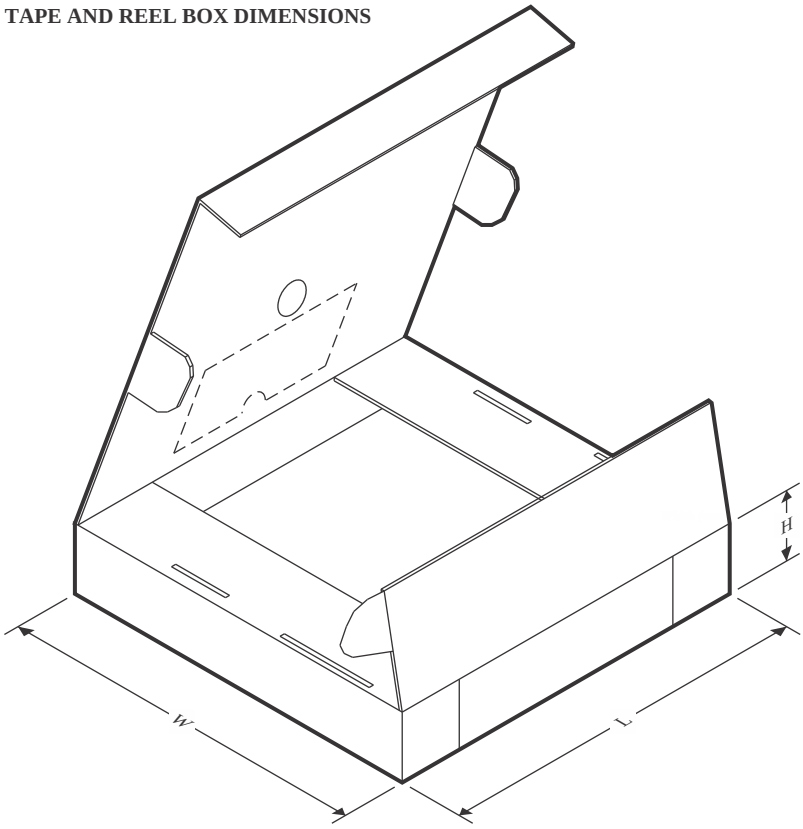
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62740DSSR | WSON | DSS | 12 | 3000 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |
| TPS62740DSSRG4 | WSON | DSS | 12 | 3000 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |
| TPS62740DSST | WSON | DSS | 12 | 250 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |
| TPS62742DSSR | WSON | DSS | 12 | 3000 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |
| TPS62742DSSRG4 | WSON | DSS | 12 | 3000 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |
| TPS62742DSST | WSON | DSS | 12 | 250 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



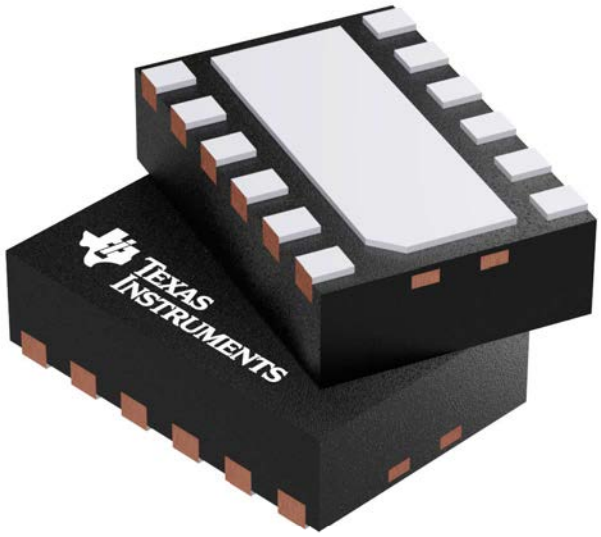

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS62740DSSR | WSON | DSS | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62740DSSRG4 | WSON | DSS | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62740DSST | WSON | DSS | 12 | 250 | 182.0 | 182.0 | 20.0 |
| TPS62742DSSR | WSON | DSS | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62742DSSRG4 | WSON | DSS | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62742DSST | WSON | DSS | 12 | 250 | 182.0 | 182.0 | 20.0 |

# GENERIC PACKAGE VIEW

## DSS 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



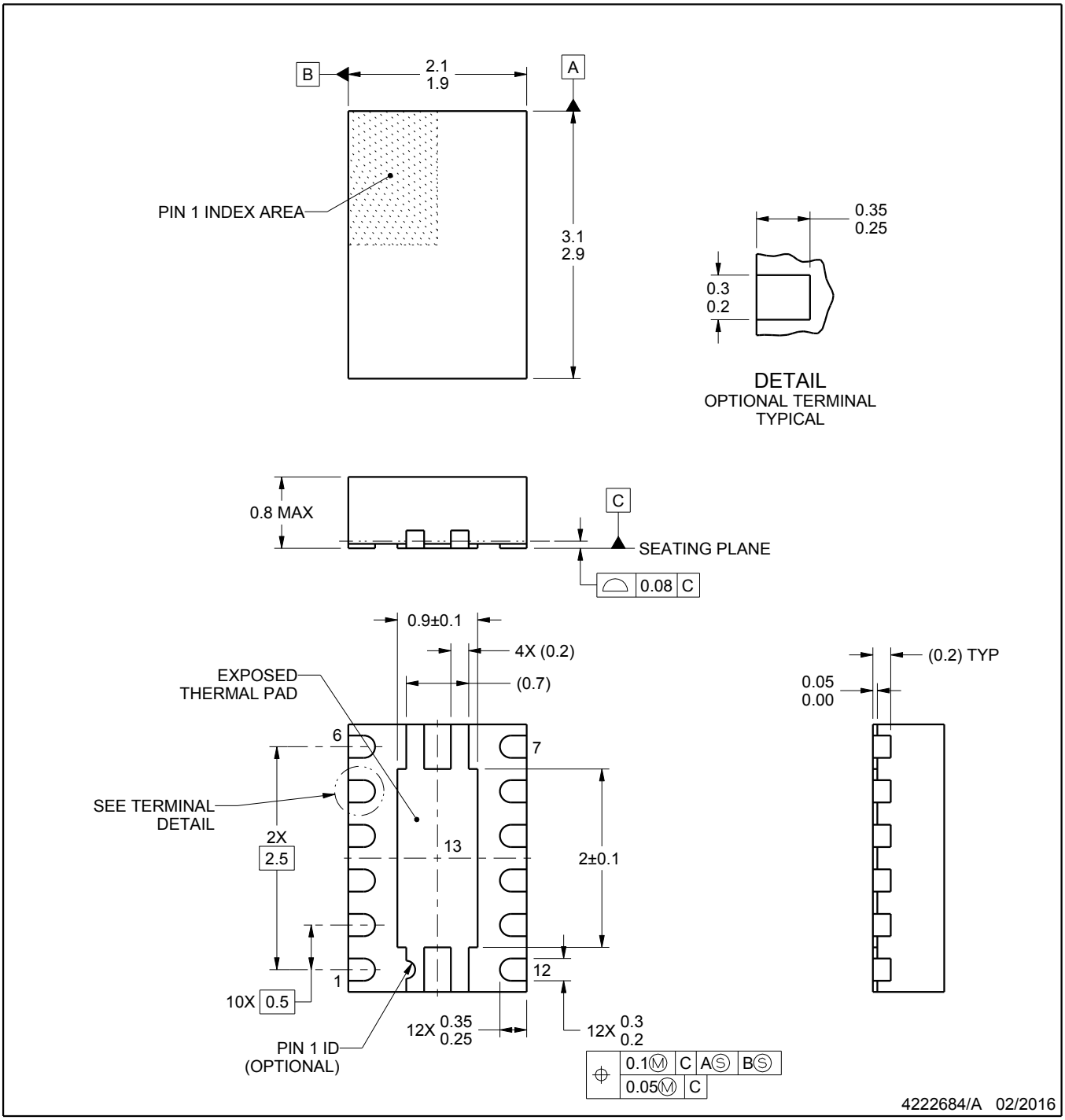

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## DSS0012A

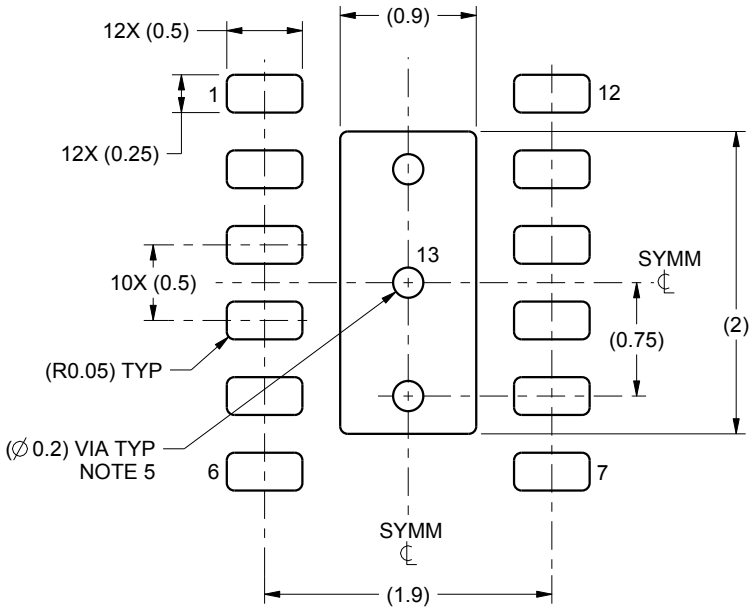
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

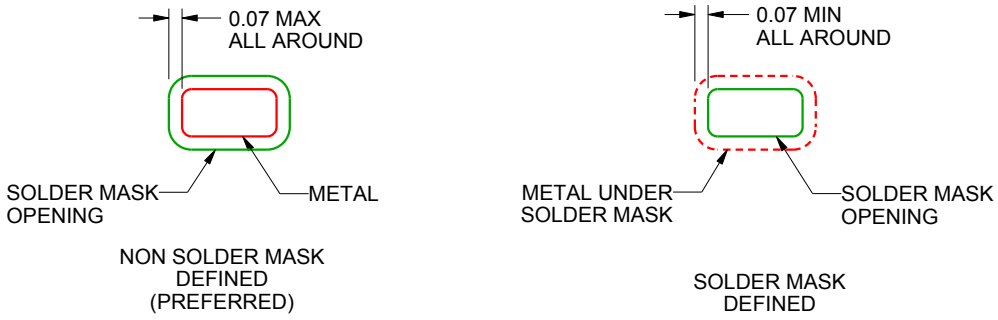



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X




SOLDER MASK DETAILS

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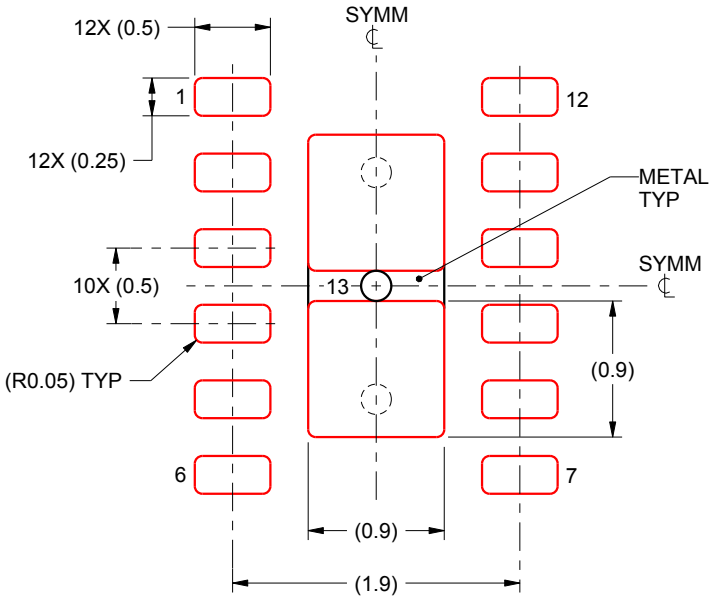
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown. It is recommended that vias located under solder paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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