TEXAS INSTRUMENTS
TPS62441, TPS62442
JAJSNC4A – NOVEMBER 2021 – REVISED MAY 2023

TPS6244x 可変周波数、1% 精度、QFN パッケージ、2.75V～6V、デュアル・チャネル降圧コンバータ

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 出力電圧:0.6V～5.5V デュアル・チャネル
- 出力電流:1A/1A、2A/2A、3A/1A
- 2.75V～6V の入力電圧範囲
- 帰還電圧精度:1% (PWM 動作)
- T_J = -40℃～+150℃
- 2 つの高精度イネーブル入力により以下を実現:
  - ユーザー定義の低電圧誤動作防止機能
  - 正確なシーケンシング
- ウィンドウ・コンパレータによる 2 つのパワー・グッド出力
- 可変スイッチング周波数:1.8MHz～4MHz
- 外部クロックへの周波数同期も可能
- スペクトラム拡散クロック供給も可能
- 強制 PWM または PWM/PFM 動作
- 最大 200µF の補償ネットワークを選択可能
- 静止電流:22µA
- 180° 位相シフト動作
- 100% デューティ・サイクル・モード
- アクティブ出力放電
- サーマル・シャットダウン保護機能
- 2.3mm × 2.7mm QFN パッケージ

2 アプリケーション

- モーター・ドライブ/ドローン・コントローラ
- ロボット HMI
- 試験および測定機器
- マシン・ビジョン
- ストリング・インバータ

3 概要

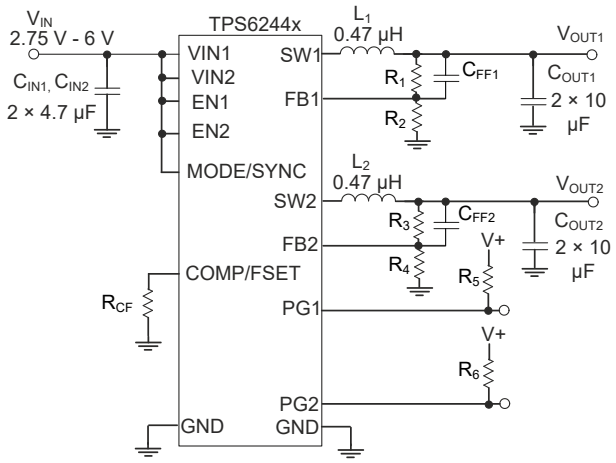
TPS6244x はピン互換のデュアル 1A、デュアル 2A および 3A/1A、高効率で使いやすい同期整流降圧 DC/DC コンバータのファミリです。このデバイスは、ピーク電流モード制御方式に基づいています。これらのデバイスは、モーター・ドライブやロボットなどの産業用アプリケーション向けに設計されています。抵抗の低いスイッチにより、高い周囲温度でも、最大 3A の連続出力電流、最大 4A の合計出力電流を供給できます。スイッチング周波数は 1.8MHz～4MHz の範囲で外部から変更でき、同じ周波数範囲の外部クロックと同期することもできます。PWM/PFM モードでは、TPS6244x は負荷が軽いときに自動的にパワーセーブ・モードへ移行するため、負荷範囲全体にわたって高い効率が維持されます。TPS6244x は PWM モードで 1% の出力電圧精度を実現しているので、出力電圧精度の高い電源の設計に役立ちます。

TPS6244x は可変電圧バージョンとして供給され、VQFN パッケージに搭載されています。

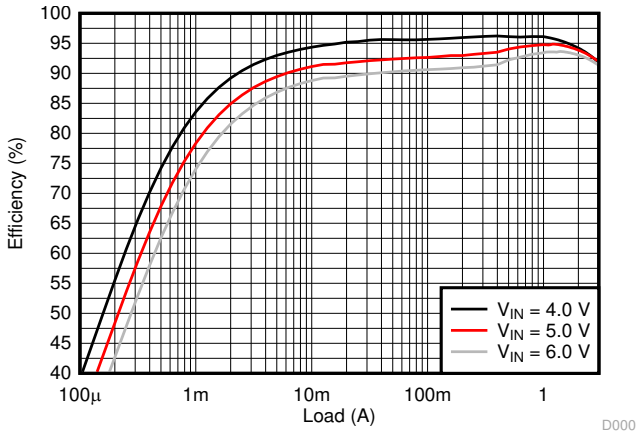
パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS62441	RQR (VQFN、14)	2.30mm × 2.70mm
TPS62442		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



回路図



効率と出力電流との関係、V_{OUT} = 3.3V、PWM/PFM、f_{sw} = 2.25MHz

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2021) to Revision A (May 2023)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

5 Device Comparison Table

DEVICE NUMBER	FEATURES	OUTPUT VOLTAGE
TPS62441RQRR	2 × 1-A output current V_{OUT} discharge	adjustable
TPS62442RQRR	2 × 2-A or 3-A and 1-A output current V_{OUT} discharge	adjustable

6 Pin Configuration and Functions

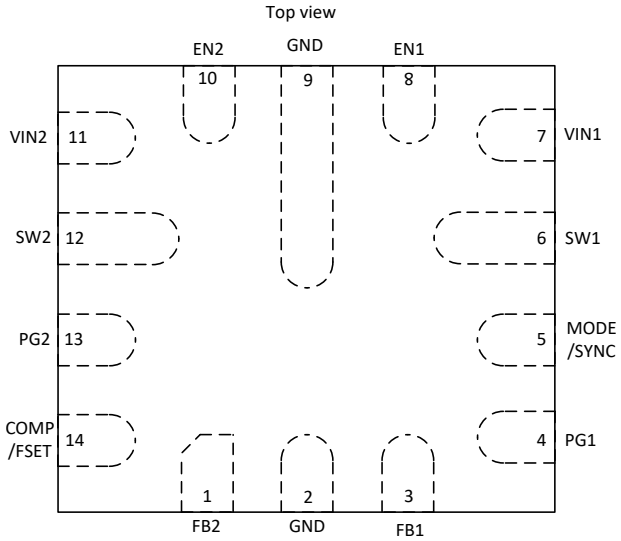


図 6-1. 14-Pin QFN RQR Package Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN1	8	I	This pin is the enable pin of converter 1. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
EN2	10	I	This pin is the enable pin of converter 2. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB1	3	I	Voltage feedback input for converter 1. Connect the resistive output voltage divider to this pin.
FB2	1	I	Voltage feedback input for converter 2. Connect the resistive output voltage divider to this pin.
PG1	4	O	Open-drain power-good output of converter 1
PG2	13	O	Open-drain power-good output of converter 2
SW1	6		This pin is the switch pin of converter 1 and is connected to the internal power MOSFETs.
SW2	12		This pin is the switch pin of converter 2 and is connected to the internal power MOSFETs.
MODE/SYNC	5	I	The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external frequency. See the electrical characteristics for the detailed specification for the digital signal applied to this pin for external synchronization.
COMP/FSET	14	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized. Do not leave this pin floating.
VIN1	7	—	Power supply input. Make sure the input capacitor is connected as close as possible between pin VIN1 and GND. Connect VIN1 to VIN2.
VIN2	11	—	Power supply input. Make sure the input capacitor is connected as close as possible between pin VIN2 and GND. Connect VIN2 to VIN1.

表 6-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2, 9	—	Ground pins. The GND pins are internally connected.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN1, VIN2	–0.3	6.5	V
	SW1, SW2 (DC)	–0.3	V_{IN} + 0.3	V
	SW1, SW2 (AC, less than 10ns)(3)	–3	10	V
	FB1, FB2	–0.3	4	V
	PG1, PG2, COMP/FSET	–0.3	V_{IN} + 0.3	V
	EN1, EN2, MODE/SYNC	–0.3	6.5	V
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN1}, V_{IN2}	Input voltage range	2.75		6	V
V_{OUT1} , V_{OUT2}	Output voltage range	0.6		5.5	V
L_1, L_2	Effective inductance	0.32	0.47	0.9	µH
C_{OUT1} , C_{OUT2}	Effective output capacitance(1)	8	10	200	µF
C_{IN1}, C_{IN2}	Effective input capacitance on each pin (1)		10		µF
R_{CF}		4.5		100	kΩ
I_{SINK_PG}	Sink current at PG pin	0		2	mA
T_J	Junction temperature	–40		150	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied. Further restrictions may apply. Please see the feature description for COMP/FSET about the output capacitance vs compensation setting and output voltage.

7.4 Thermal Information

THERMAL METRIC(1)		TPS6244x (JEDEC) 14 PINS	TPS6244x (EVM) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.7	53.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.8	n/a	°C/W

7.4 Thermal Information (continued)

THERMAL METRIC(1)		TPS6244x (JEDEC) 14 PINS	TPS6244x (EVM) 14 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	15.1	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.5	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.9	20.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

Over operating junction remperature range (T_J = -40°C to +150°C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN1 or EN2 = V_{IN}, no load, device not switching, T_J = 25°C, MODE = GND, one converter enabled			27	µA
I_Q	Quiescent current	EN1 or EN2 = V_{IN}, no load, device not switching, MODE = GND, one converter enabled		22	66	µA
I_Q	Quiescent current	EN1 = EN2 = V_{IN}, no load, device not switching, T_J = 25°C, MODE = GND, both converters enabled			38	µA
I_Q	Quiescent current	EN1 = EN2 = V_{IN}, no load, device not switching, MODE = GND, both converters enabled		33	80	µA
I_{SD}	Shutdown current	EN1 = EN2 = Low, at T_J = 25°C			2	µA
I_{SD}	Shutdown current	EN1 = EN2 = GND, Nominal value at T_J = 25°C, Max value at T_J = 150°C		1.5	26	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} rising	2.5	2.6	2.75	V
		V_{IN} falling	2.3	2.5	2.6	V
T_{JSD}	Thermal shutdown threshold	T_J rising		170		°C
	Thermal shutdown hysteresis	T_J falling		15		°C
CONTROL and INTERFACE						
$V_{EN,IH}$	Input-threshold voltage at EN1, EN2, rising edge		1.06	1.1	1.15	V
$V_{EN,IL}$	Input-threshold voltage at EN1, EN2, falling edge		0.96	1.0	1.05	V
$I_{EN,LKG}$	Input leakage current into EN1, EN2	V_{IH} = V_{IN} or V_{IL} = GND			450	nA
V_{IH}	High-level input-threshold voltage at MODE/SYNC		1.1			V
V_{IL}	Low-level input-threshold voltage at MODE/SYNC				0.3	V
I_{LKG}	Input leakage current into MODE/SYNC				700	nA
t_{Delay}	Enable delay time	Time from ENx high to device starts switching; V_{IN} applied already	110	200	300	µs
t_{Delay}	Enable delay time if one converter already enabled	Time from ENx high to device starts switching; V_{IN} applied already		100		µs
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good; device not in current limit	0.7	1.1	1.5	ms

7.5 Electrical Characteristics (continued)

Over operating junction remperature range (T_J = -40°C to +150°C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYNC}	Frequency range on MODE/SYNC pin for synchronization		2		4	MHz
	Resistance from COMP/FSET to GND for logic low	internal frequency setting with f = 2.25 MHz	0		2.5	kΩ
	Voltage on COMP/FSET for logic high	internal frequency setting with f = 2.25 MHz		V_{IN}		V
V_{TH_PG}	UVP power good threshold voltage; dc level	rising (%V_{FB})	94%	96.5%	99%	
V_{TH_PG}	UVP power good threshold voltage; dc level	falling (%V_{FB})	92%	94.5%	97%	
V_{TH_PG}	OVP power good threshold voltage; dc level	rising (%V_{FB})	104%	107%	110%	
	OVP power good threshold voltage; dc level	falling (%V_{FB})	102%	104.5%	107%	
$V_{PG,OL}$	Low-level output voltage at PG	I_{SINK_PG} = 2 mA		0.07	0.3	V
$I_{PG,LKG}$	Input leakage current into PG	V_{PG} = 5 V			100	nA
t_{PG}	PG deglitch time	for a high-level to low-level transition on the power good output		40		µs
OUTPUT						
V_{FB1}, V_{FB2}	Feedback voltage			0.6		V
$I_{FB1,LKG}$, $I_{FB2,LKG}$	Input leakage current into FB	V_{FB} = 0.6 V		1	80	nA
V_{FB1}, V_{FB2}	Feedback voltage accuracy	PWM, $V_{IN} \geq V_{OUT}$ + 1 V	–1%		1%	
V_{FB1}, V_{FB2}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, $V_{OUT} \geq$ 1.5 V, $C_{o,eff} \geq$ 22µF, L = 0.47µH	–1%		2.5%	
V_{FB1}, V_{FB2}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, 1V ≤ V_{OUT} < 1.5 V, $C_{o,eff} \geq$ 47µF, L = 0.47µH	-1%		2.5%	
	Load regulation	PWM		0.05		%/A
	Line regulation	PWM, I_{OUT} = 1 A, $V_{IN} \geq V_{OUT}$ + 1 V		0.02		%/V
R_{DIS}	Output discharge resistance			50	150	Ω
f_{SW}	PWM Switching frequency range	see the FSET pin functionality about setting the switching frequency	1.8	2.25	4	MHz
f_{SW}	PWM Switching frequency	with COMP/FSET tied to GND or V_{IN}	2.025	2.25	2.475	MHz
f_{SW}	PWM Switching frequency tolerance	using a resistor from COMP/FSET to GND	–16%		17%	
$t_{on,min}$	Minimum on-time of high-side FET	$V_{IN} \geq$ 3.3 V		50	75	ns
$t_{on,min}$	Minimum on-time of low-side FET			30		ns
$R_{DS(ON)}$	High-side FET on-resistance	$V_{IN} \geq$ 5 V		55	100	mΩ
	Low-side FET on-resistance	$V_{IN} \geq$ 5 V		25	50	mΩ
	High-side MOSFET leakage current			1	86	µA
	Low-side MOSFET leakage current			1	205	µA
I_{LIMH}	High-side FET switch current limit	DC value, for TPS62442; V_{IN} = 3 V to 6 V	3.8	4.7	5.5	A
I_{LIMH}	High-side FET switch current limit	DC value, for TPS62441; V_{IN} = 3 V to 6 V	2.1	2.6	3.1	A

7.5 Electrical Characteristics (continued)

Over operating junction remperature range (T_J = -40°C to +150°C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIMNEG}	Low-side FET negative current limit	DC value		–1.8		A

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
$f_{(SYNC)}$	Synchronization clock frequency range (MODE/SYNC)	Nominal f_{SW} determined through COMP/FSET	f_{SW}		f_{SW} + 20%	MHz
$D_{(SYNC)}$	Synchronization clock duty cycle range (MODE/SYNC)		45%		55%	

7.7 Typical Characteristics

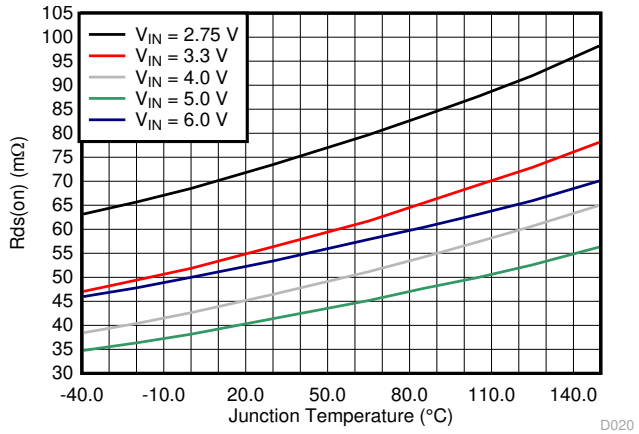


図 7-1. $R_{ds(on)}$ of High-Side Switch

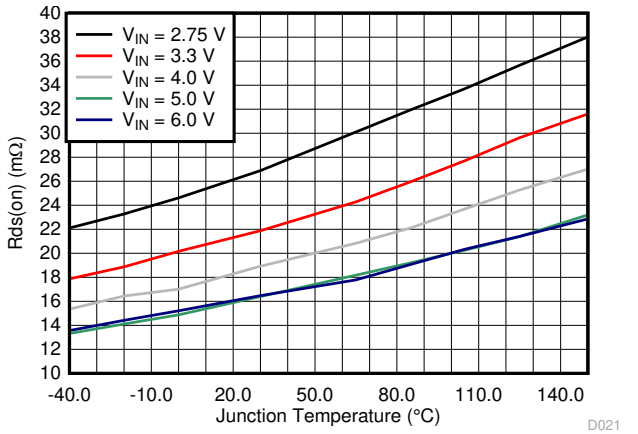


図 7-2. $R_{ds(on)}$ of Low-Side Switch

8 Parameter Measurement Information

8.1 Schematic

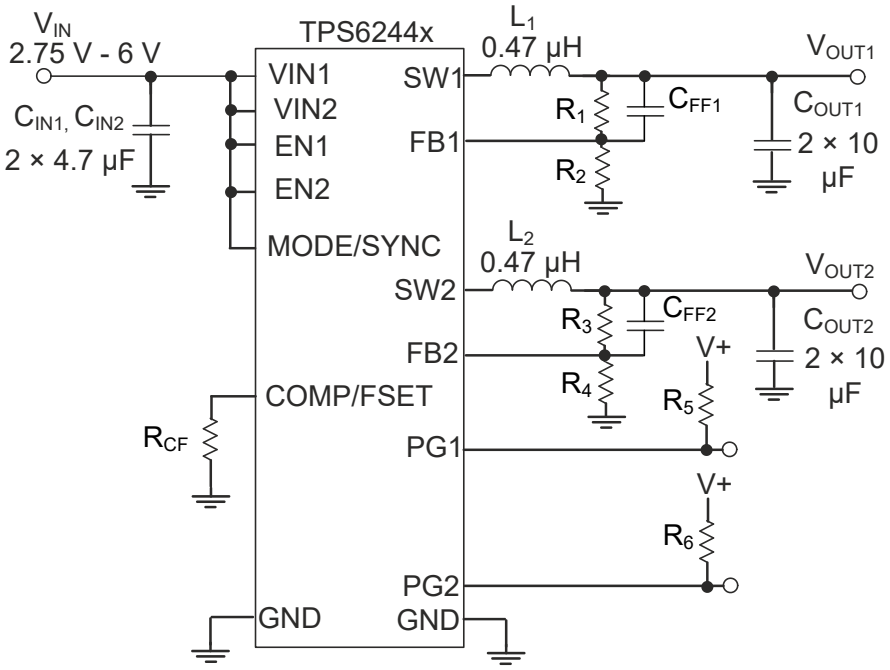


図 8-1. Measurement Setup

表 8-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPS62442RQRR	Texas Instruments
L1, L2	0.47-µH inductor DFE252012PD	Murata
C_{IN1}, C_{IN2}	4.7 µF / 6.3 V	Murata
C_{OUT1}, C_{OUT2}	2 × 10 µF / 6.3 V	Murata
R_{CF}	8.06 kΩ	any
C_{FF1}, C_{FF2}	10 pF	any
R_1	Depending on V_{OUT}	any
R_2	Depending on V_{OUT}	any
R_3	Depending on V_{OUT}	any
R_4	Depending on V_{OUT}	any
R_5, R_6	100 kΩ	any

(1) See the *Third-Party Products Disclaimer*.

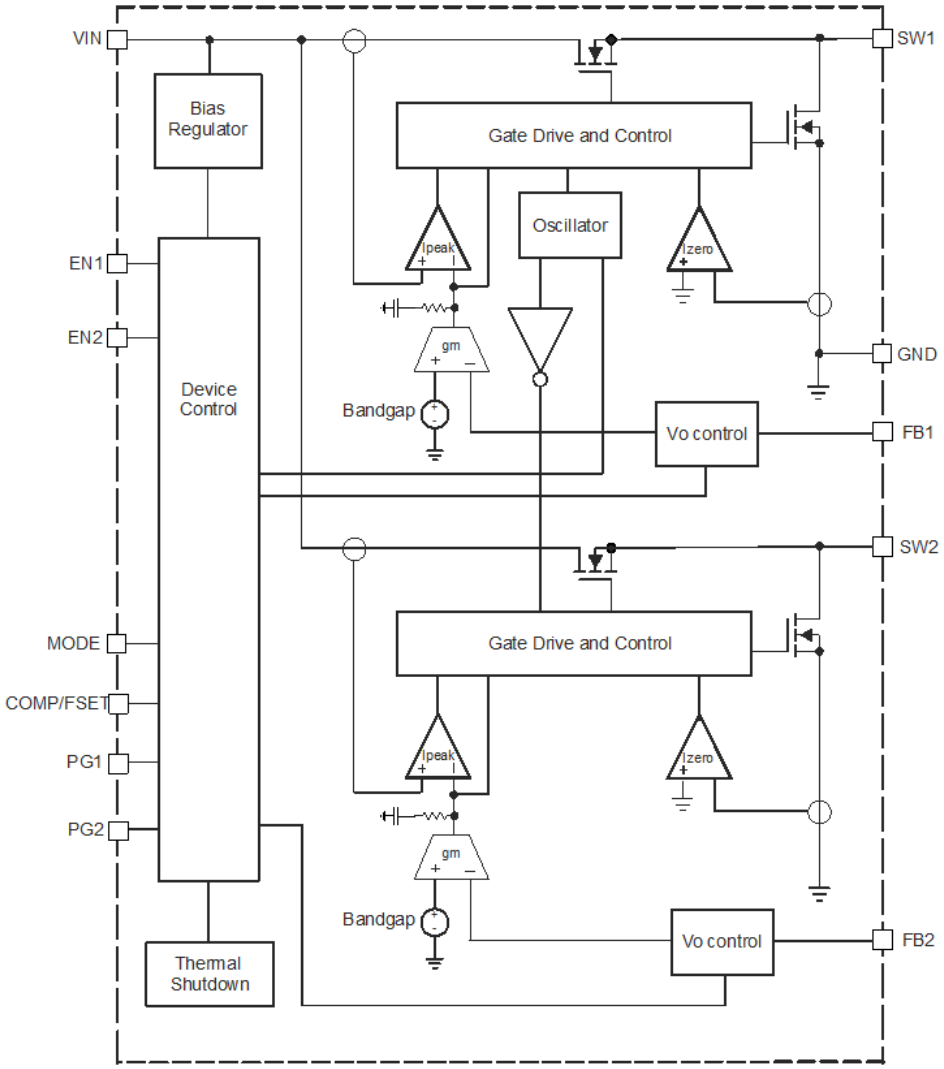
9 Detailed Description

9.1 Overview

The TPS6244x synchronous dual switch mode power converters are based on a peak current mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with TPS6244x, the internal compensation has two settings. See *COMP/FSET*. One of the two compensation settings is chosen either by a resistor from COMP/FSET to GND, or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors. The devices can be operated without a feedforward capacitor on the output voltage divider, however, using a typically 10-pF feed forward capacitor improves transient response.

The devices support forced fixed-frequency PWM operation with the MODE pin tied to a logic high level. The frequency is defined as either 2.25 MHz internally fixed when COMP/FSET is tied to GND or VIN or in a range of 1.8 MHz to 4 MHz defined by a resistor from COMP/FSET to GND. Alternatively, the devices can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz, applied to the MODE pin with no need for additional passive components. External synchronization can only be used when there is a resistor from COMP/FSET to GND. When COMP/FSET is directly tied to GND or VIN, the TPS6244x cannot be synchronized externally. The TPS6244x allows for a change from internal clock to external clock during operation. When the MODE pin is set to a logic low level, the device operates in power save mode (PFM) at low output current and automatically transfers to fixed frequency PWM mode at higher output current. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current. When a converter switches from PFM to PWM operation, there can be a maximum delay of one clock cycle because in this case, the converter has to synchronize to the other converter to achieve 180 degrees phase shift.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Precise Enable (EN)

The voltage applied at EN1 and EN2 is compared to a fixed threshold of 1.1 V for a rising voltage. This comparison allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The precise enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of EN1 and EN2.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS6244x starts operation when the rising threshold is exceeded. For proper operation, the enable (EN) pin must be terminated and must not be left floating. Pulling the enable pin low forces the device into shutdown, with a shutdown current of typically 1.5 µA. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

The enable delay time is defined from EN1 or EN2 going high to when the converter starts switching. The converter is enabled first, the internal bandgap is started, and bias currents and configuration bits are read, so its start-up delay time is longer than for the converter being enabled when this is already done.

9.3.2 COMP/FSET

This pin allows to set three different parameters:

- Internal compensation settings for the control loop (two settings available)
- The switching frequency in PWM mode from 1.8 MHz to 4 MHz
- Enable/ disable spread spectrum clocking (SSC)

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows the user to adopt the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at start-up of the converter, so a change in the resistor during operation only has an effect on the switching frequency but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined setting. Do not leave the pin floating.

The switching frequency has to be selected based on the input voltage and the output voltage to meet the specifications for the minimum on time and minimum off time.

Example:

$V_{IN} = 5.5V;\ V_{OUT} = 1\ \Rightarrow Duty\ Cycle = \frac{1V}{5.5V} = 0.2$

$t_{on,min} = \frac{1}{f_s} \times 0.2$

$f_{sw,max} = \frac{1}{t_{on,min}} \times 0.2 = \frac{1}{0.075\mu s} \times 0.2 = 2.67MHz$

The compensation range has to be chosen based on the minimum capacitance used. The capacitance can be increased from the minimum value as given in 表 9-1, up to the maximum of 200-µF effective capacitance in both compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1 with spread spectrum clocking (SSC) disabled:

$$R_{CF}(k\Omega) = \frac{18\ MHz\ \times k\Omega}{fs(MHz)} - 0.18k \quad (1)$$

For compensation (comp) setting 1 with spread spectrum clocking (SSC) enabled:

$$R_{CF}(k\Omega) = \frac{60\ MHz\ \times k\Omega}{fs(MHz)} - 0.6k \quad (2)$$

For compensation (comp) setting 2 with spread spectrum clocking (SSC) disabled:

$$R_{CF}(k\Omega) = \frac{180\ MHz\ \times k\Omega}{fs(MHz)} - 1.8k \quad (3)$$

表 9-1. Switching Frequency, Compensation, and Spread Spectrum Clocking

R_{CF}	COMPENSATION	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE FOR VOUT < 1 V	MINIMUM OUTPUT CAPACITANCE FOR 1 V ≤ VOUT < 3.3 V	MINIMUM OUTPUT CAPACITANCE FOR VOUT ≥ 3.3 V
10 kΩ .. 4.5 kΩ	for smallest output capacitance (comp setting 1) SSC disabled	1.8 MHz (10 kΩ) .. 4 MHz (4.5 kΩ) according to 式 1	11 µF	7 µF	5 µF
33 kΩ .. 18 kΩ	for smallest output capacitance (comp setting 1) SSC enabled	1.8 MHz (33 kΩ) .. 4 MHz (18 kΩ) according to 式 2	11 µF	7 µF	5 µF
100 kΩ .. 45 kΩ	for best transient response (larger output capacitance) (comp setting 2) SSC disabled	1.8 MHz (100 kΩ) ..4 MHz (45 kΩ) according to 式 3	30 µF	18 µF	15 µF
tied to GND	for smallest output capacitance (comp setting 1) SSC disabled	internally fixed 2.25 MHz	11 µF	7 µF	5 µF
tied to V_{IN}	for best transient response (larger output capacitance) (comp setting 2) SSC enabled	internally fixed 2.25 MHz	30 µF	18 µF	15 µF

Refer to セクション 10.1.2.2.2 for further details on the output capacitance required depending on the output voltage.

A too-high resistor value for R_{CF} is decoded as "tied to V_{IN}", a value below the lowest range as "tied to GND". The minimum output capacitance in 表 9-1 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

9.3.3 MODE/SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin allows the user to force PWM mode when set high. The pin also allows the user to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. Similar to COMP/FSET, the specifications for the minimum on time and minimum off time have to be observed when setting the external frequency. For use with external synchronization on the MODE/SYNC pin, the internal switching frequency must be set by R_{CF} to a similar value of the externally applied clock. This makes sure that, if the external clock fails, the switching frequency stays in the same range and the compensation settings are still valid. When there is no resistor from COMP/FSET to GND but the pin is pulled high or low, external synchronization is not possible. If the device is externally synchronized, both converters are forced to run on that clock frequency preserving 180° phase relation. The internally generated spread spectrum clocking is turned off while running on an external clock.

9.3.4 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

9.3.5 Power-Good Output (PG)

Power good is an open-drain output driven by a window comparator. PG is held low when the device is:

- Disabled
- In undervoltage lockout
- In thermal shutdown
- Not in soft start

When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the output is high impedance.

表 9-2. PG Status

EN	DEVICE STATUS	PG STATE
X	V_{IN} < 2 V	undefined
low	V_{IN} ≥ 2 V	low
high	2 V ≤ V_{IN} ≤ UVLO OR in thermal shutdown OR V_{OUT} not in regulation OR device in soft start	low
high	V_{OUT} in regulation	high impedance

9.3.6 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 170°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power FETs of both converters are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 20°C, the converters resume normal operation, beginning with soft start. When both converters are in a PFM pause, the thermal shutdown is not active. After the PFM pause, the device needs up to 9 µs to detect a too high junction temperature. If the PFM burst is shorter than this delay, the device does not detect a too high junction temperature. As long as one converter is in PWM, thermal shutdown is always active.

9.4 Device Functional Modes

9.4.1 Pulse Width Modulation (PWM) Operation

The TPS6244x has two operating modes. Forced PWM mode is discussed in this section and PWM/PFM as discussed in セクション 9.4.2.

With the MODE/SYNC pin set to high, the TPS6244x operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP pin to GND or by an external clock signal applied to the MODE/SYNC pin. With an external clock applied to MODE/SYNC, the TPS6244x follows the frequency applied to the pin. The frequency must be in a range the device can operate at, taking the minimum on time into account.

9.4.2 Power Save Mode Operation (PWM/PFM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of approximately 0.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency.

9.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as D = V_{OUT} / V_{IN}. The duty cycle increases as the input voltage comes close to the output voltage and the off time gets smaller. When the minimum off time of typically 30 ns is reached, the TPS6244x skips switching cycles while it approaches 100% mode. In 100% mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. In 100% mode, the low side switch is turned off. The maximum dropout voltage in 100% mode is the product of the on-resistance of the high-side switch plus the series resistance of the inductor and the load current.

9.4.4 Current Limit and Short-Circuit Protection

The TPS6244x is protected against overload and short circuit events. The converter is not switching with the fixed frequency when in current limit. The converter resumes the fixed frequency operation when the converter leaves current limit condition. If the inductor current exceeds the current limit, I_{LIMH}, the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side switch turns on again only if the current in the low-side switch has decreased below the low-side current limit. This can cause bursts or single pulses between the high-side and low-side current limit. Due to internal propagation delay, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \times t_{PD} \quad (4)$$

where

- I_{LIMH} is the static current limit as specified in the electrical characteristics.
- L is the effective inductance at the peak current.
- V_L is the voltage across the inductor (V_{IN} – V_{OUT}).
- t_{PD} is the internal propagation delay of typically 50 ns.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \times 50ns \quad (5)$$

9.4.5 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active after the TPS6244x has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V. Output discharge is not activated during a current limit or foldback current limit event.

9.4.6 Soft Start

The internal soft-start circuitry controls the output voltage slope during start-up. This action avoids excessive inrush current and ensures a controlled output voltage rise time. This action also prevents unwanted voltage drops from high impedance power sources or batteries. When EN1 and EN2 are set high, the device starts switching after t_{Delay}. The output voltage is ramped with a slope defined by t_{Ramp}.

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

10.1.1 Programming the Output Voltage

The output voltage of the TPS6244x is adjustable. The output voltage can be programmed for output voltages from 0.6 V to 5.5 V, using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from 式 6. TI recommends to choose resistor values, which allows a current of at least 6 µA, meaning the value of R_2 mu×–st not exceed 100 kΩ. TI recommends lower resistor values for highest accuracy and most robust design.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \tag{6}$$

10.1.2 External Component Selection

10.1.2.1 Inductor Selection

The TPS6244x is designed for a nominal 0.47-µH inductor with a switching frequency of typically 2.25 MHz. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 0.47 µH cause a larger inductor current ripple, which causes larger negative inductor current in forced PWM mode at low or no output current. For a higher or lower nominal switching frequency, the inductance must be changed accordingly.

The inductor selection is affected by several effects like the following:

- Inductor ripple current
- Output ripple voltage
- PWM-to-PFM transition point
- Efficiency

In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). THe following equation calculates the maximum inductor current.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \tag{7}$$

$$\Delta I_{L(max)} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L_{min}} \times \frac{1}{f_{sw}} \tag{8}$$

where

- $I_{L(max)}$ is the maximum inductor current.
- $\Delta I_{L(max)}$ is the peak-to-peak inductor ripple current.
- Lmin is the minimum inductance at the operating point.

表 10-1. Typical Inductors

TYPE	INDUCTANCE [µH]	CURRENT [A](1)	FOR DEVICE	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [L × B × H] mm	MANUFACTURER(2)
DFE201210U-R47M	0.47 µH, ±20%	see data sheet	TPS62442	2.25 MHz	2.0× 1.2 × 1.0	Murata
DFE201210U-R68M	0.68 µH, ±20%	see data sheet	TPS62441	2.25 MHz	2.0 × 1.2 × 1.0	Murata

表 10-1. Typical Inductors (continued)

TYPE	INDUCTANCE [µH]	CURRENT [A](1)	FOR DEVICE	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [L × B × H] mm	MANUFACTURER(2)
DFE201610E-R47M#	0.47 µH, ±20%	see data sheet	TPS62442	2.25 MHz	2.0 × 1.6 × 1.0	Murata
XEL3515-561ME	0.56 µH, ±20%	4.5	TPS62442	2.25 MHz	3.5 × 3.2 × 1.5	Coilcraft
XFL4015-701ME	0.70 µH, ±20%	5.3	TPS62442	2.25 MHz	4.0 × 4.0 × 1.6	Coilcraft
XFL4015-471ME	0.47 µH, ±20%	5.4	TPS62442	2.25 MHz	4.0 × 4.0 × 1.6	Coilcraft
TFM201610ALM-R47MTAA	0.47 µH, ±20%	5.8	TPS62442	2.25 MHz	2.0 × 1.6 × 1.0	TDK

(1) Lower of I_{RMS} at 20°C rise or I_{SAT} at 20% drop.
(2) See the *Third-Party Products Disclaimer*.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. TI recommends to add a margin of about 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well.

10.1.2.2 Capacitor Selection

10.1.2.2.1 Input Capacitor

For most applications, 10-µF nominal is sufficient and recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins.

10.1.2.2.2 Output Capacitor

The architecture of the TPS6244x allows the use of tiny ceramic output capacitors with low-equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode. By changing the device compensation with a resistor from COMP/FSET to GND, the device can be compensated in three steps based on the minimum capacitance used on the output. The maximum capacitance is 200 µF in any of the compensation settings.

10.2 Typical Application

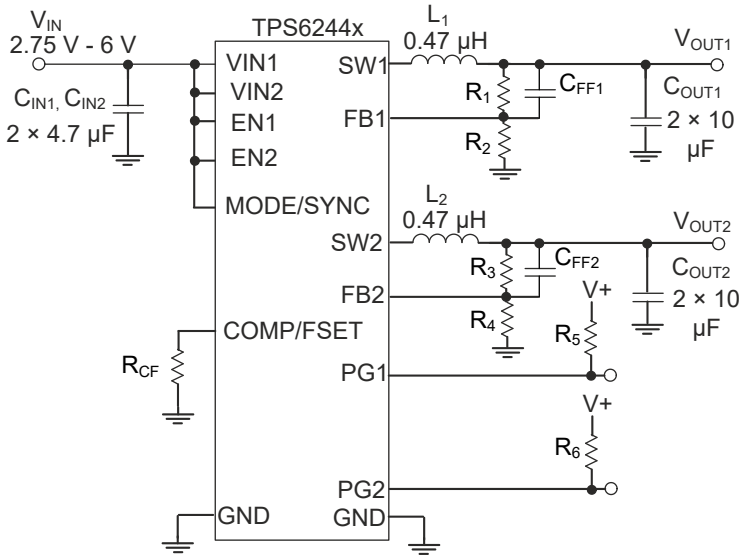


図 10-1. Typical Application Schematic

10.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

10.2.2 Detailed Design Procedure

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad (9)$$

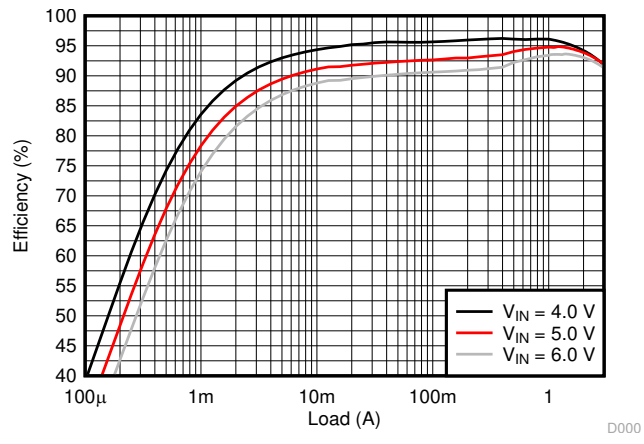
With V_{FB} = 0.6 V:

表 10-2. Setting the Output Voltage

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1, R_3	R_2, R_4	C_{FF1}, C_{FF2}	EXACT OUTPUT VOLTAGE
0.8 V	16.9 kΩ	51 kΩ	10 pF	0.7988 V
1.0 V	20 kΩ	30 kΩ	10 pF	1.0 V
1.1 V	39.2 kΩ	47 kΩ	10 pF	1.101 V
1.2 V	68 kΩ	68 kΩ	10 pF	1.2 V
1.5 V	76.8 kΩ	51 kΩ	10 pF	1.5 V
1.8 V	80.6 kΩ	40.2 kΩ	10 pF	1.803 V
2.5 V	47.5 kΩ	15 kΩ	10 pF	2.5 V
3.3 V	88.7 kΩ	19.6 kΩ	10 pF	3.315 V

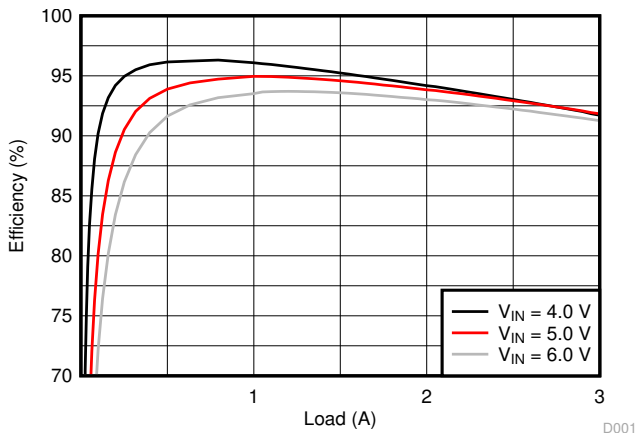
10.2.3 Application Curves

All plots have been taken with a nominal switching frequency of 2.25 MHz when set to PWM mode, unless otherwise noted. The BOM is according to 表 8-1.



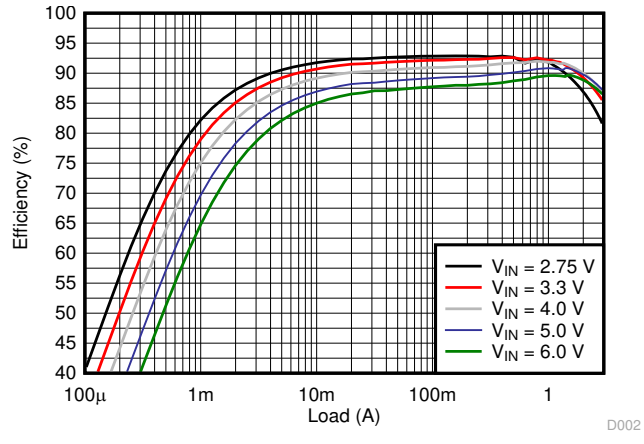
V_{OUT} = 3.3 V PFM T_A = 25°C

図 10-2. Efficiency Versus Output Current



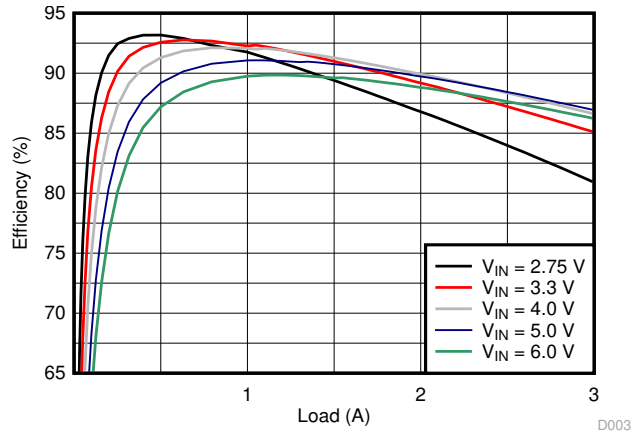
V_{OUT} = 3.3 V PWM T_A = 25°C

図 10-3. Efficiency Versus Output Current



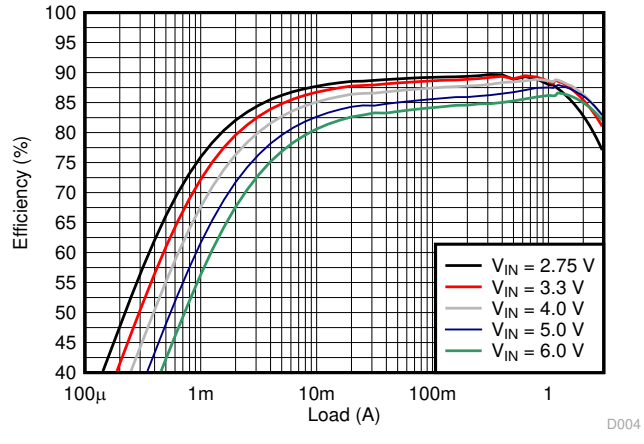
V_{OUT} = 1.8 V PFM T_A = 25°C

図 10-4. Efficiency Versus Output Current



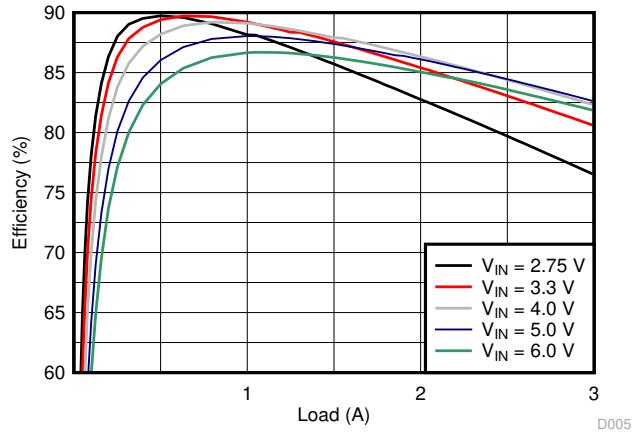
V_{OUT} = 1.8 V PWM T_A = 25°C

図 10-5. Efficiency Versus Output Current



V_{OUT} = 1.2 V PFM T_A = 25°C

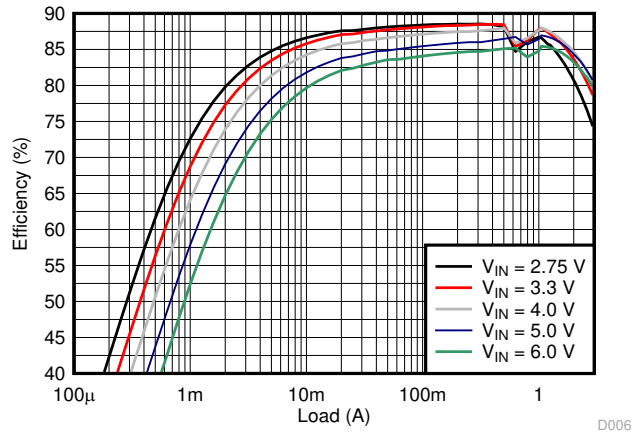
図 10-6. Efficiency Versus Output Current



V_{OUT} = 1.2 V PWM T_A = 25°C

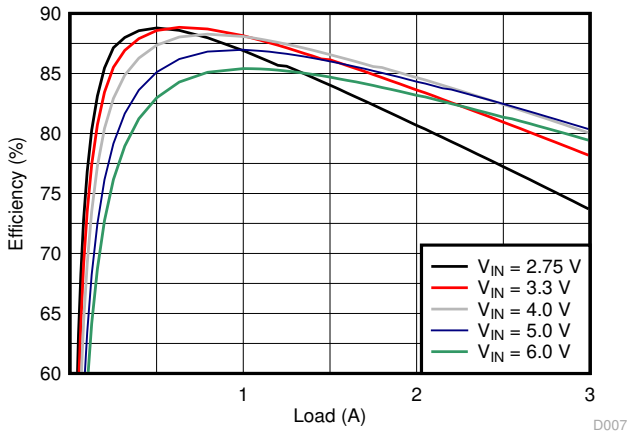
図 10-7. Efficiency Versus Output Current

10.2.3 Application Curves (continued)



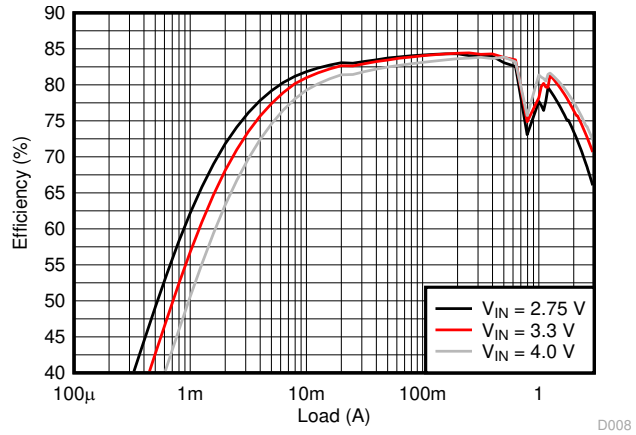
V_{OUT} = 1.0 V PFM T_A = 25°C

図 10-8. Efficiency Versus Output Current



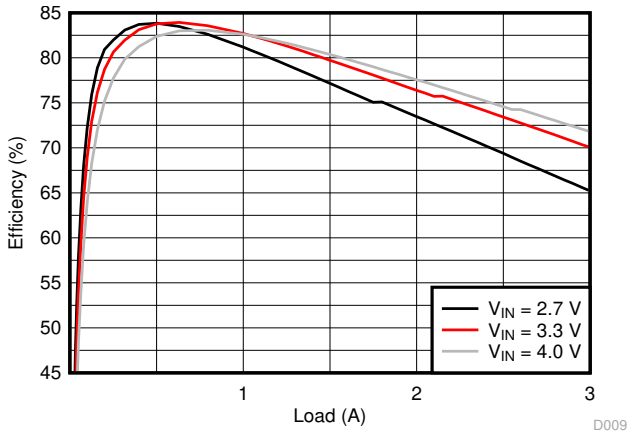
V_{OUT} = 1.0 V PWM T_A = 25°C

図 10-9. Efficiency Versus Output Current



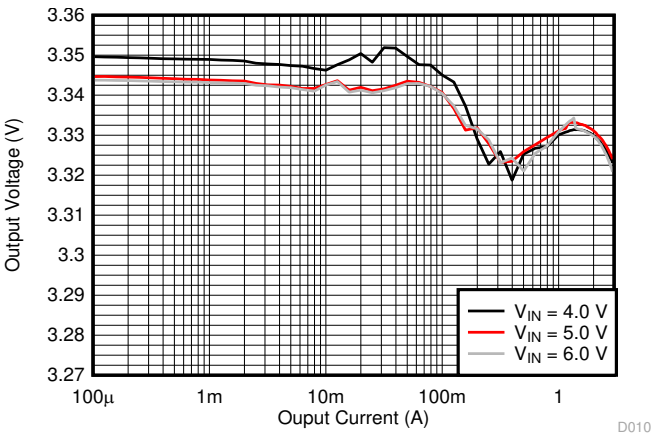
V_{OUT} = 0.6 V PFM T_A = 25°C

図 10-10. Efficiency Versus Output Current



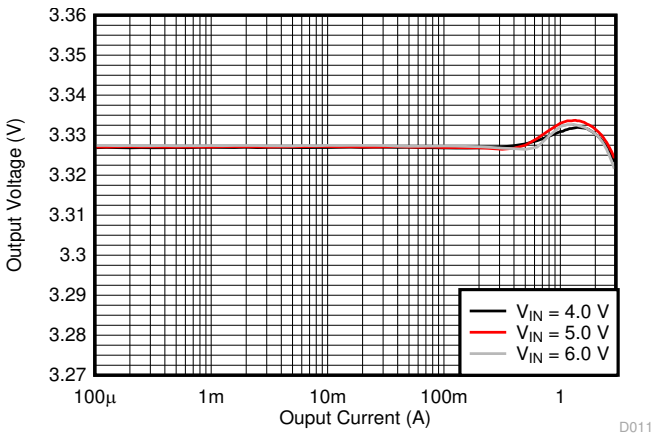
V_{OUT} = 0.6 V PWM T_A = 25°C

図 10-11. Efficiency Versus Output Current



V_{OUT} = 3.3 V PFM T_A = 25°C

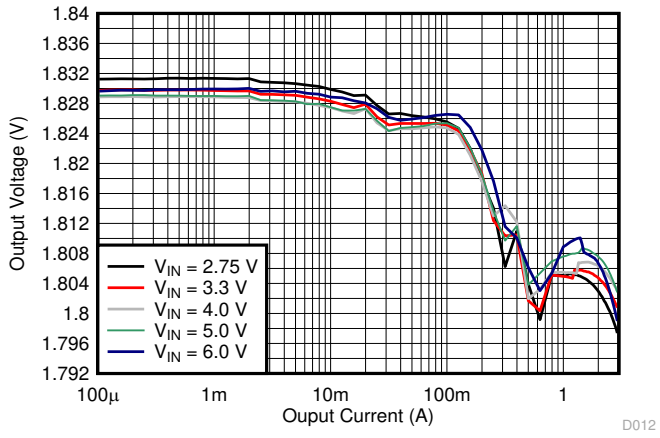
図 10-12. Output Voltage Versus Output Current



V_{OUT} = 3.3 V PWM T_A = 25°C

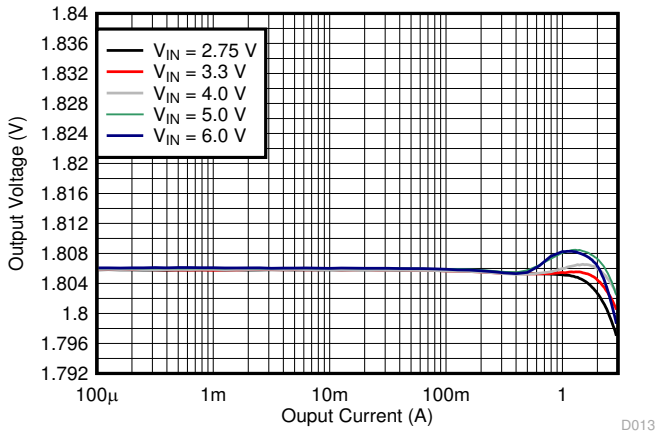
図 10-13. Output Voltage Versus Output Current

10.2.3 Application Curves (continued)



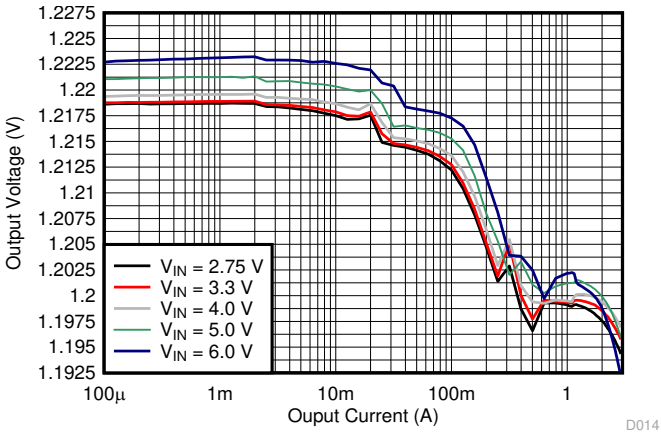
V_{OUT} = 1.8 V PFM T_A = 25°C

図 10-14. Output Voltage Versus Output Current



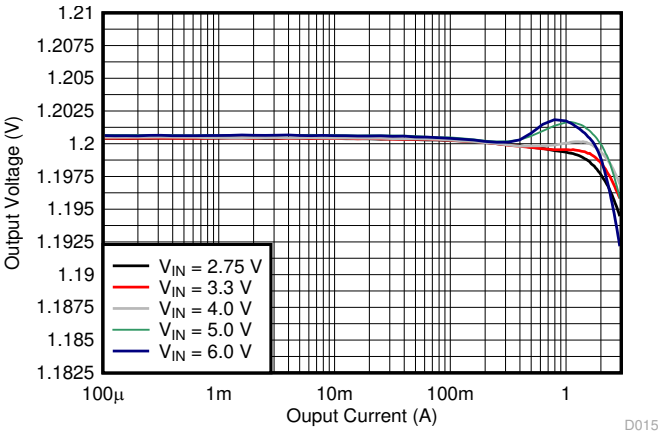
V_{OUT} = 1.8 V PWM T_A = 25°C

図 10-15. Output Voltage Versus Output Current



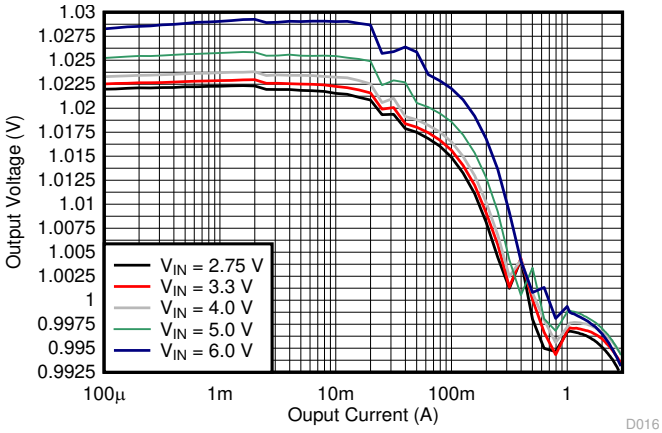
V_{OUT} = 1.2 V PFM T_A = 25°C

図 10-16. Output Voltage Versus Output Current



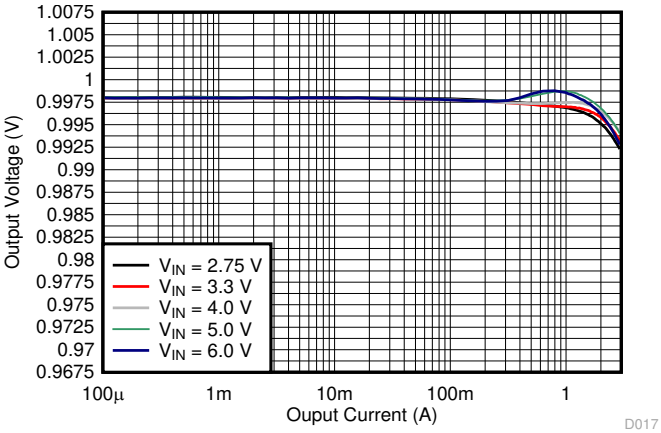
V_{OUT} = 1.2 V PWM T_A = 25°C

図 10-17. Output Voltage Versus Output Current



V_{OUT} = 1.0 V PFM T_A = 25°C

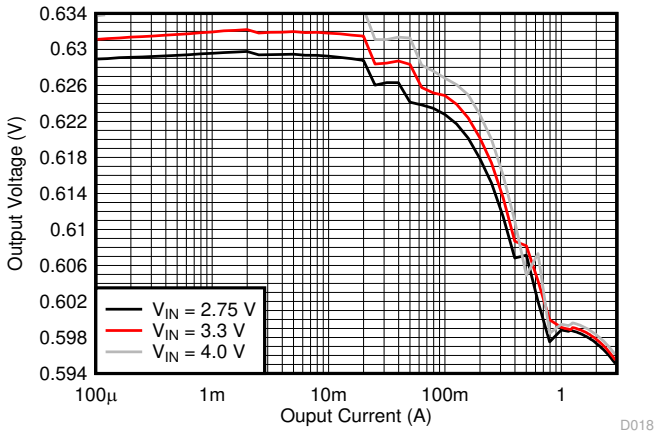
図 10-18. Output Voltage Versus Output Current



V_{OUT} = 1.0 V PWM T_A = 25°C

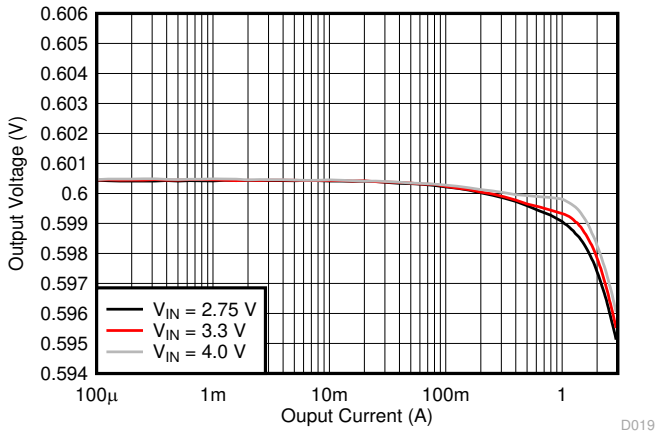
図 10-19. Output Voltage Versus Output Current

10.2.3 Application Curves (continued)



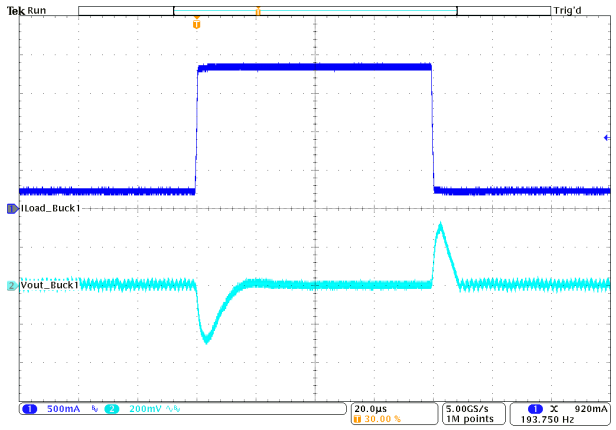
V_{OUT} = 0.6 V PFM T_A = 25°C

図 10-20. Output Voltage Versus Output Current



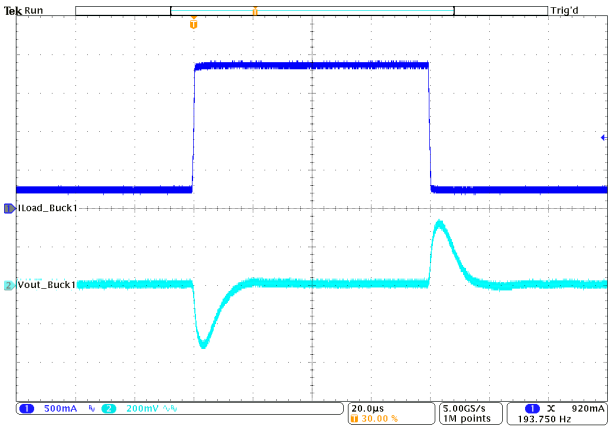
V_{OUT} = 0.6 V PWM T_A = 25°C

図 10-21. Output Voltage Versus Output Current



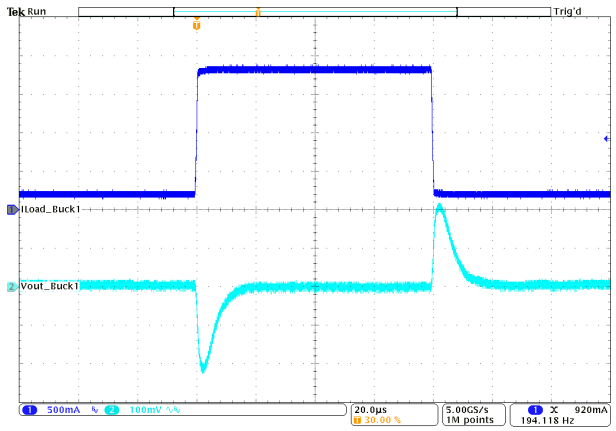
V_{OUT} = 3.3 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

図 10-22. Load Transient Response



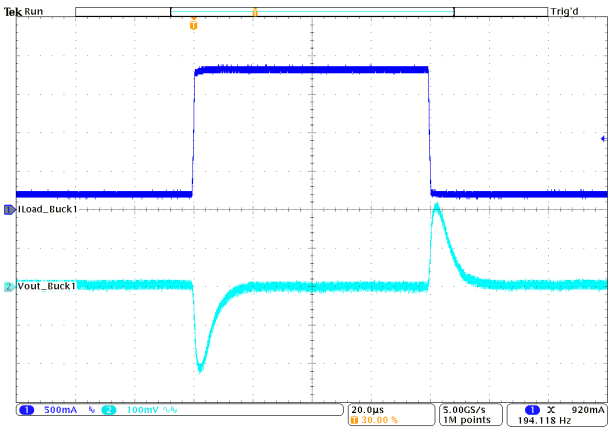
V_{OUT} = 3.3 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

図 10-23. Load Transient Response



V_{OUT} = 1.8 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

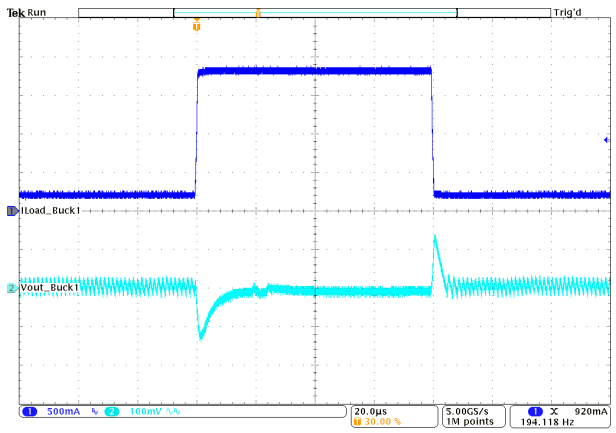
図 10-24. Load Transient Response



V_{OUT} = 1.8 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

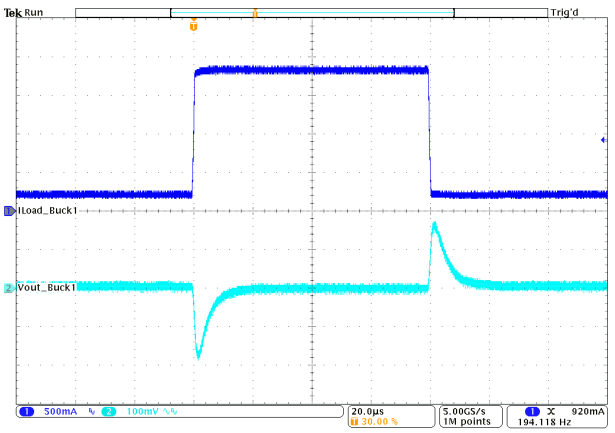
図 10-25. Load Transient Response

10.2.3 Application Curves (continued)



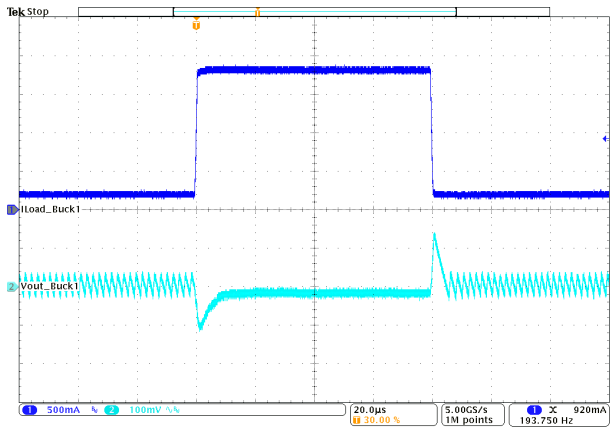
V_{OUT} = 1.2 V　　PFM　　T_A = 25°C
V_{IN} = 5.0 V　　I_{OUT} = 0.2 A to 1.8 A to 0.2 A

図 10-26. Load Transient Response



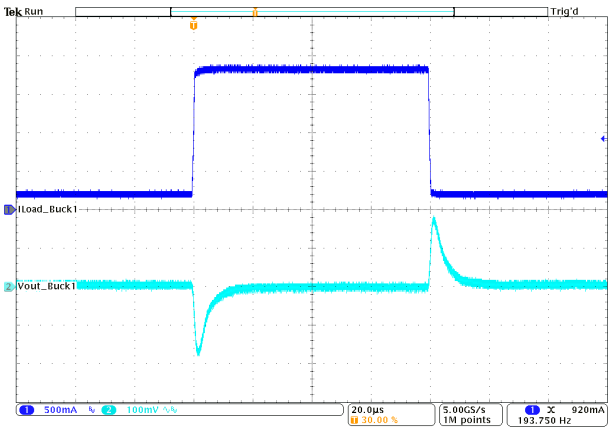
V_{OUT} = 1.2 V　　PWM　　T_A = 25°C
V_{IN} = 5.0 V　　I_{OUT} = 0.2 A to 1.8 A to 0.2 A

図 10-27. Load Transient Response



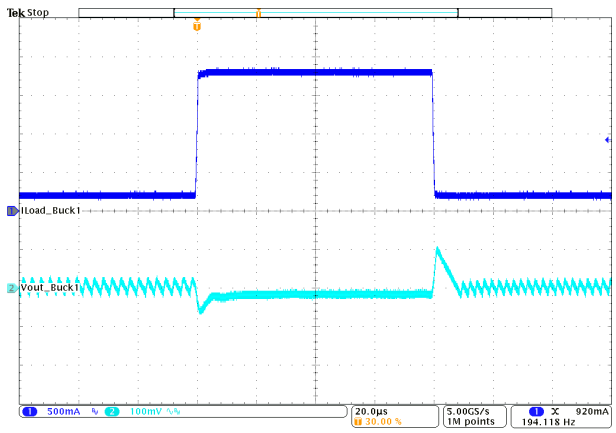
V_{OUT} = 1.0 V　　PFM　　T_A = 25°C
V_{IN} = 5.0 V　　I_{OUT} = 0.2 A to 1.8 A to 0.2 A

図 10-28. Load Transient Response



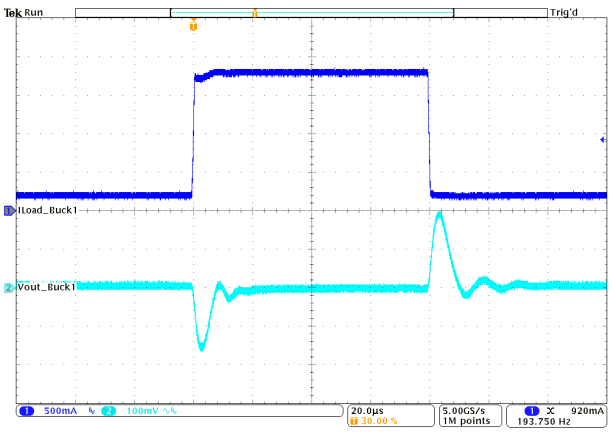
V_{OUT} = 1.0 V　　PWM　　T_A = 25°C
V_{IN} = 5.0 V　　I_{OUT} = 0.2 A to 1.8 A to 0.2 A

図 10-29. Load Transient Response



V_{OUT} = 0.6 V　　PFM　　T_A = 25°C
V_{IN} = 3.3 V　　I_{OUT} = 0.2 A to 1.8 A to 0.2 A

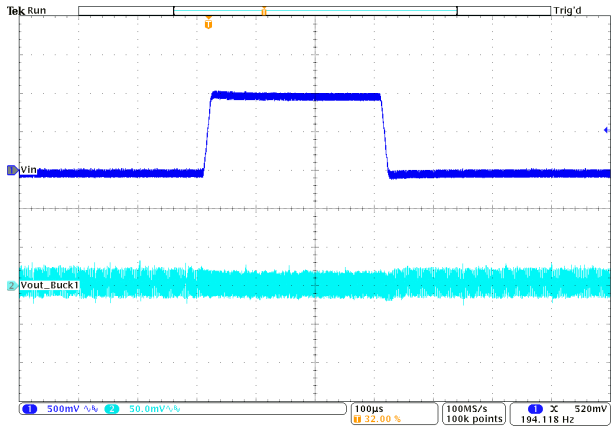
図 10-30. Load Transient Response



V_{OUT} = 0.6 V　　PWM　　T_A = 25°C
V_{IN} = 3.3 V　　I_{OUT} = 0.2 A to 1.8 A to 0.2 A

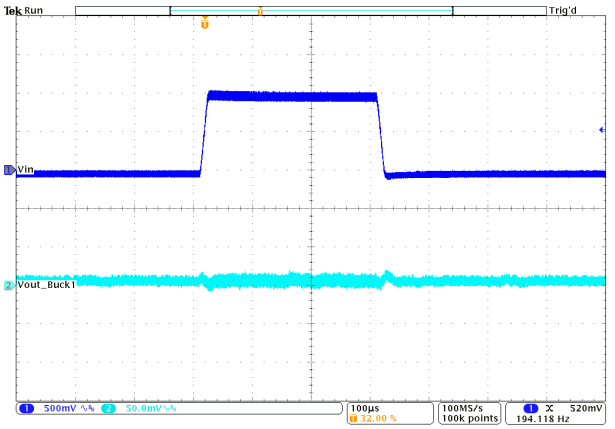
図 10-31. Load Transient Response

10.2.3 Application Curves (continued)



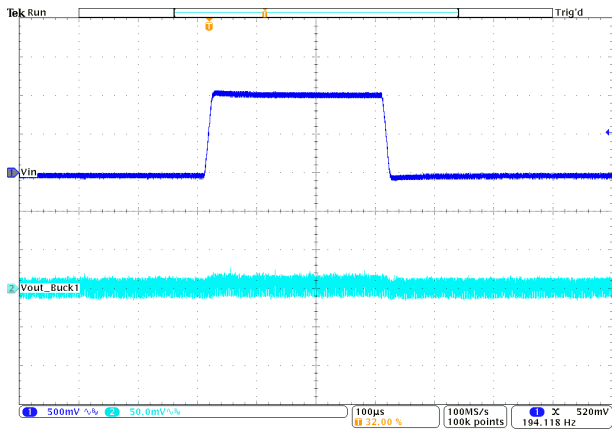
V_{OUT} = 3.3 V　　PFM　　T_A = 25°C
I_{OUT} = 0.3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

図 10-32. Line Transient Response



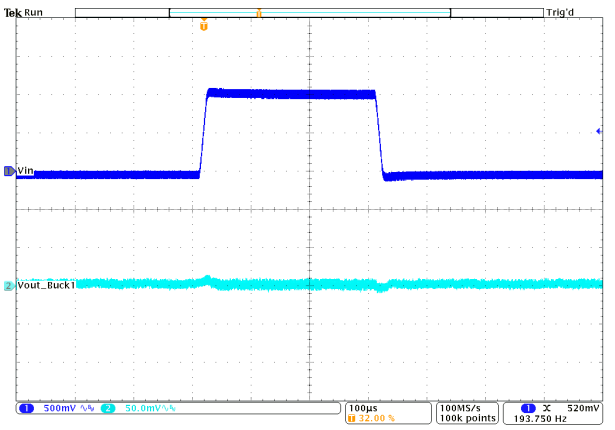
V_{OUT} = 3.3 V　　PWM　　T_A = 25°C
I_{OUT} = 3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

図 10-33. Line Transient Response



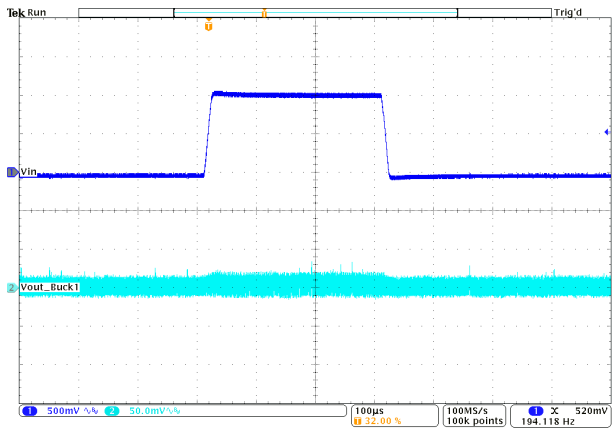
V_{OUT} = 1.8 V　　PFM　　T_A = 25°C
I_{OUT} = 0.3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

図 10-34. Line Transient Response



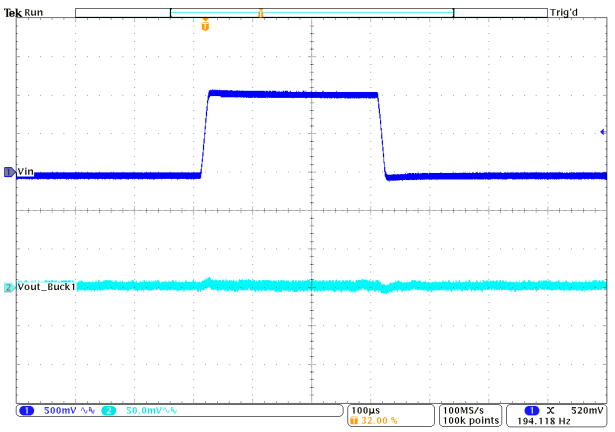
V_{OUT} = 1.8 V　　PWM　　T_A = 25°C
I_{OUT} = 3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

図 10-35. Line Transient Response



V_{OUT} = 1.2 V　　PFM　　T_A = 25°C
I_{OUT} = 0.3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

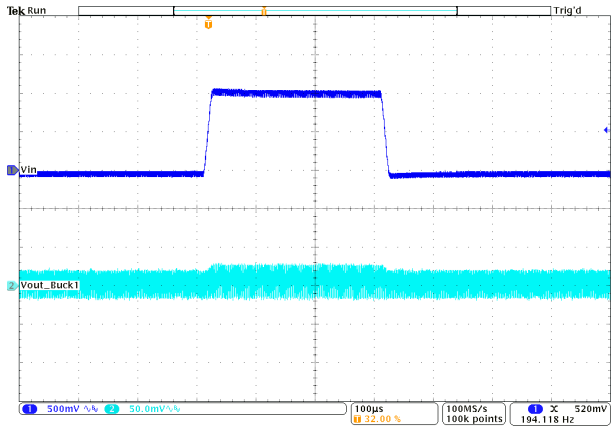
図 10-36. Line Transient Response



V_{OUT} = 1.2 V　　PWM　　T_A = 25°C
I_{OUT} = 3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

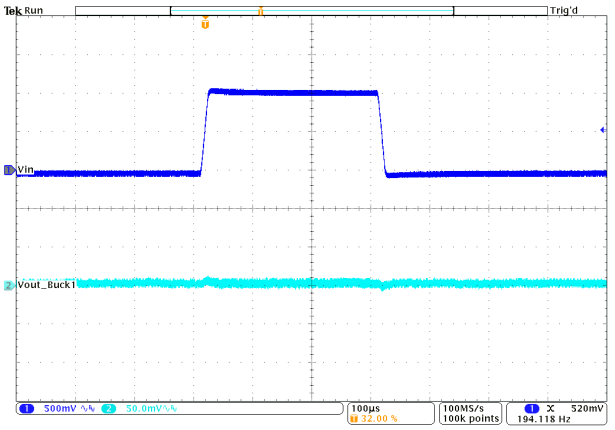
図 10-37. Line Transient Response

10.2.3 Application Curves (continued)



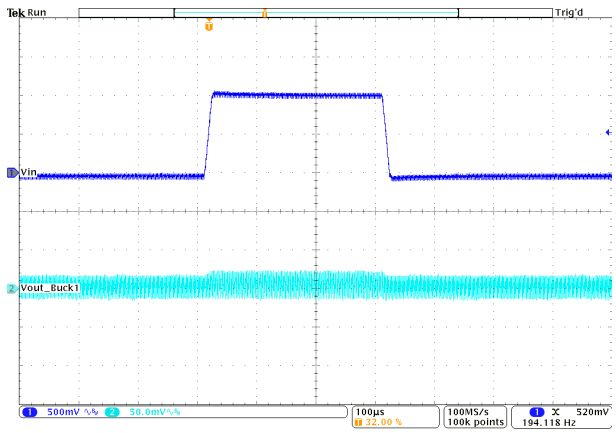
V_{OUT} = 1.0 V　　PFM　　T_A = 25°C
I_{OUT} = 0.3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

図 10-38. Line Transient Response



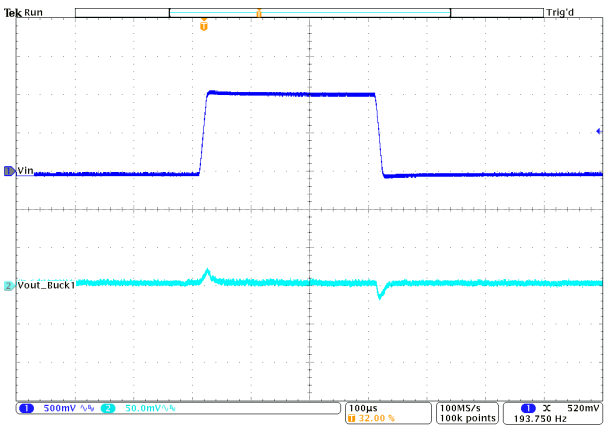
V_{OUT} = 1.0 V　　PWM　　T_A = 25°C
I_{OUT} = 3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

図 10-39. Line Transient Response



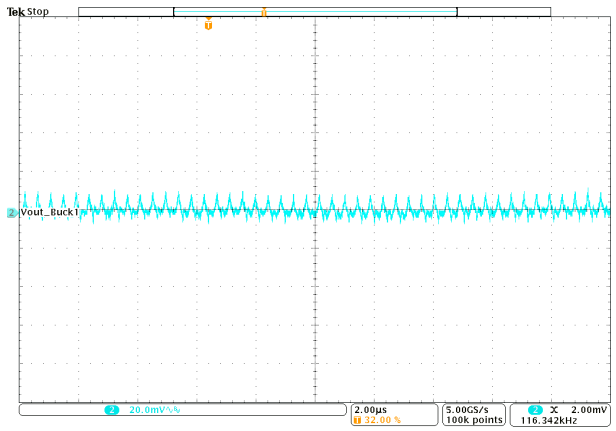
V_{OUT} = 0.6 V　　PFM　　T_A = 25°C
I_{OUT} = 0.3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

図 10-40. Line Transient Response



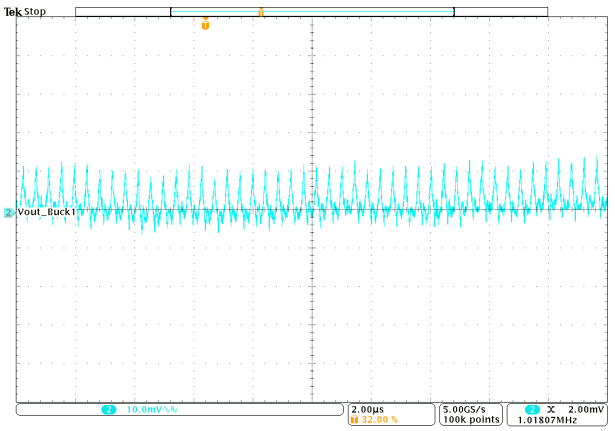
V_{OUT} = 0.6 V　　PWM　　T_A = 25°C
I_{OUT} = 3 A　　V_{IN} = 4.5 V to 5.5 V to 4.5 V

図 10-41. Line Transient Response



V_{OUT} = 3.3 V　　PFM　　T_A = 25°C
I_{OUT} = 0.3 A　　V_{IN} = 5.0 V　　BW = 20 MHz

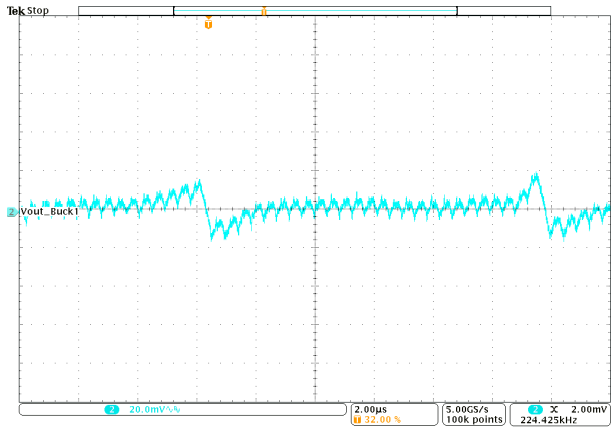
図 10-42. Output Voltage Ripple



V_{OUT} = 3.3 V　　PWM　　T_A = 25°C
I_{OUT} = 3 A　　V_{IN} = 5.0 V　　BW = 20 MHz

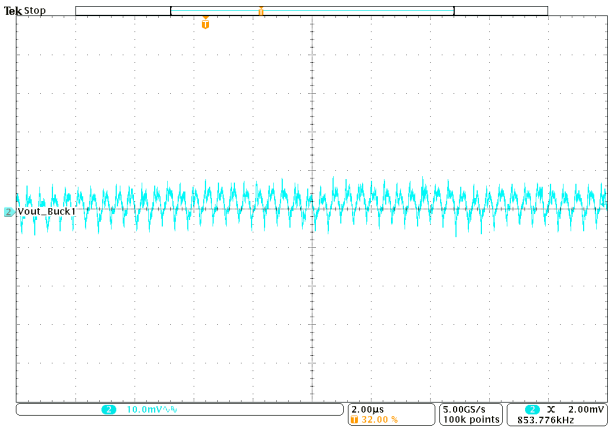
図 10-43. Output Voltage Ripple

10.2.3 Application Curves (continued)



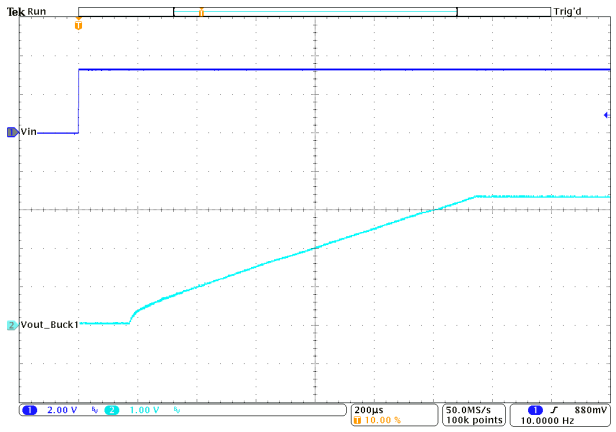
V_{OUT} = 1.8 V　PFM　T_A = 25°C
I_{OUT} = 0.3 A　V_{IN} = 5.0 V　BW = 20 MHz

図 10-44. Ouput Voltage Ripple



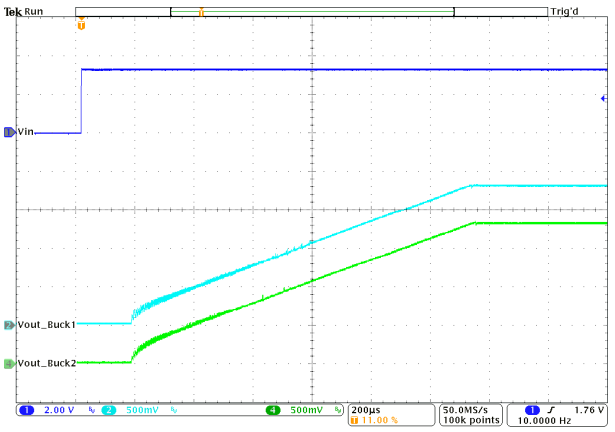
V_{OUT} = 1.8 V　PWM　T_A = 25°C
I_{OUT} = 3 A　V_{IN} = 5.0 V　BW = 20 MHz

図 10-45. Output Voltage Ripple



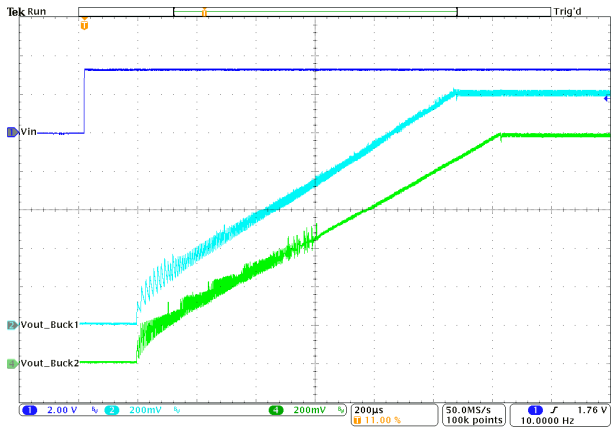
V_{OUT} = 3.3 V　PWM　T_A = 25°C
I_{OUT} = 3 A　V_{IN} = 5.0 V

図 10-46. Start-Up Timing



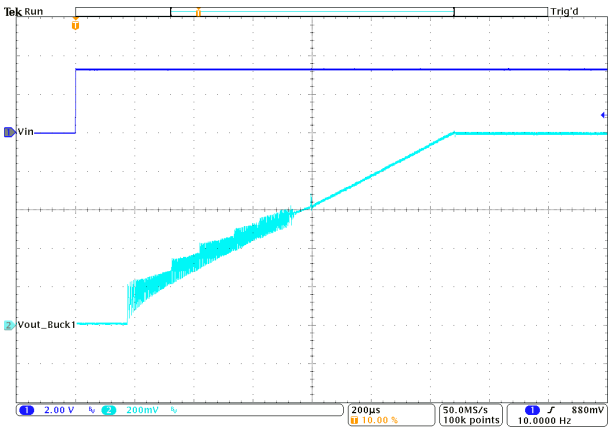
V_{OUT} = 1.8 V　PWM　T_A = 25°C
I_{OUT1} = 2 A　I_{OUT2} = 2 A　V_{IN} = 5.0 V

図 10-47. Start-Up Timing



V_{OUT} = 1.2 V　PWM　T_A = 25°C
I_{OUT1} = 1 A　I_{OUT2} = 3 A　V_{IN} = 5.0 V

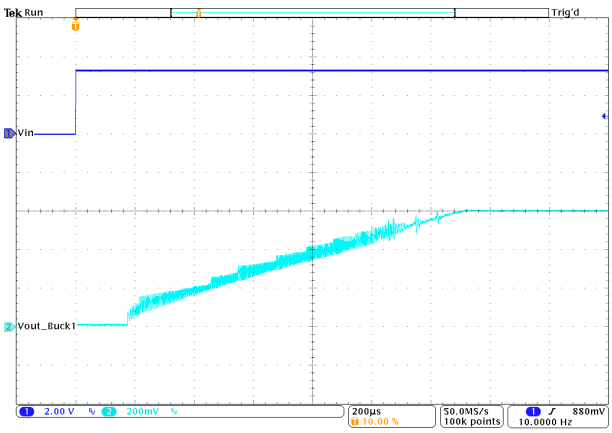
図 10-48. Start-Up Timing



V_{OUT} = 1.0 V　PWM　T_A = 25°C
I_{OUT1} = 3 A　V_{IN} = 5.0 V

図 10-49. Start-Up Timing

10.2.3 Application Curves (continued)



V_{OUT} = 0.6 V　　PWM　　T_A = 25°C
I_{OUT1} = 3 A　　V_{IN} = 5.0 V

図 10-50. Start-Up Timing

10.3 Power Supply Recommendations

The TPS6244x device family has no special requirements for its input power supply. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPS6244x.

10.4 Layout

10.4.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS6244x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like the following:

- Poor regulation (both line and load)
- Stability and accuracy weaknesses
- Increased EMI radiation
- Noise sensitivity

See 図 10-51 for the recommended layout of the TPS6244x, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces must be avoided. Loops which conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB must be connected with short wires and not nearby high dv/dt signals (for example SW). As they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The FB resistors, R_1, R_2 as well as R_3, R_4 must be kept close to the IC and connect directly to those pins and the system ground plane.

The package uses the pins for power dissipation. Thermal vias on the VIN, GND, and SW pins help to spread the heat into the PCB.

The recommended layout is implemented on the EVM and shown in the *TPS62442EVM-122 User's Guide*.

10.4.2 Layout Example

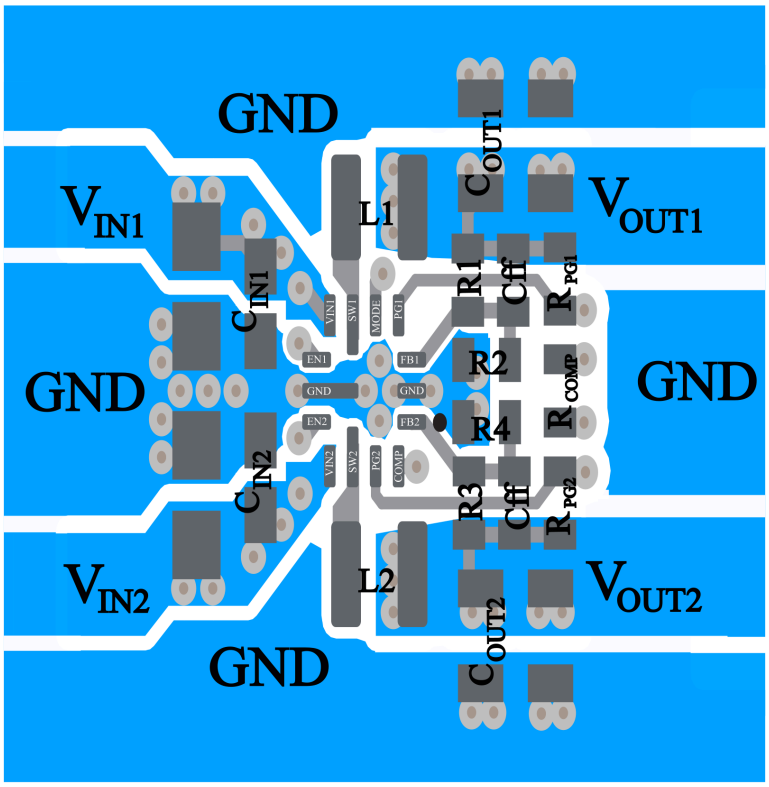


図 10-51. Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS62442EVM-122 User's Guide*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62441RQRR	Active	Production	VQFN-HR (RQR) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	62441
TPS62441RQRR.A	Active	Production	VQFN-HR (RQR) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	62441
TPS62442RQRR	Active	Production	VQFN-HR (RQR) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	441
TPS62442RQRR.A	Active	Production	VQFN-HR (RQR) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	441

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS62441, TPS62442 :

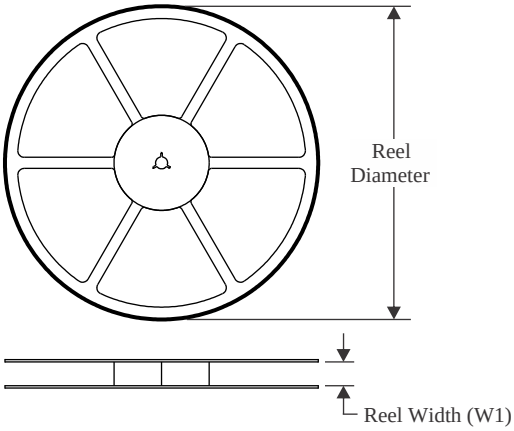
- Automotive : TPS62441-Q1, TPS62442-Q1

NOTE: Qualified Version Definitions:

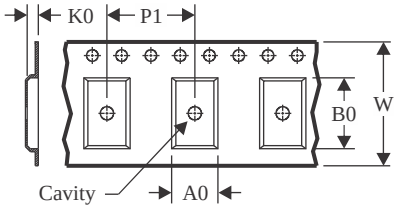
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

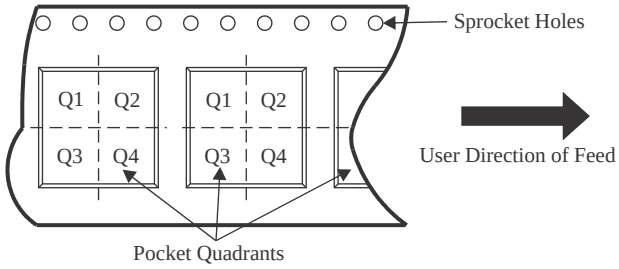


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

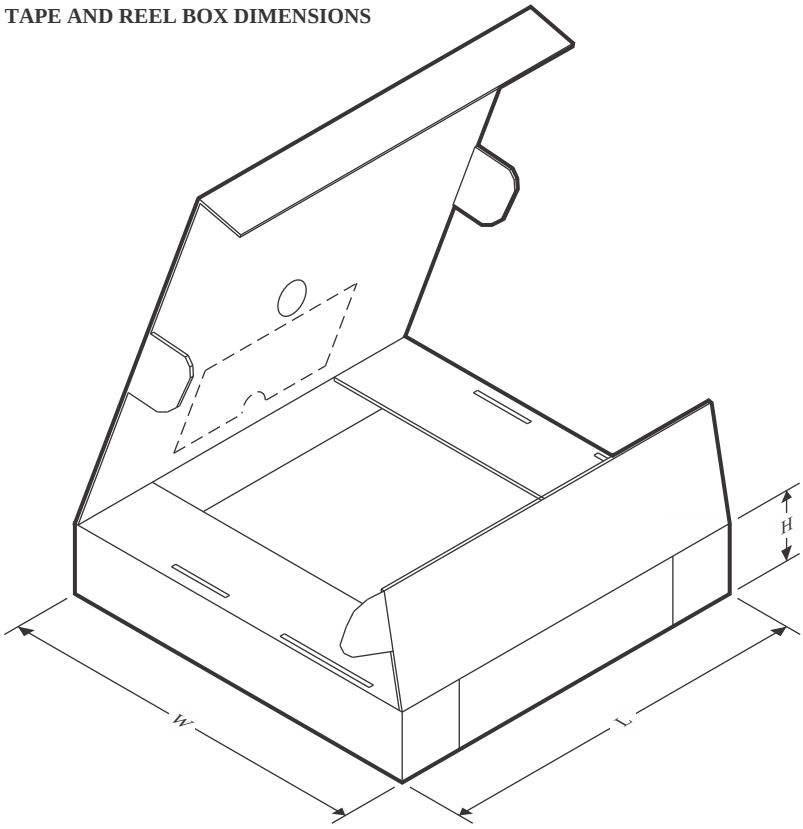
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62441RQRR	VQFN-HR	RQR	14	3000	180.0	8.4	2.6	3.0	1.2	4.0	8.0	Q1
TPS62442RQRR	VQFN-HR	RQR	14	3000	180.0	8.4	2.6	3.0	1.2	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62441RQRR	VQFN-HR	RQR	14	3000	210.0	185.0	35.0
TPS62442RQRR	VQFN-HR	RQR	14	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

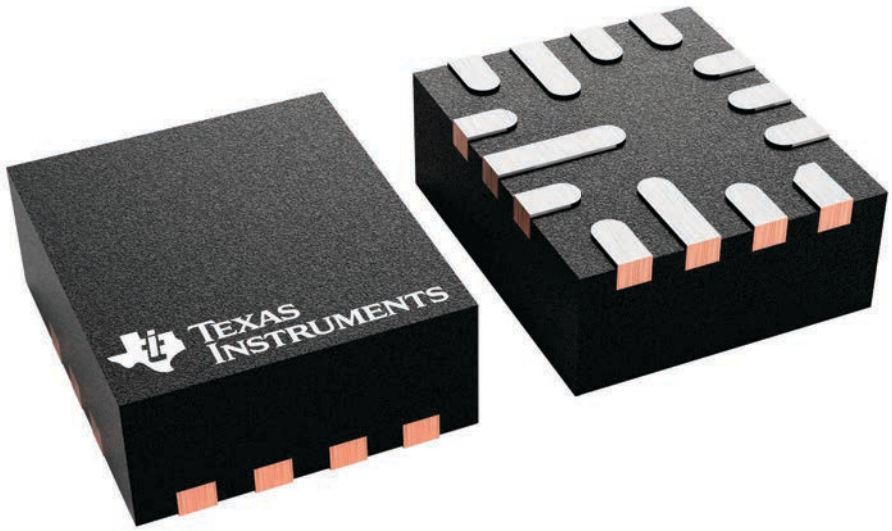
RQR 14

VQFN-HR - 1 mm max height

2.3 x 2.7, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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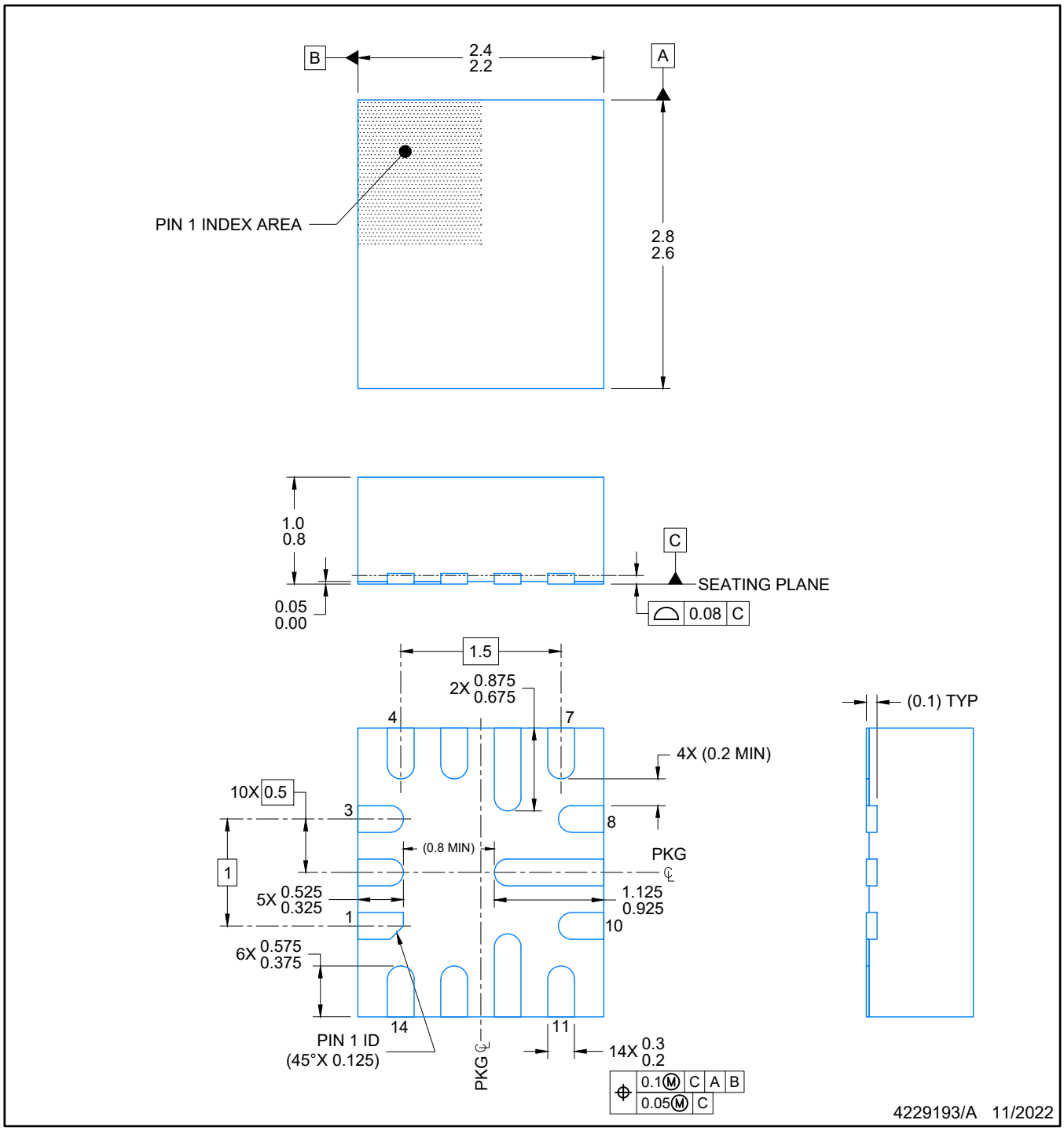
PACKAGE OUTLINE

RQR0014B

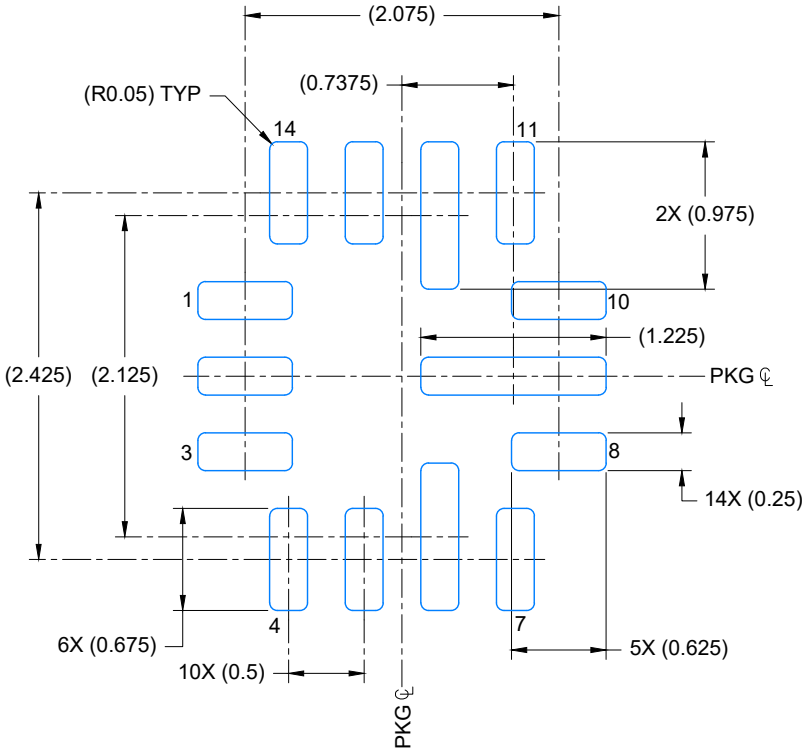
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

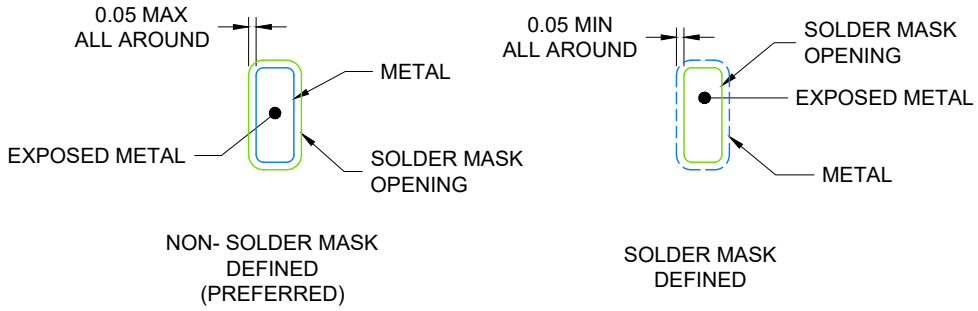


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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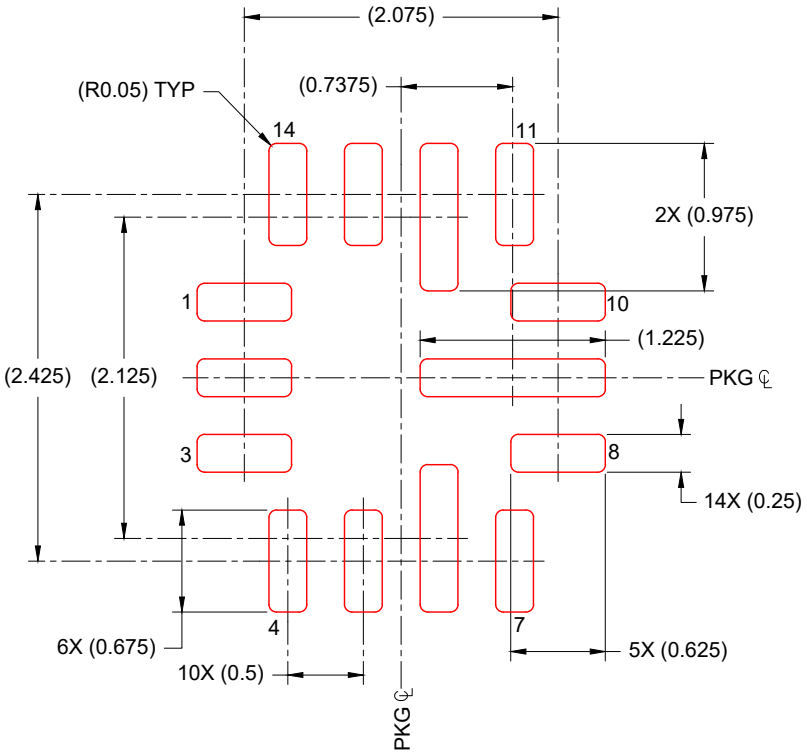
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 18X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月