17-V, 1.5-A, SYNCHRONOUS STEP-DOWN CONVERTER

Check for Samples: TPS62110-HT

FEATURES

- **High-Efficiency Synchronous Step-Down Converter With up to 95% Efficiency**
- **3.1-V to 17-V Operating Input Voltage Range**
- **Adjustable Output Voltage Range From 1.2 V to 16 V**
- **Synchronizable to External Clock Signal up to 1.4 MHz**
- **Up to 1.5-A Output Peak Current** (1)
- **32-µA Quiescent Current (Typ)**
- **High Efficiency Over a Wide Load Current Range Due to PFM/PWM Operation Mode**
- **100% Maximum Duty Cycle for Lowest Dropout**
- **Overtemperature and Overcurrent Protected**
- **Available in 16-Pin (PWP) QFP Package**

APPLICATIONS

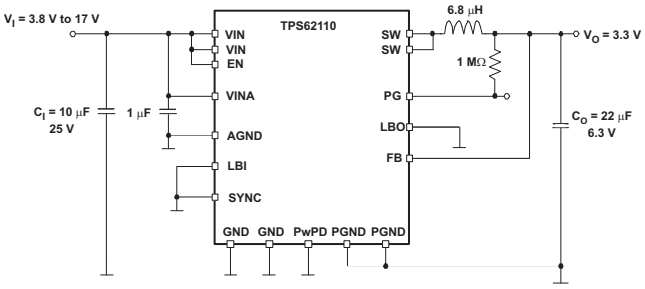
- **Down-Hole Drilling**
- **High Temperature Environments**

(1) Reduce life time may happen when 1.5-A limit is used for long time. Please refer to the EM calculations graph.

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/175°C) Temperature Range** (2)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

TYPICAL APPLICATION

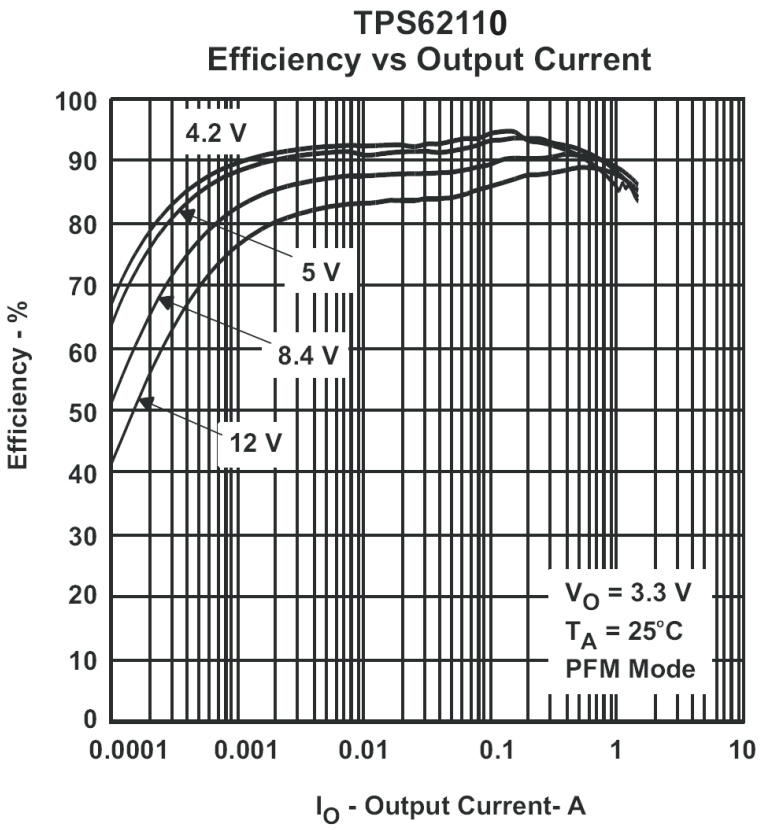


(2) Custom temperature ranges available

DESCRIPTION/ORDERING INFORMATION

The TPS62110 is a low-noise synchronous step-down dc-dc converter that is ideally suited for systems powered from a 2-cell Li-ion battery or from a 12-V or 15-V rail.

The TPS62110 is a synchronous PWM converter with integrated N-channel and P-channel power MOSFET switches. Synchronous rectification is used to increase efficiency and to reduce external component count. To achieve highest efficiency over a wide load current range, the converter enters a power-saving, pulse-frequency modulation (PFM) mode at light load currents. Operating frequency is typically 1 MHz, allowing the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 0.8 MHz to 1.4 MHz. For low noise operation, the converter can be operated in PWM-only mode. In the shutdown mode, the current consumption is reduced to less than 2 µA. The TPS62110 is available in the 16-pin (PWP) QFP package, and operates over a free-air temperature range of –55°C to 175°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 175°C	(PWP) QFP	TPS62110HPWP	TPS62110HPWP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
V_{CC}	Supply voltage at VIN, VINA	–0.3 V to 20 V
V_I	Voltage at SW	–0.3 V to V_I
	Voltage at EN, SYNC, LBO, PG	–0.3 V to 20 V
	Voltage at LBI, FB	–0.3 V to 7 V
I_O	Output current at SW	1500 mA
T_J	Maximum junction temperature	190°C
T_{stg}	Storage temperature	–65°C to 175°C
	Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds	300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS62110 PWP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	32.63	°C/W
ψ_{JT}	Junction-to-top characterization parameter(3)	0.848	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage at VIN, VINA	3.1	17	V
	Maximum voltage at power-good, LBO, EN, SYNC		17	V
	Continuous load current(1)		0.375	A
T_A	Operating temperature	–55	175	°C

(1) Higher values of continuous load current may affect long-term reliability of the device at higher operating temperatures. Please refer to Figure 1 and Figure 2.

ELECTRICAL CHARACTERISTICS

V_I = 12 V, V_O = 3.3 V, I_O = 600 mA, EN = V_I

PARAMETER		TEST CONDITIONS	T_A = -55°C to 125°C			T_A = 175°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SUPPLY CURRENT									
V_I	Input voltage range (1)		3.1		17	3.1		17	V
$I_{(Q)}$	Operating quiescent current	I_O = 0 mA, SYNC = GND, V_I = 7.2 V, T_A = 25°C (2)		20			32		µA
		I_O = 0 mA, SYNC = GND, V_I = 17 V (2)		23	30		35	70	
$I_{(SD)}$	Shutdown current	EN = GND, V_I = 12 V		1.5	5		9.5	45	µA
		EN = GND, V_I = 17 V		1.5	6		10.2	45	
ENABLE									
V_{IH}	EN high-level input voltage		1.3			1.3			V
V_{IL}	EN low-level input voltage				0.3			0.3	V
	EN trip-point hysteresis			170			170		mV
I_{IKG}	EN input leakage current	EN = GND or V_I, V_I = 17 V		0.07	0.2		0.07	0.2	µA
$I_{(EN)}$	EN input current	0.6 V ≤ $V_{(EN)}$ ≤ 4 V		10			5		µA
$V_{(UVLO)}$	Undervoltage lockout threshold	Input voltage falling	2.8	3	3.1	2.8	3	3.1	V
	Undervoltage lockout hysteresis			250			225		mV
POWER SWITCH									
$r_{DS(ON)}$	P-channel MOSFET on-resistance	V_I ≥ 5.4 V, I_O = 350 mA		165	250		165	325	mΩ
	P-channel MOSFET leakage current	V_{DS} = 17 V		0.1	1		2	7	µA
	P-channel MOSFET current limit	V_I = 7.2 V, V_O = 3.3 V		2400			2600		mA
$r_{DS(ON)}$	N-channel MOSFET on-resistance	V_I ≥ 5.4 V, I_O = 350 mA		145	200		185	270	mΩ
	N-channel MOSFET leakage current	V_{DS} = 17 V		0.1	3		2.1	18	µA
POWER GOOD OUTPUT, LBI, LBO									
$V_{(PG)}$	Power good trip voltage			V_O – 1.6%			V_O – 1.6%		V
	Power good delay time	V_O ramping positive		50			57		µs
		V_O ramping negative		190			200		
V_{OL}	PG, LBO output low voltage	$V_{(FB)}$ = 1.1 × V_O nominal, I_{OL} = 1 mA			0.3			0.3	V
I_{OL}	PG, LBO sink current			1			1		mA
	PG, LBO output leakage current	$V_{(FB)}$ = V_O nominal		0.01	0.25		0.01	0.25	µA
	Minimum supply voltage for valid power good, LBI, LBO signal			3			3		V
V_{LBI}	Low battery input trip voltage	Input voltage falling		1.256			1.260		V
ILBI	LBI input leakage current			10	100		10	100	nA
	Low battery input trip-point accuracy			1.5			1.5		%
$V_{LBI,HYS}$	Low battery input hysteresis			25			25		mV

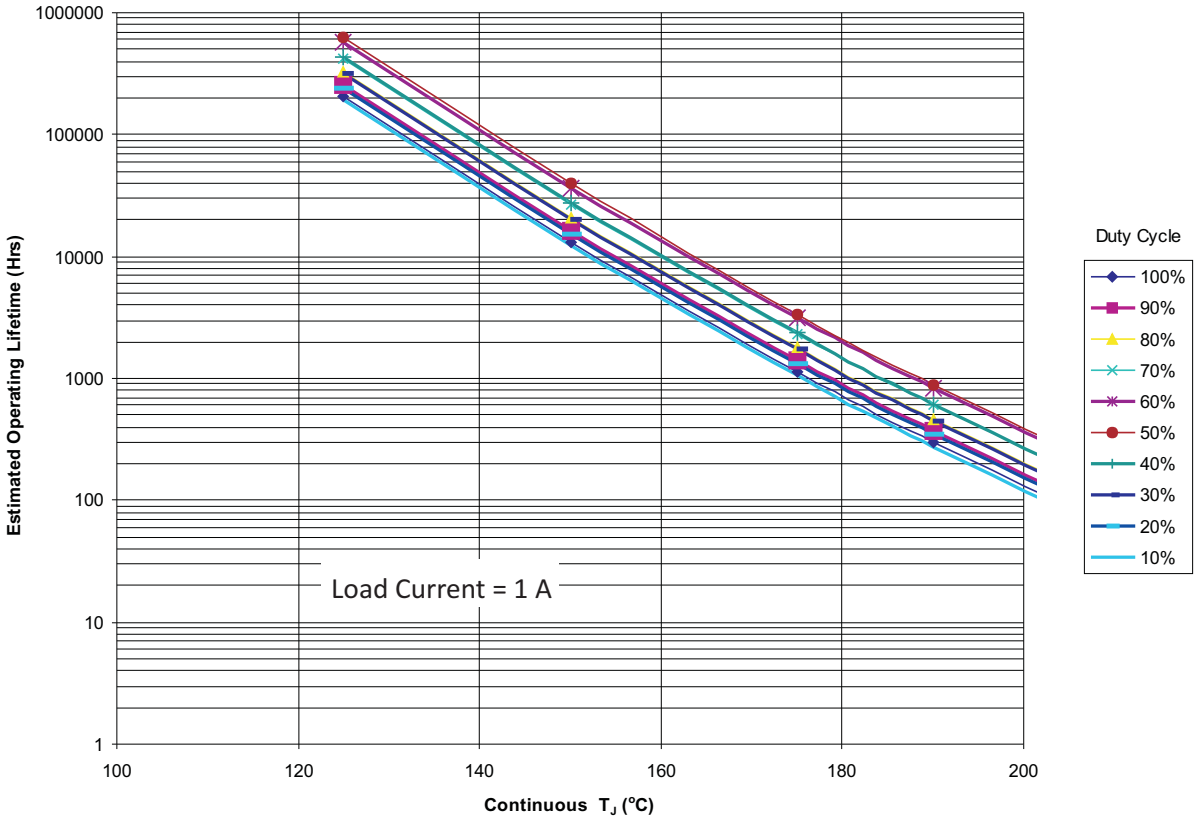
(1) Not production tested
(2) Device is not switching.

ELECTRICAL CHARACTERISTICS (continued)

V_I = 12 V, V_O = 3.3 V, I_O = 600 mA, EN = V_I

PARAMETER		TEST CONDITIONS	T_A = -55°C to 125°C			T_A = 175°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OSCILLATOR									
f_S	Oscillator frequency		900	1000	1100	900	1000	1100	kHz
$f_{(SYNC)}$	Synchronization range	CMOS-logic clock signal on SYNC pin	800		1410	800		1410	kHz
V_{IH}	SYNC high-level input voltage		1.5			1.5			V
V_{IL}	SYNC low-level input voltage				0.3			0.3	V
I_{lkg}	SYNC input leakage current	SYNC = GND or VIN		0.01	0.2		0.07	0.2	µA
	SYNC trip-point hysteresis			170			170		mV
	SYNC input current	0.6 V ≤ $V_{(SYNC)}$ ≤ 4 V		10	20		5	20	µA
	Duty cycle of external clock signal		30		90	30		90	%
OUTPUT									
V_O	Adjustable output voltage range		1.153		16	1.153		16	V
V_{FB}	Feedback voltage			1.153			1.153		V
	FB leakage current			10	100		290	2100	nA
	Feedback voltage tolerance (3)	V_I = 3.1 V to 17 V, 0 mA < I_O < 1500 mA (4)	–6		7.5	–7		8	%
I_O	Maximum output current	V_I ≥ 3 V (once undervoltage lockout voltage exceeded)		100			100		mA
		V_I ≥ 3.5 V		500			500		
		V_I ≥ 4.3 V		1200			1100		
		V_I ≥ 6 V		1500			1500		
	Current into internal voltage divider for fixed voltage versions			5			5		µA
η	Efficiency	V_I = 7.2 V, V_O = 3.3 V, I_O = 600 mA		92			82		%
		V_I = 12 V, V_O = 5 V, I_O = 600 mA		92			82		
	Duty cycle range for main switches (3)	at 1 MHz	10		100	10		100	%
	Minimum t_{on} time for main switch			100			100		ns
	Start-up time	I_O = 800 mA, V_I = 12 V, V_O = 3.3 V					1		ms

(3) Not production tested
(4) The maximum output current depends on the input voltage. See the *maximum output current* for further restrictions on the minimum input voltage.

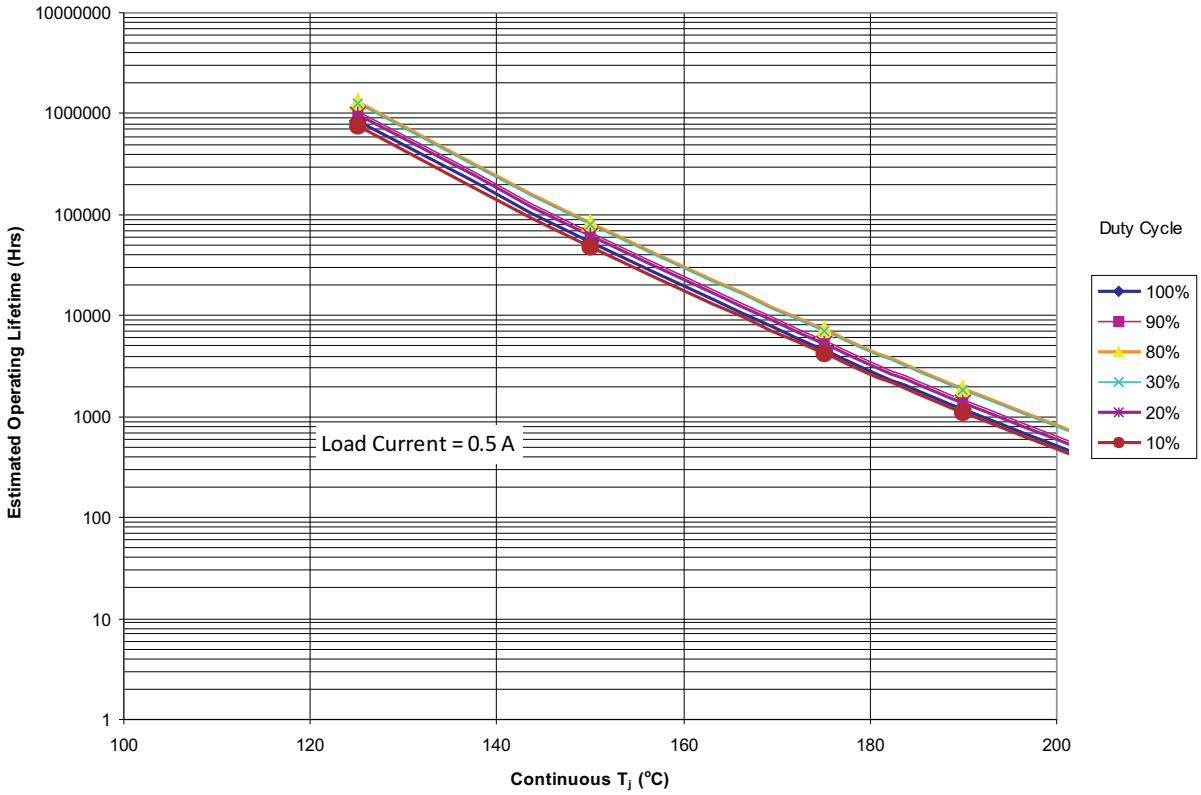


(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 1. TPS62110HPWP Operating Life Derating Chart (Load Current = 1 A)



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

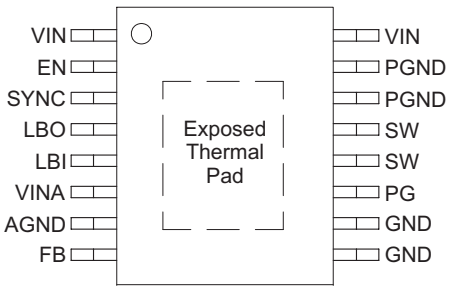
(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 2. TPS62110HPWP Operating Life Derating Chart (Load Current = 0.5 A)

DEVICE INFORMATION

PIN ASSIGNMENT TOP VIEW

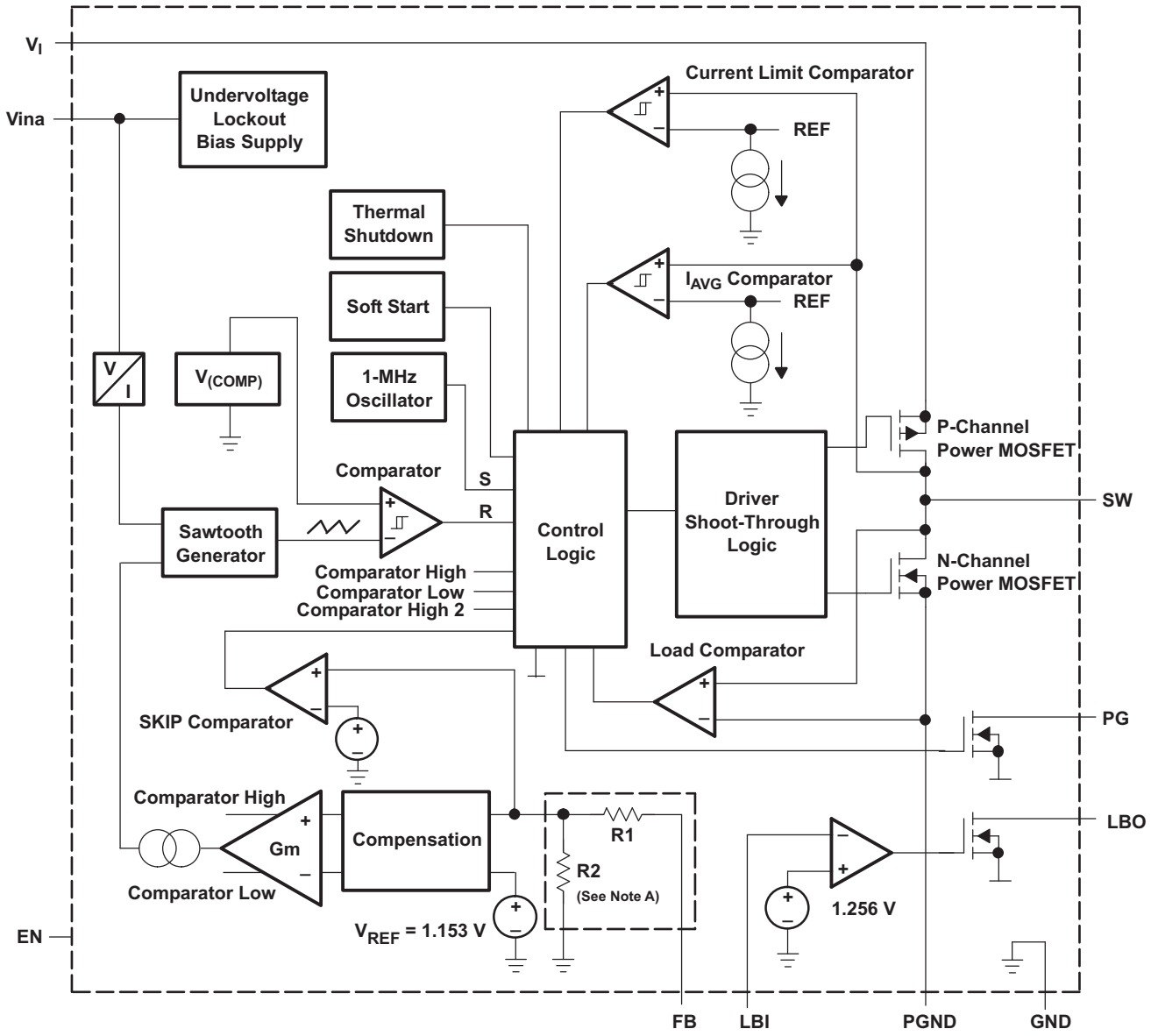
PWP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	Enable. A logic high enables the converter; logic low forces the device into shutdown mode reducing the supply current to less than 2 µA.
FB	8	I	Feedback pin for the fixed output voltage option. For the adjustable version, an external resistive divider is connected to this pin. The internal voltage divider is disabled for the adjustable version.
LBO	4	O	Open-drain, low-battery output. This pin is pulled low if LBI is below its threshold.
GND	9, 10	I	Ground
LBI	5	I	Low-battery input
SW	12, 13	O	Connect the inductor to this pin. This pin is the switch pin and connected to the drain of the internal power MOSFETS.
PG	11	O	Power good comparator output. This is an open-drain output. A pullup resistor should be connected between PG and VOUT. The output goes active high when the output voltage is greater than 98.4% of the nominal value.
PGND	14, 15	I	Power ground. Connect all power grounds to this pin.
AGND	7	I	Analog ground, connect to GND and PGND
SYNC	3	I	Input for synchronization to external clock signal. Synchronizes the converter switching frequency to an external clock signal with CMOS level: SYNC = HIGH: Low-noise mode enabled, fixed frequency PWM operation is forced SYNC = LOW (GND): Power save mode enabled, PFM/PWM mode enabled
VIN	1, 16	I	Supply voltage input (power stage)
VINA	6	I	Supply voltage input (support circuits)
PowerPAD™			Connect to AGND

FUNCTIONAL BLOCK DIAGRAM



A. For the adjustable version (TPS62110), the internal feedback divider is disabled and the FB pin is directly connected to the internal GM amplifier.

TYPICAL CHARACTERISTICS

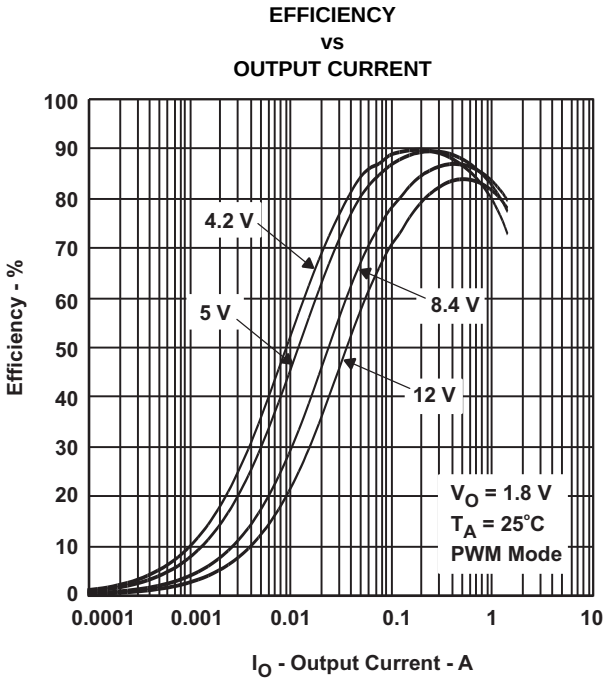


Figure 3.

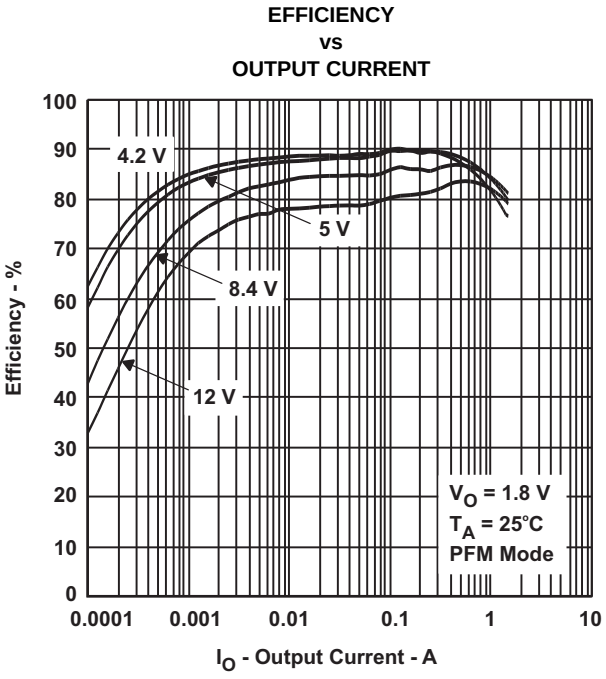


Figure 4.

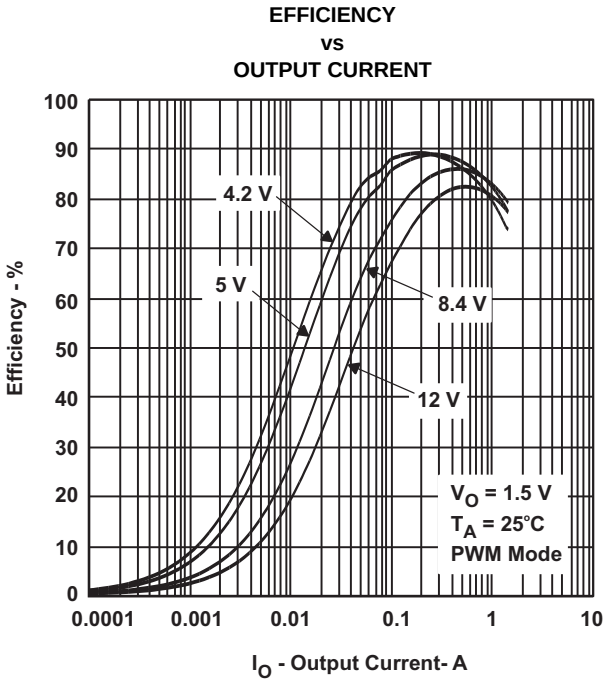


Figure 5.

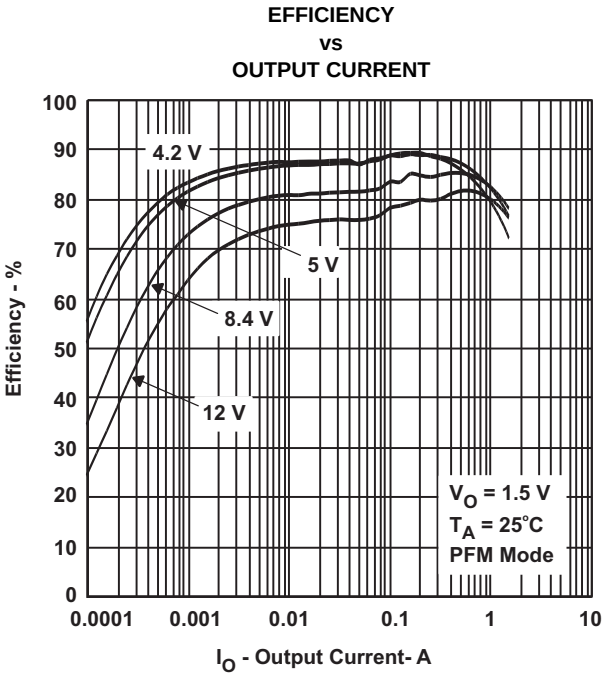


Figure 6.

TYPICAL CHARACTERISTICS (continued)

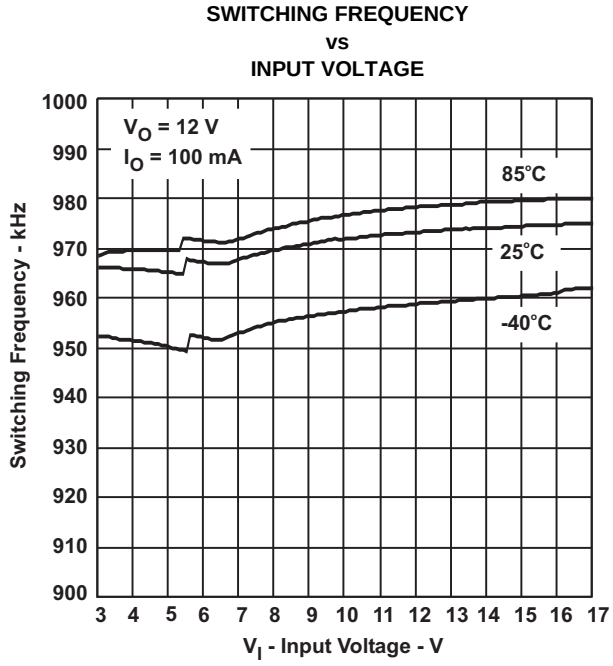


Figure 7.

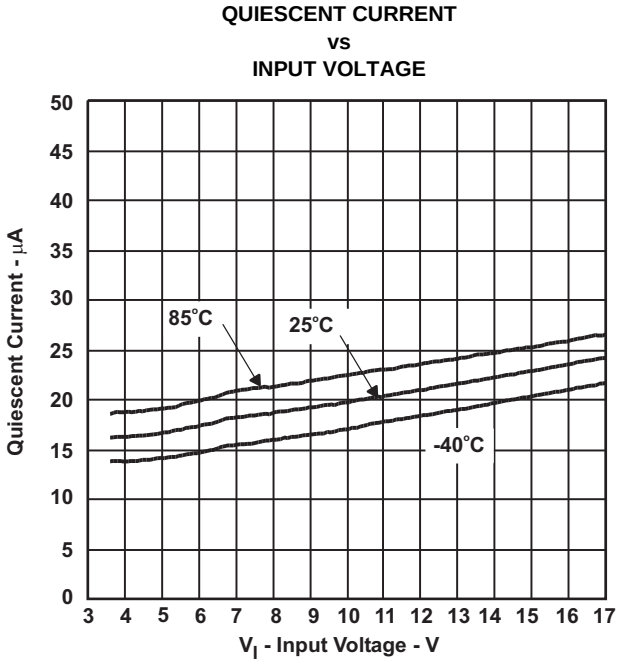


Figure 8.

The graphs were generated using the EVM with the setup according to Figure 9 unless otherwise noted. The output voltage divider was adjusted according to **Table 4** .

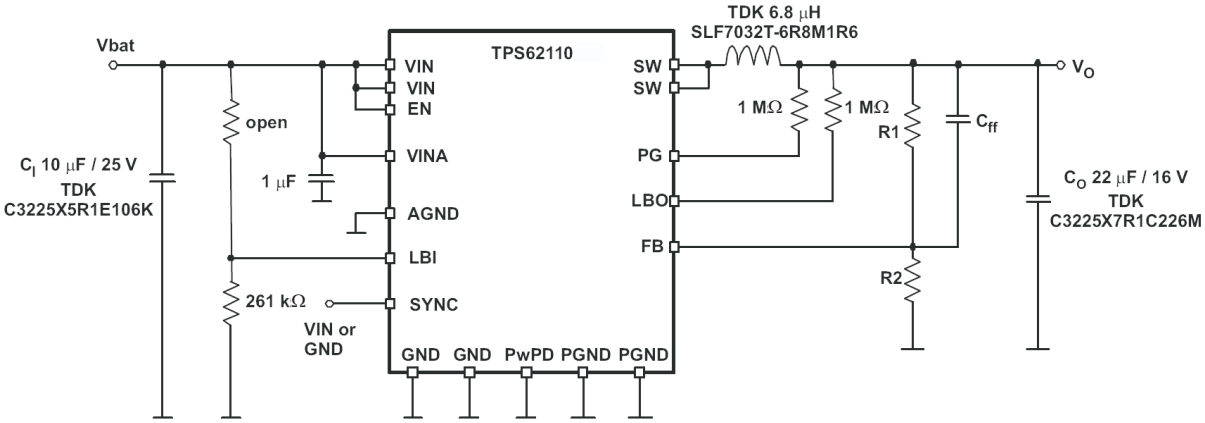


Figure 9. Test Setup

DETAILED DESCRIPTION

OPERATION

The TPS62110 is a synchronous step-down converter that operates with a 1-MHz fixed frequency pulse width modulation (PWM) at moderate-to-heavy load currents and enters the power save mode at light load current.

During PWM operation, the converter uses a unique fast response voltage mode control scheme with input voltage feedforward. Good line and load regulation is achieved with the use of small input and output ceramic capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns the switch off. The switch is turned off by the current limit comparator if the current limit of the P-channel switch is exceeded. After the dead time prevents current shoot through, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal turning off the N-channel rectifier, and turning on the P-channel switch.

The error amplifier as well as the input voltage determines the rise time of the sawtooth generator. Therefore, any change in input voltage or output voltage directly controls the duty cycle of the converter giving a very good line and load transient regulation.

CONSTANT FREQUENCY MODE OPERATION (SYNC = HIGH)

In constant frequency mode, the output voltage is regulated by varying the duty cycle of the PWM signal in the range of 100% to 10%. Connecting the SYNC pin to a voltage greater than 1.5 V forces the converter to operate permanently in the PWM mode even at light or no-load currents. The advantage is that the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads. The N-MOSFET of the devices stay on even when the current into the output drops to zero. This prevents the device from going into discontinuous mode, and the device transfers unused energy back to the input. Therefore, there is no ringing at the output, which usually occurs in discontinuous mode. The duty cycle range in constant frequency mode is 100% to 10%.

It is possible to switch from forced PWM mode to the power save mode during operation by pulling the SYNC pin LOW. The flexible configuration of the SYNC pin during operation of the device allows efficient power management by adjusting the operation of the TPS62110 to the specific system requirements.

POWER SAVE MODE OPERATION (SYNC = LOW)

As the load current decreases, the converter enters the power save mode operation. During power save mode, the converter operates with reduced switching frequency in pulse frequency modulation (PFM), and with a minimum quiescent current to maintain high efficiency. Whenever the average output current goes below the skip threshold, the converter enters the power save mode. The average current depends on the input voltage. It is about 200 mA at low input voltages and up to 400 mA with maximum input voltage. The average output current must be below the threshold for at least 32 clock cycles to enter the power save mode. During the power save mode, the output voltage is monitored with a comparator and the output voltage is regulated in to a typical value between the nominal output voltage and 0.8% above the nominal output voltage. When the output voltage falls below the nominal output voltage, the P-channel switch turns on. The P-channel switch is turned off as the peak switch current is reached. The N-channel rectifier is turned on, and the inductor current ramps down. As the inductor current approaches zero, the N-channel rectifier is turned off and the switch is turned on starting the next pulse. When the output voltage can not be reached with a single pulse, the device continues to switch with its normal operating frequency until the comparator detects the output voltage to be 0.8% above the nominal output voltage. This control method reduces the quiescent current to 20 µA (typical), and reduces the switching frequency to a minimum that achieves the highest converter efficiency.

DETAILED DESCRIPTION (continued)

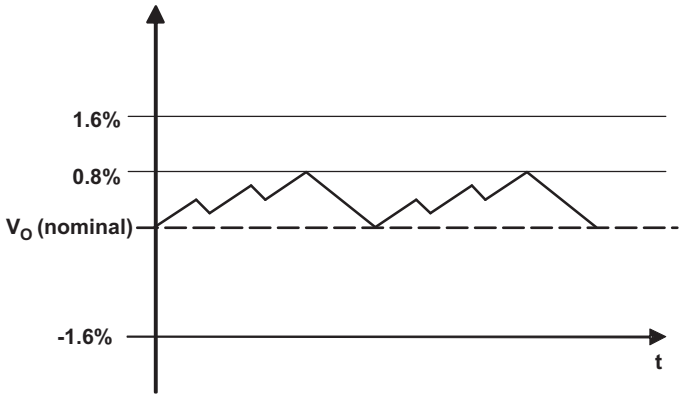


Figure 10. Power Save Mode Output Voltage Thresholds

The typical PFM (SKIP) current threshold for the TPS62110 is given by:

$$I_{SKIP} \approx \frac{V_I}{25\ \Omega} \quad (1)$$

Equation 1 is valid for input voltages up to 7 V. For higher voltages, the skip current threshold is not increased further. The converter enters the fixed frequency PWM mode as soon as the output voltage falls below V_O – 1.6% (nominal).

SOFT START

The TPS62110 has an internal soft-start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage when a battery or a high-impedance power source is connected to the input of the TPS62110.

The soft start is implemented as a digital circuit increasing the switch current in steps of 300 mA, 600 mA, 1200 mA. The typical switch current limit is 2.4 A. Therefore, the start-up time depends on the output capacitor and load current. Typical start-up time with a 22-µF output capacitor and 800-mA load current is 1 ms.

100% DUTY CYCLE LOW DROPOUT OPERATION

The TPS62110 offers the lowest possible input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve the longest operation time, taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, and is calculated as:

$$V_I\ \text{min} = V_O\ \text{max} + I_O\ \text{max} \cdot \left(r_{DS(on)}\ \text{max} + R_{(L)} \right) \quad (2)$$

with:

$I_O$max = maximum output current plus inductor ripple current
$r_{DS(on)}$max = maximum P-channel switch $r_{DS(on)}$
$R_{(L)}$ = dc resistance of the inductor
$V_O$max = nominal output voltage plus maximum output voltage tolerance

DETAILED DESCRIPTION (continued)

ENABLE

Logic low on EN forces the TPS62110 into shutdown. In shutdown, the power switch, drivers, voltage reference, oscillator, and all other functions are turned off. The supply current is reduced to less than 2 µA in the shutdown mode. When the device is in thermal shutdown, the bandgap is forced to be switched on even if the device is set into shutdown by pulling EN to GND.

If an output voltage is present when the device is disabled, which could be due to an external voltage source or a super capacitor, the reverse leakage current is specified under electrical characteristics. Pulling the enable pin high starts up the TPS62110 with the soft start. If the EN pin is connected to any voltage other than V_I or GND, an increased leakage current of typically 10 µA and up to 20 µA can occur.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low-input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The minimum input voltage to start up the TPS62110 is 3.4 V (worst case). The device shuts down at 2.8 V minimum.

SYNCHRONIZATION

If no clock signal is applied, the converter operates with a typical switching frequency of 1 MHz. It is possible to synchronize the converter to an external clock within a frequency range from 0.8 MHz to 1.4 MHz. The device automatically detects the rising edge of the first clock and synchronizes immediately to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation. The switch over is initiated if no rising edge on the SYNC pin is detected for a duration of four clock cycles. Therefore, the maximum delay time can be 6.25 µs if the internal clock has its minimum frequency of 800 kHz.

If the device is synchronized to an external clock, the power save mode is disabled, and the devices stay in forced PWM mode.

Connecting the SYNC pin to the GND pin enables the power save mode. The converter operates in the PWM mode at moderate-to-heavy loads, and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

POWER GOOD COMPARATOR

The power good (PG) comparator has an open-drain output capable of sinking 1 mA (typical). The PG is active only when the device is enabled (EN=high). When the device is disabled (EN=low), the PG pin is pulled to GND.

The PG output is valid only after a 250-µs delay when the device is enabled, and the supply voltage is greater than the undervoltage lockout $V_{(UVLO)}$. PG is low during the first 250 µs after shutdown and in shutdown.

The PG pin becomes active high when the output voltage exceeds 98.4% (typical) of its nominal value. Leave the PG pin unconnected when not used.

LOW-BATTERY DETECTOR

The low-battery output (LBO) is an open-drain type which goes low when the voltage at the low-battery input (LBI) falls below the trip point of 1.256 V ±1.5%. The voltage at which the low-battery warning is issued can be adjusted with a resistive divider as shown in Figure 11. The sum of resistors (R1 + R2) as well as the sum of (R5 + R6) is recommended to be in the 100 kΩ to 1 MΩ range for high efficiency at low output current. An external pullup resistor can be connected to OUT, or any other voltage rail in the voltage range of 0 V to 16 V. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground. The low-battery detector is disabled when the device is disabled.

The logic level of the LBO pin is not defined for the first 500 µs after EN is pulled high.

When the LBI is used to supervise the battery voltage and shut down the TPS62111 at low-input voltages, the battery voltage rises when the current drops to zero. The implemented hysteresis on the LBI pin may not be sufficient for all types of batteries. Figure 11 shows how an additional external hysteresis can be implemented.

DETAILED DESCRIPTION (continued)

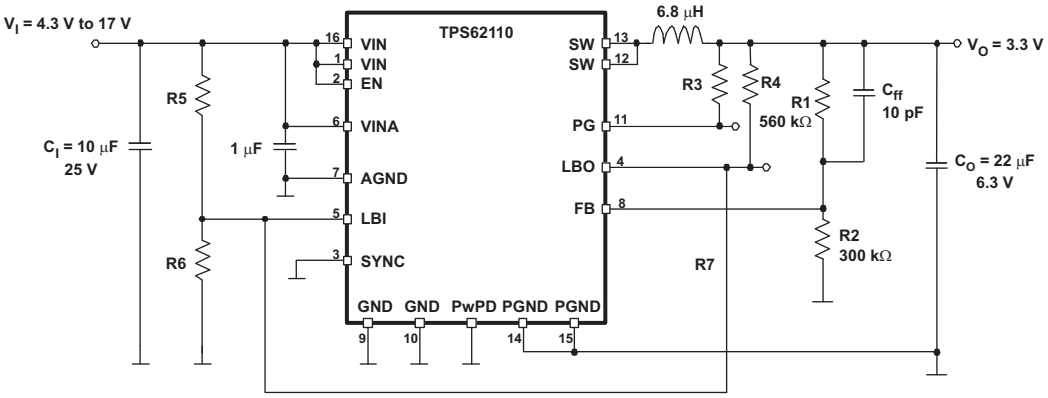


Figure 11. LBI With Increased Hysteresis

NO LOAD OPERATION

When the converter operates in the forced PWM mode and there is no load connected to the output, the converter regulates the output voltage by allowing the inductor current to reverse for a short time.

THEORY OR OPERATION / DESIGN PROCEDURE

Table 1. List of Inductors(1)(2)

MANUFACTURER (3)	TYPE	INDUCTANCE	DC RESISTANCE	SATURATION CURRENT
Coilcraft	MSS6132-682	6.8 µH	65 mR (max)	1.5 A
Epcos	B82462G4682M	6.8 µH	50 mR (max)	1.5 A
Sumida	CDRH5D28-6R2	6.2 µH	33 mR (typ)	1.8 A
TDK	SLF6028T-6R8M1R5	6.8 µH	35 mR (typ)	1.5 A
	SLF7032T-6R8M1R6	6.8 µH	41 mR (typ)	1.6 A
Wurth	7447789006	6.8 µH	44 mR (typ)	2.75 A
	7447779006	6.8 µH	33 mR (typ)	3.3 A
	744053006	6.2 µH	45 mR (typ)	1.8 A

(1) Component selections are for 25°C only and will change for new temperature range.
(2) Components have not been validated for extreme high temperature operation.
(3) The manufacturer's part numbers are used for test purposes only.

Inductor Selection

The control loop of the TPS62110 family requires a certain value for the output inductor and the output capacitor for stable operation. As long as the nominal value of L × C ≥ 6.2 µH × 22 µF, the control loop has enough phase margin and the device is stable. Reducing the inductor value without increasing the output capacitor (or vice versa) may cause stability problems. There are applications where it may be useful to increase the value of the output capacitor, e.g., for a low transient output voltage change. From a stability point of view, the inductor value could be decreased to keep the L × C product constant. However, there are drawbacks if the inductor value is decreased. A low inductor value causes a high inductor ripple current and therefore reduces the maximum dc output current. Table 2 gives the advantages and disadvantages when designing the inductor and output capacitor.

Table 2. Advantages and Disadvantages When Designing the Inductor and Output Capacitor

	INFLUENCE ON STABILITY	ADVANTAGE	DISADVANTAGE
Increase Cout (>22 µF)	Uncritical	Less output voltage ripple Less output voltage overshoot / undershoot during load transient	None
Decrease Cout (<22 µF)	Critical Increase inductor value >6.8 µH also	None	Higher output voltage ripple High output voltage overshoot / undershoot during load transient Less gain and phase margin
Increase L (>6.8 µH)	Uncritical	Less inductor current ripple Higher dc output current possible if operated close to the current limit	More energy stored in the inductor → higher voltage overshoot during load transient Smaller current rise → higher voltage undershoot during load transient → do not decrease the value of Cout due to these effects
Decrease L (<6.8 µH)	Critical Increase output capacitor value > 22 µF also	Small voltage overshoot / undershoot during load transient	High inductor current ripple especially at high input voltage and low output voltage

As it is shown in Table 2, the inductor value can be increased to higher values. For good performance, the peak-to-peak inductor current ripple should be less than 30% of the maximum dc output current. Especially at input voltages above 12 V, it makes sense to increase the inductor value to keep the inductor current ripple low. In such applications, the inductor value can be increased to 10 µH or 22 µH. Values above 22 µH should be avoided to keep the voltage overshoot during load transient in an acceptable range.

After choosing the inductor value, two additional inductor parameters should be considered:

1. current rating of the inductor
2. dc resistance

The dc resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency. To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus the inductor ripple current which is calculated as:

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_L\,max = I_O\,max + \frac{\Delta I_L}{2} \tag{3}$$

Where:

f = Switching frequency (1000 kHz typical)

L = Inductor value

ΔI_L = Peak-to-peak inductor ripple current

I_L(max) = Maximum inductor current

The highest inductor current occurs at maximum V_I. A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS62110, which is 2.4 A (typically). See Table 1 for recommended inductors.

OUTPUT CAPACITOR SELECTION

A 22-µF (typical) output capacitor is needed with a 6.8 µH inductor. For an output voltage greater than 5 V, a 33-µF (minimum) output capacitor is required for stability. For best performance, a low ESR ceramic output capacitor is needed.

The RMS ripple current is calculated as:

$$I_{RMS}(C_O) = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charge and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + R_{ESR} \right) \quad (5)$$

Where the highest output voltage ripple occurs at the highest input voltage V_I.

INPUT CAPACITOR SELECTION

The nature of the buck converter is a pulsating input current; therefore, a low ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. The input capacitor should have a minimum value of 10 µF and can be increased without any limit for better input voltage filtering. The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = I_O \text{ max} \times \sqrt{\frac{V_O}{V_I} \times \left(1 - \frac{V_O}{V_I}\right)} \quad (6)$$

The worst-case RMS ripple current occurs at D = 0.5 and is calculated as: $I_{RMS} = I_O/2$. Ceramic capacitors show a good performance because of their low ESR value, and they are less sensitive against voltage transients compared to tantalum capacitors. Place the input capacitor as close as possible to the input pin of the IC for best performance

FEEDFORWARD CAPACITOR SELECTION

The feedforward capacitor (C_{ff}) is needed to compensate for parasitic capacitance from the feedback pin to GND. Typically, a value of 4.7 pF to 22 pF is needed for an output voltage divider with a equivalent resistance (R1 in parallel with R2) in the 150 kΩ range. The value can be chosen based on best transient performance and lowest output voltage ripple in PFM mode.

RECOMMENDED CAPACITORS

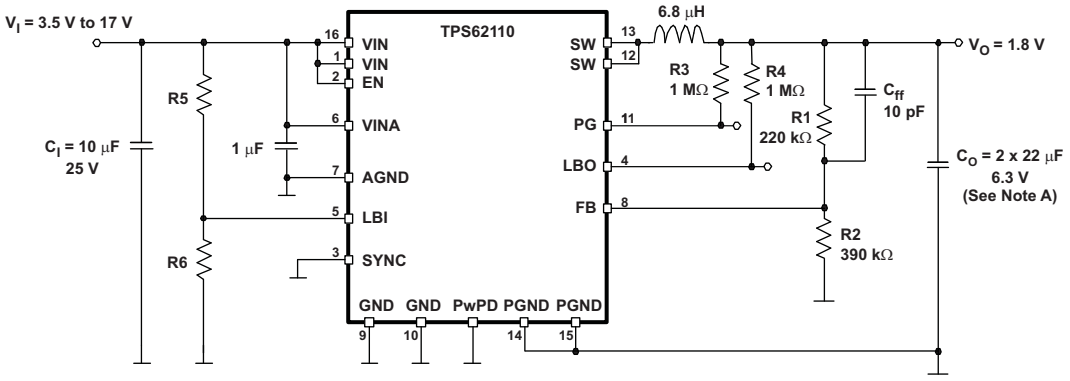
It is recommended that only X5R or X7R ceramic capacitors be used as input/output capacitors. Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output and input capacitor of a dc/dc converter. The effect may lead to a significant capacitance drop especially for high input/output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value to get the required value at the operating point. The capacitors listed in Table 3 have been tested with the TPS62110 with good performance.

Table 3. List of Capacitors(1)(2)

MANUFACTURER	PART NUMBER	SIZE	VOLTAGE	CAPACITANCE	TYPE
Taiyo Yuden	TMK316BJ106KL	1206	25 V	10 µF	Ceramic
	EMK325BJ226KM	1210	16 V	22 µF	
TDK	C3225X5R1E106M	1210	25 V	10 µF	Ceramic
	C3225X7R1C226M		16 V	22 µF	
	C3216X5R1E106MT	1206	25 V	10 µF	

(1) Component selections are for 25°C only and will change for new temperature range.
(2) Components have not been validated for extreme high temperature operation.

APPLICATION INFORMATION



A. For an output voltage lower than 2.5 V, an output capacitor of 33 µF or greater is recommended to improve load transient.

Figure 12. Standard Connection for Adjustable Version

$$V_O = V_{FB} \times \frac{R1 + R2}{R2} \qquad R1 = R2 \times \left(\frac{V_O}{V_{FB}} \right) - R2 \tag{7}$$

V_{FB} = 1.153 V

Table 4. Recommended Resistors(1)(2)

OUTPUT VOLTAGE	R1	R2	NOMINAL VOLTAGE	TYPICAL C_{ff}
9 V	680 kΩ	100 kΩ	8.993 V	22 pF
5 V	510 kΩ	150 kΩ	5.073 V	10 pF
3.3 V	560 kΩ	300 kΩ	3.305 V	10 pF
2.5 V	390 kΩ	330 kΩ	2.515 V	10 pF
1.8 V	220 kΩ	390 kΩ	1.803 V	10 pF
1.5 V	100 kΩ	330 kΩ	1.502 V	10 pF

(1) Component selections are for 25°C only and will change for new temperature range..
(2) Components have not been validated for extreme high temperature operation.

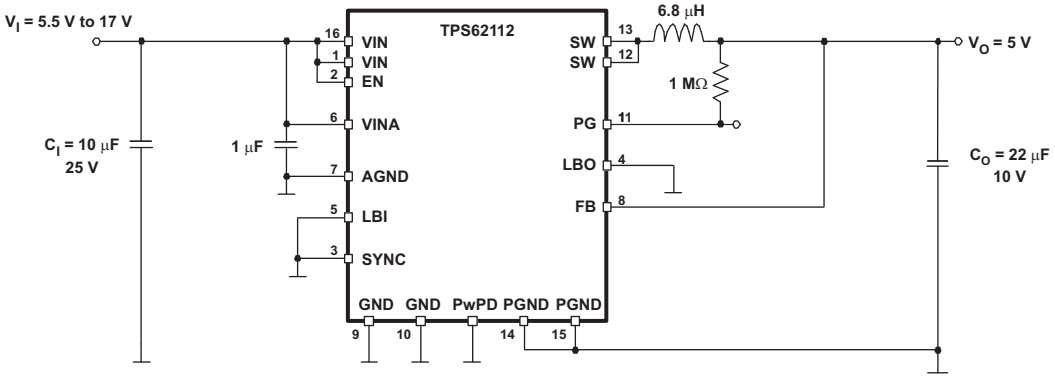
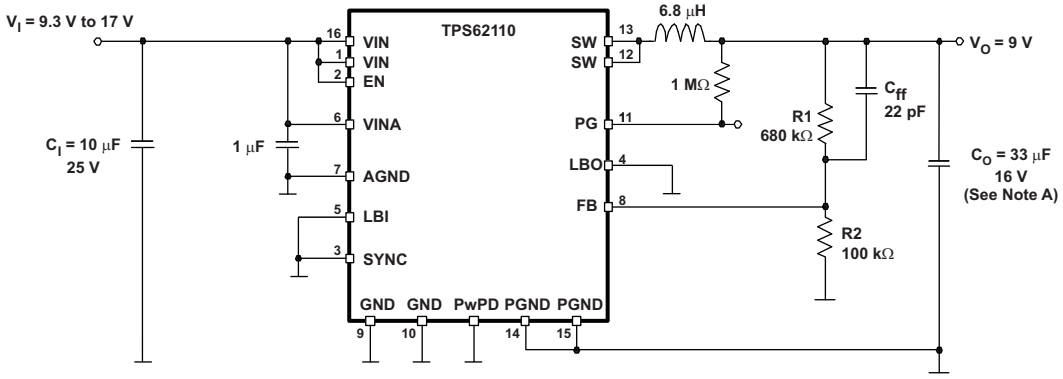


Figure 13. Standard Connection for Fixed Voltage Version



A. For an output voltage greater than 5 V, an output capacitor of 33 µF minimum is required for stability.

Figure 14. Application With 9 V Output

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62110HPWP	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 175	S62110H
TPS62110HPWPG4	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 175	S62110H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS62110-HT :

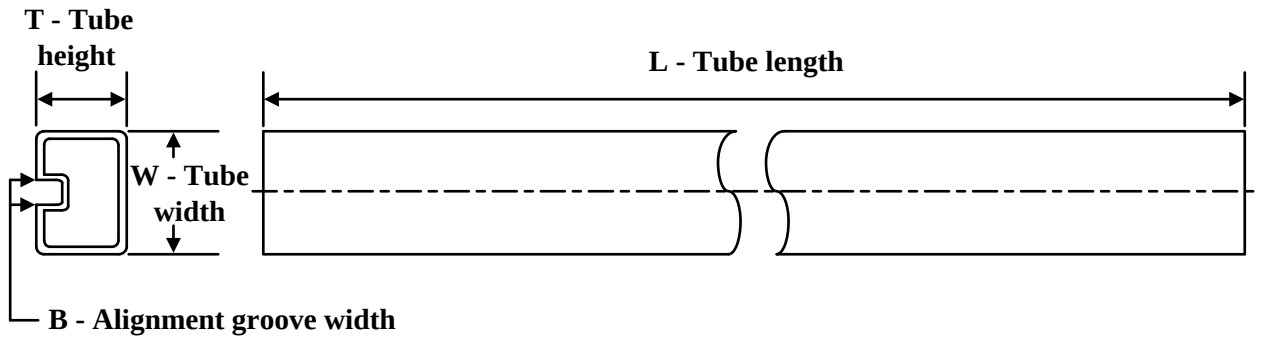
- Catalog : TPS62110

- Automotive : TPS62110-Q1
- Enhanced Product : TPS62110-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TUBE

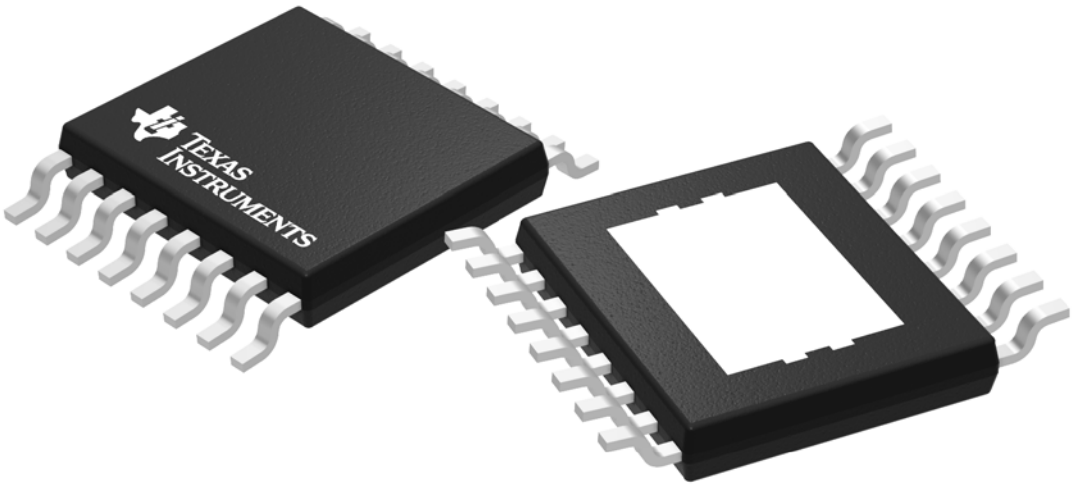


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS62110HPWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS62110HPWPG4	PWP	HTSSOP	16	90	530	10.2	3600	3.5

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

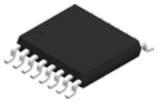
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

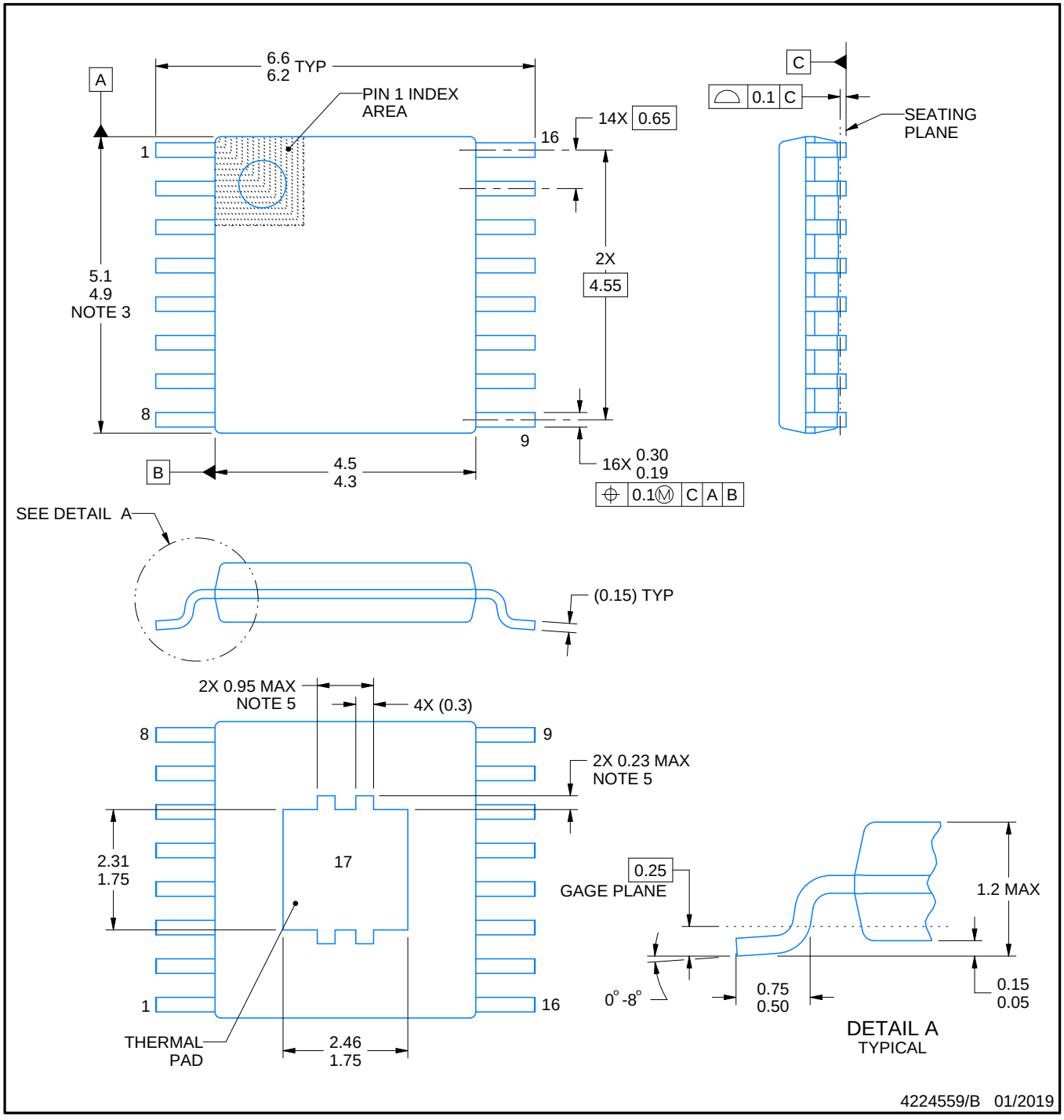
PACKAGE OUTLINE

PWP0016C



PowerPAD™ TSSOP - 1.2 mm max height

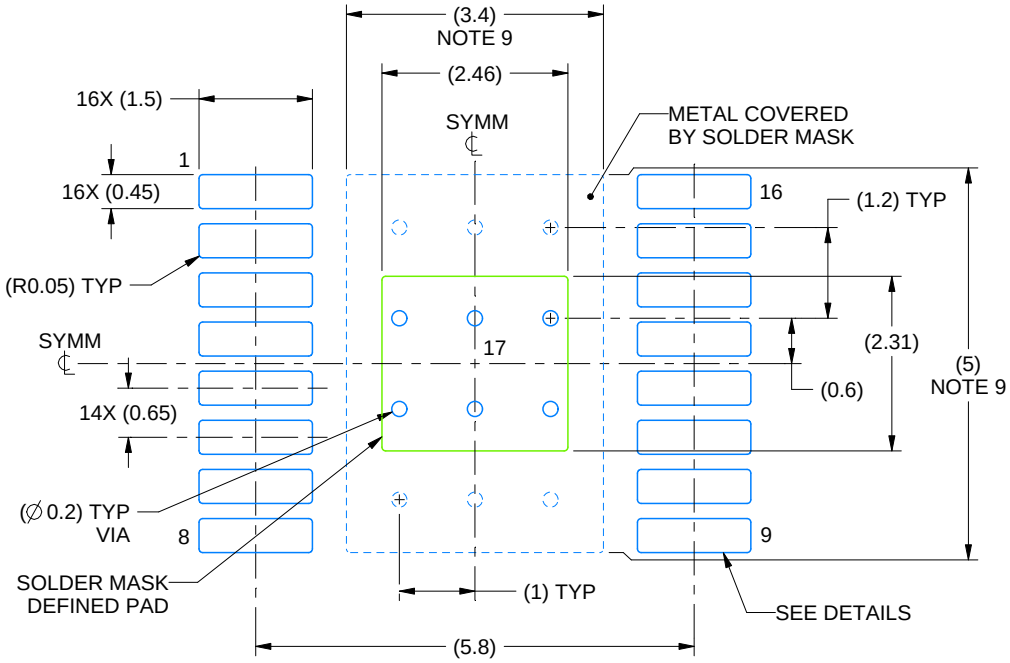
SMALL OUTLINE PACKAGE



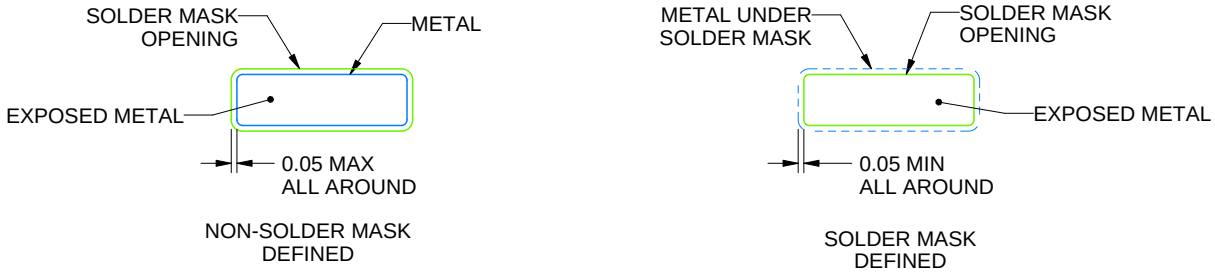
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

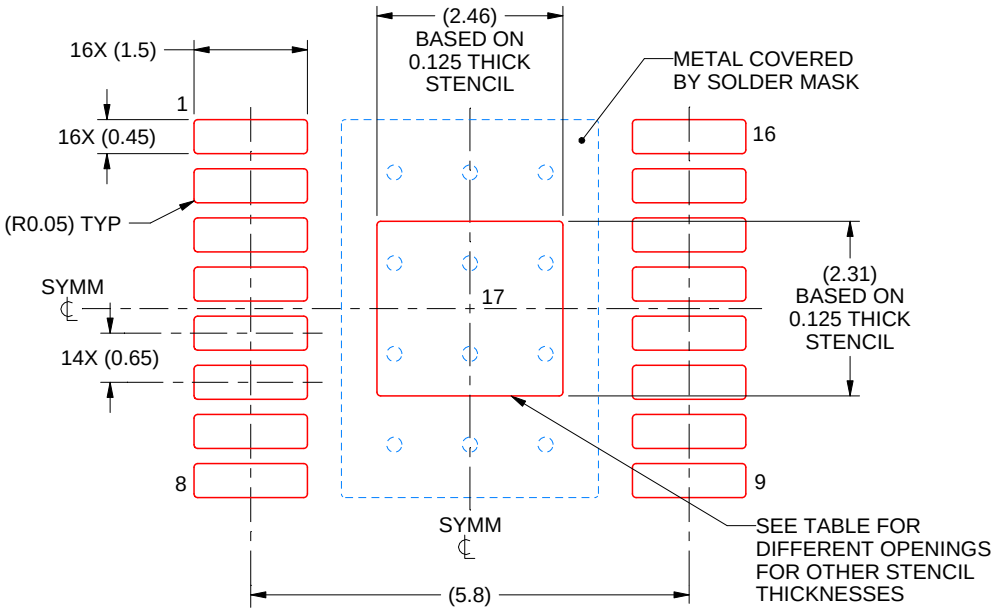


SOLDER MASK DETAILS

4224559/B 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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