TPS61372 負荷切断機能搭載、16V、3.8A、同期整流昇圧

1 特長

- 入力電圧範囲:2.5V～5.5V
- 出力電圧範囲:16V (最大値)
- オン抵抗
  - ローサイド FET - 33mΩ
  - ハイサイド FET - 104mΩ
- スイッチ・ピーク電流制限:3.8A
- V_{IN} からの静止電流:74μA
- V_{OUT} からの静止電流:10μA
- V_{IN} からのシャットダウン電流:1μA
- スイッチング周波数:1.5MHz
- ソフト・スタート時間:0.9ms
- ヒカップ出力短絡保護
- 自動 PFM と強制 PWM を選択可能
- シャットダウン中の負荷切断
- 外部ループ補償
- 出力過電圧保護
- 1.57mm × 1.52mm × 0.5mm、16 ピンの WCSP
- WEBENCH® Power Designer により、TPS61372 を使用するカスタム設計を作成

2 アプリケーション

- RF PA ドライバ
- NAND フラッシュ
- バックアップ電源
- モーター・ドライバ
- 光センサ・ドライバ

3 概要

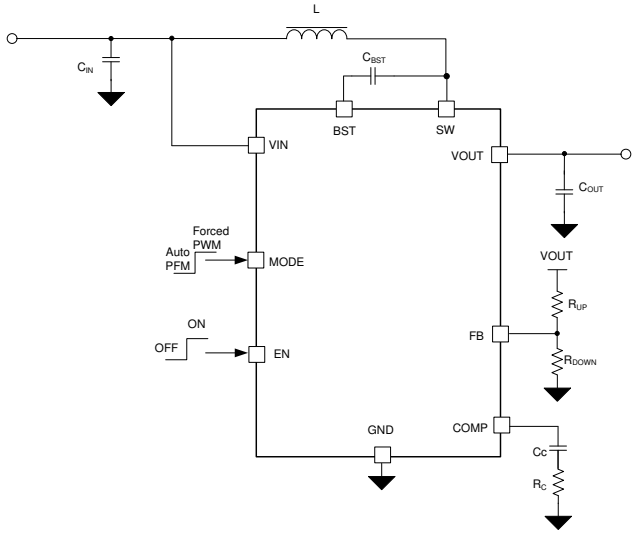
TPS61372 は、負荷を切り離す機能を備えた完全統合型同期整流昇圧コンバータです。本デバイスは最大 16V の出力電圧と 3.8A の電流制限に対応しています。入力電圧範囲は 2.5V～5.5V で、シングルセルのリチウムイオン・バッテリ、または 5V バスから給電されるアプリケーションをサポートします。

TPS61372 は、適応型オフ時間制御トポロジで、ピーク電流モードを使用します。このデバイスは、中負荷から重負荷では 1.5MHz の PWM で動作します。軽負荷の状況では、デバイスが自動的に PFM に切り替わるか、強制的に PWM で動作するかを、MODE ピン接続で構成できます。自動 PFM モードは軽負荷時の効率が高いのが利点で、これに対して強制 PWM 動作では、負荷範囲全体でスイッチング周波数が一定に保たれます。TPS61372 はソフトスタートを使用して、スタートアップ時の突入電流を最小化します。TPS61372 はシャットダウン時に負荷が切断され、ヒカップ・モードの出力短絡保護機能があります。さらに、デバイスには出力過電圧およびサーマル・シャットダウン保護機能も実装されています。TPS61372 は、1.57mm × 1.52mm、高さが 0.5mm の 16 ピン WCSP パッケージで供給されるので、小型のソリューションを実現できます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS61372	DSBGA (16)	1.57mm × 1.52mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2018) to Revision B (January 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Changed 2 to S in 式 11	17
• Updated *セクション 8.2.2.7*	19

Changes from Revision * (June 2018) to Revision A (October 2018)	Page
• 量産データのデータシートの初版	1

5 Pin Configuration and Functions

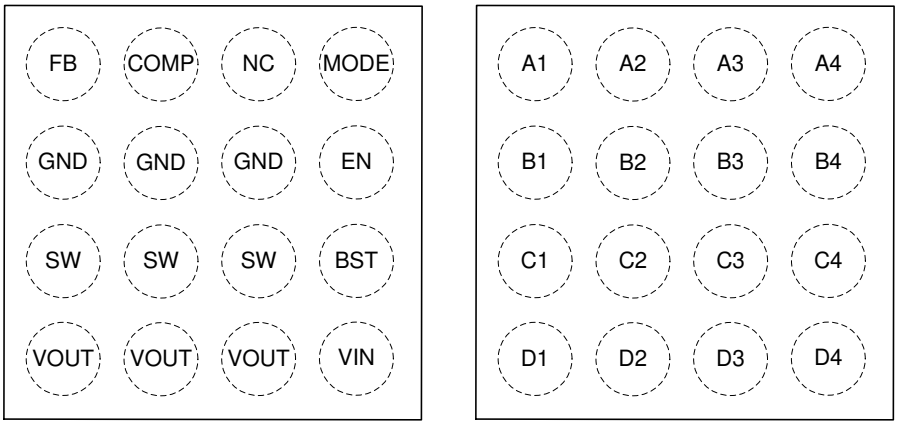


図 5-1. YKB Package 16-Pin DSBGA (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
A1	FB	I	Output voltage feedback. A resistor divider connecting to this pin sets the output voltage.
A2	COMP	O	Output of the internal error amplifier. The loop compensation network must be connected between this pin and GND.
A3	NC	I	No connection. Tie directly to VIN pin. Do not connect with GND or leave it floating.
A4	MODE	I	Operation mode selection pin. MODE = low, the device works in auto PFM mode with good light load efficiency. MODE = high, the device is in forced PWM mode and keeps the switching frequency constant across the whole load range.
B1, B2, B3	GND	-	Ground
B4	EN	I	Enable logic input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode.
C1, C2, C3	SW	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side FET and the source of the internal high-side FET.
C4	BST	O	Power supply for the high-side FET gate driver. A capacitor must be connected between this pin and the SW pin.
D1, D2, D3	VOUT	PWR	Boost converter output
D4	VIN	I	IC power supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals(2)	BST	–0.3	SW+6	V
Voltage range at terminals(2)	SW, VOUT	-0.3	19	V
Voltage range at terminals(2)	VIN, EN, COMP, FB, MODE, NC	–0.3	6	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

Over operating free-air temperature range unless otherwise noted.

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		5.5	V
V_{OUT}	Output voltage	5		16	V
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS61372 YKB 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

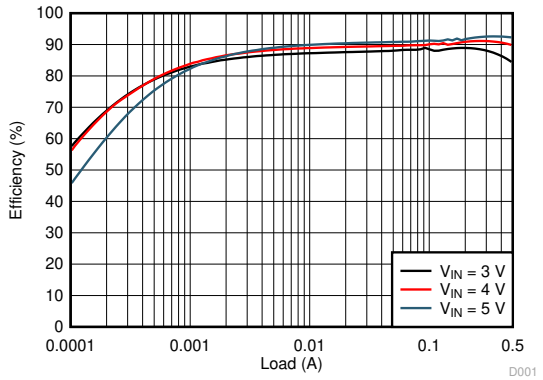
V_{IN} = 2.5 V to 5.5 V and V_{OUT} = 5 V to 16 V, T_J = - 40°C to 125°C , Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN_UVLO}	Input voltage under voltage lockout (UVLO) threshold, rising	V_{OUT} = 12 V, T_J = - 40°C to 125°C			2.32	V
	Input voltage under voltage lockout (UVLO) threshold, falling				2.1	V
I_Q	Quiescent current into VIN pin	IC enabled, no switching T_J = – 40°C to 85°C		74	110	µA
I_Q	Quiescent current into VOUT pin	IC enabled, no switching, V_{IN} = 2.5 V, V_{OUT} = 5 V to 16 V, T_J = – 40°C to 85°C		10	26	µA
I_{SD}	Shutdown current from VIN to GND	V_{IN} = 2.5 V to 5.5 V, V_{OUT} = SW = 0 V, EN = 0, T_J = - 40°C to 85°C		0.03	1	µA
OUTPUT VOLTAGE						
V_{REF}	Reference voltage on FB pin		0.585	0.594	0.603	V
	AUTO PFM mode	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		1.016		V_{REF}
I_{FB_LKG}	Leakage current into FB pin				30	nA
POWER SWITCHES						
$R_{DS(on)}$	Low-side FET on resistance	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		33		mΩ
	High-side + Dis connect FET on resistance	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		104		mΩ
CURRENT LIMIT						
I_{LIM}	Current Limit (Auto PFM)	V_{IN} = 3 V to 4.5 V, V_{OUT} = 5 V to 16 V, T_J = - 40°C to 125°C	3.4	3.8	4.3	A
	Current Limit (Forced PWM)	V_{IN} = 3 V to 4.5 V, V_{OUT} = 5 V to 16 V, T_J = - 40°C to 125°C	3.28	3.6	4.0	A
EN, MODE LOGICS						
V_{IH}	EN, MODE pin high level input voltage				1.2	V
V_{IL}	EN, MODE pin low level input voltage		0.4			V
V_{HYS}	EN, MODE pin Hysteresis			100		mV
$T_{DEGLITCH}$	EN, MODE deglitch time rising / falling	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		13		µS
R_{PD}	EN, MODE pull down resistor	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		800		kΩ
SWITCHING CHARACTER						

V_{IN} = 2.5 V to 5.5 V and V_{OUT} = 5 V to 16 V, T_J = - 40°C to 125°C , Typical values are at T_J = 25°C, unless otherwise noted.

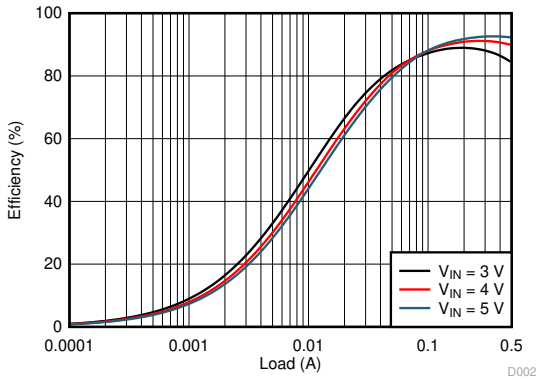
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{SW}	Switch frequency	V_{IN} = 3 V to 4.5 V, V_{OUT} = 5 V to 12 V, T_J = - 40°C to 125°C	1.2		1.7	MHz
f_{SW_FOLD}	Switch frequency foldback	V_{IN} = 4 V, T_J = - 40°C to 125°C	470	535	600	kHz
V_{FSW_LOW}	Threshold for fsw foldback (1.5 MHz normal)	V_{IN} = 4 V, T_J = - 40°C to 125°C	15%	20%	25%	V_{IN}
$V_{FSW\_LOW\_HSY}$	Hysteresis for fsw foldback	V_{IN} = 4 V, T_J = 25°C		150		mV
TIMING						
t_{ON_MIN}	Minimum on time	V_{IN} = 4 V, T_J =- 40°C to 125°C		75	95	ns
t_{SS}	Soft-start time	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		0.9		ms
t_{HIC_ON}	Off time of hiccup cycle	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		74		ms
t_{HIC_OFF}	On time of hiccup cycle	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		1.9		ms
ERROR AMPLIFIER						
V_{COMPH}	COMP output high voltage Auto PFM	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C, V_{FB} = V_{REF} - 200mV		1.4		V
	COMP output high voltage Forced PWM	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C, V_{FB} = V_{REF} - 200mV		1.5		V
V_{COMPL}	COMP output low voltage Auto PFM	V_{IN} = 4 V, $V_{°OUT}$ = 12 V, T_J = 25°C, V_{FB} = V_{REF} + 200mV		0.8		V
	COMP output low voltage Forced PWM	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C, V_{FB} = V_{REF} + 200mV		0.6		V
Gm	Error amplifier trans conductance	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		175		µS
I_{SINK_EA}	Sink current of COMP	V_{IN} = 4 V, T_J = 25°C, V_{FB} = V_{REF} + 200mV		20		µA
I_{SOURCE_EA}	Source current of COMP	V_{IN} = 4 V, T_J = 25°C, V_{FB} = V_{REF} - 200mV		20		µA
PROTECTION						
V_{OVP}	Output over-voltage protection threshold	V_{IN} = 2.5 V to 5.5 V, T_J =- 40°C to 125°C	16.5	17.3	18	V
V_{OVP_HYS}	Output over-voltage protection hysteresis	V_{IN} = 4 V, V_{OUT} = 12 V, T_J = 25°C		500		mV
THERMAL						
T_{SD}	Thermal shutdown threshold	V_{IN} = 4 V, V_{OUT} = 12 V		140		°C
T_{SD_HYS}	Thermal shutdown hysteresis	V_{IN} = 4 V, V_{OUT} = 12 V		20		°C

6.6 Typical Characteristics



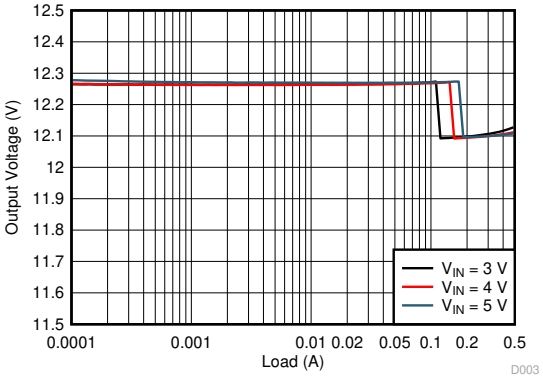
V_{OUT} = 12 V　　L = 2.2 µH　　Auto PFM

図 6-1. Efficiency vs Load



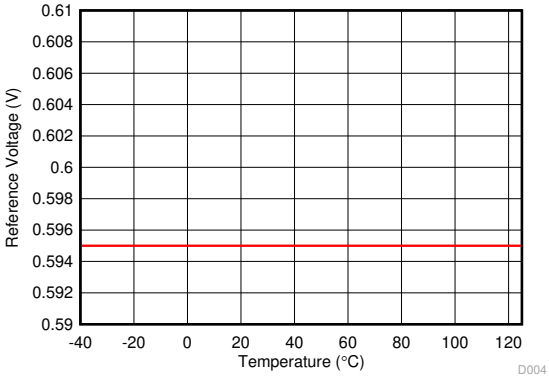
V_{OUT} = 12 V　　L = 2.2 µH　　Forced PWM

図 6-2. Efficiency vs Load



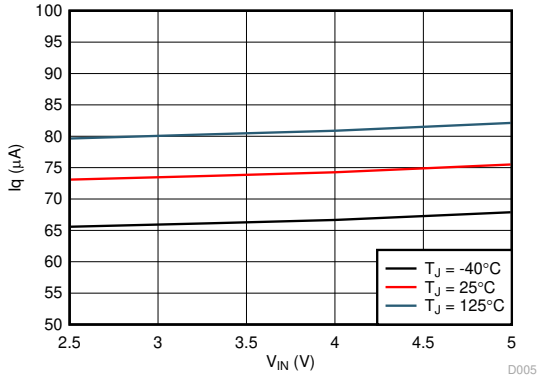
V_{OUT} = 12 V　　L = 2.2 µH　　Auto PFM

図 6-3. Load Regulation



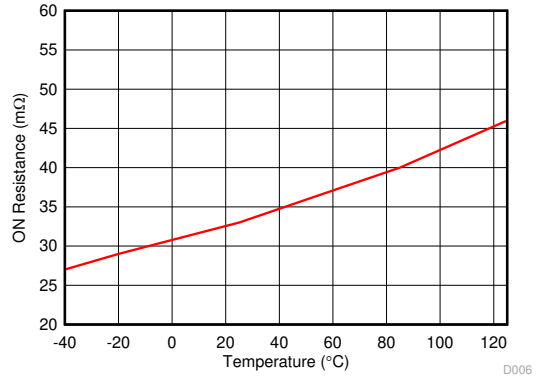
V_{IN} = 4 V

図 6-4. Reference Voltage vs Temperature



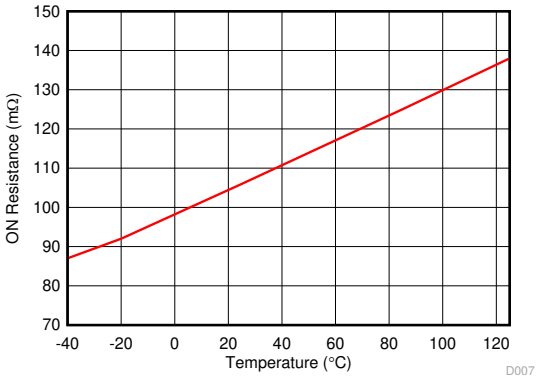
V_{IN} = 2.5 V to 5.5 V　　V_{OUT} = 12 V　　No Switching

図 6-5. I_q vs V_{IN}



V_{IN} = 4 V　　V_{OUT} = 12 V

図 6-6. Low-Side RDS_{ON} vs Temperature



V_{IN} = 4 V V_{OUT} = 12 V

図 6-7. High-side RDS_{ON} vs Temperature

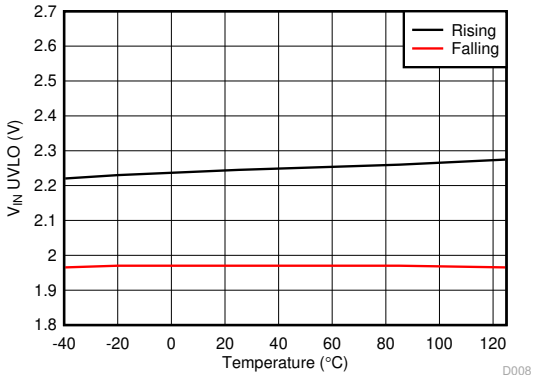


図 6-8. UVLO Threshold vs Temperature

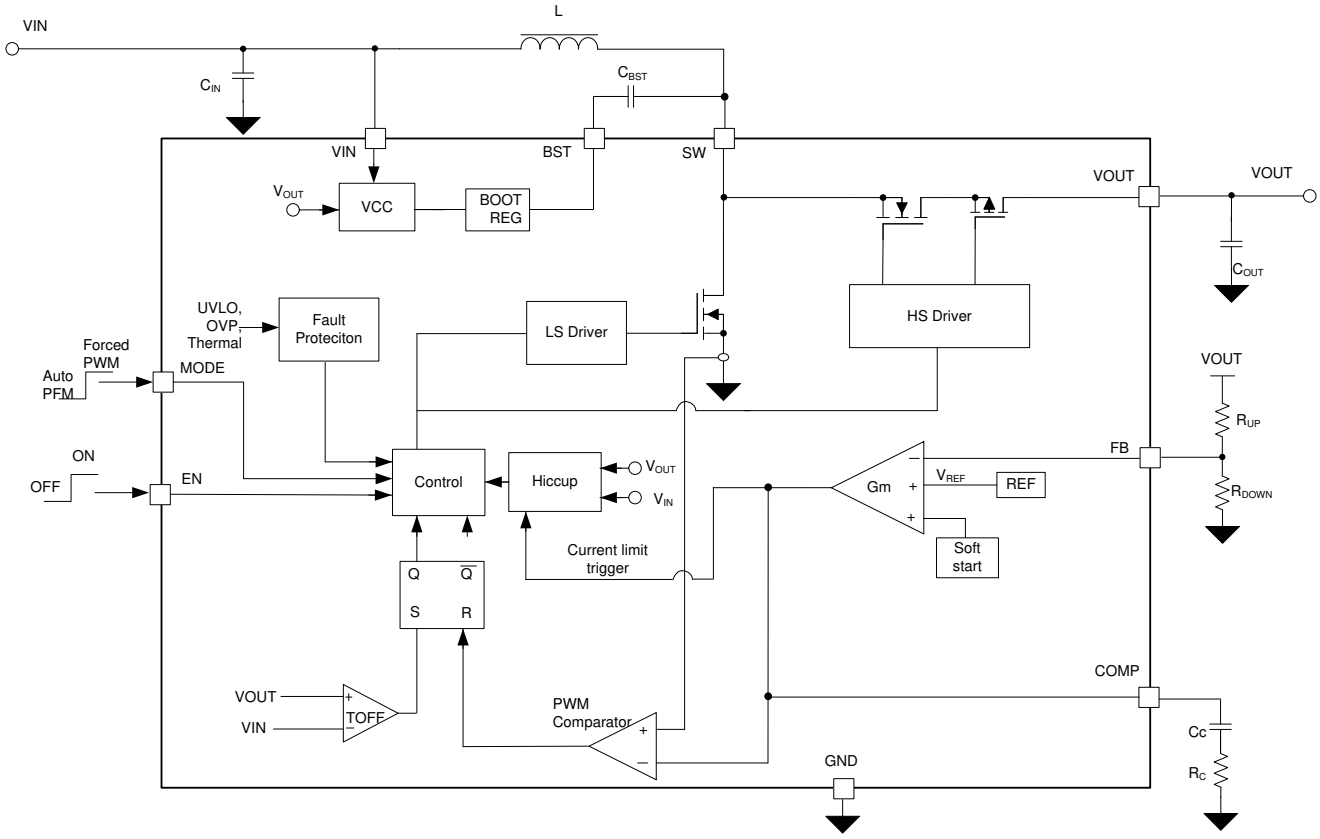
7 Detailed Description

7.1 Overview

The TPS61372 is a highly-integrated synchronous boost converter to support 16-V output with load disconnect and short protection built-in. The TPS61372 supports input voltage ranging from 2.5 V to 5.5 V. The TPS61372 uses the peak current mode with adaptive off-time control topology to regulate the output voltage. The TPS61372 operates at a quasi-constant frequency pulse-width modulation (PWM) at moderate to heavy load current. At the beginning of each cycle, the low-side FET turns on and the inductor current ramps up to reach a peak current determined by the output of the error amplifier (EA). When the peak current pre-set value determined by the output trips of the EA, the low-side FET turns off. As long as the low-side FET turns off, the high-side FET turns on after a short delay time to avoid the shoot through. The duration of low-side FET off state is determined by the V_{IN} / V_{OUT} ratio.

High efficiency is achieved at light load as the TPS61372 operates in PFM operation. The device can be also configured at forced PWM mode to keep the frequency constant across the whole load range and to have more immunity against noise sensitive applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit prevents the device from malfunctioning at the low input voltage of the battery from the excessive discharge. The device starts operation once the rising V_{IN} trips the UVLO threshold and it disables the output stage of the converter once V_{IN} is below the UVLO falling threshold.

7.3.2 Enable and Disable

When the input voltage is above the UVLO threshold and the EN pin is pulled above the high threshold (1.2 V minimum), the TPS61372 is enabled. When the EN pin is pulled below the low threshold (0.4 V maximum), the TPS61372 goes into shutdown mode.

7.3.3 Error Amplifier

The TPS61372 has a transconductance amplifier and compares the feedback voltage with the internal voltage reference (or the internal soft-start voltage during start-up phase). The transconductance of the error amplifier is 175 µA / V typically. The loop compensation components are placed between the COMP terminal and ground to optimize the loop stability and response speed.

7.3.4 Bootstrap Voltage (BST)

The TPS61372 has an integrated bootstrap regulator and requires a small ceramic capacitor between the BST and SW pin to provide the gate drive voltage for the high-side FET. The recommended value for this ceramic capacitor is between 20 nF to 200 nF.

7.3.5 Load Disconnect

The TPS61372 device provides a load disconnect function, which completely disconnects the output from the input during shutdown or fault conditions.

7.3.6 Overvoltage Protection

If the output voltage is detected above the overvoltage protection threshold (typically 17.3 V), the TPS61372 stops switching immediately until the voltage at the V_{OUT} pin drops below the output overvoltage protection recovery threshold (with 500-mV hysteresis). This function prevents the devices against the overvoltage and secures the circuits connected with the output of excessive overvoltage.

7.3.7 Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 140°C (typical). When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 120°C (typical).

7.3.8 Start-Up

The TPS61372 implements the soft start function to reduce the inrush current during start-up. The TPS61372 begins soft start when the EN pin is pulled high. There are two phases for the start-up procedure:

- When V_{OUT} is below 120% V_{IN}, the output votlage ramps up with the switching frequency of 535 kHz (typical).
- When V_{OUT} exceeds 120% V_{IN}, the switching frequency changes to 1.5 MHz typically and ramps up the output voltage to the setpoint.

7.3.9 Short Protection

The TPS61372 provides a hiccup protection mode when output short protection occurs. In hiccup mode, the TPS61372 shuts down after the 1.9-ms duration of current limit is triggered and the V_{OUT} is pulled below 105% V_{IN}. In hiccup steady state, the device shuts down itself and restarts after a 74-ms (typical) waiting time, which helps to reduce the overall thermal dissipation at continuous short condition. After the short condition releases, the device can recover automatically and restart the start-up phase.

7.4 Device Functional Modes

7.4.1 Operation

In light load condition, the TPS61372 can be configured at Auto PFM or Forced PWM. At Auto PFM operation, the switching frequency is lowered at light load and features higher efficiency, while for Forced PWM operation, the frequency keeps constant across the whole load range.

7.4.2 Auto PFM Mode

The TPS61372 integrates a power-save mode with pulse frequency modulation (PFM) at light load (set the mode pin low logic or floating). The device skips the switching cycles and regulates the output voltage at a higher threshold (typically 101.6% × V_{OUT_NORM}). 図 7-1 shows the working principle of the PFM operation. The auto PFM mode reduces the switching losses and improves efficiency at light load condition by reducing the average switching frequency.

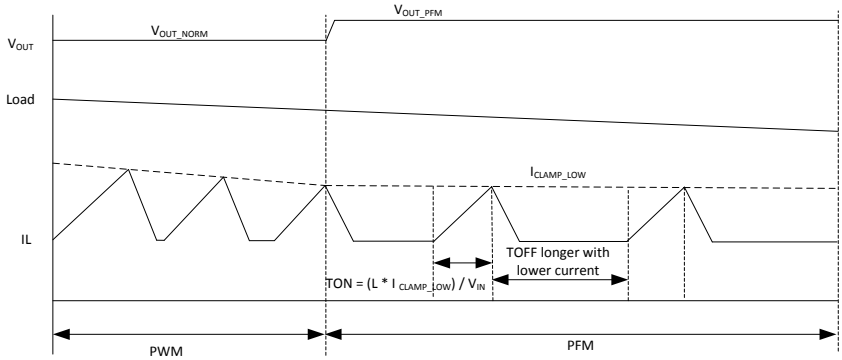


図 7-1. Auto PFM Operation Behavior

7.4.3 Forced PWM Mode

In forced PWM mode, the TPS61372 keeps the switching frequency constant across the whole load range. When the load current decreases, the output of the internal error amplifier decreases as well to lower the inductor peak current and delivers less power. The high-side FET is not turned off even if the current through the FET goes negative to keep the switching frequency be the same as that of the heavy load.

7.4.4 Mode Selectable

There is a mode pin to configure the TPS61372 into two different operation modes. The device works in auto PFM mode when pulling the mode pin to low or floating and in forced PWM mode when mode pin is high.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS61372 is a synchronous boost converter. The following design procedure can be used to select component values for the TPS61372. This section presents a simplified discussion of the design process. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an interactive design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

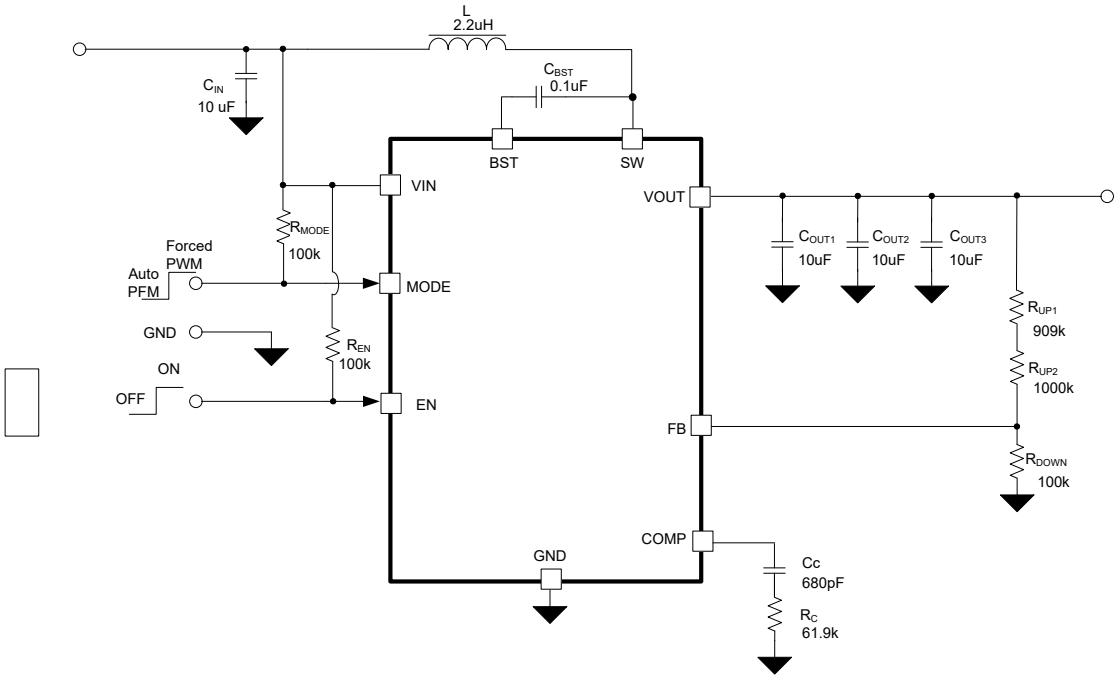


図 8-1. TPS61372 12-V Output With Load Disconnect Schematic

8.2.1 Design Requirements

For this design example, use 表 8-1 as the design parameters.

表 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	3 V to 5 V
Output voltage	12 V
Output ripple voltage	± 3%
Output current	0.4 A
Operating frequency	1.5 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61372 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Output ripple voltage
- Output current rating
- Operating frequency

8.2.2.2 Setting the Output Voltage

The output voltage of the TPS61372 is externally adjustable using a resistor divider network. The relationship between the output voltage and the resistor divider is given by 式 1.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \quad (1)$$

where

- V_{OUT} is the output voltage
- R_{UP} is the top divider resistor
- R_{DOWN} is the bottom divider resistor

Choose R_{DOWN} to be approximately 100 kΩ. Slightly increasing or decreasing R_{DOWN} can result in closer output voltage matching when using standard value resistors. In this design, R_{DOWN} = 100 kΩ and R_{UP} = 1.909 MΩ (1 MΩ + 909 kΩ) , resulting in an output voltage of 12 V.

For the best accuracy, TI recommends R_{DOWN} to be around 100 kΩ to ensure that the current following through R_{DOWN} is at least 100 times larger than FB pin leakage current. Changing R_{DOWN} towards the lower value

increases the robustness against noise injection. Changing R_{DOWN} towards the higher values reduces the quiescent current for achieving higher efficiency at the light load currents.

8.2.2.3 Selecting the Inductor

A boost converter normally requires two main passive components for storing the energy during power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency) as well as the transient behavior and loop stability, which makes the inductor to be the most critical component in application.

When selecting the inductor, as well as the inductance, the other parameters of importance are:

- The maximum current rating (RMS and peak current should be considered)
- The series resistance
- Operating temperature

Choosing the inductor ripple current with the low ripple percentage of the average inductor current results in a larger inductance value, maximizes the potential output current of the converter, and minimizes EMI. The larger ripple results in a smaller inductance value and a physically smaller inductor, which improves transient response, but results in potentially higher EMI.

The rule of thumb in choosing the inductor is to make sure the inductor ripple current (ΔI_L) is a certain percentage of the average current. The inductance can be calculated by 式 2, 式 3, and 式 4:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{2}$$

$$\Delta I_{L\_R} = \text{Ripple\%} \times \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \tag{3}$$

$$L = \frac{1}{\text{Ripple \%}} \times \frac{\eta \times V_{IN}}{V_{OUT} \times I_{OUT}} \times \frac{V_{IN} \times D}{f_{SW}} \tag{4}$$

where

- Δ_{IL} is the peak-peak inductor current ripple
- V_{IN} is the input voltage
- D is the duty cycle
- L is the inductor
- f_{SW} is the switching frequency
- Ripple% is the ripple ration versus the DC current
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- η is the efficiency

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches the saturation level, its inductance can decrease 20% to 35% from the value at 0-A bias current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

The inductor peak current varies as a function of the load, the switching frequency, and the input and output voltages and it can be calculated by 式 5 and 式 6.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L \tag{5}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{IN} is the input average current
- ΔI_L is the ripple current of the inductor

The input DC current is determined by the output voltage, the output current, and efficiency can be calculated by:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{6}$$

where

- I_{IN} is the input current of the inductor
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- η is the efficiency

While the inductor ripple current depends on the inductance, the frequency, the input voltage, and duty cycle calculated by 式 2, replace 式 2, 式 6 into 式 5 to calculate the inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \tag{7}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{OUT} is the output current
- D is the duty cycle
- η is the efficiency
- V_{IN} is the input voltage
- L is the inductor
- f_{SW} is the switching frequency

The heat rating current (RMS) is calculated by 式 8:

$$I_{L\_RMS} = \sqrt{I_{IN}^2 + \frac{1}{12}(\Delta I_L)^2} \tag{8}$$

where

- I_{L_RMS} is the RMS current of the inductor
- I_{IN} is the input current of the inductor
- ΔI_L is the ripple current of the inductor

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature related rating current of the inductors.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)

- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and footprint.

The following inductor series in 表 8-2 from the different suppliers are recommended.

表 8-2. Recommended Inductors for TPS61372

PART NUMBER	L (µH)	DCR Typ (mΩ) TYP.	SATURATION CURRENT / TYP.	SIZE (L × W × H mm)	VENDOR(1)
XAL4020-222ME	2.2	35	5.6	4 x 4 x 2	Coilcraft
DFE322512F-2R2M=P2	2.2	66	2.6	3.2 x 2.5 x 1.2	Murata
DFE322520FD-4R7M#	4.7	98	3.4	3.2 x 2.5 x 2.0	Murata

(1) See the *Third-party Products Disclaimer*.

8.2.2.4 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. Then the loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by 式 9:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (9)$$

where

- C_{OUT} is the output capacitor
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- Δ_V is the output voltage ripple required
- f_{SW} is the switching frequency

The additional output ripple component caused by ESR is calculated by 式 10:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (10)$$

where

- ΔV_{ESR} is the output voltage ripple caused by ESR
- R_{ESR} is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, it must be considered if used.

Care must be taken when evaluating the rating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate by as much as 70% of its capacitance at its rated voltage. Therefore, enough margins on the voltage rating should be considered to ensure adequate capacitance at the required output voltage.

表 8-3. Recommended Output Capacitor for TPS61372

PART NUMBER	C (µF)	PIECES	DESCRIPTION	SIZE	VENDOR(1)
GRM188R61E106MA73D	10	3	X5R, 0603, 5 V, ±20% tolerance	0603	Murata

8.2.2.5 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. Place additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, between C_{IN} and the power source lead, to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

8.2.2.6 Loop Stability and Compensation

8.2.2.6.1 Small Signal Model

The TPS61372 uses the peak current with adaptive off-time control topology. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole system, created by R_{OUT} and C_{OUT}. An external loop compensation network connecting to the COMP pin of TPS61372 is added to optimize the loop stability and the response time, a resistor R_C, capacitor C_C, and C_P shown in 図 8-2 comprises the loop compensation network.

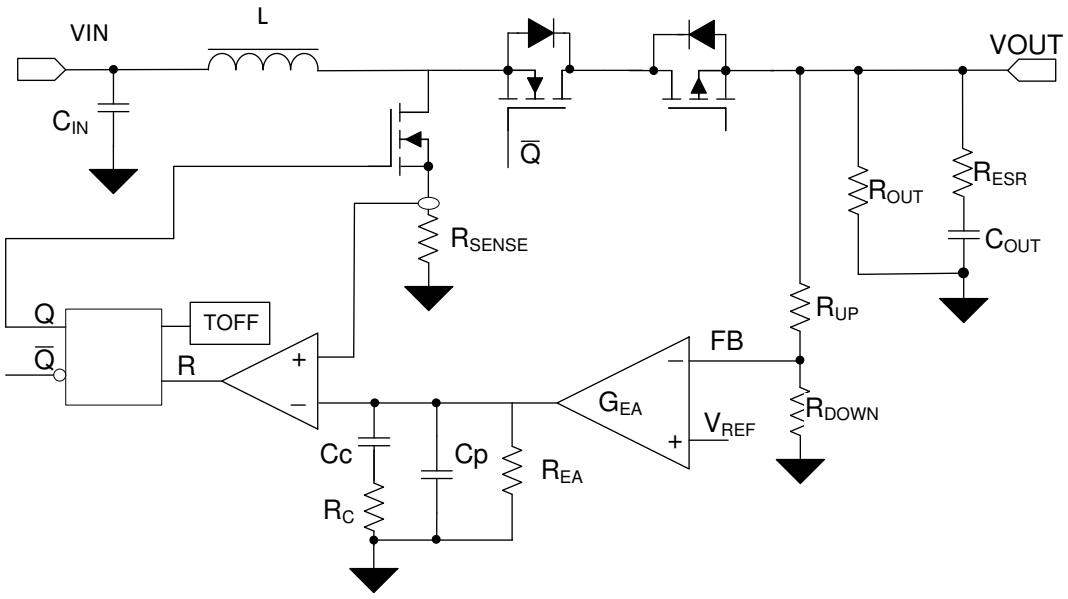


図 8-2. TPS61372 Control Equivalent Circuitry Model

The small signal of power stage including the slope compensation is:

$$G_{PS}(S) = \frac{R_{OUT} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{S}{2\pi \times f_{ESR}}\right)\left(1 - \frac{S}{2\pi \times f_{RHP}}\right)}{1 + \frac{S}{2\pi \times f_P}} \quad (11)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- R_{SENSE} is the equivalent internal current sense resistor, which is typically 0.2 Ω of TPS61372

The single pole of the power stage is:

$$f_P = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \quad (12)$$

where

- C_{OUT} is the output capacitance, for a boost converter having multiple, identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (13)$$

where

- R_{ESR} is the equivalent resistance in series of the output capacitor

The right-hand plane zero is:

$$f_{RHP} = \frac{R_{OUT} \times (1-D)^2}{2\pi \times L} \quad (14)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- L is the inductance

The TPS61372 COMP pin is the output of the internal trans-conductance amplifier.

式 15 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA}(S) = G_{EA} \times R_{EA} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \times \frac{1 + \frac{S}{2 \times \pi \times f_Z}}{(1 + \frac{S}{2 \times \pi \times f_{P1}}) \times (1 + \frac{S}{2 \times \pi \times f_{P2}})} \quad (15)$$

where

- R_{EA} is the output impedance of the error amplifier R_{EA} = 500 MΩ. G_{EA} is the transconductance of the error amplifier, G_{EA} = 175 µS.
- f_{P1}, f_{P2} is the pole's frequency of the compensation
- f_Z is the zero's frequency of the compensation network

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C_c} \quad (16)$$

where

- C_C is the zero capacitor compensation

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (17)$$

where

- C_P is the pole capacitor compensation
- R_C is the resistor of the compensation network

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (18)$$

8.2.2.7 Loop Compensation Design Steps

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

1. **Set the Crossover Frequency, f_C.**
   - The first step is to set the loop crossover frequency, f_C. The higher crossover frequency, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}. Then calculate the loop compensation network values of R_c, C_c, and C_p in following sections.
2. **Set the Compensation Resistor, R_C.**
   - By placing f_Z below f_C, for frequencies above f_C, R_C | | R_{EA} approximately = R_C, so $R_C \times G_{EA}$ sets the compensation gain. Setting the compensation gain, $K_{COMP\text{-}dB}$, at f_Z, results in the total loop gain, $T_{(s)} = G_{PS(s)} \times H_{EA(s)} \times He(s)$ being zero at f_C.
   - Therefore, to approximate a single-pole rolloff up to f_{P2}, rearrange 式 19 to solve for RC so that the compensation gain, K_{EA}, at f_C is the negative of the gain, K_{PS}, read at frequency f_C for the power stage bode plot or more simply:

$$K_{EA}(f_C) = 20 \times \log(G_{EA} \times R_C \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}) = -K_{PS}(f_C) \quad (19)$$

     where

     – K_{EA} is gain of the error amplifier network
     – K_{PS} is the gain of the power stage
     – G_{EA} is the transconductance of the amplifier, the typical value of G_{EA} = 175 µA / V
3. **Set the compensation zero capacitor, C_C.**
   - Place the compensation zero at the power stage pole position of R_{OUT}, C_{OUT} to get:

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (20)$$

   - Set $f_Z = f_P$, and get:

$$C_C = \frac{R_{OUT} \times C_{OUT}}{2R_C} \quad (21)$$

4. **Set the compensation pole capacitor, C_P.**
   - Place the compensation pole at the zero produced by the R_{ESR} and the C_{OUT}. It is useful for canceling unhelpful effects of the ESR zero.

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (22)$$

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (23)$$

   - Set $f_{P2} = f_{ESR}$, and get:

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C} \quad (24)$$

   - If the calculated value of C_P is less than 10 pF, it can be neglected.

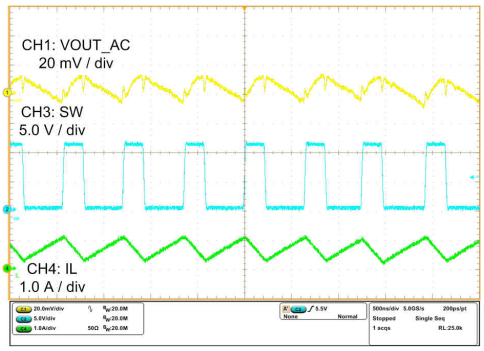
Designing the loop for greater than 45° of phase margin and greater than 6-dB gain margin eliminates output voltage ringing during the line and load transient. The R_C = 61.9 kΩ , C_C = 680 pF for this design example.

8.2.2.8 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during the turnon of each cycle and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 20 nF to 200 nF. C_{BST} should be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 100 nF is selected for this design example.

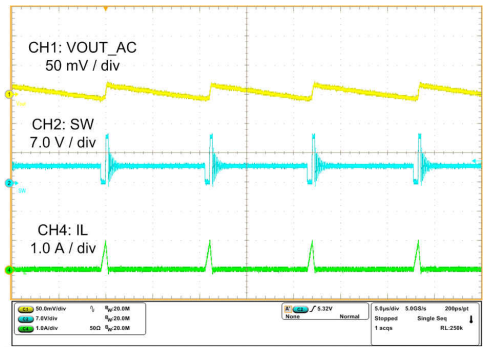
8.2.3 Application Curves

Typical condition V_{IN} = 3 V to 5 V, V_{OUT} = 12 V, temperature = 25°C, unless otherwise noted



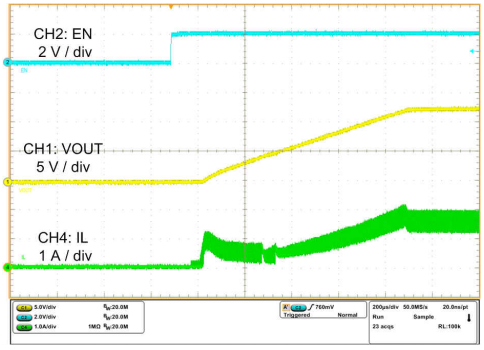
V_{IN} = 4 V V_{OUT} = 12 V Mode = Auto PFM
L = 2.2 µH C_{OUT} = 3 × 10 µF

図 8-3. Steady-State at 200-mA Load



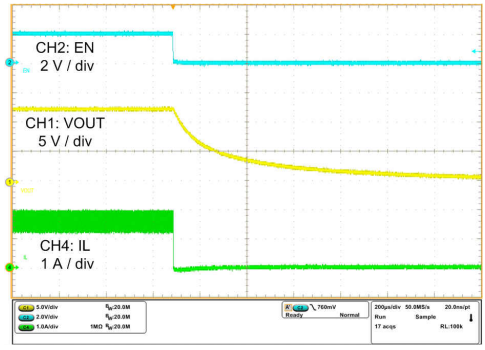
V_{IN} = 4 V V_{OUT} = 12 V Mode = Auto PFM
L = 2.2 µH C_{OUT} = 3 × 10 µF

図 8-4. Steady-State at 10-mA Load



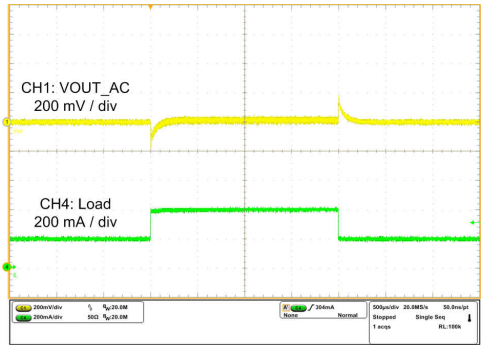
V_{IN} = 4 V V_{OUT} = 12 V Mode = Auto PFM
L = 2.2 µH C_{OUT} = 3 × 10 µF

図 8-5. Start-Up by EN, Load = 12.5 Ω



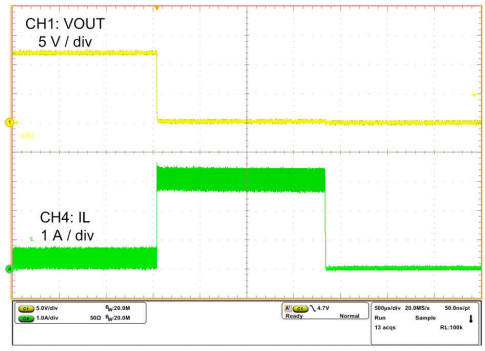
V_{IN} = 4 V V_{OUT} = 12 V Mode = Auto PFM
L = 2.2 µH C_{OUT} = 3 × 10 µF

図 8-6. Shutdown by EN, Load = 12.5 Ω



V_{IN} = 4 V V_{OUT} = 12 V Mode = Auto PFM
L = 2.2 µH C_{OUT} = 3 × 10 µF

図 8-7. Load Transient, 200 mA to 400 mA, 100 mA / µs



V_{IN} = 4 V V_{OUT} = 12 V Mode = Auto PFM
L = 2.2 µH C_{OUT} = 3 × 10 µF

図 8-8. Shorted Output

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply ranging from 2.5 V to 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS61372, the bulk

capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator can suffer from the instability or noise problems.

The following checklist is suggested that be followed to get good performance for a well-designed board:

1. Minimize the high current path from output of chip, the output capacitor to the GND of chip. This loop contains high di / dt switching currents (nano seconds per ampere) and easy to transduce the high frequency noise.
2. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize inter plane coupling.
3. Use a combination of bulk capacitors and smaller ceramic capacitors with low series resistance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for decoupling the noise.
4. The ground area near the IC must provide adequate heat dissipating area. Connect the wide power bus (for example, V_{OUT}, SW, GND) to the large area of copper, or to the bottom or internal layer ground plane, using vias for enhanced thermal dissipation.
5. Place the input capacitor being close to the V_{IN} pin and the PGND pin in order to reduce the input supply ripple.
6. Place the noise sensitive network like the feedback and compensation being far away from the SW trace.
7. Use a separate ground trace to connect the feedback and the loop compensation circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.

10.2 Layout Example

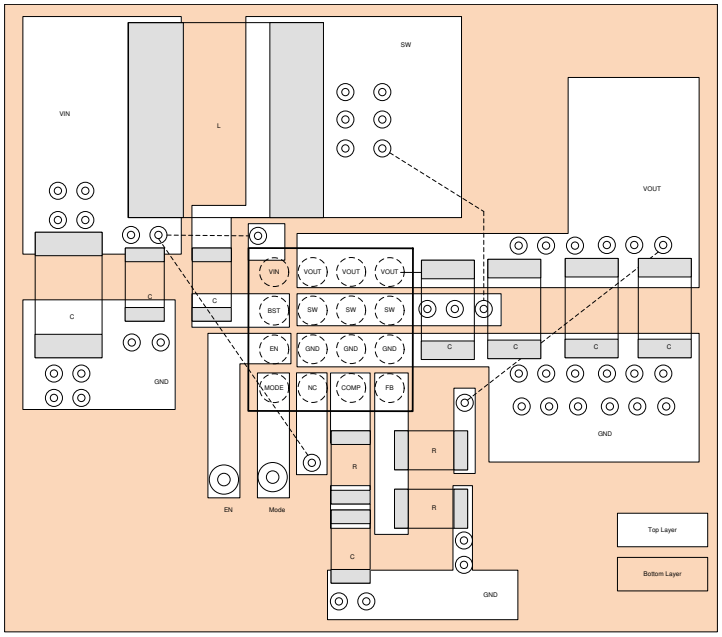


図 10-1. Recommended Layout

10.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB

As power demand in portable designs is more and more important, designers must figure the best trade-off between efficiency, power dissipation and solution size. Due to integration and miniaturization, junction temperature can increase significantly which could lead to bad application behaviors (that is, premature thermal shutdown or worst case reduce device reliability). Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. Keep the device operating junction temperature (T_J) below 125°C.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61372 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
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- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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11.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61372YKBR	Active	Production	DSBGA (YKB) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 61372
TPS61372YKBR.A	Active	Production	DSBGA (YKB) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 61372
TPS61372YKBT	Active	Production	DSBGA (YKB) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 61372
TPS61372YKBT.A	Active	Production	DSBGA (YKB) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS 61372

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

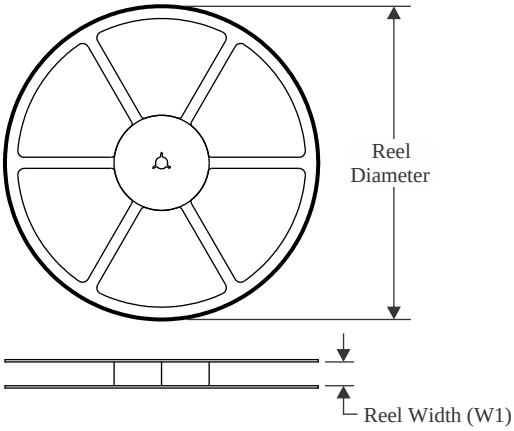
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

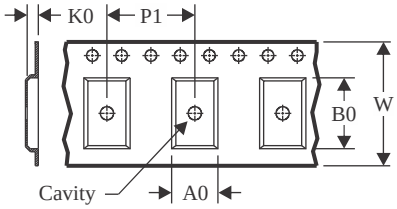
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

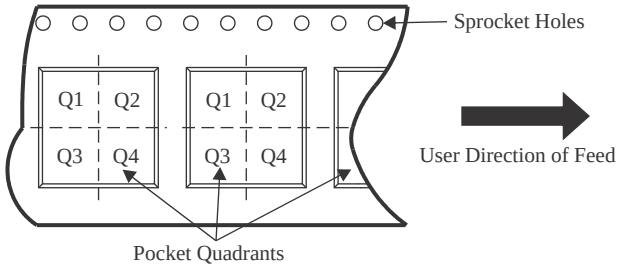


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

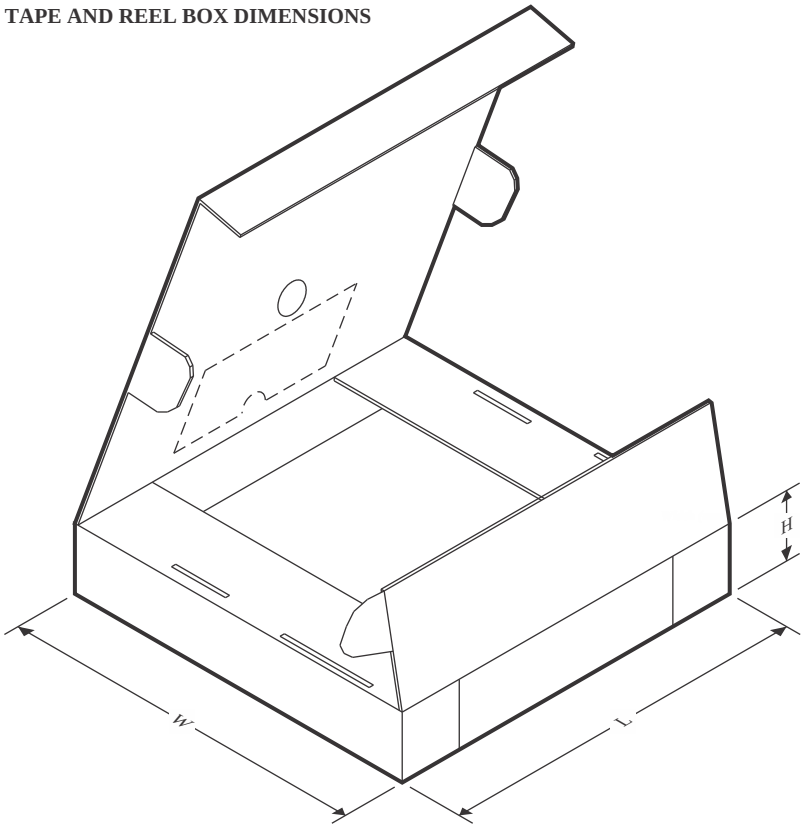
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61372YKBR	DSBGA	YKB	16	3000	180.0	8.4	1.68	1.72	0.62	4.0	8.0	Q1
TPS61372YKBT	DSBGA	YKB	16	250	180.0	8.4	1.68	1.72	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61372YKBR	DSBGA	YKB	16	3000	182.0	182.0	20.0
TPS61372YKBT	DSBGA	YKB	16	250	182.0	182.0	20.0

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