TPS61230A 5V/6A高効率昇圧型コンバータ、2.0mm×2.0mm VQFNパッケージ

1 特長

- 入力電圧範囲: 2.5V～4.5V
- 出力電圧範囲: 2.5V～5.5V
- 2つの21mΩ (LS)/18mΩ (HS) MOSFET
- 20µAの静止電流
- 6Aのバレー・スイッチング電流制限
- 1.15MHzの疑似定スイッチング周波数
- 軽負荷時のPFM動作
- 1.05msのソフトスタート時間
- 完全な負荷切断
- Vin > Vout動作には非対応
- 出力短絡保護
- 過電圧保護
- サーマル・シャットダウン
- 2.0mm×2.0mmのVQFN 7ピン・パッケージ

2 アプリケーション

- パワー・バンク、バッテリ・バックアップ・ユニット
- USB電源
- タブレットPC
- オーディオ・パワー・アンプ
- バッテリ駆動の製品

3 概要

TPS61230Aデバイスは、高効率で完全に統合された同期昇圧コンバータです。6Aで、21mΩおよび18mΩのパワー・スイッチが内蔵されており、2.5Vの入力電源で、2.4Aの出力電流を5V出力で供給できます。R_{OS_ON}が低いスイッチにより、最大96%の電力変換効率を実現し、非常に小型のソリューションでも熱ストレスを最小化できます。

標準の動作周波数は1.15MHzで、小型のコイルとコンデンサを使用できるため、ソリューションのサイズを小さくできます。TPS61230Aは、外付けの分圧抵抗を使用して出力電圧を変更できます。

軽負荷時には、TPS61230Aは自動的にPFM動作に移行し、最小の静止電流で効率を最大化します。ENピンをLOWにするとシャットダウンが行われ、入力から負荷が完全に切断されて、入力消費電流は1.0µA未満に低下します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS61230A	VQFN (7)	2.00mm×2.00mm

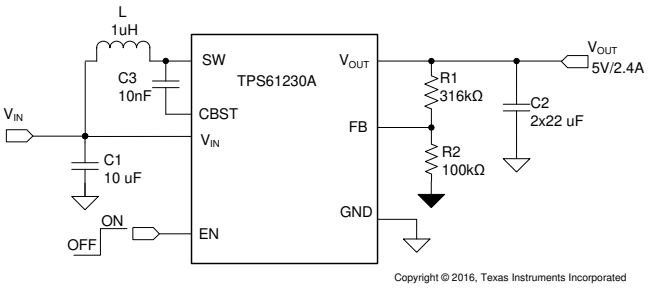
(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

デバイス比較表

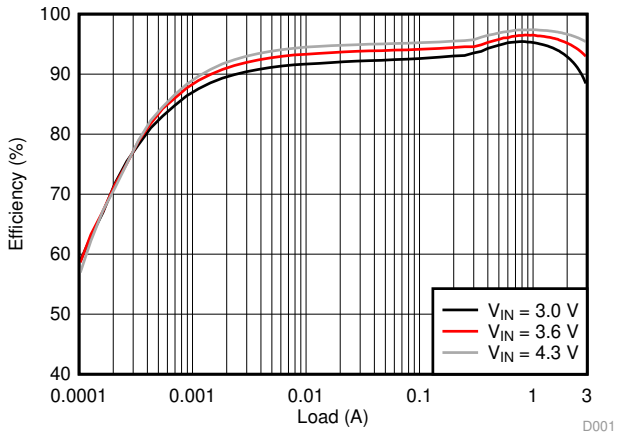
型番	出力電圧
TPS61230A	可変
TPS61230xA(1)	固定 Vout、3.7、4.3、4.5、4.8、5.0、5.1、5.4

(1) 製品プレビュー：詳細については TI 工場にお問い合わせください。

代表的なアプリケーション



効率



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4 改訂履歴

Revision A (July 2016) から **Revision B** に変更 **Page**

- Added thermal information for EVM configuration ... 5

2016年7月発行のものから更新 **Page**

- 製品プレビューから量産データへ 変更 ... 1

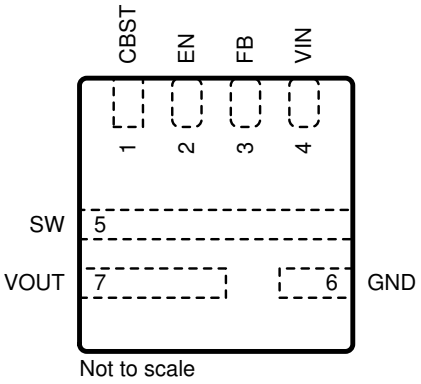
5 概要（続き）

出力が短絡すると、デバイスはヒカップ保護モードに移行し、出力短絡が解消されると自動的に回復します。出力過電圧保護、サーマル・シャットダウン保護など他の機能も搭載されています。

このデバイスは2.00mm×2.00mm×0.9mmのVQFNパッケージで供給され、必要な外付け部品数が最小限です。

6 Pin Configuration and Functions

RNS Package
7-Pin VQFN
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CBST	1	I	Boot strap capacitor for the supply of high-side MOSFET driver. An external capacitor is required between the SW and CBST pins to provide supply voltage to the high-side MOSFET gate driver.
EN	2	I	This is the enable pin of the device. Connecting this pin to ground (< 0.4 V) forces the device into shutdown mode. Pulling this pin to high (> 1.2 V) enables the device. This pin must be terminated but not floating.
FB	3	I	Voltage feedback of adjustable output voltage. Connecting a resistor divider network from the output of the converter to the FB pin. Must be connected to VOUT on fixed output voltage version.
VIN	4	I	Supply voltage for the internal circuitry.
SW	5	I/O	Switching node of the boost regulator. It is connected to the drain of the internal low side power FET and the source of the internal high-side power FET.
GND	6	–	Ground pin. Return for the internal voltage reference and analog circuits, also the source terminal of the low-side FET switch.
VOUT	7	O	Boost converter output.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, EN, VOUT, FB	-0.3	6	V
	SW	-0.3	7	V
	C_{BST}	-0.3	12	V
Operating junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.5		4.5	V
V_{OUT}	Output voltage range			5.5	V
L	Effective inductance range	0.47	1	1.3	µH
C_I	Effective input capacitance range	1	10		µF
C_O	Effective output capacitance range	15	22	80	µF
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61230A RNS 7 PINS (VQFN) Standard	TPS61230A RNS 7 PINS (VQFN) EVM(2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (no vias)	93	60.0	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (with vias underneath)	56		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.4	N/A(3)	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	57.8	N/A(3)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.1	27.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Measured on the evaluation module (EVM PWR767A), 2-layer 50mm × 63mm PCB (2 oz on all layers).
(3) N/A - Dose not apply for EVM configuration.

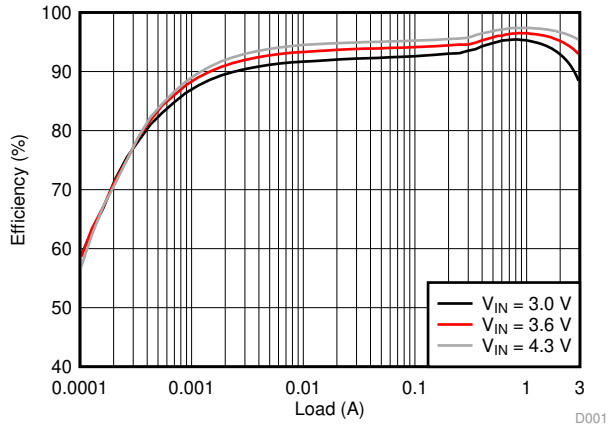
7.5 Electrical Characteristics

T_J = -40 °C to 125 °C and V_{IN} = 3.6 V. Typical values are at T_J = 25 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Input voltage range		2.5		4.5	V
V_{VIN_UVLO}	Input under voltage lockout	V_{IN} rising			2.5	V
V_{VIN_HYS}	VIN UVLO hysteresis			150		mV
I_{Q_VIN}	Quiescent current into VIN pin	IC enabled, No load , No Switching, V_{OUT} = 5 V, V_{IN} = 4.2 V		20	50	µA
I_{Q_VOUT}	Quiescent current into VOUT pin	IC enabled, No load, No Switching V_{OUT} = 5 V		25	55	µA
I_{SD}	Shutdown current into VIN	IC disabled, T_J < 85°C, V_{IN} = 4.2 V		0.2	1	µA
Output						
V_{OUT}	Output voltage range		2.5		5.5	V
V_{FB_PWM}	Feedback voltage	PWM mode	1.171	1.195	1.219	V
V_{FB_PFM}	Feedback voltage	PFM mode		101.2		% V_{FB}
V_{OVP}	Output overvoltage protection threshold		5.7	5.8	5.99	V
I_{LKG_FB}	Leakage current into FB pin	V_{FB} = 1.2 V			20	nA
Power Switch						
$R_{DS(on)}$	High-side MOSFET on resistance	V_{IN} = 3.6 V, V_{OUT} = 5 V, C_{BST} = 10 nF,		18	35	mΩ
$R_{DS(on)}$	Low-side MOSFET on resistance	V_{IN} = 3.6 V, V_{OUT} = 5 V, C_{BST} = 10 nF		21	36	mΩ
f_{sw}	Switching frequency	V_{IN} = 3.6 V, V_{OUT} = 5 V, PWM Operation	805	1150	1495	kHz
t_{ON_min}	Minimum on time				180	ns
I_{LIM_PRE}	Pre-charge mode and short circuit current limit (DC charge mode)	Linear mode, V_{OUT} = 2.5 V	1.02			A
		Linear mode, V_{OUT} = 0 V	0.06		0.6	A
I_{LIMIT}	Switching valley current limit		4.8	6.3	7.8	A
$t_{startup}$	Soft Start time (boost)	V_{IN} = 3.6 V, V_{OUT} = 5 V	0.3	1.05	1.9	ms
T_{SD}	Thermal shutdown threshold	T_J rising		160		°C
	Thermal shutdown hysteresis	T_J falling below T_{SD}		10		°C
Protection						
T_{HC_OFF}	Time for the hiccup off time	V_{IN} = 3.6 V		23		ms
T_{HC_ON}	Time for the hiccup on time	V_{IN} = 3.6 V		3.5		ms
Logic Interface						
V_{EN_H}	EN Logic high threshold				1.0	V
V_{EN_L}	EN Logic low threshold		0.4			V
I_{LKG_EN}	EN pin input leakage current	Connected to 3.6V V_{IN}		0.1	0.3	µA

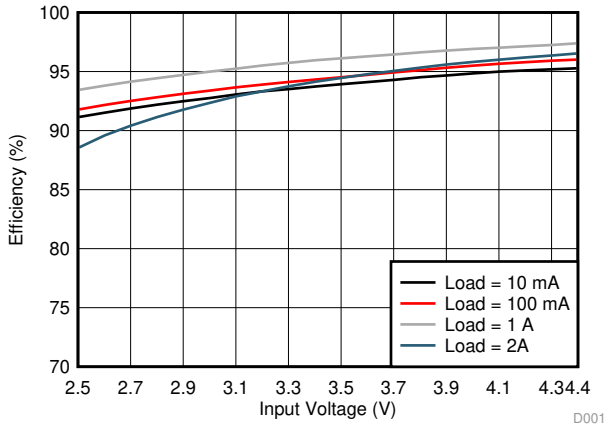
7.6 Typical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_J = -40°C to 125 °C, unless otherwise noted.



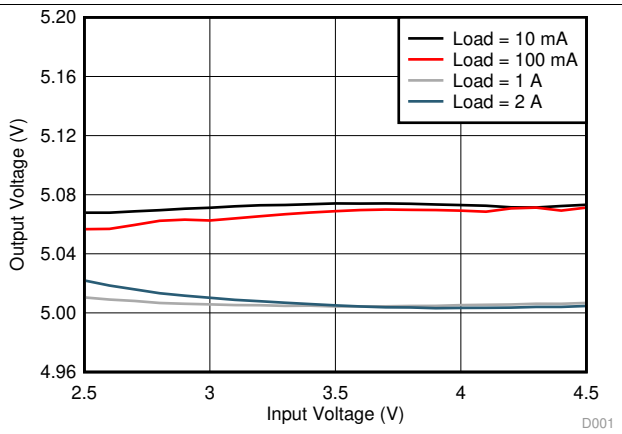
T_A = 25 ºC

図 1. Efficiency vs. Output Current



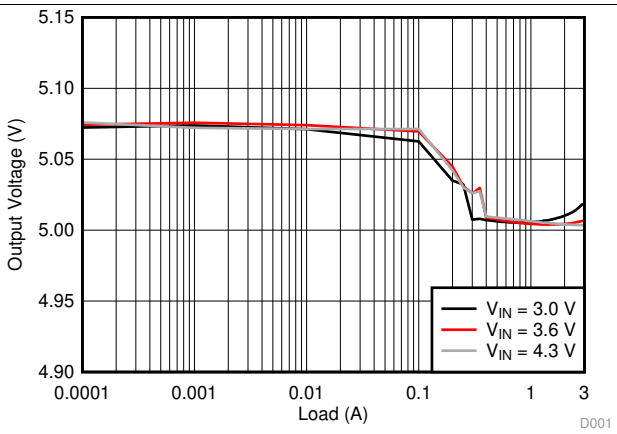
T_A = 25 ºC

図 2. Efficiency vs. Input Voltage



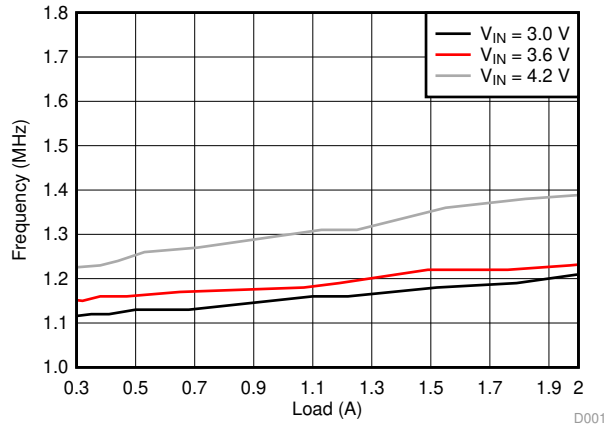
T_A = 25 ºC

図 3. Line Regulation



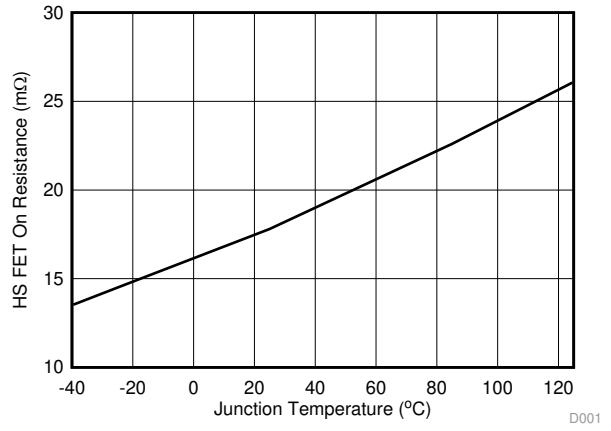
T_A = 25 ºC

図 4. Load Regulation



T_A = 25 ºC

図 5. Frequency vs. Load



V_{OUT} = 5 V V_{IN} = 3.6V

図 6. High-Side FET Rdson vs Junction Temperature

Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_J = -40°C to 125 °C, unless otherwise noted.

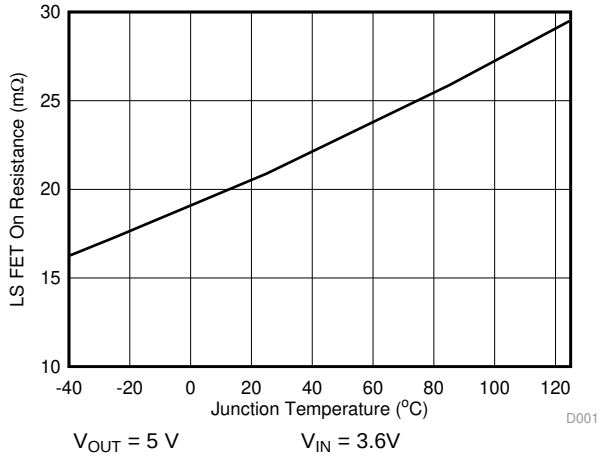


図 7. Low-Side FET Rdson vs Junction Temperature

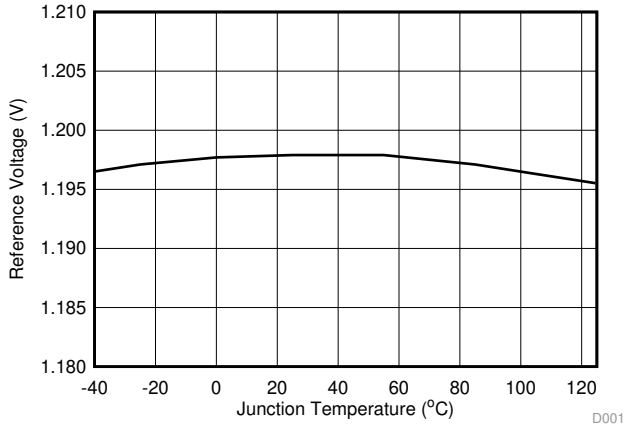


図 8. Voltage Reference vs Junction Temperature

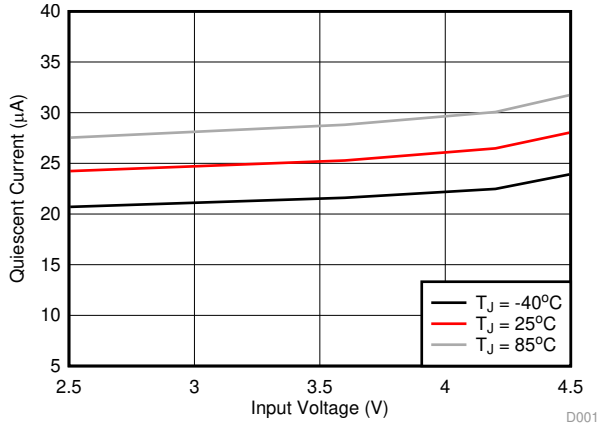


図 9. Quiescent Current vs Input Voltage

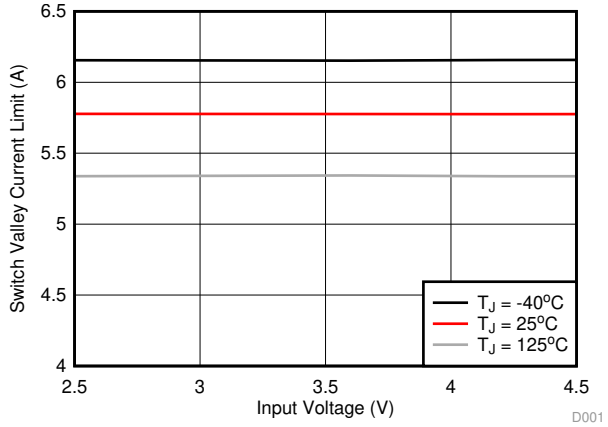


図 10. Switch Valley Current Limit vs Input Voltage

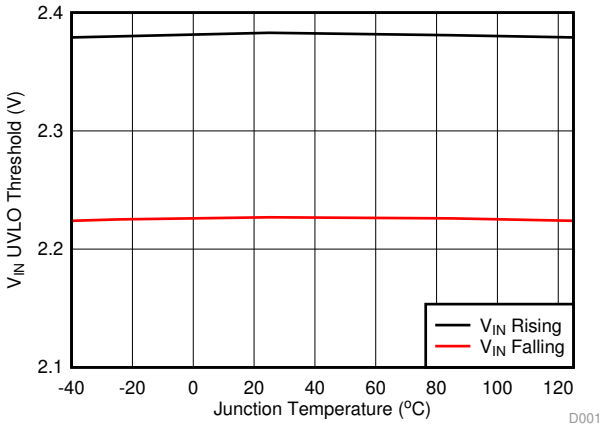


図 11. Vin UVLO Threshold vs Junction Temperature

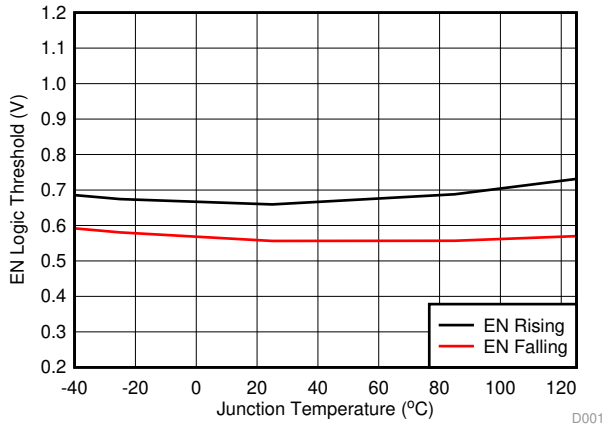


図 12. EN logic Threshold vs Junction Temperature

8 Detailed Description

8.1 Overview

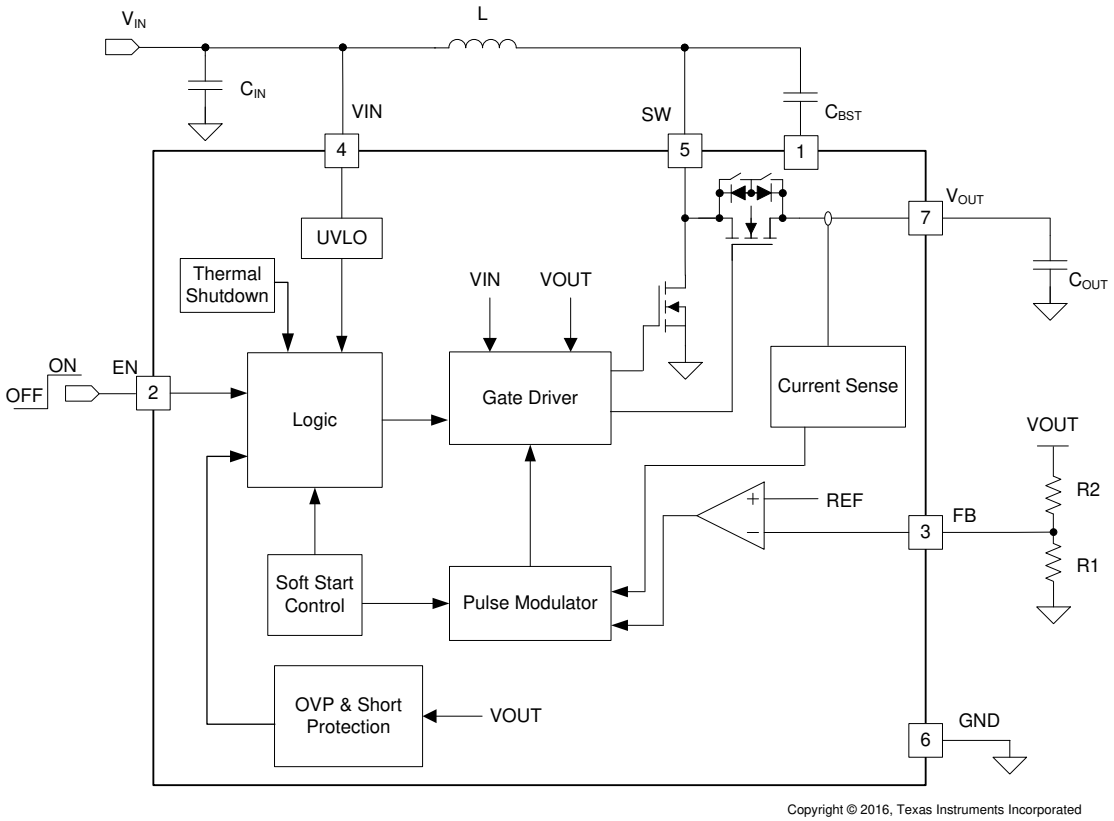
The TPS61230A is a high efficiency synchronous boost converter with integrating the 21-mΩ low side FET and 18-mΩ high side FET. The device could deliver up to 12-W output power with 5.5-V maximum output voltage from single cell Li-Iron battery. TPS61230A uses a quasi constant on-time valley current mode which provides an excellent transient response. The TPS61230xA typically operates at a quasi-constant 1.15-MHz frequency pulse width modulation (PWM) at the moderate to heavy load currents, allows the use of small inductor and capacitors to achieve a compact solution size.

During the PWM operation, a simple circuit predicts the required on time (with the VIN / VOUT ratio) of the ow-side FET. At the beginning of each switching cycle, the low-side FET turns on and the inductor current ramps up to the peak current determined by the on-time and the inductance. Once the on-timer expires, the high-side FET turns on and the inductor current decays to a preset valley current threshold determined by the Error Amplifier's output. The switching cycle repeats again by calculating the on time and activating the low-side FET.

At the light load currents, TPS61230A operates in Power Save Mode with pulse frequency modulation (PFM) and improves the efficiency under the light load.

Internal soft-start and loop compensation simplifies the design process and minimizes the number of external components.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Startup

When the device is enabled, the high-side FET turns on to charge the output capacitor linearly by a DC current which is called the pre-charge phase. The pre-charge startup phase terminates until the output voltage being close to the input voltage (typically VOUT = VIN -115mV). Once the output capacitor has been biased close to the input voltage (VOUT = VIN -115mV), the device starts switching which is called the boost soft start phase. During the soft start phase, there is a soft start voltage controlling the FB pin voltage, and the output voltage rising slope follows the soft start voltage slew rate (typically). The soft start phase completes when the soft start voltage reaches the internal reference voltage. The device begins to operate normally and regulates the output voltage at the pre-set target value.

表 1. Start-up Mode Description

MODE	DESCRIPTION	CONDITION
Pre-charge	Vout linearly startup without switching	VOUT < VIN – 115mV
Boost Soft Start	Vout startup with switching phase	VOUT > VIN -115mV

8.3.2 Enable and Disable

The device is enabled by setting EN pin to a voltage above 1.2V. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the startup is activated and the output voltage ramps up. With the EN pin pulled to ground, the device enters into the shutdown mode. In the shutdown mode, the TPS61230A stops switching and the internal control circuitry is turned off.

8.3.3 Under-Voltage Lockout (UVLO)

The under voltage lockout circuit prevents the device from malfunctioning at the low input voltage of the battery from the excessive discharge. The device starts operation once the rising VIN trips the under-voltage lockout threshold (UVLO) , and it disables the output stage of the converter once the VIN is below UVLO falling threshold.

8.3.4 Current Limit Operation

During the startup phase, the output current is limited to the pre-charge current limit which is proportional to the output voltage. The device could support minimum 1.0A output current at 2.5V input.

The TPS61230A employs a valley current sensing scheme at the normal boost switching phase. The switch valley current limit detection occurs during the off time through the sensing the voltage drop across the rectifier FET. If the switch valley current is lower than the valley current limit level, the device turns off the rectifier FET. The maximum continuous output current (IOUT_LIM), prior to entering current limit operation, can be defined by:

$$I_{OUT\_LIM} = (1 - D) \times (I_{VALLEY\_LIM} + \frac{1}{2}\Delta I_L) \quad (1)$$

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \quad (2)$$

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \quad (3)$$

If the output current is further increased and the output voltage is pulled blow the input voltage, the TPS61230A enters into the hiccup protection mode. The average current and thermal will be much lowered at the hiccup steady state and the device could recovery automatically as long as the over load condition being released.

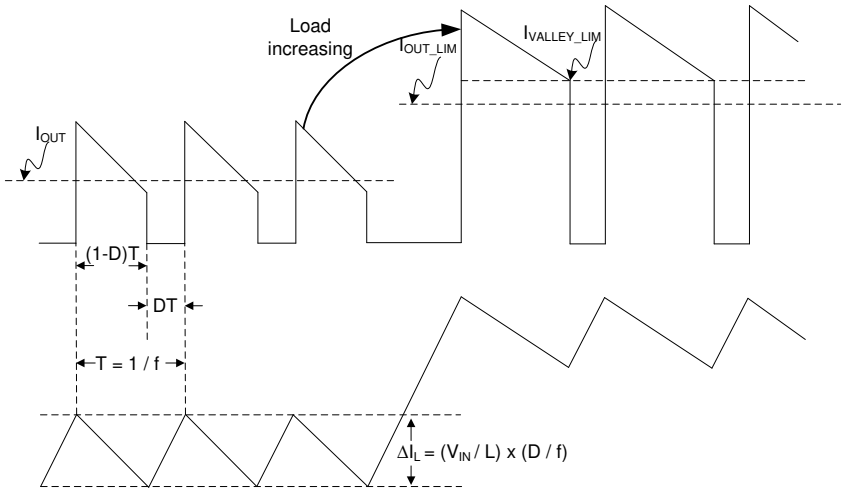


図 13. Current Limit Operation

8.3.5 Over Voltage Protection

The device stops switching as soon as the output voltage exceeds the over voltage protection (OVP) threshold. Both of the low side FET and high side FET turn off. The device resumes the normal operation when the output voltage is below the OVP threshold.

8.3.6 Load Disconnect

The TPS61230A disconnects the output from the input of the power supply when the device is shutdown. In case of a connected battery it prevents it from being discharged during the shutdown of the converter.

8.3.7 Thermal Shutdown

The TPS61230A has a built-in temperature sensor which monitors the internal junction temperature, T_J. If the junction temperature exceeds the threshold (160 °C typical), the device goes into the thermal shutdown, and the high-side and low-side FETs turn off. When the junction temperature falls below the thermal shutdown falling threshold (150 °C typical), the device resumes the operation.

8.4 Device Functional Modes

The TPS61230A has two operation modes, as shown in 表 2.

表 2. Operation Mode Description

MODE	DESCRIPTION	CONDITION
PWM	Boost in normal switching operation	Heavy load
PFM	Boost in power save operation	Light load

8.4.1 PWM Mode

The TPS61230A typically operates at a quasi-constant 1.15 MHz frequency pulse width modulation (PWM) at moderate to heavy load currents.

8.4.2 PFM Mode

The device integrates a power save mode with the pulse frequency modulation (PFM) to improve the efficiency at the light load. In the PFM mode, the device starts to switch when the output voltage trips below a set threshold voltage. When the output voltage ramping over the PFM threshold, the device stops switching. The DC output voltage in PFM mode rises above the nominal output voltage in PWM mode by 1.2%.

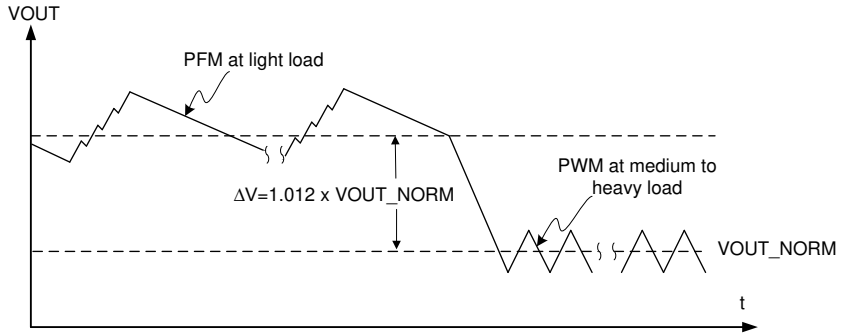


図 14. Output Voltage in PFM / PWM Mode

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS61230A is designed to operate from an input voltage supply range between 2.5 V and 4.5 V with a maximum output current of 2.4 A. The device operates in PWM mode for medium to heavy load conditions and in the PFM mode at the light load currents. In PWM mode the TPS61230A converter operates with the nominal switching frequency of 1.15 MHz which provides a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters into the PFM mode, reducing the switching frequency and minimizing the quiescent current to achieve the high efficiency over the entire load current range.

9.2 Typical Applications

9.2.1 TPS61230A 2.5-V to 4.5-V Input, 5-V Output Converter

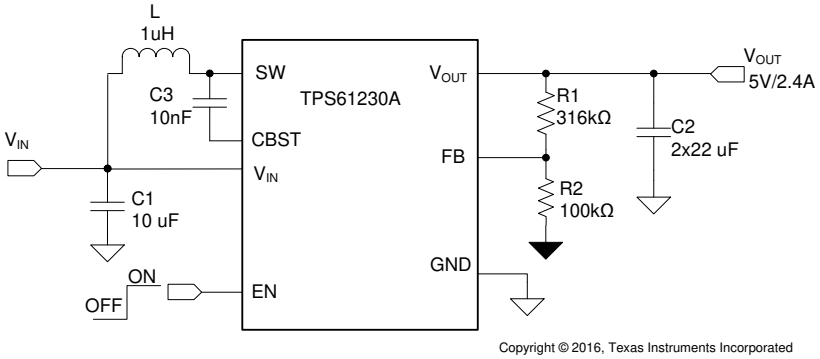


図 15. TPS61230A 5-V Output Typical Application

9.2.1.1 TPS61230A 5-V Output Design Requirements

Use the following typical application design procedure to select the external components values for the TPS61230A device.

表 3. TPS61230A 5-V Output Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.5 V to 4.5 V
Output Voltage	5.0 V
Output Voltage Ripple	+/- 3% V_{OUT}
Transient Response	+/- 10% V_{OUT}
Input Voltage Ripple	+/- 200mV
Output Current Rating	2.4 A
Operating frequency	1.15 MHz

9.2.1.2 TPS61230A 5-V Detailed Design Procedure

表 4. TPS61230A 5-V Output List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
L	1.0 μH, Power Inductor, XFL4020-102MEB	Coilcraft
CIN	22 μF 6.3V, 0805, X5R ceramic, GRM21BR61A226ME44	Murata
COUT	2 × 22 μF 10V, 0805, X5R ceramic, GRM21BR61A226ME44	Murata
CBST	10 nF, X7R ceramic	Murata
R2	316k, Resistor, Chip, 1/10W, 1%	Vishay-Dale
R1	100k,Resistor, Chip, 1/10W, 1%	Vishay-Dale

9.2.1.2.1 Programming The Output Voltage

The TPS61230A's output voltage need to be programmed via an external voltage divider to set the desired output voltage.

An external resistor divider is used, as shown in 式 4. By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is V_{FB}. The following equation can be used to calculate R1 and R2.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 1.195V \times \left(1 + \frac{R1}{R2}\right) \quad (4)$$

R2 is typically around 100kΩ to ensure that the current following through R2 is at least 100 times larger than FB pin leakage current. Changing R2 towards a lower value increases the robustness against noise injection. Changing the R2 towards higher values reduces the quiescent current for achieving highest efficiency at low load currents.

For the fixed output voltage version, the FB pin must be tied to the output directly.

9.2.1.2.2 Inductor and Capacitor Selection

The second step is the selection of the inductor and capacitor components.

9.2.1.2.2.1 Inductor Selection

A boost converter requires two main passive components for storing energy during the conversion, an inductor and an output capacitor. It is advisable to select an inductor with a saturation current rating higher than the possible peak current flowing through the power FETs. The inductor peak current varies as a function of the load, the input and output voltages and is estimated using 式 5.

$$I_{L(PEAK)} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \quad (5)$$

Where

η = Power conversion estimated efficiency

Selecting an inductor with the insufficient saturation performance can lead to the excessive peak current in the converter. This could eventually harm the device and reduce reliability. It's recommended to choose the saturation current for the inductor 20%~30% higher than the $I_{L(PEAK)}$, from 式 5. The following inductors are recommended to be used in designs.

表 5. List of Inductors

INDUCTANCE [μH]	CURRENT RATING [A]	DC RESISTANCE [mΩ]	PART NUMBER	MANUFACTURER
1.0	9.0	12	744 383 560 10	Wurth
1.0	5.1	10.8	XFL4020-102MEB	Coilcraft

9.2.1.2.2.2 Output Capacitor Selection

For the output capacitor, it is recommended to use small X5R or X7R ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor of 1 µF in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

Care must be taken when evaluating a capacitor's derating under bias. The bias can significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

The ESR impact on the output ripple must be considered as well, if tantalum or electrolytic capacitors are used. Assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the V_{Ripple} is:

$$V_{Ripple(ESR)} = I_{L(PEAK)} \times ESR \quad (6)$$

9.2.1.2.2.3 Input Capacitor Selection

Multilayer X5R or X7R ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 10 µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_{IN} and the power source to reduce the ringing that can occur between the inductance of the power source leads and C_{IN}.

9.2.1.2.3 Loop Stability, Feed Forward Capacitor

The third step is to check the loop stability. The stability evaluation is to look from a steady-state perspective at the following signals:

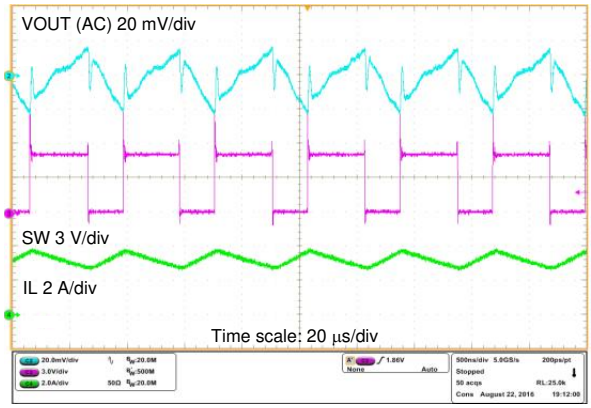
- Switching node, SW
- Inductor current, I_L
- Output ripple, $V_{Ripple(OUT)}$

When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

The load transient response is another approach to check the loop stability. During the load transient recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

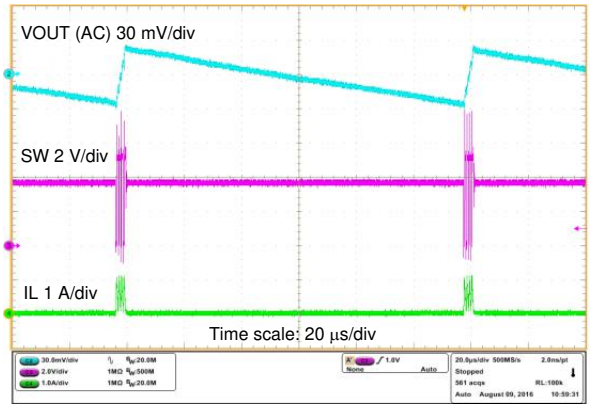
As for the heavy load transient applications such as a 2 A load step transient, a feed forward capacitor in parallel with R1 is recommended. The feed forward capacitor increases the loop bandwidth by adding a zero.

9.2.1.3 TPS61230A 5-V Output Application Performance Plots



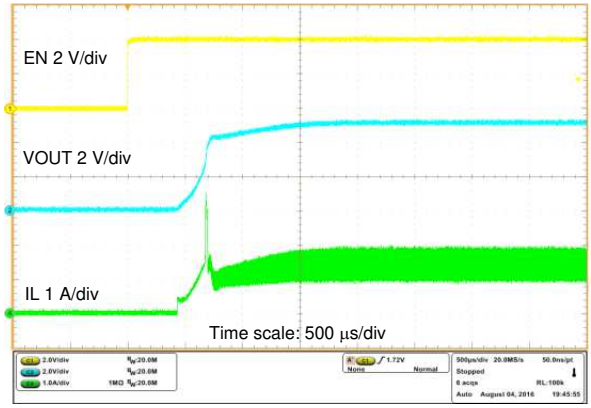
V_{OUT} = 5 V, V_{IN} = 3.6 V, I_{OUT} = 2 A, T_A = 25 ºC, L = 1 µH, C_{OUT} = 2x22 µF

図 16. Steady State Switching at PWM



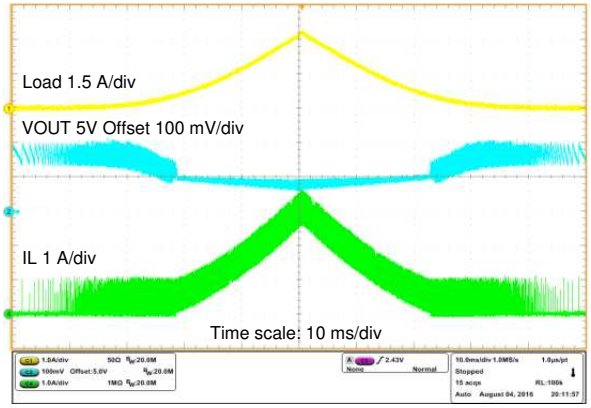
V_{OUT} = 5 V, V_{IN} = 3.6 V, I_{OUT} = 10 mA, T_A = 25 ºC

図 17. Steady State Switching at PFM



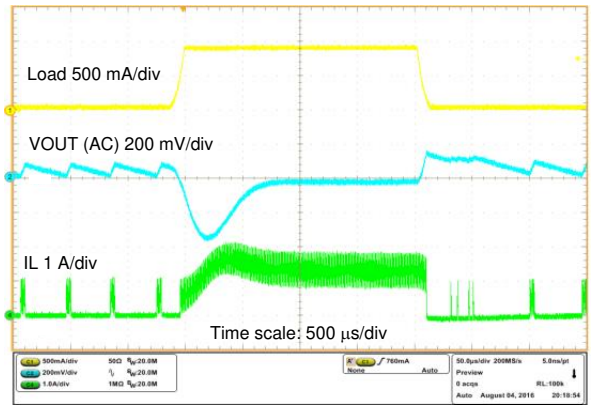
V_{OUT} = 5 V, V_{IN} = 3.6 V, R_{OUT} = 5 Ω, T_A = 25 ºC

図 18. Startup by EN



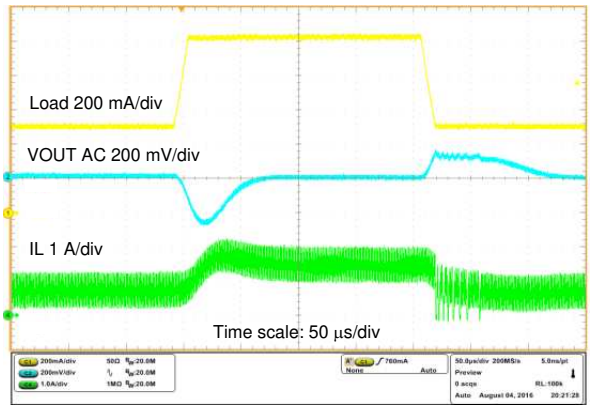
V_{OUT} = 5 V, V_{IN} = 3.6 V, I_{OUT} = 0 - 2 A Sweep, T_A = 25 ºC

図 19. Load Sweep



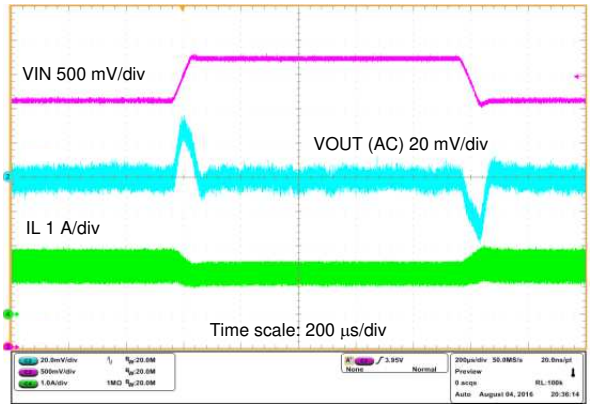
V_{OUT} = 5 V, V_{IN} = 3.6 V, I_{OUT} = 0.1 - 1 A with 10 µs slew rate, T_A = 25 ºC

図 20. Load Transient PFM / PWM



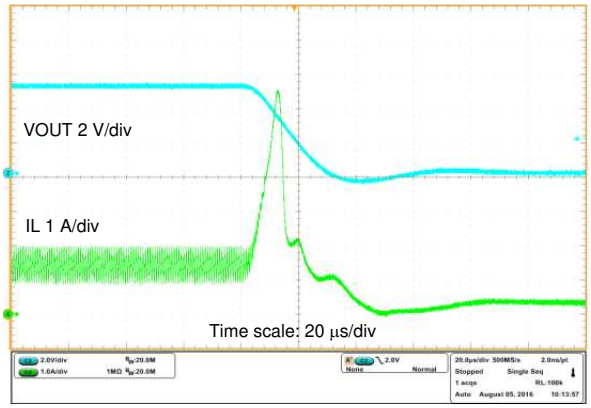
V_{OUT} = 5 V, V_{IN} = 3.6 V, I_{OUT} = 0.5 - 1 A with 10 µs slew rate, T_A = 25 ºC

図 21. Load Transient PWM



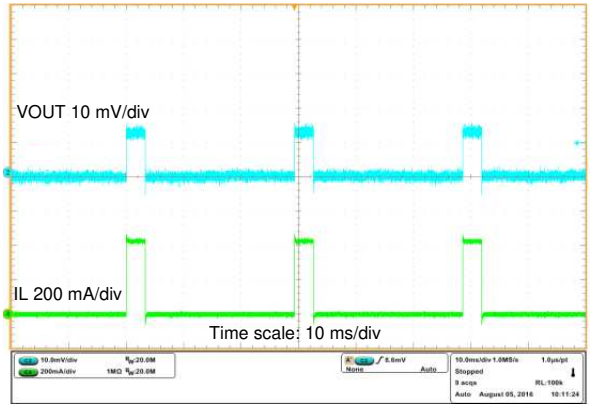
V_{OUT} = 5 V, V_{IN} = 3.6 - 4.2 V, Slew rate 50 µs, I_{OUT} = 1 A, T_A = 25 ºC

図 22. Line Transient



V_{OUT} = 5 V, V_{IN} = 3.6 V, I_{OUT} = 1 A before short, T_A = 25 ºC

図 23. Output Short Entry



V_{OUT} = 5 V, V_{IN} = 3.6 V, I_{OUT} short, T_A = 25 ºC

図 24. Output Short Steady State

9.2.2 Systems Example - TPS61230A with Feed Forward Capacitor for Best Transient Response

As for the heavy load transient applications such as a 2 A load step transient, a feed forward capacitor in parallel with R1 is recommended. The feed forward capacitor increases the loop bandwidth by adding a zero. This results in a lower output voltage drop, as shown in . See Application Note SLVA289.for the feed forward capacitor selection.

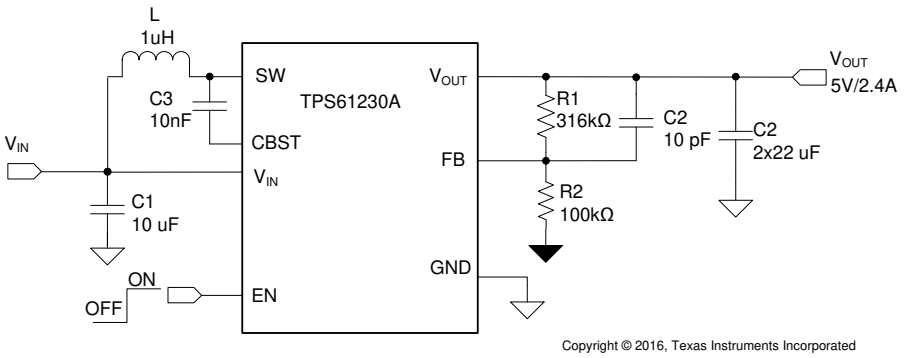


図 25. TPS61230A 5-V Output with Cff Typical Application

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 4.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 μF is a typical choice.

11 Layout

11.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at the GND pin of the IC. The most critical current path for all boost converters is from the switching FET, through the synchronous FET, then the output capacitors, and back to ground of the switching FET. Therefore, the output capacitors and their traces should be placed on the same board layer as the IC and as close as possible between the IC's VOUT and GND pin.

See 図 26 for the recommended layout.

11.2 Layout Example

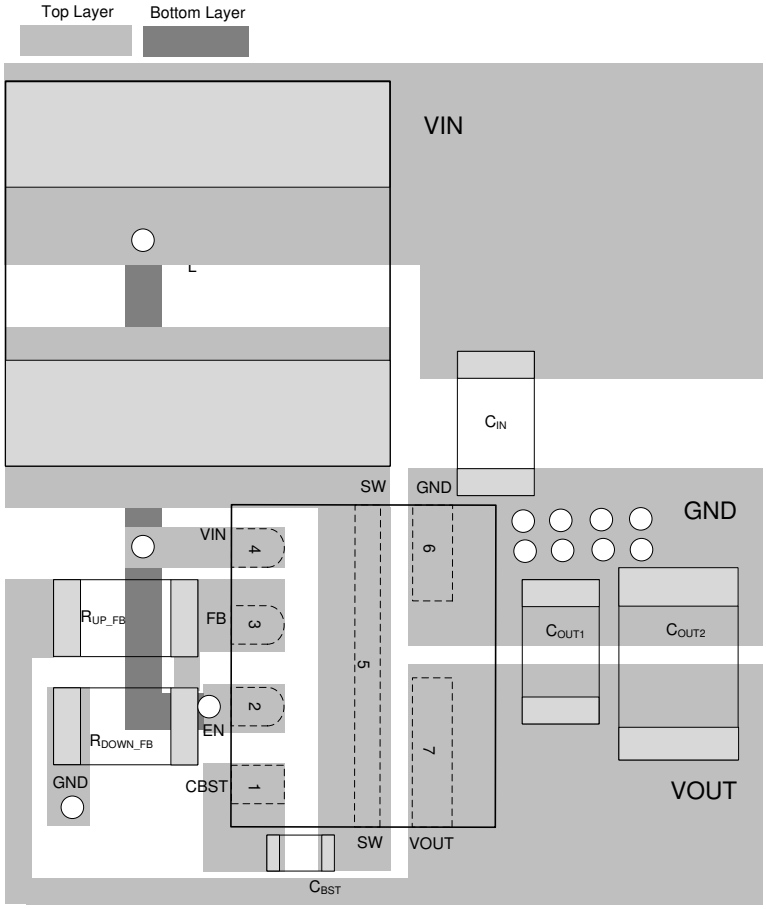


図 26. Layout Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the *Thermal Characteristics Application Note* (SZZA017) and the *IC Package Thermal Metrics Application Note* (SPRA953).

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

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12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- 『熱特性についてのアプリケーション・ノート』(SZZA017)
- 『ICパッケージの熱指標についてのアプリケーション・ノート』(SPRA953)

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61230ARNSR	Active	Production	VQFN-HR (RNS) | 7	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	12EI
TPS61230ARNSR.A	Active	Production	VQFN-HR (RNS) | 7	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	12EI
TPS61230ARNST	Active	Production	VQFN-HR (RNS) | 7	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	12EI
TPS61230ARNST.A	Active	Production	VQFN-HR (RNS) | 7	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	12EI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

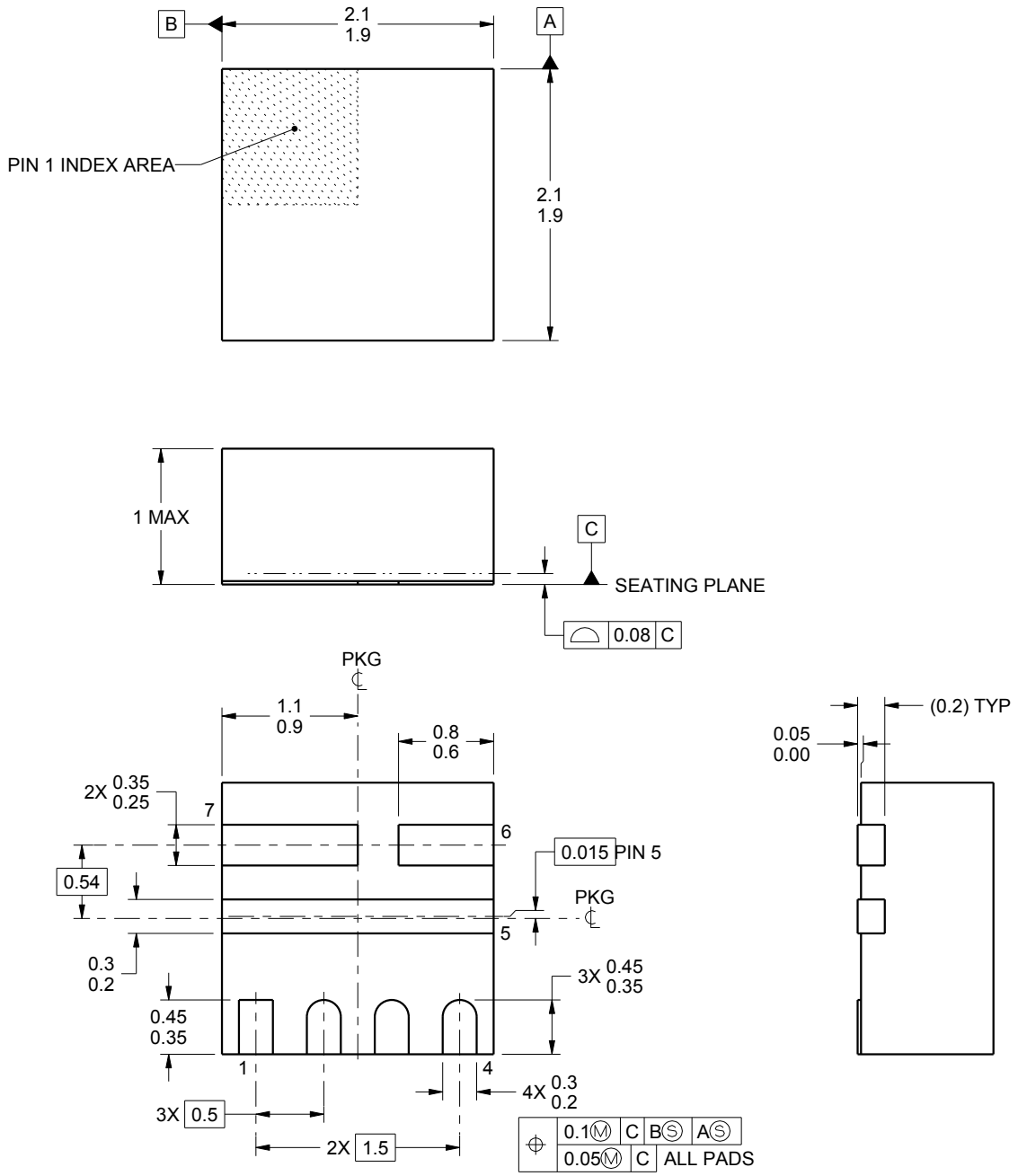
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

RNS0007A

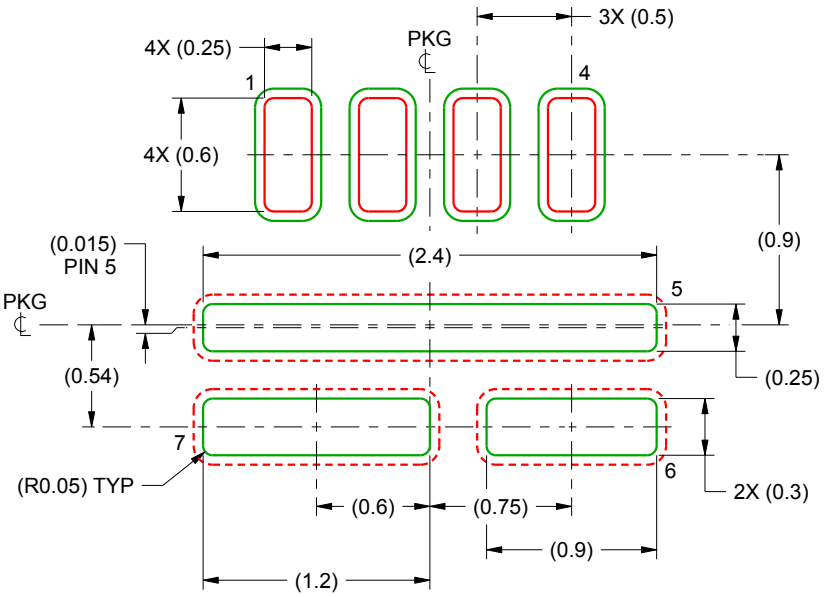
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

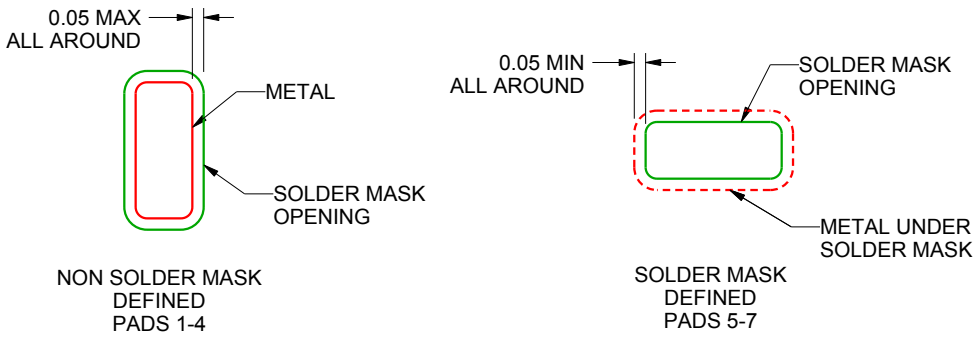


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X

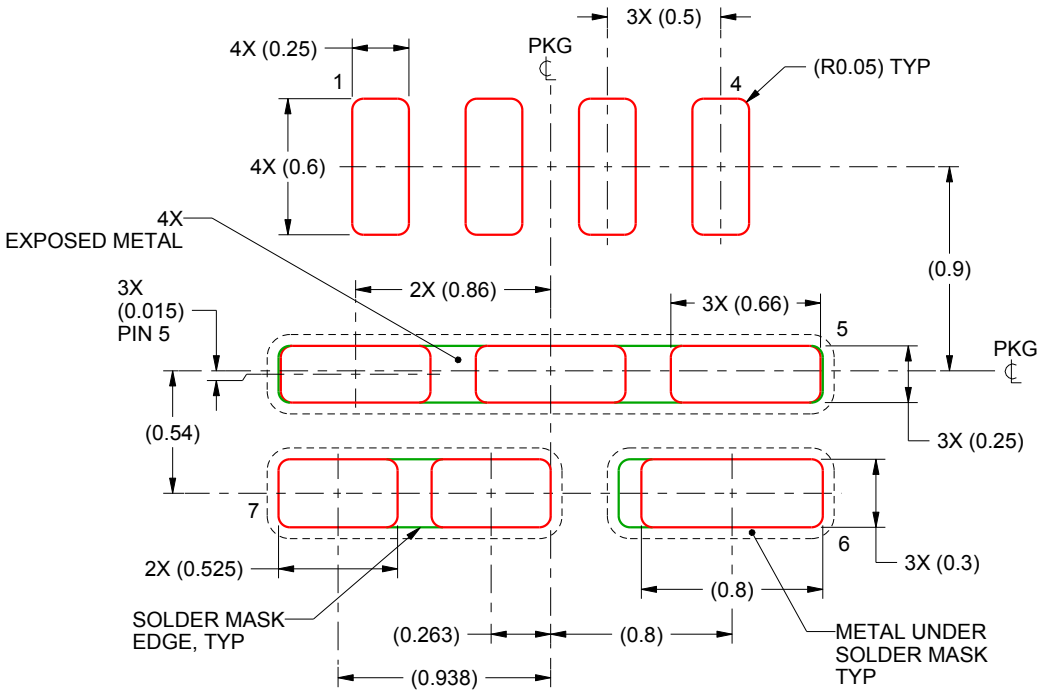


SOLDER MASK DETAILS

4222253/A 09/2015

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 5: 79%, PADS 6 & 7: 85%
SCALE:30X

4222253/A 09/2015

NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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