TPS57112C-Q1 車載用 2.95V～6V、2A、2MHz 同期整流降圧コンバータ

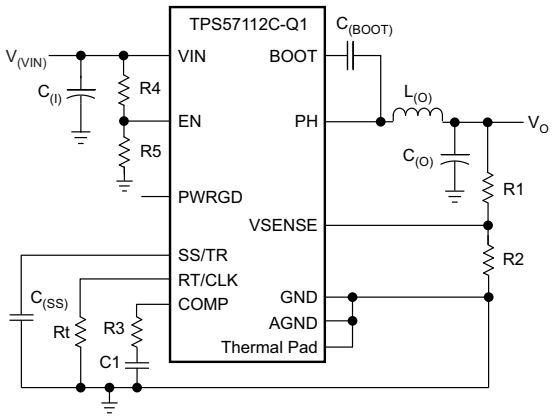
1 特長

- 車載アプリケーション用に認定済み
- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1:動作時周囲温度範囲 –40°C～+125°C
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C3B
- 2 個の 12mΩ (標準値) MOSFET により 2A の負荷で高効率を実現
- 200kHz～2MHz のスイッチング周波数
- -40℃～+150℃の温度範囲全体で 0.8V ± 1% の基準電圧
- 外部クロックに同期
- 調整可能なスロー・スタートとシーケンシング
- UV および OV のパワー・グッド出力
- 動作時の接合部温度範囲：-40℃～+150°C
- 熱的に強化された 3mm × 3mm の 16 ピン WQFN
- TPS54418 とピン互換

2 アプリケーション

- インフォテインメント用ヘッド・ユニット
- ハイブリッド・インストルメント・クラスタ
- テレマティクス制御ユニット
- ADAS カメラ・モジュール
- 高性能 DSP、FPGA、ASIC、マイクロプロセッサのポイント・オブ・ロード・レギュレーション

概略回路図



3 概要

TPS57112C-Q1 は 2 個の MOSFET を内蔵した、フル機能の 6V、2A 同期整流降圧型電流モード・コンバータです。

TPS57112C-Q1 は MOSFET を内蔵し、電流モード制御の実装により外付け部品数が少なく、スイッチング周波数が最高 2MHz と高いためインダクタを小さくでき、熱的に強化された小型 (3mm × 3mm) の QFN パッケージにより IC の占有面積を最小化できるため、小型の設計を実現できます。

TPS57112C-Q1 は、温度範囲全体で精度 ±1% の基準電圧 (V_{ref}) により、各種の負荷に対して正確なレギュレーションを行います。

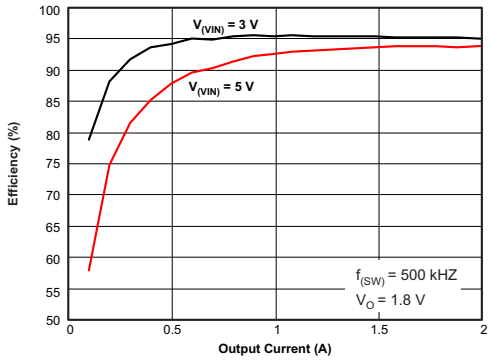
内蔵の 12mΩ MOSFET と 515µA (標準値) の消費電流により、効率を最大化できます。イネーブル・ピンを使用してシャットダウン・モードに移行すると、消費電流を 5.5µA (標準値) に低減できます。

製品情報

型番	パッケージ	本体サイズ(公称)
TPS57112C-Q1	WQFN (16)	3.00mm×3.00mm

1. 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

効率と出力電流との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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5 概要（続き）

内部の低電圧誤動作防止設定は 2.45V ですが、イネーブル・ピンの抵抗回路でスレッショルドをプログラムすることにより、設定値を高くできます。スロースタート・ピンで、出力電圧のスタートアップ・ランプを制御できます。オープン・ドレインのパワー・グッド信号は、出力が公称電圧の 93%～107% の範囲内にあることを示します。

周波数のフォールドバックとサーマル・シャットダウンにより、過電流時にデバイスが保護されます。

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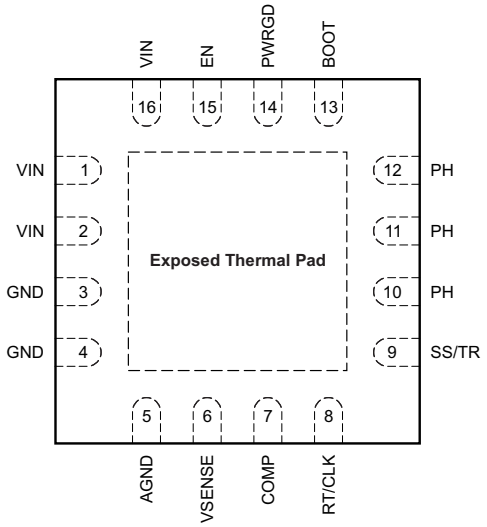
6 Pin Configuration and Functions

RTE Package
16-Pin WQFN With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	5	—	Connect analog ground electrically to GND close to the device.
BOOT	13	O	There is a requirement for a bootstrap capacitor between BOOT and PH. A voltage on this capacitor that is below the minimum required by the BOOT UVLO forces the output to switch off until the capacitor recharges.
COMP	7	O	Error amplifier output, and input to the output-switch current comparator. Connect frequency-compensation components to this pin.
EN	15	I	Enable pin, internal pullup current source. Pull below 1.2 V to disable. Float to enable. One can use this pin to set the on-off threshold (adjust UVLO) with two additional resistors.
GND	3	—	Power ground. Connect this pin electrically to the thermal pad directly under the IC.
	4		
PH	10	O	The source of the internal high-side power MOSFET, and drain of the internal low-side (synchronous) rectifier MOSFET.
	11		
	12		
PWRGD	14	O	An open-drain output; asserts low if output voltage is low due to thermal shutdown, overcurrent, overvoltage, undervoltage, or EN shutdown.
RT/CLK	8	I	Resistor-timing or external-clock input pin
SS/TR	9	I	Slow-start and tracking. An external capacitor connected to this pin sets the output-voltage rise time. Another use of this pin is for tracking.
VIN	1	I	Input supply voltage, 2.95 V to 6 V.
	2		
	16		
VSENSE	6	I	Inverting node of the transconductance (g_m) error amplifier
Thermal pad		—	Connect the GND pin to the exposed thermal pad for proper operation. Connect this thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.

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7 Specifications

7.1 Absolute Maximum Ratings

See [1]

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	7	V
	EN	–0.3	7	
	BOOT	–0.3	PH + 7	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	7	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	7	
Output voltage	BOOT-PH	–0.3	7	V
	PH	–0.6	7	
	PH 10-ns transient	–2	10	
Source current	EN		100	µA
	RT/CLK		100	
Sink current	COMP		100	µA
	PWRGD		10	mA
	SS/TR		100	µA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, 8, 9, 12, 13, 16)	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{(VIN)}$	Input voltage	2.95		6	V
T_A	Operating ambient temperature	–40		125	°C

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7.4 Thermal Information

THERMAL METRIC[1]		TPS57112C-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.8	°C/W
$R_{\theta JC(top)}$	Junction-to-ambient thermal resistance	46.1	°C/W
$R_{\theta JB}$	Junction-to-top characterization parameter	15.5	°C/W
ψ_{JT}	Junction-to-board characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-case(top) thermal resistance	15.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = –40°C to +150°C, VIN = 2.95 V to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Internal undervoltage lockout threshold	VIN UVLO START (output turns on, device starts switching)		2.45	2.6	V
	VIN UVLO STOP (output turns off, device stops switching)		2.28	2.5	
Shutdown supply current	$V_{(EN)}$ = 0 V, 25°C, 2.95 V ≤ $V_{(VIN)}$ ≤ 6 V		5.5	15	µA
Quiescent current – $I_{(q)}$	$V_{(VSENSE)}$ = 0.9 V, $V_{(VIN)}$ = 5 V, 25°C, Rt = 400 kΩ		515	750	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.25		V
	Falling		1.18		
Input current	Enable threshold + 50 mV		–3.2		µA
	Enable threshold – 50 mV		–1.65		
VOLTAGE REFERENCE (VSENSE PIN)					
Voltage reference	2.95 V ≤ $V_{(VIN)}$ ≤ 6 V, –40°C < T_J < +150°C	0.79	0.8	0.811	V
MOSFET					
High-side switch resistance	BOOT-PH = 5 V		12	30	mΩ
	BOOT-PH = 2.95 V		16	30	
Low-side switch resistance	$V_{(VIN)}$ = 5 V		13	30	mΩ
	$V_{(VIN)}$ = 2.95 V		17	30	
ERROR AMPLIFIER					
Input current			2		nA
Error amplifier transconductance (g_m)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		245		µS
Error amplifier transconductance (g_m) during slow start	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V, $V_{(VSENSE)}$ = 0.4 V		79		µS
Error amplifier source or sink	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±20		µA
COMP to high-side FET current g_m			14		S
CURRENT LIMIT					
Current-limit threshold		2.9	5.3		A
THERMAL SHUTDOWN					
Thermal shutdown			168		°C
Hysteresis			20		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Switching frequency range using Rt mode		200		2000	kHz
Switching frequency	Rt = 400 kΩ	400	500	600	kHz

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Electrical Characteristics (continued)

T_J = –40°C to +150°C, VIN = 2.95 V to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching frequency range using CLK mode		300		2000	kHz
RT/CLK voltage	Rt = 400 kΩ		0.5		V
RT/CLK high threshold			1.6	2.5	V
Delay from RT/CLK falling edge to PH rising edge	Measure at 500 kHz with Rt resistor in series with device pin		90		ns
BOOT (BOOT PIN)					
BOOT charge resistance	$V_{(VIN)}$ = 5 V		16		Ω
BOOT-PH UVLO	$V_{(VIN)}$ = 2.95 V		2.1		V
SLOW START AND TRACKING (SS/TR PIN)					
Charge current	$V_{(SS/TR)}$ = 0.4 V		2		µA
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.4 V		54		mV
SS/TR to reference crossover	98% of nominal reference voltage		1.1		V
SS/TR discharge voltage (overload)	$V_{(VSENSE)}$ = 0 V		60		mV
SS/TR discharge current (overload)	$V_{(VSENSE)}$ = 0 V, $V_{(SS/TR)}$ = 0.4 V		350		µA
SS discharge current (UVLO, EN, thermal fault)	$V_{(VIN)}$ = 5 V, $V_{(SS/TR)}$ = 0.5 V		1.9		mA
POWER GOOD (PWRGD PIN)					
VSENSE threshold	$V_{(VSENSE)}$ falling (Fault)		91		$\%V_{ref}$
	$V_{(VSENSE)}$ rising (Good)		93		
	$V_{(VSENSE)}$ rising (Fault)		109		
	$V_{(VSENSE)}$ falling (Good)		107		
Hysteresis	$V_{(VSENSE)}$ falling		2		$\%V_{ref}$
Output-high leakage	$V_{(VSENSE)} = V_{ref}$, $V_{(PWRGD)}$ = 5.5 V		7		nA
On-resistance			56	100	Ω
Output low	$I_{(PWRGD)}$ = 3 mA		0.3		V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		0.65	1.5	V

7.6 Timing Requirements

T_J = –40°C to +150°C, VIN = 2.95 V to 6 V (unless otherwise noted)

	MIN	NOM	MAX	UNIT
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)				
Minimum CLK pulse duration	75			ns

7.7 Switching Characteristics

T_J = –40°C to +150°C, V_{IN} = 2.95 V to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
RT/CLK low threshold		0.4	0.6		V
PLL lock-in time	Measure at 500 kHz		42		µs
PH (PH PIN)					
Minimum on-time	Measured at 50% points on PH, I_O = 2 A		75		ns
	Measured at 50% points on PH, $V_{(VIN)}$ = 6 V, I_O = 0 A		120		
Minimum off-time	Prior to skipping off pulses, BOOT-PH = 2.95 V, I_O = 2 A		60		ns
Rise time	$V_{(VIN)}$ = 6 V, I_O = 2 A		2.25		V/ns
Fall time	$V_{(VIN)}$ = 6 V, I_O = 2 A		2		V/ns

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7.8 Typical Characteristics Curves

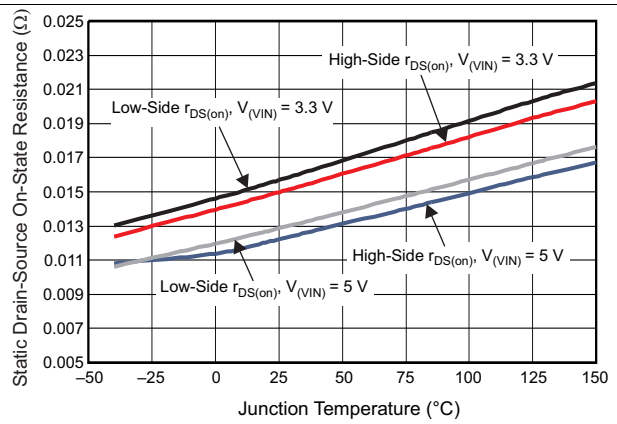

図 1. High-Side and Low-Side $r_{DS(on)}$ versus Temperature

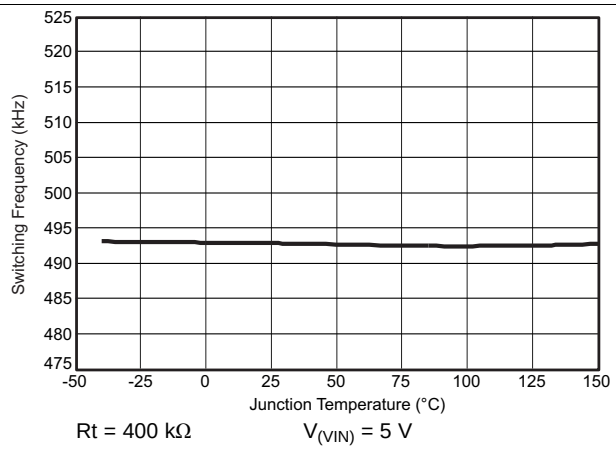

図 2. Frequency versus Temperature

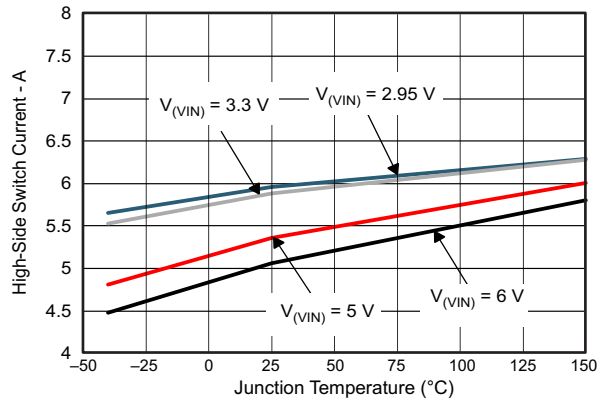

図 3. High-Side Current-Limit versus Temperature

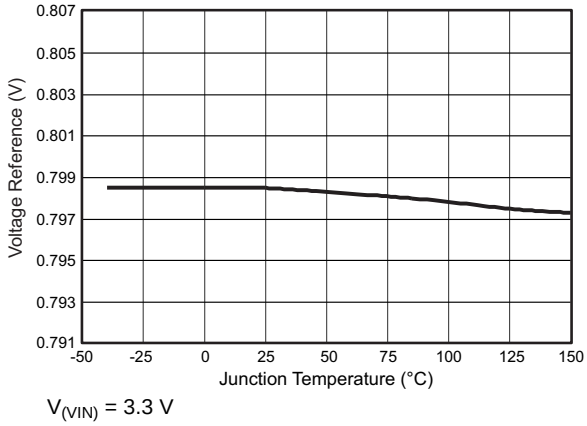

図 4. Voltage Reference versus Temperature

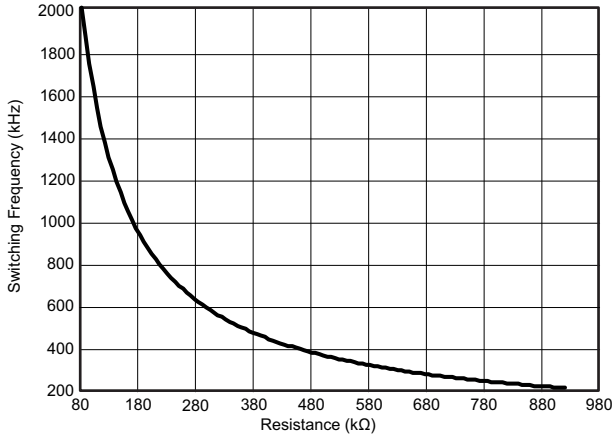

図 5. Switching Frequency versus Rt Resistance, Low-Frequency Range

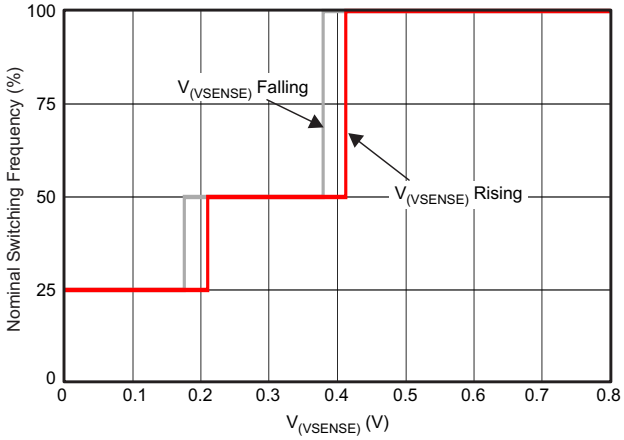

図 6. Switching Frequency versus VSENSE

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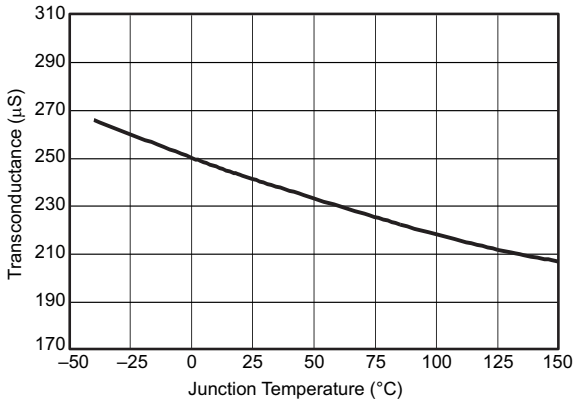
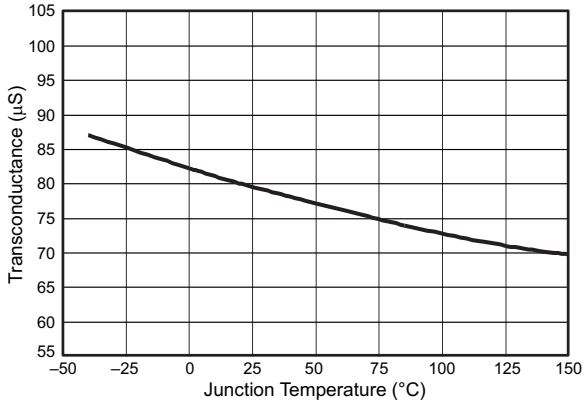
Typical Characteristics Curves (continued)



$V_{(VIN)}$ = 3.3 V

図 7. Transconductance versus Temperature



$V_{(VIN)}$ = 3.3 V

図 8. Transconductance (Slow Start) versus Junction Temperature

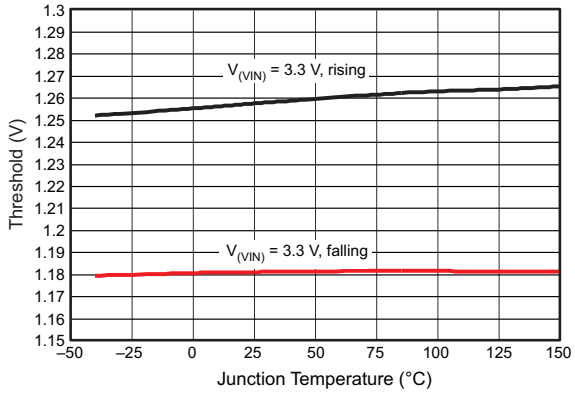
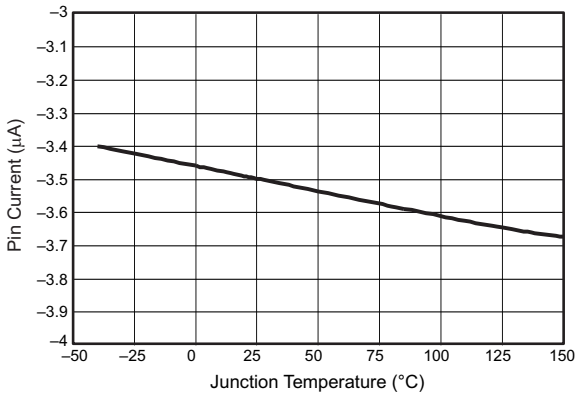
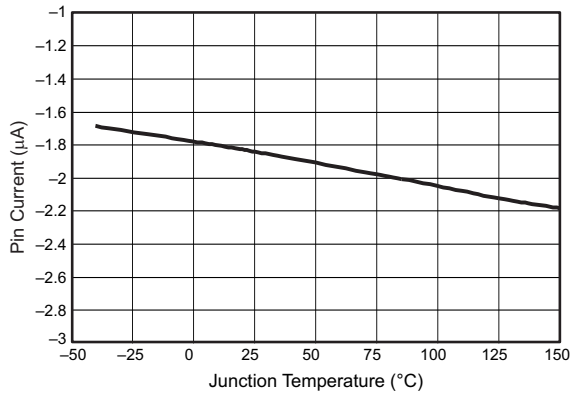


図 9. EN Pin Voltage versus Temperature



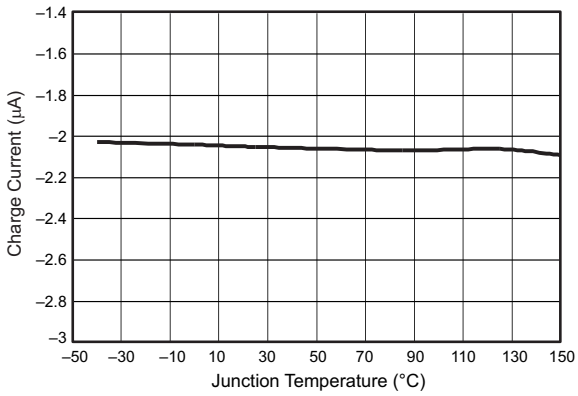
$V_{(VIN)}$ = 5 V $V_{(EN)}$ = Threshold + 50 mV

図 10. EN Pin Current versus Temperature



$V_{(VIN)}$ = 5 V $V_{(EN)}$ = Threshold – 50 mV

図 11. EN Pin Current versus Temperature



$V_{(VIN)}$ = 5 V

図 12. Charge Current versus Temperature

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Typical Characteristics Curves (continued)

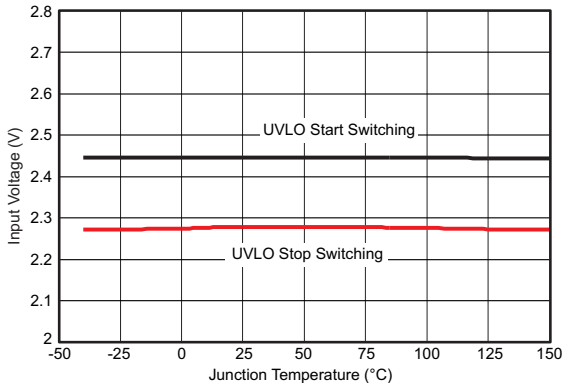
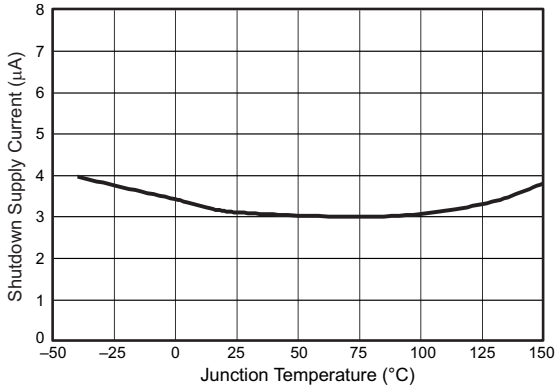
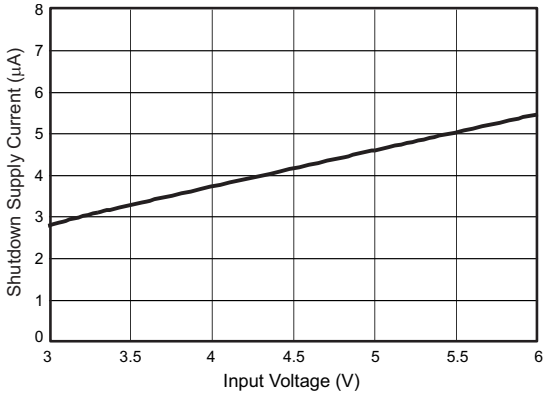


図 13. Input Voltage versus Temperature



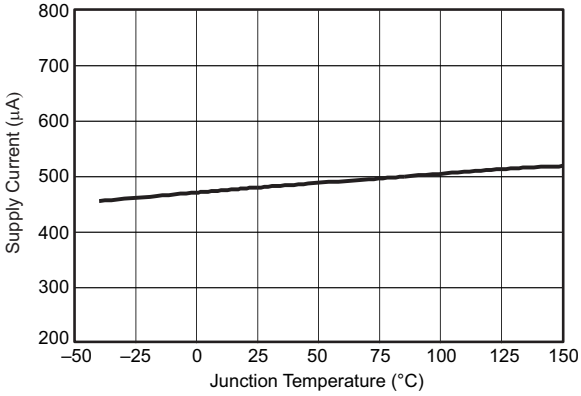
$V_{(VIN)}$ = 3.3 V

図 14. Shutdown Supply Current versus Temperature



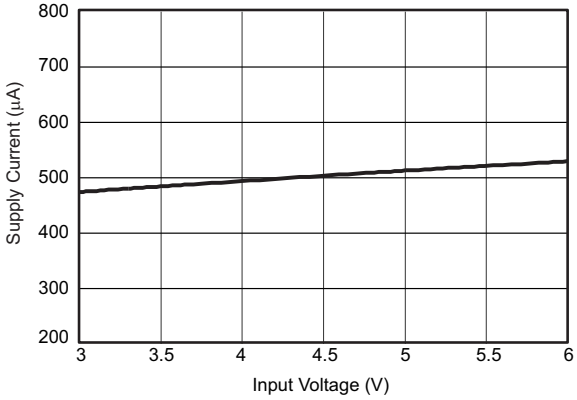
T_J = 25ºC

図 15. Shutdown Supply Current versus Input Voltage



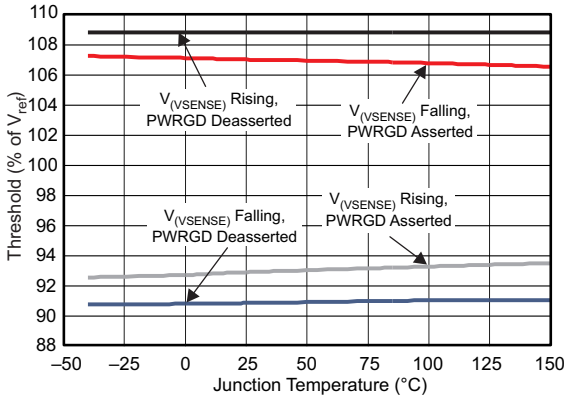
$V_{(VIN)}$ = 3.3 V

図 16. VIN Supply Current versus Junction Temperature



T_J = 25ºC

図 17. VIN Supply Current versus Input Voltage



$V_{(VIN)}$ = 5 V

図 18. PWRGD Threshold versus Temperature

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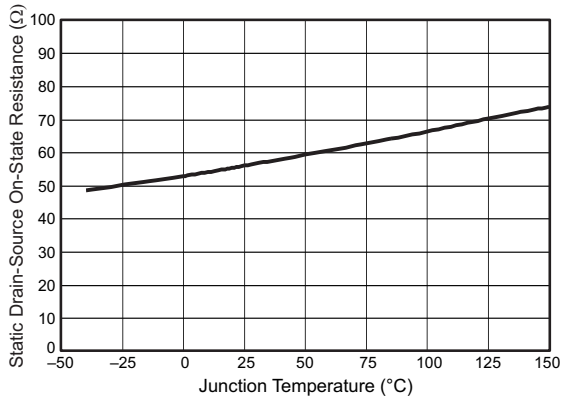
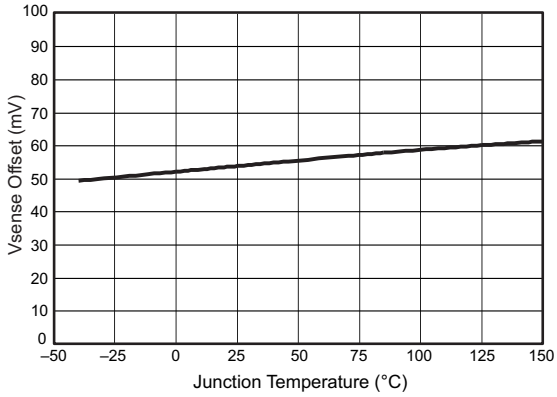
Typical Characteristics Curves (continued)



$V_{(VIN)}$ = 5 V

図 19. PWRGD On-Resistance versus Temperature



$V_{(VIN)}$ = 5 V $V_{(SS/TR)}$ = 0.4 V

図 20. SS/TR-to-VSENSE Offset versus Temperature

8 Detailed Description

8.1 Overview

The TPS57112C-Q1 device is a 6-V, 2-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant-frequency, peak-current-mode control which reduces output capacitance and simplifies external frequency-compensation design. The wide switching-frequency range of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output-filter components. The switching-frequency adjustment uses a resistor to ground on the RT/CLK pin. The device has an internal phase-lock loop (PLL) on the RT/CLK pin that synchronizes the power-switch turnon to the falling edge of an external system clock.

The TPS57112C-Q1 device has a typical default start-up voltage of 2.45 V. The EN pin has an internal pullup current source that one can use to adjust the undervoltage lockout (UVLO) of the input voltage with two external resistors. In addition, the pullup current provides a default condition that allows the device to operate when the EN pin is floating. The total operating current for the TPS57112C-Q1 device is typically 515 μA when not switching and under no load. When the device is disabled, the supply current is typically 5.5 μA.

The integrated 12-mΩ MOSFETs allow for high-efficiency power-supply designs with continuous output currents up to 2 A.

The TPS57112C-Q1 device reduces the external component count by integrating the boot recharge diode. The bias-voltage supply for the integrated high-side MOSFET is from a capacitor between the BOOT and PH pins. A UVLO circuit monitors the boot-capacitor voltage and turns off the high-side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS57112C-Q1 device to operate approaching 100% duty cycle. The lower limit for stepping down the output voltage is the 0.8-V reference.

The TPS57112C-Q1 device has a power-good comparator (PWRGD) with 2% hysteresis.

The TPS57112C-Q1 device minimizes excessive output overvoltage transients by taking advantage of the overvoltage power-good comparator. The regulated output voltage exceeding 109% of the nominal voltage activates the overvoltage comparator, turning off the high-side MOSFET and masking it from turning on until the output voltage is lower than 107% of the nominal voltage.

A use of the SS/TR (slow-start or tracking) pin is to minimize inrush currents or provide power-supply sequencing during power up. Couple a small-value capacitor to the pin for slow start. The SS/TR pin discharges before the output power up to ensure a repeatable restart after an overtemperature fault, UVLO fault, or disabled condition.

The use of a frequency foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help limit the inductor current.

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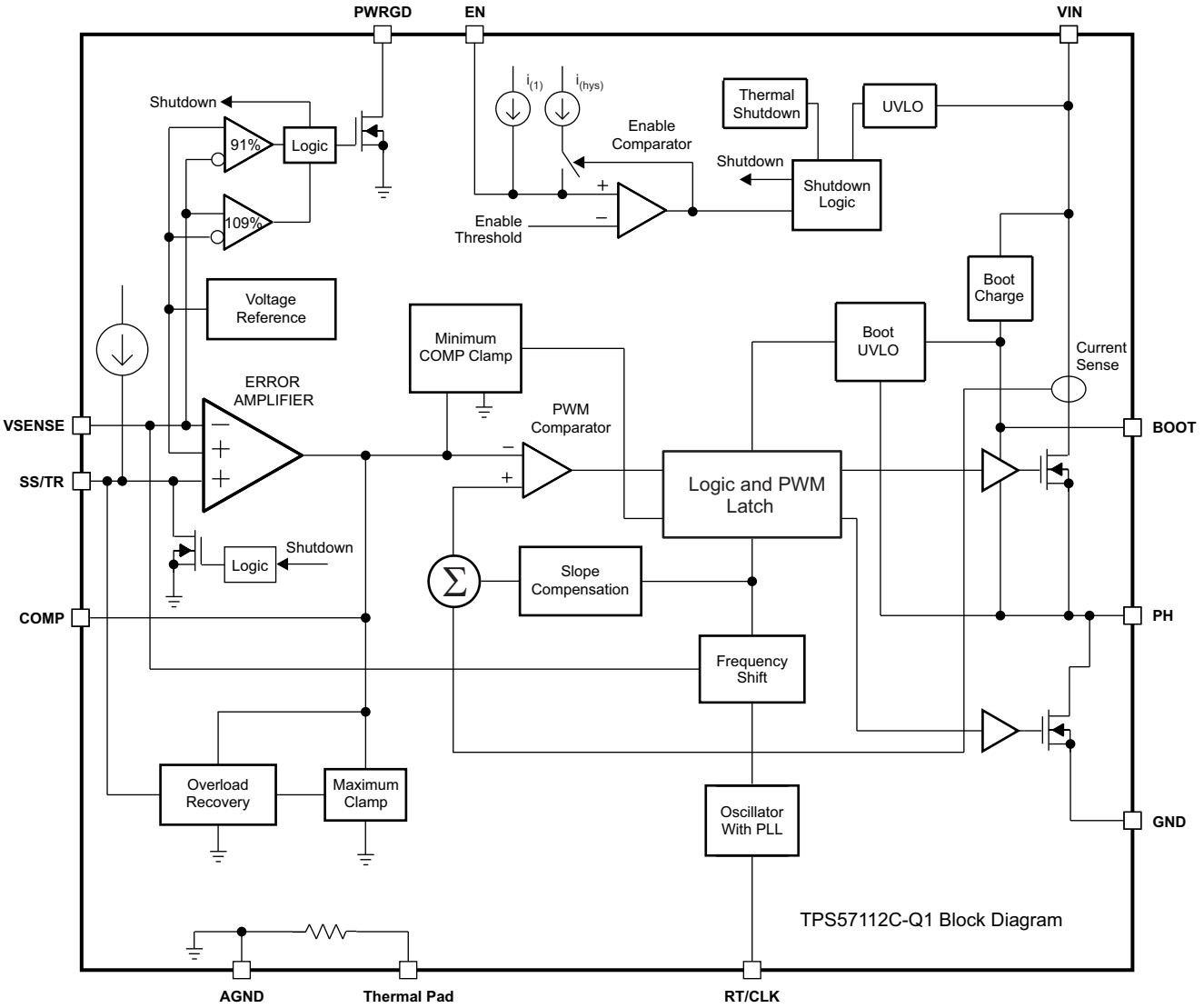
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed-Frequency PWM Control

The TPS57112C-Q1 device uses an adjustable fixed-frequency peak-current-mode control. External resistors on the VSENSE pin compare the output voltage to an internal voltage reference by an error amplifier that drives the COMP pin. An internal oscillator initiates the turnon of the high-side power switch. The device performs a comparison of the error-amplifier output to the high-side power-switch current. When the power-switch current reaches the COMP voltage level, the high-side power switch turns off and the low-side power switch turns on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level, and also implements a minimum clamp for improved transient-response performance.

8.3.2 Slope Compensation and Output Current

The TPS57112C-Q1 device adds a compensating ramp to the switch-current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

Feature Description (continued)

8.3.3 Bootstrap Voltage (BOOT) and Low-Dropout Operation

The TPS57112C-Q1 device has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 μF. TI recommends a ceramic capacitor with a voltage rating of 10 V or higher, and an X7R or X5R grade dielectric because of the stable characteristics over temperature and voltage.

To improve dropout, the TPS57112C-Q1 device operates at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.2 V. A UVLO circuit turns off the high-side MOSFET, allowing for the low-side MOSFET to conduct when the voltage from BOOT to PH drops below 2.2 V. Because the supply current sourced from the BOOT pin is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor; thus, the effective duty cycle of the switching regulator is high.

8.3.3.1 Error Amplifier

The TPS57112C-Q1 device has a transconductance amplifier that it uses as its error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance of the error amplifier is 245 μS during normal operation. When the voltage of the VSENSE pin is below 0.8 V and the device is regulating using the SS/TR voltage, the g_m is typically greater than 79 μS, but less than 245 μS. Placement of the frequency-compensation components is between the COMP pin and ground.

8.3.4 Voltage Reference

The voltage-reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature-stable band-gap circuit. The band-gap and scaling circuits produce 0.8 V at the non-inverting input of the error amplifier.

8.4 Device Functional Modes

8.4.1 Adjusting the Output Voltage

A resistor divider from the output node to the VSENSE pin sets the output voltage. TI recommends using divider resistors with 1% tolerance or better. Start with 100 kΩ for the R1 resistor and use 式 1 to calculate R2. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the VSENSE input current are noticeable.

$$R2 = R1 \times \left(\frac{0.8\ V}{V_O - 0.8\ V} \right) \tag{1}$$

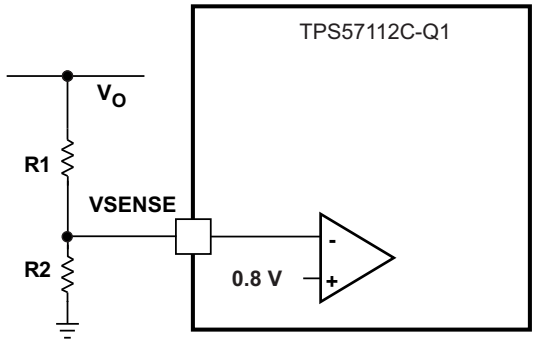


図 21. Voltage-Divider Circuit

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Device Functional Modes (continued)

8.4.2 Enable Functionality and Adjusting Undervoltage Lockout

The VIN pin voltage falling below 2.6 V disables the TPS57112C-Q1 device. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in to adjust the input voltage UVLO by using two external resistors. TI recommends using the EN resistors to set the UVLO falling threshold (V_{STOP}) above 2.6 V. Set the rising threshold (V_{START}) to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pullup current source that provides the default condition of the TPS57112C-Q1 device operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 1.6 μA of hysteresis is added. Pulling the EN pin below 1.18 V removes the 1.6 μA. This additional current facilitates input voltage hysteresis.

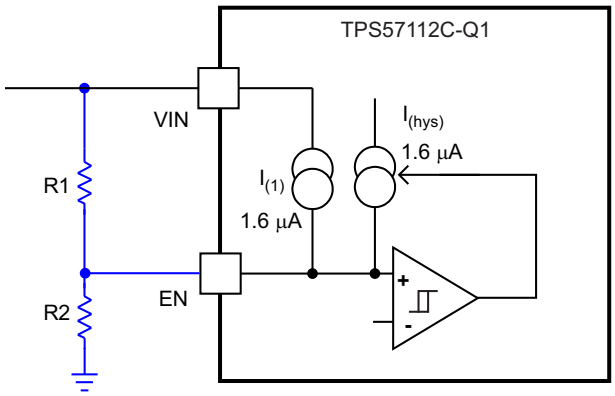

図 22. Adjustable Undervoltage Lockout

$$R1 = \frac{V_{(START)}\left(\frac{V_{(ENFALLING)}}{V_{(ENRISING)}}\right) - V_{(STOP)}}{I_{(1)}\left(1 - \frac{V_{(ENFALLING)}}{V_{(ENRISING)}}\right) + I_{(hys)}}$$

$$R2 = \frac{R1 \times V_{(ENFALLING)}}{V_{(STOP)} - V_{(ENFALLING)} + R1 \times (I_{(1)} + I_{(hys)})} \quad (2)$$

where

- $I_{(hys)}$ = 1.6 μA
- $I_{(1)}$ = 1.6 μA
- $V_{(ENRISING)}$ = 1.25 V
- $V_{(ENFALLING)}$ = 1.18 V (3)

8.4.3 Slow-Start or Tracking Pin

The TPS57112C-Q1 device regulates to the lower of the SS/TR pin or the internal reference voltage. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS57112C-Q1 device has an internal pullup current source of 2 μA that charges the external slow-start capacitor. 式 4 calculates the required slow-start capacitor value where $t_{(SS/TR)}$ is the desired slow-start time in ms, $I_{(SS/TR)}$ is the internal slow-start charging current of 2 μA, and V_{ref} is the internal voltage reference of 0.8 V.

$$C_{(SS/TR)}\ (nF) = \frac{t_{(SS/TR)}\ (ms) \times I_{(SS/TR)}\ (\mu A)}{V_{ref}\ (V)} \quad (4)$$

If during normal operation, VIN goes below UVLO, the EN pin goes below 1.2 V, or a thermal shutdown event occurs, the TPS57112C-Q1 device stops switching. On VIN going above UVLO, the release of pulling high of EN, or exit from a thermal shutdown, SS/TR discharges to below 60 mV before reinitiating a powering-up sequence. The VSENSE voltage follows the SS/TR pin voltage with a 54-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% of the internal reference voltage, the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference.

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Device Functional Modes (continued)

8.4.4 Sequencing

One can implement many of the common power-supply sequencing methods using the SS/TR, EN, and PWRGD pins. Implementation of the sequential method uses an open-drain or open-collector output of a power-on-reset pin of another device. shows the sequential method. Coupling power-good to the EN pin on the TPS57112C-Q1 device enables the second power supply once the primary supply reaches regulation.

Ratiometric start-up is achieved by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, double the pullup current source in 式 4. illustrates the ratiometric method.

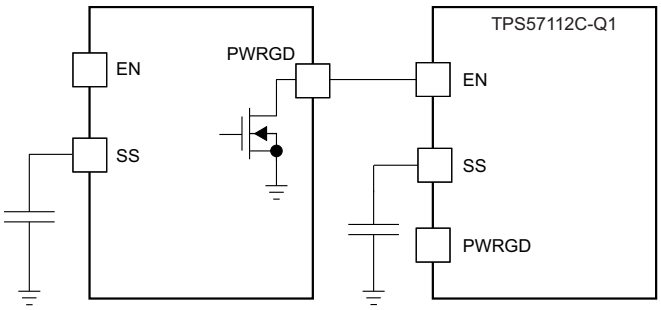

図 23. Sequential Start-Up Sequence

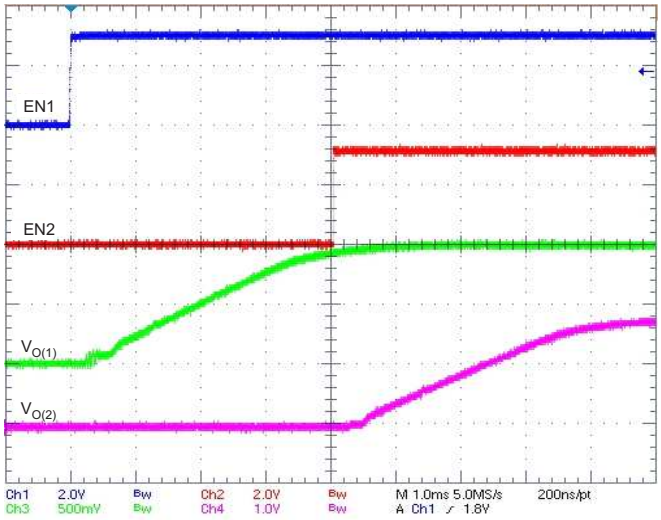

図 24. Sequential Start-up Using EN and PWRGD

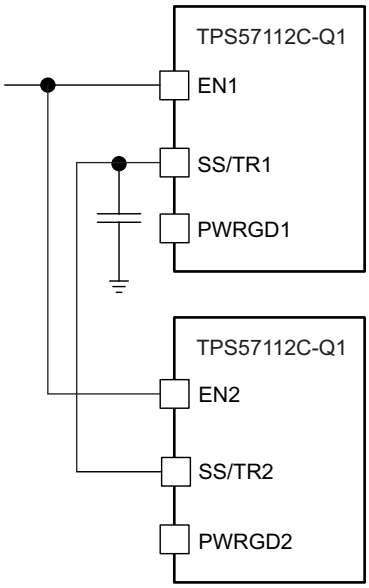

図 25. Schematic for Ratiometric Start-Up Sequence

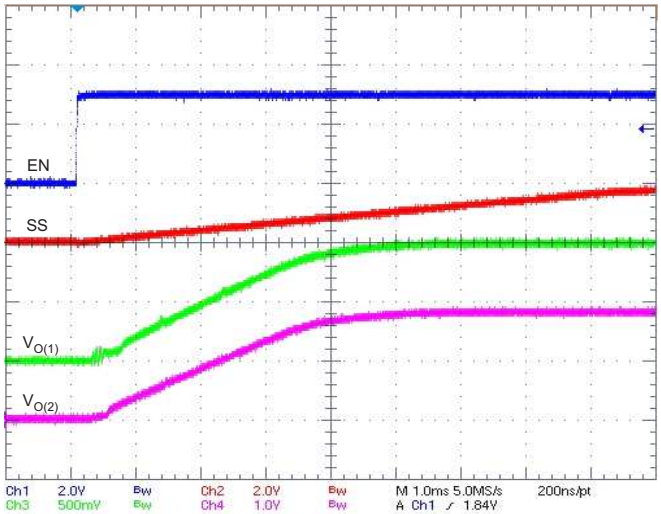

図 26. Ratiometric Start-up With $V_{O(1)}$ Leading $V_{O(2)}$

One can implement ratiometric and simultaneous power-supply sequencing by connecting the resistor network of R1 and R2 shown in to the output of the power supply that requires tracking, or to another voltage reference source. Using 式 5 and 式 6, one can calculate the tracking resistors to initiate $V_{O(2)}$ slightly before, after, or at the same time as $V_{O(1)}$. $V_{O(1)} - V_{O(2)}$ is 0 V for simultaneous sequencing. Including $V_{(ssoffset)}$ and $I_{(SS/TR)}$ as variables in the equations minimizes both the effect of the inherent SS/TR-to-VSENSE offset ($V_{(ssoffset)}$) in the slow-start circuit, and the offset created by the pullup current source ($I_{(SS)}$) and tracking resistors. Because of the

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Device Functional Modes (continued)

requirement to pull the SS/TR pin below 40 mV before starting after an EN, UVLO, or thermal shutdown fault, one must carefully select the tracking resistors to ensure the device can restart after a fault. Make sure the calculated R1 value from 式 5 is greater than the value calculated in 式 7 to ensure the device can recover from a fault. As the SS/TR voltage becomes more than 85% of the nominal reference voltage, $V_{(ssoffset)}$ becomes larger as the slow-start circuits gradually hand off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.1 V for a complete handoff to the internal voltage reference, as shown in 図 26.

$$R1 = \frac{V_{O(1)}}{V_{ref}} \times \frac{V_{(ssoffset)}}{I_{(SS/TR)}} \tag{5}$$

$$R2 = \frac{V_{ref} \times R1}{V_{O(1)} - V_{ref}} \tag{6}$$

$$R1 > 2930 \times V_{O(1)} - 145 \times (V_{O(1)} - V_{O(2)}) \tag{7}$$

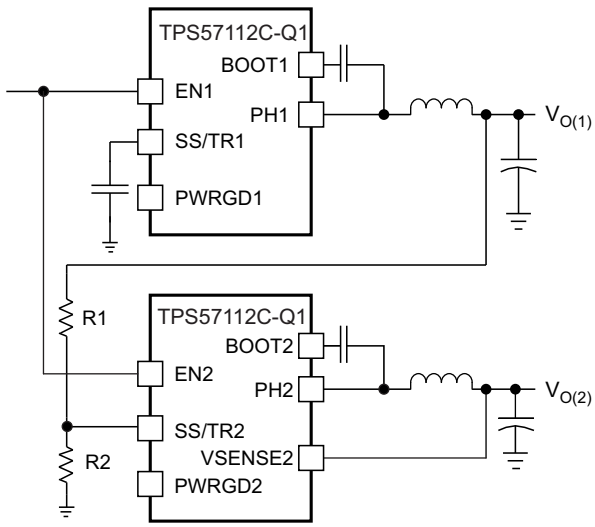

図 27. Schematic for Ratiometric and Simultaneous Start-Up Sequence

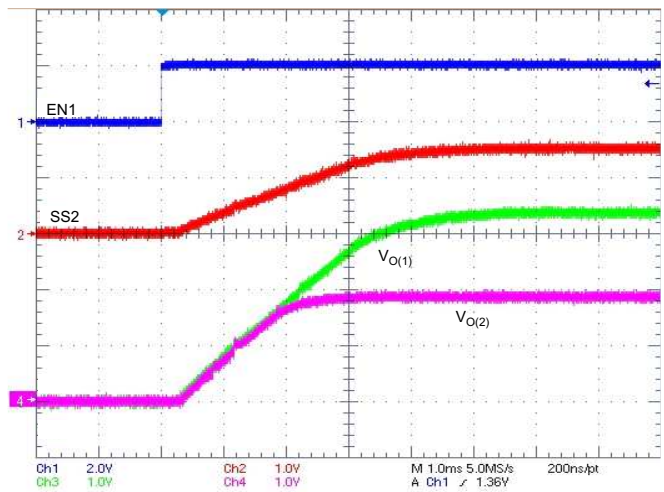

図 28. Ratiometric Start-Up Using Coupled SS/TR Pins

8.4.5 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS57112C-Q1 device is adjustable over a wide range from 200 kHz to 2000 kHz by placing a resistor on the RT/CLK pin with a value calculated by 式 8. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in 図 5 or 式 8.

$$Rt(k\Omega) = \frac{247\,530\ (M\Omega/s)}{f_{(SW)}^{1.0533}(kHz)} \tag{8}$$

$$f_{(SW)}(kHz) = \frac{131\,904\ (M\Omega/s)}{Rt^{0.9492}(k\Omega)} \tag{9}$$

To reduce the solution size, set the switching frequency as high as possible, but consider tradeoffs of the efficiency, maximum input voltage, and minimum controllable on-time.

The minimum controllable on-time is typically 65 ns at full-current load and 120 ns at no load, and limits the maximum operating input voltage or output voltage.

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Device Functional Modes (continued)

8.4.6 Overcurrent Protection

The TPS57112C-Q1 device implements a cycle-by-cycle current limit. During each switching cycle, a comparison occurs between a voltage derived from the high-side switch current and the voltage on the COMP pin. When the instantaneous switch-current voltage intersects the COMP voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. An internal clamp on the error amplifier output functions as a switch-current limit.

8.4.7 Frequency Shift

To operate at high switching frequencies and provide protection during overcurrent conditions, the TPS57112C-Q1 device implements a frequency shift. Without the frequency shift, during an overcurrent condition the low-side MOSFET may not turn off long enough to reduce the current in the inductor, causing a current runaway. With frequency shift, an overcurrent condition reduces the switching frequency from 100% to 50%, then 25%, as the voltage decreases from 0.8 V to 0 V on the VSENSE pin. The frequency shift allows the low-side MOSFET to be off long enough to decrease the current in the inductor. During start-up, the switching frequency increases as the voltage on VSENSE increases from 0 V to 0.8 V. See 図 6 for details.

8.4.8 Reverse Overcurrent Protection

The TPS57112C-Q1 device implements low-side current protection by detecting the voltage across the low-side MOSFET. When the converter sinks current through its low-side FET, the control circuit turns off the low-side MOSFET if the reverse current is typically more than 4.5 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into pre-biased outputs.

8.4.9 Synchronize Using the RT/CLK Pin

The RT/CLK pin can synchronize the converter to an external system clock. See . To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on-time of at least 75 ns. If the square wave pulls the pin above the PLL upper threshold, a mode change occurs, and the pin becomes a synchronization input. The CLK mode disables the internal amplifier, and the pin is a high-impedance clock input to the internal PLL. Stopping the clocking edges re-enables the internal amplifier, and the mode returns to the frequency set by the resistor. The square-wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V, typically. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of PH synchronizes to the falling edge of the RT/CLK pin.

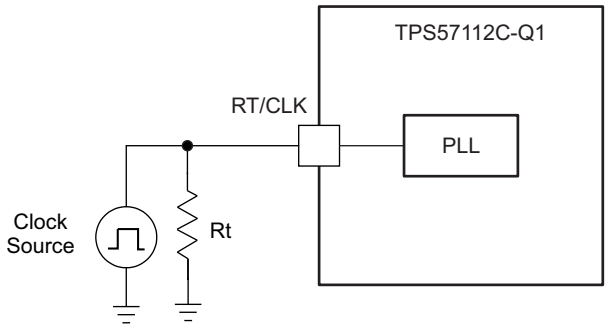

図 29. Synchronizing to a System Clock

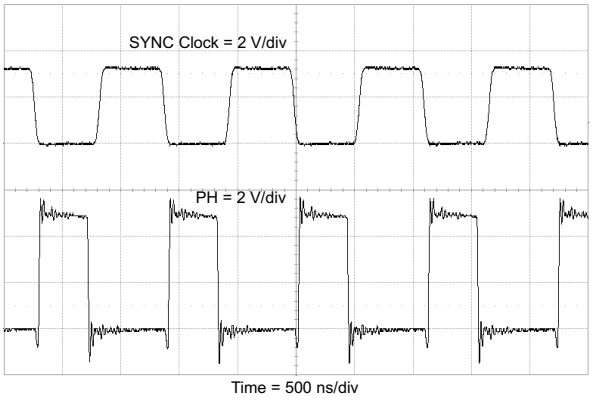

図 30. Plot of Synchronizing to System Clock

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Device Functional Modes (continued)

8.4.10 Power Good (PWRGD Pin)

The PWRGD pin output is an open-drain MOSFET. The output goes low when the VSENSE voltage enters the fault condition by falling below 91% or rising above 109% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the VSENSE voltage rises to the good condition above 93% or falls below 107% of the internal voltage reference, the PWRGD output MOSFET turns off. TI recommends using a pullup resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 6 V or less. PWRGD is in a valid state once the VIN input voltage is greater than 1.1 V.

8.4.11 Overvoltage Transient Protection

The TPS57112C-Q1 device incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to the OVTP threshold, which is 109% of the internal voltage reference. A VSENSE pin voltage greater than the OVTP threshold disables the high-side MOSFET, preventing current from flowing to the output and minimizing output overshoot. The VSENSE voltage dropping lower than the OVTP threshold allows the high-side MOSFET to turn on during the next clock cycle.

8.4.12 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 168°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 148°C, the device reinitiates the power-up sequence by discharging the SS pin to below 60 mV. The thermal shutdown hysteresis is 20°C.

8.4.13 Small-Signal Model for Loop Response

図 31 shows an equivalent model for the TPS57112C-Q1 control loop, which one can model in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a g_m of 245 µS. One can model the error amplifier using an ideal voltage-controlled current source. Resistor R0 and capacitor C0 model the open-loop gain and frequency response of the amplifier. The 1-mV ac voltage source between nodes a and b effectively breaks the control loop for the frequency-response measurements. Plotting a over c vs frequency shows the small-signal response of the frequency compensation. Plotting a over b vs frequency shows the small-signal response of the overall loop. One can check the dynamic loop response by replacing $R_{(L)}$ with a current source with the appropriate load-step amplitude and step rate in a time-domain analysis.

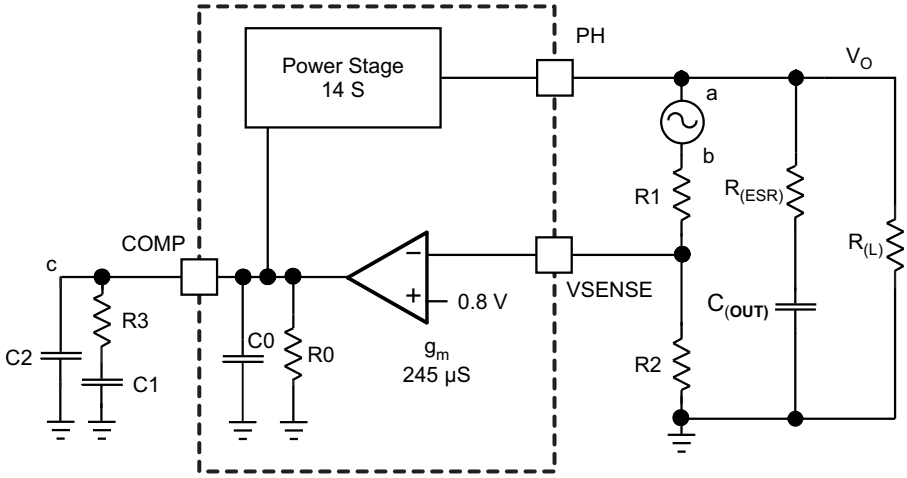

図 31. Small-Signal Model for Loop Response

Device Functional Modes (continued)

8.4.14 Simple Small-Signal Model for Peak-Current-Mode Control

図 31 is a simple small-signal model that one can use to understand how to design the frequency compensation. A voltage-controlled current source (duty-cycle modulator) supplying current to the output capacitor and load resistor approximates the TPS57112C-Q1 power stage. 式 10 shows the control-to-output transfer function, which consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in 図 31) is the power-stage transconductance. The g_m for the TPS57112C-Q1 device is 14 S. The low-frequency gain of the power-stage frequency response is the product of the transconductance and the load resistance, as shown in 式 11. As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but the dominant pole moves with load current [see 式 12]. The dashed line in the right half of 図 32 highlights the combined effect. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes it easier to design the frequency compensation.

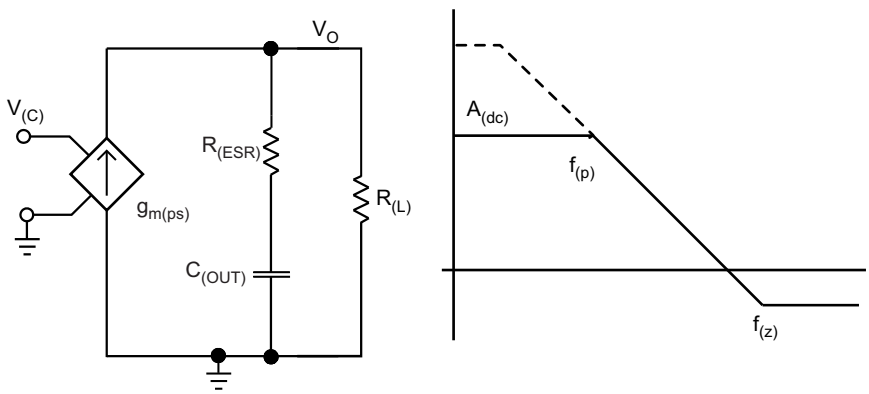

図 32. Simple Small-Signal Model and Frequency Response for Peak-Current-Mode Control

$$\frac{V_O}{V_{(C)}} = A_{(dc)} \times \frac{\left(1 + \frac{s}{2\pi \times f_{(z)}}\right)}{\left(1 + \frac{s}{2\pi \times f_{(p)}}\right)} \tag{10}$$

$$A_{(dc)} = g_{m(ps)} \times R_{(L)} \tag{11}$$

$$f_{(p)} = \frac{1}{C_{(OUT)} \times R_{(L)} \times 2\pi} \tag{12}$$

$$f_{(z)} = \frac{1}{C_{(OUT)} \times R_{(ESR)} \times 2\pi} \tag{13}$$

8.4.15 Small-Signal Model for Frequency Compensation

The TPS57112C-Q1 device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency-compensation circuits. 図 33 shows the compensation circuits. The most likely implementation of Type 2B circuits is in high-bandwidth power-supply designs using low-ESR output capacitors. Type 2A includes one additional high-frequency pole to attenuate high-frequency noise.

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Device Functional Modes (continued)

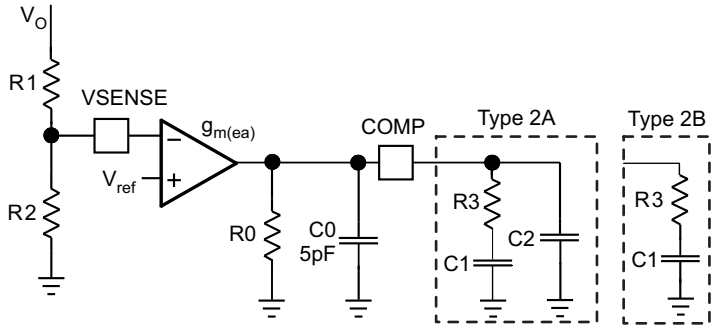

図 33. Types of Frequency Compensation

Device Functional Modes (continued)

The design guidelines for TPS57112C-Q1 loop compensation are as follows:

1. Calculate the modulator pole, $f_{(p,mod)}$, and the ESR zero, $f_{(z,mod)}$, using 式 14 and 式 15. Derating the output capacitor ($C_{(OUT)}$) may be necessary if the output voltage is a high percentage of the capacitor rating. Use the capacitor manufacturer information to derate the capacitor value. Use 式 16 and 式 17 to estimate a starting point for the crossover frequency, $f_{(c)}$. 式 16 is the geometric mean of the modulator pole and the ESR zero, and 式 17 is the mean of modulator pole and the switching frequency. Use the lower value of 式 16 or 式 17 as the maximum crossover frequency.

$$f_{(p,mod)} = \frac{I_{O(max)}}{2\pi \times V_O \times C_{(OUT)}} \tag{14}$$

$$f_{(z,mod)} = \frac{1}{2\pi \times R_{(ESR)} \times C_{(OUT)}} \tag{15}$$

$$f_{(c)} = \sqrt{f_{(p,mod)} \times f_{(z,mod)}} \tag{16}$$

$$f_{(c)} = \sqrt{f_{(p,mod)} \times \frac{f_{(SW)}}{2}} \tag{17}$$

2. Use 式 18 to calculate the value of R3.

$$R3 = \frac{2\pi \times f_{(c)} \times V_O \times C_{(OUT)}}{g_{m(ea)} \times V_{ref} \times g_{m(ps)}} \tag{18}$$

where

- $gm_{(ea)}$ is the amplifier gain (245 µS)
- $gm_{(ps)}$ is the power-stage gain (14 S)

3. Place a compensation zero at the dominant pole $f_{(p)} = \frac{1}{C_{(OUT)} \times R_{(L)} \times 2\pi}$
4. Use 式 19 to calculate the value of C1.

$$C1 = \frac{R_{(L)} \times C_{(OUT)}}{R3} \tag{19}$$

5. The use of C2 is optional. If using C2 is necessary, use it to cancel the zero from the ESR of $C_{(OUT)}$.

$$C2 = \frac{R_{(ESR)} \times C_{(OUT)}}{R3} \tag{20}$$

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9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Details on how to use this device in automotive applications appear throughout this device specification. The following sections provide the typical application use case with equations and methods on selecting the external components, as well as layout guidelines.

9.2 Typical Application

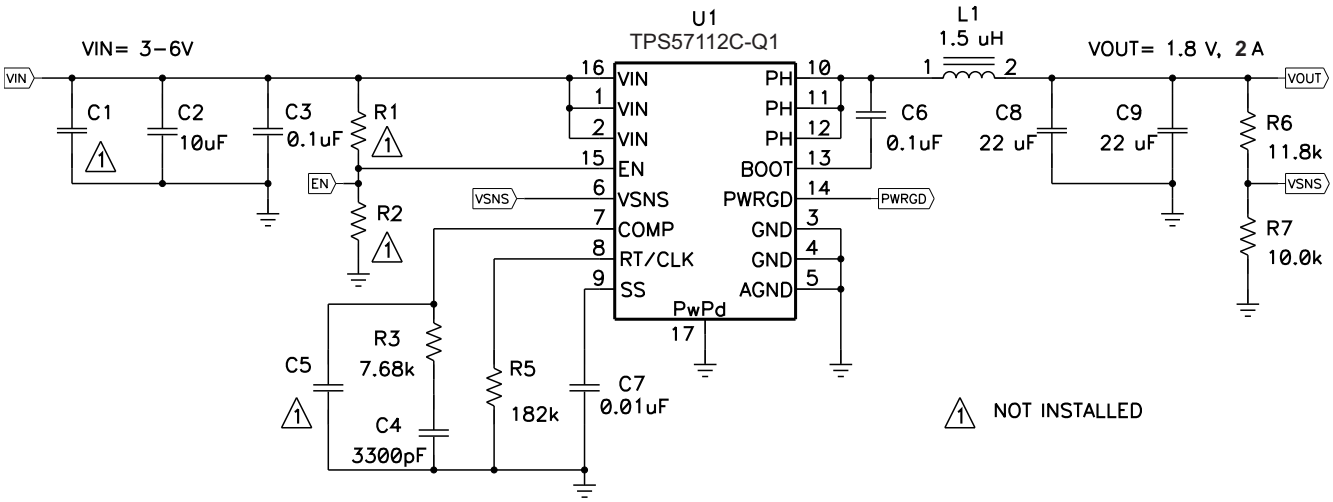

図 34. High-Frequency, 1.8-V Output Power-Supply Design With Adjusted UVLO

9.2.1 Design Requirements

This example details the design of a high-frequency switching-regulator design using ceramic output capacitors. A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, use the following known parameters:

PARAMETER	VALUE
Output voltage	1.8 V
Transient response for load step from 1 A to 2 A	$\Delta V_{(OUT)}$ = 5%
Maximum output current	2 A
Input voltage	5 V nominal, 3 V to 6 V
Output-voltage ripple	< 30 mV p-p
Switching frequency ($f_{(SW)}$)	1000 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, one wants to choose the highest switching frequency possible, because this produces the smallest solution size. The high switching frequency allows for lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the performance of the converter. The converter is capable of running from 200 kHz to 2 MHz. Unless a small solution size is an ultimate goal, select a moderate switching frequency of 1 MHz to achieve both a small solution size and high-efficiency operation. Using 式 8, calculate the value of R5 to be 180 kΩ. The choice for the design is a standard 1% 182-kΩ value.

9.2.2.2 Output Inductor Selection

The inductor selected works for the entire TPS57112C-Q1 input-voltage range. To calculate the value of the output inductor, use 式 21. The $k_{(IND)}$ coefficient represents the amount of ripple current in the inductor relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, $k_{(IND)}$ is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use $k_{(IND)}$ = 0.3; the calculated value of the inductor is 2.2 µH. For this design, the choice is a nearest standard value of 1.5 µH. For the output-filter inductor, it is important not to exceed the rms current and saturation current ratings. Use 式 23 and 式 24 to find the rms and peak inductor currents.

For this design, the rms inductor current is 2 A and the peak inductor current is 2.42 A. The chosen inductor is a Coilcraft XLA4020-152ME_. It has a saturation current rating of 9.6 A and an rms current rating of 7.5 A.

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The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated previously. In transient conditions, the inductor current can increase up to the switch-current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch-current limit rather than the peak inductor current.

$$L1 = \frac{V_{I(max)} - V_O}{I_O \times k_{(IND)}} \times \frac{V_O}{V_{I(max)} \times f_{(SW)}} \tag{21}$$

$$I_{(ripple)} = \frac{V_{I(max)} - V_O}{L1} \times \frac{V_O}{V_{I(max)} \times f_{(SW)}} \tag{22}$$

$$I_{(Lrms)} = \sqrt{I_O^2 + \frac{1}{12} \times \left(\frac{V_O \times (V_{I(max)} - V_O)}{V_{I(max)} \times L1 \times f_{(SW)}} \right)^2} \tag{23}$$

$$I_{(Lpeak)} = I_O + \frac{I_{(ripple)}}{2} \tag{24}$$

9.2.2.3 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the most-stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after removal of the input power. The regulator is temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load, such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. Sizing of the output capacitor must be adequate to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. 式 25 shows the minimum output capacitance necessary to meet this requirement.

For this example, the transient load response is specified as a 5% change in V_O for a load step from 0 A (no load) to 1.5 A (50% load). For this example, ΔI_O = 1.5 A – 0 A = 1.5 A and ΔV_O = 0.05 × 1.8 = 0.09 V. Using these numbers gives a minimum capacitance of 33 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

式 26 calculates the minimum output capacitance needed to meet the output voltage ripple specification. In this case, the maximum output-voltage ripple is 30 mV. Under this requirement, 式 26 yields 2.3 µF.

$$C_{(OUT)} > \frac{2 \times \Delta I_O}{f_{(SW)} \times \Delta V_O}$$

where

- ΔI_O is the change in output current
- $f_{(SW)}$ is the switching frequency of the regulator
- ΔV_O is the allowable change in the output voltage (25)

$$C_{(OUT)} > \frac{1}{8 \times f_{(SW)}} \times \frac{1}{\frac{V_{O(ripple)}}{I_{(ripple)}}}$$

where

- $f_{(SW)}$ is the switching frequency
- $V_{O(ripple)}$ is the maximum allowable output voltage ripple
- $I_{(ripple)}$ is the inductor ripple current (26)

式 27 calculates the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. 式 27 indicates the ESR should be less than 55 mΩ. In this case, the ESR of the ceramic capacitor is much less than 55 mΩ.

Factor in additional capacitance de-ratings for aging, temperature, and dc bias, which increase this minimum value. For this example, use two 22-µF 10-V X5R ceramic capacitors with 3 mΩ of ESR.

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Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. Specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root-mean-square (RMS) value of the maximum ripple current. One can use 式 28 to calculate the rms ripple current the output capacitor must support. For this application, 式 28 yields 333 mA.

$$R_{(ESR)} < \frac{V_{O(ripple)}}{I_{(ripple)}} \tag{27}$$

$$I_{(Co,rms)} = \frac{V_O \times (V_{I(max)} - V_O)}{\sqrt{12} \times V_{I(max)} \times L1 \times f_{(SW)}} \tag{28}$$

9.2.2.4 Input Capacitor

The TPS57112C-Q1 device requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor with at least 4.7 µF of effective capacitance, and in some applications a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input ripple current of the TPS57112C-Q1 device. Calculate the input ripple current using 式 29.

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. Minimize the capacitance variations due to temperature by selecting a dielectric material that is stable over temperature. The usual selection for power regulator capacitors is an X5R or X7R ceramic dielectric, because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor selection must also take the dc bias into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

This example design requires a ceramic capacitor with at least a 10-V voltage rating to support the maximum input voltage. The selection for this example is one 10-µF capacitor in parallel with one 0.1-µF capacitor, both with 10-V ratings. The input capacitance value determines the input ripple voltage of the regulator. Use 式 30 to calculate the input voltage ripple.

$$I_{(Ci,rms)} = I_O \times \sqrt{\frac{V_O}{V_{I(min)}} \times \frac{\left(V_{I(min)} - V_O\right)}{V_{I(min)}}} \tag{29}$$

$$\Delta V_I = \frac{I_{O(max)} \times 0.25}{C_{(IN)} \times f_{(SW)}} \tag{30}$$

Using the design example values, $I_{O(max)}$ = 2 A, $C_{(IN)}$ = 10 µF, $f_{(SW)}$ = 1 MHz, yields an input voltage ripple of 50 mV and an RMS input ripple current of 0.98 A.

9.2.2.5 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. Slow start is useful if a load requires a controlled voltage-slew rate. Another use for slow start is if the output capacitance is large and would require large amounts of current to charge the capacitor quickly to the output-voltage level. The large currents necessary to charge the capacitor may make the TPS57112C-Q1 device reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output-voltage slew rate solves both of these problems.

One can calculate the slow-start capacitor value using 式 31. For the example circuit, the slow-start time is not too critical because the output-capacitor value is 44 µF which does not require much current to charge to 1.8 V. The example circuit has the slow-start time set to an arbitrary value of 4 ms, which requires a 10 nF capacitor. In the TPS57112C-Q1 device, $I_{(SS/TR)}$ is 2.2 µA and V_{ref} is 0.8 V.

$$C_{(SS)}\ (nF) = \frac{t_{(SS)}\ (ms) \times I_{(SS/TR)}\ (\mu A)}{V_{ref}\ (V)} \tag{31}$$

9.2.2.6 Bootstrap Capacitor Selection

Connect a 0.1-µF ceramic capacitor between the BOOT and PH pins for proper operation. TI recommends using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 10-V or higher voltage rating.

9.2.2.7 Output Voltage and Feedback Resistor Selection

For the example design, the R6 selection is 100 kΩ. Using 式 32, the calculated value of R7 is 80 kΩ. The nearest standard 1% resistor is 80.5 kΩ.

$$R7 = \frac{V_{ref}}{V_O - V_{ref}} \times R6 \tag{32}$$

Because of the internal design of the TPS57112C-Q1 device, any given input voltage has a minimum output voltage limit. The output voltage can never be lower than the internal voltage reference of 0.8 V. Above 0.8 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by 式 33

$$V_{O(min)} = t_{(ONmin)} \times f_{(SWmax)} \times \left(V_{I(max)} - I_{O(min)} \times 2 \times r_{DS(on)}\right) - I_{O(min)} \times \left(R_{(L)} + r_{DS(on)}\right)$$

where

- $V_{O(min)}$ = minimum achievable output voltage
- $t_{(ONmin)}$ = minimum controllable on-time (65 ns typical. 120 ns no load)
- $f_{(SWmax)}$ = maximum switching frequency, including tolerance
- $V_{I(max)}$ = maximum input voltage
- $I_{O(min)}$ = minimum load current
- $r_{DS(on)}$ = minimum high-side MOSFET on-resistance (15 mΩ–19 mΩ)
- $R_{(L)}$ = series resistance of output inductor (33)

There is also a maximum achievable output voltage which is limited by the minimum off-time. The maximum output voltage is given by 式 34

$$V_{O(max)} = \left(1 - t_{(OFFmax)} \times f_{(SWmax)}\right) \times \left(V_{I(min)} - I_{O(max)} \times 2 \times r_{DS(on)}\right) - I_{O(max)} \times \left(R_{(L)} + r_{DS(on)}\right)$$

where

- $V_{O(max)}$ = maximum achievable output voltage
- $t_{(OFFmax)}$ = maximum off-time (60 ns typical)
- $f_{(SWmax)}$ = maximum switching frequency, including tolerance
- $V_{I(min)}$ = minimum input voltage
- $I_{O(max)}$ = maximum load current
- $r_{DS(on)}$ = maximum high-side MOSFET on-resistance (19 mΩ–30 mΩ)
- $R_{(L)}$ = series resistance of output inductor (34)

9.2.2.8 Compensation

There are several industry techniques used to compensate dc-dc regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS57112C-Q1 device. As a result of ignoring the slope compensation, the actual crossover frequency is usually lower than the crossover frequency used in the calculations. Use SwitcherPro software for a more-accurate design.

To get started, calculate the modulator pole, $f_{(p,mod)}$, and the ESR zero, $f_{(z,mod)}$, using 式 35 and 式 36. For $C_{(OUT)}$, derating the capacitor is not needed, as the 1.8-V output is a small percentage of the 10-V capacitor rating. If the output is a high percentage of the capacitor rating, use the manufacturer information for the capacitor to derate the capacitor value. Use 式 37 and 式 38 to estimate a starting point for the crossover frequency, $f_{(c)}$. For the example design, $f_{(p,mod)}$ is 6.03 kHz and $f_{(z,mod)}$ is 1210 kHz. 式 37 is the geometric mean of the modulator pole

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and the ESR zero, and 式 38 is the mean of modulator pole and the switching frequency. 式 37 yields 85.3 kHz and 式 38 gives 54.9 kHz. Use the lower value of 式 37 and 式 38 as the approximate crossover frequency. For this example, $f_{(c)}$ is 56 kHz. Next, calculate the compensation components. Use a resistor in series with a capacitor to create a compensating zero. A capacitor in parallel with these two components forms the compensating pole (if needed).

$$f_{(p,mod)} = \frac{I_{O(max)}}{2\pi \times V_O \times C_{(OUT)}} \tag{35}$$

$$f_{(z,mod)} = \frac{1}{2\pi \times R_{(ESR)} \times C_{(OUT)}} \tag{36}$$

$$f_{(c)} = \sqrt{f_{(p,mod)} \times f_{(z,mod)}} \tag{37}$$

$$f_{(c)} = \sqrt{f_{(p,mod)} \times \frac{f_{(SW)}}{2}} \tag{38}$$

The compensation design takes the following steps:

1. Set up the anticipated crossover frequency. Use 式 39 to calculate the resistor value for the compensation network. In this example, the anticipated crossover frequency ($f_{(c)}$) is 56 kHz. The power-stage gain (gm_{ps}) is 14 S, and the error-amplifier gain (gm_{ea}) is 245 µS.

$$R3 = \frac{2\pi \times f_{(c)} \times V_O \times C_{(OUT)}}{g_{m(ea)} \times V_{ref} \times g_{m(ps)}} \tag{39}$$

2. Place compensation zero at the pole formed by the load resistor and the output capacitor. Calculate the capacitor for the compensation network from 式 40.

$$C3 = \frac{R0 \times C0}{R3} \tag{40}$$

3. An extra pole can be added to attenuate high-frequency noise. In this application, the extra pole is not necessary.

From the procedures above, the compensation network includes a 7.68-kΩ resistor and a 3300-pF capacitor.

9.2.2.9 Power-Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous-conduction-mode (CCM) operation. The power dissipation of the IC (P_T) includes conduction loss ($P_{(con)}$), dead-time loss ($P_{(d)}$), switching loss ($P_{(SW)}$), gate-drive loss ($P_{(gd)}$), and supply-current loss ($P_{(q)}$).

$$P_{(con)} = I_O^2 \times r_{DS(on)(Temp)}$$

where

- I_O is the output current (A)
- $r_{DS(on)(Temp)}$ is the on-resistance of the high-side MOSFET with given temperature (Ω) (41)

$$P_{(d)} = f_{(SW)} \times I_O \times 0.7 \times 60 \times 10^{-9}$$

where

- $f_{(SW)}$ is the switching frequency (Hz) (42)

$$P_{(SW)} = 1/2 \times V_I \times I_O \times f_{(SW)} \times 8 \times 10^{-9}$$

where

- V_I is the input voltage (V) (43)

$$P_{(gd)} = 2 \times V_I \times f_{(SW)} \times 2 \times 10^{-9} \tag{44}$$

$$P_{(q)} = V_I \times 515 \times 10^{-6} \tag{45}$$

Therefore:

$$P_T = P_{(con)} + P_{(d)} + P_{(SW)} + P_{(gd)} + P_{(q)}$$

where

- P_T is the total device power dissipation (W) (46)

For a given T_A:

$$T_J = T_A + R_{\theta JA} \times P_T$$

where

- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- $R_{\theta JA}$ is the thermal resistance of the package (°C/W) (47)

For a given $T_{J(max)}$:

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} \times P_T$$

where

- $T_{J(max)}$ is maximum junction temperature (°C)
- $T_{A(max)}$ is maximum ambient temperature (°C) (48)

Additional power losses occur in the regulator circuit because of the inductor ac and dc losses and trace resistance that impact the overall efficiency of the regulator.

9.2.3 Application Curves

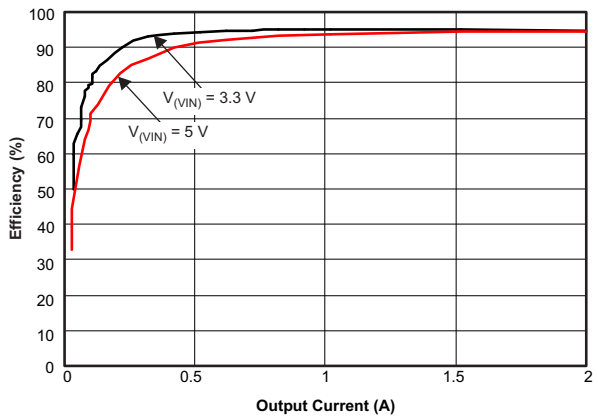


図 35. Efficiency versus Load Current

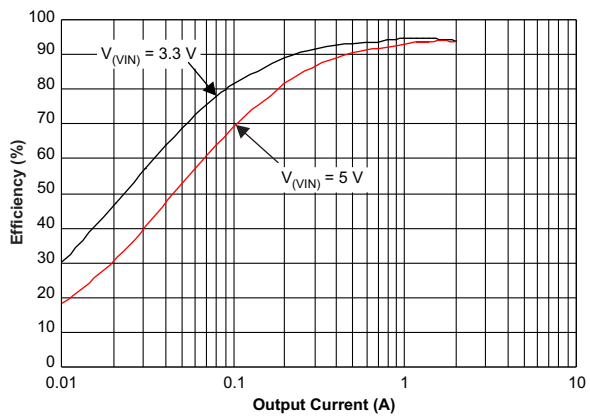
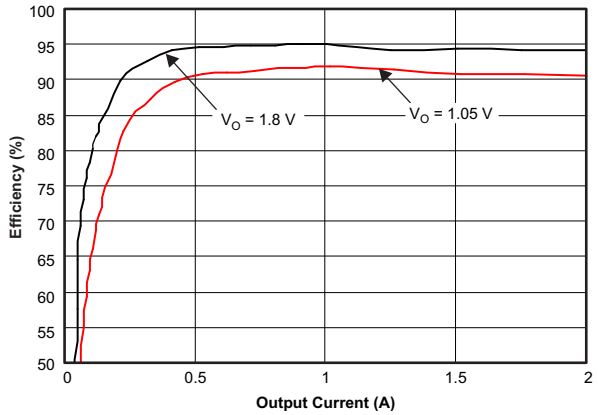
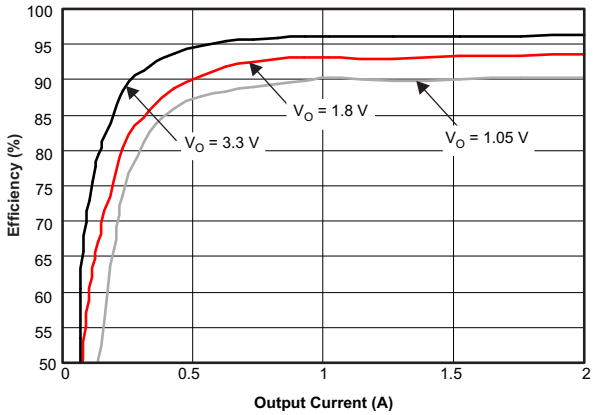


図 36. Efficiency versus Load Current



$V_{(VIN)}$ = 3.3 V $f_{(SW)}$ = 1 MHz T_A = 25ºC

図 37. Efficiency versus Load Current
1 MHz, 3.3 VIN, T_A = 25°C



$V_{(VIN)}$ = 5 V $f_{(SW)}$ = 1 MHz T_A = 25ºC

図 38. Efficiency versus Load Current
1 MHz, 5 VIN, T_A = 25°C

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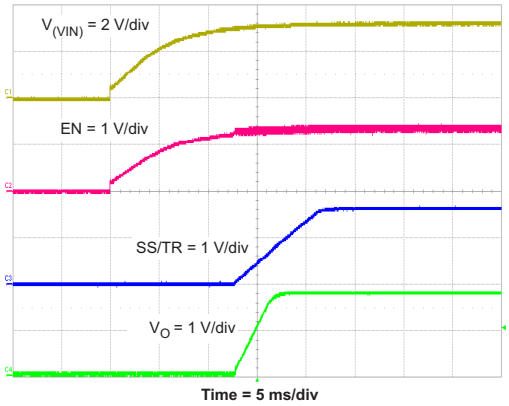

図 39. Power-Up V_O, $V_{(VIN)}$

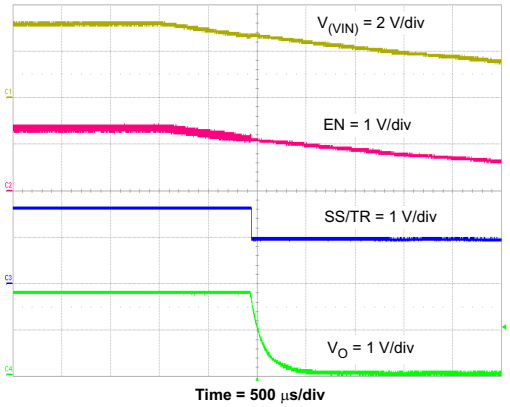

図 40. Power-Down V_O, $V_{(VIN)}$

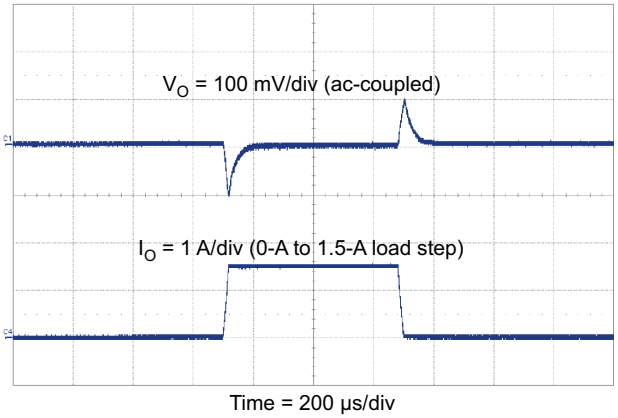

図 41. Transient Response, 1.5-A Step

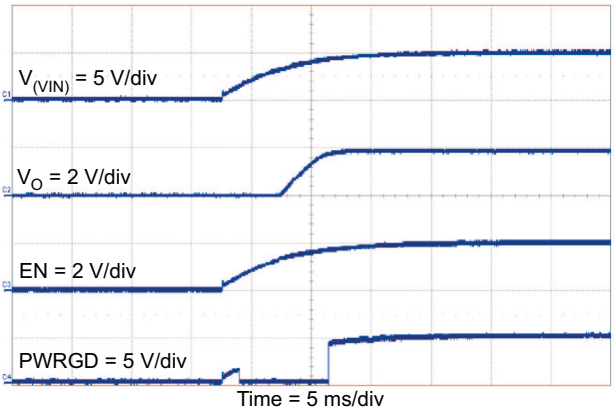

図 42. Power-Up V_O, $V_{(VIN)}$

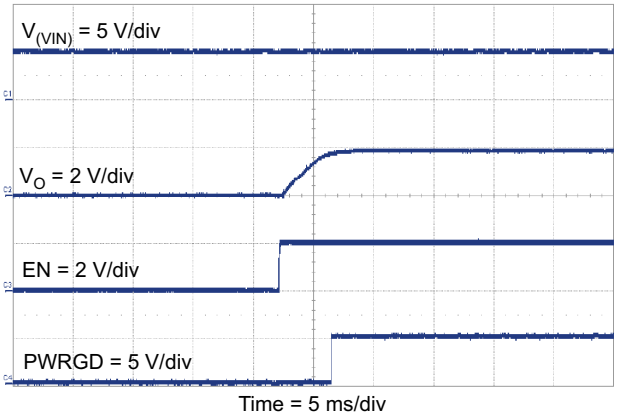

図 43. Power-Up V_O, EN

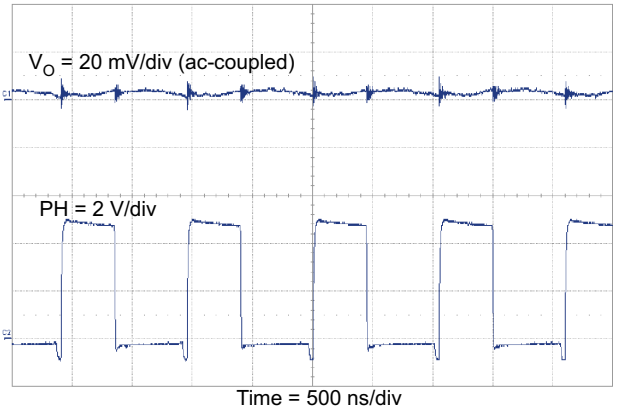

図 44. Output Ripple, 2 A

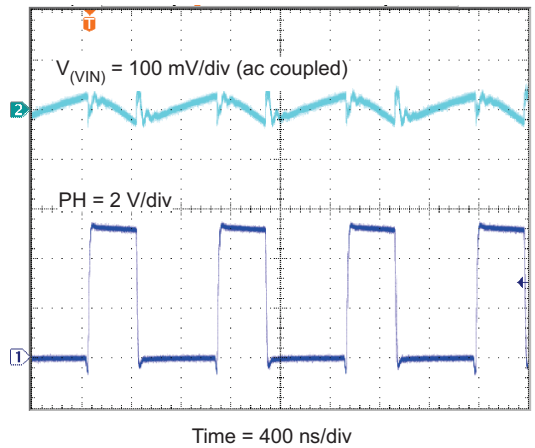

図 45. Input Ripple, 2 A

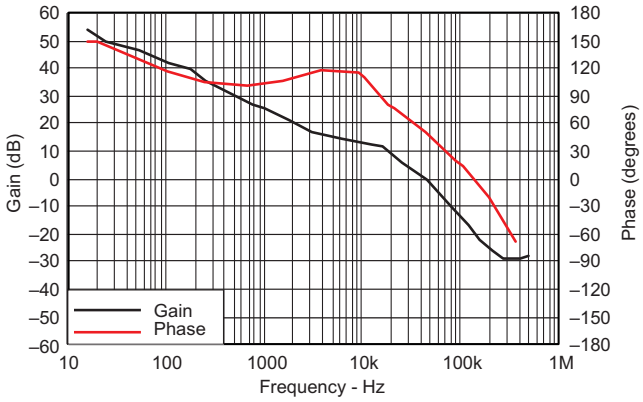

図 46. Closed-Loop Response, $V_{(VIN)}$ (5 V), 2 A

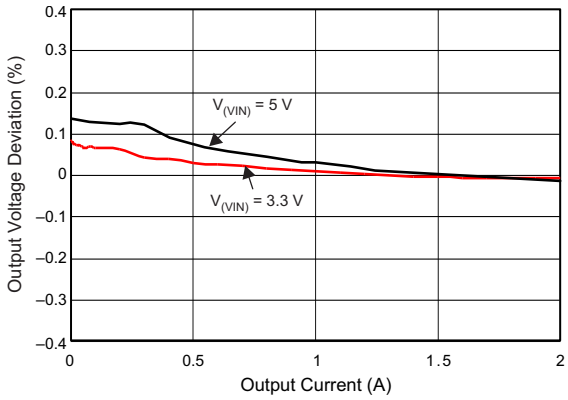

図 47. Load Regulation versus Load Current

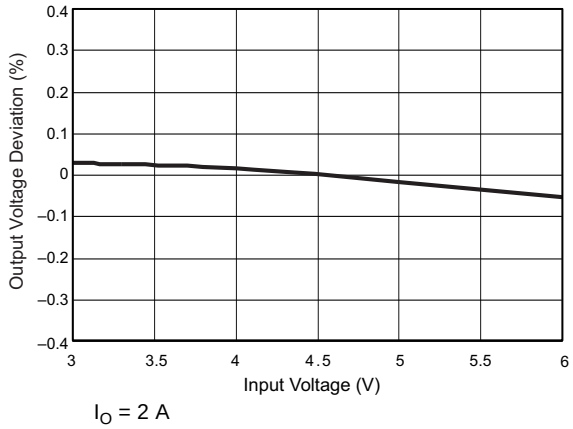

図 48. Regulation versus Input Voltage

10 Power Supply Recommendations

By design, the TPS57112C-Q1 device works with an analog supply voltage range of 2.95 V to 6 V. Ensure good regulation for the input supply, and connect the supply to the VIN pins with the appropriate input capacitor as calculated in the *Input Capacitor* section. If the input supply is located more than a few inches from the TPS57112C-Q1 device, the design may require extra capacitance in addition to the recommended value.

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11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. Take care to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See 図 49 for a PCB layout example. Tie the GND pins and AGND pin directly to the thermal pad under the IC. Connect the thermal pad to any internal PCB ground planes using multiple vias directly under the IC. One can use additional vias to connect the top-side ground area to the internal planes near the input and output capacitors. For operation at full-rated load, the top-side ground area, along with any additional internal ground planes, must provide adequate heat dissipating area.

Locate the input bypass capacitor as close to the IC as possible. Route the PH pins to the output inductor. Because the PH connection is the switching node, locate the output inductor close to the PH pins, and minimize the area of the PCB conductor to prevent excessive capacitive coupling. Also locate the boot capacitor close to the device. Connect the sensitive analog ground connections for the following to a separate analog ground trace as shown:

- Feedback voltage divider
- Compensation components
- Slow-start capacitor
- Frequency-set resistor

The RT/CLK pin is particularly sensitive to noise, so locate the RT resistor as close as possible to the IC and route traces to minimize their lengths. One can place the additional external components approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts. However, this layout, meant as a guideline, demonstrably produces good results.

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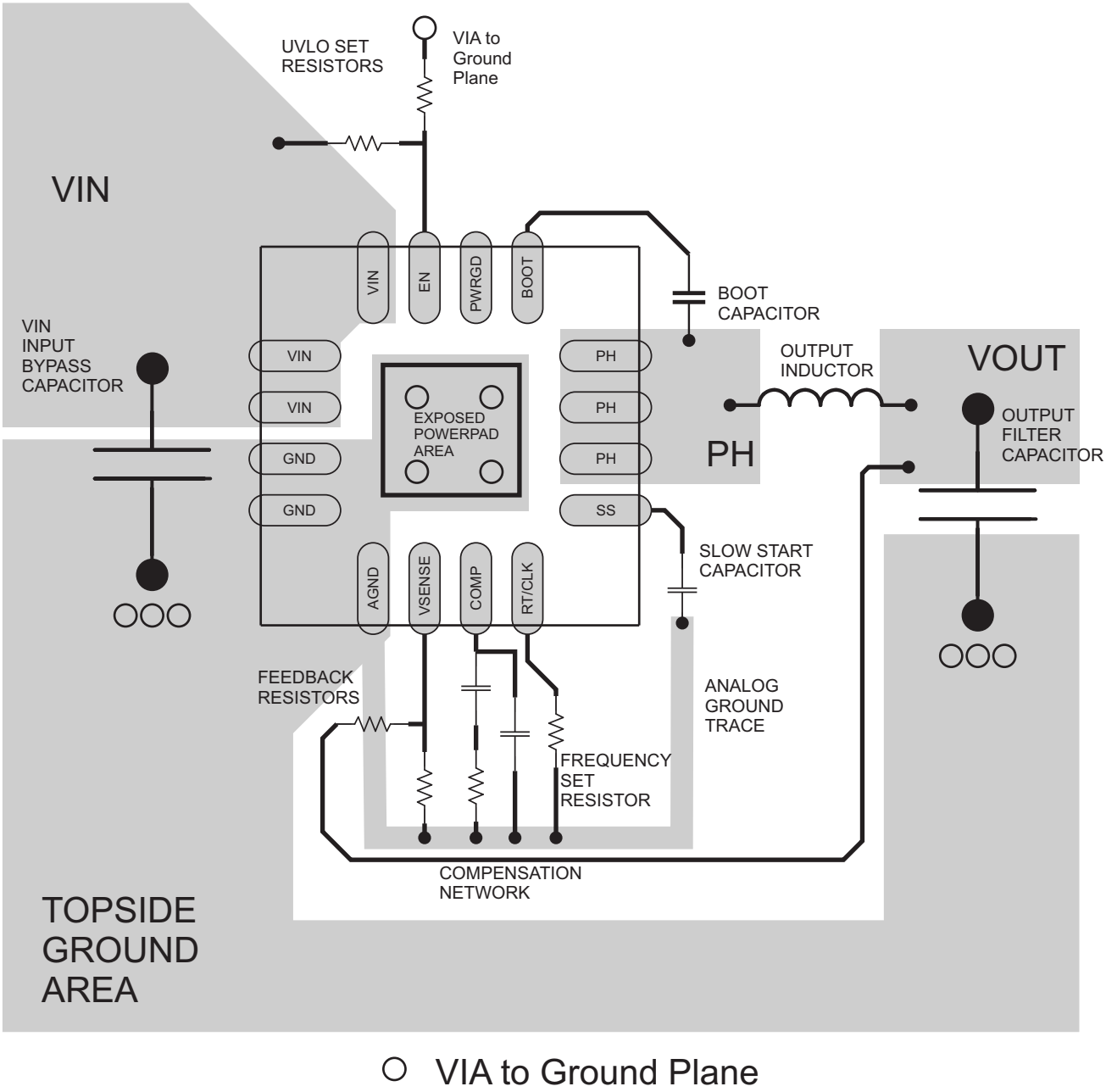
11.2 Layout Example



○ VIA to Ground Plane

図 49. PCB Layout Example

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

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12.1.2 開発サポート

SWIFT™の詳しいドキュメントについては、TI の Web サイト (www.ti.com/swift) を参照してください。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『Enable Functionality and Adjusting Undervoltage Lockout for TPS57112-Q1』* (英語)
- テキサス・インスツルメンツ、*『Interfacing TPS57xxx-Q1,TPS65320-Q1 Family, and TPS65321-Q1 Devices With Low Impendence External Clock Drivers』* (英語)
- テキサス・インスツルメンツ、*『TPS57112-Q1 High Frequency (2.35 MHz) Operation』* (英語)
- テキサス・インスツルメンツ、*『TPS57112EVM User's Guide』* (英語)

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12.4 サポート・リソース

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS57112CQRTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7112Q
TPS57112CQRTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7112Q
TPS57112CQRTERQ1.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7112Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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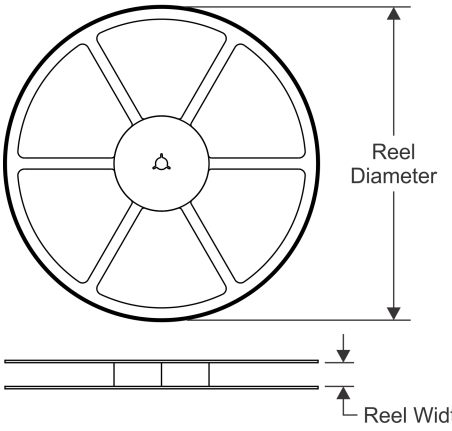
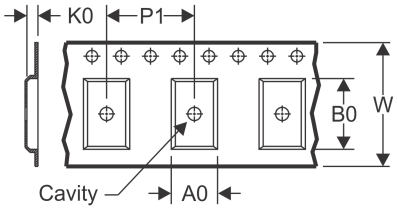
TAPE AND REEL INFORMATION

REEL DIMENSIONS

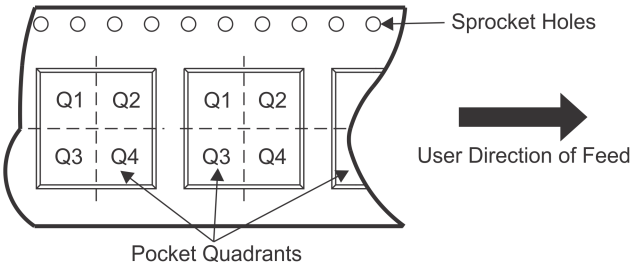


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

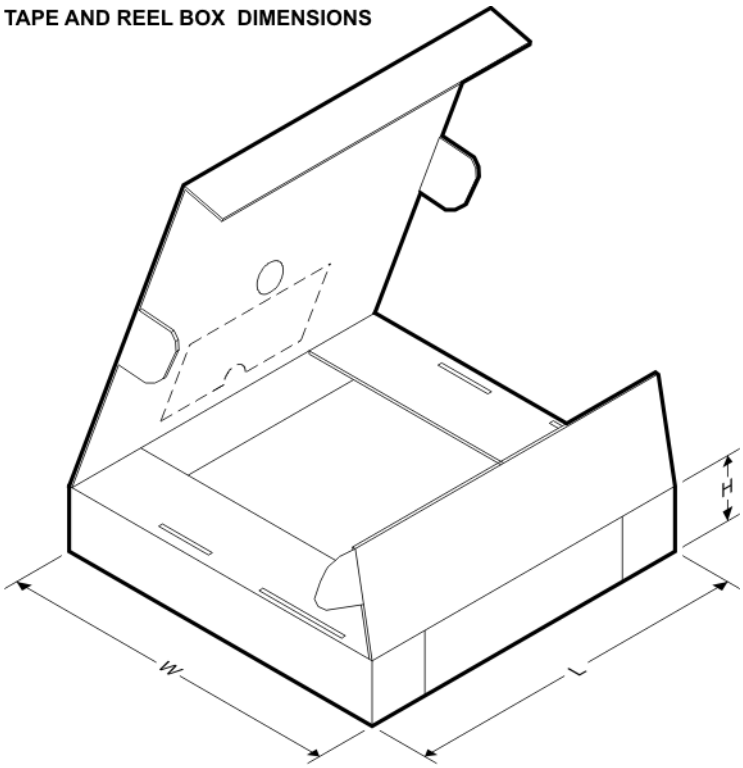
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS57112CQRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS57112CQRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

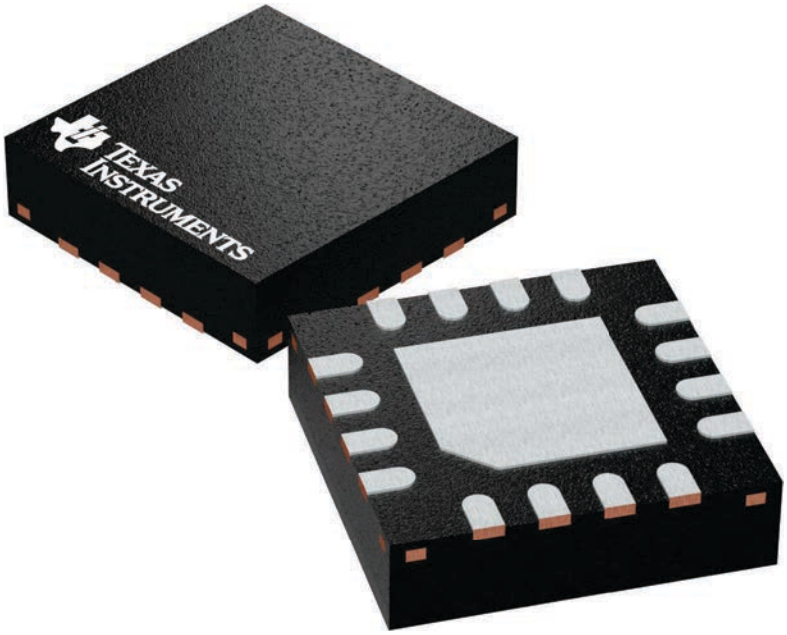
RTE 16

WQFN - 0.8 mm max height

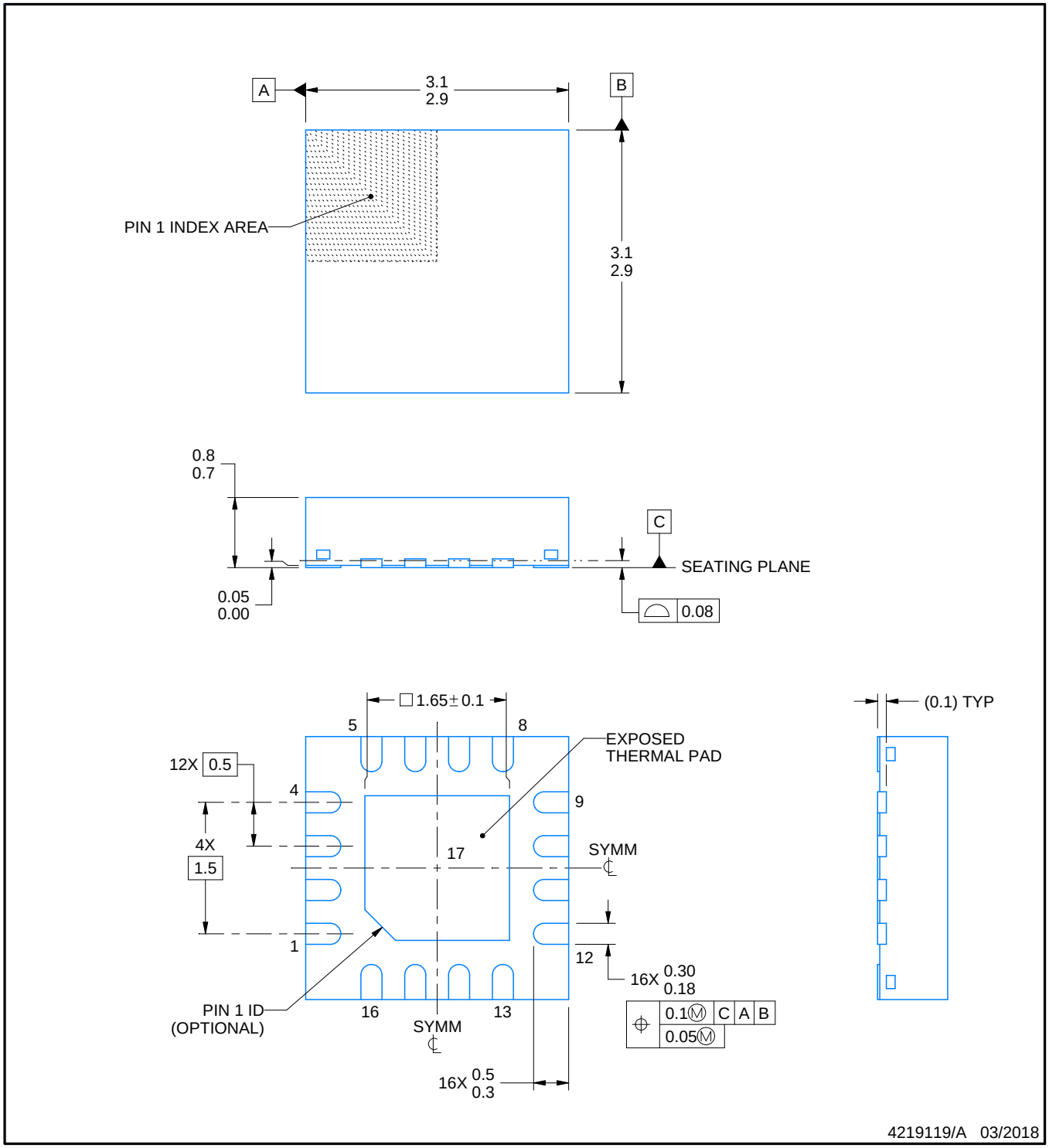
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

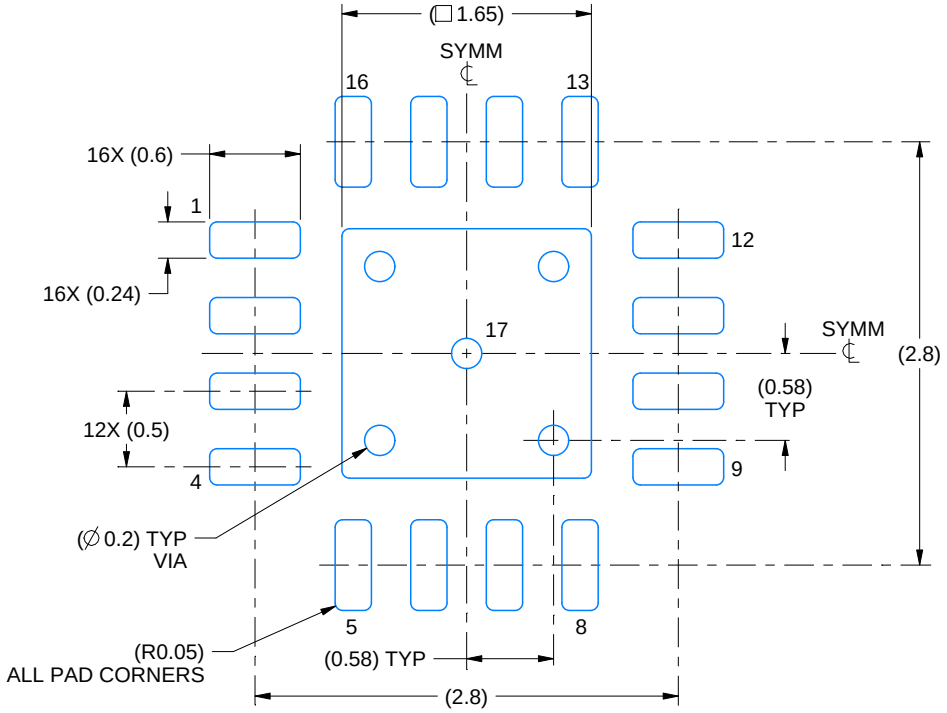


4225944/A

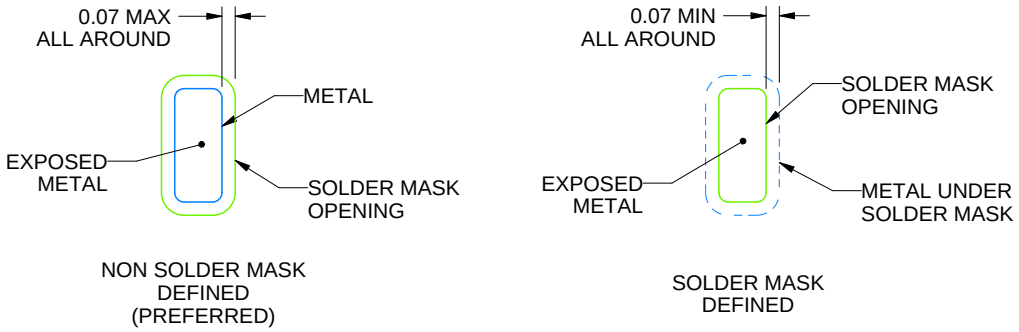


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

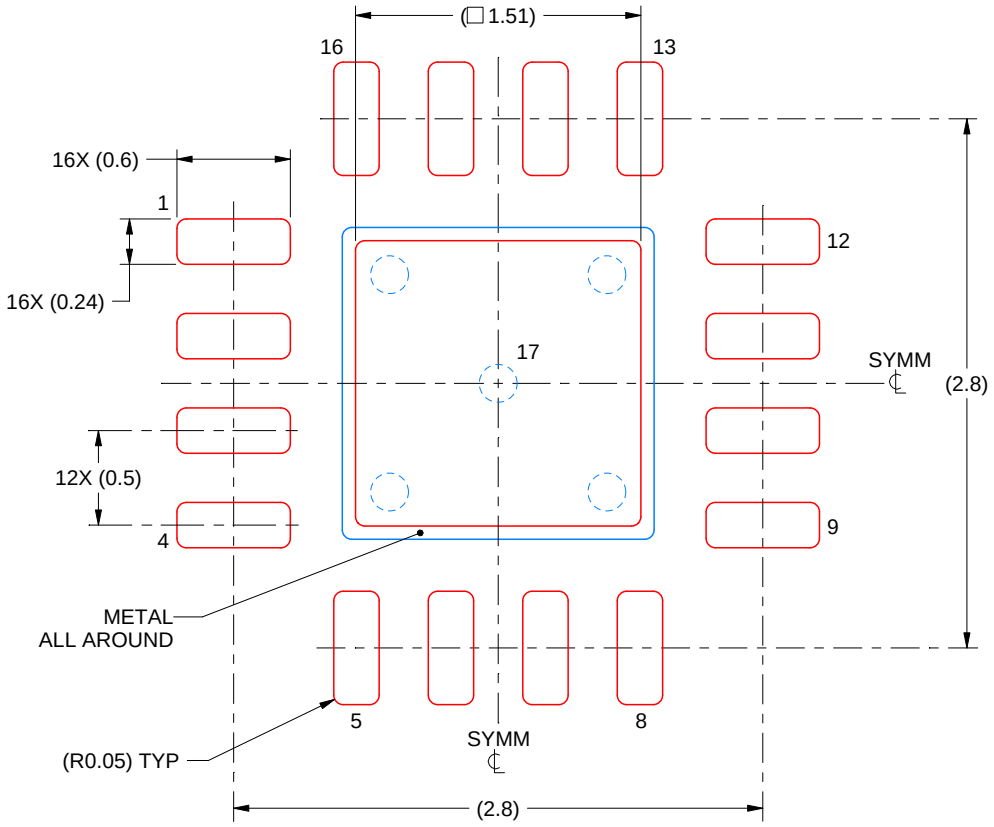


SOLDER MASK DETAILS

4219119/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219119/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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