



TPS565208 4.5V～17V入力、5A、SOT-23パッケージ、同期整流降圧型 電圧レギュレータ

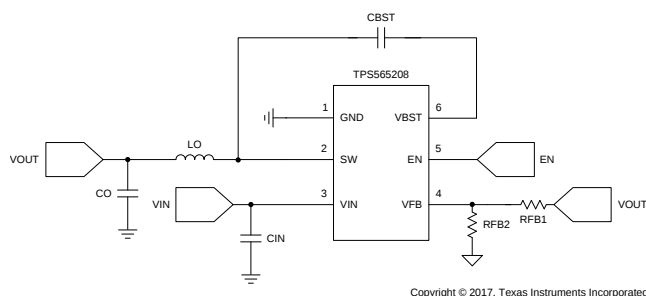
1 特長

- 最大出力電流: 5A
- 31mΩおよび16mΩの内蔵FET
- D-CAP2™モード制御による高速過渡応答
- 入力電圧範囲: 4.5V～17V
- 出力電圧範囲: 0.76V～7V
- 連続電流モード
- 500kHzのスイッチング周波数
- 低いシャットダウン電流: 1μA未満
- 1%の帰還電圧精度
- プリバイアス出力電圧からのスタートアップ
- サイクルごとの電流制限
- ヒカップ・モードによる過電流保護
- 非ラッチUVPおよびTSD保護
- 固定ソフトスタート: 1.0ms
- WEBENCH® Power Designerにより、TPS565208を使用するカスタム設計を作成

2 アプリケーション

- デジタル・テレビ用電源
- 高精細 Blu-ray™ディスク・プレイヤー
- ネットワーク・ホーム・ターミナル
- デジタル・セットトップ・ボックス (STB)
- 監視機器

概略回路図



Copyright © 2017, Texas Instruments Incorporated

3 概要

TPS565208は単純で使いやすい、5A同期整流降圧型コンバータで、SOT-23パッケージに搭載されています。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が低くなるよう最適化されています。

このスイッチ・モード電源(SMPS)デバイスは D-CAP2™モード制御を採用しているため、高速な過渡応答を実現し、外付けの補償部品を必要としません。D-CAP2™により、低い等価直列抵抗(ESR)の特化ポリマー・コンデンサおよびセラミック・コンデンサを使用できます。

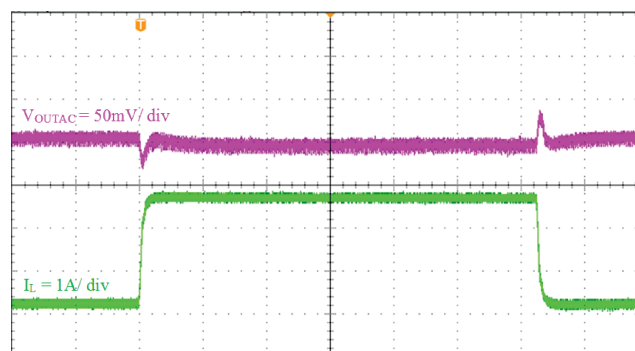
TPS565208は6ピンの1.6mm×2.9mm SOT (DDC)パッケージで供給され、-40℃～125℃の接合部温度範囲で動作します。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS565208	DDC (6)	1.60mm×2.90mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

TPS565208の負荷レギュレーション



目次

1	特長	1	7.4	Device Functional Modes.....	11
2	アプリケーション	1	8	Application and Implementation	12
3	概要	1	8.1	Application Information.....	12
4	改訂履歴	2	8.2	Typical Application	12
5	Pin Configuration and Functions	3	9	Power Supply Recommendations	18
6	Specifications	4	10	Layout	19
6.1	Absolute Maximum Ratings	4	10.1	Layout Guidelines	19
6.2	ESD Ratings.....	4	10.2	Layout Example	19
6.3	Recommended Operating Conditions.....	4	11	デバイスおよびドキュメントのサポート	20
6.4	Thermal Information	4	11.1	開発サポート.....	20
6.5	Electrical Characteristics.....	5	11.2	ドキュメントの更新通知を受け取る方法.....	20
6.6	Typical Characteristics	6	11.3	コミュニティ・リソース	20
7	Detailed Description	9	11.4	商標	20
7.1	Overview	9	11.5	静電気放電に関する注意事項	20
7.2	Functional Block Diagram	9	11.6	Glossary	20
7.3	Feature Description.....	10	12	メカニカル、パッケージ、および注文情報	21

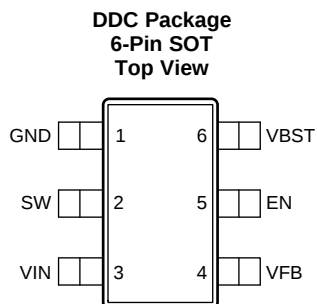
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (September 2017) から Revision B に変更	Page
• 追加 テープ・アンド・リールの情報と歩留まり向上	21

2017年9月発行のものから更新	Page
• 最初の公開リリース	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin. Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 μ F capacitor between VBST and SW pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN, EN	−0.3	19	V
	VBST	−0.3	25	V
	VBST (10 ns transient)	−0.3	27	V
	VBST (vs SW)	−0.3	6.5	V
	VFB	−0.3	6.5	V
	SW	−2	19	V
	SW (10 ns transient)	−3.5	21	V
Operating junction temperature, T _J		−40	150	°C
Storage temperature, T _{stg}		−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Supply input voltage range	4.5		17	V
V _I	Input voltage range	VBST		23	V
		VBST (10 ns transient)		26	
		VBST (vs SW)		6.0	
		EN		17	
		VFB		5.5	
		SW		17	
		SW (10 ns transient)		20	
T _J	Operating junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS565208	UNIT
		DDC (SOT)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	95.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	35.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	16.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	16.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

 $T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VIN}	Operating – non-switching supply current	V _{IN} current, EN = 5 V, V _{FB} = 1 V		590	780	μA
I _{VINSDN}	Shutdown supply current	V _{IN} current, EN = 0 V		0.8	5	μA
LOGIC THRESHOLD						
V _{ENH}	EN high-level input voltage		1.6			V
V _{ENL}	EN low-level input voltage				0.8	V
R _{EN}	EN pin resistance to GND	V _{EN} = 12 V	120	245	400	kΩ
V _{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V _{FBTH}	V _{FB} threshold voltage		753	760	767	mV
I _{VFB}	V _{FB} input current	T _A = 25°C, V _{FB} = 0.8 V		0	±0.1	μA
MOSFET						
R _{DS(on)h}	High-side switch resistance	T _A = 25°C, V _{BST} – V _{SW} = 5.5 V		31		mΩ
R _{DS(on)l}	Low-side switch resistance	T _A = 25°C		16		mΩ
CURRENT LIMIT						
I _{OCL}	Current limit		5.3	6.7	8	A
THERMAL SHUTDOWN						
T _{SDN}	Thermal shutdown threshold ⁽¹⁾	Shutdown temperature		172		°C
		Hysteresis		38		
ON-TIME TIMER CONTROL						
t _{OFF(MIN)}	Minimum off time	V _{FB} = 0.61 V		236	280	ns
SOFT START						
t _{SS}	Soft-start time	Internal soft-start time		1.0		ms
FREQUENCY						
F _{SW}	Switching frequency	V _{IN} = 12 V, V _{OUT} = 5 V, CCM mode		500		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V _{UVP}	Output UVP threshold	Hiccup detect (H > L)		65		%
T _{HICCUP_WAIT}	Hiccup on time			1.8		ms
T _{HICCUP_RE}	Hiccup time before restart			14.9		ms
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage		4.0	4.3	V
		Shutdown VIN voltage	3.3	3.6		
		Hysteresis VIN voltage ⁽¹⁾		0.4		

(1) Not production tested.

6.6 Typical Characteristics

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

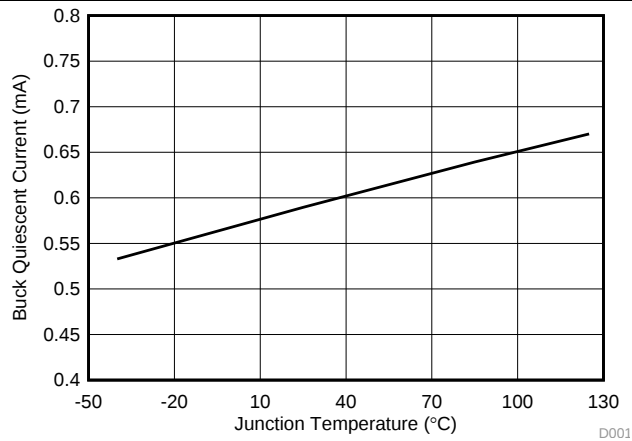


Figure 1. TPS565208 Supply Current vs Junction Temperature

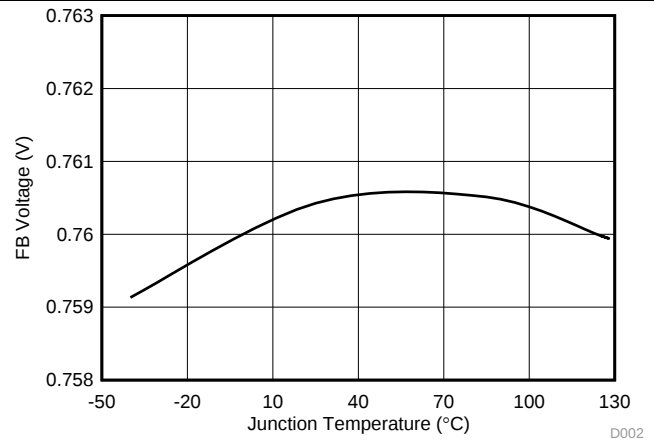


Figure 2. VFB Voltage vs Junction Temperature

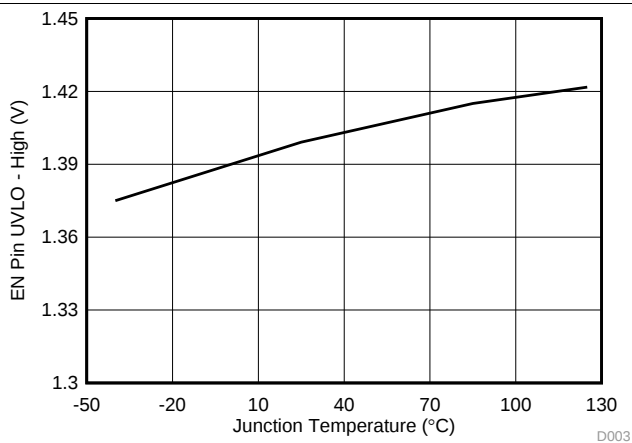


Figure 3. EN Pin UVLO Low Voltage vs Junction Temperature

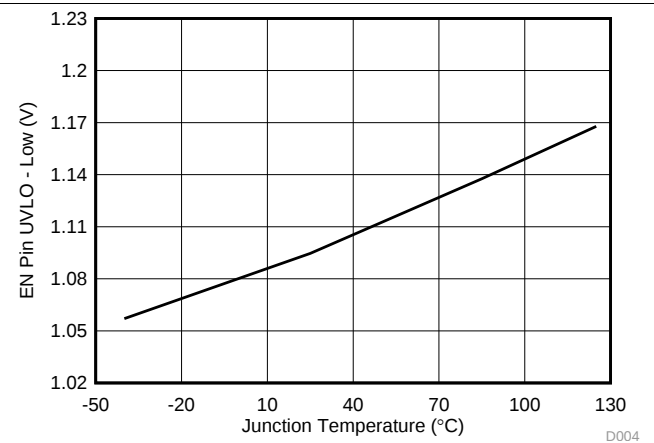


Figure 4. TPS565208 EN Pin UVLO High Voltage vs Junction Temperature

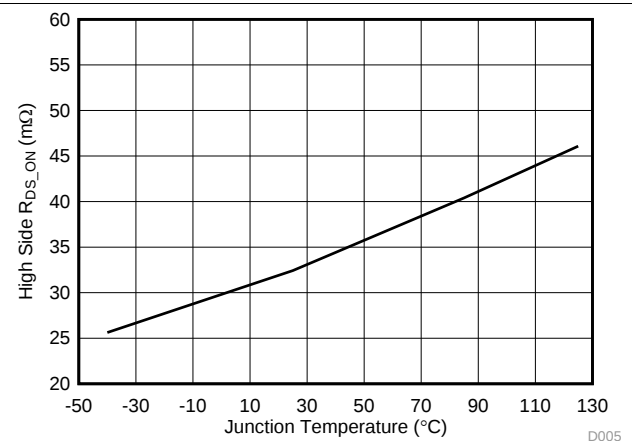


Figure 5. High-Side R_{ds-On} vs Junction Temperature

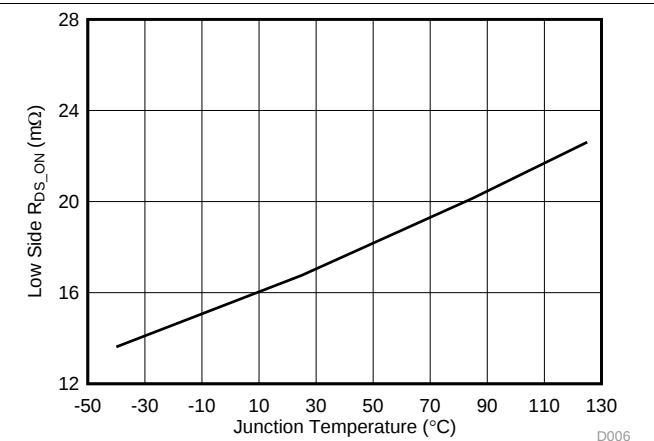


Figure 6. Low-Side R_{ds-On} vs Junction Temperature

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

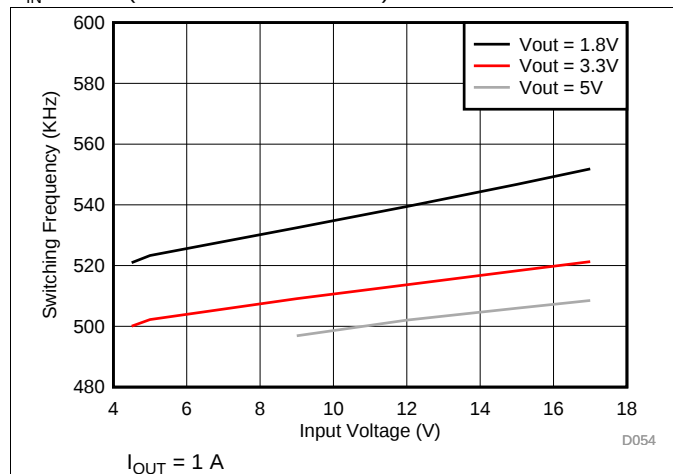


Figure 7. TPS565208 Switching Frequency vs Input Voltage

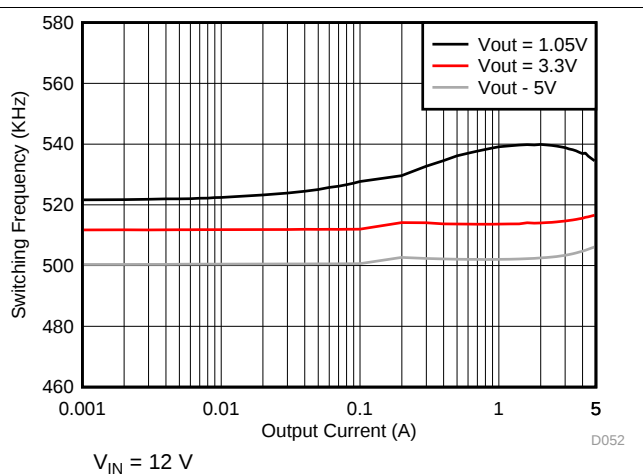


Figure 8. TPS565208 Switching Frequency vs Output Current

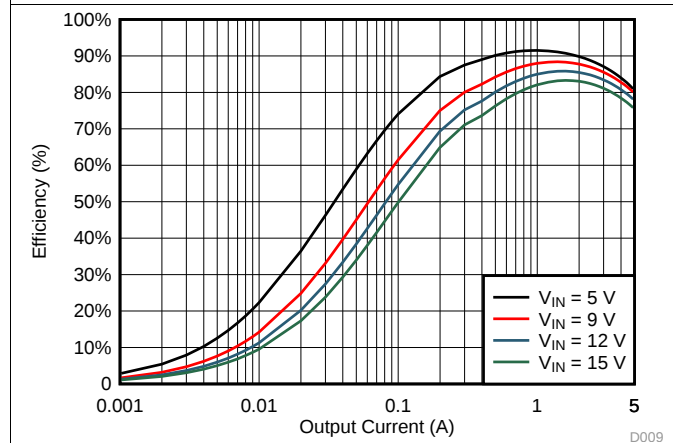


Figure 9. TPS565208 $V_{OUT} = 1.05\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

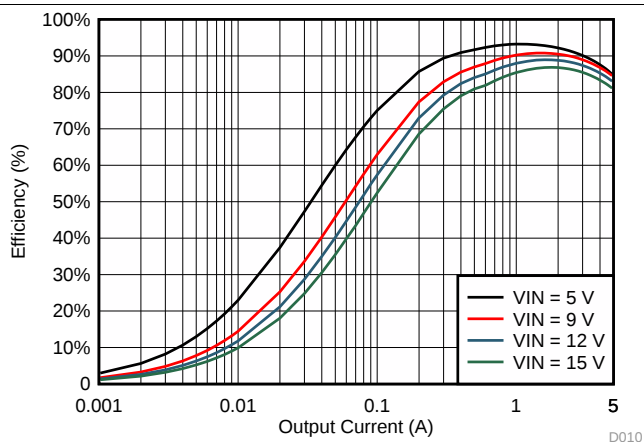


Figure 10. TPS565208 $V_{OUT} = 1.5\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

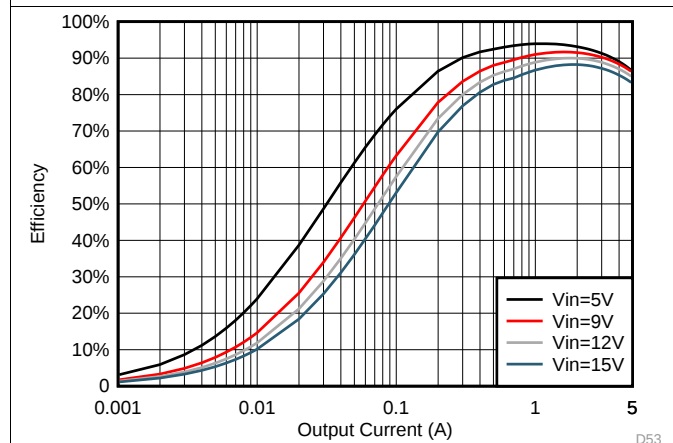


Figure 11. TPS565208 $V_{OUT} = 1.8\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

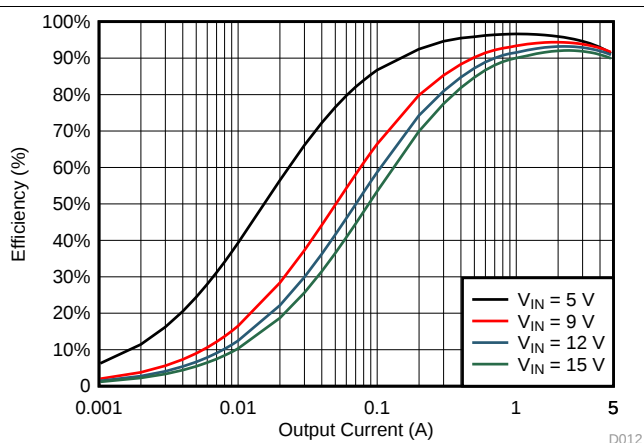


Figure 12. TPS565208 $V_{OUT} = 3.3\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

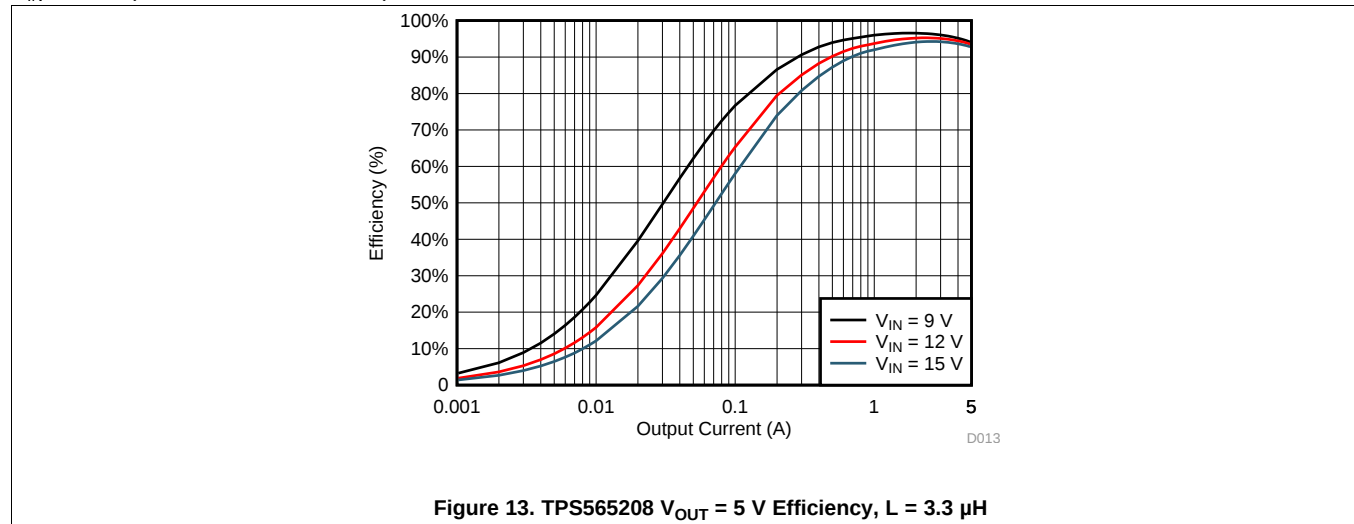
TPS565208

JAJSOW1B – SEPTEMBER 2017 – REVISED JUNE 2018

www.ti.com

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

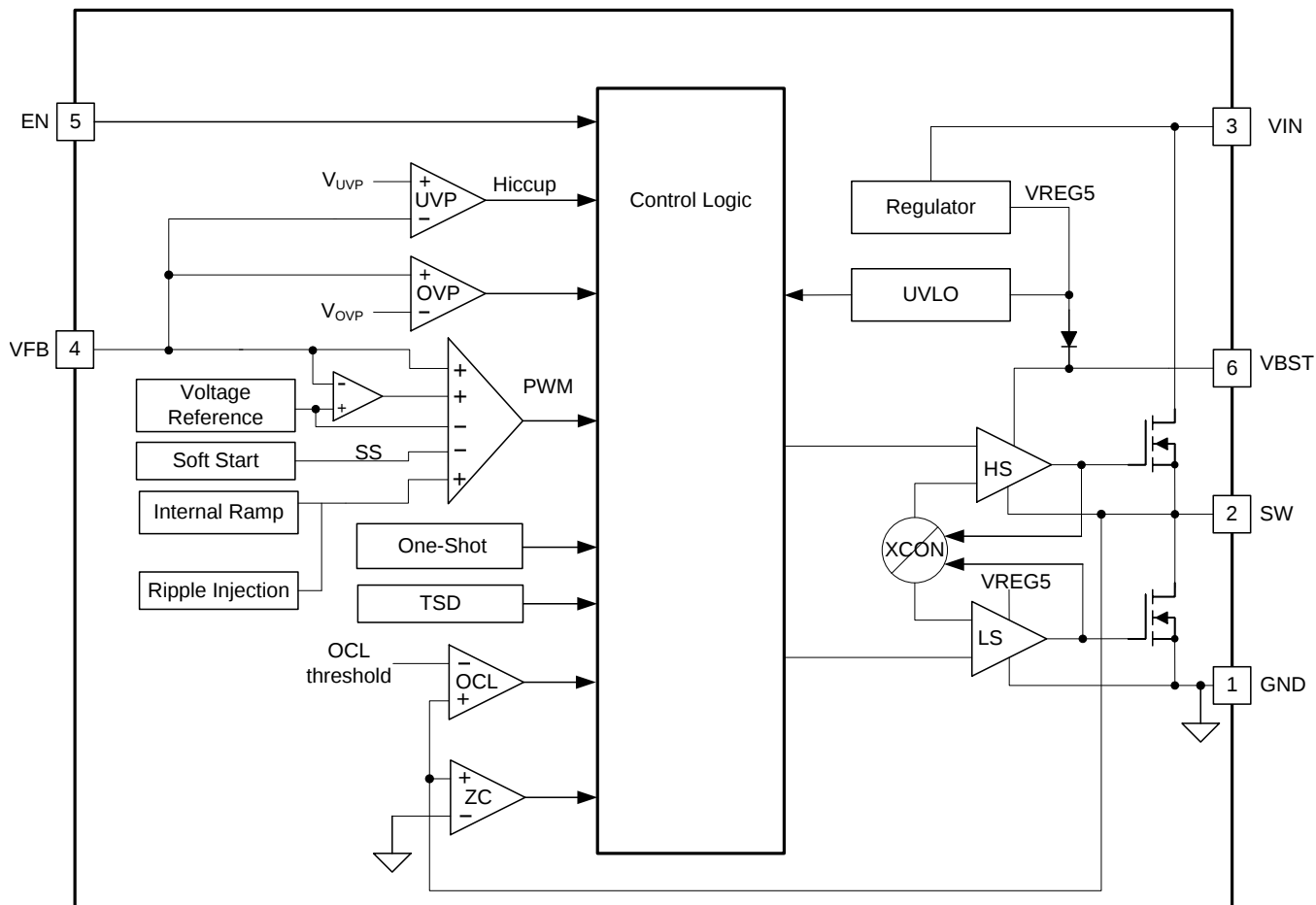


7 Detailed Description

7.1 Overview

The TPS564208 is a 5-A synchronous step-down converter. The proprietary D-CAP2™ mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2™ mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS565208 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. The D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with low-ESR ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot duration is set inversely proportional to the converter input voltage, V_{IN} , and proportional to the output voltage V_O , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An ripple is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

7.3.2 Soft Start and Pre-Biased Soft Start

The TPS565208 has an internal 1.0-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB} . This scheme ensures that the converter ramps up smoothly into regulation point.

7.3.3 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The inductor current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN} , V_{OUT} , and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT} . If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the V_{FB} voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device shuts down after the UVP delay time (typically 24 μ s) and re-starts after the hiccup time (typically 14.9 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

7.3.4 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.5 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 172°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS565208 operates in the normal switching mode. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS565208 operates at a quasi-fixed frequency of 550 kHz.

7.4.2 Standby Operation

When the TPS565208 is operating in normal CCM, it may be placed in standby by asserting the EN pin low.

8 Application and Implementation

NOTE

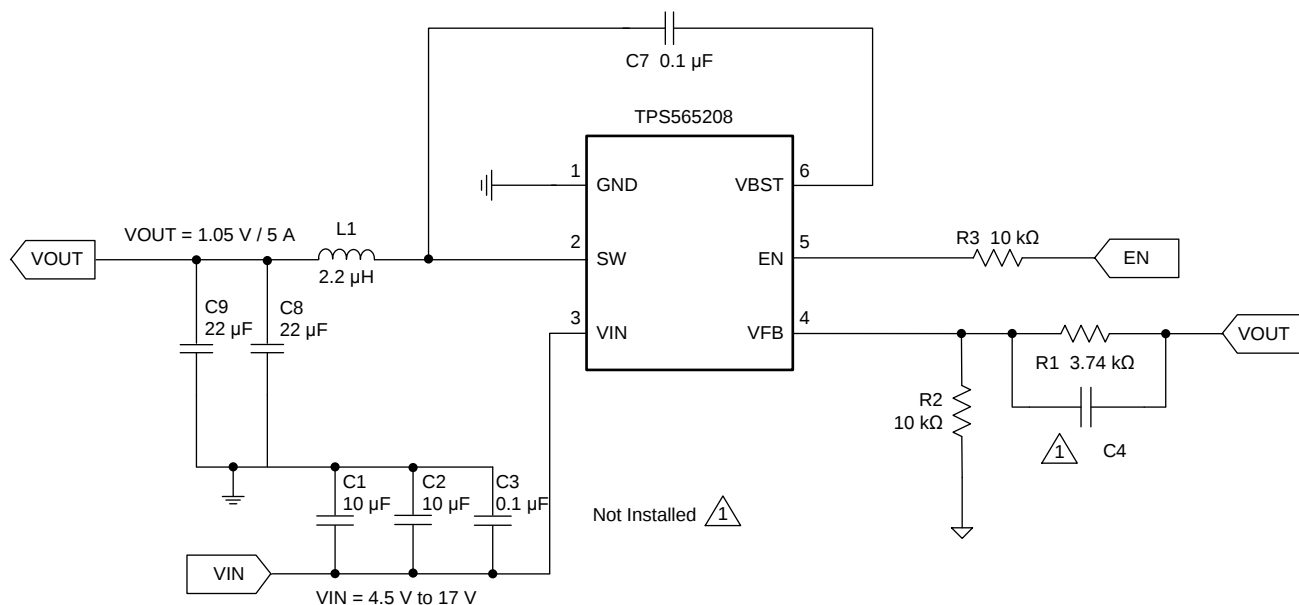
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical step-down DC-DC converter for converting a higher dc voltage to a lower dc voltage with a maximum available output current of 5 A. The following design procedure can be used to select component values for the TPS565208. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in [Figure 14](#) shows the TPS565208 4.5-V to 17-V input, 1.05-V output converter design meeting the requirements for 5-A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.



Copyright © 2017, Texas Instruments Incorporated

Figure 14. TPS565208 1.05-V, 5-A Reference Design

Typical Application (continued)

8.2.1 Design Requirements

Table 1 shows the design parameters for this application.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 17 V
Output voltage	1.05 V
Transient response, 1A/us slew rate	$\Delta V_{out} = \pm 5\%$
Input ripple voltage	400 mV
Output ripple voltage	20 mV
Output current rating	5 A
Operating frequency	550 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click [here](#) to create a custom design using the TPS565208 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using to calculate V_{OUT} .

To improve efficiency at very light loads consider using larger value resistors. However, using too high of resistance causes the circuit to be more susceptible to noise; and, voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.760 \times \left(1 + \frac{R1}{R2} \right) \quad (1)$$

8.2.2.3 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (2)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 2 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)			C8 + C9 (μF)
			MIN	TYP	MAX	
1	3.09	10.0	1	2.2	4.7	20 to 68
1.05	3.74	10.0	1	2.2	4.7	20 to 68
1.2	5.76	10.0	1	2.2	4.7	20 to 68
1.5	9.53	10.0	1.5	2.2	4.7	20 to 68
1.8	13.7	10.0	1.5	2.2	4.7	20 to 68
2.5	22.6	10.0	2.2	2.2	4.7	20 to 68
3.3	33.2	10.0	2.2	2.2	4.7	20 to 68
5	54.9	10.0	3.3	3.3	4.7	20 to 68
6.5	75	10.0	3.3	3.3	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 3, Equation 4, and Equation 5. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 550 kHz for f_{SW} . Make sure the chosen inductor is rated for the peak current of Equation 4 and the RMS current of Equation 6.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (3)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (4)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (5)$$

For this design example, the calculated peak current is 5.4 A and the calculated RMS current is 5 A. The inductor used is a WE 744311220 with a peak current rating of 13 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS565208 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 μF to 68 μF. Use Equation 6 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (6)$$

For this design two TDK C3216X5R0J226M 22-μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.229 A.

8.2.2.4 Input Capacitor Selection

The TPS565208 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 μF for the decoupling capacitor. An additional 0.1-μF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.5 Bootstrap Capacitor Selection

A 0.1- μ F ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.3 Application Curves

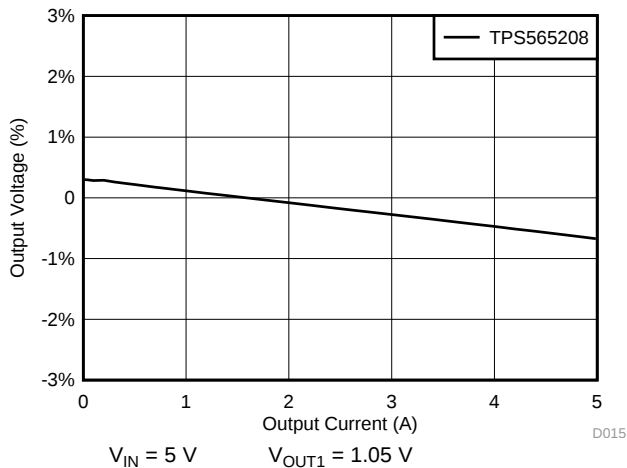


Figure 15. TPS565208 Load Regulation, $V_{IN} = 5\text{ V}$

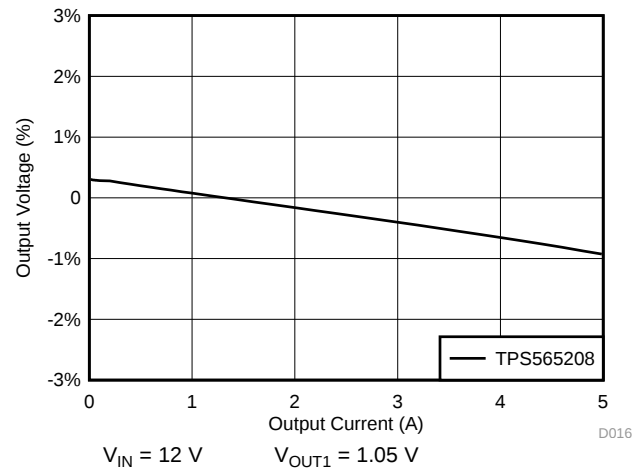


Figure 16. TPS565208 Load Regulation, $V_{IN} = 12\text{ V}$

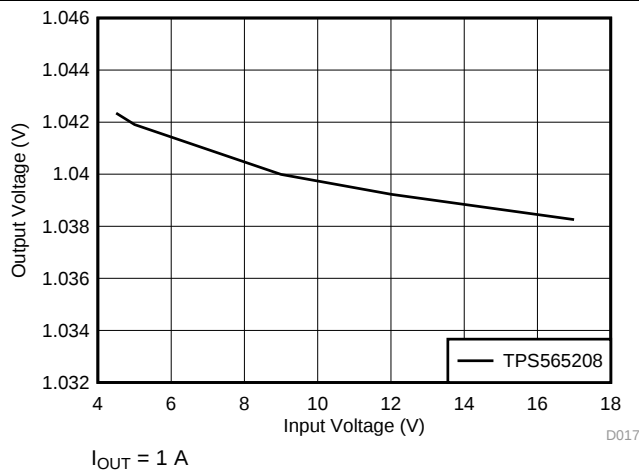


Figure 17. TPS565208 Line Regulation

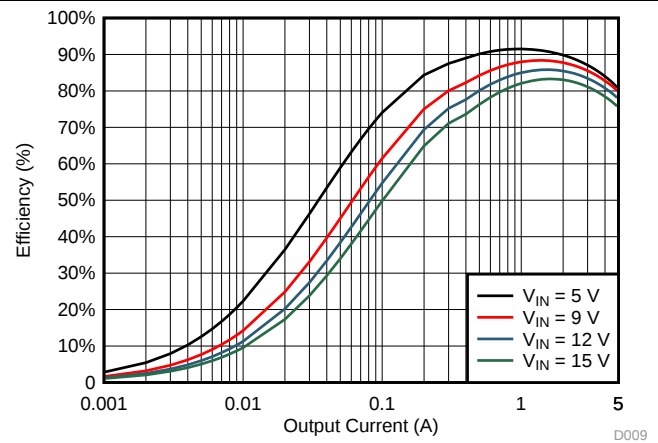


Figure 18. TPS565208 Efficiency, $V_{out} = 1.05\text{ V}$

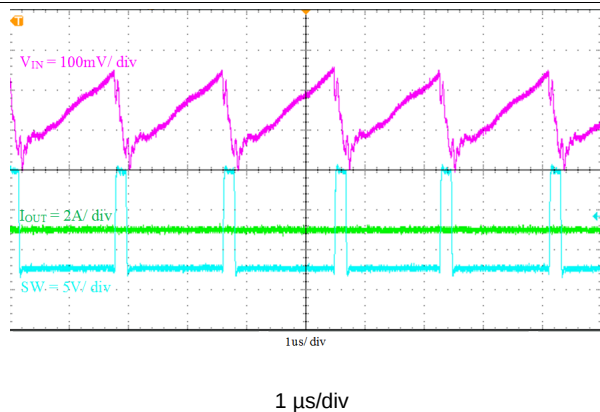


Figure 19. TPS565208 Input Voltage Ripple

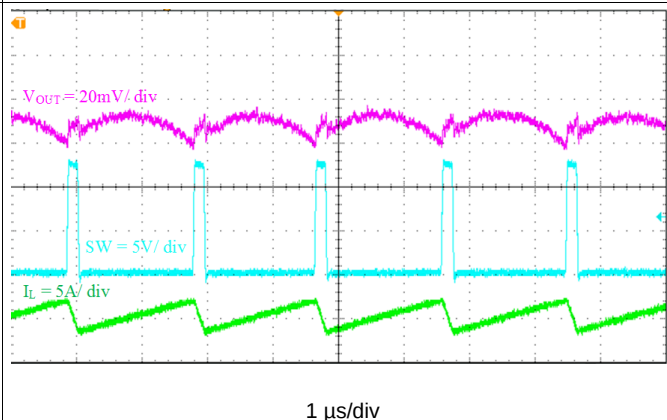
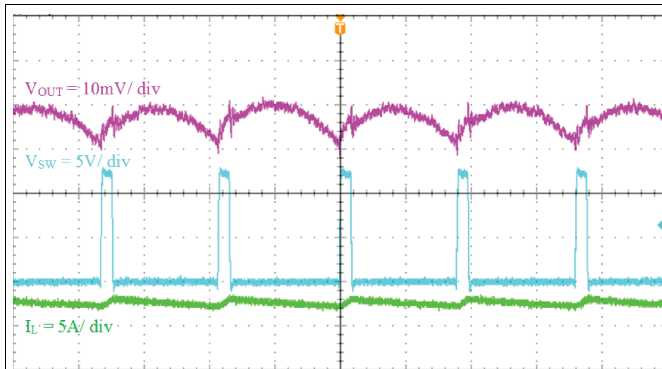
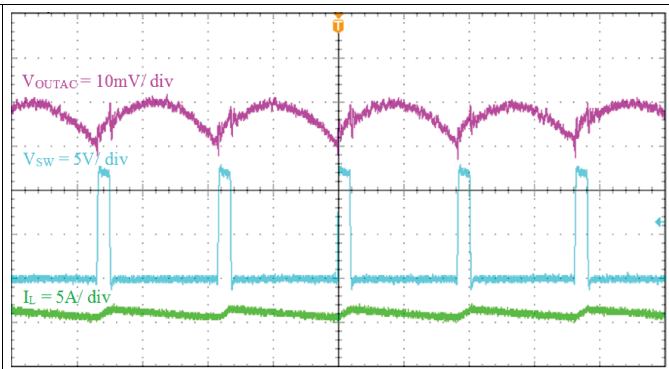


Figure 20. TPS565208 Output Voltage Ripple, No Load



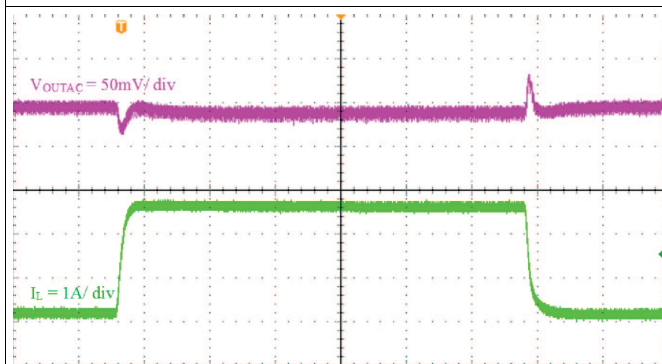
1 μ s/div

Figure 21. TPS565208 Output Voltage Ripple, I_{OUT} 2.5 A



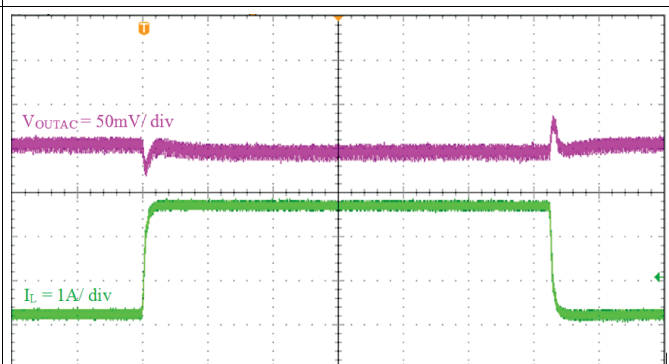
1 μ s/div

Figure 22. TPS565208 Output Voltage Ripple, I_{OUT} 5 A



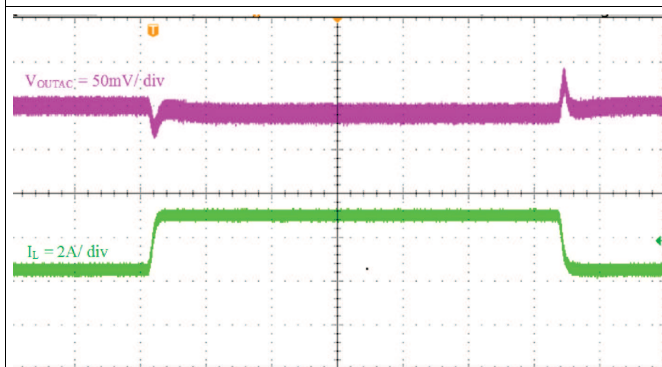
100 μ s/div

Figure 23. TPS565208 Transient Response 0.1 to 2.5 A



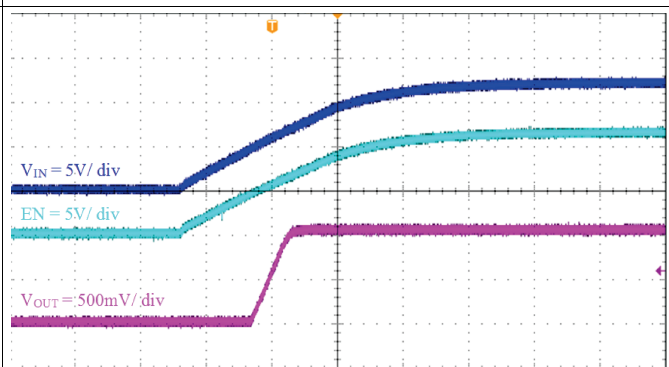
100 μ s/div

Figure 24. TPS565208 Transient Response, 1.25 to 3.75 A



100 μ s/div

Figure 25. TPS565208 Transient Response, 2.5 to 5 A



2 ms/div

Figure 26. TPS565208 Startup Relative to V_{IN}

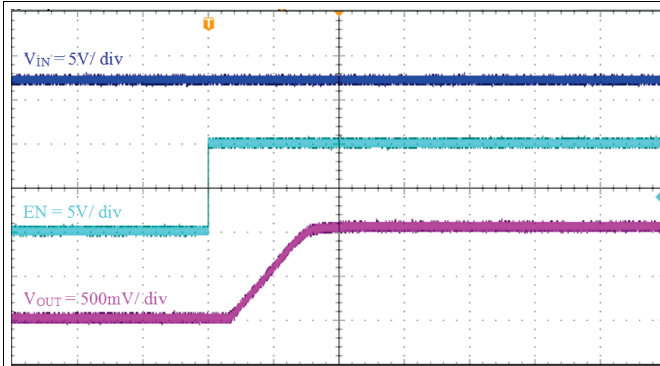
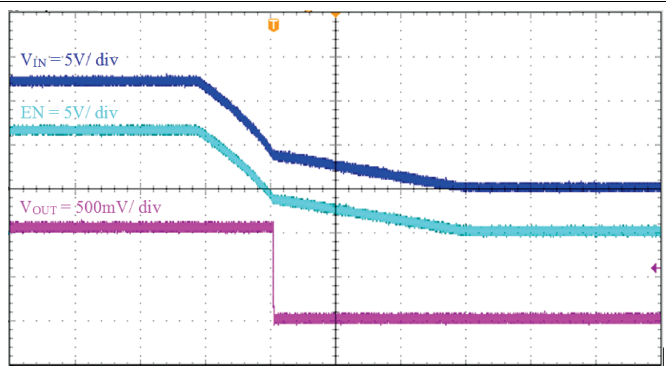

 400 μ s/div

Figure 27. TPS565208 Startup Relative to EN


20 ms/div

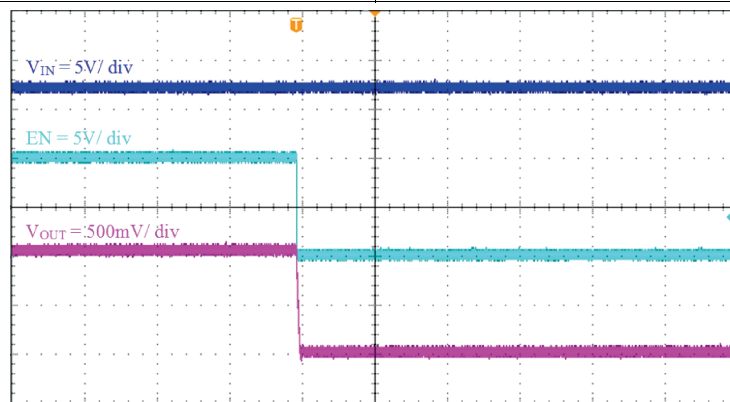
Figure 28. TPS565208 Shutdown Relative to V_{IN}

 400 μ s/div

Figure 29. TPS565208 Shutdown Relative to EN

9 Power Supply Recommendations

The TPS565208 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 83%. Using that criteria, the minimum recommended input voltage is $V_O / 0.83$.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

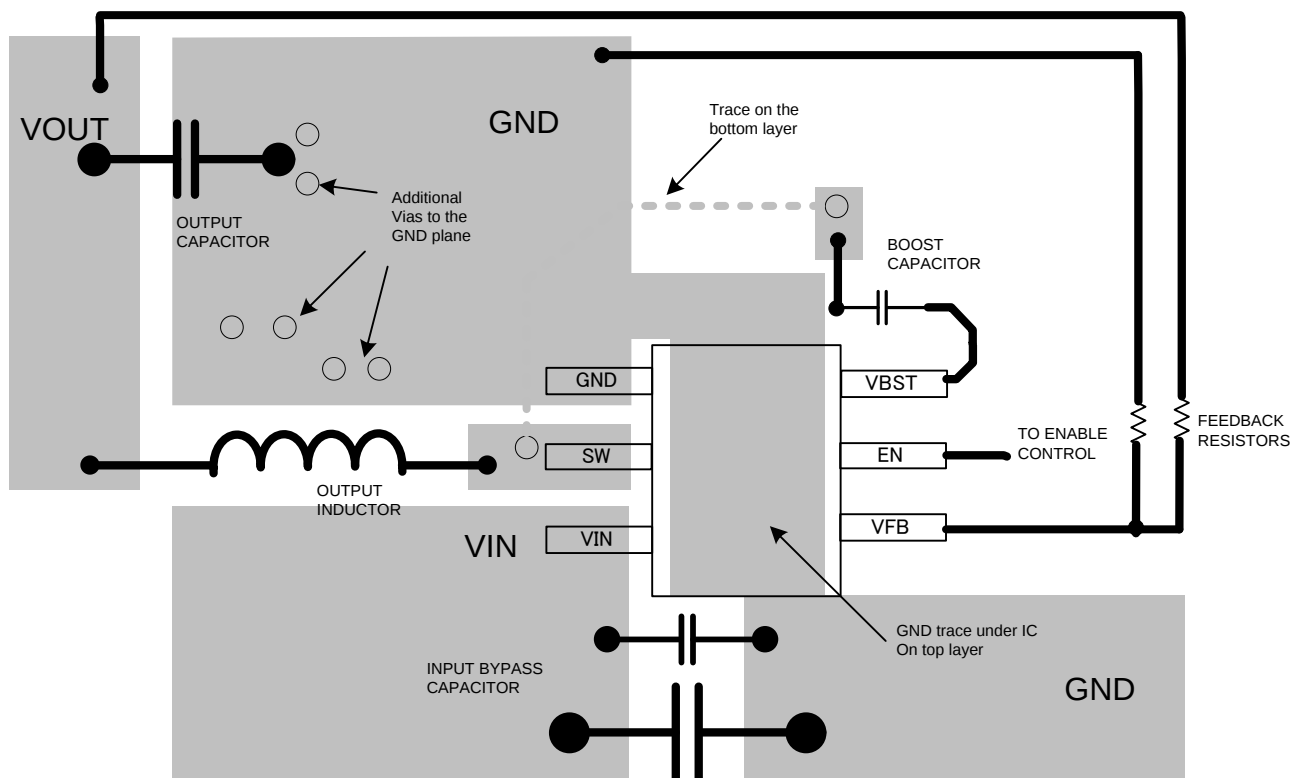


Figure 30. TPS565208 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 開発サポート

11.1.1 WEBENCH®ツールによるカスタム設計

[ここをクリック](#)すると、WEBENCH® Power Designerにより、TPS565208デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

D-CAP2, E2E are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

Blu-ray is a trademark of Blu-ray Disc Association.

11.5 静電気放電に関する注意事項



これらのデバイスは、限定的なESD (静電破壊) 保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS565208DDCR	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5208
TPS565208DDCR.A	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5208
TPS565208DDCT	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5208
TPS565208DDCT.A	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5208

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS565208DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS565208DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

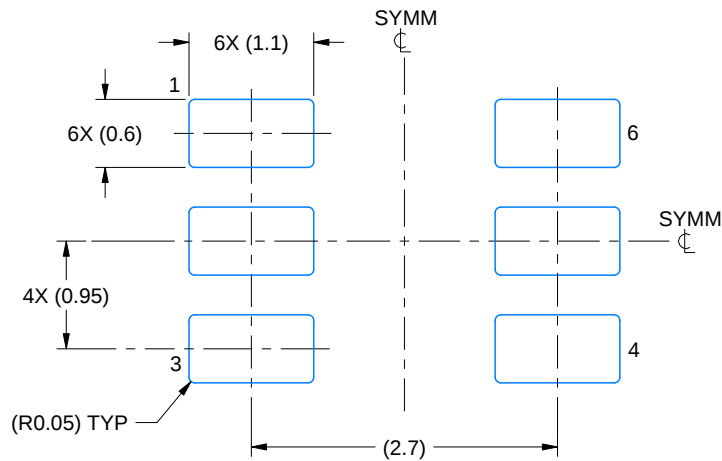
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS565208DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS565208DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

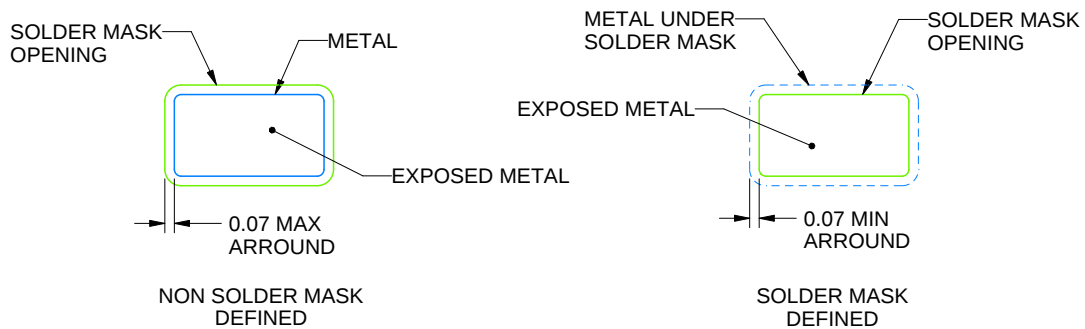
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X

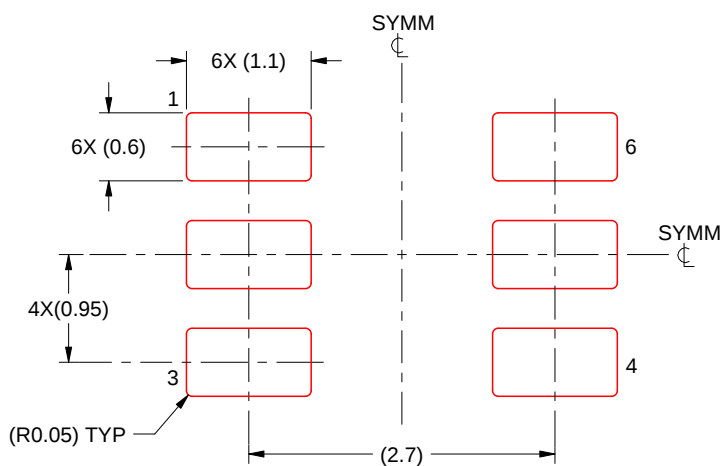


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated