TPS56424x 3V～16V 入力電圧、4A 同期整流降圧コンバータ、SOT-563 パッケージ

1 特長

- 多様なアプリケーションに適した構成
  - 3V～16V の入力電圧範囲
  - 0.6V～7V の出力電圧範囲
  - 0.6V の基準電圧
  - 25℃で ±1% の基準電圧精度
  - –40℃～125℃で ±1.5% の基準電圧精度
  - R_{DSON} 28.8mΩ および 15.4mΩ の FET を内蔵
  - 低い静止電流：120μA
  - 1.2MHz のスイッチング周波数
  - 最大 95% のデューティ・サイクル動作をサポート
  - 高精度の EN スレッショルド電圧
  - 1.39ms (標準値) の固定ソフトスタート時間
- 使いやすく小さいソリューション・サイズ
  - 軽負荷時の Eco モード (TPS564242) および FCCM モード (TPS564247)
  - 4A、5A、6A および FCCM/Eco 動作のためのソリューションを含む P2P ファミリ全体の一部
  - D-CAP3™ 制御トポロジ
  - あらかじめ出力にバイアスが印加された状態でのスタートアップをサポート
  - ラッチなしの OV/OT/UVLO 保護
  - ヒカップ・モードによる UV 保護
  - サイクル単位の OC および NOC 制限
  - 6 ピン SOT-563 パッケージ
- WEBENCH® Power Designer により、TPS564242 を使用するカスタム設計を作成
- WEBENCH® Power Designer により、TPS564247 を使用するカスタム設計を作成

2 アプリケーション

- LCD TV、STB および DVR、ストリーミング・メディア・プレーヤ
- IP ネットワーク・カメラ、ビデオ・ドアベル、ビルのセキュリティ・ゲートウェイ
- WLAN/Wi-Fi アクセス・ポイント、モデム (ケーブル / DSL / GFAST)、ソリッド・ステート・ドライブ

3 概要

TPS56424x は、シンプルで使いやすい、高電力密度、高効率の同期整流降圧コンバータです。このデバイスは、SOT-563 パッケージで、3V～16V の入力電圧および最大 4A の連続電流をサポートします。

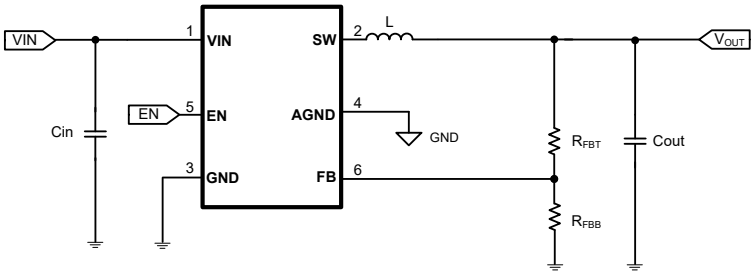
TPS56424x は、DCAP3 トポロジを採用しているため、高速過渡応答が可能で、外部補償不要で低 ESR 出力コンデンサをサポートします。このデバイスは、2 つのグランド (GND、AGND) を備えており、これらを相互に接続すれば放熱性能を最適化できます。AGND は、良好な負荷およびライン・レギュレーションにも役立ちます。このデバイスは、最大 95% のデューティでの動作をサポートできます。

TPS564242 は Eco モードで動作することで、軽負荷時も高い効率を維持します。 TPS564247 は FCCM モードで動作することで、すべての負荷条件で同じ周波数と小さい出力リップルを維持します。このデバイスは、OVP、OCP、UVLO、OTP、UVP (ヒカップ機能付き) を含む完全な保護機能を備えています。このデバイスは、PCB を簡単にレイアウトできるように最適化されたピン配置を持つ 1.6mm × 1.6mm SOT-563 パッケージで供給されます。接合部温度の仕様は –40℃～125℃です。

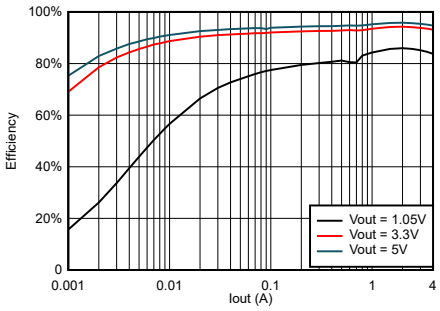
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS564242	SOT-563 (6)	1.60mm × 1.60mm
TPS564247		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



TPS564242 の効率 (V_{IN} = 12V)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
April 2022	*	Initial Release

5 Pin Configuration and Functions

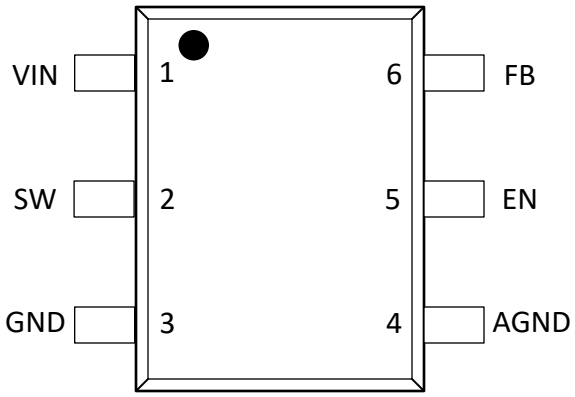


図 5-1. 6-Pin SOT-563 DRL Package (Top View)

表 5-1. Pin Functions

Pin		Type(1)	Description
Name	No.		
VIN	1	I	Input voltage supply pin
SW	2	O	Switch node connection between the high-side NFET and low-side NFET
GND	3	—	Ground pin source terminal of the low-side power NFET as well as the ground terminal for controller circuit
AGND	4	—	Ground of internal analog circuitry. Connect AGND to the GND plane.
EN	5	I	Enable input to converter. Driving EN high enables the converter.
FB	6	I	Converter feedback input. Connect to the output voltage with a feedback resistor divider.

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	18	V
	FB, EN	–0.3	6	
	AGND, PGND	–0.3	0.3	
Output voltage	SW	–2	18	V
	SW (< 20 ns)	–6.5	20	
Operating junction temperature range, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP157 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN	3		16	V
	FB, EN	–0.1		5.5	
	AGND, PGND	–0.1		0.1	
Output voltage	SW	–1		16	V
	SW (< 20 ns)	–6		18	
Output current	IO	0		6	A
T_J	Operating junction temperature	–40		125	°C
T_{stg}	Storage temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRL (SOT-563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.1	°C/W
$R_{\theta JA\_effective}$ (2)	Junction-to-ambient thermal resistance on EVM board	58	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Y_{JB}	Junction-to-board characterization parameter	16.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) This $R_{\theta JA\_effective}$ is tested on TPS564242EVM board (2 layer, copper thickness of top and bottom layer are 2 oz) at V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 4 A , T_A = 25°C.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
V_{IN}	Input voltage range	V_{IN}	3		16	V
I_{VIN}	VIN supply current	No load, V_{EN} = 5 V, V_{FB} = 0.65 V, non-switching, ECO version		120		µA
		No load, V_{EN} = 5 V, V_{FB} = 0.65 V, non-switching, FCCM version		400		µA
I_{INSDN}	VIN shutdown current	No load, V_{EN} = 0 V		2		µA
UVLO						
UVLO	VIN undervoltage lockout	Wake-up VIN voltage	2.75	2.92	3	V
UVLO	VIN undervoltage lockout	Shutdown VIN voltage	2.6	2.72	2.9	V
UVLO	VIN undervoltage lockout	Hysteresis VIN voltage		200		mV
FEEDBACK VOLTAGE						
V_{REF}	FB voltage	T_J = 25°C	594	600	606	mV
V_{REF}	FB voltage	T_J = –40°C to 125°C	591	600	609	mV
MOSFET						
$R_{DS\ (ON)HI}$ (1)	High-side MOSFET $R_{DS(ON)}$	T_J = 25°C, V_{VIN} ≥ 5 V		28.8		mΩ
	High-side MOSFET $R_{DS(ON)}$	T_J = 25°C, V_{VIN} = 3 V		30.5		mΩ
$R_{DS\ (ON)LO}$	Low-side MOSFET $R_{DS(ON)}$	T_J = 25°C, V_{VIN} ≥ 5 V		15.4		mΩ
$R_{DS\ (ON)LO}$	Low-side MOSFET $R_{DS(ON)}$	T_J = 25°C, V_{VIN} = 3 V		16.3		mΩ
I_{OCL_LS}	Overcurrent threshold	Valley current setpoint	4.5	6	7.5	A
I_{NOCL}	Negative overcurrent threshold		1.5	2.5	3.5	A
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	T_J = 25°C, V_{VOUT} = 3.3 V		1200		kHz
$T_{ON(MIN)}$ (1)	Minimum on time	T_J = 25°C		50		ns
$T_{OFF(MIN)}$ (1)	Minimum off time	V_{FB} = 0.5 V		100		ns
LOGIC THRESHOLD						
$V_{EN(ON)}$	EN threshold high level		1.07	1.18	1.33	V
$V_{EN(OFF)}$	EN threshold low level		0.95	1	1.2	V
V_{ENHYS}	EN hystersis			180		mV
REN1	EN pulldown resistor			2		MΩ
SOFT START						
t_{SS}	Internal soft-start time			1.39		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold		115%	120%	125%	
t_{OVPDLY}	OVP prop deglitch	T_J = 25°C		24		µs
V_{UVP}	UVP trip threshold		55%	60%	65%	
t_{UVPDLY}	UVP prop deglitch			256		µs
t_{UVPDEL}	Output hiccup delay relative to SS time	UVP detect		256		µs
t_{UVPEN}	Output hiccup enable delay relative to SS time	UVP detect		13		ms
THERMAL PROTECTION						
T_{OTP} (2)	OTP trip threshold			155		°C

6.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{OTPHSY} (2)	OTP hysteresis			20		°C

(1) Specified by design
(2) Not production tested

6.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

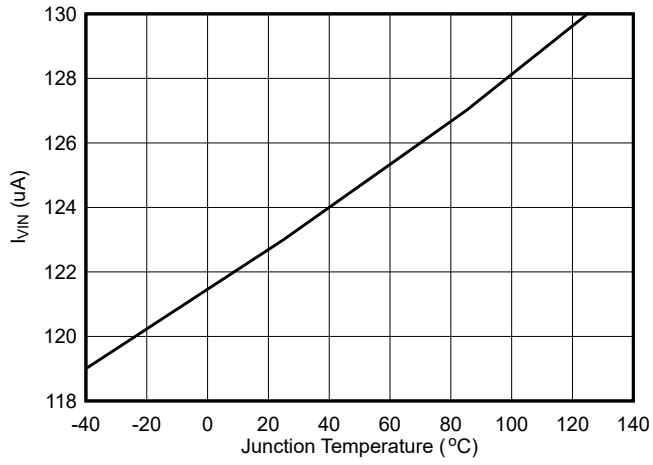


図 6-1. TPS564242 Quiescent Current

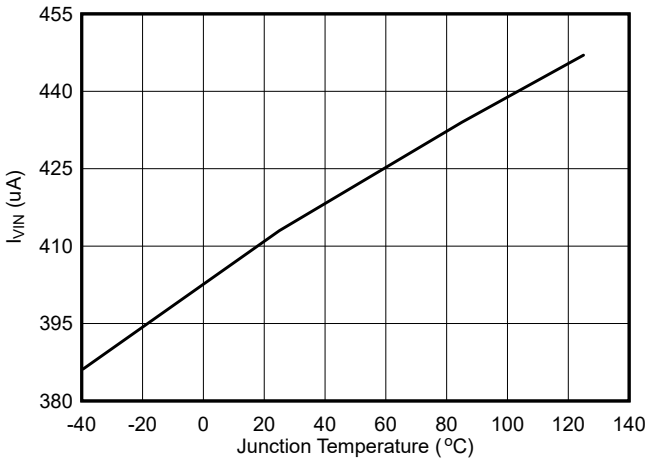


図 6-2. TPS564247 Quiescent Current

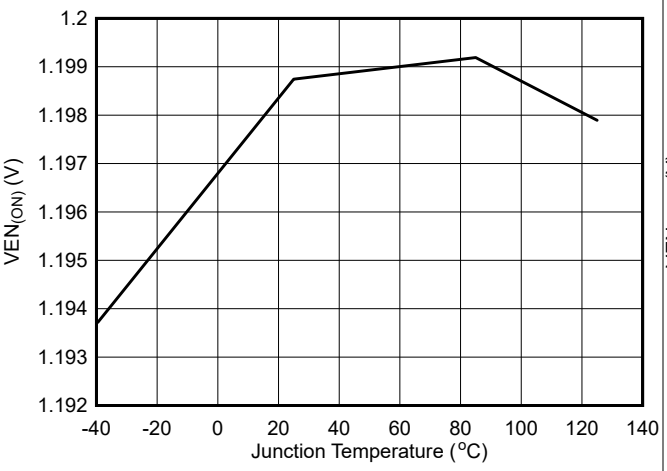


図 6-3. Enable On Threshold Voltage

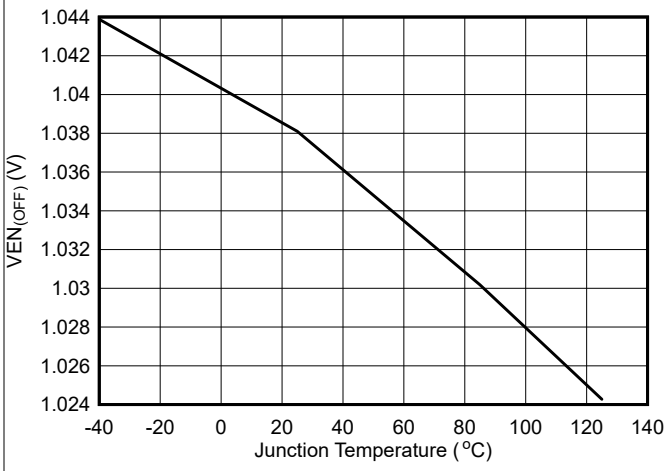


図 6-4. Enable Off Threshold Voltage

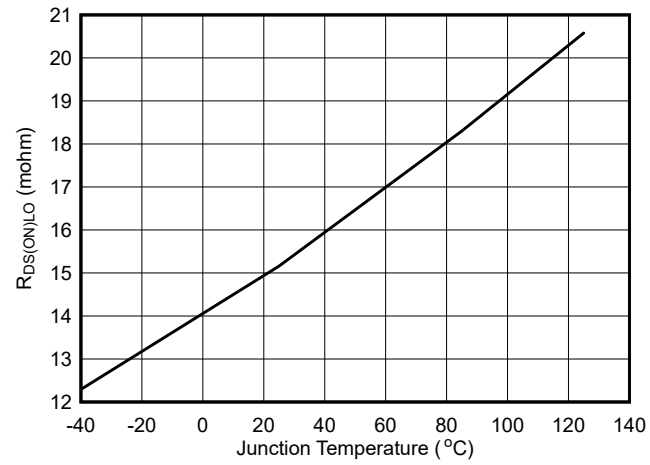


図 6-5. Low-Side $R_{DS(ON)}$

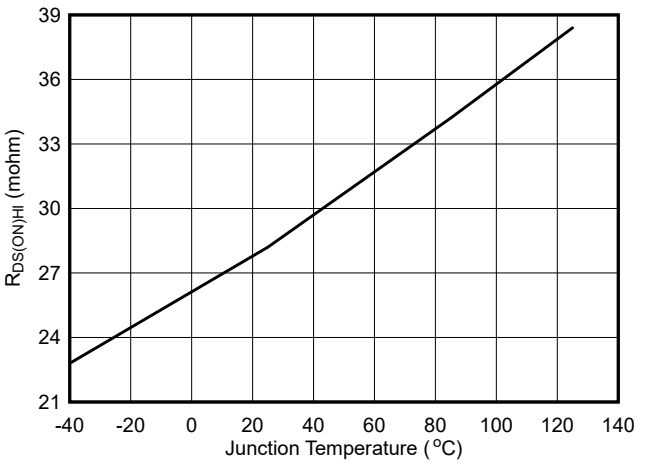


図 6-6. High-Side $R_{DS(ON)}$

6.6 Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

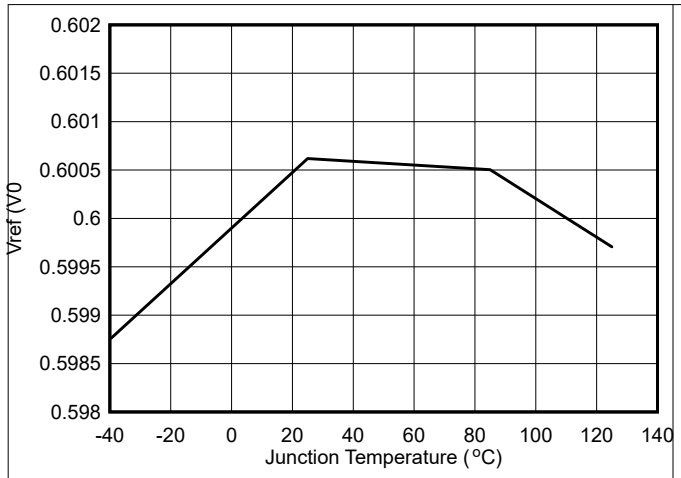


図 6-7. V_{REF} Voltage

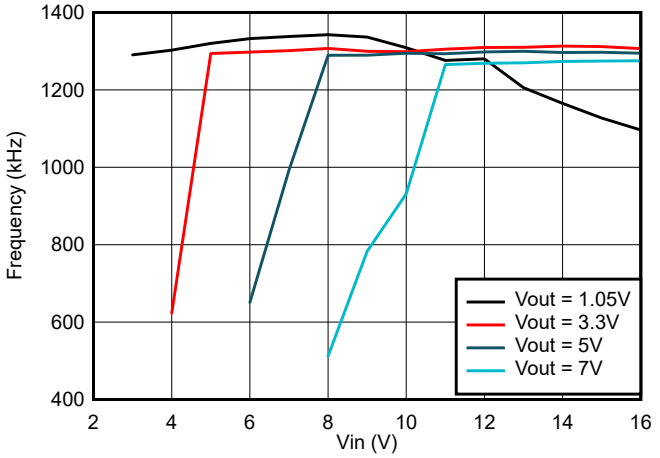


図 6-8. Frequency vs Input Voltage at 4-A Loading

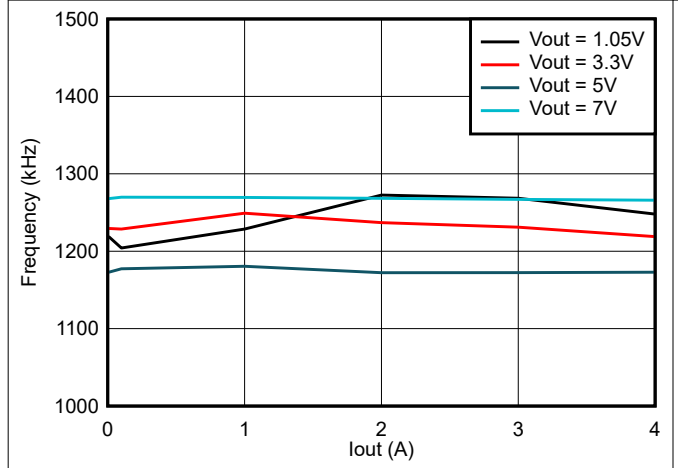


図 6-9. TPS564247 Frequency vs Loading

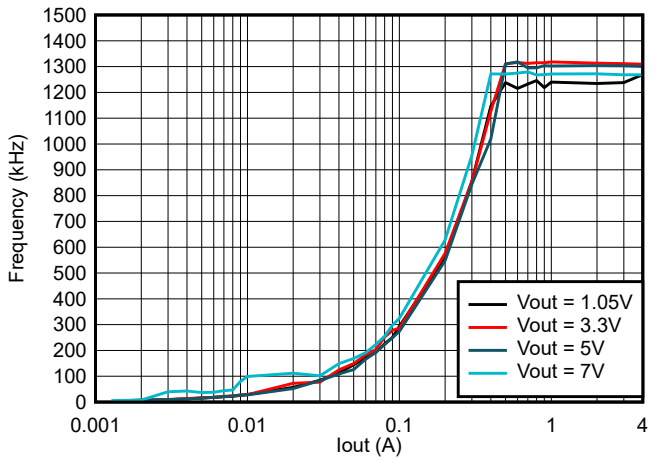


図 6-10. TPS564242 Frequency vs Loading

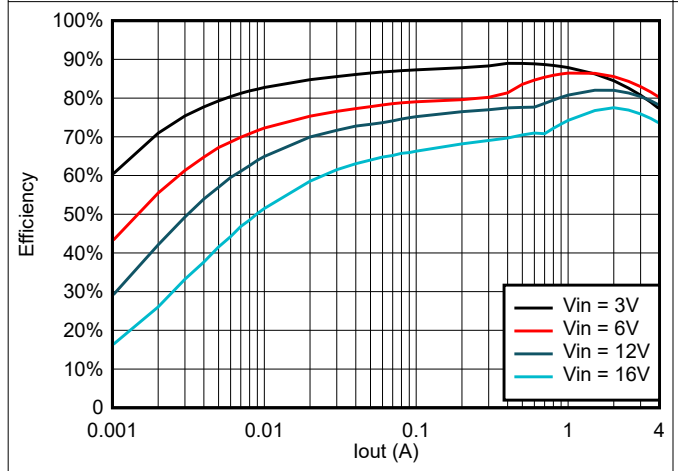


図 6-11. TPS564242 Efficiency at 0.6 V_{OUT} with a 0.82-µH Inductor

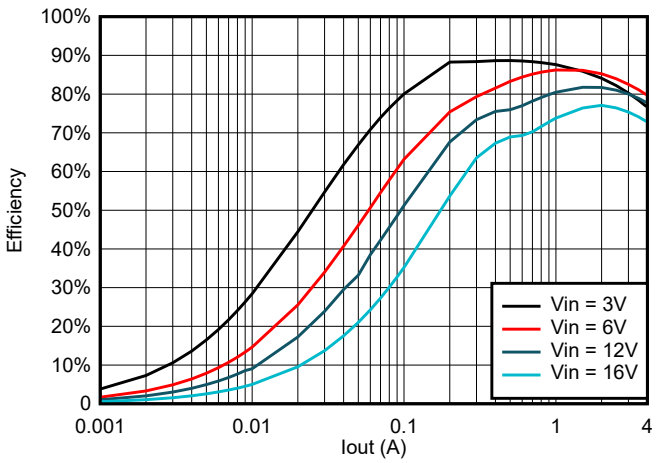


図 6-12. TPS564247 Efficiency at 0.6 V_{OUT} with a 0.82-µH Inductor

6.6 Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

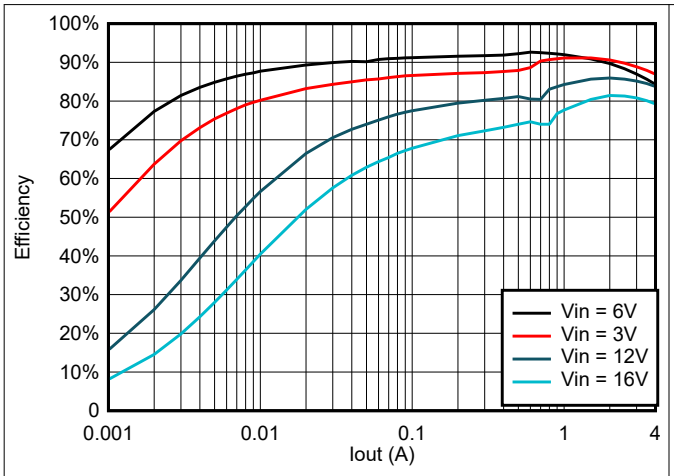


図 6-13. TPS564242 Efficiency at 1.05 V_{OUT} with a 0.82-µH Inductor

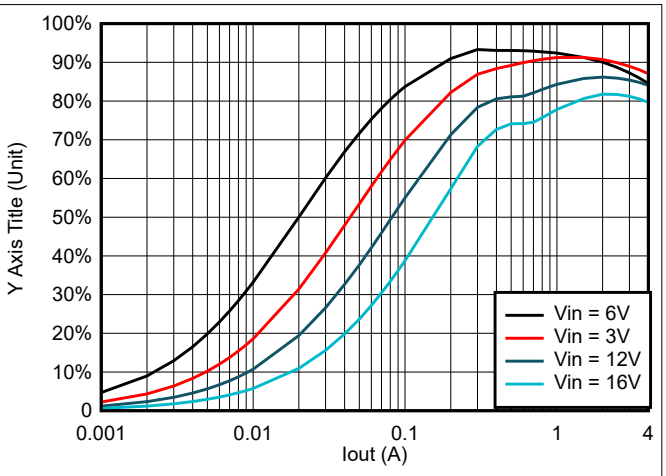


図 6-14. TPS564247 Efficiency at 1.05 V_{OUT} with a 0.82-µH Inductor

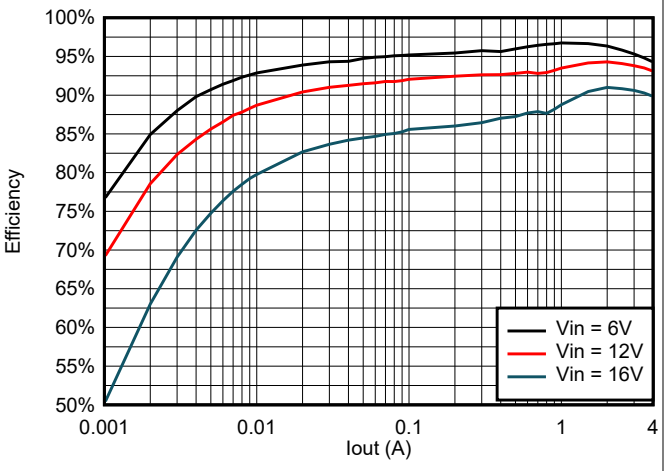


図 6-15. TPS564242 Efficiency at 3.3 V_{OUT} with a 1.5-µH Inductor

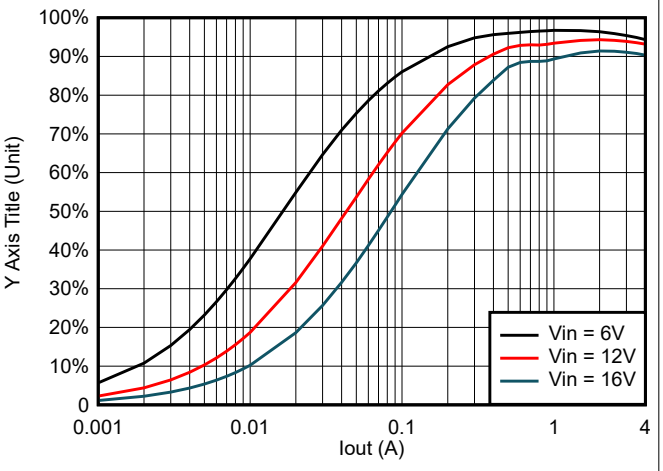


図 6-16. TPS564247 Efficiency at 3.3 V_{OUT} with a 1.5-µH Inductor

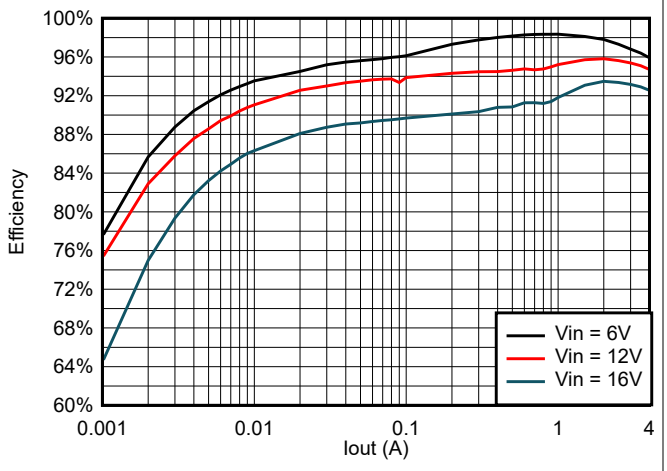


図 6-17. TPS564242 Efficiency at 5 V_{OUT} with a 1.8-µH Inductor

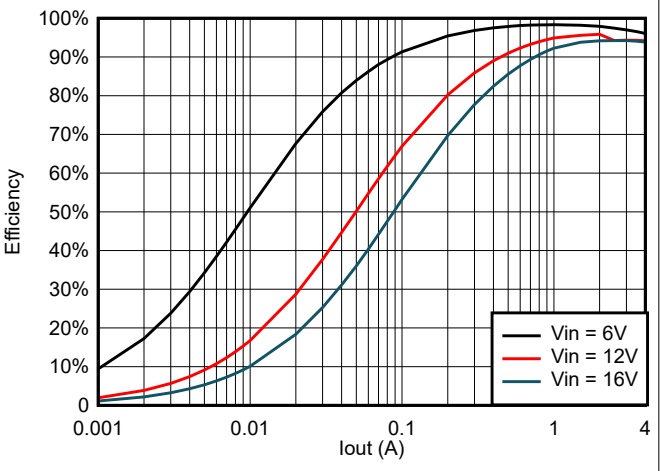


図 6-18. TPS564247 Efficiency at 5 V_{OUT} with a 1.8-µH Inductor

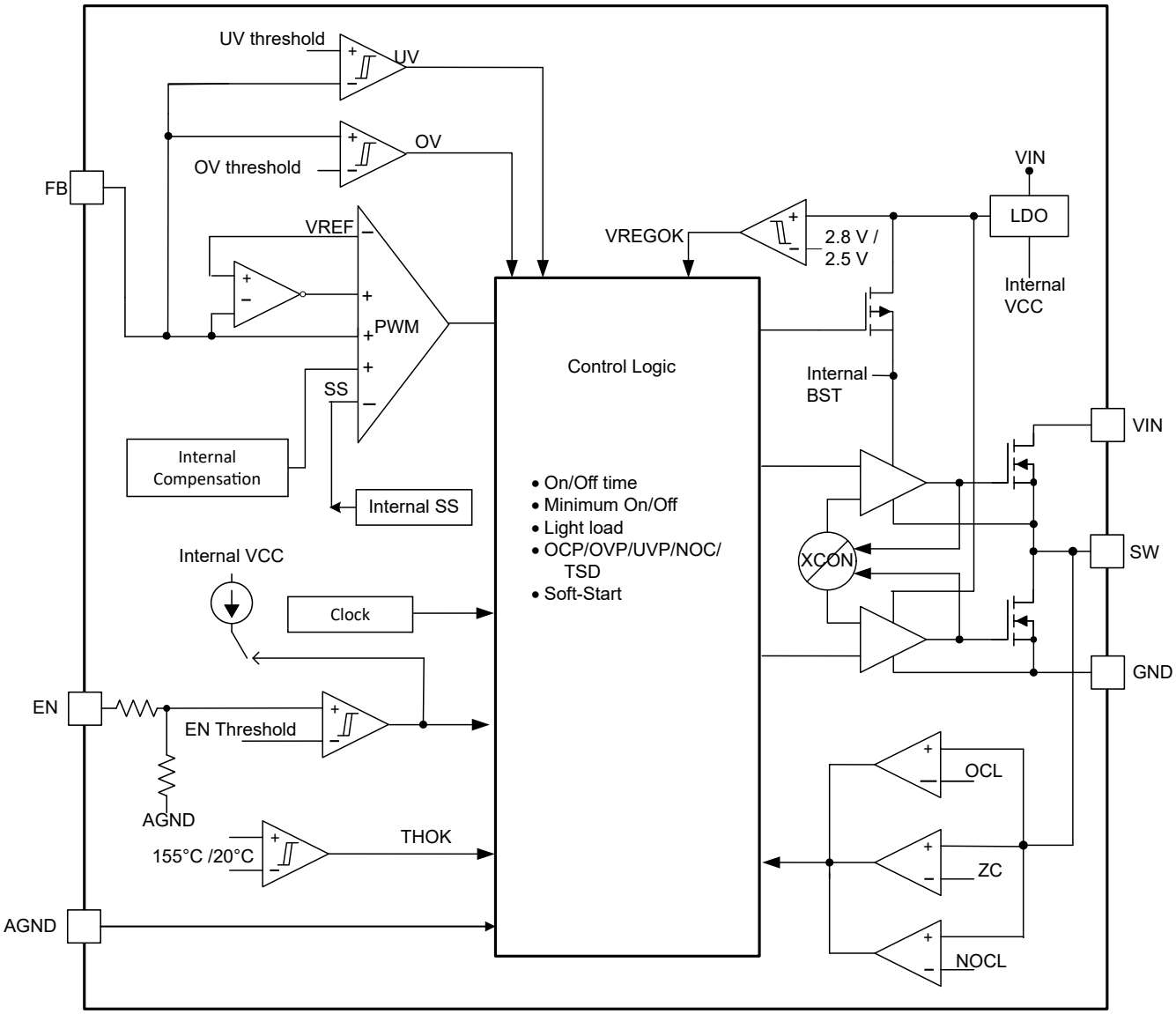
7 Detailed Description

7.1 Overview

The TPS56424x is a 4-A integrated FET and BST pin synchronous step-down buck converter that operates from 3-V to 16-V input voltage (V_{IN}) and 0.6-V to 7-V output voltage. This device also integrates the BST pin in an internal IC and adds one AGND pin. The device employs D-CAP3 topology that provides fast transient response with no external compensation components and an accurate feedback voltage. The proprietary D-CAP3 mode enables low external component count, ease of design, and optimization of the power design for cost, size, and efficiency. The topology provides a seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition.

The Eco-mode version allows the TPS564242 to maintain high efficiency at light load. The FCCM version allows the TPS564247 to maintain a fixed switching frequency and lower output voltage ripple. The TPS56424x is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3 Control

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3 mode control. The DCAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS56424x also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the converter input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to the reference voltage to emulate the output ripple, enabling the use of very low-ESR output capacitors such as multilayered ceramic capacitors (MLCC). No external current sense network or loop compensation is required for DCAP3 control topology.

7.3.2 Eco-Mode Control

The TPS56424x is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current and keeps the light load efficiency high. The transition point to the light load operation, $I_{OUT(LL)}$ current, can be calculated in 式 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Soft Start and Prebiased Soft Start

The TPS56424x has an internal fixed soft start. The EN default status is low. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage, V_{FB}. This scheme makes sure that the converter ramps up smoothly into the regulation point.

7.3.4 Overvoltage Protection

The TPS56424x has the overvoltage protection feature. When the output voltage becomes higher than the OVP threshold, OVP is triggered with a 24-µs deglitch time. Both the high-side MOSFET driver and the low-side MOSFET driver are turned off. When the overvoltage condition is removed, the device returns to switching.

7.3.5 Large Duty Operation

The TPS56424x can support large duty operations up to 95% by smoothly dropping down the switching frequency. When V_{IN} / V_{OUT} < 1.6 and V_{FB} is lower than internal V_{REF}, the switching frequency is allowed to smoothly drop to make TON extended to implement the large duty operation and improve the performance of the load transient performance. Please refer frequency test waveform in 図 6-18. The minimum switching frequency is limited to about 450 kHz.

7.3.6 Current Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by the following:

- V_{IN}
- V_{OUT}
- On time
- Output inductor value

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, I_{OUT}. If the monitored valley current is above the OCL level, the converter maintains a low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter, which can cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects it and the device shuts down after the UVP delay time (typically 256 µs) and restarts after the hiccup wait time (typically 13 ms).

When the overcurrent condition is removed, the output voltage returns to the regulated value.

The TPS564247 is a FCCM mode part. In this mode, the device has negative inductor current at light loading. The device has NOC (negative overcurrent) protection to avoid too large negative current. NOC protection detects the valley of inductor current. When the valley value of inductor current exceeds the NOC threshold, the IC turns off the low side then turns on the high side. When the NOC condition is removed, the device returns to normal switching.

Because the TPS564247 is a FCCM mode port, if the inductance is so small that the device trigger NOC, it will cause output voltage to be higher than target value. The minimum inductance is identified as 式 2.

$$L = \frac{V_{out} \times \left(1 - \frac{V_{out}}{V_{in}}\right)}{2 \times Frequency \times NOC_{min}} \tag{2}$$

7.3.7 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.8 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value, the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Eco-Mode Operation

The TPS564242 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on

time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

7.4.2 FCCM Mode Control

The TPS564247 operates in forced CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency (FSW) is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is typical buck DC/DC converters. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 4 A. The following design procedure can be used to select component values for the TPS56424x. Alternately, the WEBENCH® software can be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in 図 8-1 was developed to meet the requirements in 表 8-1. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

図 8-1 shows the TPS56424x 12-V input, 1.05-V output converter schematic.

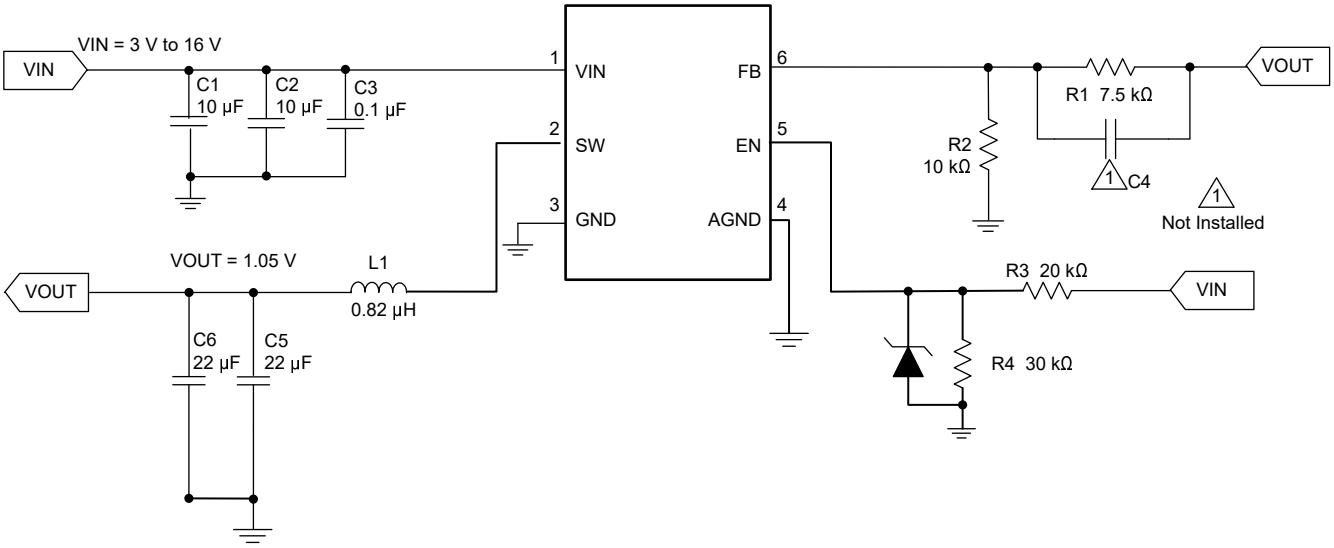


図 8-1. Schematic

8.2.1 Design Requirements

表 8-1 shows the design parameters for this application.

表 8-1. Design Parameters

Parameter	Example Value
Input voltage range	3 to 16 V
Output voltage	1.05 V
Transient response, 2.5-A load step	ΔVout = ±5%
Output ripple voltage	20 mV
Output current rating	4 A
Operating frequency	1200 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS564242 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS564247 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 式 3 to calculate V_{OUT}.

To improve efficiency at very light loads, consider using larger value resistors because too high of resistance will be more susceptible to noise and voltage errors from the FB input current will be more noticeable. It is suggested to use a 10-kΩ resistor for R2 to start the design.

$$V_{OUT} = 0.6 \times (1 + \frac{R1}{R2}) \tag{3}$$

8.2.2.3 Output Filter Selection

The LC filter used as the output filter has a double pole at 式 4. In this equation, C_{OUT} should use its effective value after derating, not its nominal value.

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{4}$$

For any control topology that is compensated internally, there is a range of the output filter it can support. At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops has a 180 degree drop. The internal ripple generation network introduces a

high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is about 100 kHz. The inductor and capacitor selected for the output filter is recommended that the double pole is located about 30 kHz, so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency (FSW).

表 8-2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	Minimum L1 (µH)	Typical L1 (µH)(1)	Maximum L1 (µH)	Minimum C_{OUT} (µF)	Typical C_{OUT} (µF)(1)	Maximum C_{OUT} (µF)	CFF (pF)
0.6	0	10.0	0.33	0.82	2.2	22	44	100	—
1.05	7.5	10.0	0.47	0.82	2.2	22	44	100	—
1.8	20.0	10.0	0.68	1.0	2.2	22	44	100	10–470
2.5	95.0	30.0	1	1.5	4.7	22	44	100	10–470
3.3	135.0	30.0	1.2	1.5	4.7	22	44	100	10–470
5	220.0	30.0	1.5	1.8	4.7	22	44	100	10–470
7	320.0	30.0	1.8	2.2	4.7	22	44	100	10–470

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using 式 5, 式 6, and 式 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$II_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (5)$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2} \quad (6)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} II_{P-P}^2} \quad (7)$$

For this design example, the calculated peak current is 4.8 A and the calculated RMS current is 4.2 A. The inductor used is WE744311100 with 8-A saturation current and 15-A rated current.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS56424x are intended for use with ceramic or other low-ESR capacitors. Use 式 8 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (8)$$

For this design, four MuRata GRM21BR61A226ME44L 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.47 A and each output capacitor is rated for 4 A.

8.2.2.4 Input Capacitor Selection

The TPS56424x requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.3 Application Curves

The following data is tested with V_{IN} = 12 V, V_{OUT} = 1.05 V, T_A = 25°C, unless otherwise specified.

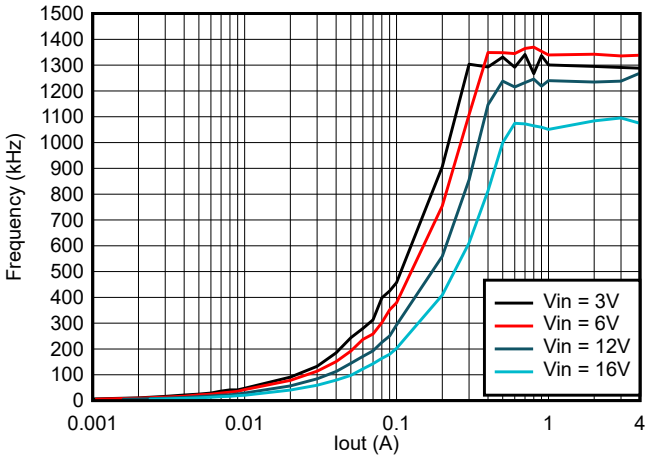


図 8-2. TPS564242 Frequency vs Loading

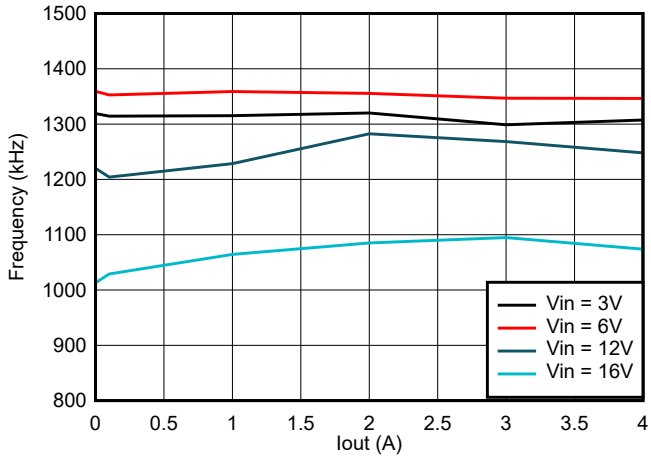


図 8-3. TPS564247 Frequency vs Loading

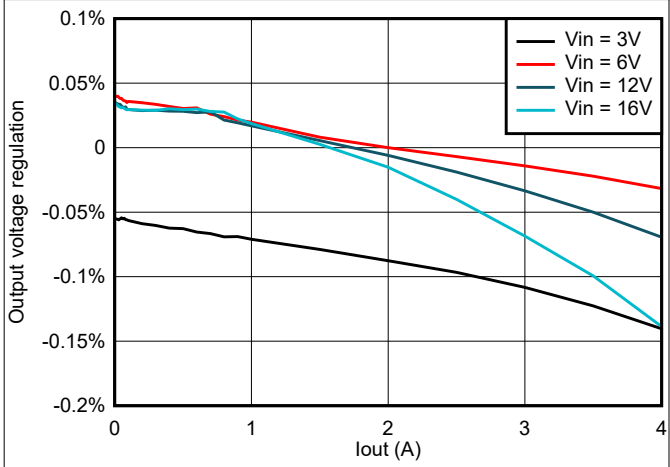


図 8-4. TPS564242 Load Regulation vs Loading

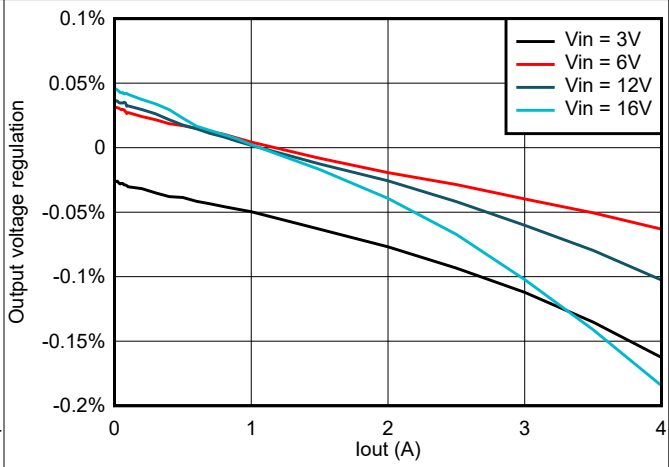


図 8-5. TPS564247 Load Regulation vs Loading

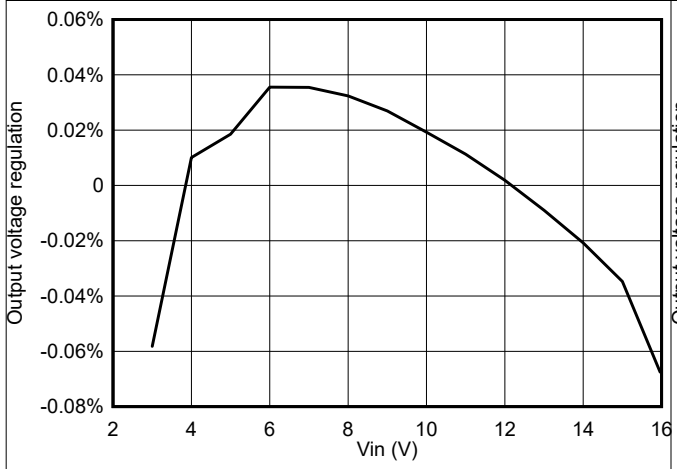


図 8-6. TPS564242 Line Regulation vs V_{IN} with 4-A Loading

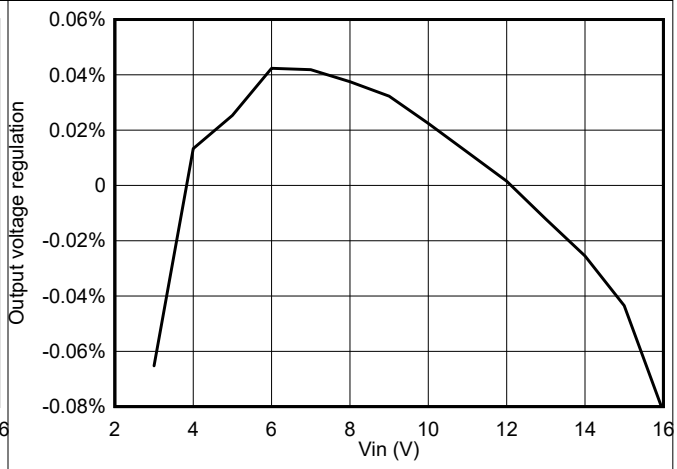


図 8-7. TPS564247 Line Regulation vs V_{IN} with 4-A Loading

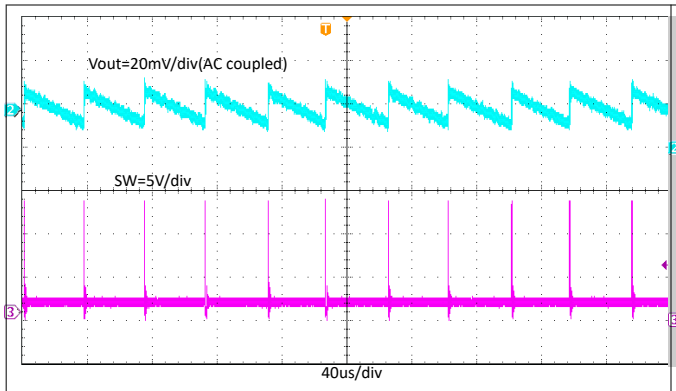


図 8-8. TPS564242 Output Voltage Ripple with 0.01-A Loading

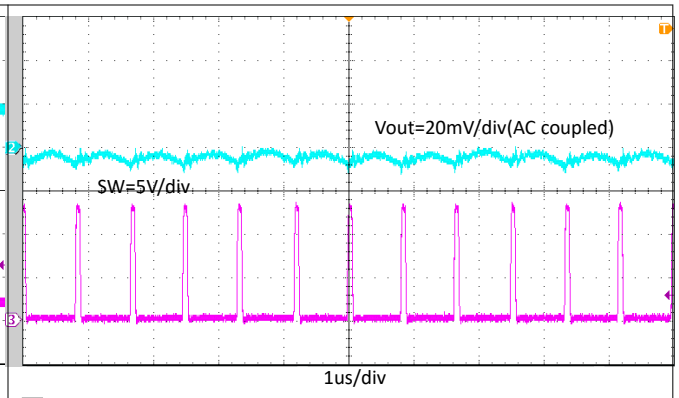


図 8-9. TPS564247 Output Voltage Ripple with 0.01-A Loading

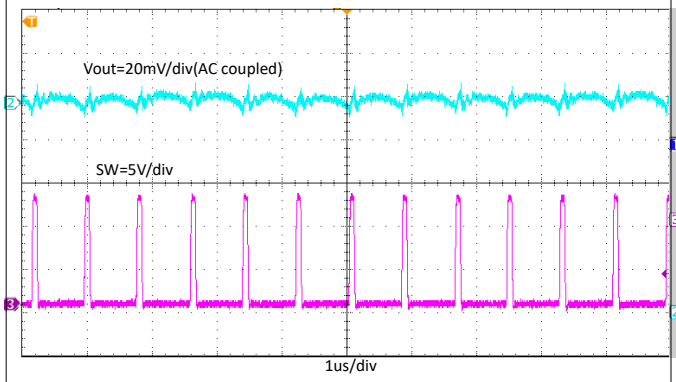


図 8-10. Output Voltage Ripple with 4-A Loading

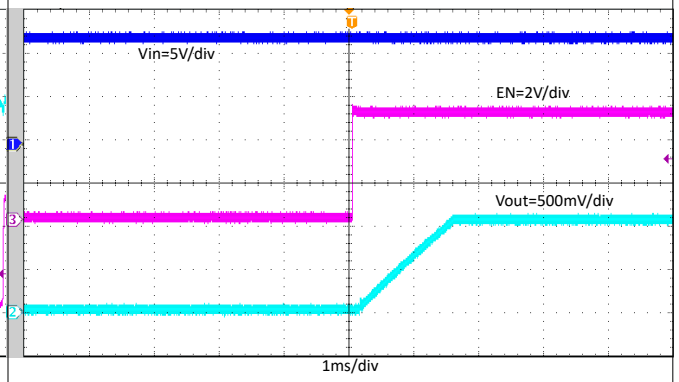


図 8-11. Start-Up Through EN, I_{OUT} = 4 A

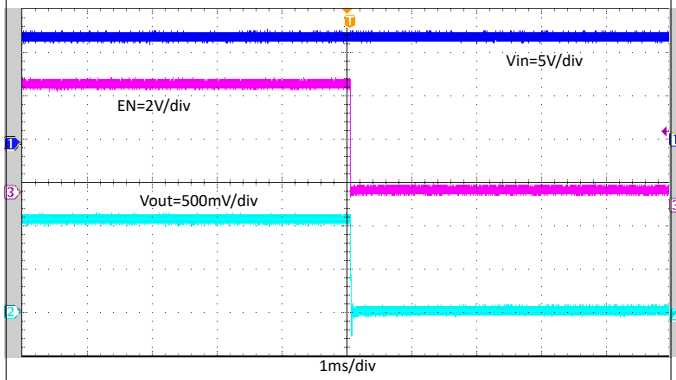


図 8-12. Shutdown Through EN, I_{OUT} = 4 A

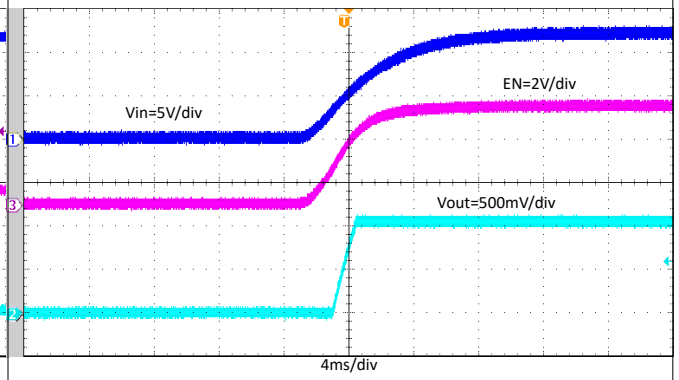


図 8-13. Start-Up with V_{IN} Rising, IOUT = 4 A

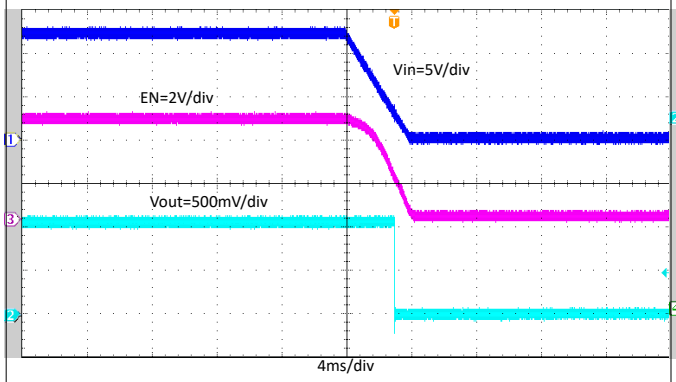


図 8-14. Start-Up with V_{IN} Falling, IOUT = 4 A

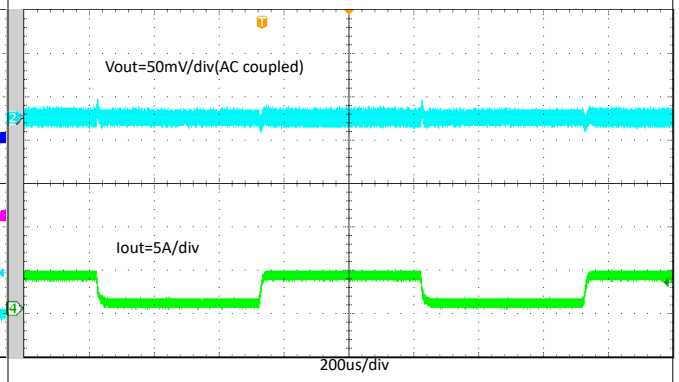


図 8-15. TPS564242 Transient Response with 0.4 A to 3.6 A by 2.5-A/µs Load Step

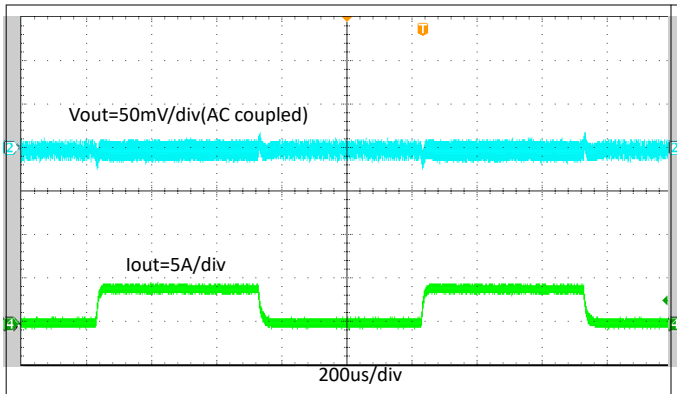


図 8-16. TPS564242 Transient Response with 0.1 A to 4 A by 2.5-A/µs Load Step

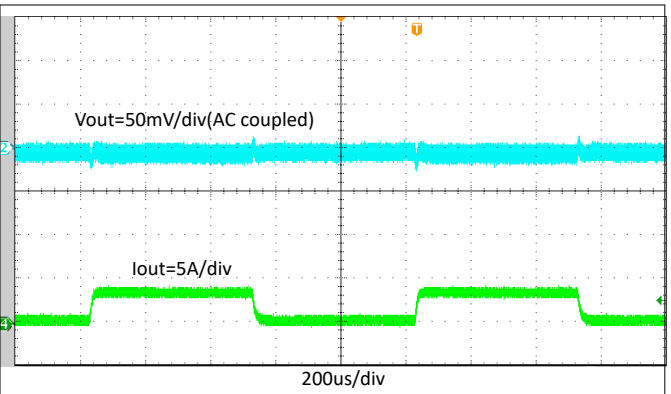


図 8-17. TPS564247 Transient Response with 0.4 A to 3.6 A by 2.5-A/µs Load Step

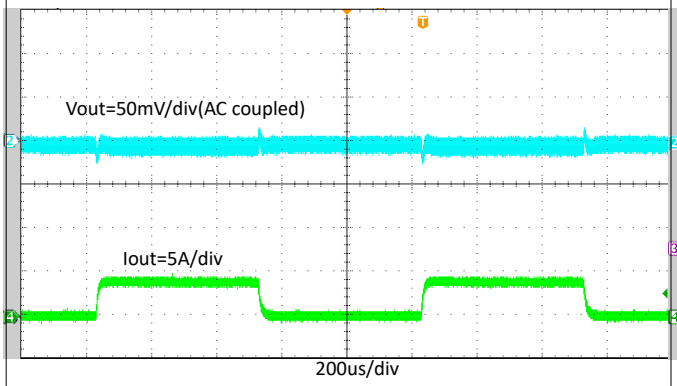


図 8-18. TPS564247 Transient Response with 0.1 A to 4 A by 2.5-A/µs Load Step

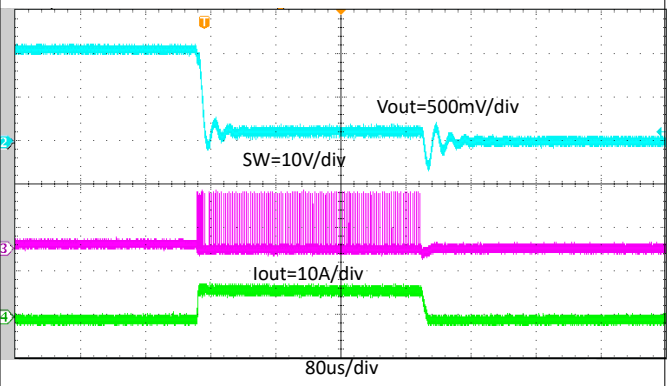


図 8-19. TPS564242 Normal Operation to Output Hard Short

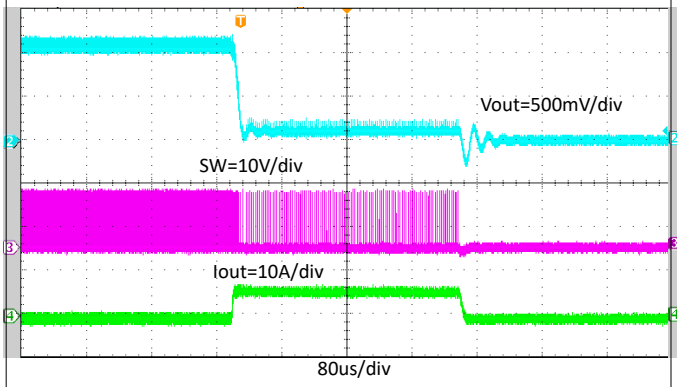


図 8-20. TPS564247 Normal Operation to Output Hard Short

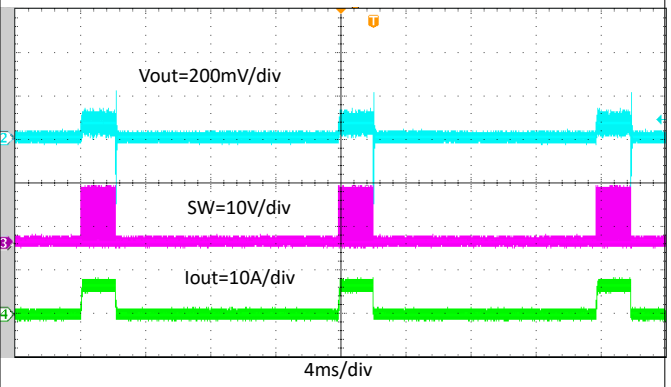


図 8-21. Output Hard Short Hiccup

9 Power Supply Recommendations

The TPS56424x are designed to operate from input supply voltages in the range of 3 V to 16 V. Buck converters require the input voltage to be higher than the output voltage for proper operation.

10 Layout

10.1 Layout Guidelines

- VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also an advantage from the view point of heat dissipation.

- The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- A separate VOUT path should be connected to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
- The trace of the FB node should be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

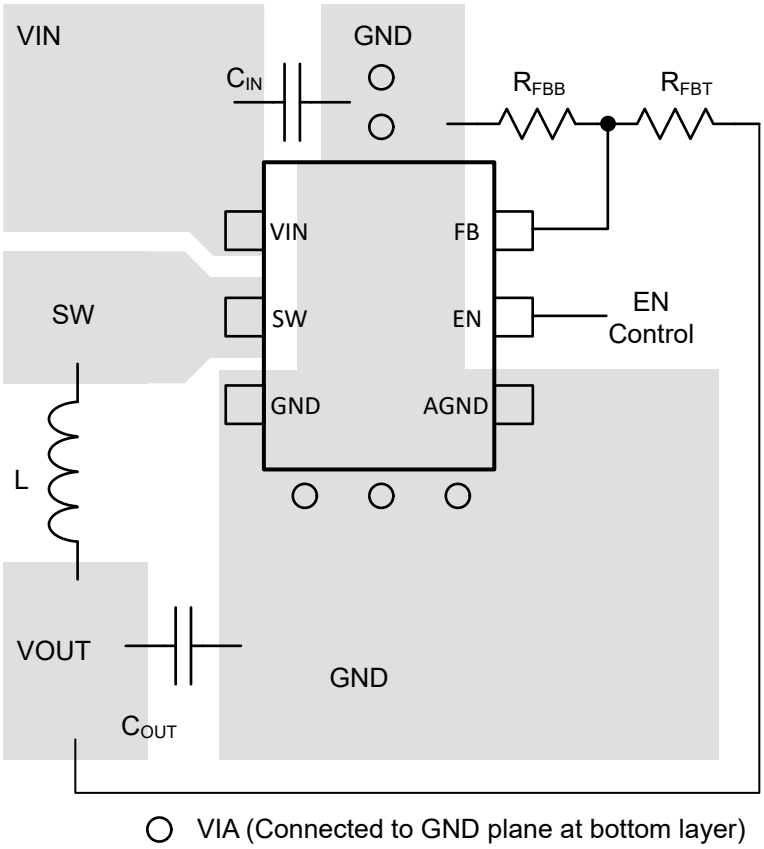


図 10-1. Suggested Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS564242 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS564247 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
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In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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WEBENCH® is a registered trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS564242DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	4242
TPS564242DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4242
TPS564247DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	4247
TPS564247DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4247

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

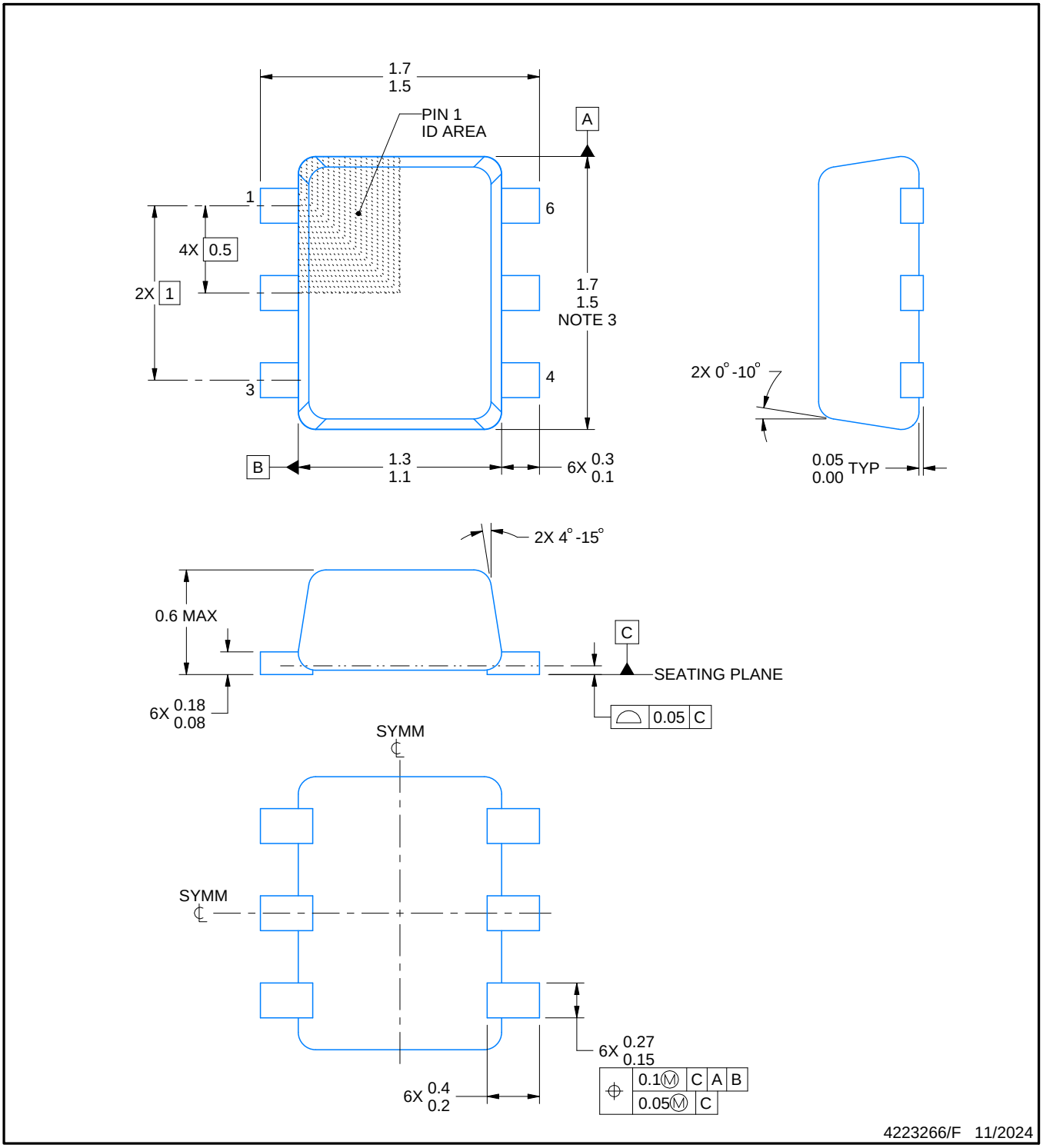
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

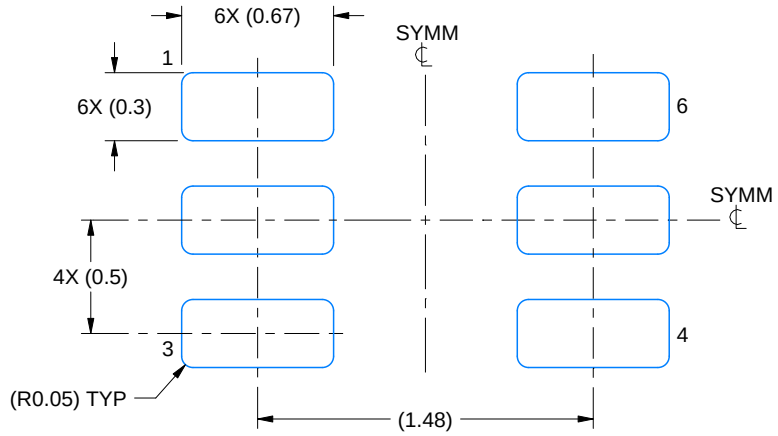
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

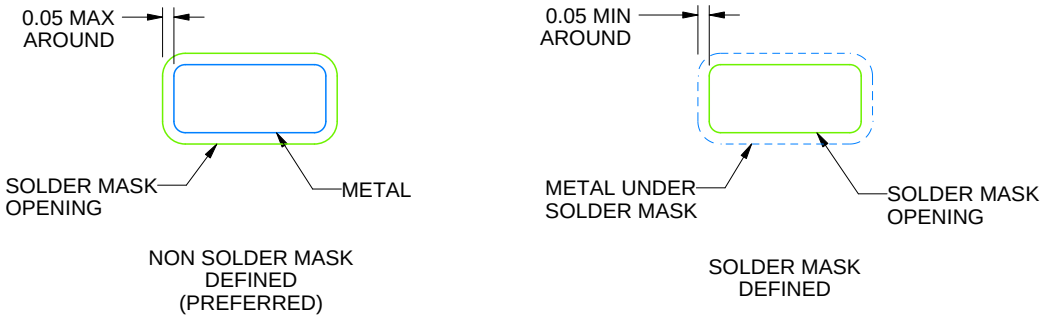
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

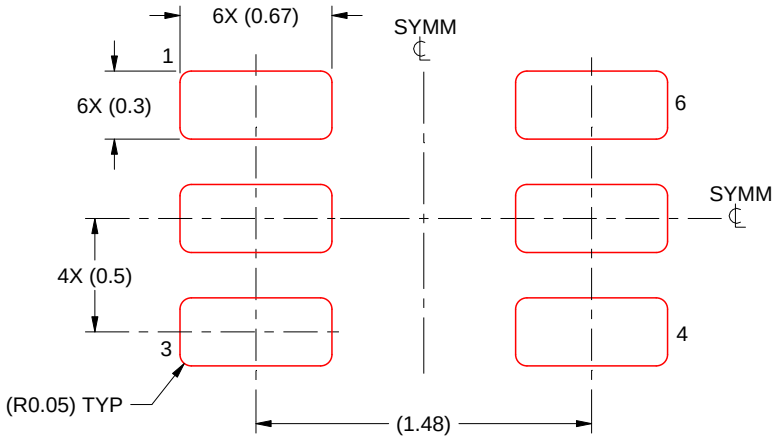
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月