TEXAS INSTRUMENTS
TPS563300
JAJSNR4 – JULY 2022

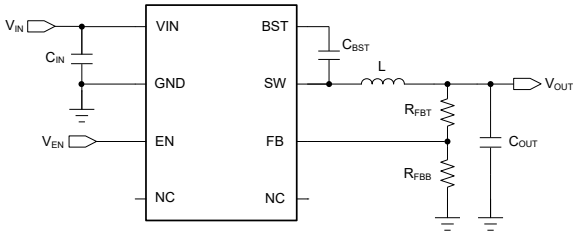
TPS563300 3.8V～28V、3A 同期整流降圧コンバータ、SOT583 パッケージ

1 特長

- 多様なアプリケーションに適した構成
  - 入力電圧範囲:3.8V～28V
  - 出力電圧範囲:0.8V～22V
  - 連続出力電流:3A
  - 0.8V ±1.5% の基準電圧 (25℃)
  - 動作時接合部温度:-40℃～150℃
  - 76mΩ および 32mΩ の MOSFET を内蔵
  - 20μA の低い静止電流 (標準値)
  - 最大 98% のデューティ・サイクル動作
  - 高精度の EN スレッショルド
- 使いやすさと小さなソリューション・サイズ
  - 内部補償付きピーク電流制御モード
  - パルス周波数変調 (PFM) による軽負荷時の効率向上
  - 固定スイッチング周波数:500kHz
  - 周波数スペクトラム拡散による EMI 低減
  - あらかじめ出力にバイアスが印加された状態でのスタートアップをサポート
  - ハイサイドおよびローサイド両方の MOSFET でサイクルごとの OC 制限
  - ラッチなしの OTP、OCP、OVP、UVP、UVLO 保護
  - 1.6mm × 2.1mm の SOT583 パッケージ
- WEBENCH® Power Designer により、TPS563300 を使用するカスタム設計を作成

2 アプリケーション

- ビル・オートメーション、家電製品、産業用 PC
- 多機能プリンタ、企業向けプロジェクタ
- 携帯型電子機器、ネットワーク接続の周辺機器
- スマート・スピーカ、モニタ
- 5V、12V、19V、24V 入力を備えた分散電源システム



概略回路図

3 概要

TPS563300 は、3.8V～28 V の広い入力電圧範囲を持ち高効率で使いやすい同期整流降圧コンバータであり、最大 3A の連続出力電流と 0.8V～22V の出力電圧をサポートしています。

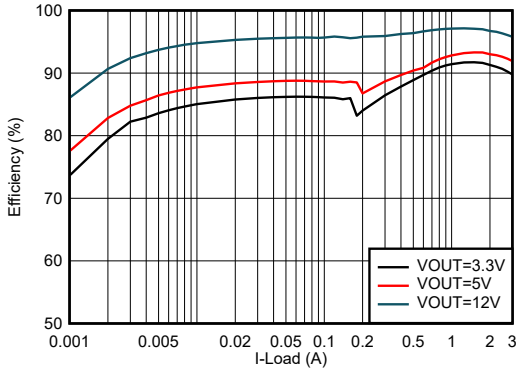
このデバイスは、固定周波数ピーク電流制御モードを採用して、高速な過渡応答と優れたラインおよび負荷レギュレーションを実現しています。内部ループ補償を最適化することで、幅広い出力電圧と動作周波数にわたって外付け補償部品を不要にしています。パルス周波数変調 (PFM) モードにより、軽負荷時の効率を最大限に高めることができます。低消費電力動作で長いバッテリ寿命を実現しようとする場合、低静止電流機能が役に立ちます。このデバイスは、EMI ノイズの低減に有効な周波数スペクトラム拡散機能も備えています。

このデバイスは、OTP、OVP、UVLO、サイクルごとの OC 制限、ヒカップ・モード付き UVP などの保護機能を完備しています。このデバイスは 0.5mm ピン・ピッチの小さな SOT583 (1.6mm × 2.1mm) パッケージに封止されています。PCB を簡単にレイアウトできるように最適化されたピン配置を採用しており、EMI 性能も優れています。

パッケージ情報

型番	パッケージ(1)	本体サイズ (公称)
TPS563300	SOT583 (8)	1.60mm × 2.10mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TPS563300 の効率 (V_{IN} = 24V、f_{SW} = 500kHz)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
July 2022	*	Initial release

5 Pin Configuration and Functions

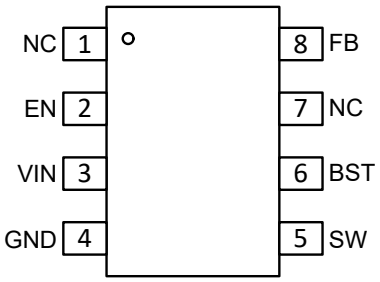


図 5-1. 8-Pin SOT583 DRL Package (Top View)

表 5-1. Pin Functions

Pin		Type(1)	Description
Name	NO.		
NC	1	A	Reserved pin. The user must leave this pin floating.
EN	2	A	Enable input to converter. Driving EN high or leaving this pin floating enables the converter. An external resistor divider can be used to implement an adjustable V_{IN} UVLO function.
VIN	3	P	Supply input pin to the internal LDO and high-side FET. Input bypass capacitors must be directly connected to this pin and GND.
GND	4	G	Ground pin. Connected to the source of the low-side FET as well as the ground pin for the controller circuit. Connect to system ground and the ground side of C_{IN} and C_{OUT}. The path to C_{IN} must be as short as possible.
SW	5	P	Switching output of the convertor. Internally connected to the source of the high-side FET and drain of the low-side FET. Connect to the power inductor.
BST	6	P	Bootstrap capacitor connection for the high-side FET driver. Connect a high-quality, 100-nF ceramic capacitor from this pin to the SW pin.
NC	7	A	Reserved pin. The user must leave this pin floating.
FB	8	A	Output feedback input. Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.

(1) A = Analog, P = Power, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	30	V
	EN	–0.3	6	
	FB	–0.3	6	
Output voltage	SW, DC	–0.3	30	
	SW, transient < 10 ns	–3	31	
	BST	–0.3	SW + 6	
	BST–SW	–0.3	6	
T_J	Operating junction temperature(2)	–40	150	°C
T_{stg}	Storage temperature	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Operating at junction temperatures greater than 150°C, although possible, degrades the lifetime of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted(1)

		MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	3.8		28	V
	EN	–0.1		5.5	
	FB	–0.1		5.5	
Output voltage	V_{OUT}	0.8		22	
	SW, DC	–0.1		28	
	SW, transient < 10 ns	–3		29	
	BST	–0.1		SW + 5.5	
	BST-SW	–0.1		5.5	
Ouput current	I_{OUT}	0		3	A
Temperature	Operating junction temperature, T_J	–40		150	°C

(1) The *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For compliant specifications, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)		DRL (SOT583), 8 PINS		UNIT
		JEDEC(2)	EVM(3)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	N/A	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.1	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.2	N/A	°C/W
$R_{\theta JA\_EVM}$	Junction-to-ambient thermal resistance on official EVM board	N/A	60.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were simulated on a standard JEDEC board. They do not represent the performance obtained in an actual application.
(3) The real $R_{\theta JA}$ on TI EVM is approximately 60.2°C/W, test condition: V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 3 A, T_A = 25°C

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_J = –40°C to +150°C, V_{IN} = 3.8 V to 30 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		3.8		28	V
I_Q	Nonswitching quiescent current	EN = 5 V, V_{FB} = 0.85 V		20		µA
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V		2		µA
V_{IN_UVLO}	Input undervoltage lockout thresholds	Rising threshold	3.4	3.6	3.8	V
		Falling threshold	3.1	3.3	3.5	V
		Hysteresis		300		mV
ENABLE (EN PIN)						
V_{EN_RISE}	Enable threshold	Rising enable threshold		1.21	1.28	V
V_{EN_FALL}	Disable threshold	Falling disable threshold	1.1	1.17		V
I_p	EN pullup current	V_{EN} = 1.0 V		0.7		µA
I_h	EN pullup hysteresis current	V_{EN} = 1.5 V		1.4		µA
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	FB voltage	T_J = 25°C	788	800	812	mV
		T_J = –40°C to 150°C	784	800	816	mV
I_{FB}	Input leakage current	V_{FB} = 0.8 V			0.15	µA
INTEGRATED POWER MOSFETS						
R_{DSON_HS}	High-side MOSFET on-resistance	T_J = 25°C, V_{BST} – SW = 5 V		76		mΩ
R_{DSON_LS}	Low-side MOSFET on-resistance	T_J = 25°C		32		mΩ
CURRENT LIMIT						
I_{HS_LIMIT}	High-side MOSFET current limit		4.2	5	5.8	A
I_{LS_LIMIT}	Low-side MOSFET current limit		2.9	3.8	4.5	A
I_{PEAK_MIN}	Minimum peak inductor current			0.75		A
SOFT START						
T_{SS}	Fixed internal soft-start time	Time from 0% × V_{OUT} to 100% × V_{OUT}		2		ms
OSCILLATOR FREQUENCY (RT PIN)						
f_{SW}	Switching center frequency		450	500	550	kHz
t_{ON_MIN} (1)	Minimum ON pulse width			70		ns

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_J = –40°C to +150°C, V_{IN} = 3.8 V to 30 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF_MIN} (1)	Minimum OFF pulse width			140		ns
t_{ON_MAX} (1)	Maximum ON pulse width			7		µs
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP detect (L→H)	112%	115%	118%	
		Hysteresis		5%		
V_{UVP}	Output UVP threshold	UVP detect (H→L)		65%		
t_{hiccup_ON}	UV hiccup ON time before entering hiccup mode after soft start ends			256		µs
t_{hiccup_OFF}	UV hiccup OFF time before restart			10.5 × t_{SS}		S
THERMAL SHUTDOWN						
T_{SHDN} (1)	Thermal shutdown threshold	Shutdown temperature		165		°C
T_{HYS} (1)		Hysteresis		30		°C
SPREAD SPECTRUM FREQUENCY						
f_m	Modulation frequency			f_{SW} / 128		kHz
f_{spread}	Internal spread oscillator frequency			±6%		

(1) Not production tested, specified by design

6.6 Typical Characteristics

T_J = –40°C to 150°C, V_{IN} = 12 V, unless otherwise noted

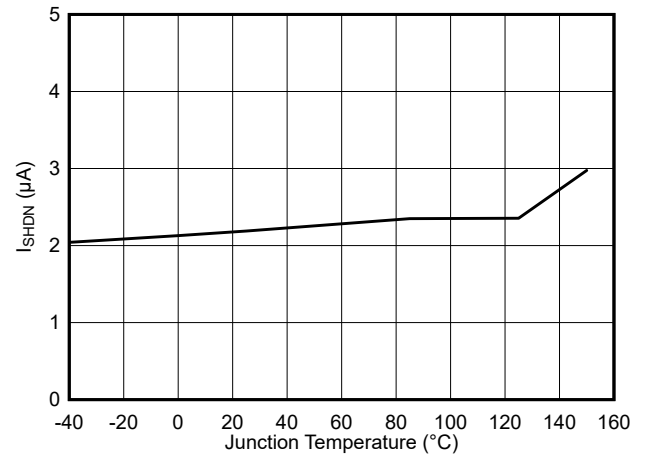


図 6-1. Shutdown Current vs Junction Temperature

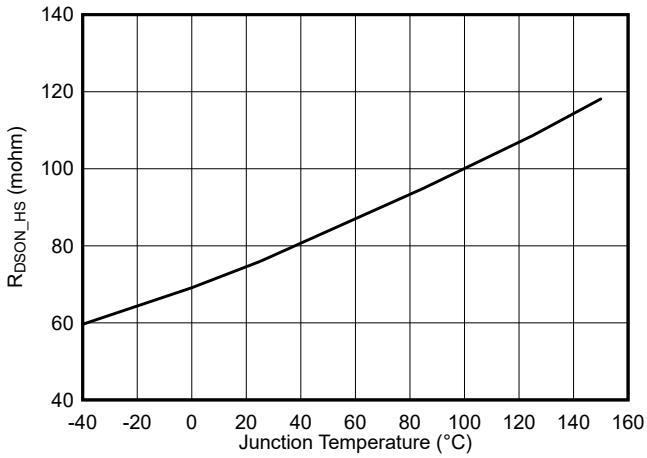


図 6-2. High-Side R_{DSON} vs Junction Temperature

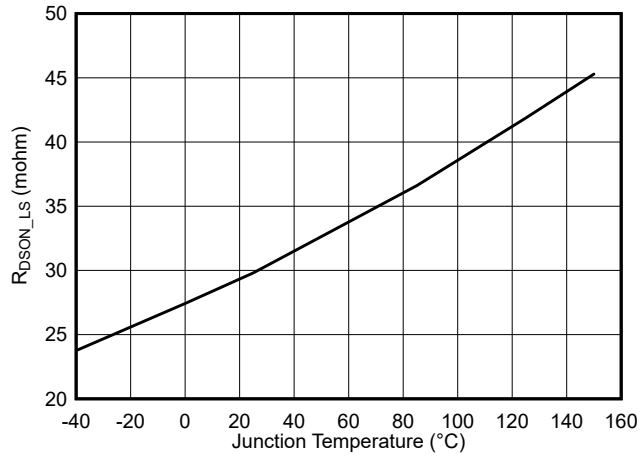


図 6-3. Low-Side R_{DSON} vs Junction Temperature

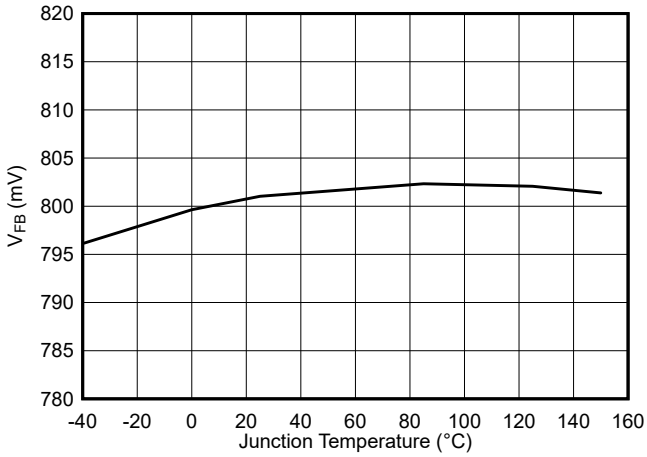


図 6-4. Feedback Voltage vs Junction Temperature

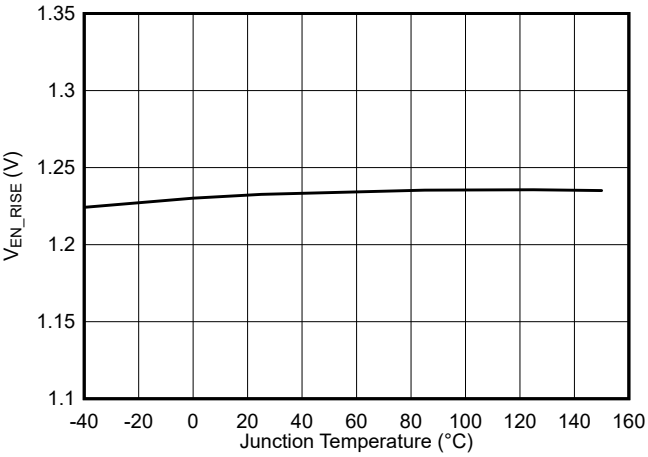


図 6-5. Enable Threshold vs Junction Temperature

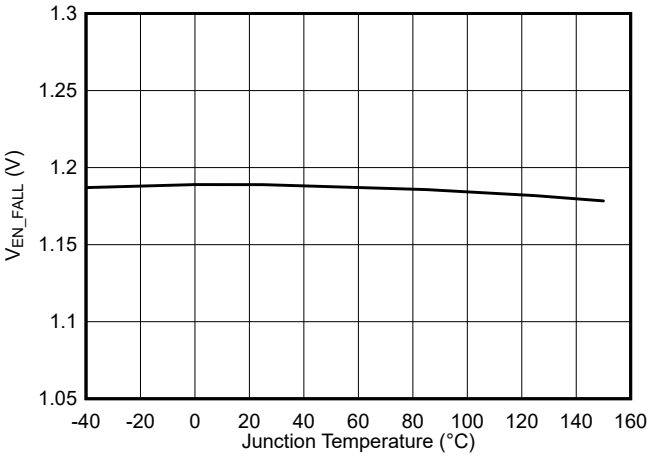


図 6-6. Disable Threshold vs Junction Temperature

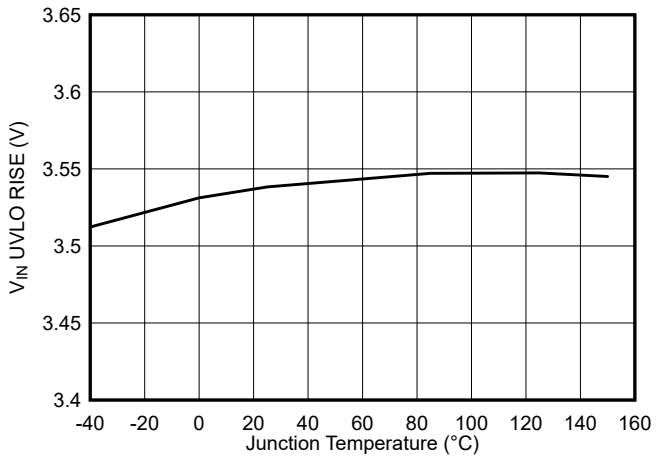


図 6-7. V_{IN} UVLO Rising Threshold vs Junction Temperature

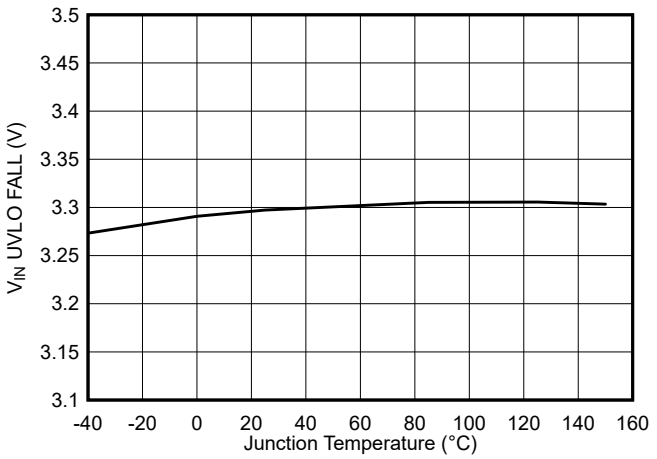


図 6-8. V_{IN} UVLO Falling Threshold vs Junction Temperature

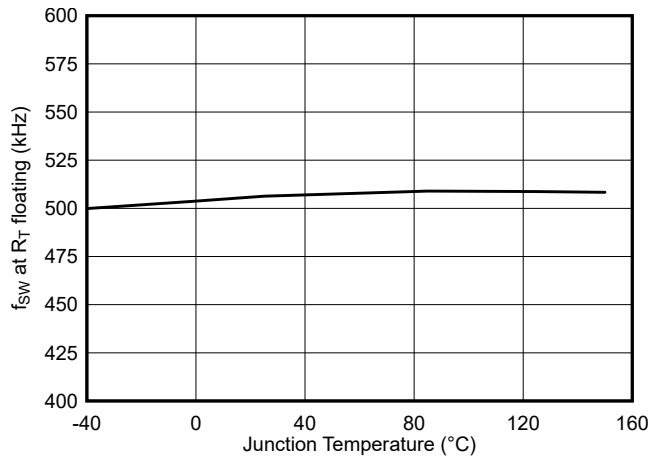


図 6-9. Switching Frequency vs Junction Temperature

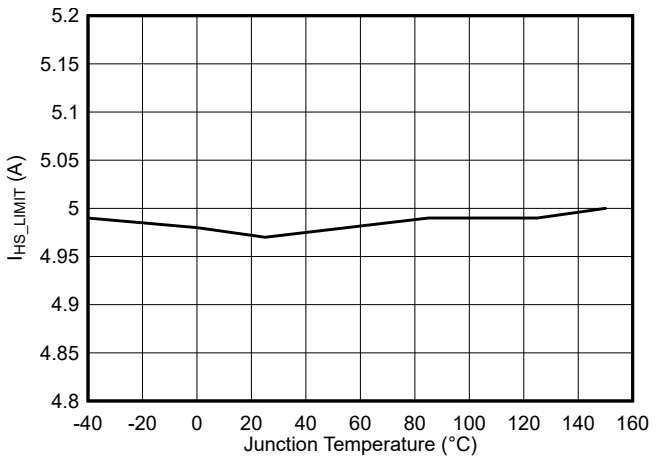


図 6-10. High-Side Current Limit vs Junction Temperature

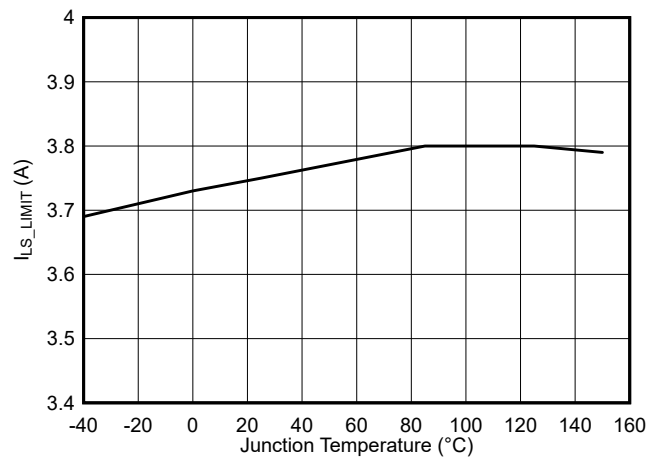


図 6-11. Low-Side Current Limit vs Junction Temperature

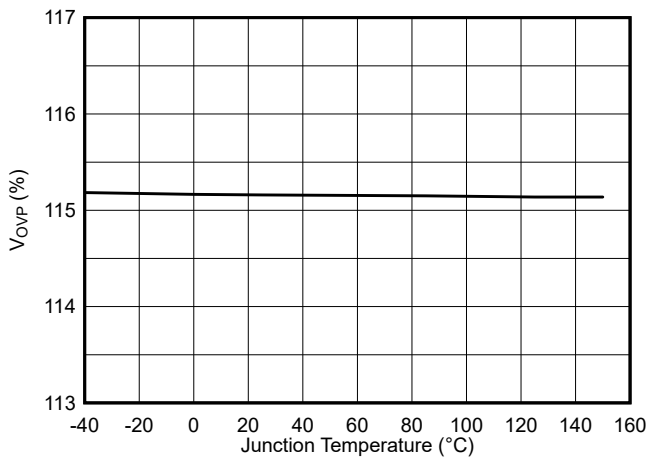


図 6-12. OVP Threshold vs Junction Temperature

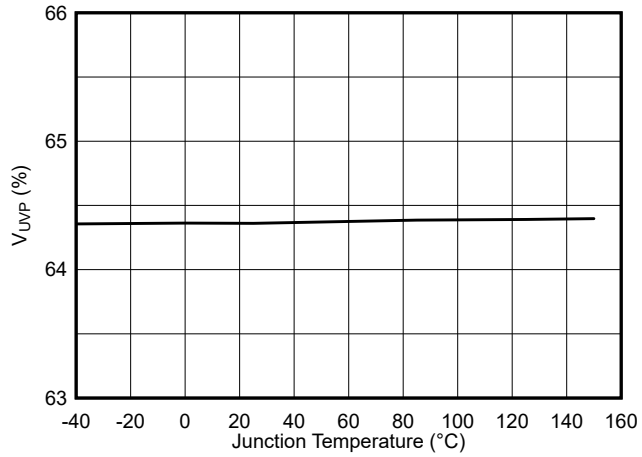


図 6-13. UVP Threshold vs Junction Temperature

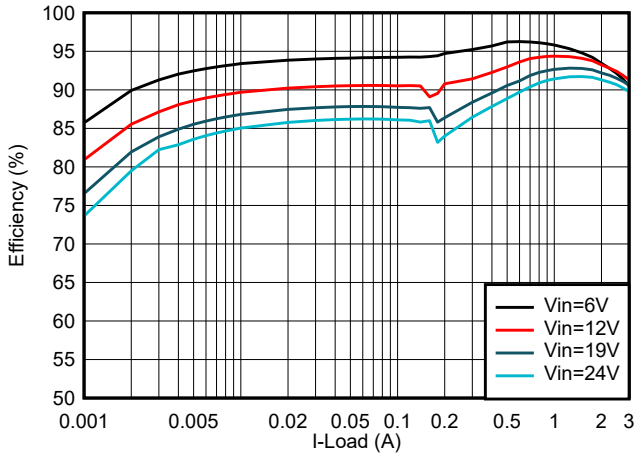


図 6-14. Efficiency, V_{OUT} = 3.3 V, f_{SW} = 500 kHz, L = 4.7 µH

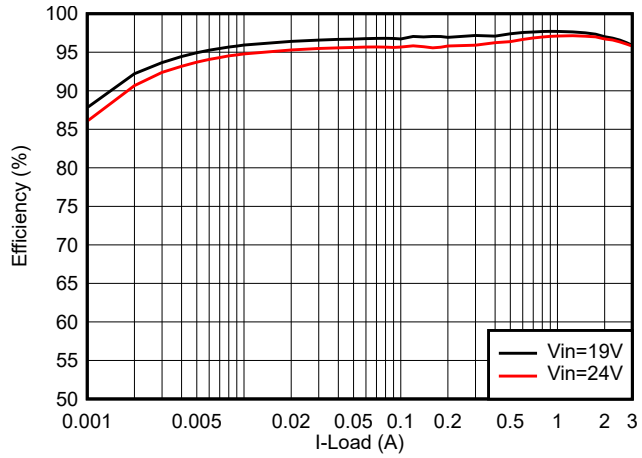


図 6-15. Efficiency, V_{OUT} = 12 V , f_{SW} = 500 kHz, L = 12 µH

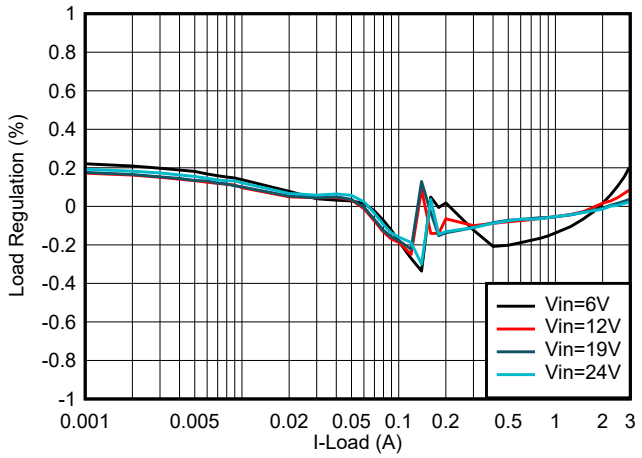


図 6-16. Load Regulation, V_{OUT} = 3.3 V, f_{SW} = 500 kHz

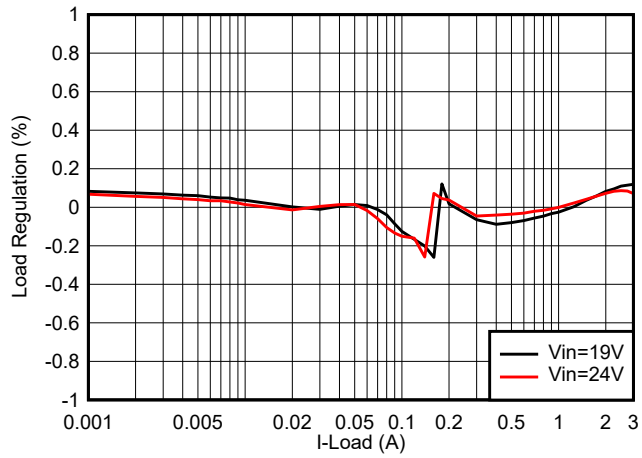


図 6-17. Load Regulation, V_{OUT} = 12 V, f_{SW} = 500 kHz

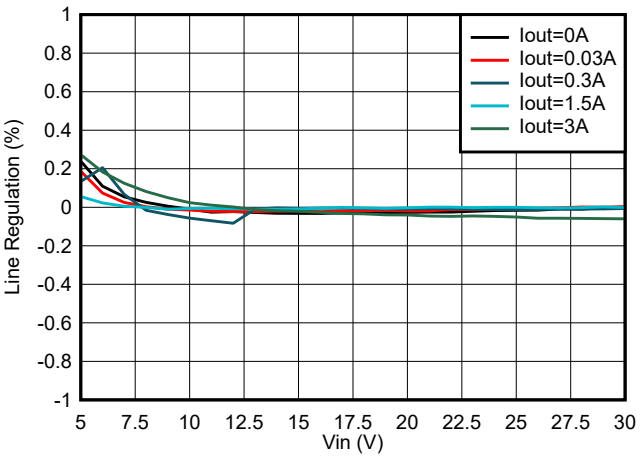


図 6-18. Line Regulation, V_{OUT} = 3.3 V, f_{SW} = 500 kHz

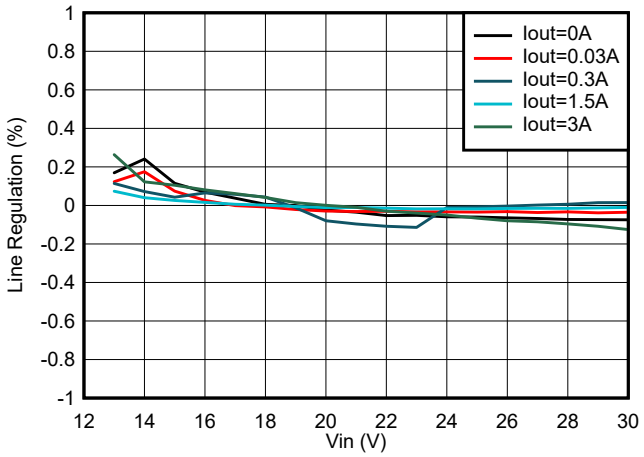


図 6-19. Line Regulation, V_{OUT} = 12 V, f_{SW} = 500 kHz

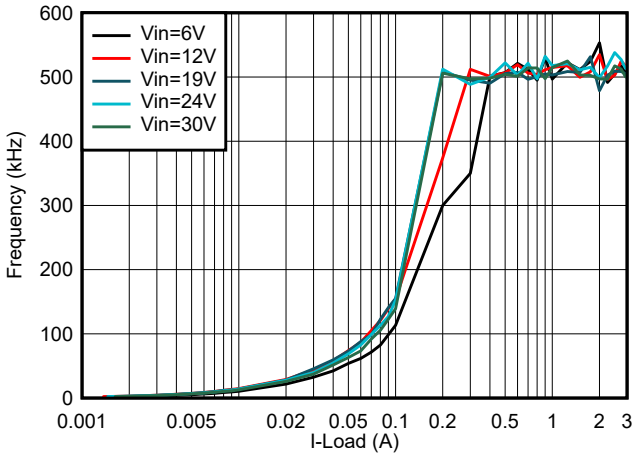


図 6-20. Switching Frequency vs Load Current, V_{OUT} = 3.3 V

7 Detailed Description

7.1 Overview

The TPS563300 is a 28-V, 3-A, synchronous buck (step-down) converter with two integrated n-channel MOSFETs. The device employs fixed-frequency peak current control mode for fast transient response and good line and load regulation. With the optimized internal loop compensation, the device eliminates the external compensation components over a wide range of output voltage and switching frequency.

The integrated 76-mΩ and 32-mΩ MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 3 A. The feedback reference voltage is designed at 0.8 V. The output voltage can be stepped down from 0.8 V to 22 V. The device is ideally suited for systems powered from the following power-bus rails:

- 5-V
- 12-V
- 19-V
- 24-V

The TPS563300 has been designed for safe monotonic start-up into prebiased loads. The default start-up is at V_{IN} equal to 3.8 V. After the device is enabled, the output rises smoothly from 0 V to its regulated voltage. The total operating current is 20 µA (typical) when not switching under no load. When the device is disabled, the supply current is approximately 2 µA (typical). The pulse frequency modulation (PFM) mode maximizes the light load efficiency. These features are extremely beneficial for long battery life time in low-power operation.

The EN pin has an internal pullup current that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current. This device also has frequency spread spectrum feature, which helps with lowering down EMI noise.

The device has the on-time extension function with a maximum on time of 7 µs (typical). During the low dropout operation, the high-side MOSFET can turn on up to 7 µs, then the high-side MOSFET turns off and the low-side MOSFET turns on with a minimum off time of 140 ns (typical). The device supports the maximum 98% duty cycle.

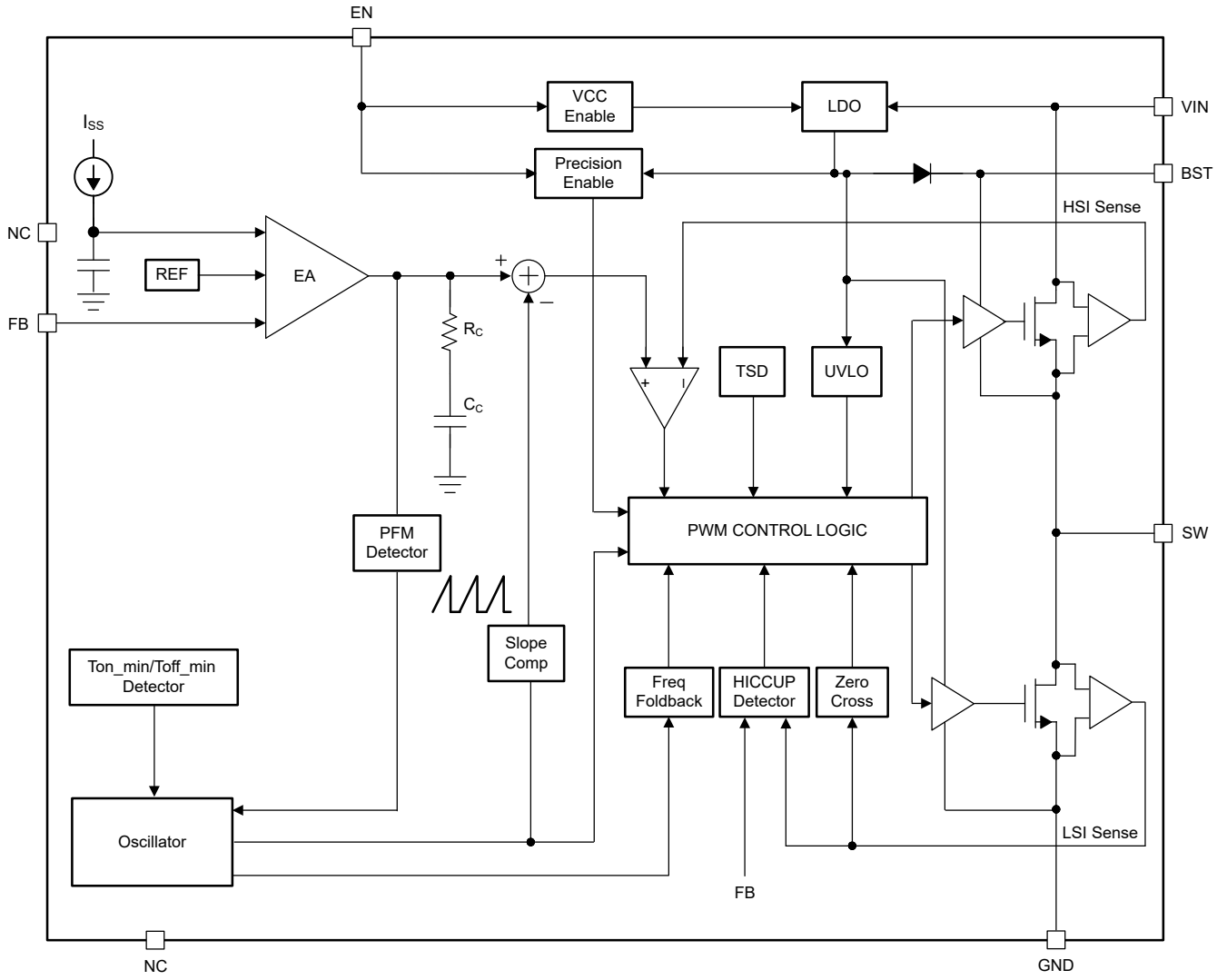
The device reduces the external component count by integrating the bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and SW pins. A UVLO circuit monitors the bootstrap capacitor voltage, V_{BST-SW}. When it falls below a preset threshold of 2.5 V (typical), the SW pin is pulled low to recharge the bootstrap capacitor.

Cycle-by-cycle current limiting on the high-side MOSFET protects the device in overload situations and is enhanced by a low-side sourcing current limit, which prevents current runaway. The TPS563300 provides output undervoltage protection (UVP) when the regulated output voltage is lower than 65% of the nominal voltage due to overcurrent being triggered, approximately 256-µs (typical) deglitch time later, both the high-side and low-side MOSFET turn off and the device steps into hiccup mode.

The device minimizes excessive output overvoltage transient by taking advantage of the overvoltage comparator. When the regulated output voltage is greater than 115% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 110%.

Thermal shutdown disables the device when the die temperature, T_J, exceeds 165°C and enables the device again after T_J decreases below the hysteresis amount of 30°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency Peak Current Mode

The following operation description of the TPS563300 refers to the functional block diagram and to the waveforms in 図 7-1. The TPS563300 is a synchronous buck converter with integrated high-side (HS) and low-side (LS) MOSFETs (synchronous rectifier). The TPS563300 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch on time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current, i_L, increases with linear slope (V_{IN} – V_{OUT}) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot–through dead time. Inductor current discharges through the low-side switch with a slope of –V_{OUT} / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / t_{SW}, where t_{ON} is the high-side switch on time and t_{SW} is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

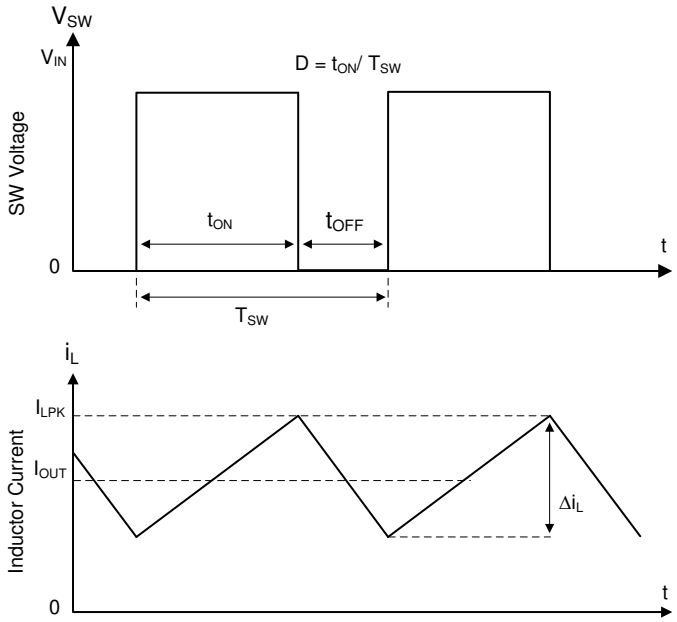


図 7-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The TPS563300 employs the fixed-frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the HS switch and compared to the peak current threshold to control the on time of the HS switch. The voltage feedback loop is internally compensated, which allows for fewer external components, making it easy to design, and provides stable operation with almost any combination of output capacitors. The converter operates with fixed switching frequency at normal-load condition. At light-load condition, the TPS563300 operates in PFM mode to maintain high efficiency.

7.3.2 Pulse Frequency Modulation

The TPS563300 is designed to operate in pulse frequency modulation (PFM) mode at light load currents to boost light-load efficiency.

When the load current is lower than half of the peak-to-peak inductor current in CCM, the TPS563300 operates in discontinuous conduction mode (DCM). In DCM operation, the low-side switch is turned off when the inductor current drops to approximately 0 A to improve efficiency. Both switching losses and conduction losses are reduced in DCM when compared to forced CCM operation at light load.

At even lighter current load, pulse frequency modulation (PFM) mode is activated to maintain high-efficiency operation. When either the minimum high-side switch on time, t_{ON_MIN}, or the minimum peak inductor current, I_{PEAK_MIN} (typically 750 mA), is reached, the switching frequency decreases to maintain regulation. In PFM

mode, the switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching actions. Since the integrated current comparator catches the peak inductor current only, the average load current entering PFM mode varies with the applications and external output LC filters.

In PFM mode, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the feedback voltage catches V_{REF}. The periodicity of these bursts is adjusted to regulate the output, while zero current crossing detection turns off the low-side MOSFET to maximize efficiency. This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. PWM trades off very good light-load efficiency for larger output voltage ripple and variable switching frequency.

7.3.3 Voltage Reference

The internal reference voltage, V_{REF}, is designed at typical 0.8 V, the negative feedback system of converter produces a precise ±2% feedback voltage V_{FB} over full temperature by scaling the output of a temperature stable internal band-gap circuit.

7.3.4 Output Voltage Setting

A precision 0.8-V internal reference voltage, V_{REF}, is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from the output voltage to the FB pin. TI recommends using 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor, R_{FBB}, for the desired divider current and use 式 1 to calculate the top-side resistor, R_{FBT}. Lower R_{FBB} increases the divider current and reduces efficiency at very light load. Larger R_{FBB} makes the FB voltage more susceptible to noise, so the larger R_{FBB} value requires more carefully designed feedback path on the PCB. Setting R_{FBB} = 10 kΩ and R_{FBT} in the range of 10 kΩ to 300 kΩ is recommended for most applications.

The tolerance and temperature variation of the resistor dividers affect the output voltage regulation.

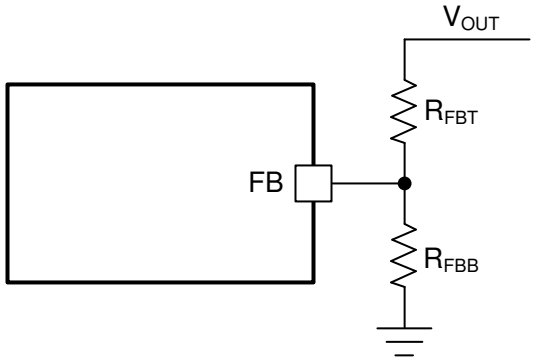


図 7-2. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (1)$$

where

- V_{REF} is 0.8 V.
- R_{FBB} is 10 kΩ (recommended).

7.3.5 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage exceeds the enable threshold voltage, V_{EN_RISE}, the TPS563300 begins operation. If the EN pin voltage is pulled below the disable threshold voltage, V_{EN_FALL}, the converter stops switching and enters shutdown mode.

The EN pin has an internal pullup current source, which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector or GPIO output logic to interface with the pin.

The TPS563300 implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN_UVLO} threshold. The internal V_{IN_UVLO} threshold has a hysteresis of typical 300 mV. If an application requires a higher UVLO threshold on the VIN pin, the EN pin can be configured as shown in 図 7-3. When using the external UVLO function, setting the hysteresis at a value greater than 500 mV is recommended.

The EN pin has a small pullup current, I_p, which sets the default state of the EN pin to enable when no external components are connected. The pullup hysteresis current, I_h, is used to control the hysteresis voltage for the UVLO function when the EN pin voltage crosses the enable threshold. Use 式 2 and 式 3 to calculate the values of R1 and R2 for a specified UVLO threshold. Once R1 and R2 are settled down, the V_{EN} can be calculated by 式 4, which must be lower than 5.5 V with max V_{IN}.

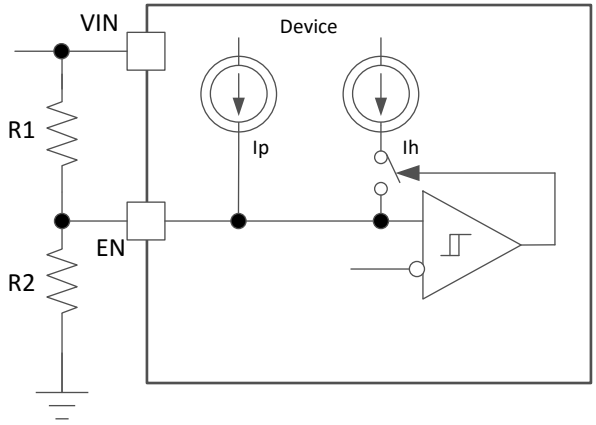


図 7-3. Adjustable V_{IN} Undervoltage Lockout

$$R_1 = \frac{V_{START} \times \frac{V_{EN\_FALL}}{V_{EN\_RISE}} - V_{STOP}}{I_p \times \left(1 - \frac{V_{EN\_FALL}}{V_{EN\_RISE}}\right) + I_h} \quad (2)$$

$$R_2 = \frac{R_1 \times V_{EN\_FALL}}{V_{STOP} - V_{EN\_FALL} + R_1 \times \left(I_p + I_h\right)} \quad (3)$$

$$V_{EN} = \frac{R_2 \times V_{IN} + R_1 \times R_2 \times \left(I_p + I_h\right)}{R_1 + R_2} \quad (4)$$

where

- I_p is 0.7 µA.
- I_h is 1.4 µA.
- V_{EN_FALL} is 1.17 .
- V_{EN_RISE} is 1.21 V.
- V_{START} is the input voltage enabling the device.
- V_{STOP} is the input voltage disabling the device.

7.3.6 Minimum On Time, Minimum Off Time, and Frequency Foldback

Minimum on time, t_{ON_MIN}, is the smallest duration of time that the high-side switch can be on. t_{ON_MIN} is typically 70 ns in the TPS563300. Minimum off time, t_{OFF_MIN}, is the smallest duration that the high-side switch can be off. t_{OFF_MIN} is typically 140 ns. In CCM operation, t_{ON_MIN} and t_{OFF_MIN} limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \quad (5)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \quad (6)$$

Given a required output voltage, the maximum V_{IN} without frequency foldback is:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \quad (7)$$

The minimum V_{IN} without frequency foldback is:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}} \quad (8)$$

In TPS563300, a frequency foldback scheme is employed once t_{ON_MIN} or t_{OFF_MIN} is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on time decreases while V_{IN} voltage increases. Once the on time decreases to t_{ON_MIN}, the switching frequency starts to decrease while V_{IN} continues to go up, which lowers the duty cycle further to keep V_{OUT} in regulation according to 式 5.

The frequency foldback scheme also works once larger duty cycle is needed under low V_{IN} condition. The frequency decreases once the device hits its t_{OFF_MIN}, which extends the maximum duty cycle according to 式 6. Wide range of frequency foldback allows the TPS563300 output voltage to stay in regulation with a much lower supply voltage V_{IN}, which allows a lower effective dropout.

With frequency foldback, V_{IN_MAX} is raised, and V_{IN_MIN} is lowered by decreased f_{SW}.

7.3.7 Frequency Spread Spectrum

In order to reduce EMI, the TPS563300 introduces frequency spread spectrum. The jittering span is typically Δfc = ±6% of the switching frequency with the modulation frequency of $f_m = f_{SW} / 128$. The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. 図 7-4 shows the frequency spread spectrum modulation. 図 7-5 shows the energy is spread out at the center frequency, f_c.

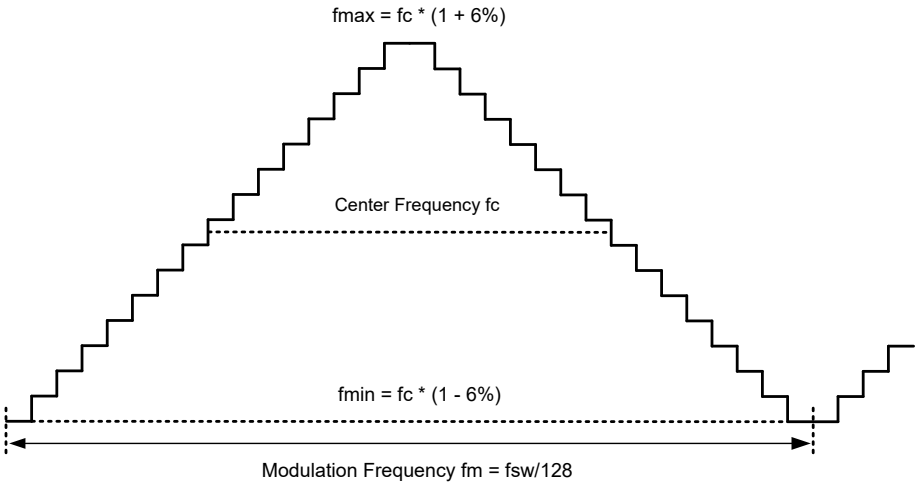


図 7-4. Frequency Spread Spectrum Diagram

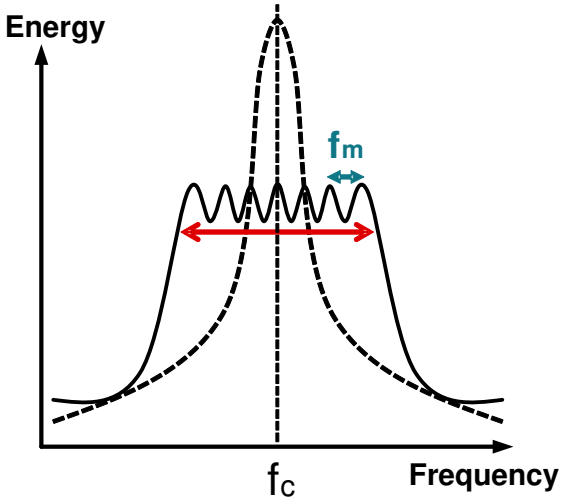


図 7-5. Energy vs Frequency

7.3.8 Overvoltage Protection

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold of 115%, the high-side MOSFET is turned off, which prevents current from flowing to the output and minimizes output overshoot. When the FB pin voltage drops lower than the OVP threshold minus hysteresis, the high-side MOSFET is allowed to turn on at the next clock cycle. This function is non-latch operation.

7.3.9 Overcurrent and Undervoltage Protection

The TPS563300 incorporates both peak and valley inductor current limits to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current run-away during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Hiccup mode is also incorporated for sustained short circuits.

The high-side switch current is sensed when it is turned on after a set blanking time (t_{ON_MIN}), the peak current of high-side switch is limited by the peak current threshold, I_{HS_LIMIT}. The current going through the low-side switch is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down.

As the device is overloaded, a point is reached where the valley of the inductor current cannot reach below I_{LS_LIMIT} before the next clock cycle, then the low-side switch is kept on until the inductor current ramps below the valley current threshold, I_{LS_LIMIT}, then the low-side switch is turned off and the high-side switch is turned on after a dead time. When this occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, but the output voltage remains in regulation. As the overload is increased, both the inductor current ripple and peak current increase until the high-side current limit, I_{HS_LIMIT}, is reached. When this limit is tripped, the switch duty cycle is reduced and the output voltage falls out of regulation, which represents the maximum output current from the converter and is given approximately by 式 9. The output voltage and switching frequency continue to drop as the device moves deeper into overload while the output current remains at approximately I_{OMAX}. If the inductor ripple current is large, the high-side current limit can be tripped before the low-side limit is reached. In this case, 式 10 gives the approximate maximum output current.

$$I_{OMAX} \approx \frac{I_{HS\_LIMIT} + I_{LS\_LIMIT}}{2} \tag{9}$$

$$I_{OMAX} \approx I_{HS\_LIMIT} - \frac{(V_{IN} - V_{OUT})}{2 \times L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \tag{10}$$

Furthermore, if a severe overload or short circuit causes the FB voltage to fall below V_{UVP} threshold, 65% of the V_{REF}, and triggering current limit, and the condition occurs for more than the hiccup on time (typically 256 µs), the converter enters hiccup mode. In this mode, the device stops switching for hiccup off time, 10.5 × t_{SS}, and then goes to a normal restart with soft-start time. If the overload or short-circuit condition remains, the device runs in current limit and then shuts down again. This cycle repeats as long as the overload or short-circuit condition persists. This mode of operation reduces the temperature rise of the device during a sustained overload or short circuit condition on the output. Once the output short is removed, the output voltage recovers normally to the regulated value.

7.3.10 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 165°C (typical), the device goes into thermal shut down, both the high-side and low-side power FETs are turned off. When T_J decreases below the hysteresis amount of 30°C (typical), the converter resumes normal operation, beginning with a soft start.

7.4 Device Functional Modes

7.4.1 Modes Overview

The TPS563300 moves among CCM, DCM, and PFM modes as the load changes. Depending on the load current, the TPS563300 is in one of below modes:

- Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple
- Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation
- Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load

7.4.2 Heavy Load Operation

The TPS563300 operates in continuous conduction mode (CCM) when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. CCM provides excellent line and load regulation and minimum output voltage ripple, and the maximum continuous output current of 3 A can be supplied by the TPS563300.

7.4.3 Light-Load Operation

For PFM version, when the load current is lower than half of the peak-to-peak inductor current in CCM, the device operates in discontinuous conduction mode (DCM), also known as diode emulation mode (DEM). In DCM operation, the LS switch is turned off when the inductor current drops to I_{LS_ZC} (150 mA typical) to improve efficiency. Both switching losses and conduction losses are reduced in DCM when compared to forced CCM operation at light load.

At even lighter current load, pulse frequency modulation (PFM) mode is activated to maintain high efficiency operation. When either the minimum on time, t_{ON_MIN}, or the minimum peak inductor current, I_{PEAK_MIN} (typically 750 mA) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching actions. The output current for mode change depends on the input voltage, inductor value, and the programmed switching frequency. For applications where the switching frequency must be known for a given condition, the transition between PFM and CCM must be carefully tested before the design is finalized.

7.4.4 Dropout Operation

The dropout performance of any buck converter is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off time of the high-side MOSFET starts to approach the minimum value. Beyond this point, the switching frequency becomes erratic and the output voltage can fall out of regulation. To avoid this problem, the TPS563300 automatically reduces the switching frequency (on-time extension function) to increase the effective duty cycle and maintain in regulation until the switching frequency reach to the lowest limit of about 140 kHz, the period is equal to (t_{ON_MAX} + t_{OFF_MIN}) (typically 7.14 µS). In this condition, the difference voltage between V_{IN} and V_{OUT} is defined as dropout voltage. The typical overall dropout characteristics can be found as 図 7-6.

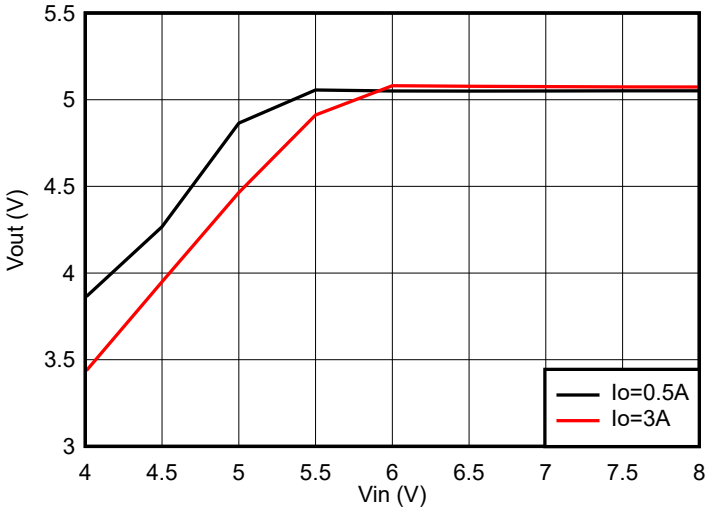


図 7-6. Overall Dropout Characteristic, V_{OUT} = 5 V

7.4.5 Minimum On-Time Operation

Every switching converter has a minimum controllable on time dictated by the inherent delays and blanking times associated with the control circuits, which imposes a minimum switch duty cycle and, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the TPS563300 automatically reduces the switching frequency when the minimum on-time limit is reached. This way, the converter can regulate the lowest programmable output voltage at the maximum input voltage. Use 式 11 to find an estimate for the approximate input voltage for a given output voltage before frequency foldback occurs. The values of t_{ON_MIN} and f_{SW} can be found in セクション 6.5.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON\_MIN} \times f_{SW}} \tag{11}$$

As the input voltage is increased, the switch on time (duty-cycle) reduces to regulate the output voltage. When the on time reaches the minimum on time, t_{ON_MIN}, the switching frequency drops while the on time remains fixed.

7.4.6 Shutdown Mode

The EN pin provides electrical ON and OFF control for the device. When V_{EN} is below typical 1.1 V, the TPS563300 is in shutdown mode. The device also employs VIN UVLO protection. If V_{IN} voltage is below their respective UVLO level, the converter is turned off too.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS563300 is a highly integrated, synchronous, step-down, DC-DC converter. This device is used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 3 A.

8.2 Typical Application

The application schematic of 図 8-1 was developed to meet the requirements of the device. This circuit is available as the TPS563300EVM evaluation module. The design procedure is given in this section.

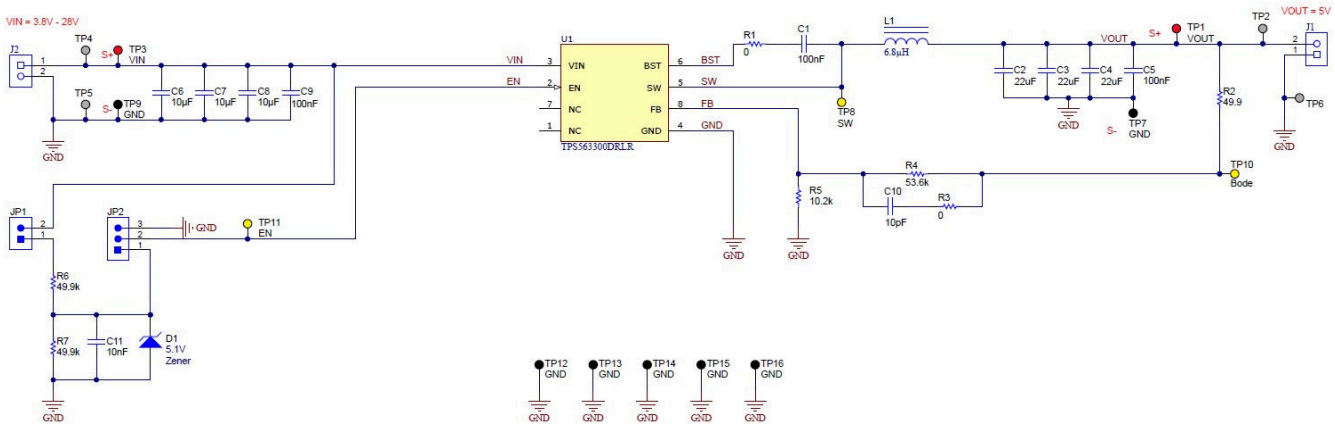

図 8-1. TPS563300 5-V Output, 3-A Reference Design

8.2.1 Design Requirements

表 8-1 shows the design parameters for this application.

表 8-1. Design Parameters

Parameter		Conditions	MIN	TYP	MAX	Unit
V_{IN}	Input voltage		5.5	24	28	V
V_{OUT}	Output voltage			5		V
I_{OUT}	Output current rating			3		A
ΔV_{OUT}	Transient response	Load step from 0.5 A→2.5 A→0.5 A, 0.8-A/µS slew rate		±5% × V_{OUT}		V
$V_{IN(ripple)}$	Input ripple voltage			400		mV
$V_{OUT(ripple)}$	Output ripple voltage			30		mV
F_{SW}	Switching frequency			500		kHz
t_{SS}	Soft-start time			2		mS
V_{START}	Start input voltage (Rising V_{IN})			8		V
V_{STOP}	Stop input voltage (Falling V_{IN})			7		V
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Create a custom design using the TPS563300 with the WEBENCH® Power Designer

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Referring to the application schematic of 図 8-1, start with 10.2 kΩ for R7 and use 式 12 to calculate R6 = 53.6 kΩ. To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the converter is more susceptible to noise and voltage errors from the FB input leakage current are noticeable.

$$R_6 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_7 \tag{12}$$

表 8-2 shows the recommended components value for common output voltages.

8.2.2.3 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BST to SW pins for proper operation. TI recommends using a ceramic capacitor with X5R or better grade dielectric. The capacitor C5 must have a 16-V or higher voltage rating.

In addition, adding one BST resistor R4 to reduce the spike voltage on the SW node, the resistance smaller than 10 Ω is recommended to be used between BST to the bootstrap capacitor.

8.2.2.4 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between VIN and the EN pin of the TPS563300 and R2 is connected between EN and GND. The UVLO has two thresholds: one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply turns on and start switching when the input voltage increases above 8 V (V_{START}). After the converter starts switching, it continues to do so until the input voltage falls below 7 V (V_{STOP}). 式 2 and 式 3 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified, the nearest standard resistor value for R1 is 511 kΩ and for R2 is 80.7 kΩ.

8.2.2.5 Output Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current, Δi_L, which can be calculated by 式 13.

$$\Delta I_L = \frac{V_{OUT}}{V_{IN\_MAX}} \times \frac{V_{IN\_MAX} - V_{OUT}}{L \times f_{SW}} \tag{13}$$

Usually, define K coefficient represents the amount of inductor ripple current relative to the maximum output current of the device, a reasonable value of K must be 20% to 60%, experience shows that the best value of K is 40%. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L. Use 式 14 to calculate the minimum value of the output inductor.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUT\_MAX}} \times \frac{V_{OUT}}{V_{IN}} \tag{14}$$

where

- K is the ripple ratio of the inductor current (ΔI_L / I_{OUT_MAX}).

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. Too low of an inductance also generates more inductor core loss since the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors.

After inductance L is determined, the maximum inductor peak current and RMS current can be calculated by 式 15 and 式 16.

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \tag{15}$$

$$I_{L\_RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}} \tag{16}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, I_{HS_LIMIT} (see セクション 6.5), which ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LS_LIMIT}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly, this can lead to component damage, so do not allow the inductor to saturate. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

For this design example, choose the following values:

- K = 0.4
- V_{IN_MAX} = 30 V
- f_{SW} = 500 kHz
- I_{OUT_MAX} = 3 A

The inductor value is calculated to be 6.94 µH. Choose the nearest standard value of 6.8 µH. This gives a new K value of 0.408. The max I_{HS_LIMIT} is 5.8 A, the calculated peak current is 3.61 A, and the calculated RMS current is 3.02 A. The chosen inductor is a Würth Elektronik, 74439346068, 6.8 µH, which has a saturation current rating of 10 A and a RMS current rating of 6.5 A.

The maximum inductance is limited by the minimum current ripple required for the peak current mode control to perform correctly. To avoid subharmonic oscillation, as a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current (3 A) under nominal conditions.

8.2.2.6 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters, which is generally desired to use as little output capacitance as possible to keep cost and size down. The output capacitance, C_{OUT}, must be chosen with care since it directly affects the following specifications:

- Steady state output voltage ripple
- Loop stability

- Output voltage overshoot and undershoot during load current transient

The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the equivalent series resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR = K \times I_{OUT} \times ESR \tag{17}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{18}$$

K is the ripple ratio of the inductor current (ΔI_L / I_{OUT_MAX}). The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

Output capacitance is usually limited by the load transient requirements rather than the output voltage ripple if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a large load step happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The control loop of the converter usually needs eight or more clock cycles to regulate the inductor current equal to the new load level. The output capacitance must be large enough to supply the current difference for about eight clock cycles to maintain the output voltage within the specified range. 式 19 shows the minimum output capacitance needed for specified V_{OUT} overshoot and undershoot.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT} \times K} \times \left[(1-D) \times (1+K) + \frac{K^2}{12} (2-D) \right] \tag{19}$$

where

- D is V_{OUT} / V_{IN} (duty cycle of steady state).
- ΔV_{OUT} is the output voltage change.
- ΔI_{OUT} is the output current change.

For this design example, the target output ripple is 30 mV. Presuppose ΔV_{OUT_ESR} = ΔV_{OUT_C} = 30 mV and choose K = 0.4. 式 17 yields ESR no larger than 25 mΩ and 式 18 yields C_{OUT} no smaller than 10 µF. For the target overshoot and undershoot limitation of this design, ΔV_{OUT_SHOOT} < 5% × V_{OUT} = 250 mV for an output current step of ΔI_{OUT} = 1.5 A. C_{OUT} is calculated to be no smaller than 25 µF by 式 19. In summary, the most stringent criterion for the output capacitor is 25 µF. Considering the ceramic capacitor has DC bias de-rating, it can be achieved with a bank of 2 × 22-µF, 35-V, ceramic capacitor C3216X5R1V226M160AC in the 1206 case size.

More output capacitors can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases, an aluminum electrolytic capacitor can be placed in parallel with the ceramics to build up the required value of capacitance. When using a mixture of aluminum and ceramic capacitors, use the minimum recommended value of ceramics and add aluminum electrolytic capacitors as needed.

The recommendations given in 表 8-2 provide typical and minimum values of output capacitance for the given conditions. These values are the effective figures. If the minimum values are to be used, the design must be tested over all of the expected application conditions, including input voltage, output current, and ambient temperature. This testing must include both bode plot and load transient assessments. The maximum value of total output capacitance can be referred to the application note (C_{OUT} selection and C_{FF} selection) on the TPS62933 product page. Large values of output capacitance can adversely affect the start-up behavior of the converter as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed

before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can help reduce spikes on the output caused by inductor and board parasitics.

表 8-2 shows the recommended LC combination.

表 8-2. Recommended LC Combination

V_{OUT}(V)	R_{TOP}(kΩ)	R_{DOWN}(kΩ)	Typical Inductor L (µH)	Typical Effective C_{OUT} (µF)	Minimum Effective C_{OUT} (µF)
3.3	31.3	10.0	4.7	40	15
5	52.5	10.0	6.8	20	10
12	140.0	10.0	12	15	10

8.2.2.7 Input Capacitor Selection

The TPS563300 device requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF, and an additional 0.1-µF capacitor from the VIN pin to ground is recommended to provide high frequency filtering.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. X5R and X7R ceramic dielectrics are recommended because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The capacitor must also be selected with the DC bias taken into account. The effective capacitance value decreases as the DC bias increases.

The capacitor voltage rating needs to be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS563300. The input ripple current can be calculated using 式 20.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \times \frac{V_{IN\_MIN} - V_{OUT}}{V_{IN\_MIN}}} \tag{20}$$

For this example design, two TDK CGA5L1X7R1H106K160AC (10-µF, 50-V, 1206, X7R) capacitors have been selected. The effective capacitance under input voltage of 24 V for each one is 3.45 µF. The input capacitance value determines the input ripple voltage of the converter. The input voltage ripple can be calculated using 式 21. Using the design example values, I_{OUT_MAX} = 3 A, C_{IN_EFF} = 2 × 3.45 = 6.9 µF, and f_{SW} = 500 kHz, yields an input voltage ripple of 222 mV and a RMS input ripple current of 1.22 A.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX} \times 0.25}{C_{IN} \times f_{SW}} + (I_{OUT\_MAX} \times R_{ESR\_MAX}) \tag{21}$$

where

- R_{ESR_MAX} is the maximum series resistance of the input capacitor (approximately 1.5 mΩ of two capacitors in paralleled).

8.2.2.8 Feedforward Capacitor C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT} in combination with the parasitic capacitance at the FB pin can create a small signal pole that interferes with the loop stability. A C_{FF} helps mitigate this effect. Use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor.

The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor Application Report* is helpful when experimenting with a feedforward capacitor.

For this example design, a 10-pF capacitor C9 can be mounted to boost load transient performance.

8.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the TPS563300 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$, of the device
- PCB combination

The maximum internal die temperature for the TPS563300 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 22 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. Note that these curves include the power loss in the inductor. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the value of $R_{\theta JA}$ given in the *Thermal Information* table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application. The data given for $R_{\theta JC(bott)}$ and Ψ_{JT} can be useful when determining thermal performance. See the *Semiconductor and IC Package Thermal Metrics Application Report* for more information and the resources given at the end of this section.

$$I_{OUT\_MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{1-\eta} \times \frac{1}{V_{OUT}} \tag{22}$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

8.2.3 Application Curves

V_{IN} = 24 V, V_{OUT} = 5 V, L_1= 6.8 µH, C_{OUT} = 44 µF, T_A = 25°C (unless otherwise noted)

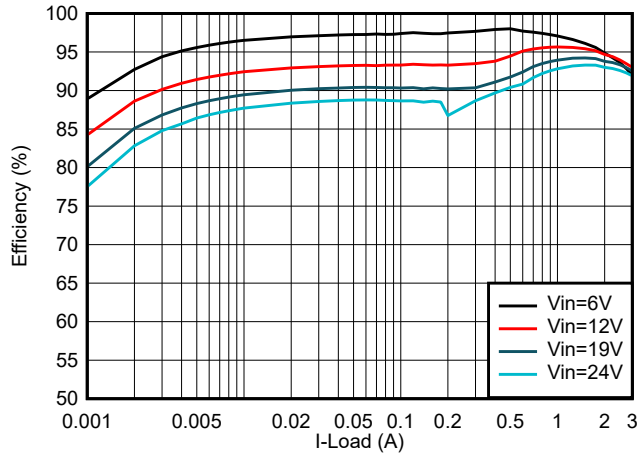

図 8-2. Efficiency

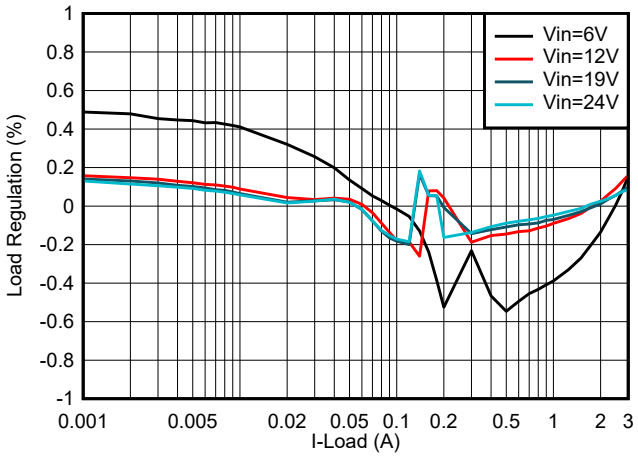

図 8-3. Load Regulation

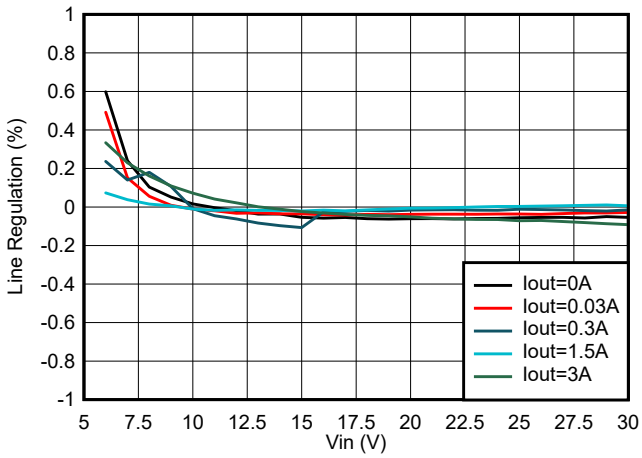

図 8-4. Line Regulation

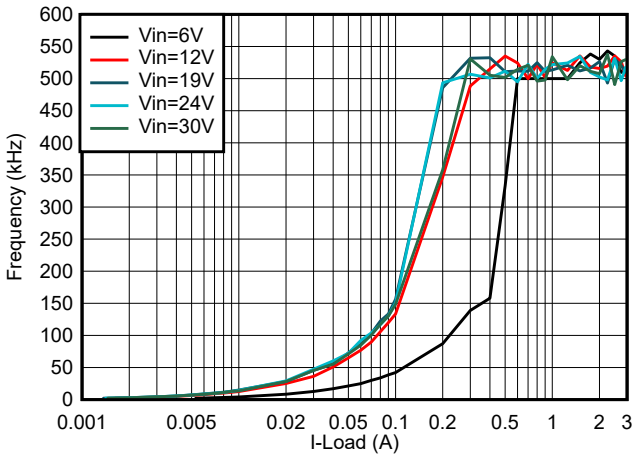

図 8-5. Switching Frequency vs Load Current

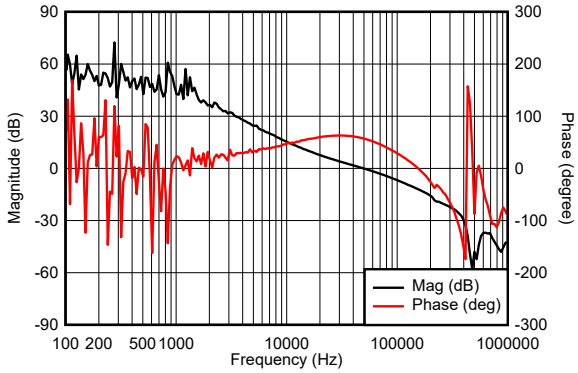

図 8-6. Loop Frequency Response, I_{OUT} = 3 A, BW = 49.4 kHz, PM = 57°, GM = –12 dB

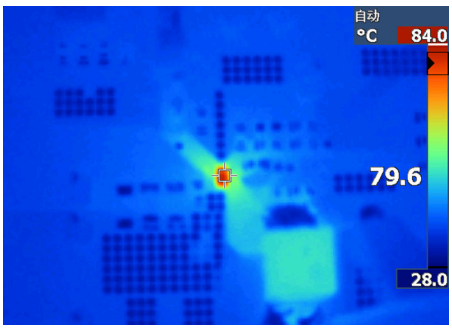

図 8-7. Case Temperature, V_{IN} = 24 V, I_{OUT} = 3 A, f_{SW} = 500 kHz

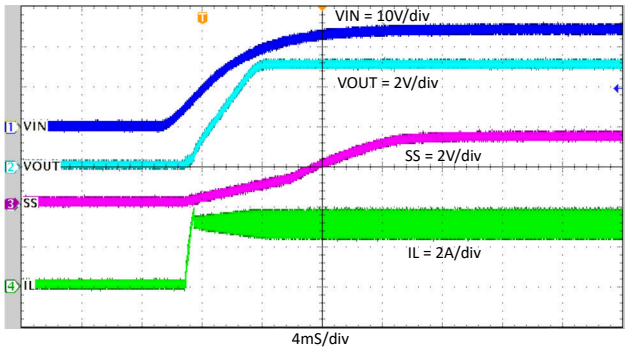

図 8-8. Start-Up Relative to V_{IN}, I_{OUT} = 3 A

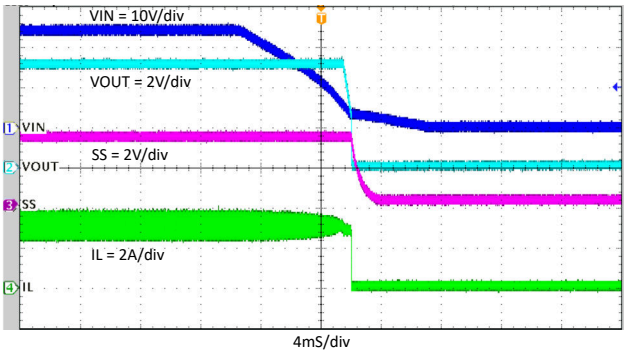

図 8-9. Shutdown Relative to V_{IN}, I_{OUT} = 3 A

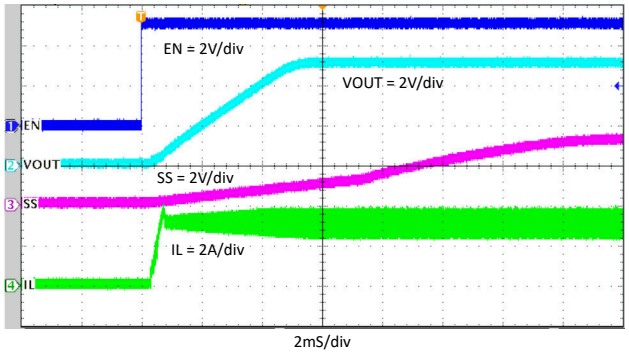

図 8-10. Start-Up Through EN, I_{OUT} = 3 A

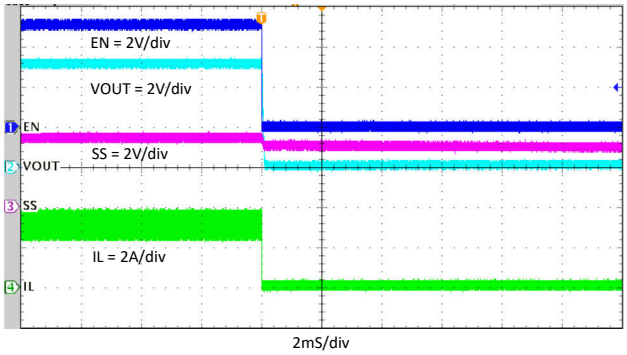

図 8-11. Shutdown Through EN, I_{OUT} = 3 A

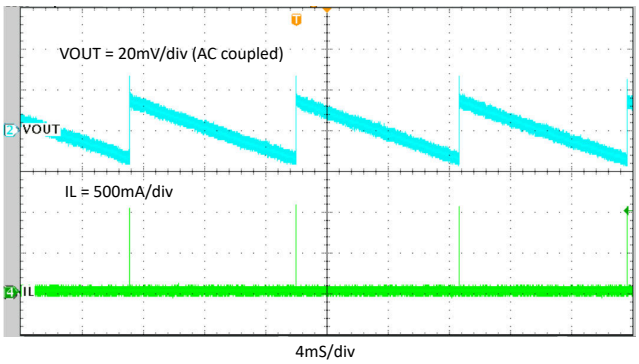

図 8-12. Steady State, I_{OUT} = 0 A

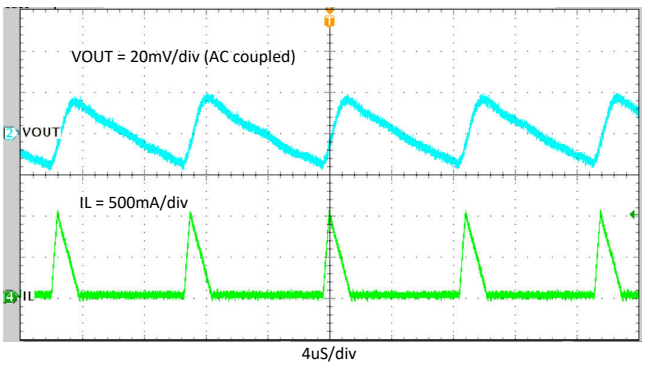

図 8-13. Steady State, I_{OUT} = 0.1 A

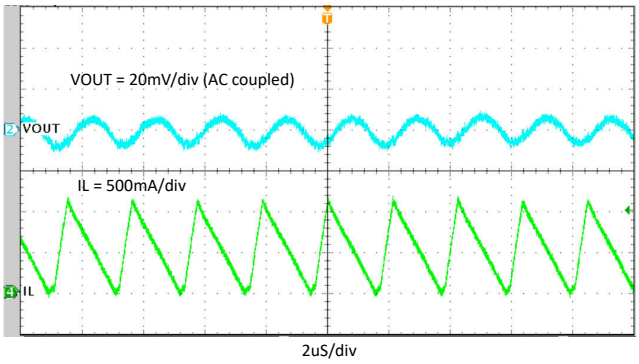

図 8-14. Steady State, I_{OUT} = 0.5 A

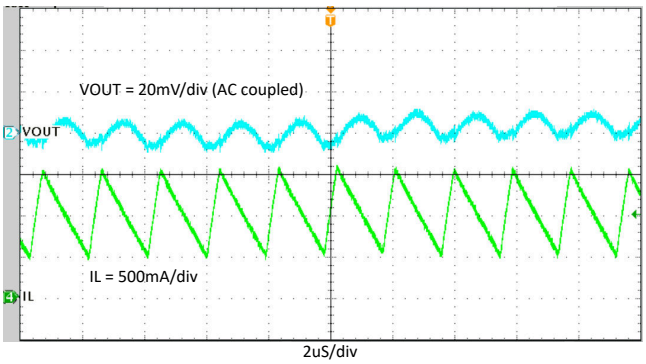

図 8-15. Steady State, I_{OUT} = 1 A

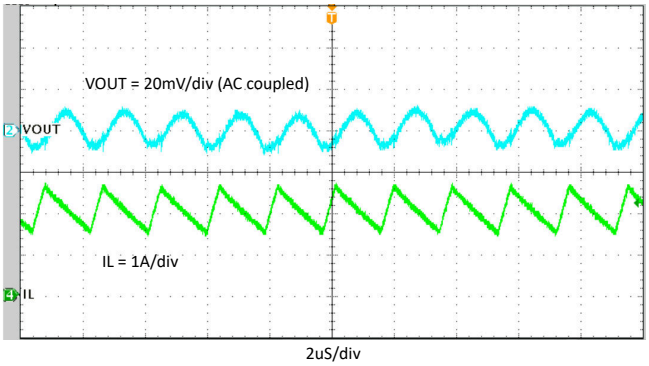

図 8-16. Steady State, I_{OUT} = 2 A

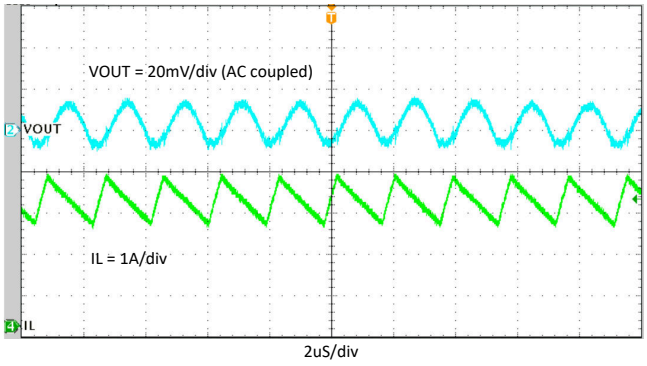

図 8-17. Steady State, I_{OUT} = 3 A

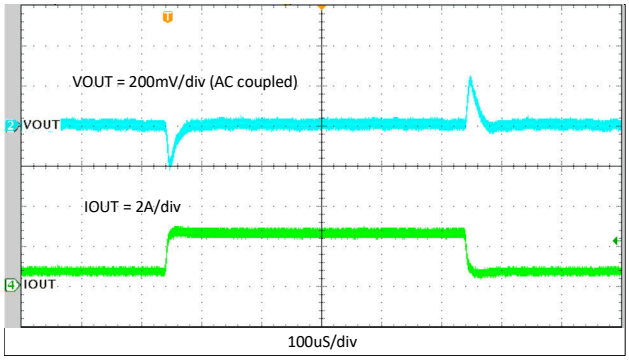

図 8-18. Load Transient Response, 0.5 to 2.5 A, Slew Rate = 0.8 A/µS

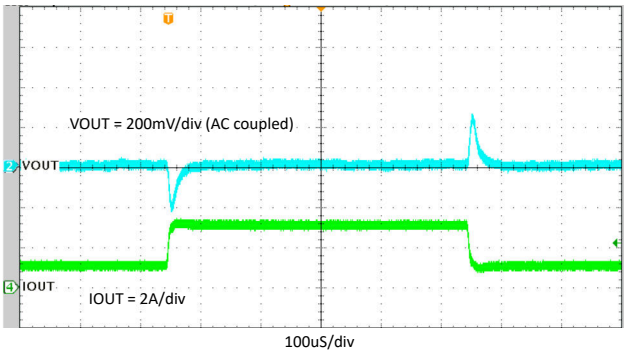

図 8-19. Load Transient Response, 1 to 3 A, Slew Rate = 0.8 A/µS

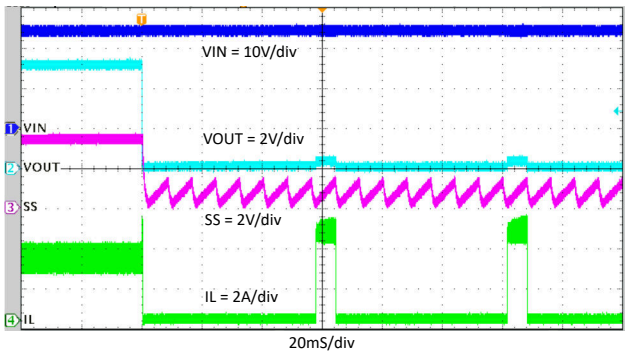

図 8-20. V_{OUT} Hard Short Protection

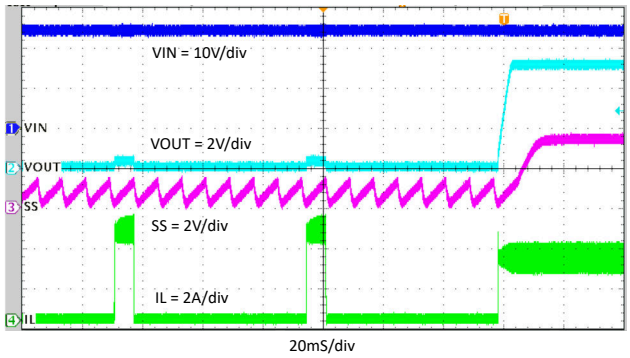

図 8-21. V_{OUT} Hard Short Recovery

8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings.*
- Do not exceed the *Recommended Operating Conditions.*
- Do not exceed the *ESD Ratings.*
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Do not use the value of $R_{\theta JA}$ given in the *Thermal Information* table to design your application. See セクション 8.2.2.9.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.
- Use a 100-nF capacitor connected directly to the VIN and GND pins of the device. See セクション 8.2.2.7 for details.

8.4 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.8 V and 30 V. This input supply must be well regulated and compatible with the limits found in the specifications of this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded converter. The average input current can be estimated with 式 23.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{23}$$

where

- η = efficiency

If the converter is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the converter. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the converter. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the converter to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the converter and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help damp the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

It is recommended that the input supply must not be allowed to fall below the output voltage by more than 0.3 V. Under such conditions, the output capacitors discharges through the body diode of the high-side power MOSFET. The resulting current can cause unpredictable behavior, and in extreme cases, possible device

damage. If the application allows for this possibility, then use a Schottky diode from VIN to VOUT to provide a path around the converter for this current.

In some cases, a transient voltage suppressor (TVS) is used on the input of converters. One class of this device has a snap-back characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the converter, the output capacitors discharges through the device, as mentioned above.

Sometimes, for other system considerations, an input filter is used in front of the converter. This can lead to instability as well as some of the effects mentioned above, unless it is designed carefully. The *AN-2162 Simple Success with Conducted EMI from DCDC Converters User's Guide* provides helpful suggestions when designing an input filter for any switching converter.

8.5 Layout

8.5.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of a good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitors and power ground, as shown in 図 8-22. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance.

TI recommends a 2-layer board with 2-oz copper thickness of top and bottom layer, and proper layout provides low current conduction impedance, proper shielding, and lower thermal resistance. 図 8-23 and 図 8-24 show the recommended layouts for the critical components of the TPS563300.

- Place the inductor, input and output capacitors, and the IC on the same layer.
- Place the input and output capacitors as close as possible to the IC. The VIN and GND traces must be as wide as possible and provide sufficient vias on them to minimize trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
- Place a 0.1-µF ceramic decoupling capacitor or capacitors as close as possible to VIN and GND, which is key to EMI reduction.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Place a BST capacitor and resistor close to BST pin and SW node. > 10-mil width trace is recommended to reduce the parasitic inductance.
- Place the feedback divider as close as possible to the FB pin. > 10-mil width trace is recommended for heat dissipation. Connect a separate V_{OUT} trace to the upper feedback resistor. Place the voltage feedback loop away from the high-voltage switching trace. The feedback loop preferably has ground shield.

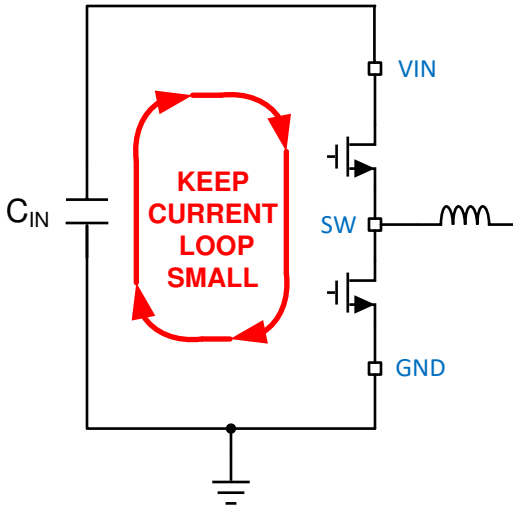

図 8-22. Current Loop With Fast Edges

8.5.2 Layout Example

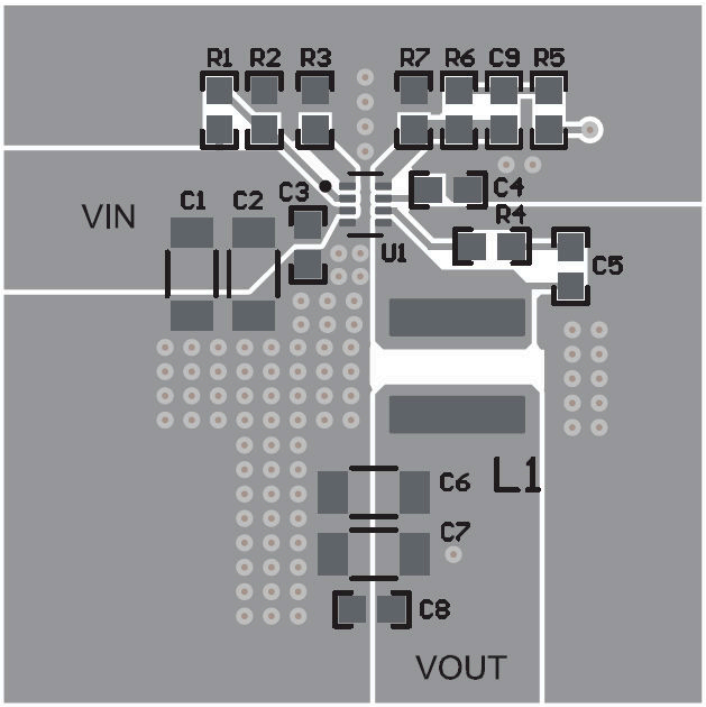

図 8-23. TPS563300 Top Layout Example

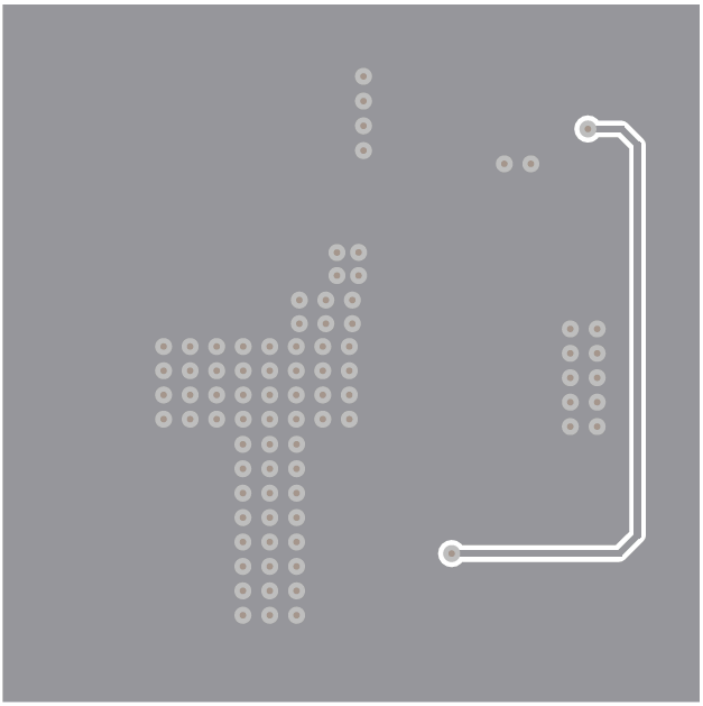

図 8-24. TPS563300 Bottom Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS563300 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application report
- Texas Instruments, *AN-2162 Simple Success with Conducted EMI from DCDC Converters* user's guide

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS563300DRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 150	3300
TPS563300DRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3300
TPS563300DRLR.B	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 150	3300

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

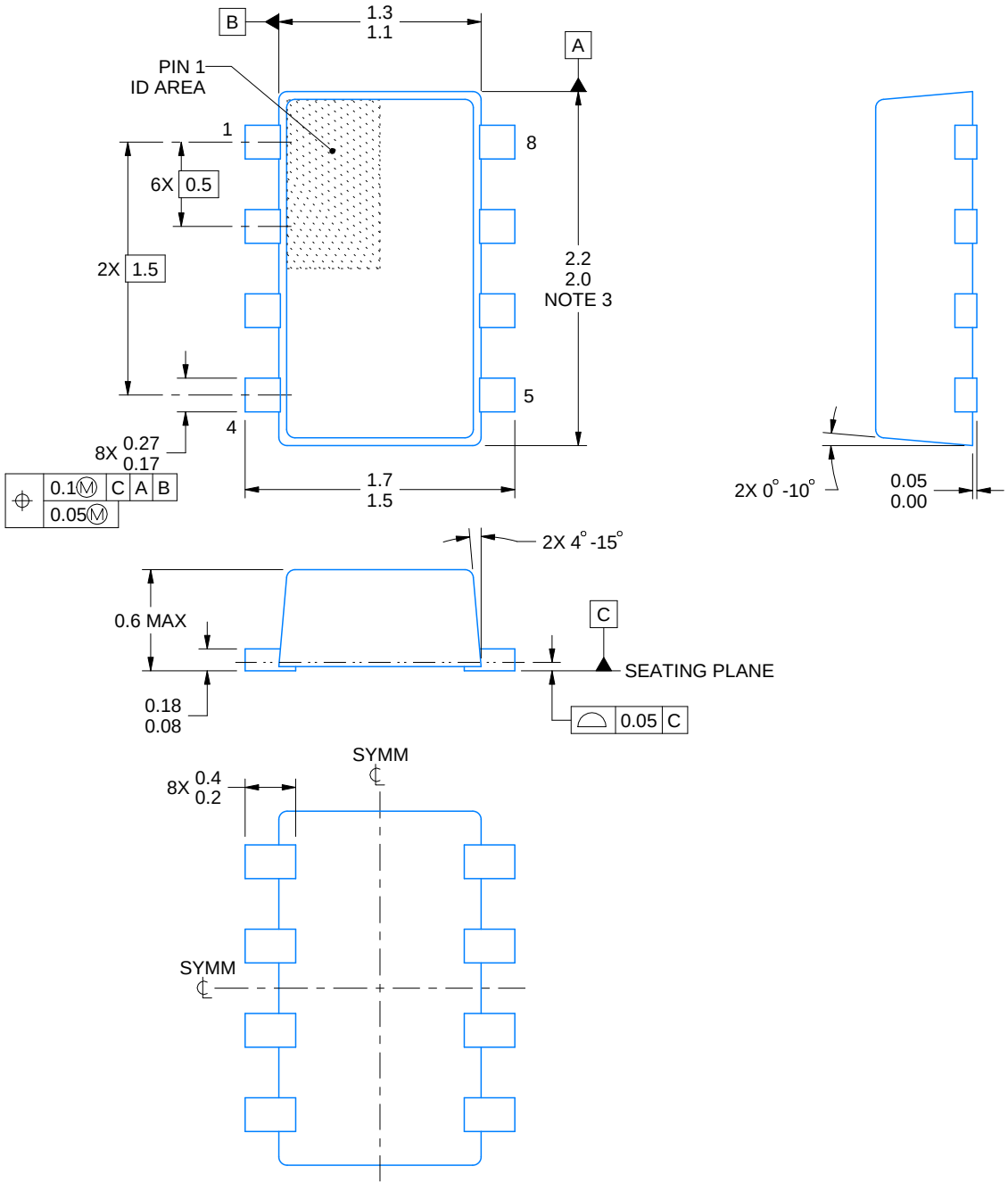
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

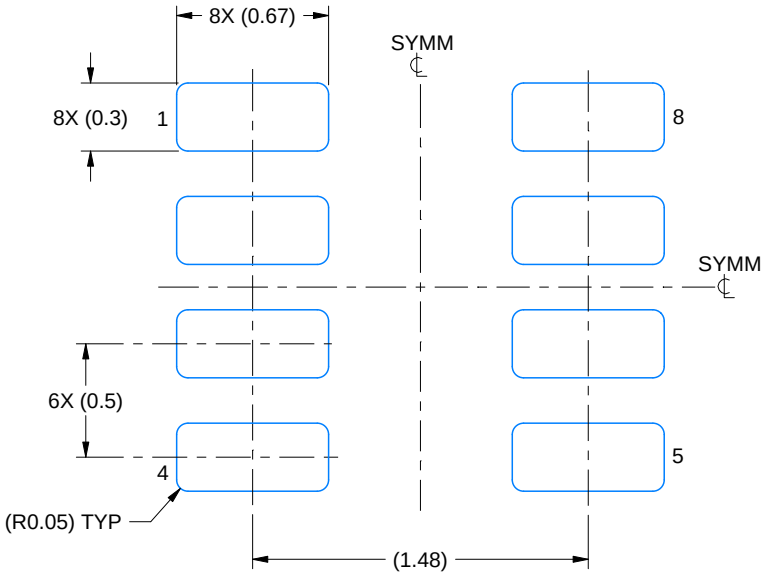
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

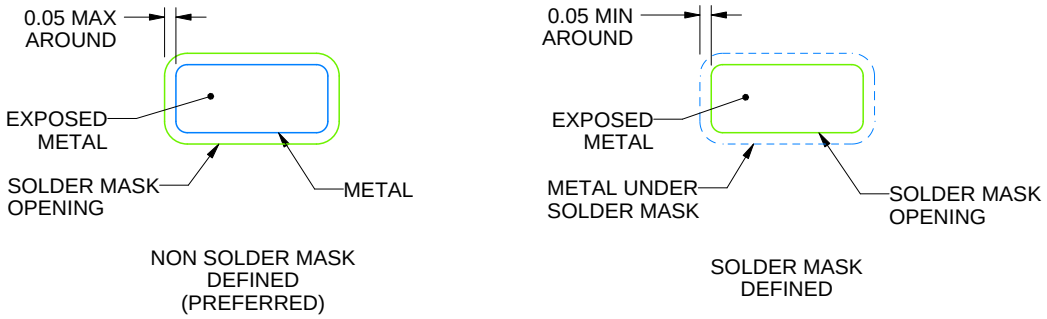
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

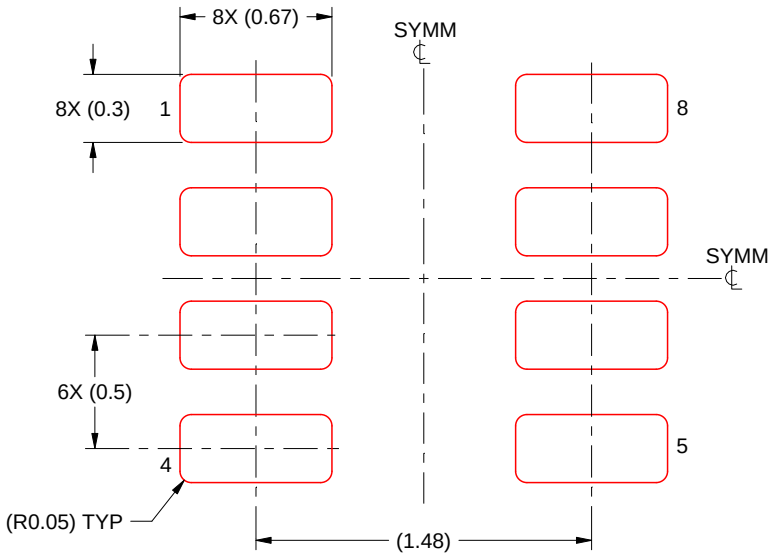
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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