



TPS563249 17V、3A、固定 1.4MHz 同期整流降圧電圧レギュレータ

1 特長

- 70mΩおよび 30mΩのFET内蔵の3Aコンバータ
- D-CAP3™モード制御による高速過渡応答
- 入力電圧範囲: 4.5V~17V
- 出力電圧範囲: 0.6V~7V
- 強制連続導通モード
- 固定1.4MHzのスイッチング周波数
- 低いシャットダウン電流: 10μA未満
- 帰還電圧精度: 1% (25°C)
- プリバイアス出力電圧からのスタートアップ
- サイクル単位の過電流制限
- ヒカップ・モードによる過電流保護
- 非ラッチUVPおよびTSD保護
- 固定ソフトスタート: 1.7ms

2 アプリケーション

- ブロードバンド・モデム
- アクセス・ポイント・ネットワーク
- ワイヤレス・ルータ
- 監視機器
- TV、セットトップ・ボックス

3 概要

TPS563249は、単純で使いやすい3A同期整流降圧型コンバータで、SOT-23パッケージに搭載されています。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が低くなるよう最適化されています。

このスイッチング・レギュレータは、D-CAP3 モード制御によって高速の過渡応答を実現します。また、特殊ポリマーなど ESR (等価直列抵抗) の低い出力コンデンサと、超低 ESR のセラミック・コンデンサの両方を、外部補償部品なしでサポートします。

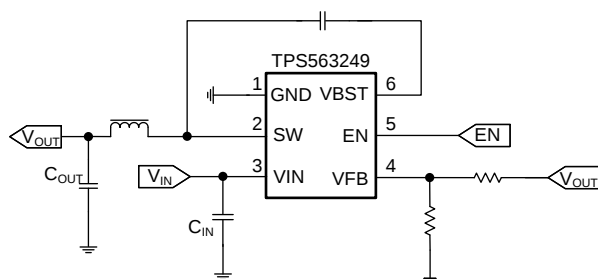
TPS563249は強制連続導通モード(FCCM)で動作し、軽負荷での動作時にも1.4MHzの固定スイッチング周波数を維持し、システムの干渉を排除します。TPS563249は6ピンの1.6mm×2.9mm SOT (DDC)パッケージで供給され、接合部温度-40°C~125°Cで動作が規定されています。

製品情報⁽¹⁾

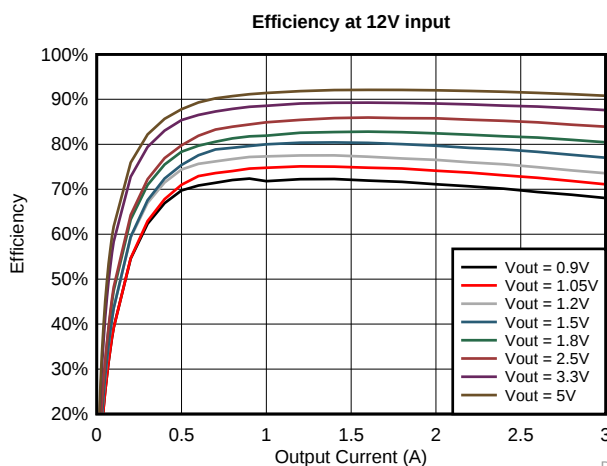
型番	パッケージ	本体サイズ(公称)
TPS563249	SOT-23-THIN (6)	1.60mm×2.90mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



TPS563249の効率



D001



目次

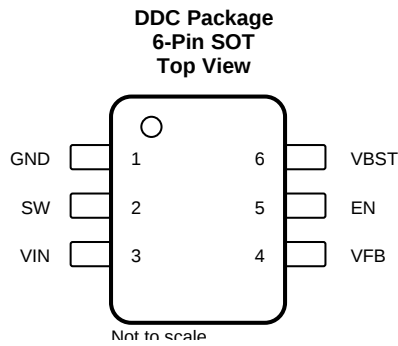
1	特長	1	7.4	Device Functional Modes.....	11
2	アプリケーション	1	8	Application and Implementation	12
3	概要	1	8.1	Application Information.....	12
4	改訂履歴	2	8.2	Typical Application	12
5	Pin Configuration and Functions	3	9	Power Supply Recommendations	16
6	Specifications	4	10	Layout	17
6.1	Absolute Maximum Ratings	4	10.1	Layout Guidelines	17
6.2	ESD Ratings.....	4	10.2	Layout Example	17
6.3	Recommended Operating Conditions.....	4	11	デバイスおよびドキュメントのサポート	18
6.4	Thermal Information	4	11.1	ドキュメントの更新通知を受け取る方法.....	18
6.5	Electrical Characteristics.....	5	11.2	コミュニティ・リソース	18
6.6	Typical Characteristics	6	11.3	商標	18
7	Detailed Description	9	11.4	静電気放電に関する注意事項	18
7.1	Overview	9	11.5	Glossary	18
7.2	Functional Block Diagram	9	12	メカニカル、パッケージ、および注文情報	18
7.3	Feature Description.....	9			

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2018年12月	*	初版

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 μ F capacitor between VBST and SW pins.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	V _{IN}	−0.3	19	V
	V _{BST}	−0.3	24.5	V
	V _{BST} (10 ns transient)	−0.3	26.5	V
	V _{BST} (vs SW)	−0.3	5.5	V
	V _{FB}	−0.3	5.5	V
	SW	−2	19	V
	SW (10 ns transient)	−3.5	21	V
	EN	−0.3	V _{IN} + 0.3	V
Operating junction temperature, T _J		−40	150	°C
Storage temperature, T _{stg}		−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Supply input voltage range	4.5		17	V
EN	EN Input voltage range	−0.1		V _{IN}	V
T _J	Operating junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS563249	UNIT
		DDC (SOT)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	117.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	57.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	31.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	11.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	31.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

 $T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VIN(SDN)}	Shutdown supply current	V _{IN} current, EN = 0 V, T _J = 25°C	2.5	10		μA
LOGIC THRESHOLD						
V _{ENH}	Enable threshold	Rising	1.27	1.34		V
V _{ENL}	Enable threshold	Falling	1.08	1.15		V
R _{EN}	EN pin resistance to GND	V _{EN} = 1 V	800	1000	1200	kΩ
V _{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V _{FB}	FB voltage	T _J = 25°C	594	600	606	mV
			588	600	612	mV
I _{FB}	FB input current	V _{FB} = 0.7 V	0	±50		nA
MOSFET						
R _{DS(on)h}	High-side switch resistance	T _J = 25°C	70			mΩ
R _{DS(on)l}	Low-side switch resistance	T _J = 25°C	30			mΩ
CURRENT LIMIT						
I _{ocl_h_source}	High side FET source Current limit		5.5	6.3	7.1	A
I _{ocl_l_source}	Low side FET source Current limit		3.1	3.9	4.7	A
I _{ocl_l_sink}	Low side FET sink Current limit		1.1	1.7		A
THERMAL SHUTDOWN						
T _{SDN}	Thermal shutdown threshold ⁽¹⁾	Shutdown temperature	160			°C
		Hysteresis	25			
ON-TIME TIMER CONTROL						
t _{ON(MIN)}	Minimum on time ⁽¹⁾	V _{IN} = 12 V, load = 3 A	50			ns
t _{OFF(MIN)}	Minimum off time		250			ns
SOFT START						
t _{ss}	Soft-start time	Internal soft-start time	1.7			ms
FREQUENCY						
F _{sw}	Switching frequency		1250	1400	1550	kHz
OUTPUT UNDERVOLTAGE PROTECTION						
V _{UVP}	Output UVP threshold	Hiccup detect (H > L)	65%			
t _{UVPDLY}	UVP propagation delay		0.36			ms
t _{HIC}	UVP protection Hiccup Time before restart		25			ms
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage	4.2	4.4		V
		Shutdown VIN voltage	3.6	3.8		
		Hysteresis VIN voltage	0.4			

(1) Not production tested.

6.6 Typical Characteristics

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

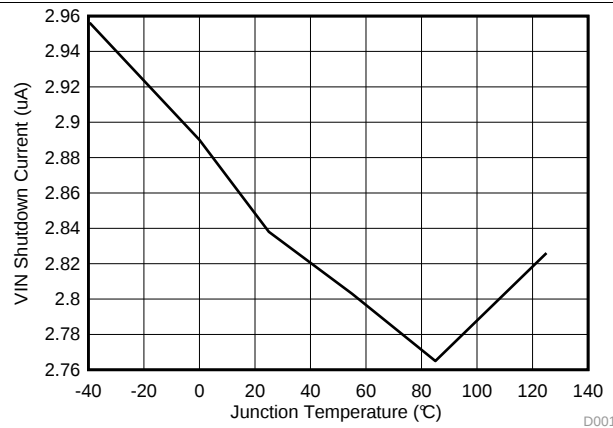


图 1. Shutdown Current vs Junction Temperature

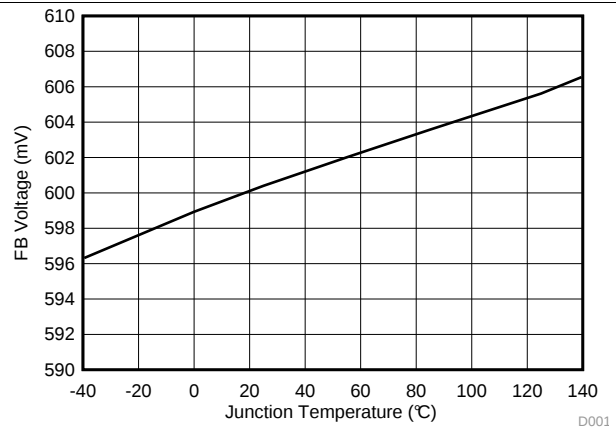


图 2. VFB Voltage vs Junction Temperature

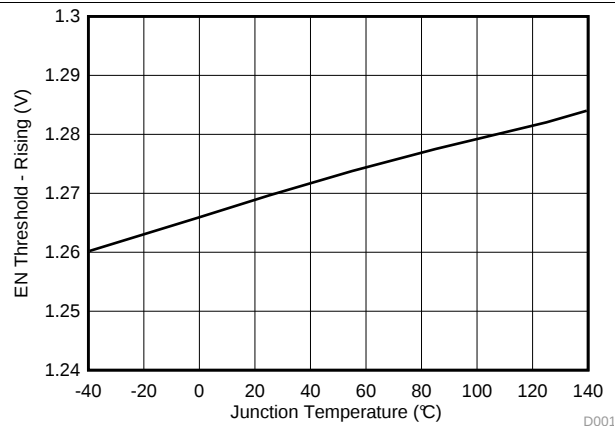


图 3. EN Rising threshold vs Junction Temperature

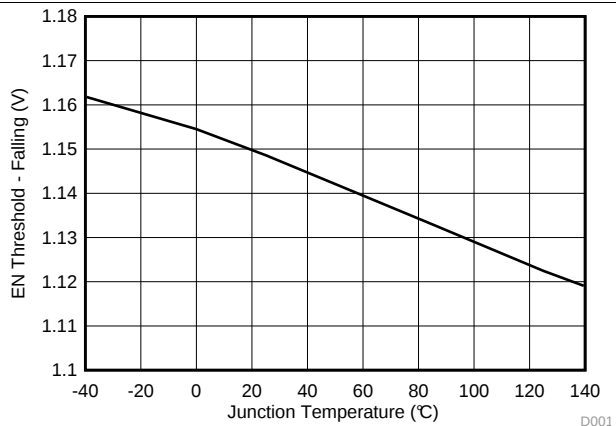


图 4. EN Falling threshold vs Junction Temperature

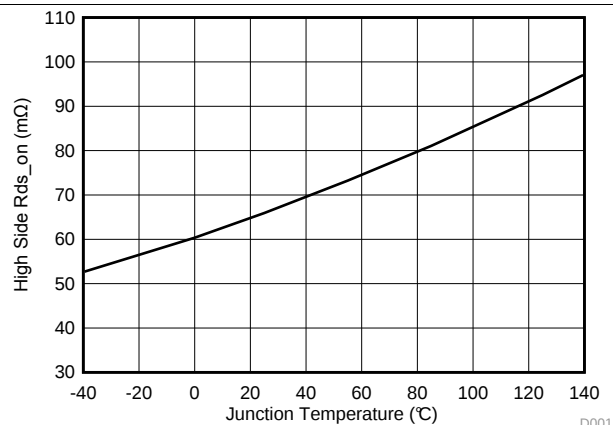


图 5. High-Side $R_{ds(on)}$ vs Junction Temperature

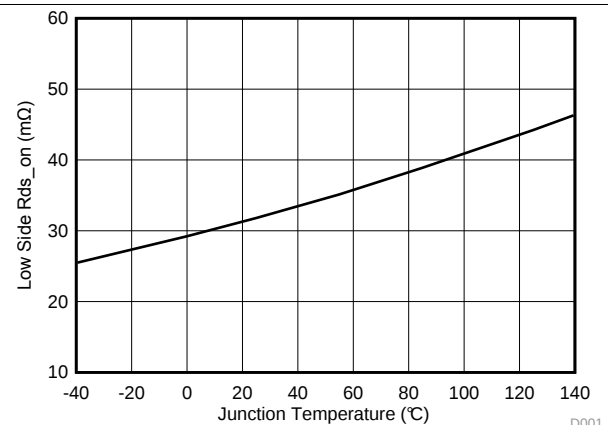


图 6. Low-Side $R_{ds(on)}$ vs Junction Temperature

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

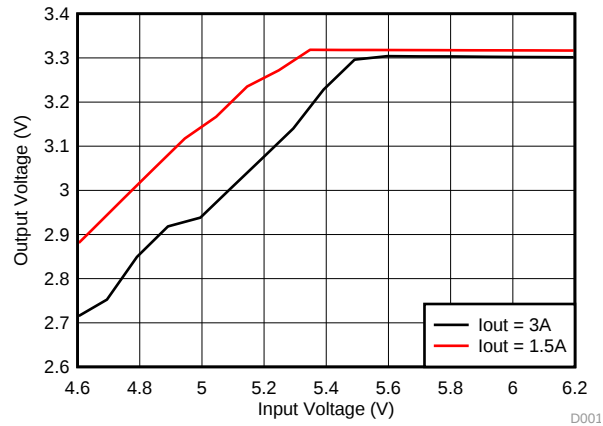


FIG 7. Dropout for 3.3 V Output Voltage

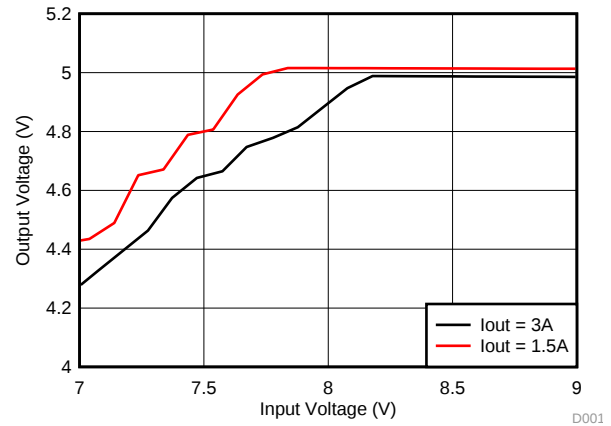


FIG 8. Dropout for 5 V Output Voltage

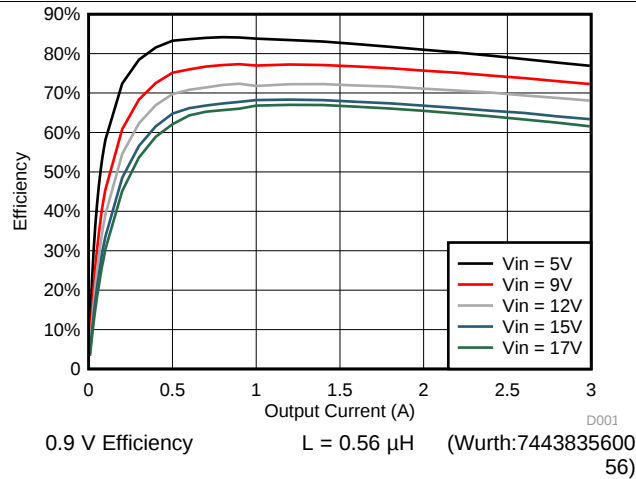


FIG 9. Efficiency vs Output Current, $V_{OUT} = 0.9\text{ V}$

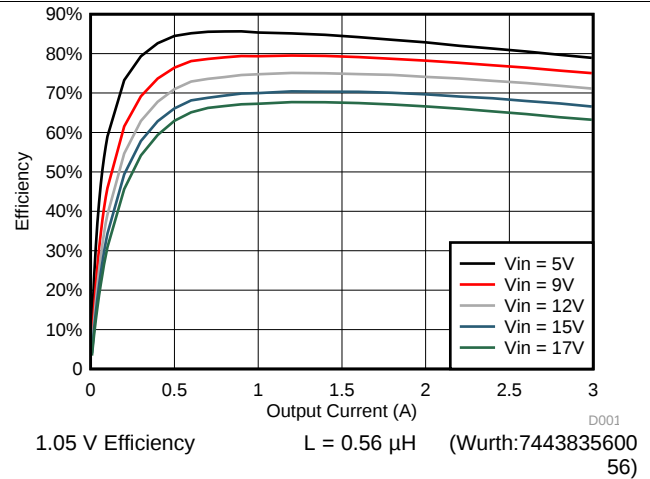


FIG 10. Efficiency vs Output Current, $V_{OUT} = 1.05\text{ V}$

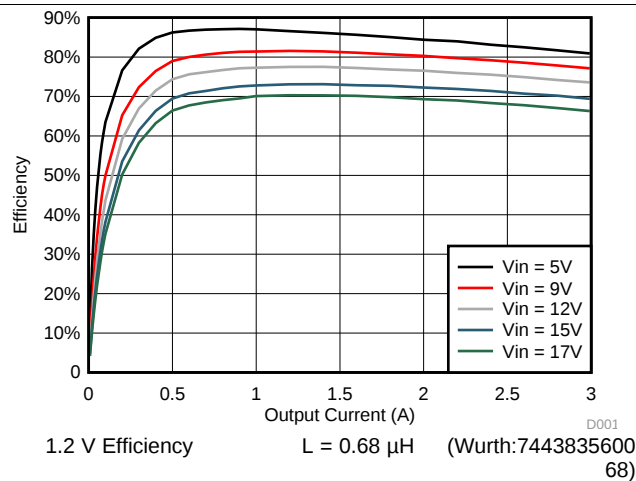


FIG 11. Efficiency vs Output Current, $V_{OUT} = 1.2\text{ V}$

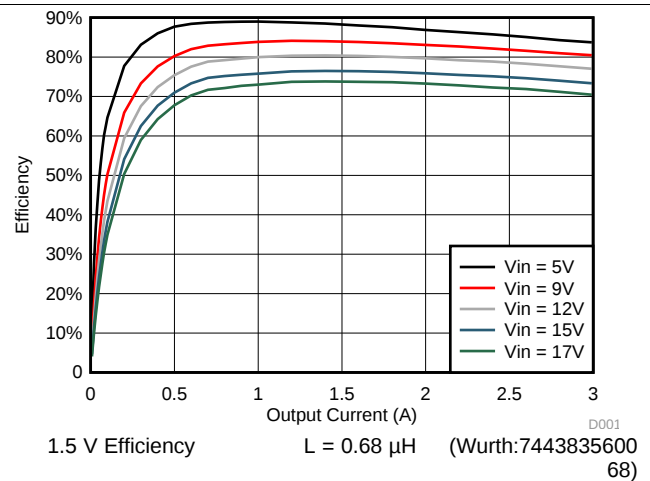


FIG 12. Efficiency vs Output Current, $V_{OUT} = 1.5\text{ V}$

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

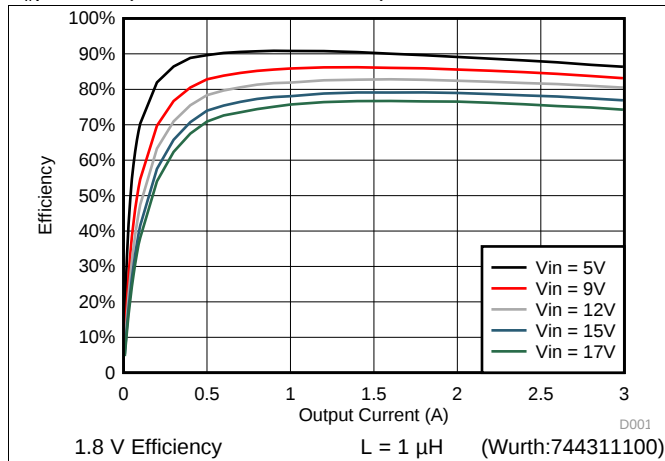


Fig 13. Efficiency vs Output Current, $V_{OUT} = 1.8\text{ V}$

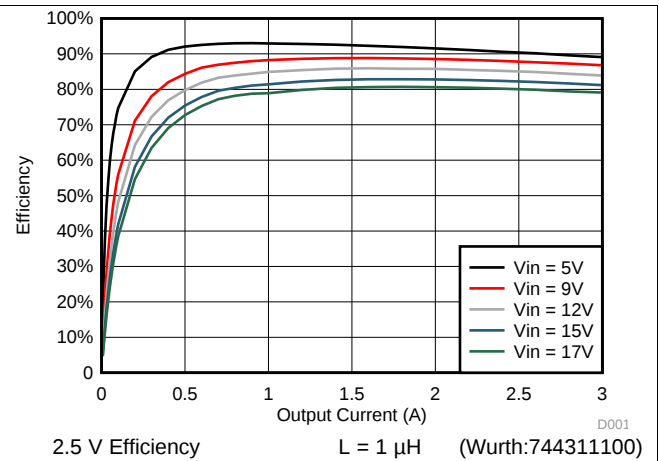


Fig 14. Efficiency vs Output Current, $V_{OUT} = 2.5\text{ V}$

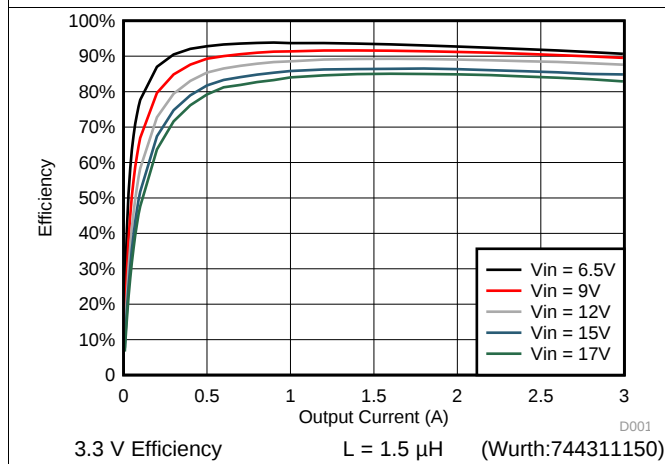


Fig 15. Efficiency vs Output Current, $V_{OUT} = 3.3\text{ V}$

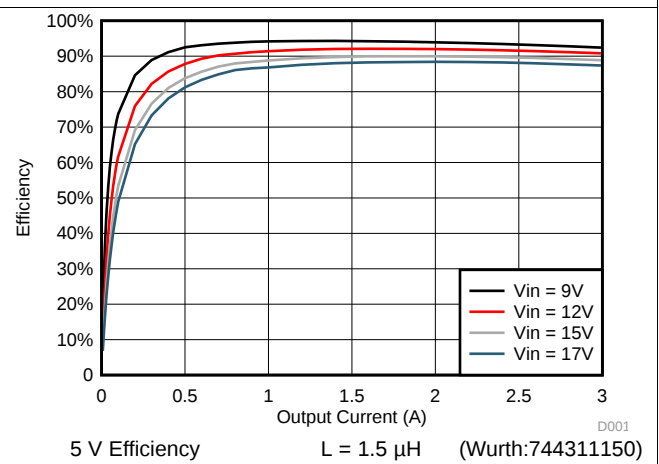


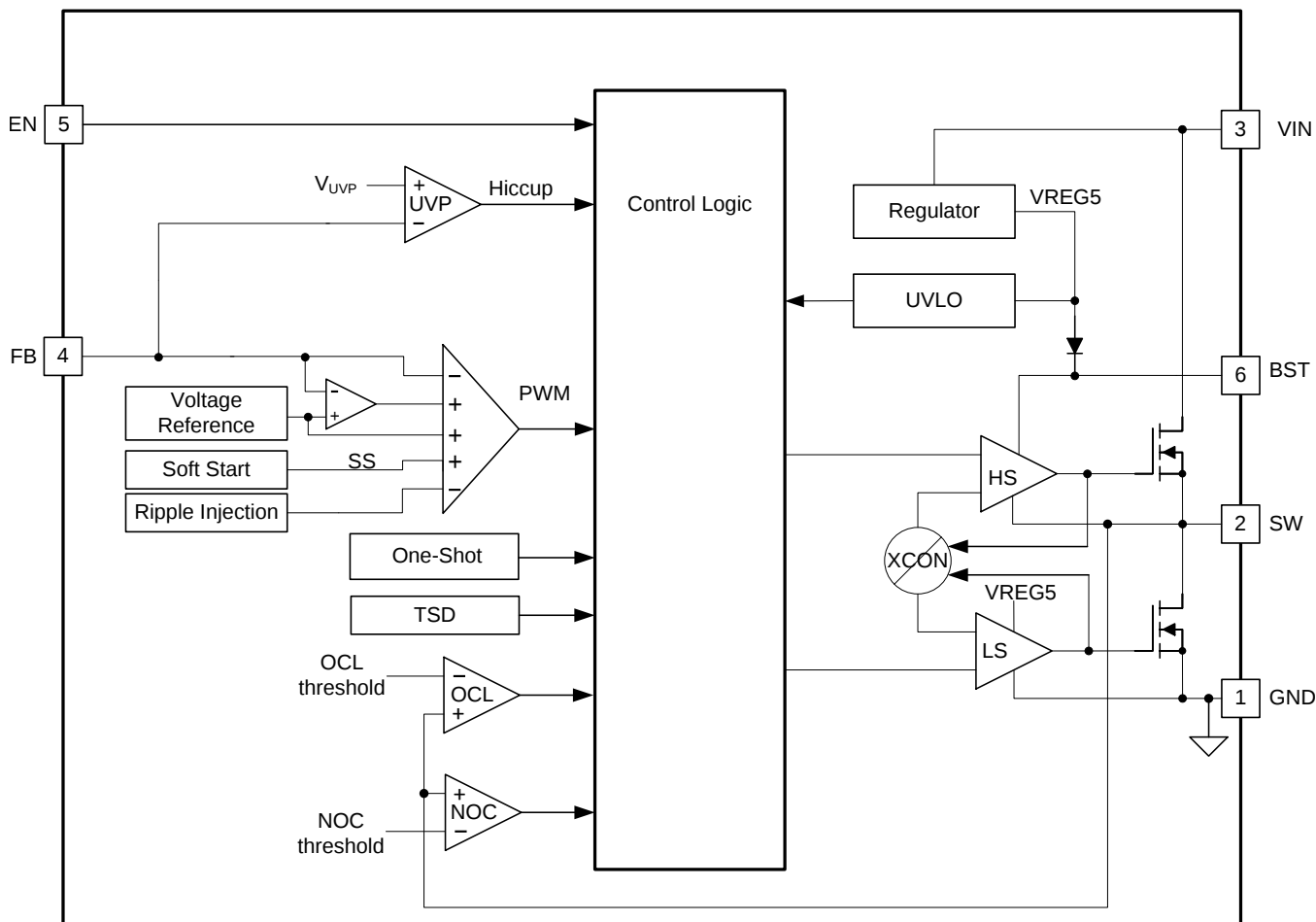
Fig 16. Efficiency vs Output Current, $V_{OUT} = 5\text{ V}$

7 Detailed Description

7.1 Overview

The TPS563249 is a 3-A synchronous step-down converter. The proprietary D-CAP3 mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP3 mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS563249 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 mode control. The D-CAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, V_{IN} , and inversely proportional to the output voltage, V_O , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP3 mode control.

Feature Description (continued)

7.3.2 Soft Start and Pre-Biased Soft Start

The TPS563249 has an internal 1.7-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB} . This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.3 Current Protection

There are three kinds of current protection in TPS563249: High-side FET source current limit, low-side FET source current limit, and low-side FET sink current limit.

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the low-side FET switch, the inductor current flow through low-side FET and decreases linearly. The average value of the inductor current is the load current I_{OUT} . If the monitored current is above the low-side FET source current limit level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current cross the low-side FET source current limit level. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the V_{FB} voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 0.36 ms) and re-start after the hiccup time (typically 25 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

During the on time of the high-side FET switch, the inductor current flow through high-side FET and increases at a linear rate determined by V_{IN} , V_{OUT} , the on-time and the output inductor value. The switch current is compared with high-side FET source current limit after a short blanking time. If the cross-limit event detected before the one shot timer expires, the high-side FET is turn off immediately, and is not allowed on in the following 1 μ S period.

TPS563249 works in Forced Continuous Conduction Mode (FCCM). To support light load operation, the current flowing through low-side FET is allowed to be negative, which means the current flow from drain to source of low-side FET. This negative current is compared with low-side FET sink current limit to prevent device from being over-current damaged. Once the sink current cross limit, the low-side FET is turn off immediately. Both high-side FET and low-side FET will keep off until the V_{FB} voltage falls below reference voltage.

7.3.4 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.5 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the thermal shutdown threshold value (typically 160°C), the device will shut off. This is a non-latch protection. The device will resume normal working once the temperature return below the recovery threshold value (typically 135°C).

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS563249 can operate in the continuous conduction mode (CCM) at a fixed frequency of 1.4 MHz. If EN pin is driven by a control signal, the required power on sequence is that applying input voltage at VIN pin firstly, then pull EN pin high. Be sure that the EN pin voltage isn't higher than VIN pin voltage. If EN pin is not used, it can be tied to VIN pin directly.

7.4.2 Standby Operation

TPS563249 can be placed in standby by asserting the EN pin low.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical step-down DC-DC converter. It is typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the TPS563249. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in [Figure 17](#) was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

[Figure 17](#) shows the TPS563249 6.5-V to 17-V input, 3.3-V output converter schematic.

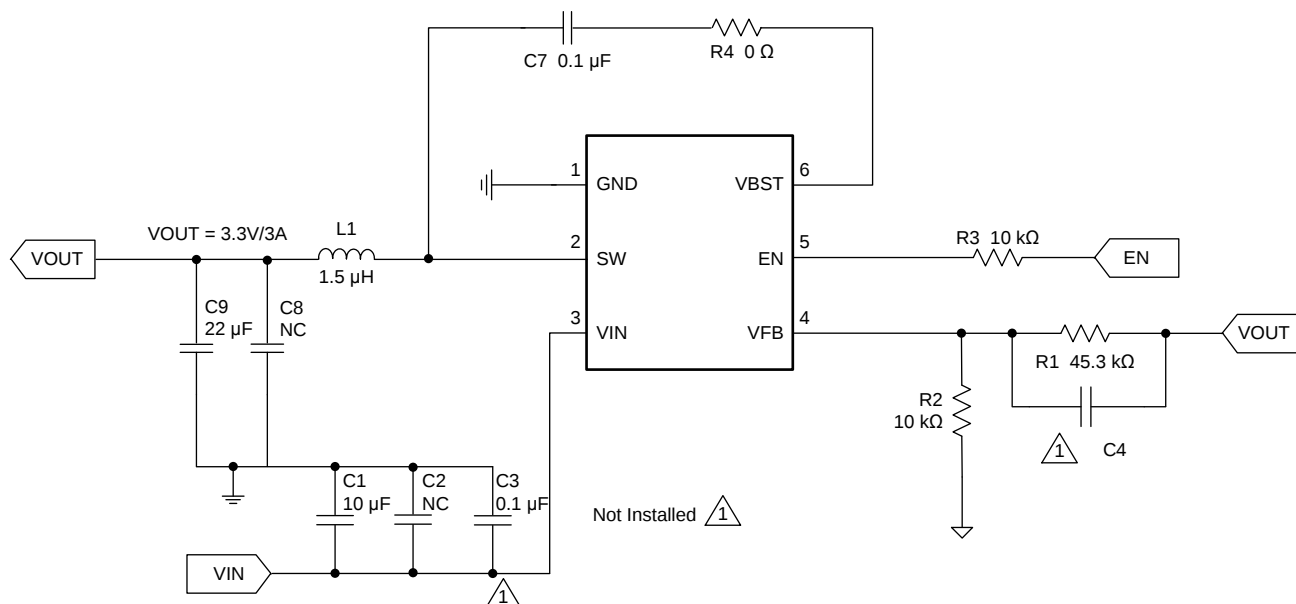


Figure 17. 3.3-V/3-A Reference Design

Typical Application (continued)

8.2.1 Design Requirements

表 1 shows the design parameters for this application.

表 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	6.5 to 17 V
Output voltage	3.3 V
Transient response, 1.5-A load step	$\Delta V_{OUT} = \pm 5\%$
Input ripple voltage	400 mV
Output ripple voltage	100 mV
Output current rating	3 A
Operating frequency	1.4 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 式 1 to calculate V_{OUT} .

Too high of resistance is more susceptible to noise, and voltage errors from the VFB input current is more noticeable.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (2)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP3 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 2 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 2.

表 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)			C8 + C9 (μF)
			MIN	TYP	MAX	
1	6.65	10.0	0.33	0.56	1	10 to 44
1.05	7.5	10.0	0.33	0.56	1	10 to 44
1.2	10	10.0	0.47	0.68	1.5	10 to 44
1.5	15	10.0	0.47	0.82	1.5	10 to 44
1.8	20	10.0	0.56	1	2.2	10 to 44
2.5	31.6	10.0	0.68	1	2.2	10 to 44
3.3	45.3	10.0	0.82	1.5	3.3	10 to 44
5	73.2	10.0	1	1.5	3.3	10 to 44
6.5	97.6	10.0	1	1.5	3.3	10 to 44

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 3, 式 4, and 式 5. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (3)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (4)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (5)$$

For this design example, the calculated peak current is 3.63 A and the calculated RMS current is 3.02 A. The inductor used is a WE 744311150 with a rated current of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563249 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 10 μ F to 44 μ F. Use 式 6 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (6)$$

For this design one Murata GRM31CR61A226KE19 22- μ F output capacitor is used. The typical ESR is 2 m Ω . The calculated RMS current is 0.365 A and output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS563249 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 μ F for the decoupling capacitor. An additional 0.1- μ F capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1- μ F ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.2.5 Dropout

With a constant 1.4-MHz switching frequency, there is a minimum input voltage limit for a given output voltage to be regulated. This is due to the minimum off time limit. If the input voltage less than the minimum input voltage limit, the output voltage drops accordingly, which is called dropout condition. 图 7 and 图 8 show the typical dropout curve for 3.3 V and 5 V output voltage with 3 A and 1.5 A load respectively. 式 7 can be used to estimate this minimum input voltage limit.

$$V_{IN(MIN)} = \frac{\frac{V_{OUT}}{F_{SW}} + (R_{dsl} + R_L) \times I_O \times (t_{off(min)} - t_{d1} - t_{d2}) + (V_d + R_L \times I_O) \times (t_{d1} + t_{d2})}{\frac{1}{F_{SW}} - t_{off(min)}} + (R_{dsh} + R_L) \times I_O$$

where

- V_{OUT} = target output voltage
- F_{SW} = maximum switching frequency including tolerance
- $t_{off(min)}$ = minimum off time including tolerance
- R_{dsl} = low side FET on resistance
- R_{dsh} = high side FET on resistance
- R_L = inductor DC resistance
- I_O = maximum load current
- t_{d1} = dead time between high side FET off and low side FET on, 15nS typical
- t_{d2} = dead time between low side FET off and high side FET on, 10nS typical
- V_d = forward voltage of low side FET body diode

(7)

8.2.3 Application Curves

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{ V}$ (unless otherwise noted)

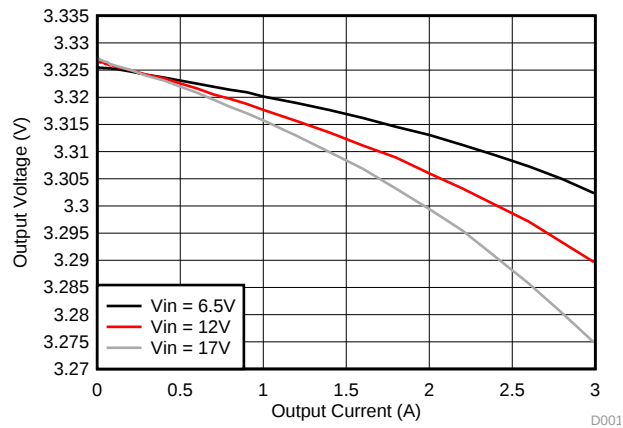


Figure 18. Load Regulation

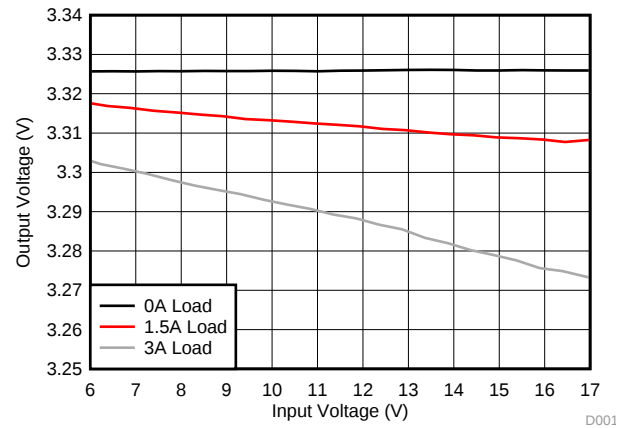


Figure 19. Line Regulation

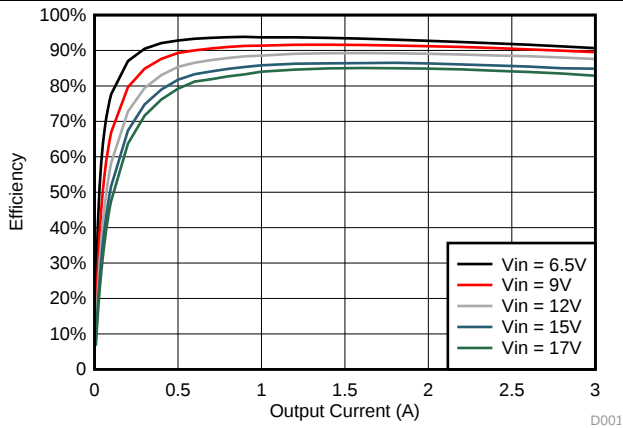


Figure 20. Efficiency

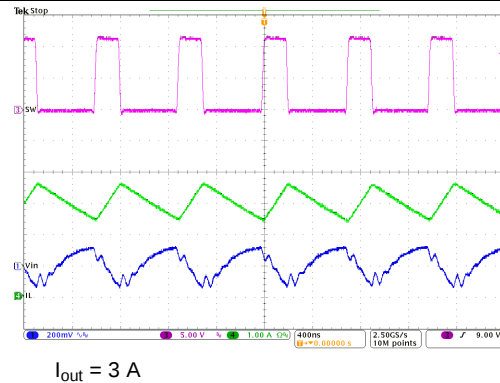


Figure 21. Input Voltage Ripple

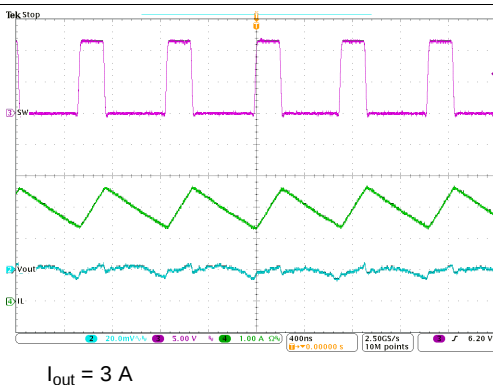


Figure 22. Output Voltage Ripple

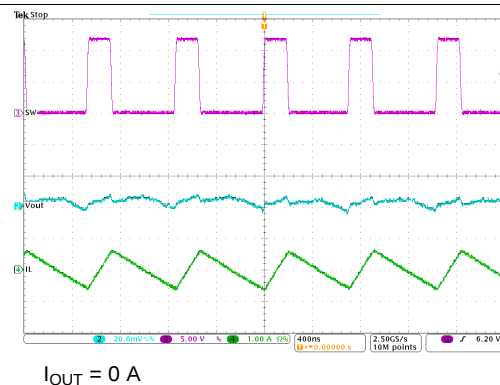
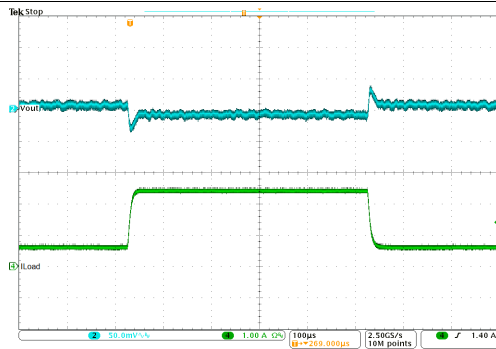
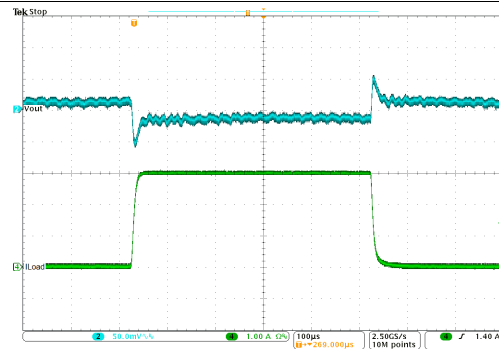


Figure 23. Output Voltage Ripple



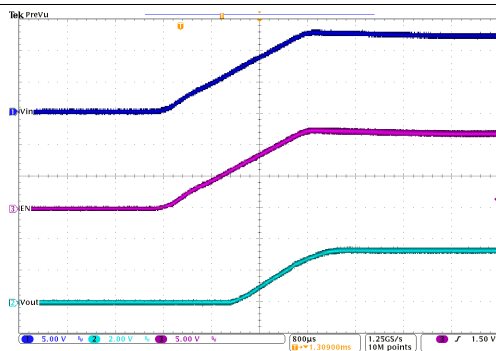
Slew rate is 1.6 A/µS

24. Transient Response, 0.6 to 2.4 A



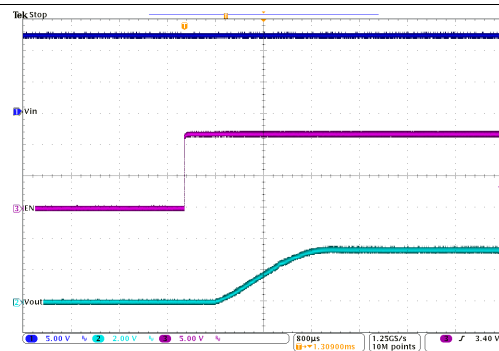
Slew rate is 1.6 A/µS

25. Transient Response, 0 to 3 A



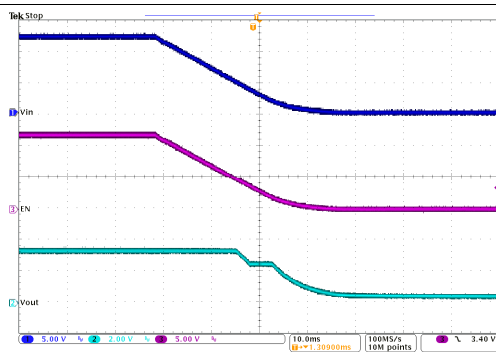
$I_{OUT} = 0$ A

26. Start Up Relative to V_{IN}



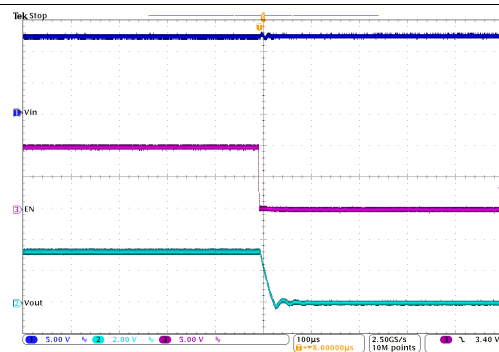
$I_{OUT} = 3$ A

27. Start-Up Relative to EN



$I_{OUT} = 0$ A

28. Shutdown Relative to V_{IN}



$I_{OUT} = 3$ A

29. Shutdown Relative to EN

9 Power Supply Recommendations

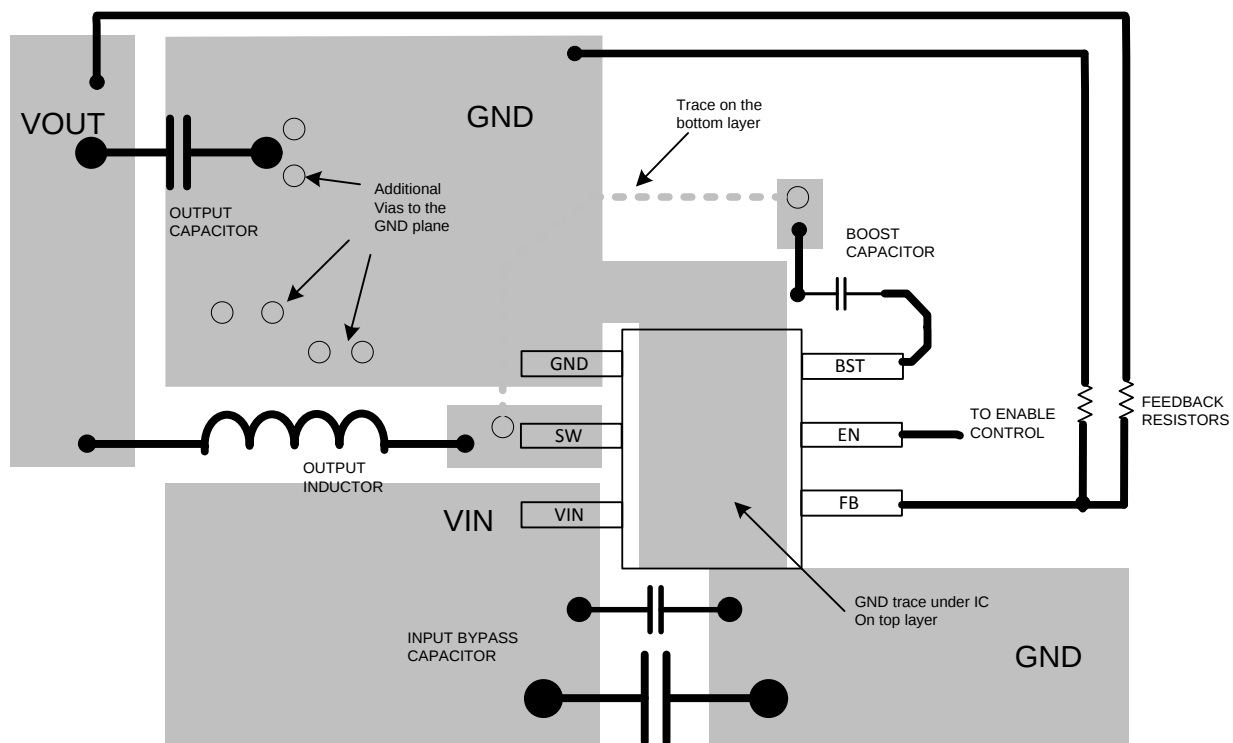
TPS563249 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not suggest routing SW copper under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example



✎ 30. Example Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.3 商標

D-CAP3, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS563249DDCR	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	Call TI Sn	Level-1-260C-UNLIM	-40 to 125	249
TPS563249DDCR.A	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	249
TPS563249DDCR.B	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	249
TPS563249DDCT	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	Call TI Sn	Level-1-260C-UNLIM	-40 to 125	249
TPS563249DDCT.A	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	249

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS563249DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563249DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS563249DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS563249DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0



SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



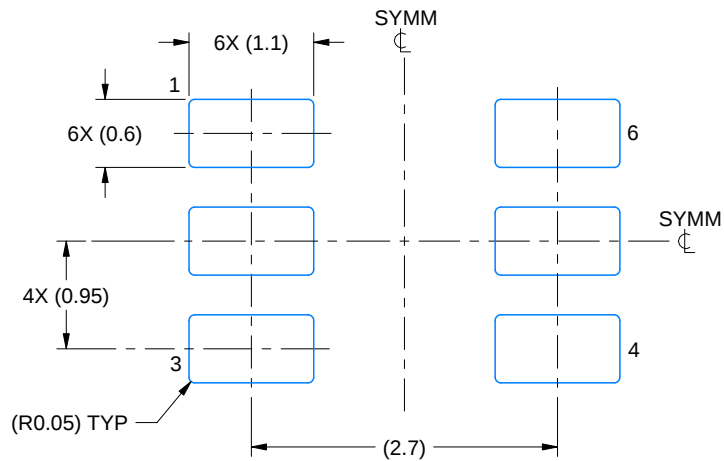
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

EXAMPLE BOARD LAYOUT

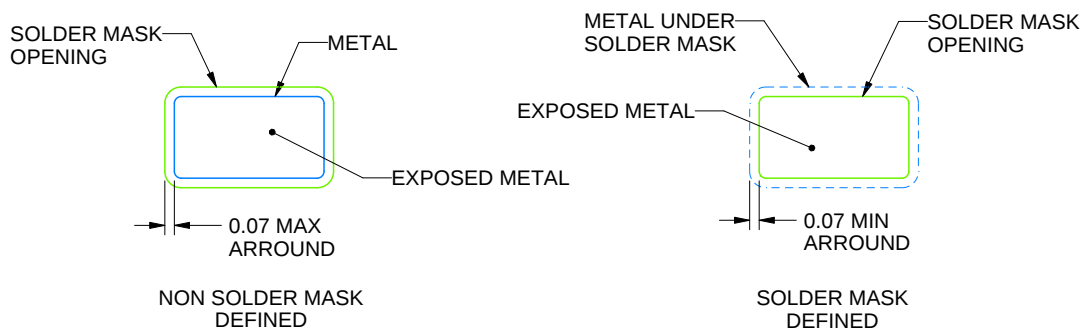
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

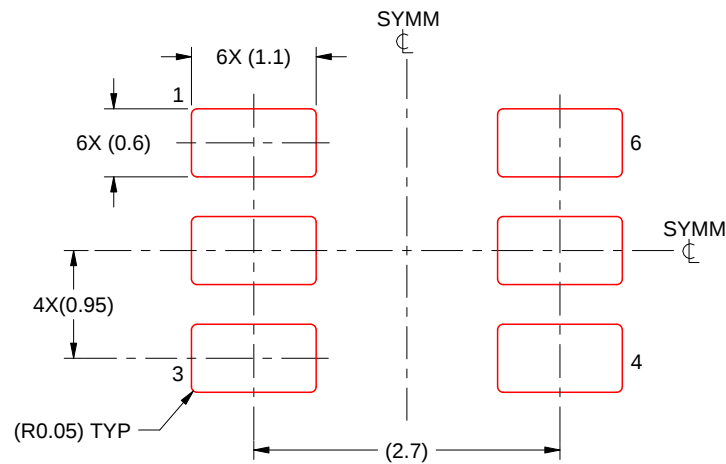
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated