



TPS563240 17V、3A、1.4MHz 同期整流降压レギュレータ

1 特長

- 70mΩ および 30mΩ の FET を内蔵した 3A コンバータで、過渡 3.5A をサポート
- D-CAP3™モード制御による高速過渡応答
- 入力電圧範囲: 4.5~17V
- 出力電圧範囲: 0.6V~7V
- パルス・スキップ・モードと Out-of-Audio™(OOA) 動作により、軽負荷動作時でも 25kHz を超える F_s
- 1.4MHz のスイッチング周波数
- 低いシャットダウン電流: 10μA 未満
- 帰還電圧精度: 1% (25°C)
- プリバイアス出力電圧からのスタートアップ
- サイクル単位の過電流制限
- ヒカップ・モードによる過電流保護
- 非ラッチ UVP および TSD 保護
- 固定ソフトスタート: 1.7ms

2 アプリケーション

- TV、セットトップ・ボックス
- ブロードバンド・モデム
- アクセス・ポイント・ネットワーク
- ワイヤレス・ルータ
- 監視機器

3 概要

TPS563240 は単純で使いやすい 3A 同期整流降压型レギュレータで、SOT-23 パッケージに搭載されています。3.5A までのピーク過渡出力電流に対応できます。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が小さくなるよう最適化されています。

このスイッチング・レギュレータは、D-CAP3 モード制御によって高速の過渡応答を実現します。また、特殊ポリマーなど ESR (等価直列抵抗) の低い出力コンデンサと、超低 ESR のセラミック・コンデンサの両方を、外付け補償部品なしでサポートします。

TPS563240 はパルス・スキップ・モードで動作し、軽負荷での動作時に高い効率を維持します。TPS563240 には Out-of-Audio™(OOA) 動作が実装されているため、軽負荷時でも 25kHz を超える F_{sw} を維持します。

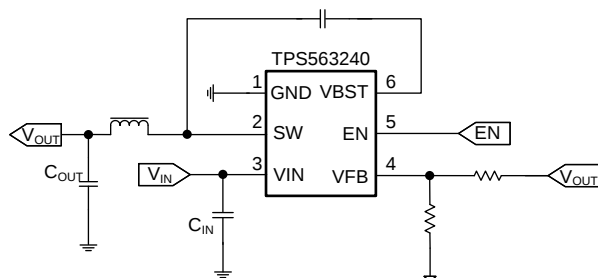
TPS563240 は 6 ピンの 1.6mm×2.9mm SOT (DDC) パッケージで供給され、接合部温度 -40°C~125°C で動作が規定されています。

製品情報⁽¹⁾

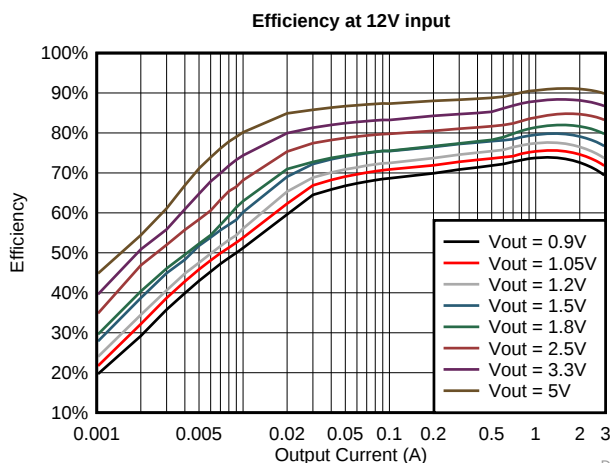
型番	パッケージ	本体サイズ(公称)
TPS563240	DDC (6)	1.60mm×2.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



TPS563240 の効率



D001



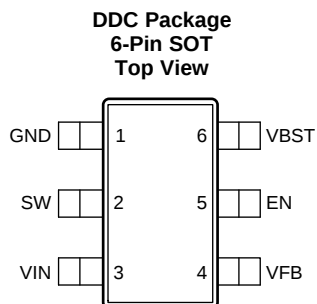
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4 改訂履歴

日付	リビジョン	注
2018年12月	*	初版

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 μ F capacitor between VBST and SW pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	V _{IN}	−0.3	19	V
	V _{BST}	−0.3	24.5	V
	V _{BST} (10 ns transient)	−0.3	26.5	V
	V _{BST} (vs SW)	−0.3	5.5	V
	V _{F_B}	−0.3	5.5	V
	SW	−2	19	V
	SW (10 ns transient)	−3.5	21	V
	EN	−0.3	V _{IN} + 0.3	V
Operating junction temperature, T _J		−40	150	°C
Storage temperature, T _{stg}		−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Supply input voltage range	4.5		17	V
EN	EN Input voltage range	−0.1		V _{IN}	V
T _J	Operating junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS563240	UNIT
		DDC (SOT)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	117.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	57.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	31.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	11.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	31.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

 $T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VIN}	Operating – non-switching supply current	V _{IN} current, EN = 5 V, V _{FB} = 0.7 V, T _J = 25°C		235	300	μA
I _{VIN(SDN)}	Shutdown supply current	V _{IN} current, EN = 0 V, T _J = 25°C		2.5	10	μA
LOGIC THRESHOLD						
V _{ENH}	Enable threshold	Rising		1.27	1.34	V
V _{ENL}	Enable threshold	Falling	1.08	1.15		V
R _{EN}	EN pin resistance to GND	V _{EN} = 1 V	800	1000	1200	kΩ
V _{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V _{FB}	FB voltage	Continuous mode operation, T _J = 25°C	594	600	606	mV
		Continuous mode operation	588	600	612	mV
I _{FB}	FB input current	V _{FB} = 0.7 V		0	±50	nA
MOSFET						
R _{DS(on)h}	High-side switch resistance	T _J = 25°C		70		mΩ
R _{DS(on)l}	Low-side switch resistance	T _J = 25°C		30		mΩ
CURRENT LIMIT						
I _{ocl_h_source}	High side FET source Current limit		5.5	6.3	7.1	A
I _{ocl_l_source}	Low side FET source Current limit		3.1	3.9	4.7	A
I _{ocl_l_sink}	Low side FET sink Current limit			0		A
THERMAL SHUTDOWN						
T _{SDN}	Thermal shutdown threshold ⁽¹⁾	Shutdown temperature		160		°C
		Hysteresis		25		
ON-TIME TIMER CONTROL						
t _{ON(MIN)}	Minimum on time ⁽¹⁾	V _{IN} = 12 V, load = 3 A		50		ns
t _{OFF(MIN)}	Minimum off time			250		ns
SOFT START						
t _{ss}	Soft-start time	Internal soft-start time		1.7		ms
FREQUENCY						
F _{sw}	Switching frequency			1400		kHz
OUTPUT UNDERVOLTAGE PROTECTION						
V _{UVP}	Output UVP threshold	Hiccup detect (H > L)		65%		
t _{UVPDLY}	UVP propagation delay			0.36		ms
t _{HIC}	UVP protection Hiccup Time before restart			25		ms
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage		4.2	4.4	V
		Shutdown VIN voltage	3.6	3.8		
		Hysteresis VIN voltage		0.4		

(1) Not production tested.

6.6 Typical Characteristics

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

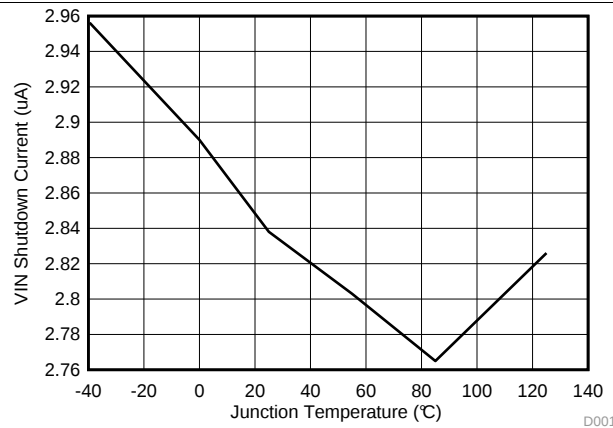


图 1. Shutdown Current vs Junction Temperature

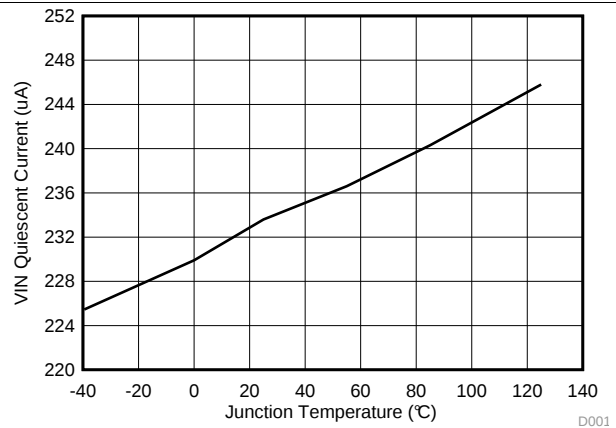


图 2. Supply Current vs Junction Temperature

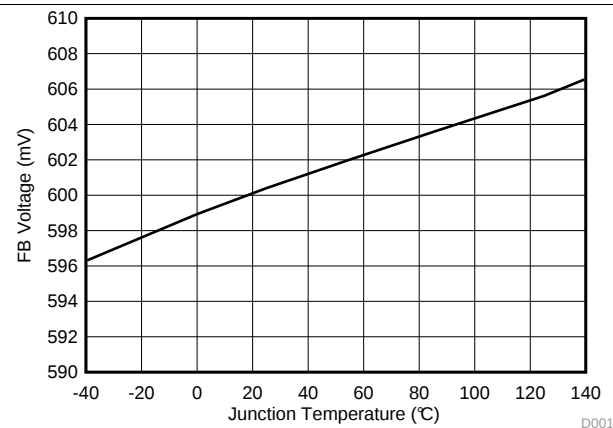


图 3. VFB Voltage vs Junction Temperature

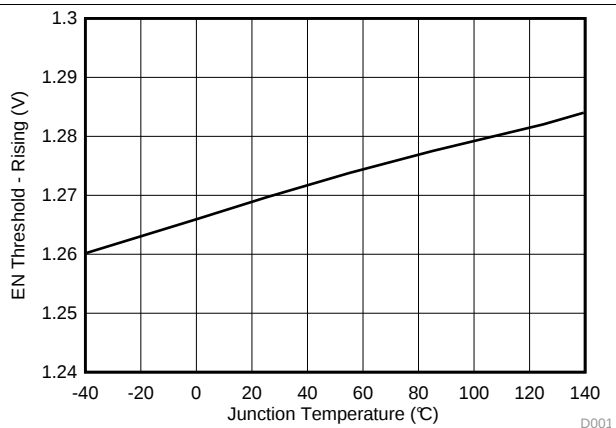


图 4. EN Rising threshold vs Junction Temperature

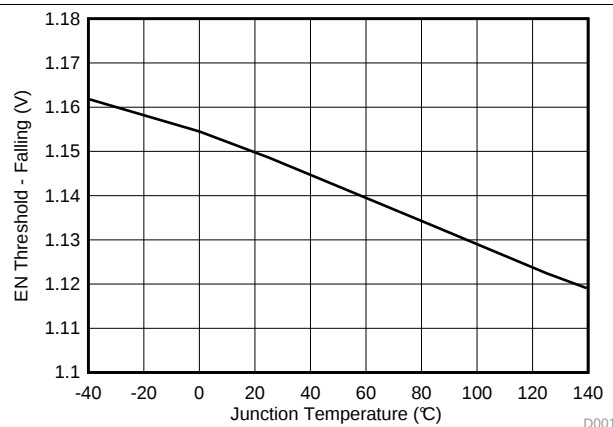


图 5. EN Falling threshold vs Junction Temperature

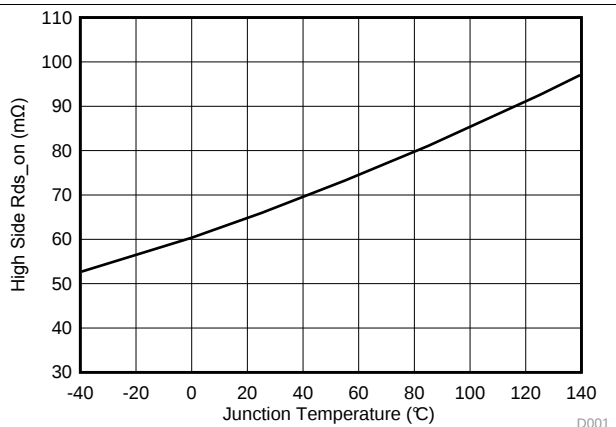


图 6. High-Side R_{ds-on} vs Junction Temperature

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

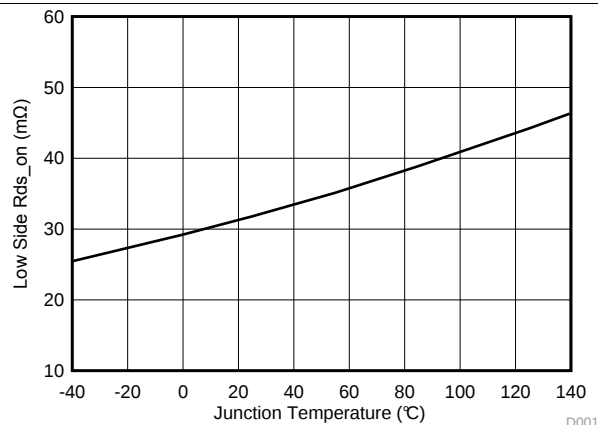


Figure 7. Low-Side R_{ds-On} vs Junction Temperature

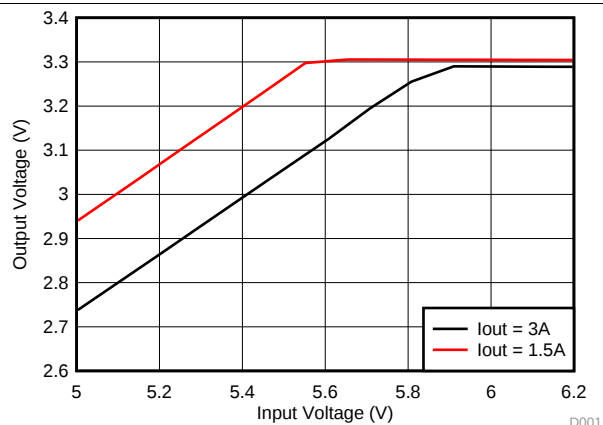


Figure 8. Dropout for 3.3 V Output Voltage

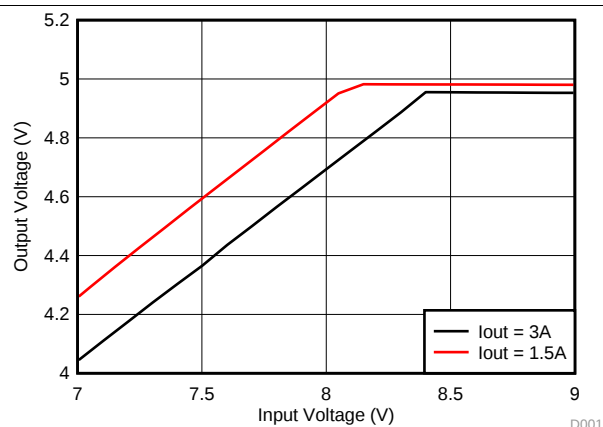


Figure 9. Dropout for 5 V Output Voltage

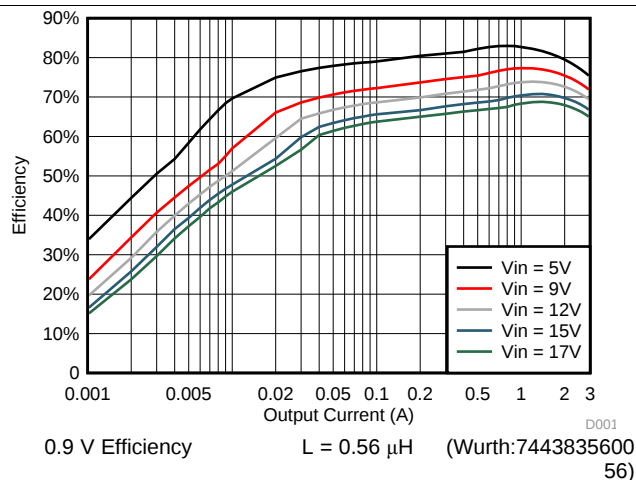


Figure 10. Efficiency vs Output Current, $V_{OUT} = 0.9\text{ V}$

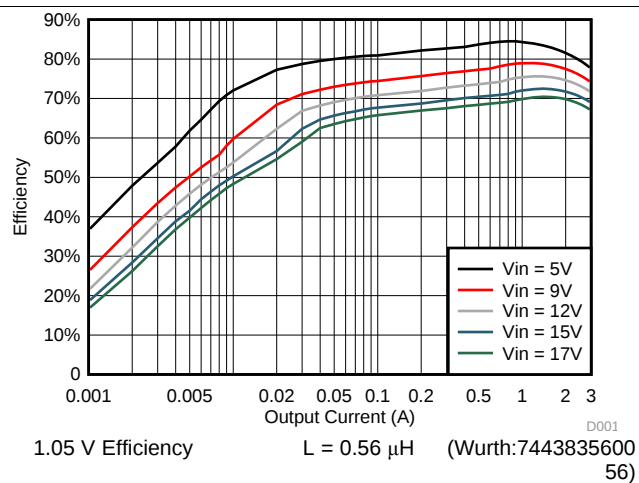


Figure 11. Efficiency vs Output Current, $V_{OUT} = 1.05\text{ V}$

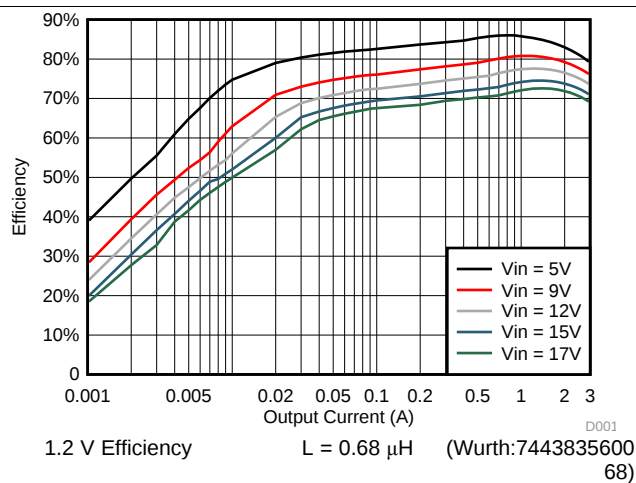
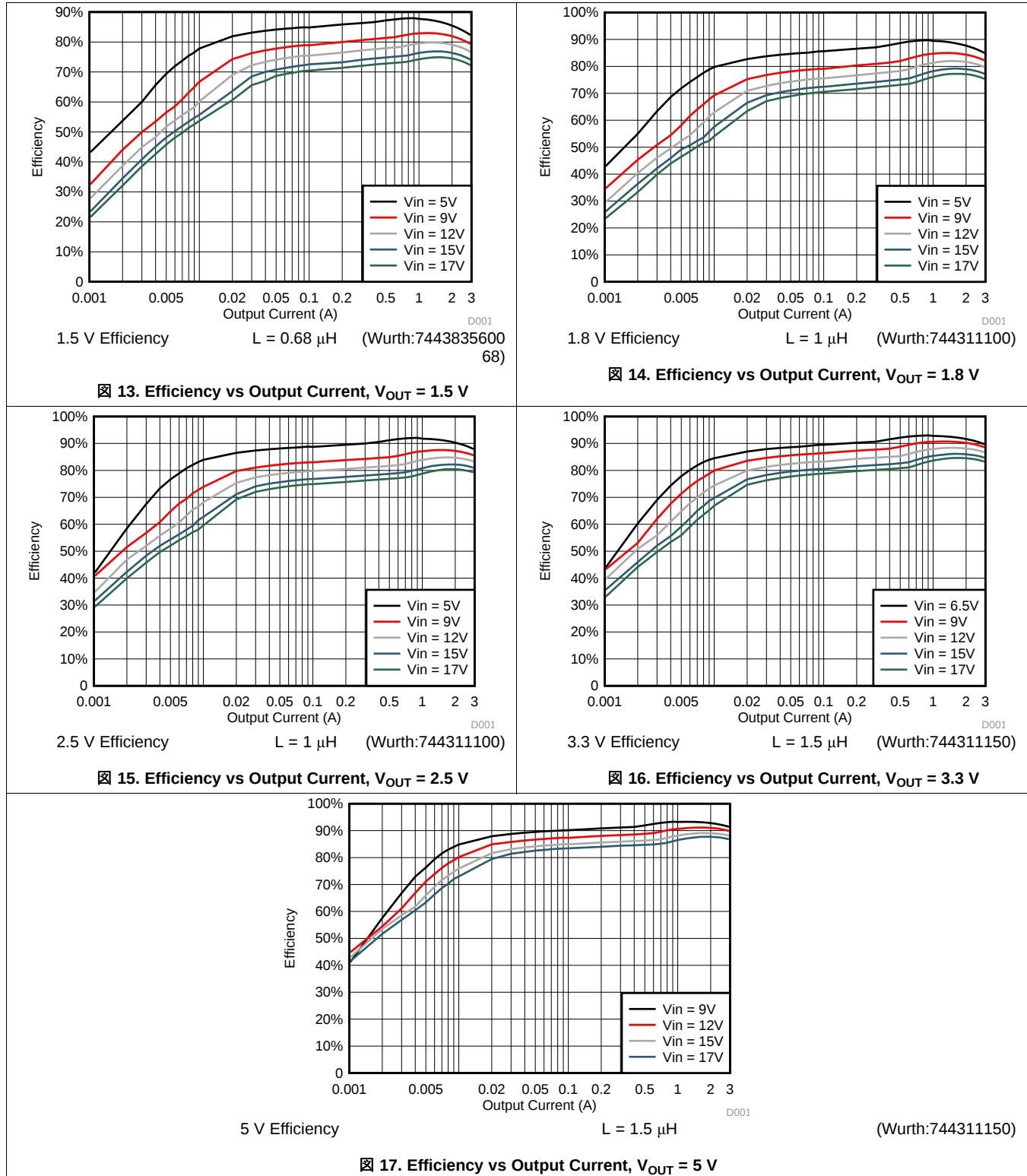


Figure 12. Efficiency vs Output Current, $V_{OUT} = 1.2\text{ V}$

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

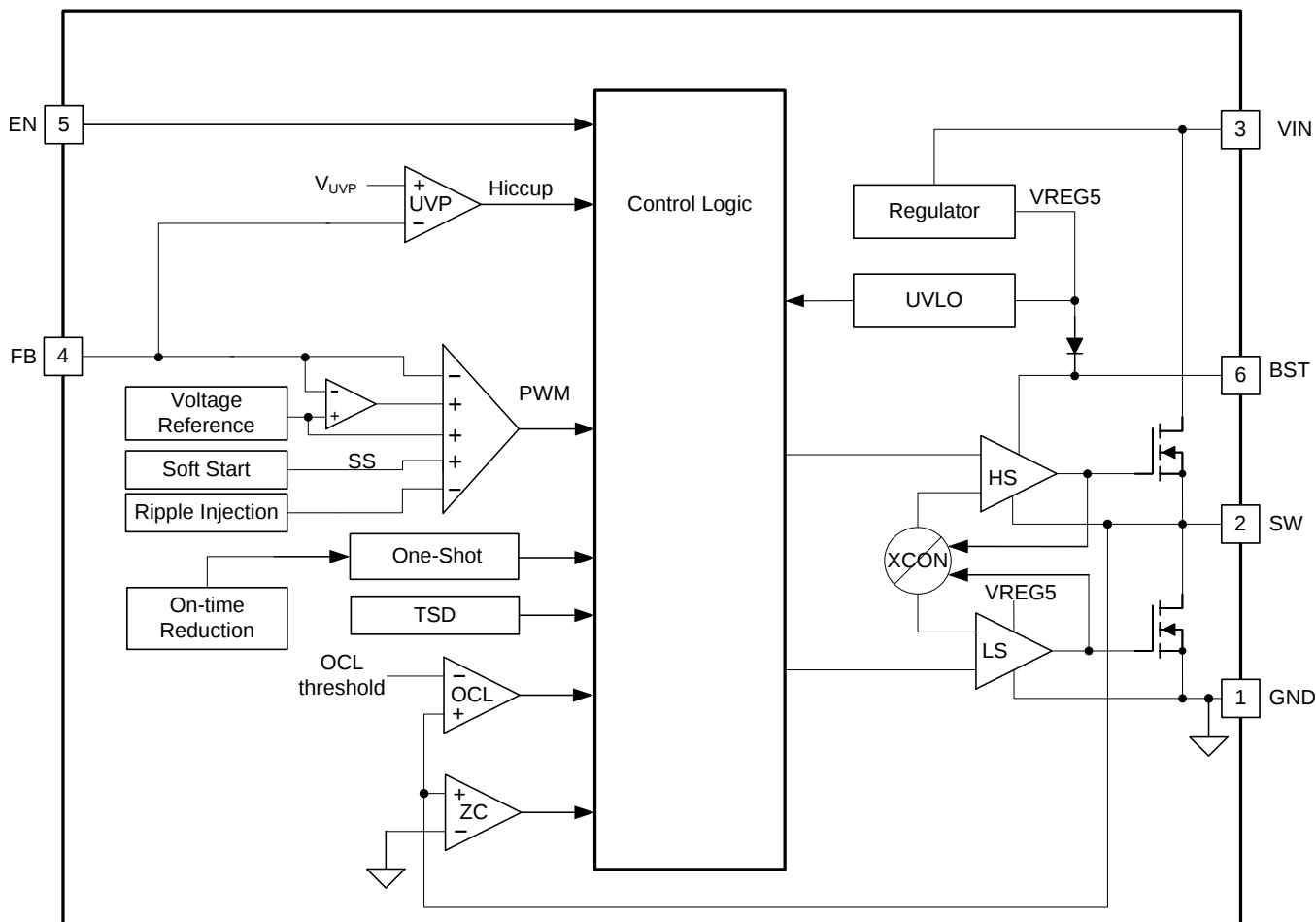


7 Detailed Description

7.1 Overview

The TPS563240 is a 3-A synchronous step-down converter. The proprietary D-CAP3 mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP3 mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS563240 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 mode control. The D-CAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, V_{IN} , and inversely proportional to the output voltage, V_O , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP3 mode control.

Feature Description (continued)

7.3.2 Pulse Skip Control

The TPS563240 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in 式 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Out-of-Audio™ (OOA) Operation

As the load current continues to decrease, the switching frequency can decrease into the acoustic audible frequency range. To prevent this from happening, Out-of-Audio™ (OOA) operation under light-load condition is implemented. The OOA control circuit monitors the states of both the high-side and low-side FETs. When both high-side and low-side FETs are off for a period longer than 30 μ s, the on time generated by one shot timer is decreased by a little step, thus the off time of both FETs will be reduced to a length lower than 30 μ s. If the load current decreases further, and cause the off time of both FETs longer than 30 μ s again, the above described on time reduction process will repeat. By this means, the switching frequency is maintained higher than ~33kHz as load decrease. When the on time reduces to ~30% of that in CCM operation, the on time will keep at this minimum length. If load current decreases further, the switching frequency can't be maintained at ~33kHz anymore, instead, it will decrease linearly towards zero.

When the load current increases from zero, the on time is kept at minimum length, which is ~30% of that in CCM operation, and the switching frequency increases linearly as load increases. When the off time of both FETs decreases to a length lower than 20 μ s, the on time generated by one shot timer will increase by a step, thus the off time of both FETs will be increased above 20 μ s. If the load current increases further, and cause the off time of both FETs shorter than 20 μ s again, the above described on time increase process will repeat. By this means, the switching frequency is maintained lower than ~50kHz as load increases. When the on time increases to the length of that in CCM operation, the on time can't be increased anymore. If load current continue increases, the switching frequency will increase linearly towards 1.4MHz nominal frequency. Below figure shows the frequency VS load curve at 12Vin/5Vout condition with 1.5 μ H inductor used.

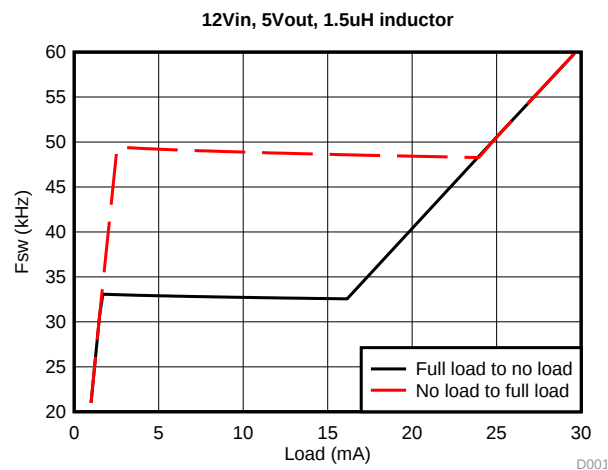


图 18. Frequency VS load current at 12Vin/5Vout condition with 1.5 μ H inductor used

Feature Description (continued)

7.3.4 Soft Start and Pre-Biased Soft Start

The TPS563240 has an internal 1.7-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB} . This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.5 Current Protection

There are two kinds of current protection in TPS563240: High-side FET source current limit and low-side FET source current limit.

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the low-side FET switch, the inductor current flow through low-side FET and decreases linearly. The average value of the inductor current is the load current I_{OUT} . If the monitored current is above the low-side FET source current limit level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current cross the low-side FET source current limit level. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the V_{FB} voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 0.36 ms) and re-start after the hiccup time (typically 25 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

During the on time of the high-side FET switch, the inductor current flow through high-side FET and increases at a linear rate determined by V_{IN} , V_{OUT} , the on-time and the output inductor value. The switch current is compared with high-side FET source current limit after a short blanking time. If the cross-limit event detected before the one shot timer expires, the high-side FET will be turn off immediately, and will not be allowed on in the following 1 μ s period.

7.3.6 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.7 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 160°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS563240 can operate in normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS563240 operates at a quasi-fixed frequency of 1.4MHz.

Device Functional Modes (continued)

7.4.2 Eco-mode Operation

When the TPS563240 is in the normal CCM operating mode and the switch current falls to 0 A, the TPS563240 begins operating in pulse skipping Eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below reference voltage. As the output current decreases, the sleep time between switching pulses increases.

7.4.3 Standby Operation

When the TPS563240 is operating in either normal CCM or Eco-mode, it may be placed in standby by asserting the EN pin low.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical step-down DC-DC converter. It's typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the TPS563240. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in [Figure 19](#) was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

[Figure 19](#) shows the TPS563240 6.5-V to 17-V input, 3.3-V output converter schematics.

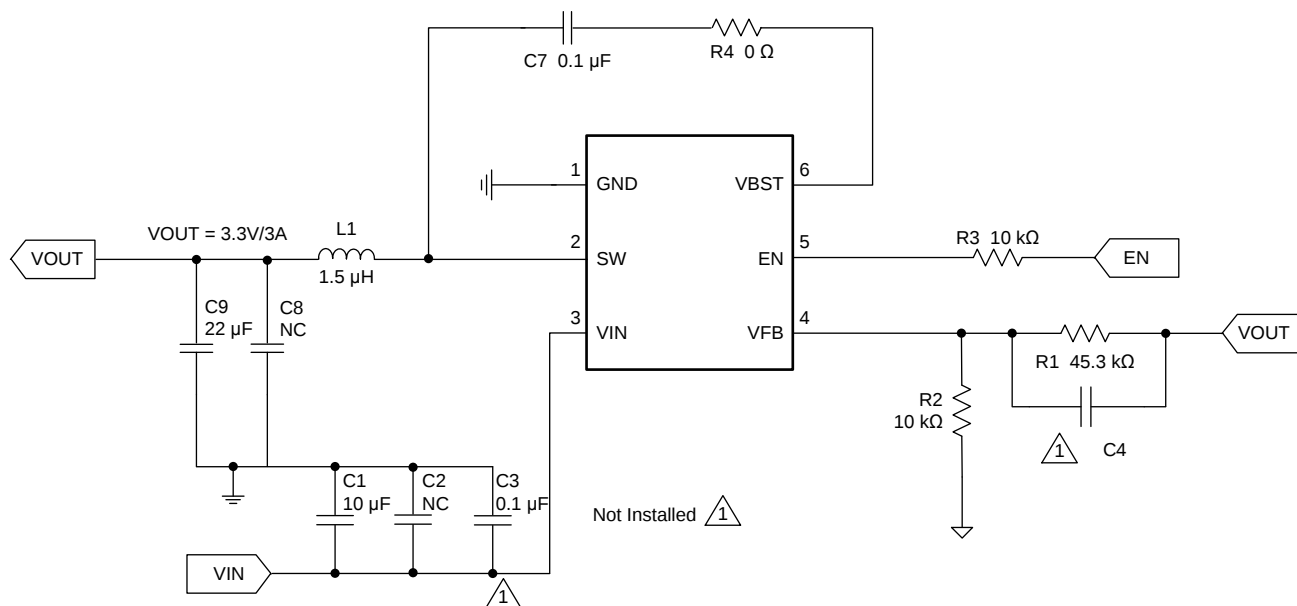


Figure 19. 3.3-V/3-A Reference Design

Typical Application (continued)

8.2.1 Design Requirements

表 1 shows the design parameters for this application.

表 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	6.5 to 17 V
Output voltage	3.3 V
Transient response, 1.5-A load step	$\Delta V_{out} = \pm 5\%$
Input ripple voltage	400 mV
Output ripple voltage	100 mV
Output current rating	3 A
Operating frequency	1.4 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 式 2 to calculate V_{OUT} .

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP3 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 2.

表 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)			C8 + C9 (μF)
			MIN	TYP	MAX	
1	6.65	10.0	0.33	0.56	1	10 to 44
1.05	7.5	10.0	0.33	0.56	1	10 to 44
1.2	10	10.0	0.47	0.68	1.5	10 to 44
1.5	15	10.0	0.47	0.82	1.5	10 to 44
1.8	20	10.0	0.56	1	2.2	10 to 44
2.5	31.6	10.0	0.68	1	2.2	10 to 44
3.3	45.3	10.0	0.82	1.5	3.3	10 to 44
5	73.2	10.0	1	1.5	3.3	10 to 44
6.5	97.6	10.0	1	1.5	3.3	10 to 44

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 4, 式 5, and 式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 3.63 A and the calculated RMS current is 3.02 A. The inductor used is a WE 744311150 with a rated current of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563240 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 10 µF to 44 µF. Use 式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design one Murata GRM31CR61A226KE19 22-µF output capacitor is used. The typical ESR is 2 mΩ. The calculated RMS current is 0.365 A and output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS563240 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.2.5 Dropout

With a constant 1.4-MHz switching frequency, there is a minimum input voltage limit for a given output voltage to be regulated. This is due to the minimum off time limit. If the input voltage less than the minimum input voltage limit, the output voltage drops accordingly, which is called dropout condition. 图 8 and 图 9 show the typical dropout curve for 3.3 V and 5 V output voltage with 3 A and 1.5 A load respectively. 式 8 can be used to estimate this minimum input voltage limit.

$$V_{IN(MIN)} = \frac{\frac{V_{OUT}}{F_{SW}} + (R_{dsl} + R_L) \times I_O \times (t_{off(min)} - t_{d1} - t_{d2}) + (V_d + R_L \times I_O) \times (t_{d1} + t_{d2})}{\frac{1}{F_{SW}} - t_{off(min)}} + (R_{dsh} + R_L) \times I_O$$

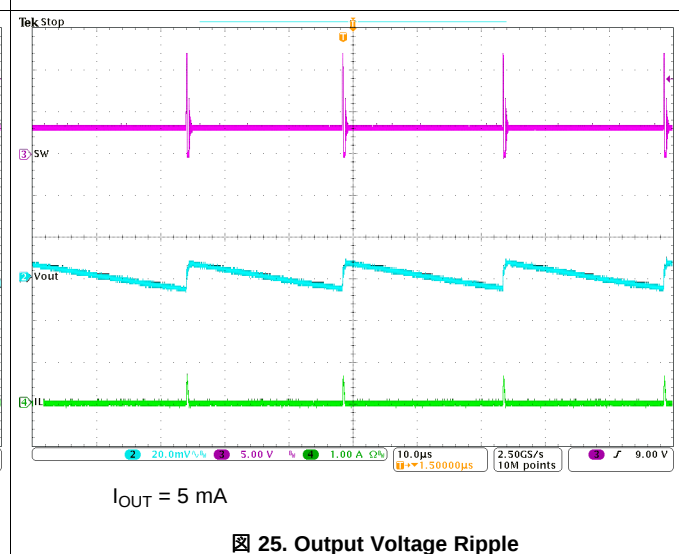
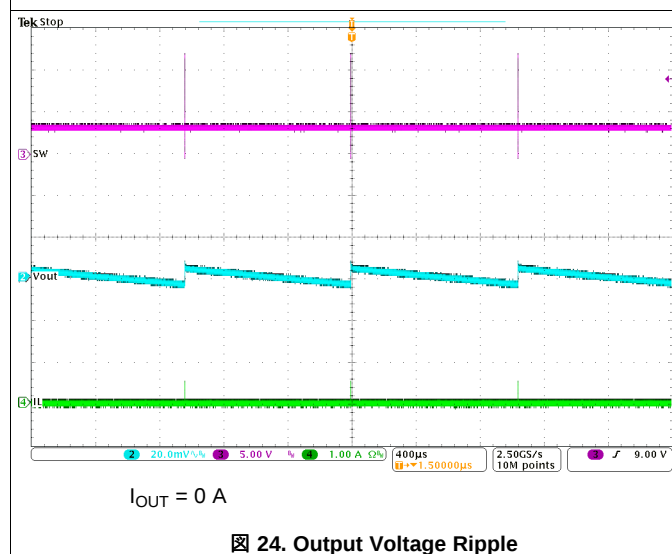
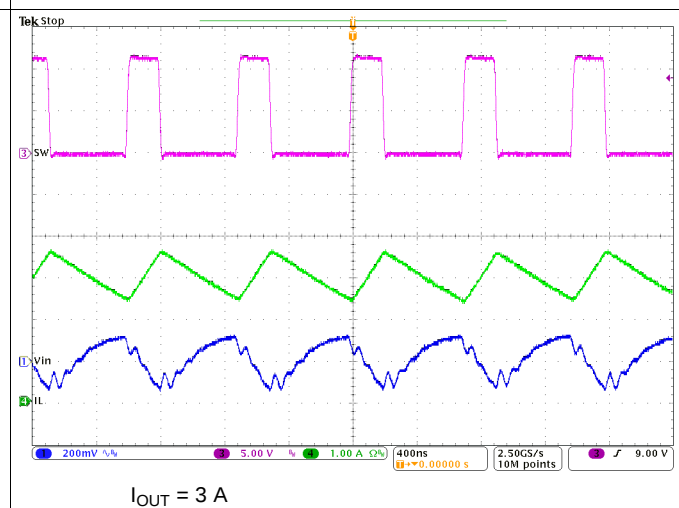
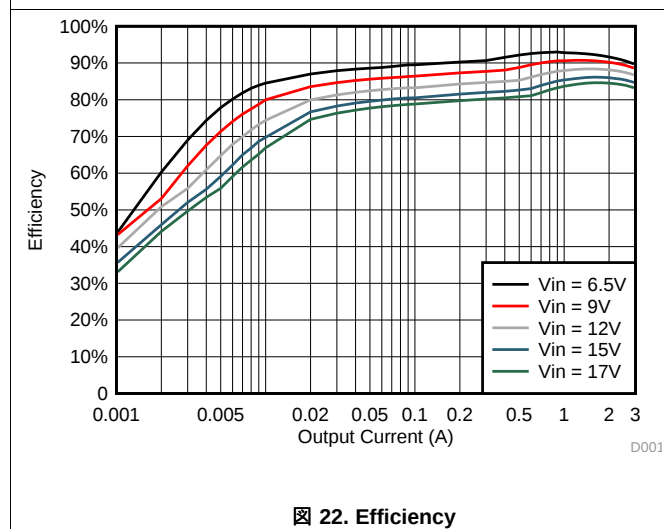
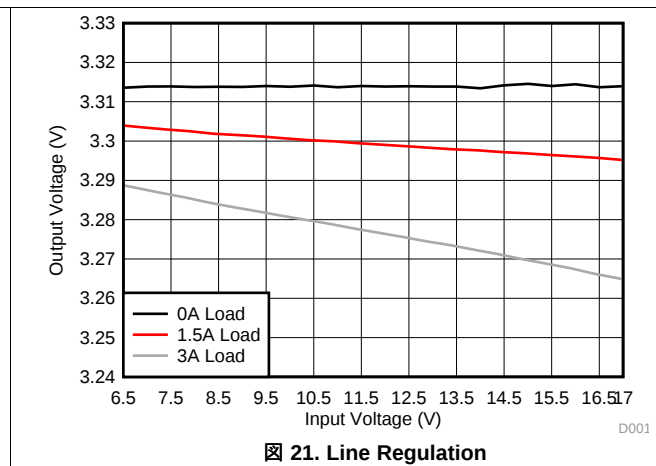
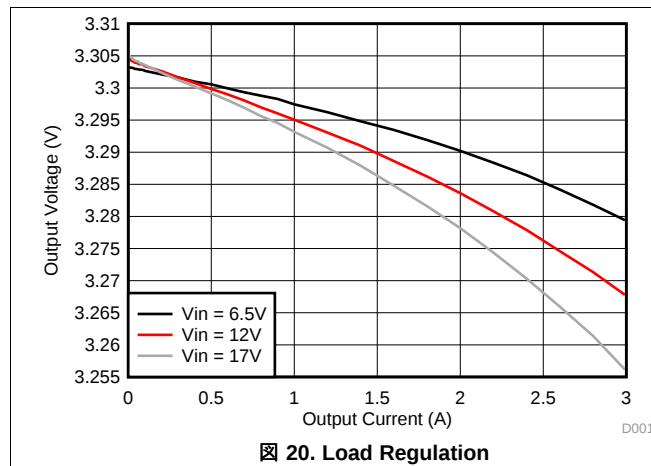
where

- V_{OUT} = target output voltage
- F_{SW} = maximum switching frequency including tolerance
- $t_{off(min)}$ = minimum off time including tolerance
- R_{dsl} = low side FET on resistance
- R_{dsh} = high side FET on resistance
- R_L = inductor DC resistance
- I_O = maximum load current
- t_{d1} = dead time between high side FET off and low side FET on, 15nS typical
- t_{d2} = dead time between low side FET off and high side FET on, 10nS typical
- V_d = forward voltage of low side FET body diode

(8)

8.2.3 Application Curves

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{ V}$ (unless otherwise noted)



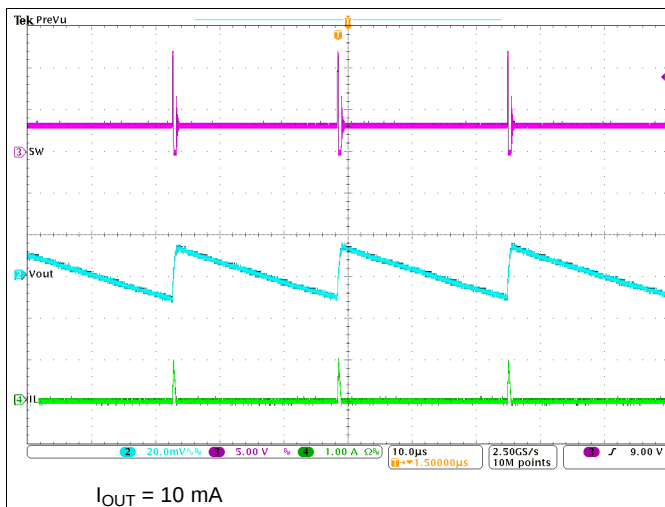


図 26. Output Voltage Ripple

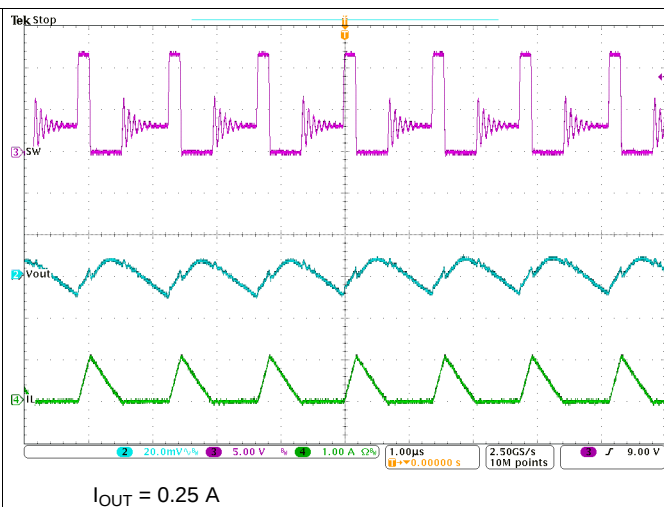


図 27. Output Voltage Ripple

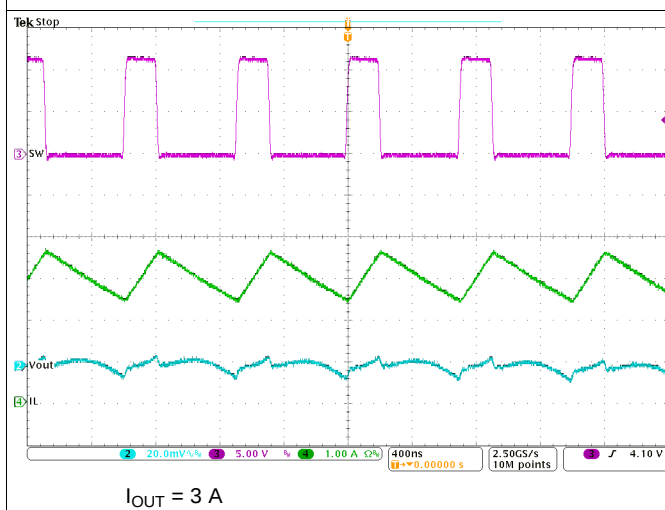


図 28. Output Voltage Ripple

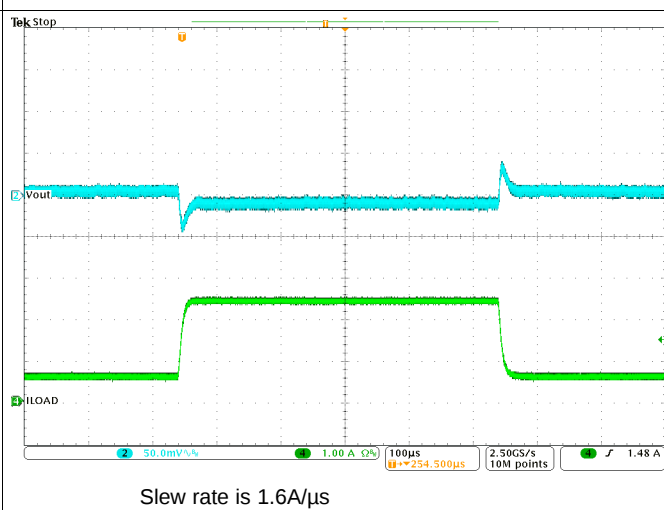


図 29. Transient Response, 0.6 to 2.4A

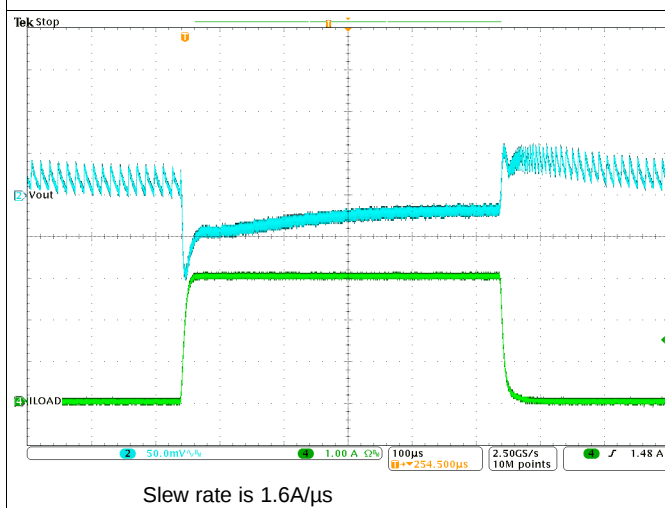


図 30. Transient Response, 0 to 3 A

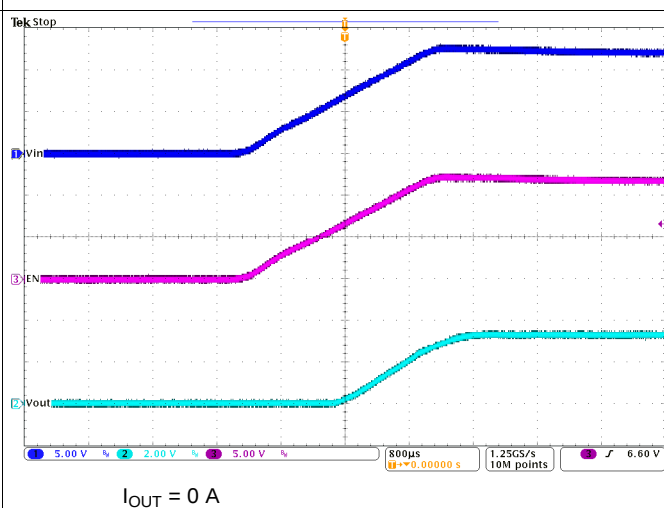
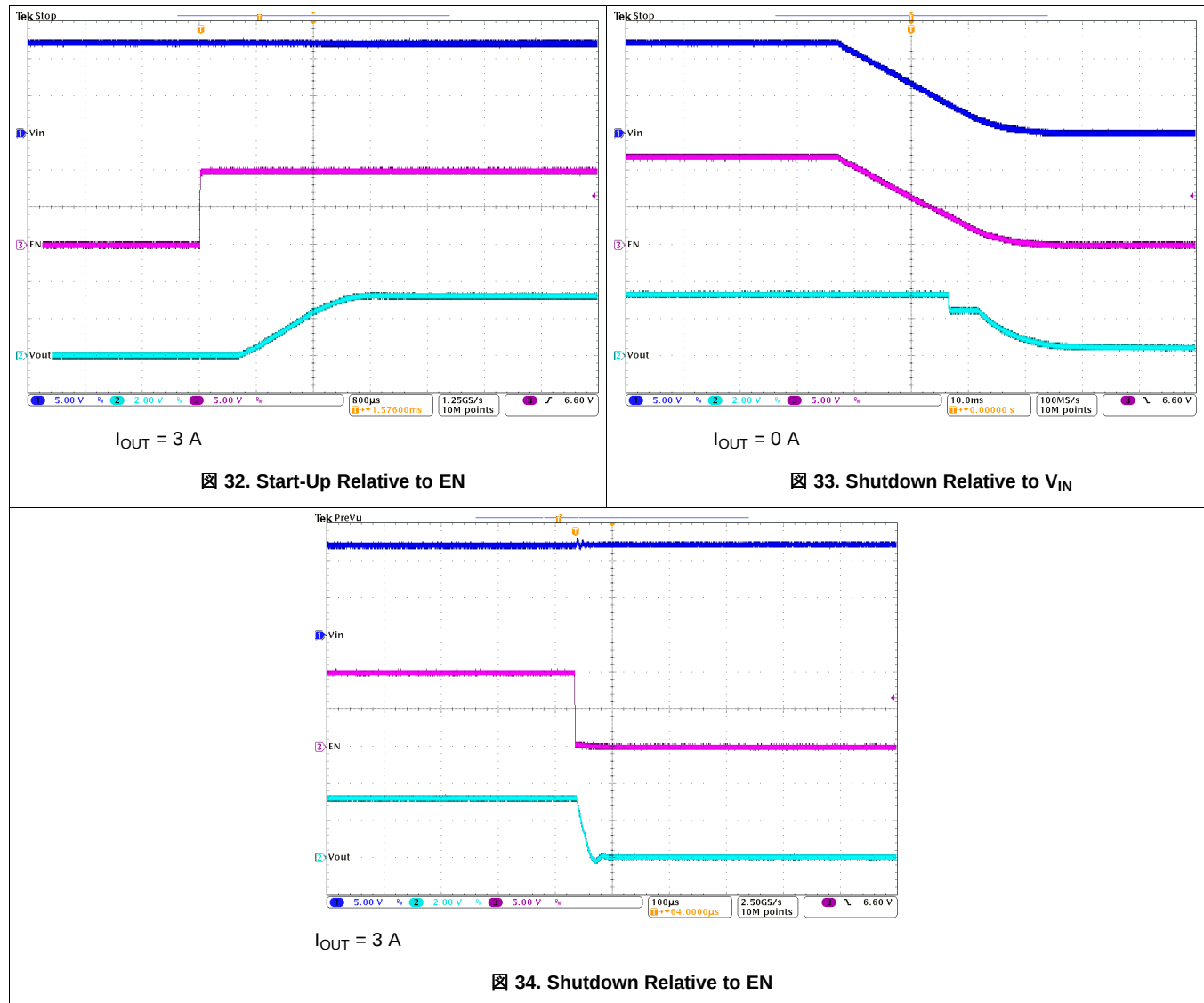


図 31. Start Up Relative to V_{IN}



9 Power Supply Recommendations

TPS563240 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not suggest routing SW copper under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

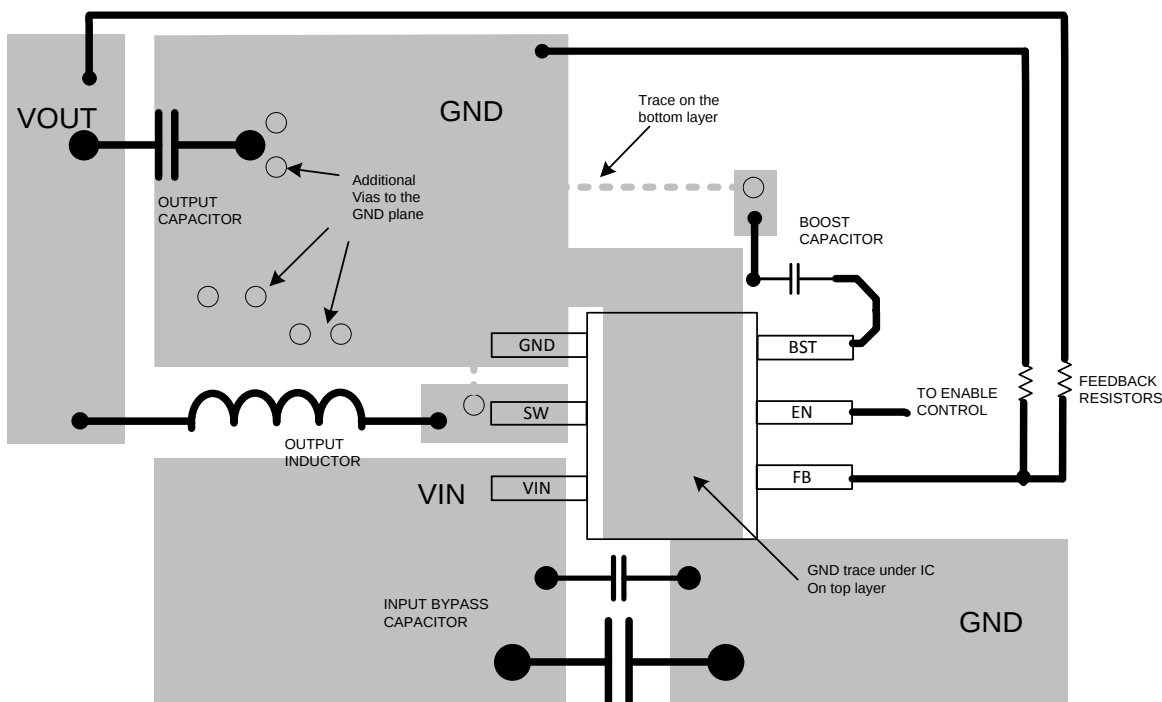


图 35. Example Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

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11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS563240DDCR	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3240
TPS563240DDCR.A	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3240
TPS563240DDCT	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3240
TPS563240DDCT.A	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3240

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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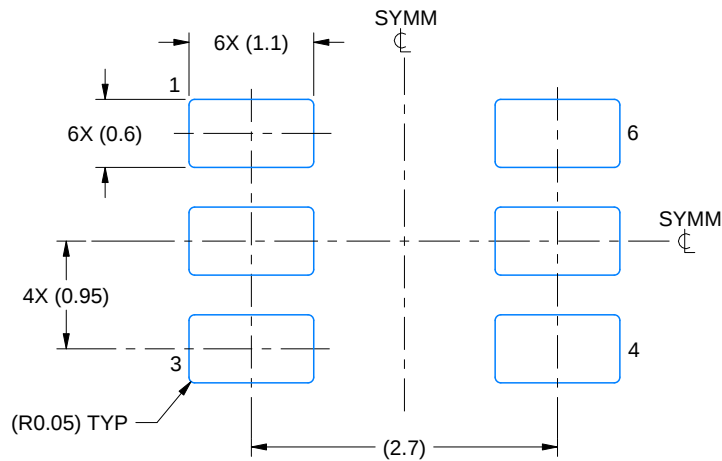


SOT-23 - 1.1 max height

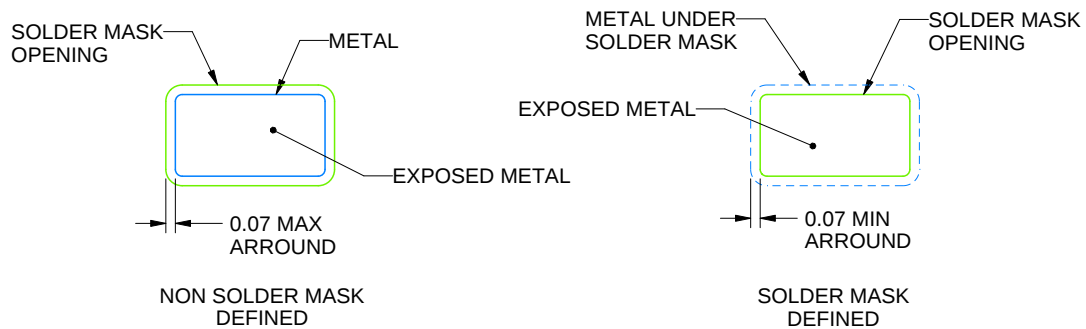
SMALL OUTLINE TRANSISTOR



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X

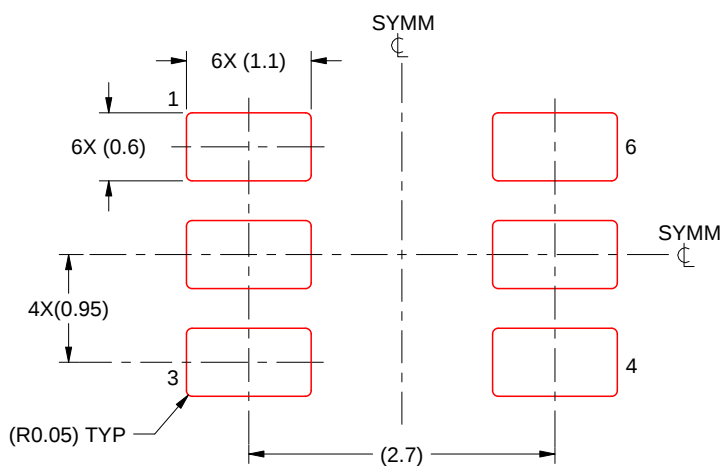


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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