TPS563231 SOT563パッケージ、4.5V～17V入力、3Aの同期整流降圧型電圧レギュレータ

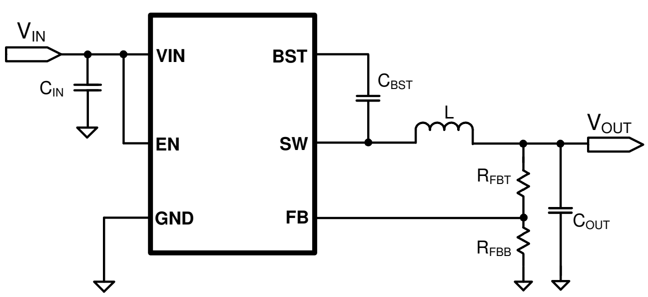
1 特長

- 95mΩ および 55mΩ の FET 内蔵の 3A コンバータ
- D-CAP3™モード制御による高速過渡応答
- 入力電圧範囲: 4.5～17V
- 出力電圧範囲: 0.6V～7V
- パルス・スキップ・モード
- 600kHz のスイッチング周波数
- 低いシャットダウン電流： 12µA 未満
- 帰還電圧精度: 2% (25°C)
- プリバイアス出力電圧からのスタートアップ
- サイクル単位の過電流制限
- ヒカップ・モードによる過電流保護
- 非ラッチ UVP および TSD 保護
- 6 ピン SOT563 パッケージ

2 アプリケーション

- デジタル・テレビ用電源
- 高解像度 Blu-ray™ディスク・プレーヤー
- ネットワーク・ホーム・ターミナル
- デジタル・セットトップ・ボックス (STB)
- 監視機器

概略回路図



3 概要

TPS563231 は単純で使いやすい 3A 同期整流降圧型コンバータで、SOT563 パッケージに搭載されています。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が低くなるよう最適化されています。

これらのスイッチ・モード電源(SMPS)デバイスは、D-CAP3モード制御を採用し、高速の過渡応答を実現します。また、特殊ポリマーなどESR (等価直列抵抗)の低い出力コンデンサと、超低ESRのセラミック・コンデンサの両方を、外部補償部品なしでサポートします。

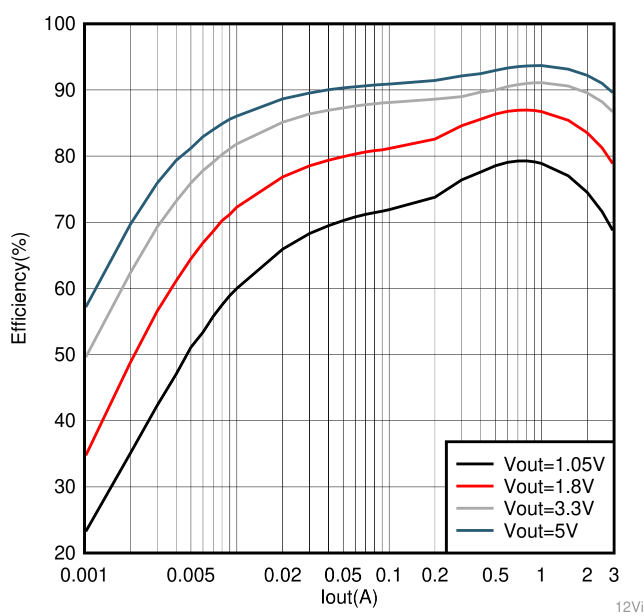
TPS563231は軽負荷動作時にパルス・スキップ・モード(PSM)で動作し、高い効率を維持します。TPS563231は6ピン、1.6mm×1.6mmのSOT563 (DRL)パッケージで供給され、接合部温度-40°C～125°Cで動作が規定されています。

製品情報[1]

型番	パッケージ	本体サイズ(公称)
TPS563231	DRL (6)	1.60mm×1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

TPS563231の効率



English Data Sheet: SLUSD65

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4 改訂履歴

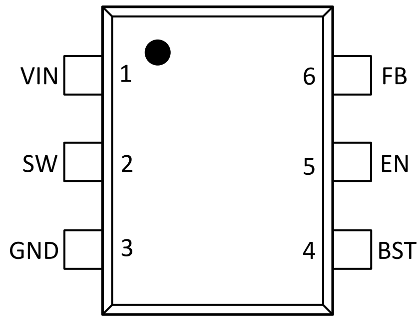
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (January 2019) から **Revision B** に変更	**Page**
• Changed FB I/O Version from 'O' to 'I'	5
• 変更 Function Block Diagram Pin number	10

2018年**7**月発行のものから更新	**Page**
• マーケティング・ステータスを「事前情報」から「最終版」に 変更	1

5 Pin Configuration and Functions

DRL Package
6-Pin SOT563
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	4	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between BST and SW pins.
EN	5	I	Enable input control. High = On, Low = Off. Can be connected to VIN. Do not float. Adjust the input undervoltage lockout with EN resistor divider.
FB	6	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
GND	3	—	Power ground terminals, connected to the source of low-side FET internally. Connect to system ground, ground side of C_{IN} and C_{OUT}. Path to C_{IN} must as short as possible.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	1	I	Input voltage supply pin. The drain terminal of high-side power NFET.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	19	V
	BST	–0.3	24.5	V
	BST (10 ns transient)	–0.3	26.5	V
	BST to SW	–0.3	5.5	V
	FB	–0.3	5.5	V
	EN	–0.3	VIN + 0.3	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	4.5	17	V
	BST	–0.1	22	V
	BST to SW	–0.1	5	
	EN	–0.1	VIN	
	FB	–0.1	4.5	
	SW	–1.8	17	
Operating junction temperature	T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS56323x DRL 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	135.8	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	45.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	23.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
I_{VIN}	Operating – non-switching supply current	V_{EN} = 5 V, V_{FB} = 0.7 V		220	300	µA
I_{VINSDN}	Shutdown supply current	V_{EN} = 0 V		2	12	µA
V_{IN_UVLO}	Undervoltage lockout thresholds	Rising threshold		4.0	4.3	V
		Falling threshold	3.3	3.6		V
		Hysteresis		0.4		V
ENABLE (EN PIN)						
V_{ENH}	EN high-level input voltage		1.10	1.24	1.42	V
V_{ENL}	EN low-level input voltage		1.00	1.13	1.30	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		1000		kΩ
VOLTAGE REFERENCE (FB PIN)						
V_{REF}	Reference voltage	V_{IN} = 4.5 V to 17 V, T_J = 25 °C	588	600	612	mV
		V_{IN} = 4.5 V to 17 V, T_J = –40°C to 125°C		600		mV
I_{FB}	V_{FB} input current	V_{FB} = 0.6 V		0	±100	nA
MOSFET						
R_{DSON_H}	High-side switch resistance	T_J = 25°C, V_{BST} – V_{SW} = 5V		95		mΩ
R_{DSON_L}	Low-side switch resistance	T_J = 25°C		55		mΩ
CURRENT LIMIT						
I_{OC_LS}	Low side FET source current limit		3	3.9	4.8	A
I_{ZC}	Zero cross current detection			0		A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature		160		°C
		Hysteresis		25		°C
ON-TIME TIMER CONTROL						
$t_{ON(MIN)}$	Minimum on time(1)			80		ns
$t_{OFF(MIN)}$	Minimum off time(1)	V_{FB} = 0.5 V		250		ns
SOFT START						
Tss	Soft-start time	Internal soft-start time		1.5		ms
FREQUENCY						
F_{sw}	Switching frequency	V_{IN} = 12 V, V_{OUT} = 3.3 V, CCM mode		600		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{UVP}	Output UVP falling threshold	Hiccup detect		65		%
T_{HICCUP_WAIT}	UVP propagation delay			0.8		ms
T_{HICCUP_RE}	Hiccup time before restart			24		ms

(1) Not production tested.

6.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

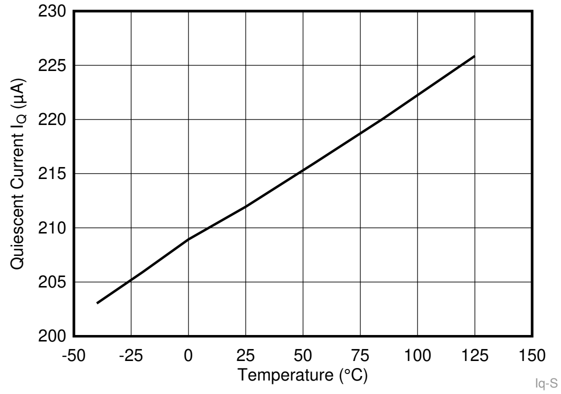


図 1. I_Q vs Junction Temperature

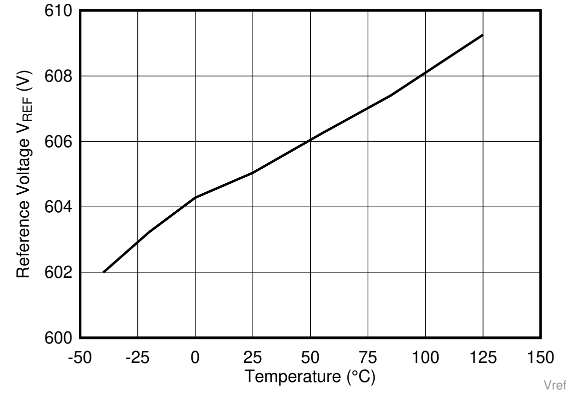


図 2. V_{REF} Voltage vs Junction Temperature

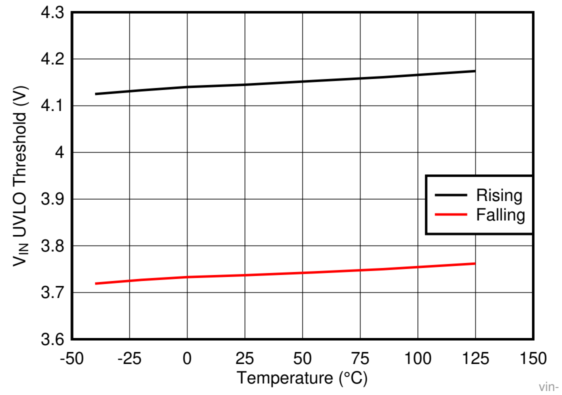


図 3. V_{IN} UVLO vs Junction Temperature

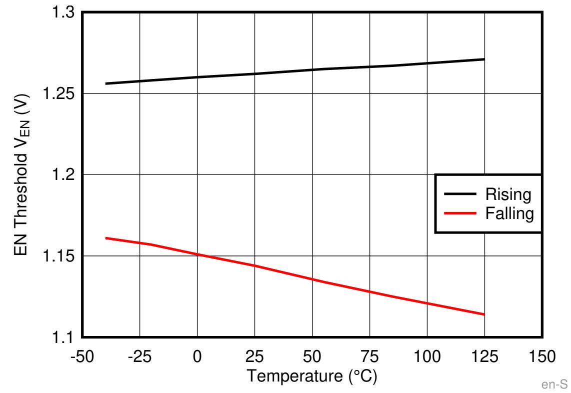


図 4. EN Pin UVLO vs Junction Temperature

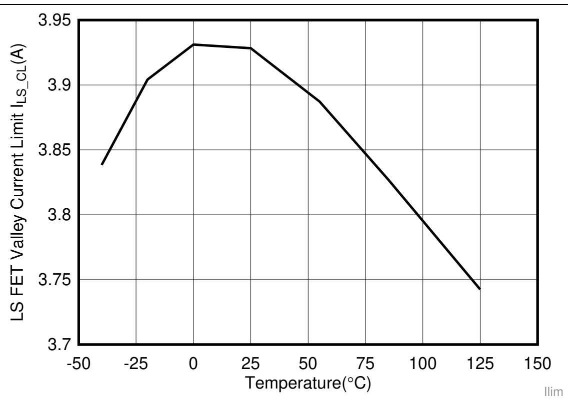


図 5. Current Limit vs Junction Temperature

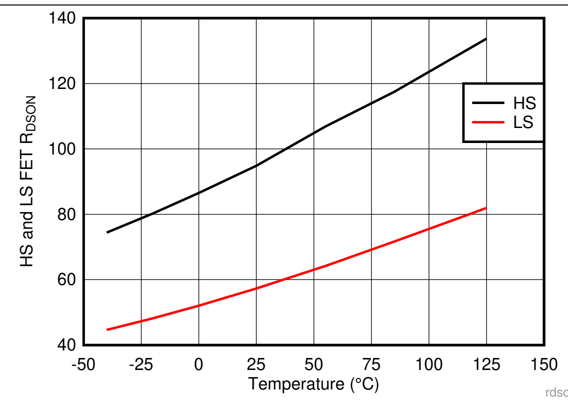


図 6. $R_{DS\text{-}ON}$ vs Junction Temperature

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

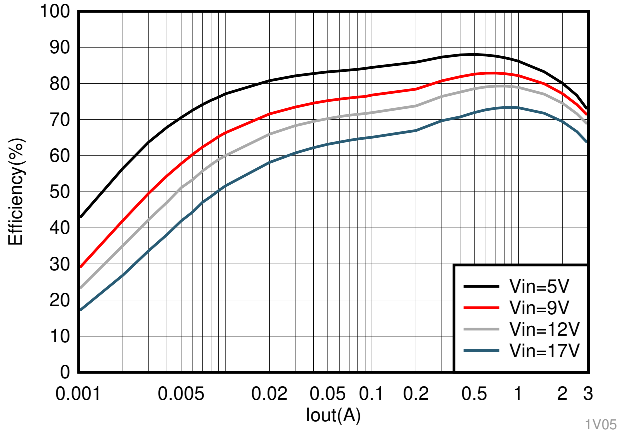


図 7. TPS563231 V_{OUT} = 1.05 V Efficiency

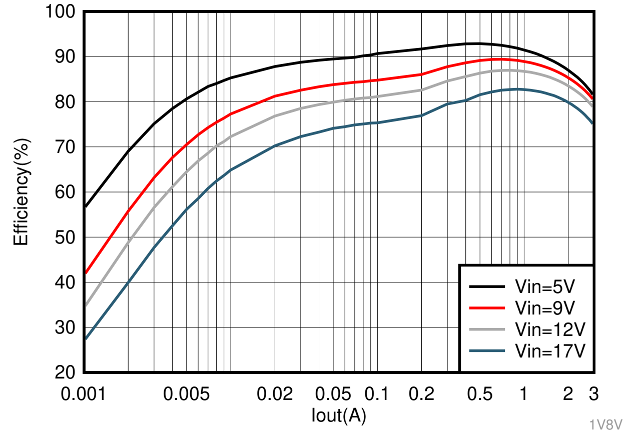


図 8. TPS563231 V_{OUT} = 1.8 V Efficiency

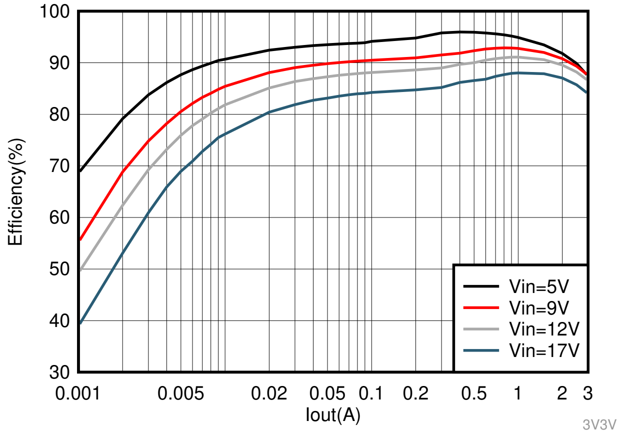


図 9. TPS563231 V_{OUT} = 3.3 V Efficiency

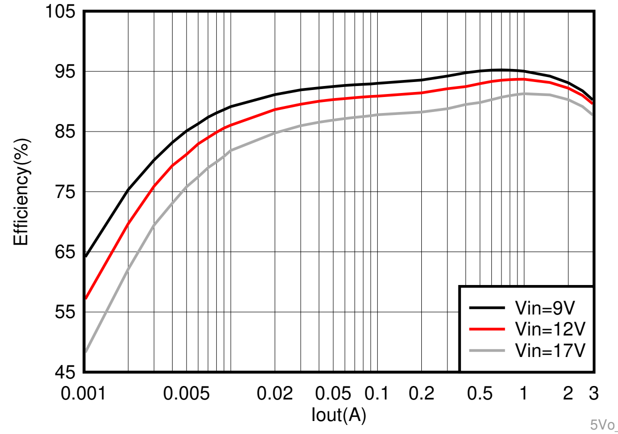


図 10. TPS563231 V_{OUT} = 5 V Efficiency

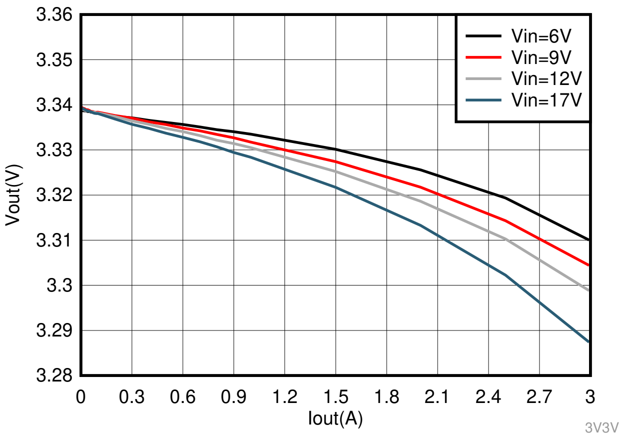


図 11. TPS563231 V_{OUT} = 3.3V Load Regulation

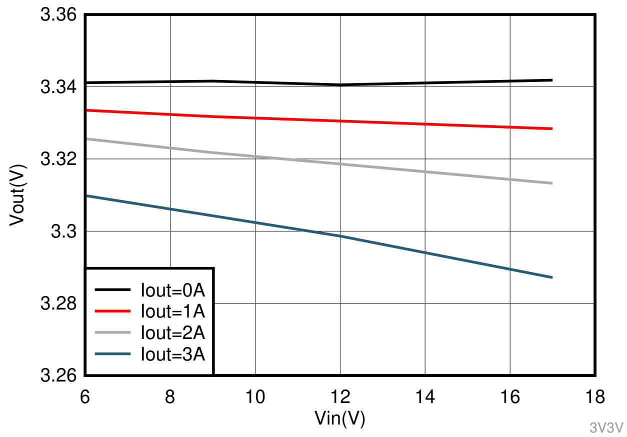


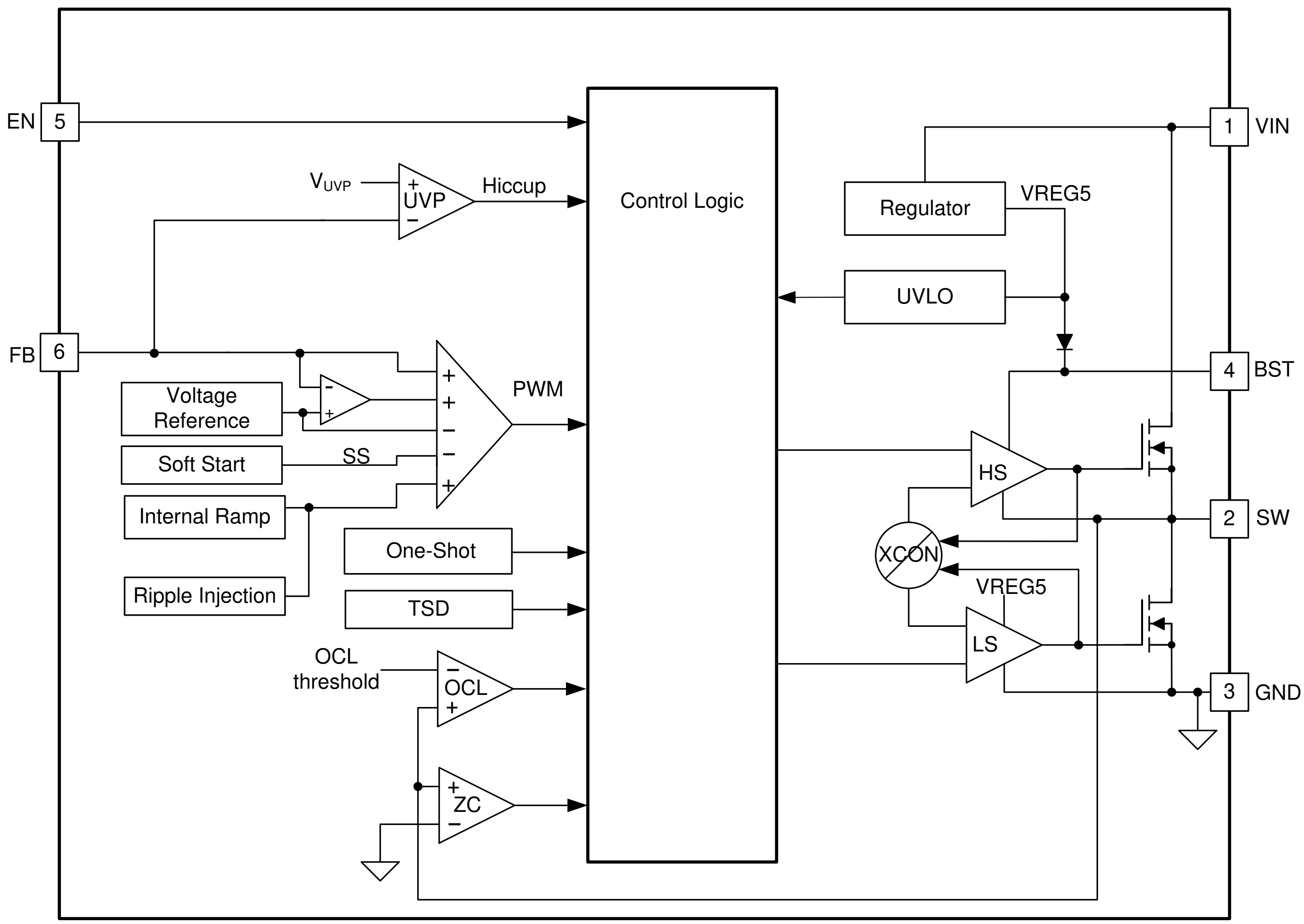
図 12. TPS563231 V_{OUT} = 3.3 V Line Regulation

7 Detailed Description

7.1 Overview

The TPS563231 is 3-A synchronous step-down converter. The proprietary D-CAP3 mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP3 mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS563231 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 mode control. The D-CAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal on-shot timer expires. This one shot duration is set proportional to the converter output voltage, V_{OUT} , and inversely proportional to the input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The on-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP3 mode control.

Feature Description (continued)

7.3.2 Soft Start and Pre-Biased Soft Start

The TPS563231 has an internal 1.5-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage from 0 V to 0.6 V linearly.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.3 Over Current and Short Circuit Protection

The TPS563231 is protected from over-current conditions by cycle-by-cycle current limit on the valley of the inductor current. Hiccup mode will be activated if a fault condition persists to prevent over-heating.

The current going through low-side (LS) MOSFET is sensed and monitored. When the LS MOSFET turns on, the inductor current begins to ramp down. The LS MOSFET will not be turned OFF if its current is above the LS current limit I_{LS_LIMIT} even the feedback voltage, V_{FB}, drops below the reference voltage V_{REF}. The LS MOSFET is kept ON so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit I_{LS_LIMIT}. Then the LS MOSFET is turned OFF and the HS switch is turned on after a dead time.

As the inductor current is limited by I_{LS_LIMT}, the output voltage tends to drop as the inductor current may be smaller than the load current. Hiccup current protection mode is activated once the V_{FB} drops below the UVP threshold after a delay time (800 µs typically). In hiccup mode, the regulator is shut down and kept off for 24 ms typically before the TPS563231 try to start again. If over-current or short-circuit fault condition still exists, hiccup will repeat until the fault condition is removed. Hiccup mode reduces power dissipation under severe over-current conditions, prevents over-heating and potential damage to the device.

7.3.4 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.5 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 160°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPS563231. When V_{EN} is below its threshold (1.13 V typically), the device is in shutdown mode. The switching regulator is turned off and the quiescent current drops to 2.0 µA typically. The TPS563231 also employs V_{IN} under voltage lock out protection. If V_{IN} voltage is below its UVLO threshold (3.6 V typically), the regulator is turned off.

7.4.2 Continuous Conduction Mode (CCM)

Continuous Conduction Mode (CCM) operation is employed when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is pseud fixed, output voltage ripple will be at a minimum in this mode and the maximum output current of 3-A can be supplied.

Device Functional Modes (continued)

7.4.3 Pulse Skip Mode (PSM, TPS563231)

The TPS563231 is designed with Advanced Eco-mode™ to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The low-side MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation current I_{OUT_LL} can be calculated in 式 1.

$$I_{OUT\_LL} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{1}$$

As the load current continues to decrease, the switching frequency also decreases. The on-time starts to decrease once the switching frequency is lower than 250 kHz. The on-time can be about 22% reduced at most for extremely light load condition. This function is employed to achieve smaller ripple at extremely light load condition.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is typical step-down DC-DC converter. It is typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the TPS563231. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The TPS563231 only requires a few external components to convert from a higher variable voltage supply to a fixed output voltage. 図 13 shows a basic schematic of 3.3-V output application. This section provides the design procedure.

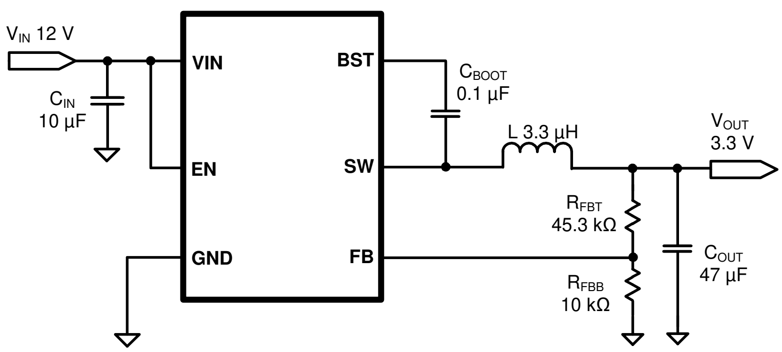


図 13. TPS563231 3.3V/3-A Reference Design

8.2.1 Design Requirements

表 1 shows the design parameters for this application.

表 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 17 V
Output voltage	3.3 V
Transient response, 3-A load step	ΔVout = ±5%
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	600 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. 1% tolerance or better divider resistors are recommended. Start by using 式 2 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the FB input current will be more noticeable.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right) \quad (2)$$

Choose the value of R_{FBB} to be 10 kΩ. With the desired output voltage set to 3.3 V and the V_{REF} = 0.6 V, the R_{FBT} value can then be calculated using 式 2. The formula yields to a value 45.3 kΩ of R_{FBT}.

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP3 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 2.

表 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
1	6.65	10.0	1	1.2	4.7	20 to 68
1.05	7.5	10.0	1	1.2	4.7	20 to 68
1.2	10	10.0	1.2	1.5	4.7	20 to 68
1.5	15	10.0	1.5	1.5	4.7	20 to 68
1.8	20	10.0	1.5	2.2	4.7	20 to 68
2.5	31.6	10.0	2.2	2.2	4.7	20 to 68
3.3	45.3	10.0	2.2	3.3	4.7	20 to 68
5	73.2	10.0	3.3	4.7	4.7	20 to 68
6.5	97.6	10.0	3.3	4.7	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 4, 式 5, and 式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{L\_PP} = \frac{V_{OUT}}{V_{IN\_MAX}} \times \frac{V_{IN\_MAX} - V_{OUT}}{L \times f_{SW}} \quad (4)$$

$$I_{L\_PK} = I_{OUT} + \frac{I_{L\_PP}}{2} \quad (5)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} I_{L\_PP}^2} \quad (6)$$

For this design example, the calculated peak current is 3.67 A and the calculated RMS current is 3.02 A. The inductor used is a WE 74437349033 with a peak current rating of 12 A and an RMS current rating of 6 A.

The capacitor value and ESR determine the amount of output voltage ripple. The TPS563231 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use 式 7 to determine the required RMS current rating for the output capacitor.

$$I_{C\_RMS} = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{\sqrt{12} \times V_{IN\_MAX} \times L \times f_{SW}} \quad (7)$$

For this design two Murata GRM21BR61A226ME44L 22-µF/10-V output capacitors are used in parallel. The typical ESR is 3mΩ each. The calculated RMS current is 0.39 A and each output capacitor is rated for 5 A.

8.2.2.3 Input Capacitor Selection

The TPS563231 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10-µF for the decoupling capacitor. An additional 0.1-µF capacitor from VIN pin to GND pin is also recommended to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage, 25 V or higher voltage rating is recommended.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BST to SW pin for proper operation. 10 V or higher voltage rating is recommended.

8.2.3 Application Curves

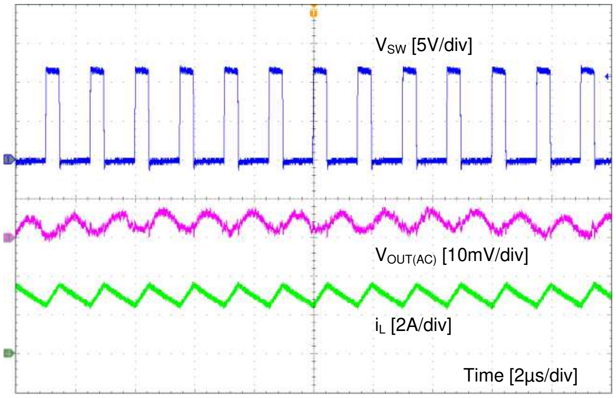


図 14. CCM Mode

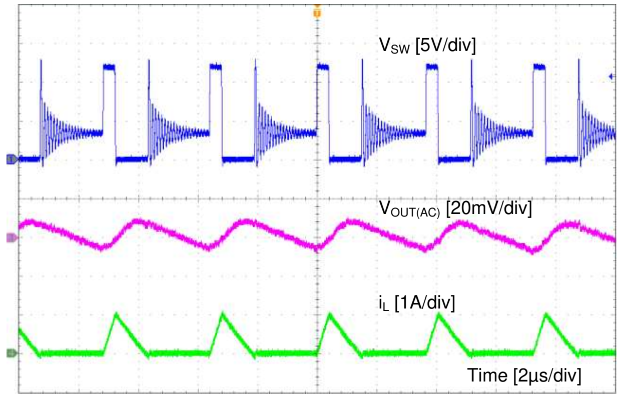
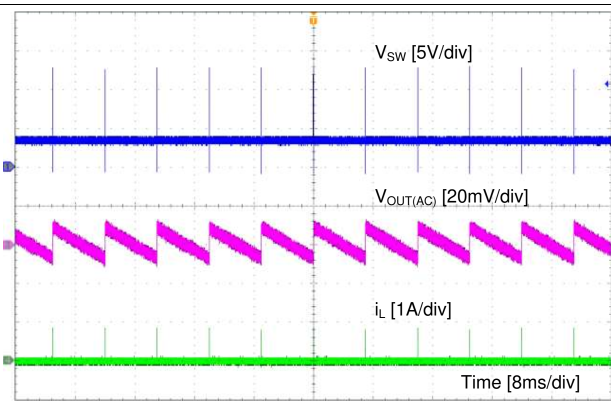


図 15. DCM Mode



I_{OUT} of TPS563231: 10 mA

図 16. PSM Mode

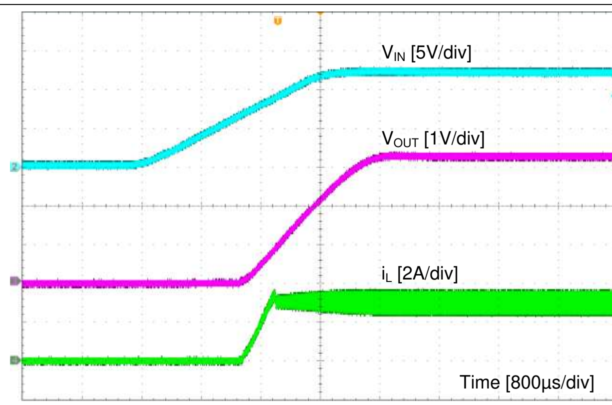


図 17. Start-up by V_{IN}

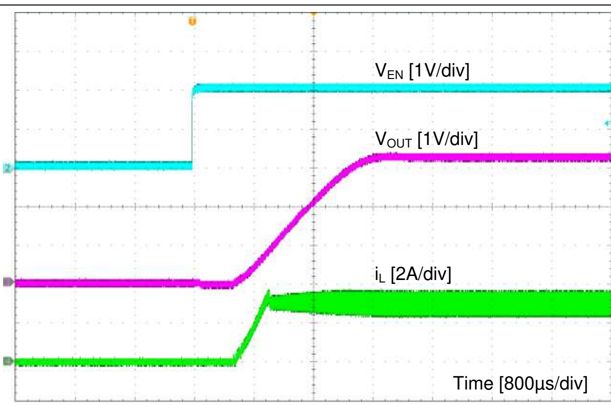


図 18. Start-up by EN

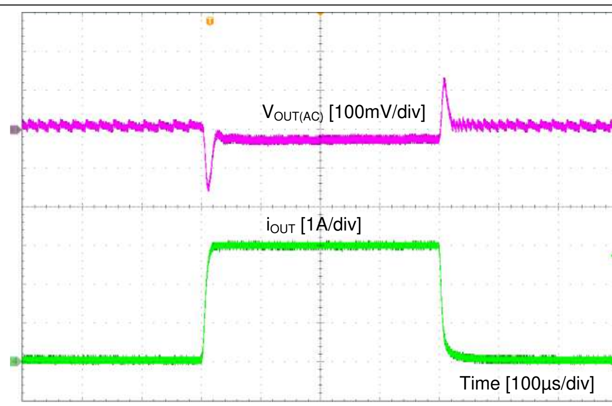


図 19. Load Transient

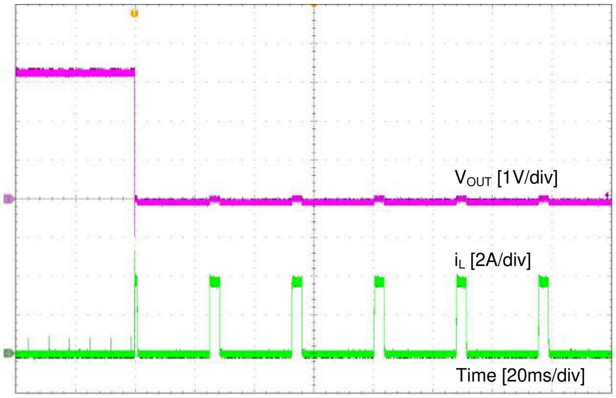


図 20. Short Protection

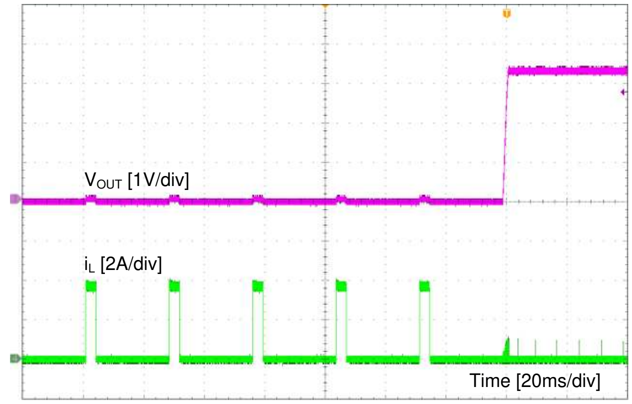


図 21. Short Recovery

9 Power Supply Recommendations

TPS563231 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 72%. Using that criteria, the minimum recommended input voltage is V_O / 0.72.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

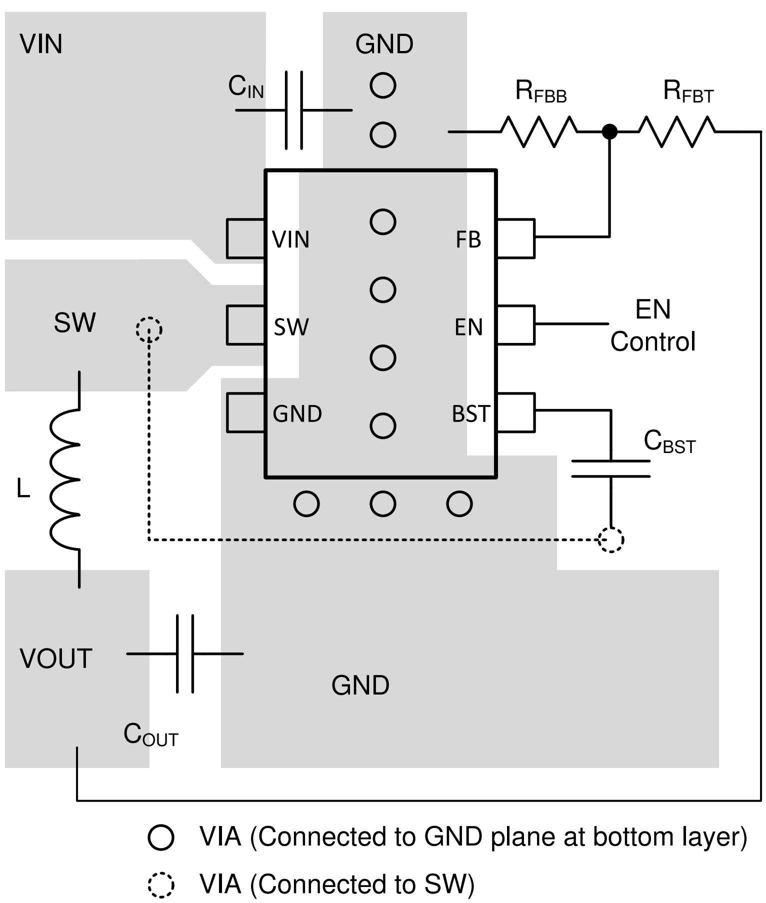


図 22. TPS563231 Layout

11 デバイスおよびドキュメントのサポート

11.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS563231	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS563231DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	3231
TPS563231DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3231
TPS563231DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	3231
TPS563231DRLT	Active	Production	SOT-5X3 (DRL) | 6	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	3231
TPS563231DRLT.A	Active	Production	SOT-5X3 (DRL) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3231
TPS563231DRLT.B	Active	Production	SOT-5X3 (DRL) | 6	250 | SMALL T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	3231

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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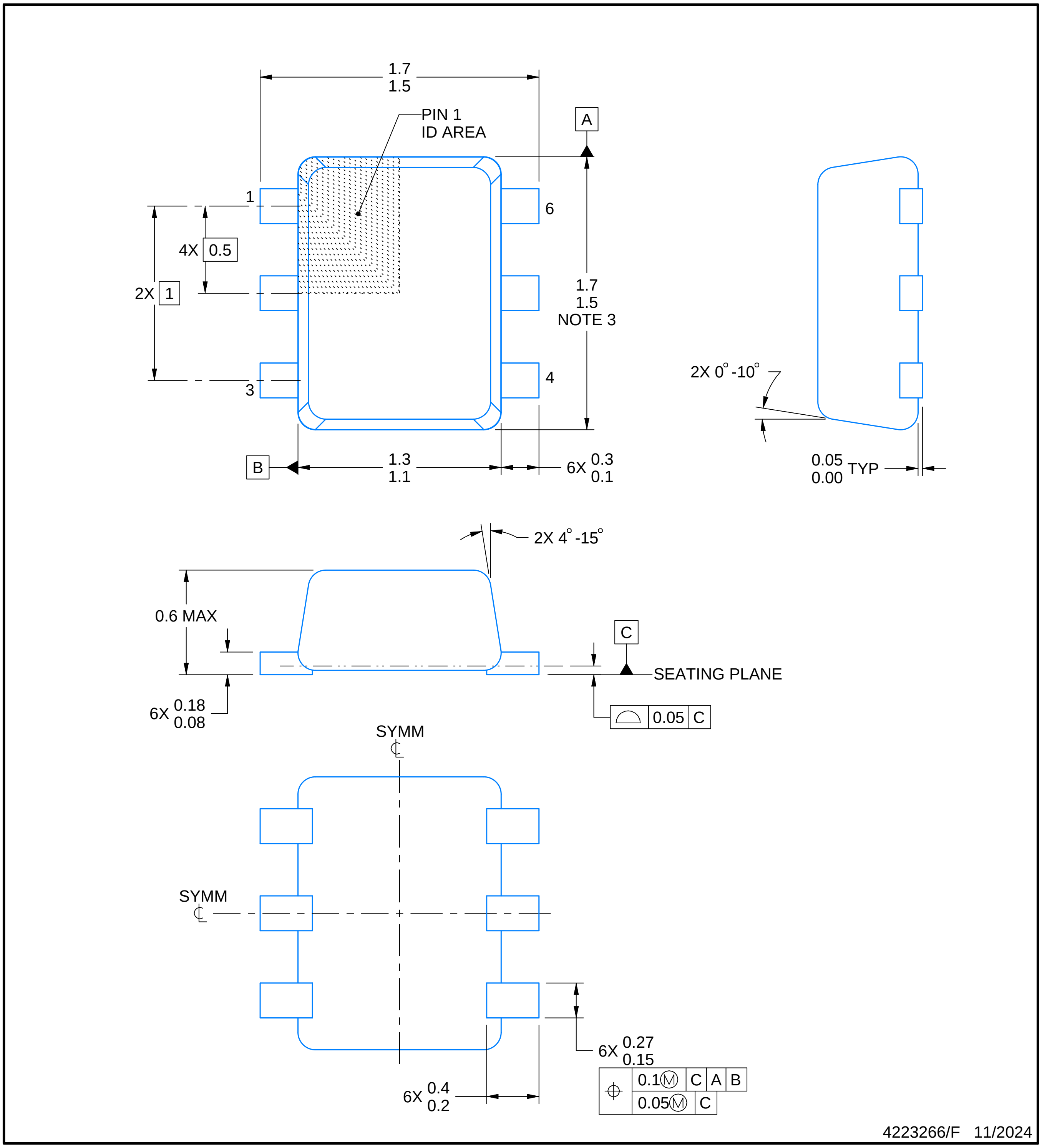
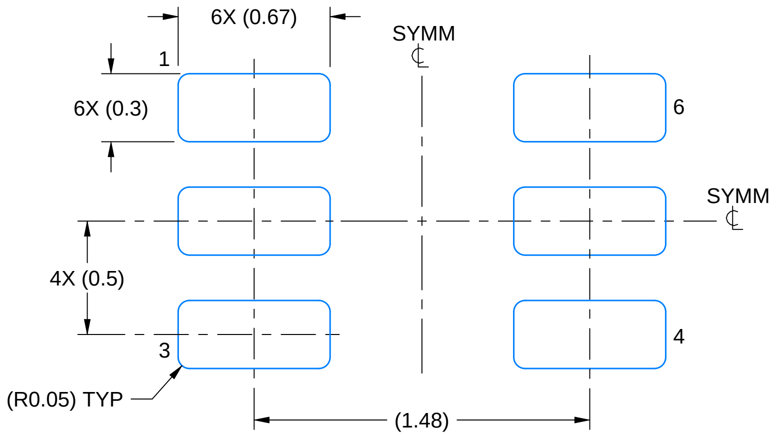
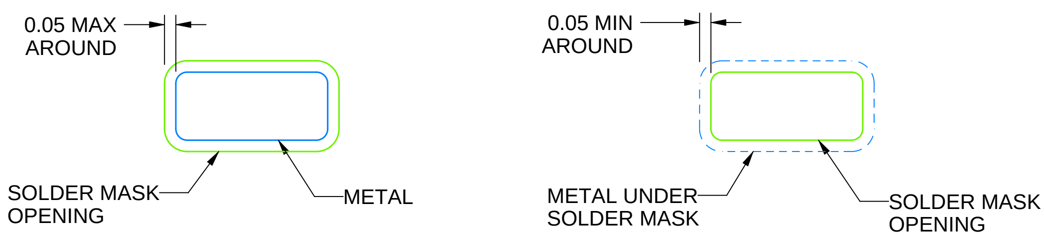


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDERMASK DETAILS

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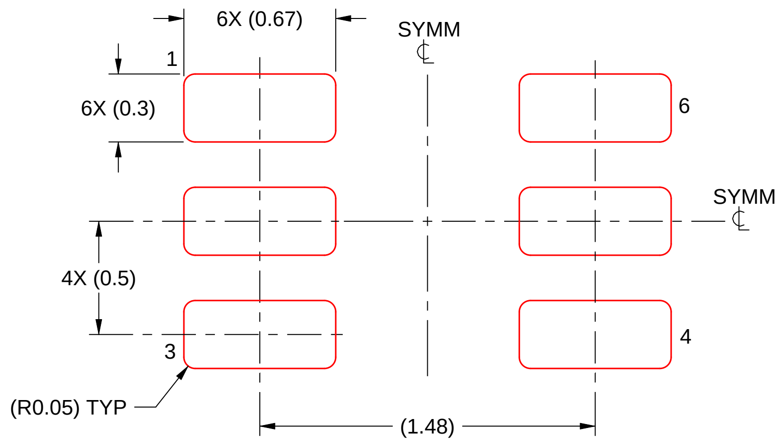
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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