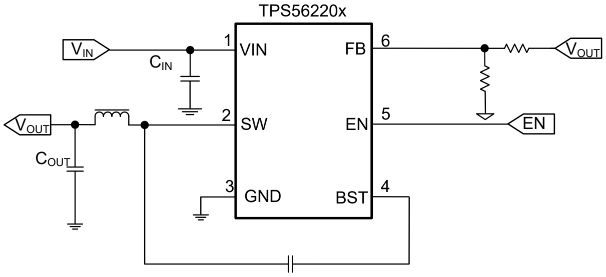
TPS56220x 4.2V～17V 入力、2A、同期整流型降圧コンバータ、SOT563 パッケージ

1 特長

- 多様なアプリケーションに適した構成
  - 入力電圧範囲:4.2V～17V
  - 出力電圧範囲:0.6V～7V
  - 基準電圧:0.6V
  - 25°C で ±1.5% の基準電圧精度
  - -40℃～125℃で ±2% の基準電圧精度
  - 100mΩ および 55mΩ FET を内蔵
  - TPS562203 の低静止時電流:110μA
  - スイッチング周波数:600kHz
  - 最大 95% の高デューティ サイクル動作
  - 固定ソフトスタート時間:1.4ms
- 使いやすく小さい設計サイズ
  - TPS562203 の軽負荷時の Eco-mode
  - TPS562206 の軽負荷時の FCCM モード
  - 高速過渡応答の D-CAP3™ 制御モード
  - あらかじめ出力にバイアスが印加された状態でのスタートアップをサポート
  - ラッチなしの OT および UVLO 保護
  - サイクル単位の過電流制限
  - ヒカップ モードによる UV 保護
  - 動作時の接合部温度範囲:-40℃～125℃
  - SOT563 パッケージ:1.6mm × 1.6mm
- WEBENCH® Power Designer により、TPS562203 を使用するカスタム設計を作成
- WEBENCH® Power Designer により、TPS562206 を使用するカスタム設計を作成

2 アプリケーション

- テレビ
- デジタル・セットトップ・ボックス (STB)
- ビルディング・オートメーション
- ブロードバンド固定回線アクセス



概略回路図

3 概要

TPS562203、TPS562206 は単純で使いやすい 2A 同期整流式降圧コンバータで、SOT563 パッケージに搭載されています。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が小さくなるよう設計されています。

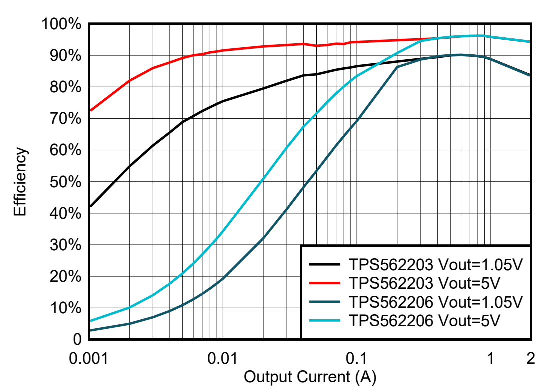
このスイッチ モード電源 (SMPS) デバイスは、D-CAP3 制御モードを採用し、高速の過渡応答を実現します。また、特殊ポリマーなど ESR (等価直列抵抗) の低い出力コンデンサと、超低 ESR のセラミック コンデンサの両方を、外部補償部品なしでサポートします。

TPS562203 は ECO モードで動作することで、軽負荷動作中も高い効率を維持します。TPS562206 は FCCM モードで動作することで、すべての負荷条件で同じ周波数と小さい出力リップルを維持します。このデバイスは、OCP、UVLO、OTP、UVP (ヒカップ機能付き) による完全な保護機能を備えています。TPS56220x は 6 ピン、1.6mm × 1.6mm の SOT563 (DRL) パッケージで供給され、接合部温度 -40℃～125℃で動作が規定されています。

製品情報

部品番号	モード	パッケージ (1)	パッケージ サイズ (2)
TPS562203	ECO モード	DRL (SOT563、6)	1.60mm x 1.60mm
TPS562206	FCCM (強制連続導通モード) モード		

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



TPS562203 と TPS562206 の効率

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4 Pin Configuration and Functions

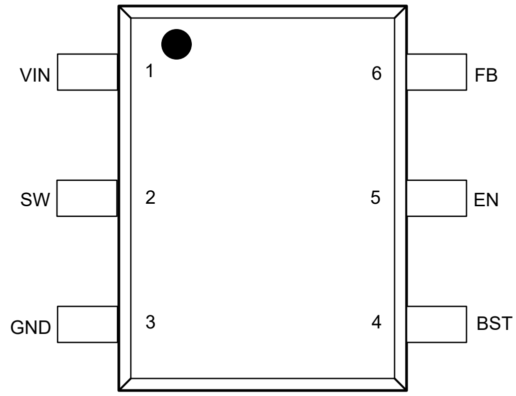


図 4-1. 6-Pin SOT563 DRL Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIN	1	I	Input voltage supply pin
SW	2	O	Switch node connection between high-side NFET and low-side NFET
GND	3	—	Ground pin source terminal of low-side power NFET, as well as the ground terminal for controller circuit. Connect sensitive FB to this GND at a single point.
BST	4	O	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between the BST and SW pin.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
FB	6	I	Converter feedback input. Connect to output voltage with feedback resistor divider.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	18	V
Input voltage	FB, EN	–0.3	6	V
Input voltage	GND	–0.3	0.3	V
Output voltage	BST	–0.3	25	V
Output voltage	BST (< 20ns)	–0.3	27	V
Output voltage	SW	–2	18	V
Output voltage	SW (< 20ns)	–6.5	20	V
Operating Junction Temperature Range, TJ		–40	150	°C
Storage temperature, Tstg	Storage temperature, Tstg	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN	4.2		17	V
Input voltage	FB, EN	–0.1		5.5	V
GND	GND	–0.1		0.1	V
Output voltage	BST	–0.1		23	V
Output voltage	BST (< 20ns)	–0.1		25	V
Output voltage	SW	–1		17	V
Output voltage	SW (< 20ns)	–6		19	V
Output Current	IO	0		2	A
T_J	Operating junction temperature	–40		125	°C
Tstg	Storage temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		DRL (SOT-563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.4	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance on EVM board	73[2]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) This $R_{\theta JA\_effective}$ is tested on TPS562203EVM board (2 layer, copper thickness of top and bottom layer are 2oz) at Vin = 12V, Vout = 5V, Iout = 2A , TA = 25ºC.

5.5 Electrical Characteristics

Over operating T_J = –40ºC – 125ºC, V_{Vin} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
Vin	Input voltage range		4.2		17	V
I_{Vin}	Vin supply current	No load, V_{EN} = 5V, non-switching, PSM version		110		µA
		No load, V_{EN} = 5V, VFB = 0.7V, FCCM version		350		µA
I_{InSdn}	Vin shutdowncurrent	V_{EN} = 0V		7		µA
UVLO						
UVLO	Vin undervoltage lockout	Wake up VIN voltage	3.6	3.8	4	V
UVLO	Vin undervoltage lockout	Shut down VIN voltage	3.2	3.4	3.6	V
UVLO	Vin undervoltage lockout	Hysteresis VIN voltage		400		mV
FEEDBACK VOLTAGE						
VFB	FB voltage	T_J = 25°C, Vin = 4.2 – 17V	591	600	609	mV
VFB	FB voltage	T_J = –40°C to 125°C, Vin = 4.2 – 17V	588	600	612	mV
MOSFET						
$R_{DS\ (on)Hi}$	High-side MOSFET Rds(on)	T_J = 25°C		100		mΩ
$R_{DS\ (on)Lo}$	Low-side MOSFET Rds(on)	T_J = 25°C		55		mΩ
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	V_{VOUT} = 3.3V		600		kHz
$T_{OFF(Min)}$	Minimum off-time [1]	V_{FB} = 0.5V		100		ns
$T_{ON(Min)}$	Minimum on-time [1]			55		ns
CURRENT LIMIT						
I_{OCL_LS}	Over current threshold	Valley current set point	2.5	3.9	4.8	A
I_{NOCL}	Negative over current threshold	Valley current set point	0.7	1.3	1.9	A
LOGIC THRESHOLD						
$V_{EN(On)}$	EN threshold high-level		1.15	1.21	1.27	V
$V_{EN(Off)}$	EN threshold low-level		0.95	1.00	1.05	V
V_{ENHys}	EN hysteris			200		mV
OUTPUT DISCHARGE and SOFT START						

5.5 Electrical Characteristics (続き)

Over operating T_J = –40ºC – 125ºC, V_{Vin} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IEN	EN pulldown current	VEN = 1.5V		1		uA
t_{SS}	Internal soft-start time	Vout from 0 to target value.		1.4		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{UVP}	UVP trip threshold		55	60	65	%
t_{UVPDly}	UVP prop deglitch			256		us
t_{UVPOn}	In continuous hiccup mode, the switching time	Hard short, UVP detect		1.5		ms
t_{UVPOff}	In continuous hiccup mode, non-switching time	Hard short, UVP detect		13		ms
THERMAL PROTECTION						
T_{OTP}	OTP trip threshold			155		°C
T_{OTPHsy}	OTP hysteresis			20		°C

(1) Specified by design

5.6 Typical Characteristics

V_{IN} = 12V (unless otherwise noted)

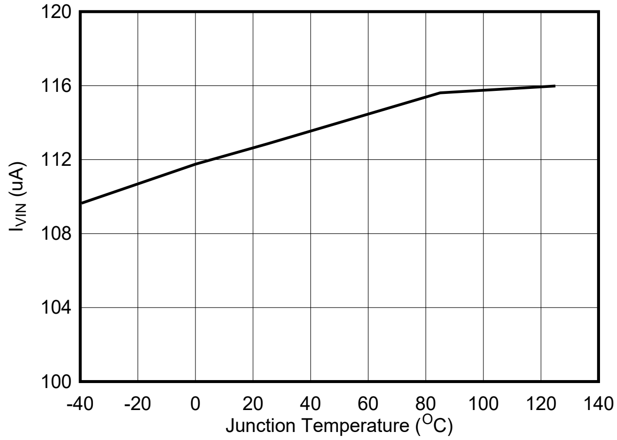


図 5-1. TPS562203 Quiescent Current

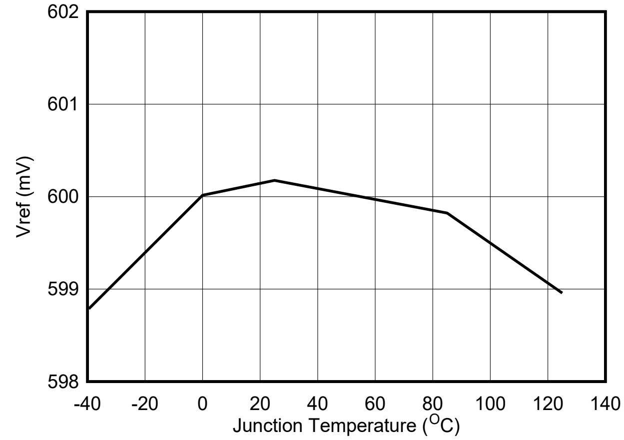


図 5-2. Vref Voltage

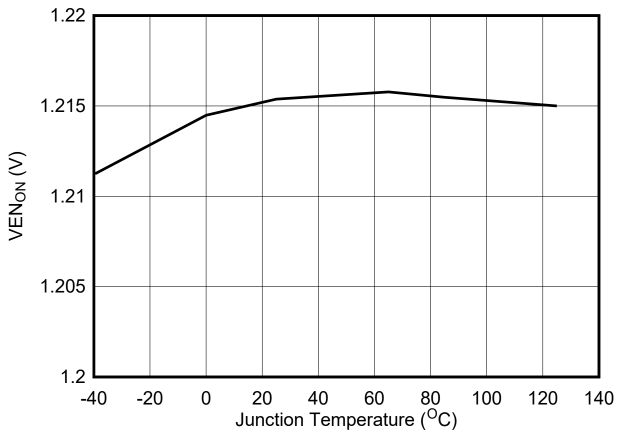


図 5-3. Enable On Threshold Voltage

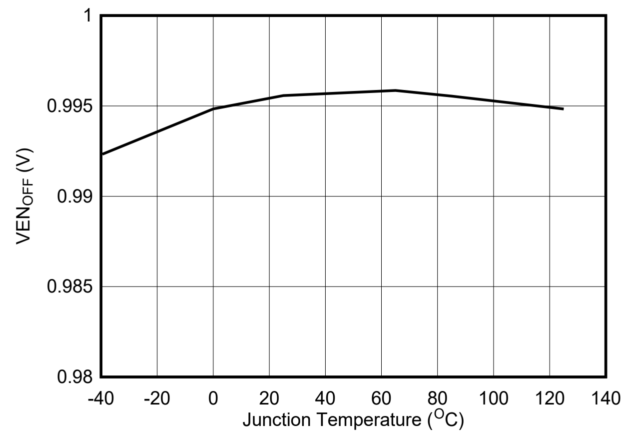


図 5-4. Enable Off Threshold Voltage

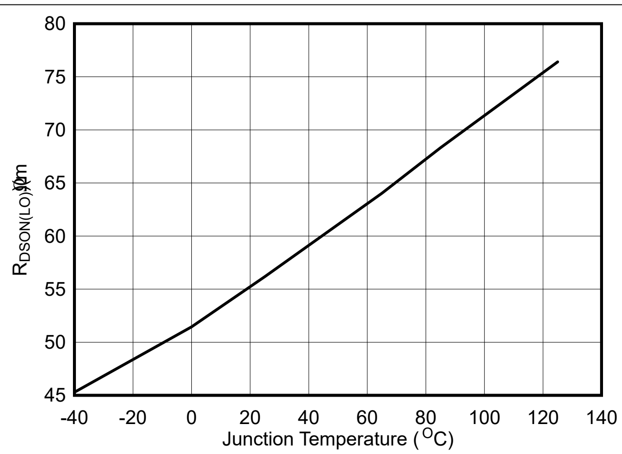


図 5-5. Low-Side Rdson

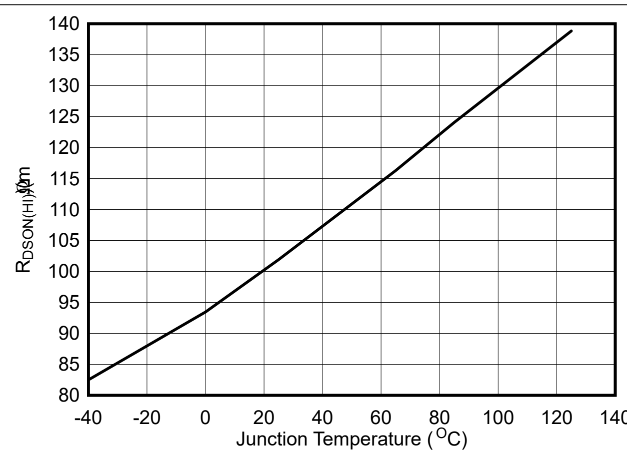


図 5-6. High-Side Rdson

5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

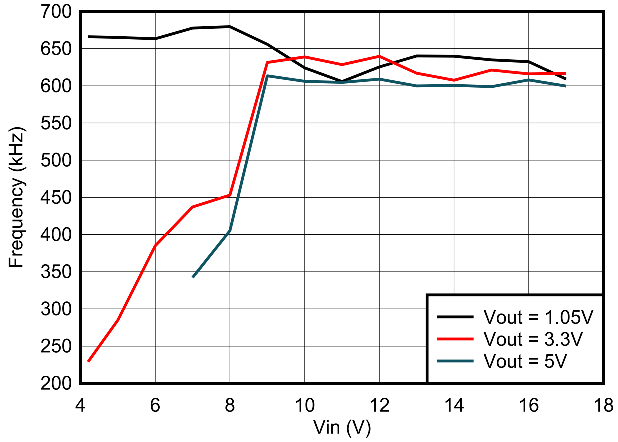


図 5-7. Frequency vs Input Voltage at 2A Loading

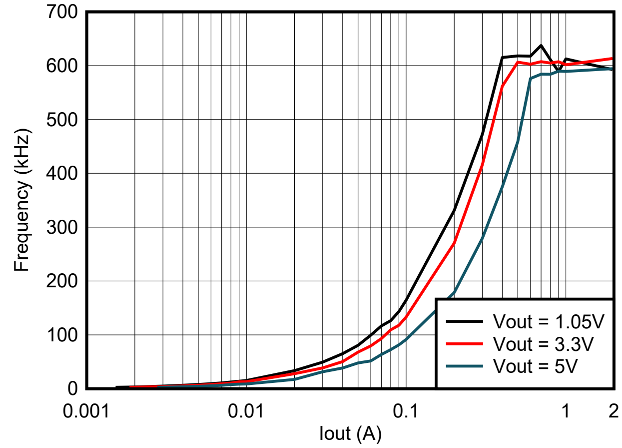


図 5-8. TPS562203 Frequency vs Loading

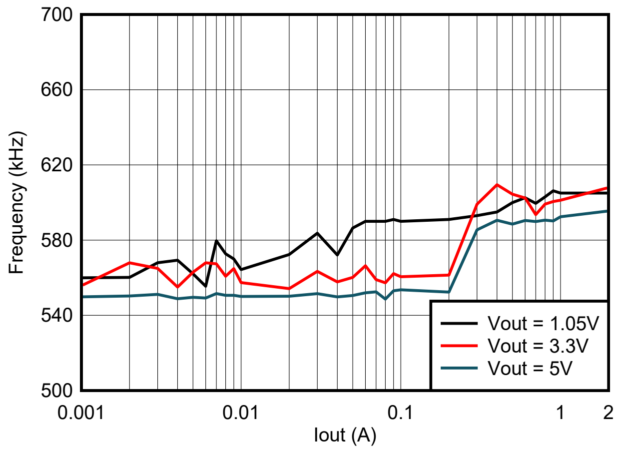


図 5-9. TPS562206 Frequency vs Loading

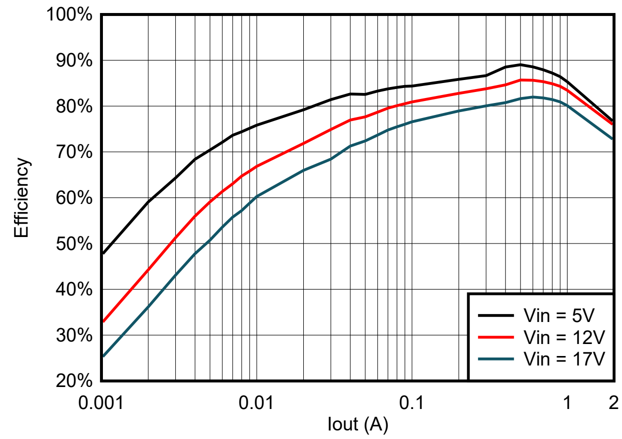


図 5-10. TPS562203 Efficiency at 0.6 Vout With 1.5uH Inductor

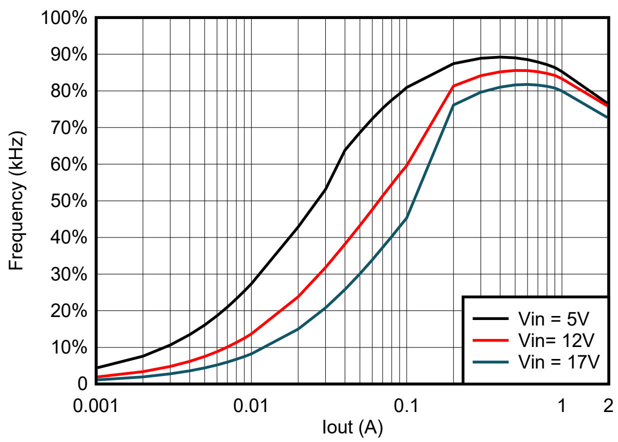


図 5-11. TPS562206 Efficiency at 0.6 Vout With 1.5uH Inductor

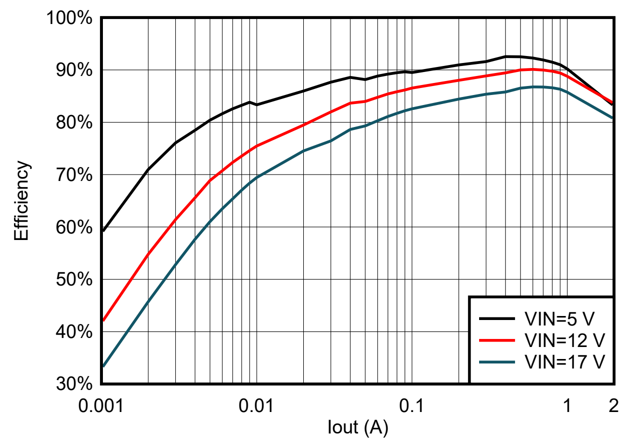


図 5-12. TPS562203 Efficiency at 1.05 Vout With 2.2uH Inductor

5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

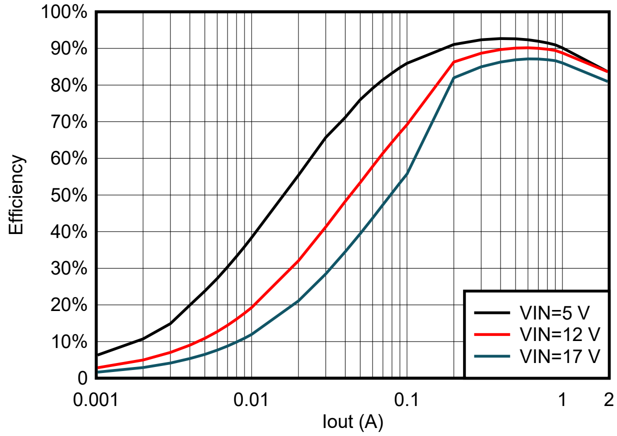


図 5-13. TPS562206 Efficiency at 1.05 Vout With 2.2uH Inductor

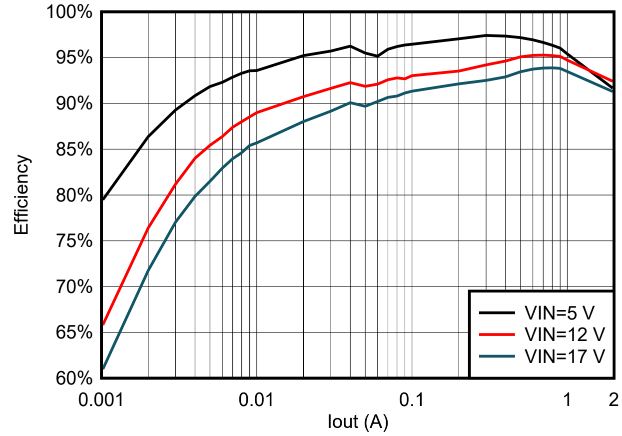


図 5-14. TPS562203 Efficiency at 3.3 Vout With 4.7uH Inductor

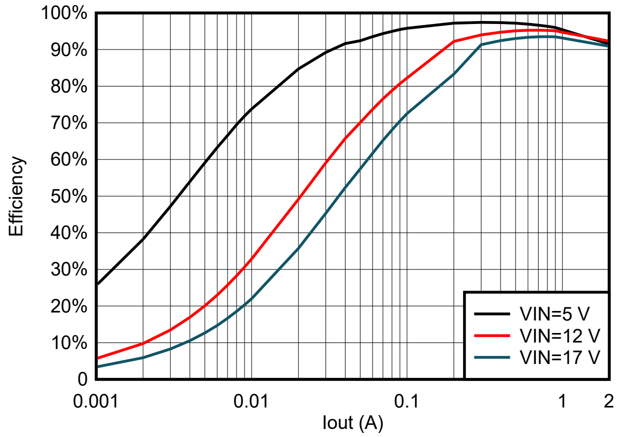


図 5-15. TPS562206 Efficiency at 3.3 Vout With 4.7uH Inductor

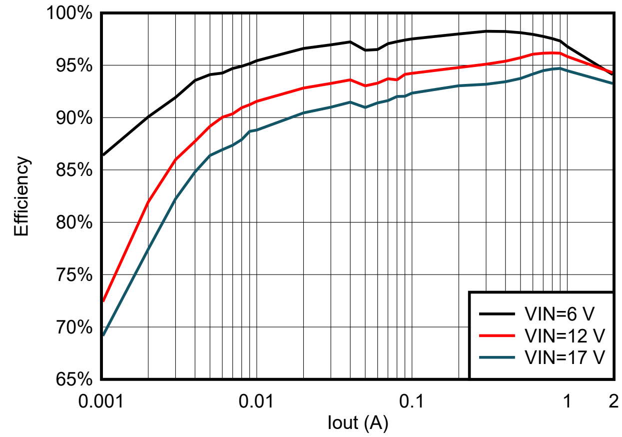


図 5-16. TPS562203 Efficiency at 5 Vout With 4.7uH Inductor

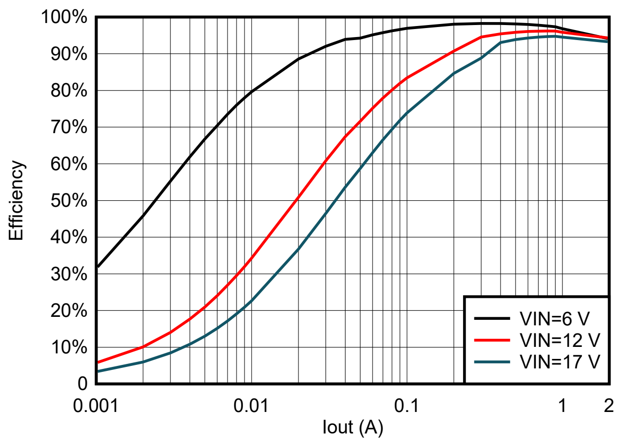


図 5-17. TPS562206 Efficiency at 5 Vout With 4.7uH Inductor

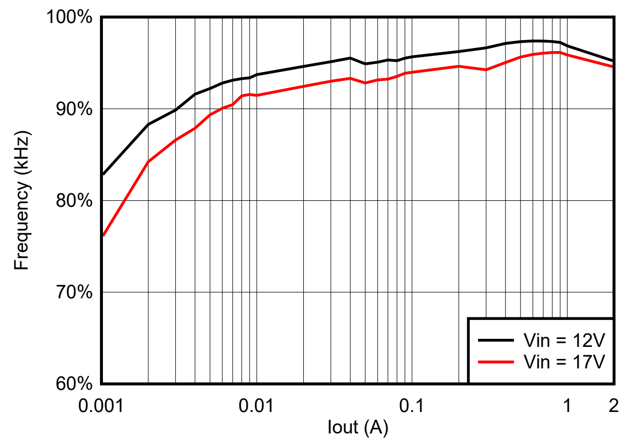


図 5-18. TPS562203 Efficiency at 7 Vout With 6.8uH Inductor

5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

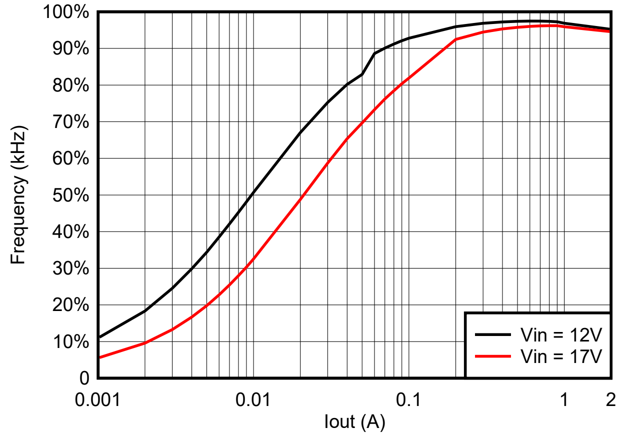


図 5-19. TPS562206 Efficiency at 7 Vout With 6.8uH Inductor

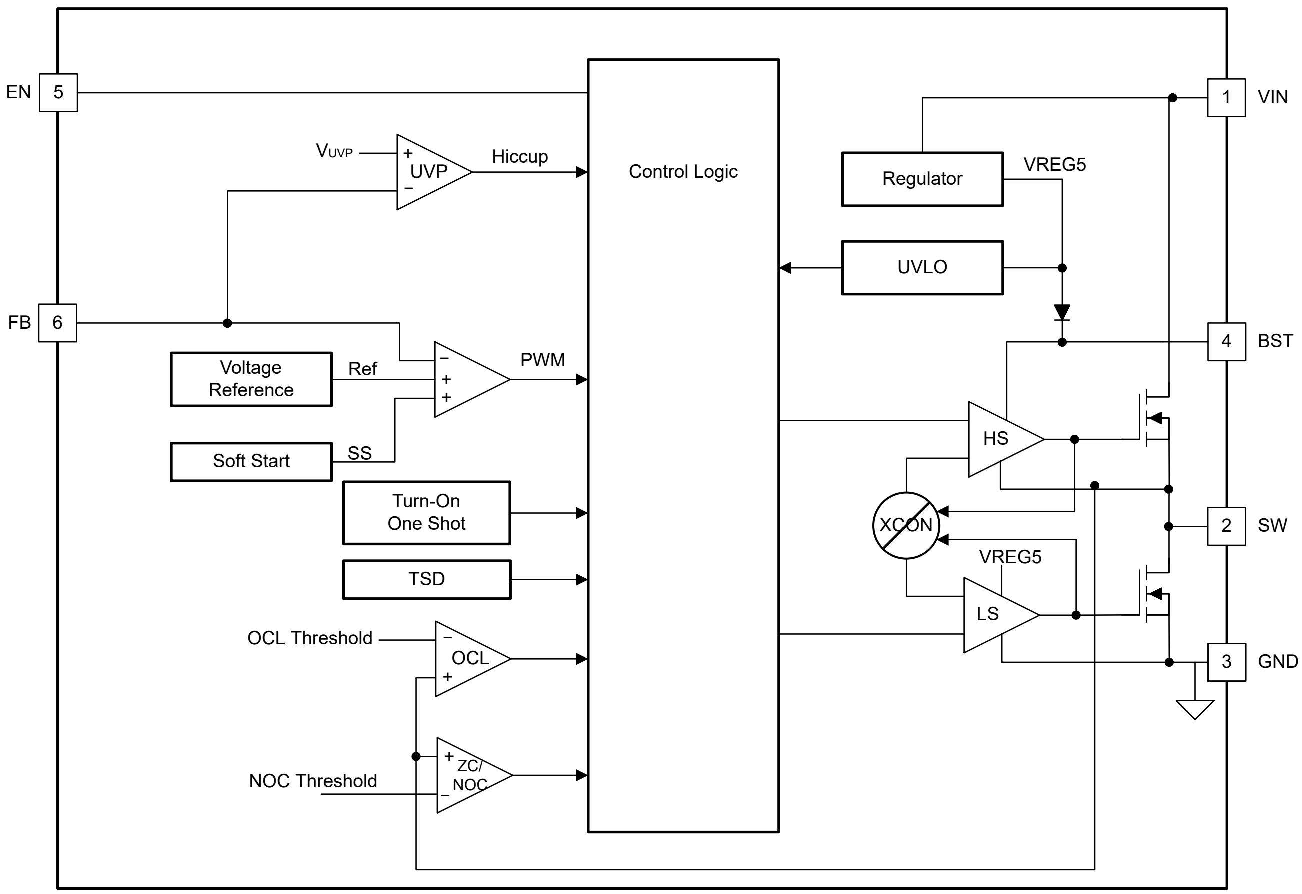
6 Detailed Description

6.1 Overview

The TPS56220x is a 2A, integrated, FET, synchronous step-down buck converter that operates from 4.2V to 17V input voltage (VIN) and 0.6V to 7V output voltage. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The proprietary D-CAP3 control mode enables low external component count, ease of design, and optimization of the power design for cost, size, and efficiency. The topology provides a seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition.

The Eco-mode version allows the TPS562203 to maintain high efficiency at light load. The FCCM mode version allows the TPS562206 to maintain a fixed switching frequency and lower output voltage ripple. The TPS56220x is able to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP and ultra-low ESR ceramic capacitors.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS56220x is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The D-CAP3 control mode is stable even with virtually no ripple at the output. The TPS56220x also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after the internal one shot timer expires. This one shot duration is set proportional to the output voltage, V_O, and inversely proportional to the converter input voltage, VIN, to maintain a pseudo-fixed frequency over the input voltage range, hence called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP3 control mode.

6.3.2 Eco-mode Control

TPS562203 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that the ripple valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as in the continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes a longer time. This action makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Use 式 1 to calculate the transition point to the light load operation $I_{OUT(LL)}$ current.

$$I_{out(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{1}$$

6.3.3 Soft Start and Prebiased Soft Start

TPS56220x have an internal typical 1.4ms soft start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme makes sure that the converters ramp up smoothly into regulation point.

6.3.4 Large Duty Operation

The TPS56220x can support large duty operations up to 95% by smoothly dropping down the switching frequency. When input voltage Vin < 7V and VFB is lower than internal reference voltage, the switching frequency is allowed to smoothly drop to make TON extended to keep output voltage and improve the load transient performance. The minimum switching frequency is limited to about 200kHz.

6.3.5 Current Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time, and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{out}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter. This event even can cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects the fall. Then, the device shuts down after the UVP delay time and re-starts after the hiccup time.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

The TPS562206 is an FCCM mode part. In this mode, the device has negative inductor current at light loading. The device has NOC (negative overcurrent) protection to avoid too large negative current. NOC protection detects the valley of inductor current. When the valley value of inductor current exceeds the NOC threshold, the IC turns off the low side then turns on the high side. When NOC protection is triggered eight times continuously, IC turns off both high side FET and low side FET. When the NOC condition is removed and output voltage returns to target value, the device returns to normal switching.

Because the TPS562206 is an FCCM mode port, if the inductance is so small that the device triggers NOC, the output voltage becomes higher than the target value. The minimum inductance is identified as 式 2.

$$L = \frac{V_{out} \times \left(1 - \frac{V_{out}}{V_{in}}\right)}{2 \times Frequency \times NOC_{min}} \quad (2)$$

6.3.6 Enable Circuit

The EN pin controls the turn-on and turn-off of the device. When the EN pin voltage is above the turn-on threshold, the device starts switching, and when the EN pin voltage falls below the turn-off threshold, the device stops switching. The default status is low because there is a 1uA pulldown current in internal IC.

EN can be controlled by a typical divider resistor circuit from Vin or by a voltage of lower than 5.5V.

TPS56220x also allows EN to connect to Vin by only a pullup resistor, which must be a 100kohm resistor. EN voltage is clamped by a Zener diode. This Zener diode is not allowed to go through large current. R1 is not allowed smaller than 80k ohm. R1 must also not use a too large resistor to avoid EN not being able to turn on. So R1 range is 80k ohm to 3M ohm. R1 must use 100k ohm.

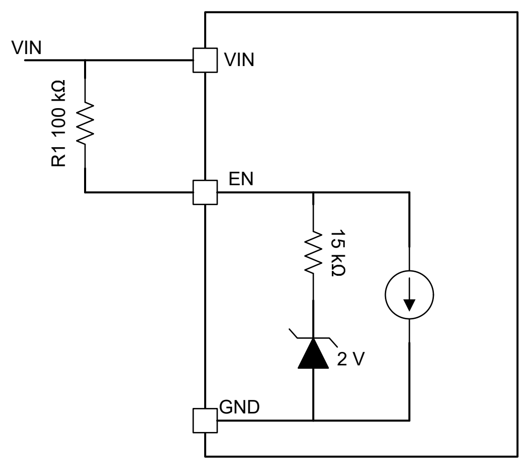


図 6-1. EN Block Circuit

6.3.7 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

6.3.8 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This protection is a non-latch protection.

6.4 Device Functional Modes

6.4.1 Eco-mode Operation

The TPS562203 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This fact makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

6.4.2 FCCM Mode Operation

The TPS562206 operates in forced CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency (FSW) is maintained at an almost constant level over the entire load range, which is designed for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The devices are typical buck DC/DC converters. The devices are typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 2A. The following design procedure can be used to select component values for TPS56220x. Alternately, the WEBENCH® software can be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

7.2 Typical Application

The application schematic in 図 7-1 is developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The section provide the design procedure.

図 7-1 shows the TPS562203 4.2V to 17V input, 1.05V output converter schematics.

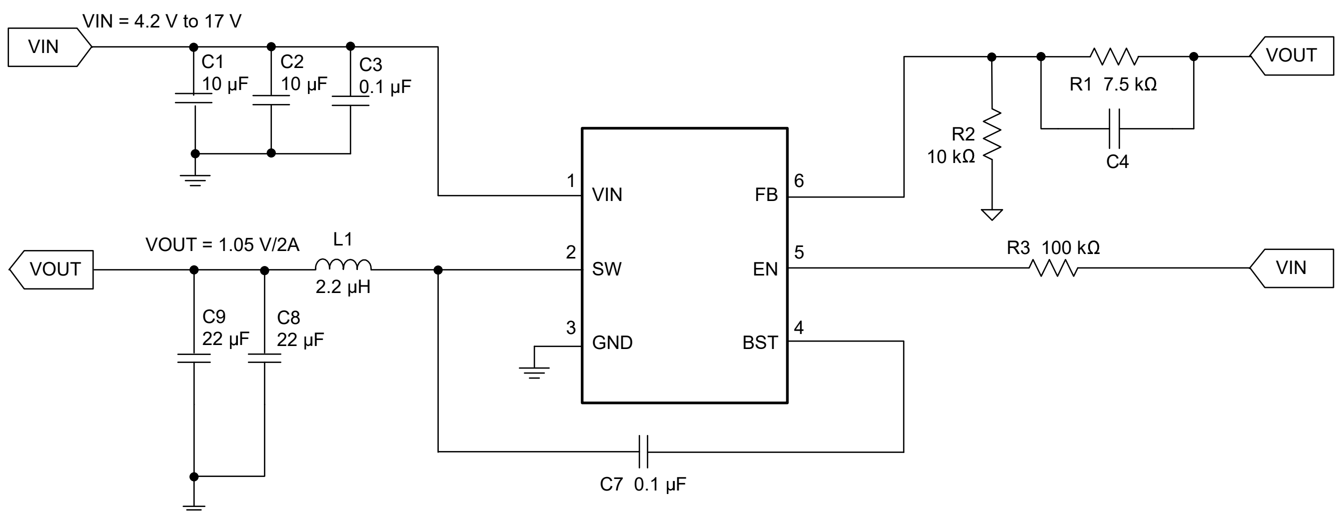


図 7-1. TPS562203 1.05V/2A Reference Design

7.2.1 Design Requirements

表 7-1 shows the design parameters for this application.

表 7-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.2V to 17V
Output voltage	1.05V
Transient response, 1.5A load step	ΔVout = ±5%
Input ripple voltage	100mV
Output ripple voltage	20mV
Output current rating	2A
Operating frequency	600 kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS562203 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS562206 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 式 3 to calculate V_{OUT}.

To improve efficiency at very light loads, consider using larger value resistors. Too high of resistance is more susceptible to noise and voltage errors from the FB input current are more noticeable.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right) \tag{3}$$

7.2.2.3 Output Filter Selection

The LC filter used as the output filter has a double pole at 式 4. In this equation, C_{OUT} must use effective value after derating, not nominal value.

$$Frequency_{doublepole} = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \tag{4}$$

For any control topology that is compensated internally, there is a range of the output filter control topology can support. At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40dB per decade rate and the phase drops has a 180 degree drop. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is about 41kHz. TI recommends the inductor and capacitor selected for the output filter that the double pole is located about 20kHz, so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. For higher than 2V output voltage, TI suggests to add a CFF (Cap of Feed Forward) C4 in schematic to increase the bandwidth and phase margin. The suggested CFF range is 10pF to 100pF. The crossover frequency of the overall system must usually be targeted to be less than one-third of the switching frequency.

表 7-2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	Min L(uH)	TYP L (uH)	Max L(uH)	Min Cout(uF)	Typ Cout(uF)	Max Cout(uF)	CFF(pF)
0.8	3.33	10.0	1.2	1.5	2.2	22	66	110	-
1.05	7.5	10.0	1.2	2.2	3.3	22	44	110	-
2.5	95.0	30.0	2.2	3.3	4.7	22	44	110	10
3.3	135.0	30.0	3.3	4.7	6.8	22	44	110	18
5	220.0	30.0	3.3	4.7	6.8	22	44	110	18
7	320.0	30.0	3.3	4.7	6.8	22	44	110	18

Use 式 5, 式 6, and 式 7 to calculate the inductor peak-to-peak ripple current, peak current and RMS current. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$II_{P-P} = \frac{V_{OUT}}{V_{IN(Max)}} \times \frac{V_{IN(Max)} - V_{OUT}}{L_{OUT} \times f_{SW}} \tag{5}$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2} \tag{6}$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} \times II_{P-P}^2} \tag{7}$$

For this design example, the calculated peak current is 3.68A and the calculated RMS current is 3.03A. The inductor used is a WE 74437349022.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS562203 are intended for use with ceramic or other low ESR capacitors. TI recommends to use 2 × 22μF output cap. Use 式 8 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times f_{SW}} \tag{8}$$

For this design, two MuRata GRM21BR61A226ME44L 22μF output capacitors are used. The typical ESR is 2mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 4A.

7.2.2.4 Input Capacitor Selection

The TPS562203 requires an input decoupling capacitor, and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10μF for the decoupling capacitor. An additional 0.1μF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

7.2.2.5 Bootstrap Capacitor Selection

Connect a 0.1μF ceramic capacitor between the BST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

7.2.3 Application Curves

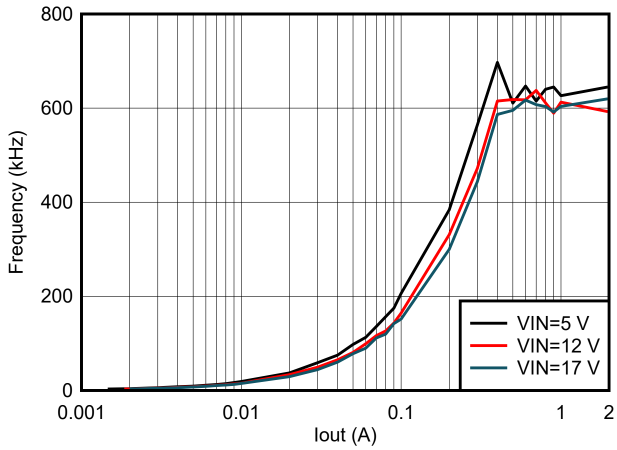


図 7-2. TPS562203 Frequency vs Loading

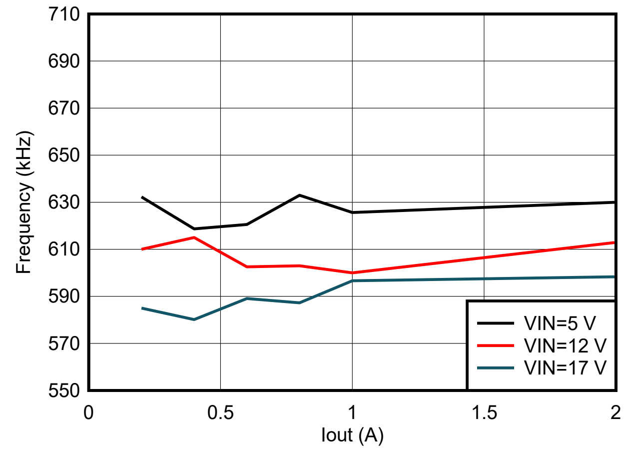


図 7-3. TPS562206 Frequency vs Loading

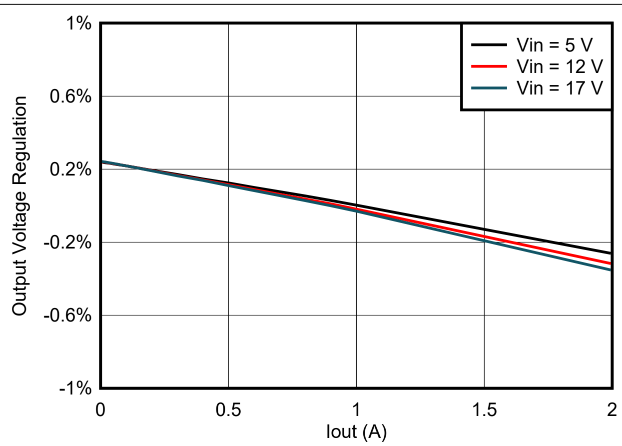


図 7-4. TPS562203 Load Regulation vs Loading

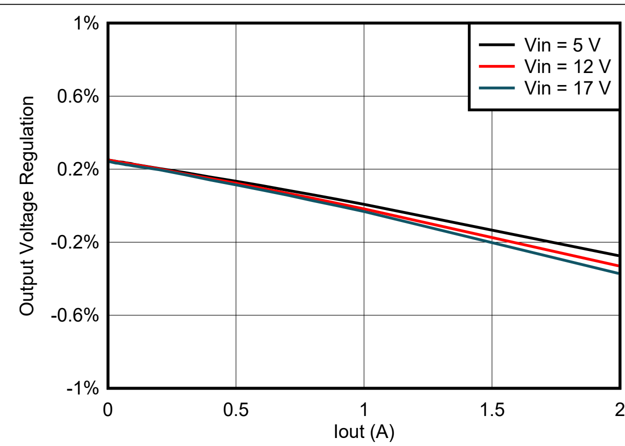


図 7-5. TPS562206 Load Regulation vs Loading

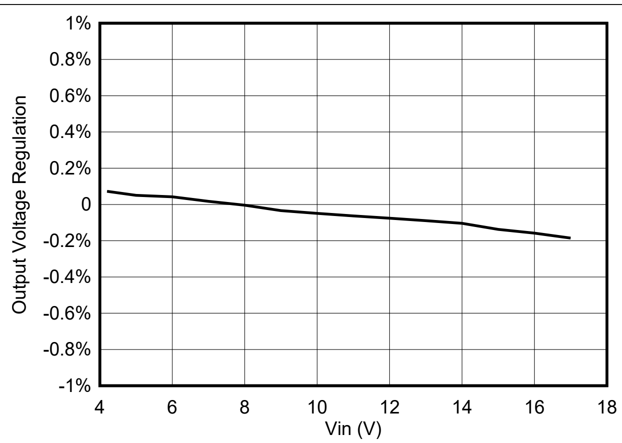


図 7-6. TPS562203 Line Regulation vs Vin at 1A Loading

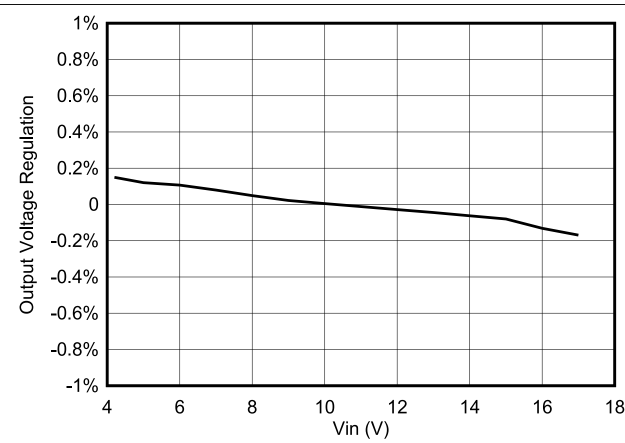


図 7-7. TPS562206 Line Regulation vs Vin at 1A Loading

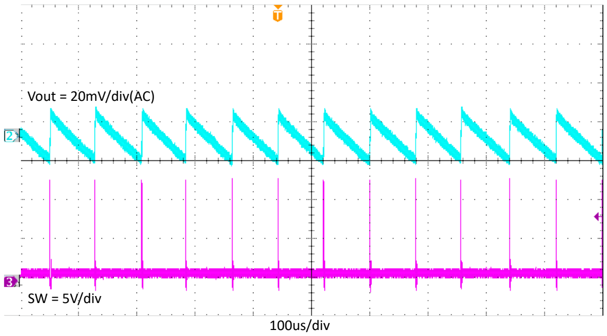


図 7-8. TPS562203 Output Voltage Ripple With 0.1A Loading

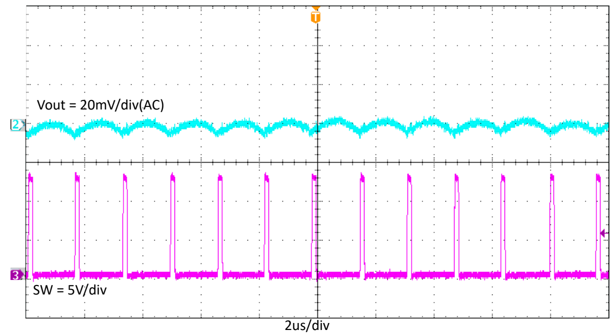


図 7-9. TPS562206 Output Voltage Ripple With 0.1A Loading

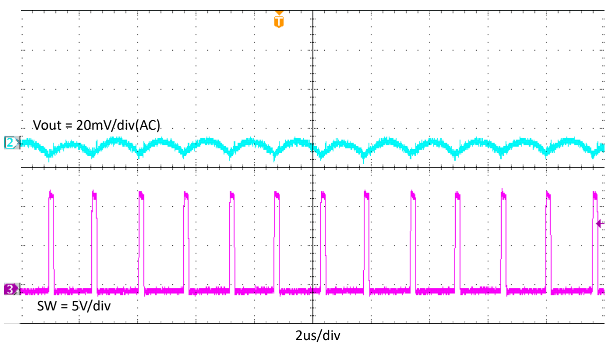


図 7-10. TPS562203 Output Voltage Ripple With 2A Loading

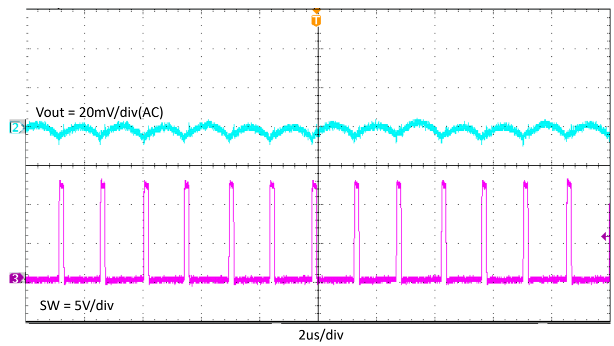


図 7-11. TPS562206 Output Voltage Ripple With 2A Loading

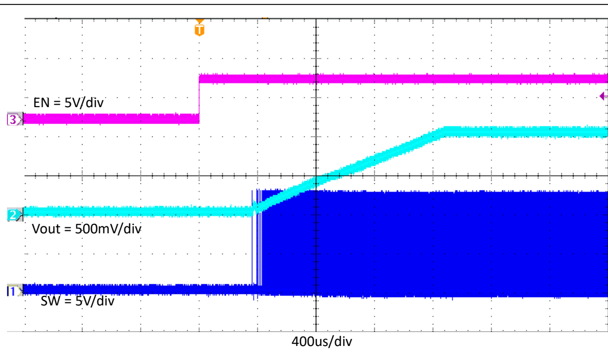


図 7-12. TPS562203 Enable On With 2A Loading

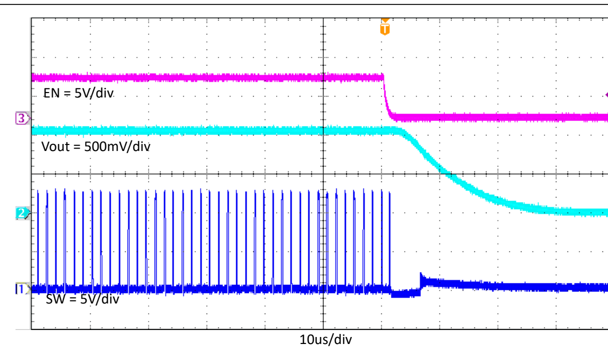


図 7-13. TPS562203 Enable Off With 2A Loading

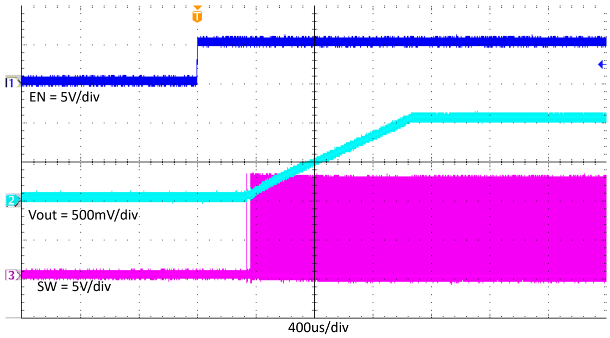


図 7-14. TPS562206 Enable On With 2A Loading

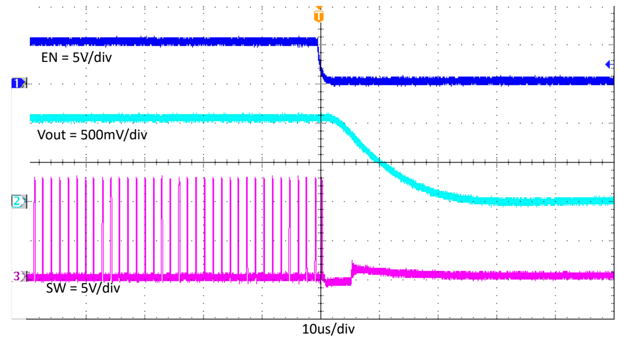


図 7-15. TPS562206 Enable Off With 2A Loading

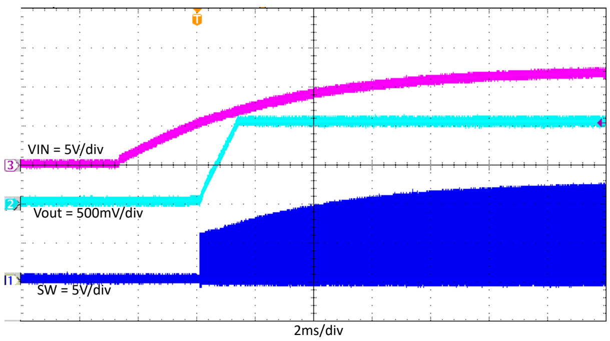


図 7-16. TPS562203 Power On With 2A Loading

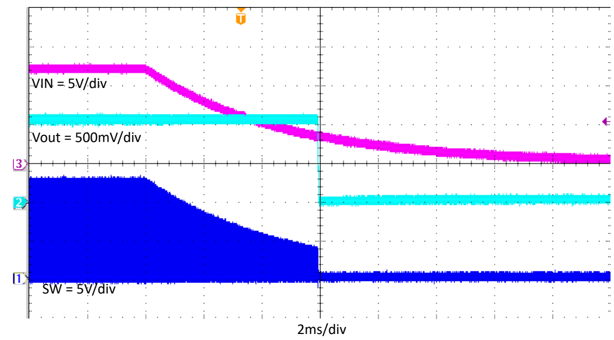


図 7-17. TPS562203 Power Off With 2A Loading

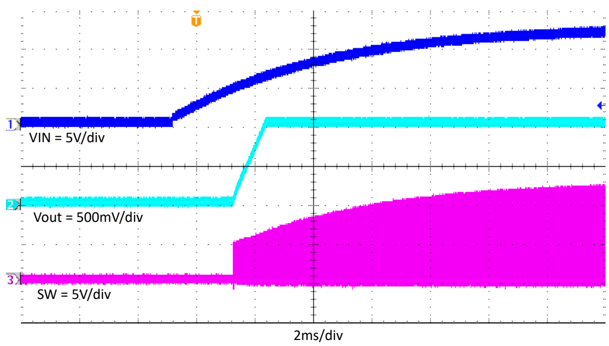


図 7-18. TPS562206 Power On With 2A Loading

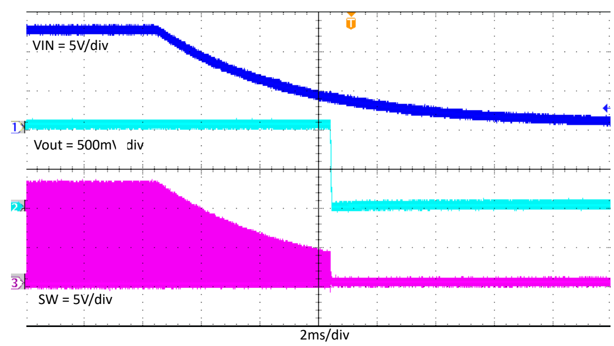


図 7-19. TPS562206 Power Off With 2A Loading

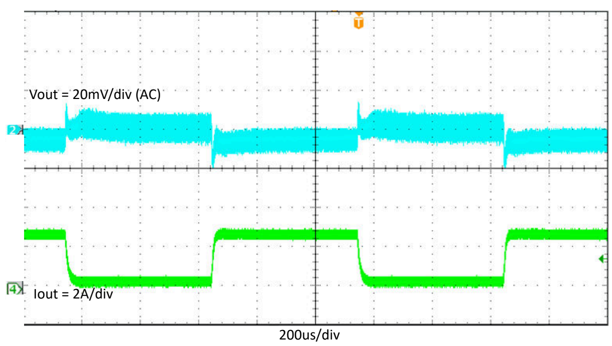


図 7-20. TPS562203 Load Transient With 0A to 2A

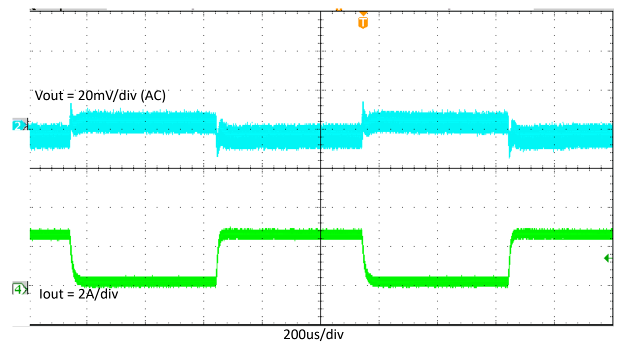


図 7-21. TPS562206 Load Transient With 0A to 2A

7.3 Power Supply Recommendations

TPS56220x are designed to operate from input supply voltages in the range of 4.2V to 17V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum duty is 95%.

7.4 Layout

7.4.1 Layout Guidelines

1. Make VIN and GND traces as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. connect a separate VOUT path to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Place a voltage feedback loop away from the high-voltage switching trace, and preferably has ground shield.
9. Make the trace of the FB node as small as possible to avoid noise coupling.
10. Make the GND trace between the output capacitor and the GND pin as wide as possible to minimize trace impedance.

7.4.2 Layout Example

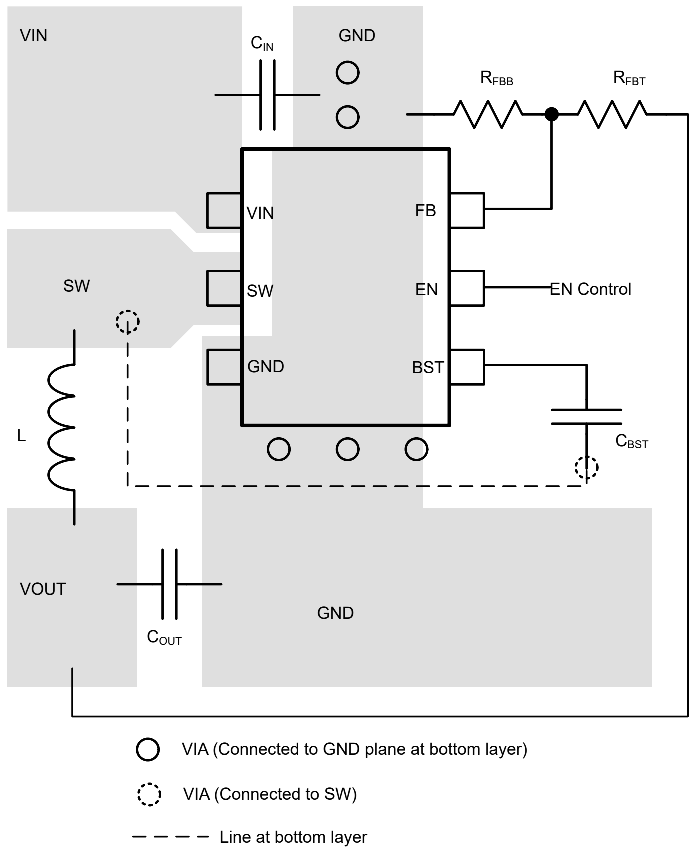


図 7-22. TPS562203 Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS562203 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS562206 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
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The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

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- Export customized schematic and layout into popular CAD formats
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8.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

Changes from Revision * (June 2023) to Revision A (January 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS562203DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	2203
TPS562203DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2203
TPS562203DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	2203
TPS562206DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	2206
TPS562206DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2206
TPS562206DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	2206

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

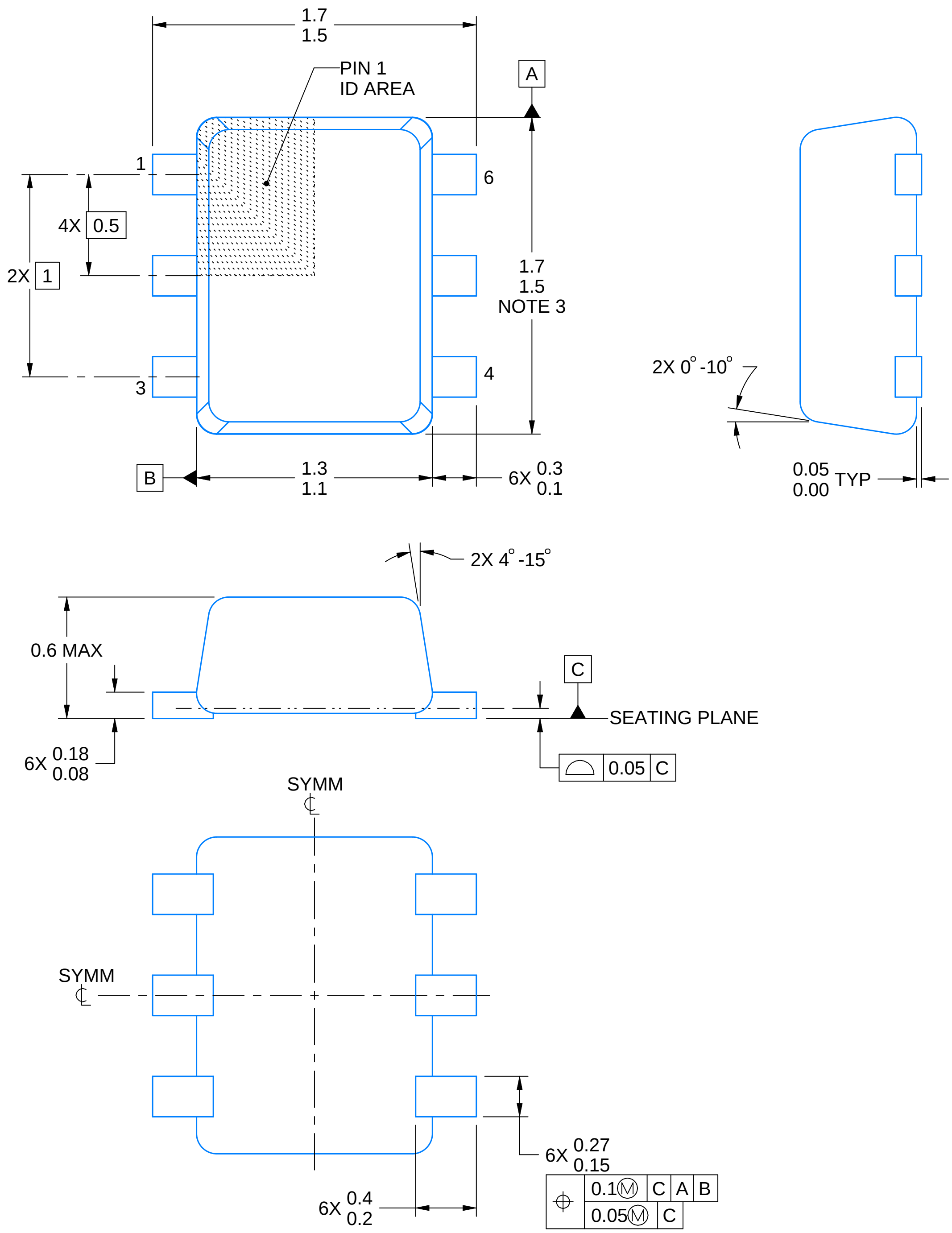
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



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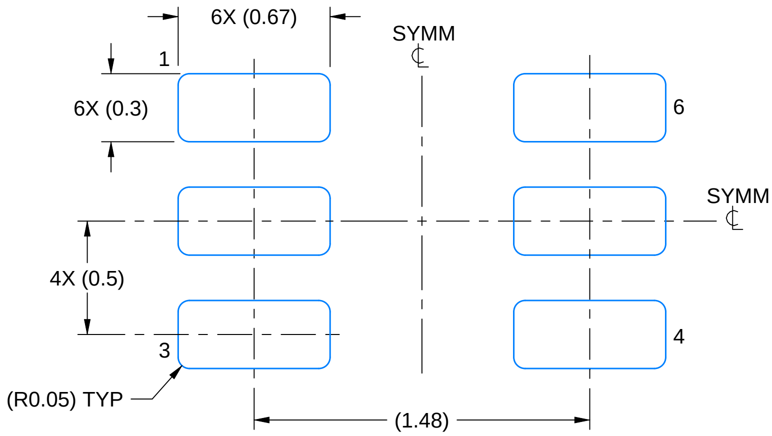
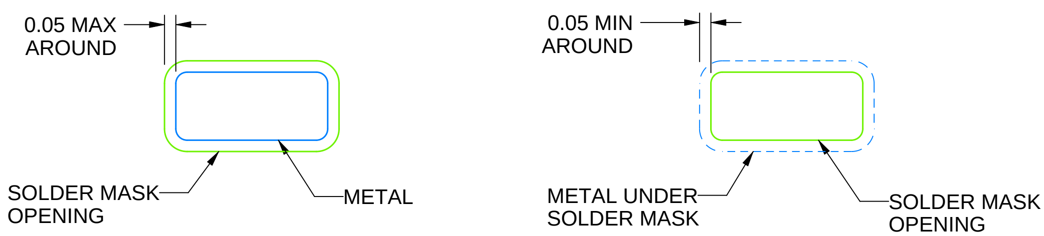
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDERMASK DETAILS

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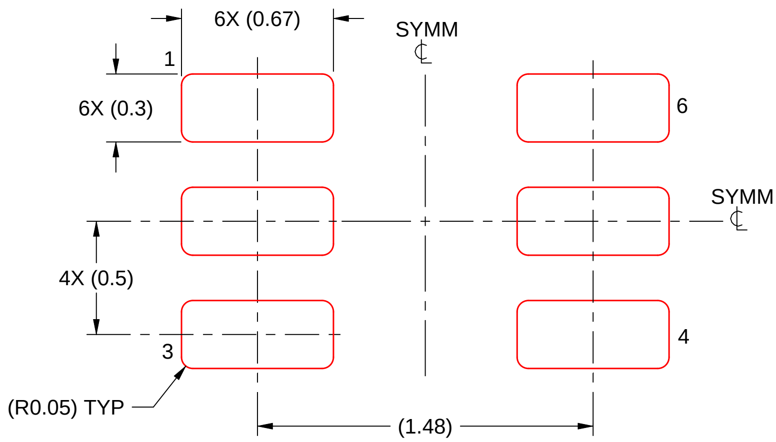
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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