TEXAS INSTRUMENTS
TPS560200-Q1
JAJSHA1B – APRIL 2016 – REVISED MAY 2019

TPS560200-Q1 4.5V～17V 入力、500mA 同期整流降圧コンバータ、高性能 Eco-mode™ 付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
  - 温度範囲:グレード 1、-40℃～+125℃
  - HBM ESD 分類:H2
  - CDM ESD分類:C4B
- モノリシック 0.95Ω ハイサイドおよび 0.33Ω ローサイド MOSFET を内蔵
- 500mA の連続出力電流
- 出力電圧範囲: 0.8V～6.5V
- 0.8V の基準電圧、温度範囲全体にわたって ±1.3% の精度
- 自動スキップ高性能 Eco-mode™により軽負荷時に高効率を実現
- D-CAP2™モードにより高速な過渡応答が可能
- 外部補償が不要
- 600kHz のスイッチング周波数
- 2ms の内部ソフトスタート
- プリバイアスした VOUT への安全なスタートアップ
- サーマル・シャットダウン
- 動作時の接合部温度範囲：-40℃～125℃
- 8 ピンの MSOP パッケージで供給

2 アプリケーション

- 電気自動車 (EV) の充電ステーション
- インフォテインメント・システム

3 概要

TPS560200-Q1 は、MOSFET を内蔵した 17V、500mA、低 Iq、適応型オン時間 D-CAP2 モードの同期整流モノリシック降圧コンバータであり、使いやすい 8 ピン MSOP パッケージに搭載されています。

TPS560200-Q1 を採用することで、各種最終製品の電源バス・レギュレータに対して、コスト効率の優れた、部品数の少ない、低スタンバイ電流のソリューションを実現できます。本デバイスの主制御ループは、外部補償部品なしで高速な過渡応答が得られる D-CAP2 モード制御を使用しています。適応型オン時間制御により、重負荷時には PWM モード動作、軽負荷時には高性能 Eco-Mode 動作へシームレスに移行できます。

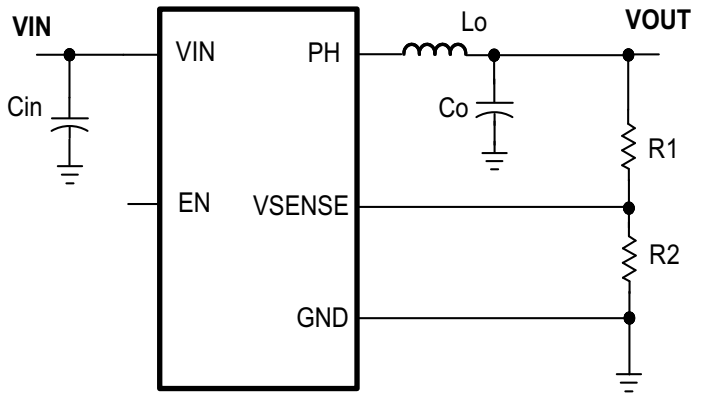
また TPS560200-Q1 には、POSCAP/SP-CAP などの低 ESR (等価直列抵抗) 出力コンデンサだけでなく、超低 ESR のセラミック・コンデンサにも対応できる、独自の回路が採用されています。このデバイスは、4.5V～17V の VIN 入力で動作します。出力電圧は、0.8V～6.5V の範囲でプログラムできます。ソフト・スタート時間は 2ms 固定です。このデバイスは、8 ピン MSOP パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS560200-Q1	VSSOP (8)	3.00mm x 3.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

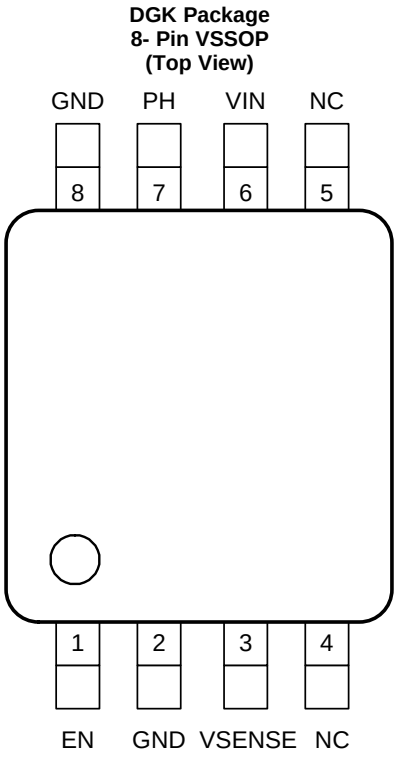
Revision A (May 2016) から **Revision B** に変更 **Page**

- 編集上の変更のみ、技術上の変更なし ... 1

2016年4月 発行のものから更新 **Page**

- デバイスのステータスを「プレビュー」から「量産」に変更 ... 1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Float to enable
GND	2, 8	—	Return for control circuitry and low-side power MOSFET
VSENSE	3	I	Converter feedback input. Connect to output voltage with feedback resistor divider
NC	4, 5	—	No connection inside, can be connected to any node or can be floating
VIN	6	I	Supplies the control circuitry of the power converter
PH	7	O	The switch node

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	19	V
	EN	–0.3	7	V
	VSENSE	–0.3	3	V
Output voltage	PH	–0.6	19	V
	PH 10-ns transient	–2	21	V
Source current	EN		±100	µA
	PH	Current limit		A
Sink current	PH	Current limit		A
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all –2000, 2000 pins(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011, all pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage range	4.5	17	V
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS560200-Q1 DGK (VSSOP) 8 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	106.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	104.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, VIN = 4.5 V to 17 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
VIN Operating input voltage		4.5		17	V
VIN Internal UVLO wakeup	VIN Rising		4.35	4.5	V
VIN Internal UVLO shutdown	VIN Fallling	3.9	4.15		V
VIN Shutdown supply current	EN = 0 V, V_{IN} = 12 V	2.0	3.7	9	µA
VIN Operating – non switching supply current	VSENSE = 850 mV, V_{IN} = 12 V	35	60	95	µA
ENABLE (EN PIN)					
Enable threshold	Rising		1.16	1.29	V
	Falling	1.05	1.13		V
Internal Soft-Start	VSENSE ramps from 0 V to 0.8 V		2		ms
OUTPUT VOLTAGE					
Voltage reference	25°C, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 5 mA, Pulse-Skipping	0.796	0.804	0.812	V
	25°C, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 100 mA, Continuous current mode	0.792	0.800	0.808	V
	V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 100 mA, Continuous current mode	0.789	0.800	0.811	V
MOSFET					
High-side switch resistance(1)	V_{IN} = 12 V	0.50	0.95	1.50	Ω
Low-side switch resistance(1)	V_{IN} = 12 V	0.20	0.33	0.55	Ω
CURRENT LIMIT					
Low-side switch sourcing current limit	L_{OUT} = 10 µH, Valley current, V_{OUT} = 1.05 V	570	670	795	mA
THERMAL SHUTDOWN					
Thermal shutdown			160		°C
Thermal shutdown hysteresis			10		°C
ON-TIME TIMER CONTROL					
On time	V_{IN} = 12 V	130	165	200	ns
Minimum off time	25°C, VSENSE = 0.5 V		250	400	ns
OUTPUT UNDERVOLTAGE PROTECTION					
Output UVP threshold	Falling	56	63	69	%VREF
Hiccup time			15		ms

(1) Not production tested

6.6 Typical Characteristics

V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).

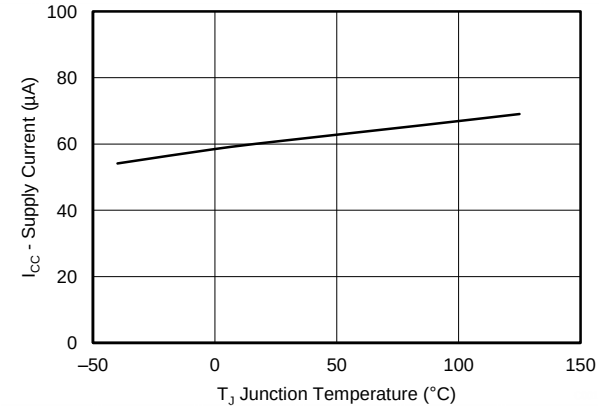


図 1. Supply Current vs Junction Temperature

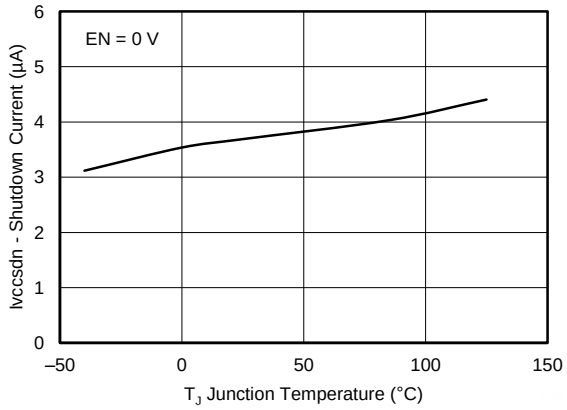


図 2. Shutdown Current vs Junction Temperature

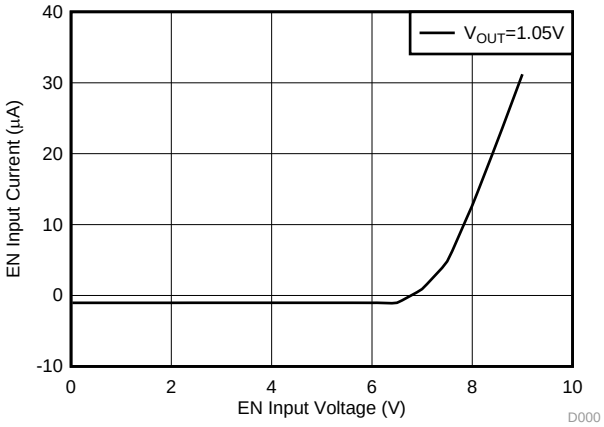


図 3. EN Input Current vs EN Input Voltage

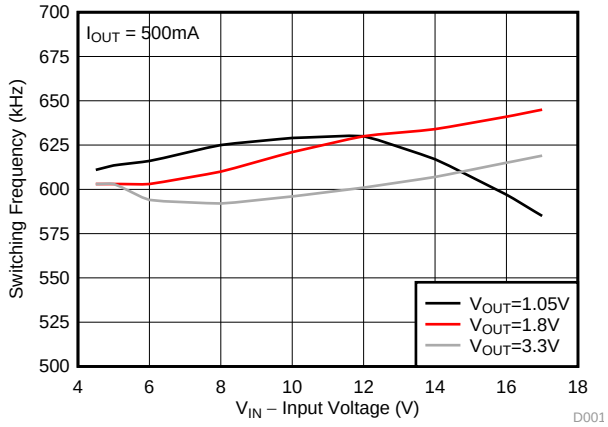


図 4. Switching Frequency vs Input Voltage

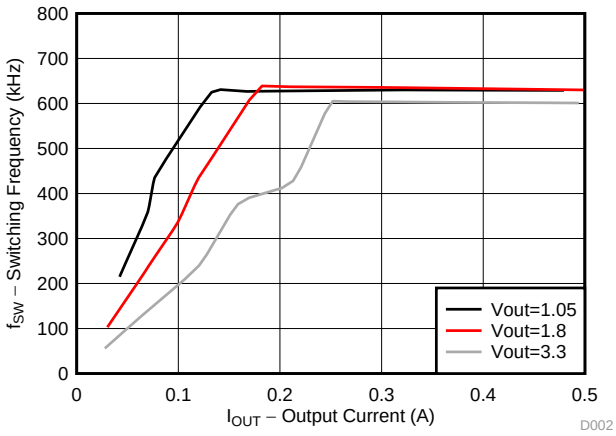


図 5. Switching Frequency vs Output Current

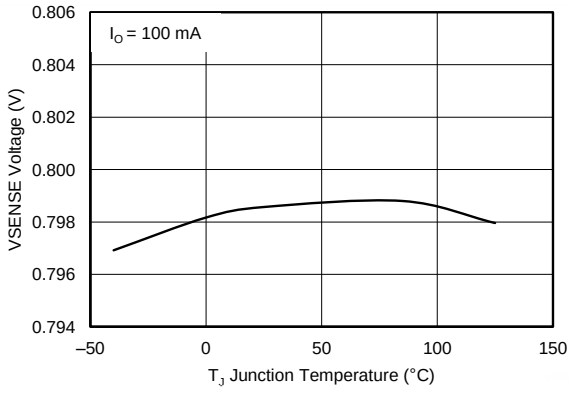


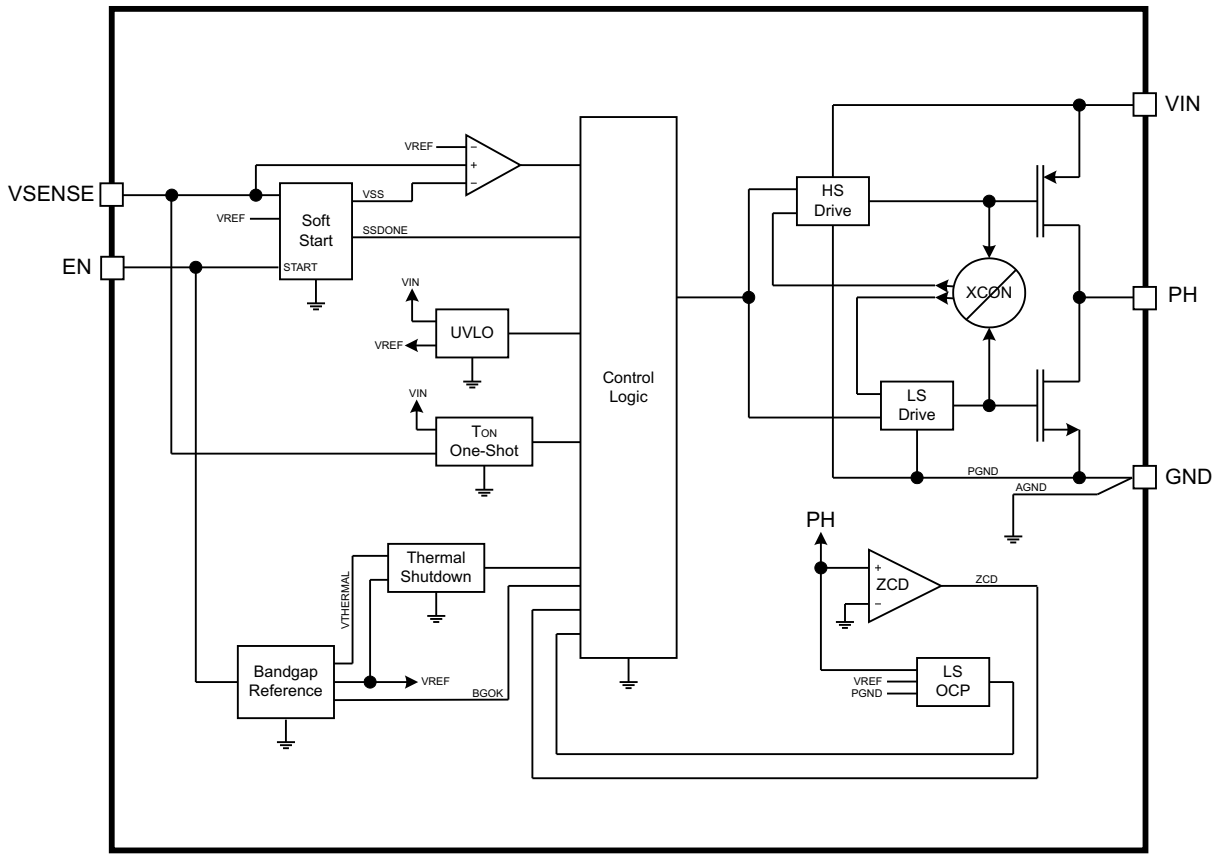
図 6. VSENSE Voltage vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS560200-Q1 is a 500-mA synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2 mode control. The fast transient response of D-CAP2 control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS560200-Q1 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VOUT, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

Feature Description (continued)

7.3.2 PWM Frequency and Adaptive On-Time Control

TPS560200-Q1 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS560200-Q1 runs with a pseudo-constant frequency of 600 kHz by using the input voltage and output voltage to set the on-time, one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

7.3.3 Advanced Auto-Skip Eco-Mode Control

The TPS560200-Q1 is designed with advanced auto-skip Eco-Mode to increase higher light-load efficiency. As the output current decreases from heavy-load condition, the inductor current is also reduced. If the output current is reduced enough, the inductor current ripple valley reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying low-side MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept approximately the same as is in continuous conduction mode. The off-time increases as it takes more time to discharge the output capacitor to the level of the reference voltage with smaller load current. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in 式 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times fsw} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.4 Soft-Start and Prebiased Soft-Start

The TPS560200-Q1 has an internal 2-ms soft-start. When the EN pin becomes high, internal soft-start function begins ramping up the reference voltage to the PWM comparator.

The TPS560200-Q1 contains a unique circuit to prevent current from being pulled from the output during start-up if the output is prebiased. When the soft-start commands a voltage higher than the prebias level (internal soft-start becomes greater than feedback voltage V_{VSENSE}), the controller slowly activates synchronous rectification by starting the first low-side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the prebias output, and ensure that the out voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from prebiased start-up to normal mode operation.

7.3.5 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the PH pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. The TPS560200-Q1 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each switching cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The peak current is the average load current plus one half of the peak-to-peak inductor current. The valley current is the average load current minus one half of the peak-to-peak inductor current. Because the valley current is used to detect the overcurrent threshold, the load current is higher than the overcurrent threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This protection is nonlatching. When the VSENSE voltage becomes lower than 63% of the target voltage, the UVP comparator detects it. After 7 µs detecting the UVP voltage, device shuts down and re-starts after hiccup time.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

Feature Description (continued)

7.3.6 Thermal Shutdown

TPS560200-Q1 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 160°C), the device is shut off. This is nonlatch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS560200-Q1 can operate in its normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS560200-Q1 operates at a quasi-fixed frequency of 600 kHz.

7.4.2 Eco-Mode Operation

When the TPS560200-Q1 is in the normal CCM operating mode and the switch current falls to 0 A, the TPS560200-Q1 begins operating in pulse-skipping Eco-Mode. Each switching cycle is followed by a period of energy-saving sleep time. The sleep time ends when the VFB voltage falls below the Eco-Mode threshold voltage. As the output current decreases the perceived time between switching pulses increases.

7.4.3 Standby Operation

When the TPS560200-Q1 is operating in either normal CCM or Eco-Mode, it may be placed in standby by asserting the EN pin low.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS560200-Q1 is used as a step-down converter which converts a voltage of 4.5 V to 17 V to a lower voltage. WEBENCH® software is available to aid in the design and analysis of circuits.

8.2 Typical Application

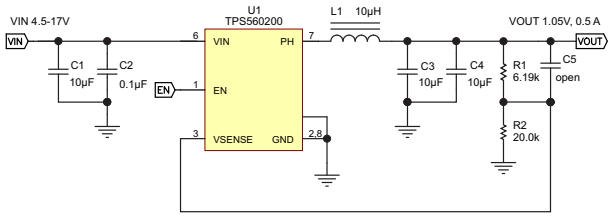


図 7. Typical Application Schematic

8.2.1 Design Requirements

For this design example, refer to the application parameters shown in 表 1.

表 1. Design Parameters

PARAMETER	VALUES
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	500 mA
Output voltage ripple	30 mV/pp

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using 1% tolerance or better divider resistors. Start by using 式 2 to calculate V_{OUT}.

To improve efficiency at light loads, consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VSENSE input current are more noticeable.

$$R2 = \frac{R1 \times 0.8\ V}{V_{OUT} - 0.8V} \quad (2)$$

8.2.2.2 Output Filter Selection

The output filter used with the TPS560200-Q1 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS560200-Q1. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of 式 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 2.

表 2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C5 (pF)	L1 (µH)			C3 + C4 (µF)
				MIN	TYP	MAX	
1.0	4.99	20.0			10		10 + 10
1.05	6.19	20.0			10		10 + 10
1.2	10.0	20.0			10		10 + 10
1.5	17.4	20.0			10		10 + 10
1.8	24.9	20.0	optional		10		10 + 10
2.5	42.2	20.0	optional		10		10 + 10
3.3	61.9	20.0	optional		10		10 + 10
5.0	105	20.0	optional		10		10 + 10

Because the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. Additional phase boost can be achieved by adding a feed-forward capacitor (C5) in parallel with R1. The feed-forward capacitor is most effective for output voltages at or above 1.8 V.

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using 式 4, 式 5, and 式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 600 kHz for f_{SW}.

Use 600 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 式 5 and the RMS current of 式 6.

$$I_{LPP} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_{OUT} \times fsw} \quad (4)$$

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (5)$$

$$I_{L_{OUT}(RMS)} = \sqrt{I_{OUT}^2 + \frac{1}{12} I_{LPP}^2} \quad (6)$$

For this design example, the calculated peak current is 0.582 A and the calculated RMS current is 0.502 A. The inductor used is a Würth 744777910 with a peak current rating of 2.6 A and an RMS current rating of 2 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS560200-Q1 is intended for use with ceramic or other low-ESR capacitors. The recommended values are given in 表 2. Use 式 7 to determine the required RMS current rating for the output capacitor.

$$I_{C_{OUT}(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times fsw} \quad (7)$$

For this design two MuRata GRM32DR61E106KA12L 10-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.047 A and each output capacitor is rated for 3 A.

8.2.2.3 Input Capacitor Selection

The TPS560200-Q1 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1-µF capacitor (C2) from pin 6 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

8.2.3 Application Curves

V_{IN} = 12 V, V_{OUT} = 1.05 V, T_A = 25°C (unless otherwise noted).

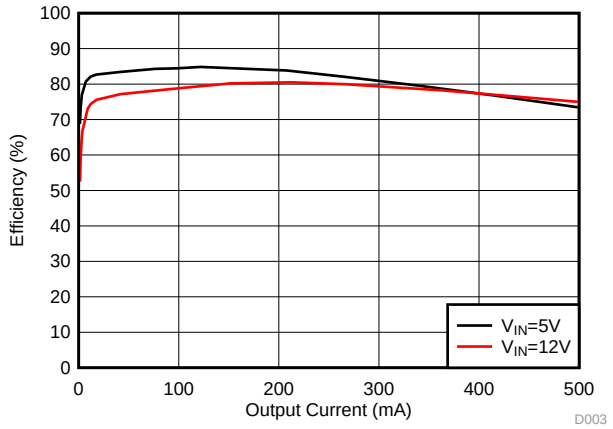


図 8. Efficiency

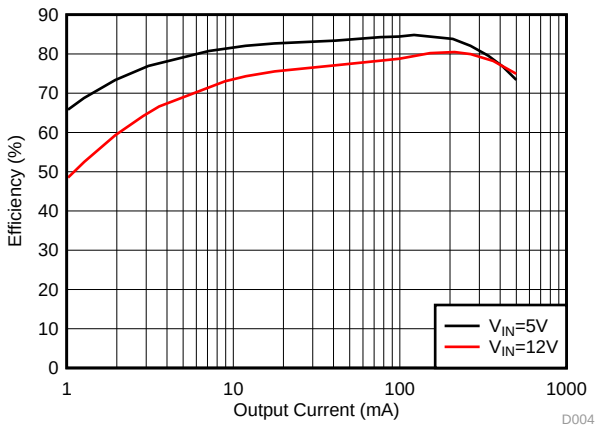


図 9. Light-Load Efficiency

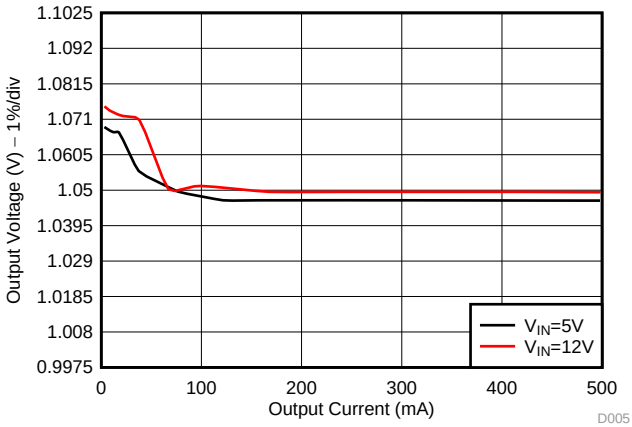


図 10. Load Regulation

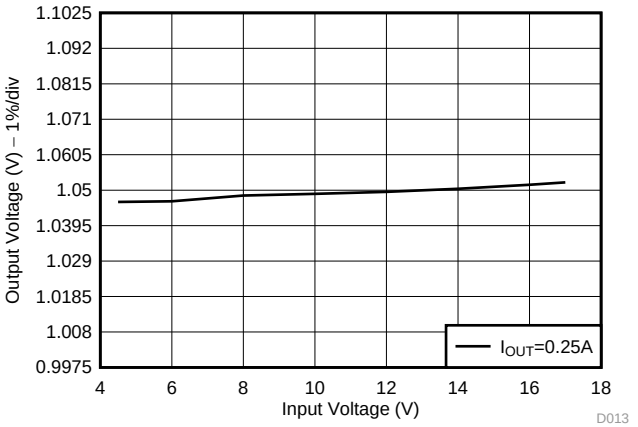


図 11. Line Regulation

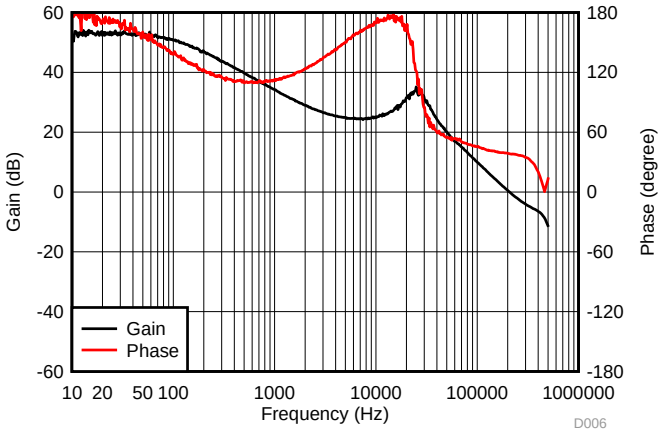


図 12. Loop Response, I_{OUT} = 0.25 A

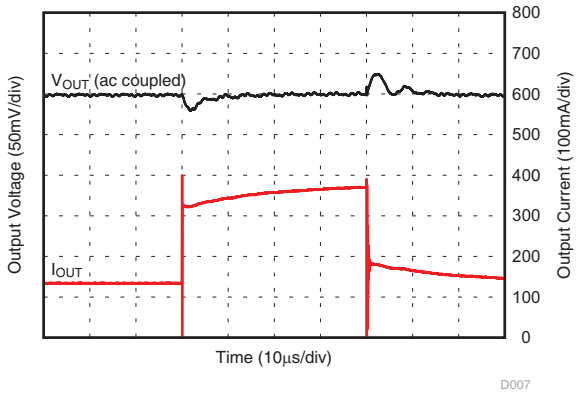


図 13. Transient Response, 25% to 75% Load Step

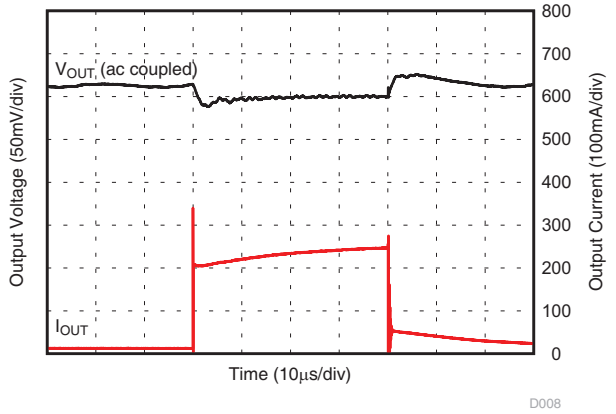


図 14. Transient Response, 2% to 50% Load Step

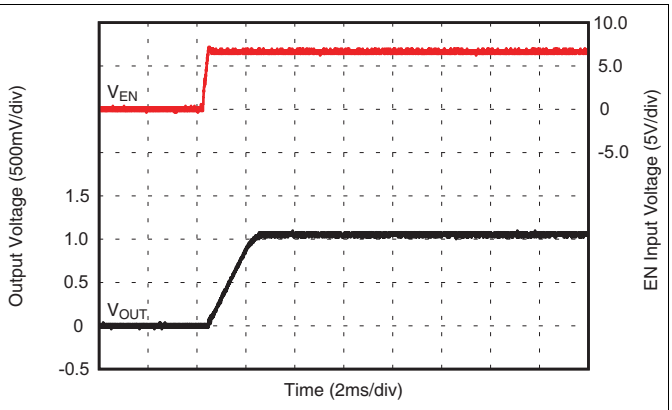


図 15. Start-Up Relative to EN

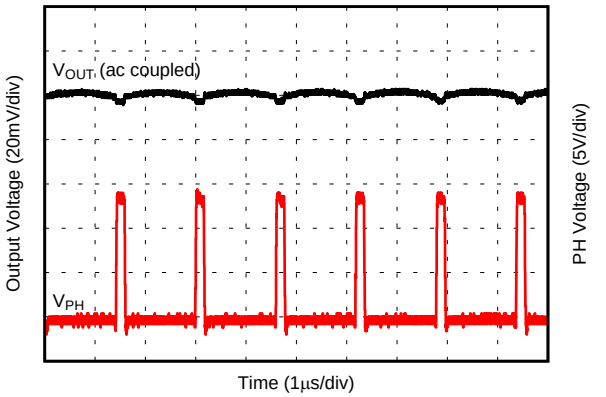


図 16. Output Ripple, I_{OUT} = 500 mA

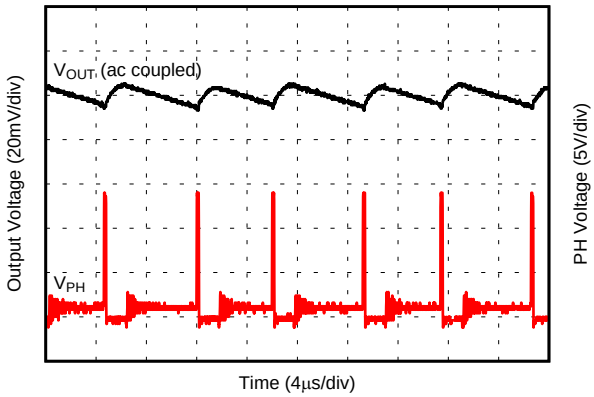


図 17. Output Ripple, I_{OUT} = 30 mA

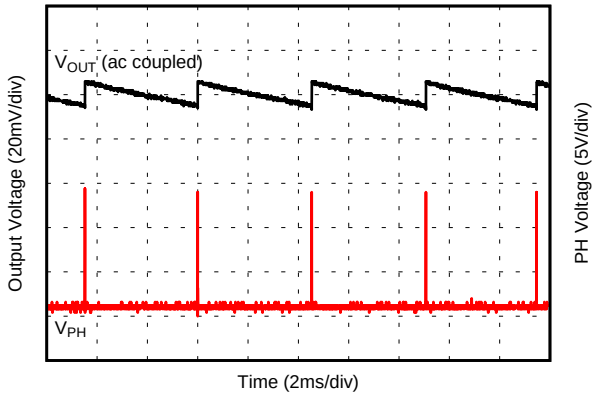


図 18. Output Ripple, I_{OUT} = 0 mA

9 Power Supply Recommendations

The TPS560200-Q1 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is VO / 0.75.

10 Layout

10.1 Layout Guidelines

The VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor. Take care to minimize the loop area formed by the bypass capacitor connection, the VIN pin, and the GND pin of the IC. The typical recommended bypass capacitance is 10-μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN and GND pins of the device. An additional high-frequency bypass capacitor may be added. See for a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the IC. The PH pin should be routed to a small copper area directly adjacent to the pin. Make the circulating loop from PH to the output inductor, output capacitors and back to GND as tight as possible while preserving adequate etch width to reduce conduction losses in the copper. Use vias adjacent to the IC to tie top-side ground copper plane to the internal or bottom layer ground planes. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate layout schemes; however, this layout produced good results and is intended as a guideline.

10.2 Layout Example

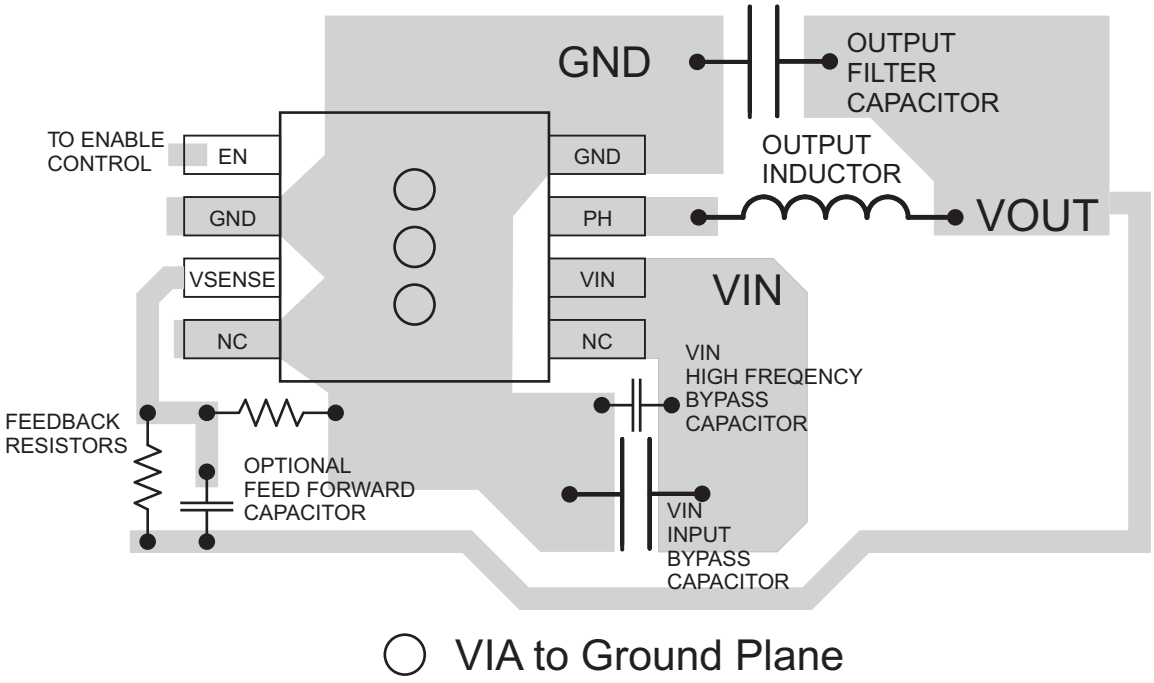


図 19. Layout Schematic

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商標

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WEBENCH is a registered trademark of Texas Instruments.
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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS560200QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKTQ1	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKTQ1.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKTQ1.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS560200-Q1 :

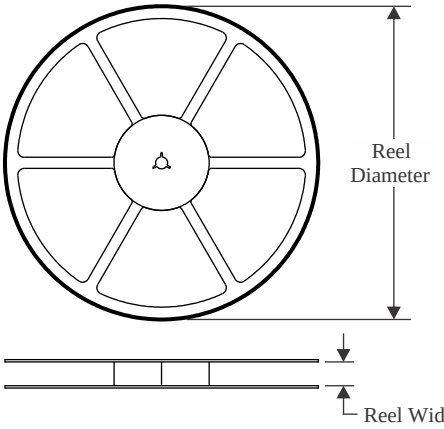
- Catalog : TPS560200

NOTE: Qualified Version Definitions:

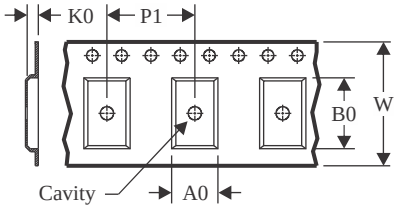
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

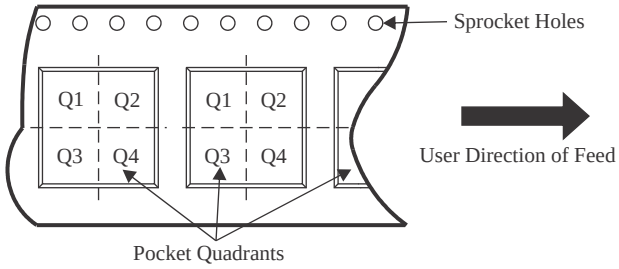


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

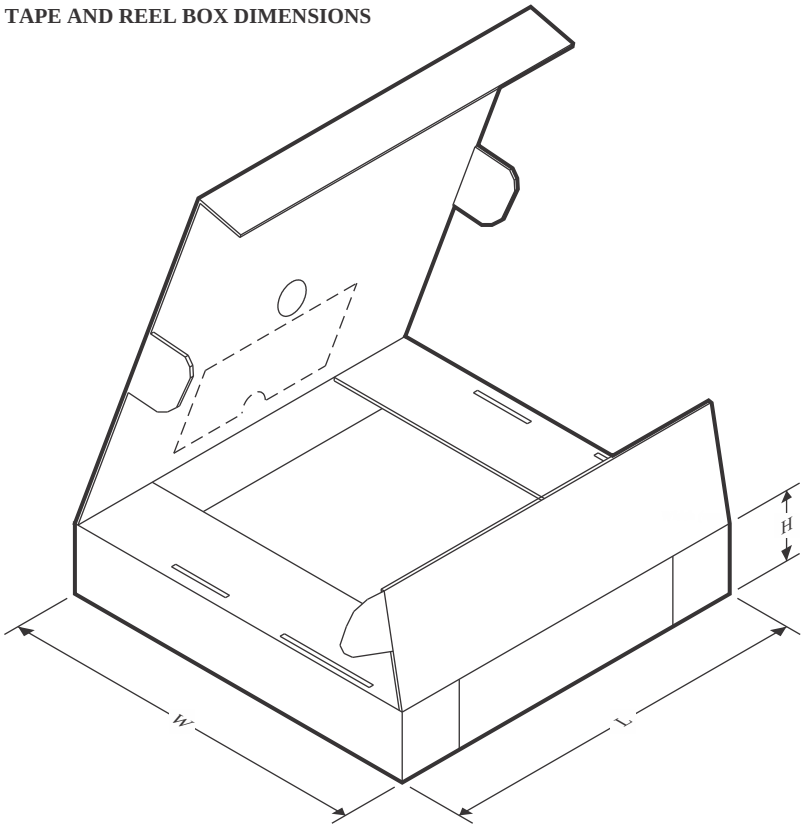
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS560200QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS560200QDGKTQ1	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS560200QDGKTQ1	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

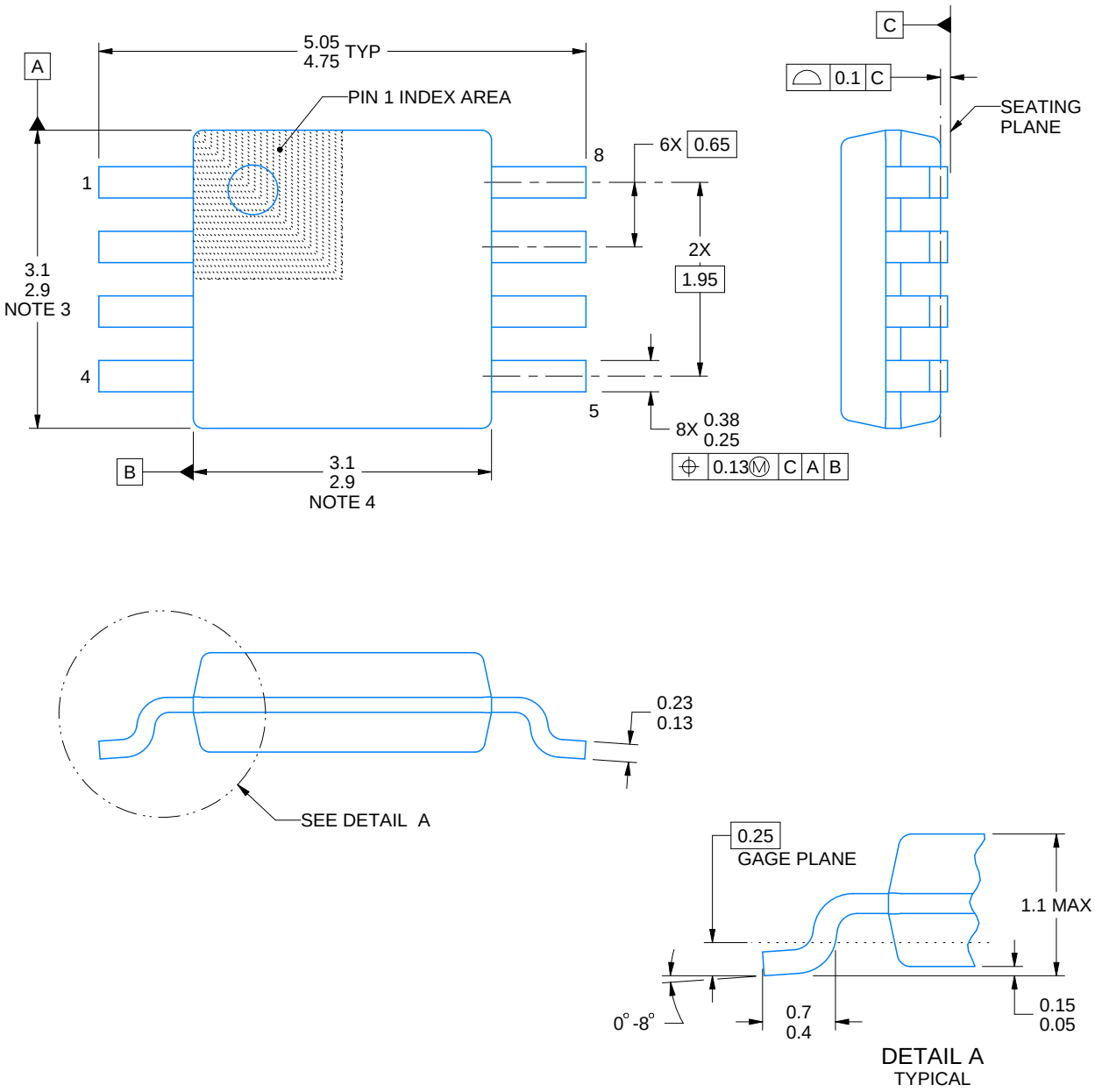
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS560200QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TPS560200QDGKTQ1	VSSOP	DGK	8	250	353.0	353.0	32.0
TPS560200QDGKTQ1	VSSOP	DGK	8	250	366.0	364.0	50.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

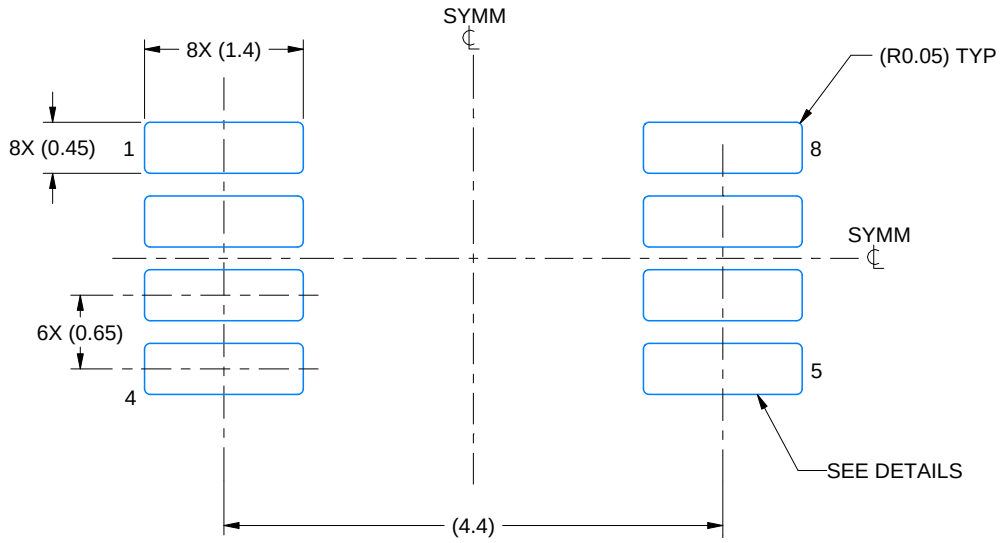
SMALL OUTLINE PACKAGE



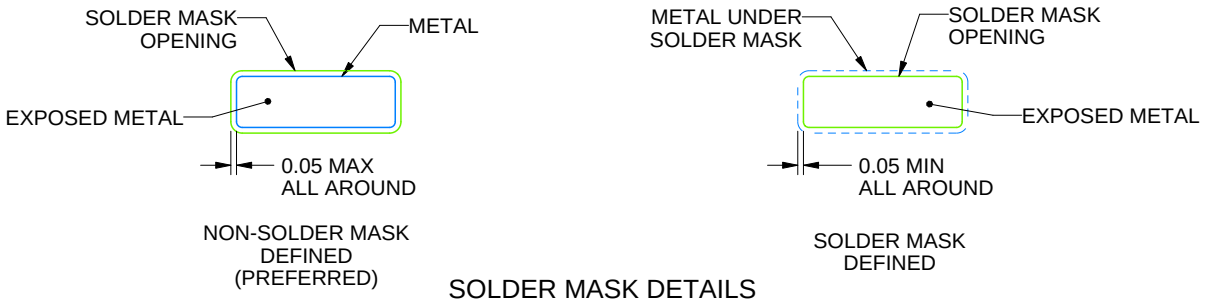
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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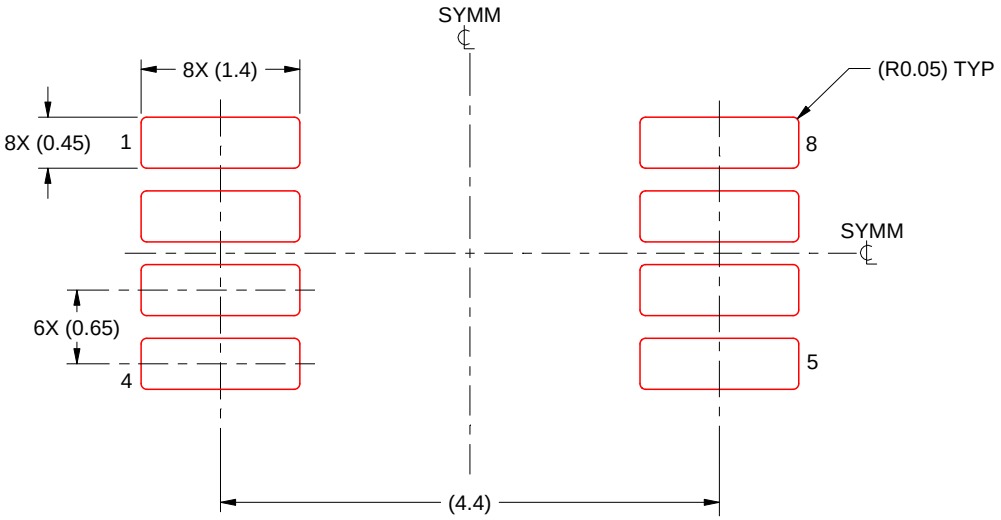
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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