TPS549B22 1.5V～18V V_{IN}、4.5V～22V V_{DD}、25A SWIFT™ 整流降圧コンバータ、完全差動センス機能と PMBus® 付き

1 特長

- 入力電圧 (PV_{IN}):1.5V～18V
- 入力バイアス電圧 (V_{DD}) 範囲:4.5V～22V
- 出力電圧範囲:0.6V～5.5V
- 4.1mΩ および 1.9mΩ のパワー MOSFET を内蔵し、25A の連続出力電流に対応
- 基準電圧は VSEL ピンを使用して 0.6V～1.2V に 50mV 刻みで設定可能
- 精度 ±0.5% の 0.9V_{REF}:接合部温度 –40℃～+125℃
- 真の差動リモート センス アンプ
- D-CAP3™ 制御モード
- 8 つの PMBus® 周波数を設定可能なアダプティブ オンタイム制御:315kHz、425kHz、550kHz、650kHz、825kHz、900kHz、1.025MHz、1.125MHz
- R_{ILIM} と OC クランプ付きで、温度補償済みのプログラマブルな電流制限
- ヒカップまたはラッチオフの OVP/UVP を選択可能
- 高精度の EN による V_{DD} UVLO の外部調整
- プリバイアス スタートアップのサポート
- Eco-mode と FCCM を選択可能
- フォルト保護および PGOOD 機能を完備
- 標準の VOUT_COMMAND および VOUT_MARGIN (HIGH および LOW)
- ピン ストラッピングおよび即時プログラミング
- フォルト通知と警告
- 選択したコマンドの NVM へのバックアップ
- PEC および SMB_ALRT# 付きの 1MHz PMBus
- WEBENCH® Power Designer により、TPS549B22 を使用するカスタム設計を作成

2 アプリケーション

- エンタープライズ ストレージ、SSD、NAS
- ワイヤレスおよび有線の通信インフラストラクチャ
- 産業用 PC、オートメーション、ATE、PLC、ビデオ監視
- エンタープライズ サーバー、スイッチ、ルータ
- ASIC、SoC、FPGA、DSP コア、I/O レール

3 概要

TPS549B22 デバイスは小型のシングル降圧型コンバータで、アダプティブ オンタイム D-CAP3 モード制御機能が搭載されています。高精度、高効率、高速な過渡応答、使いやすさ、外付け部品数の少なさ、容積の削減が要求される電源システム用に設計されています。

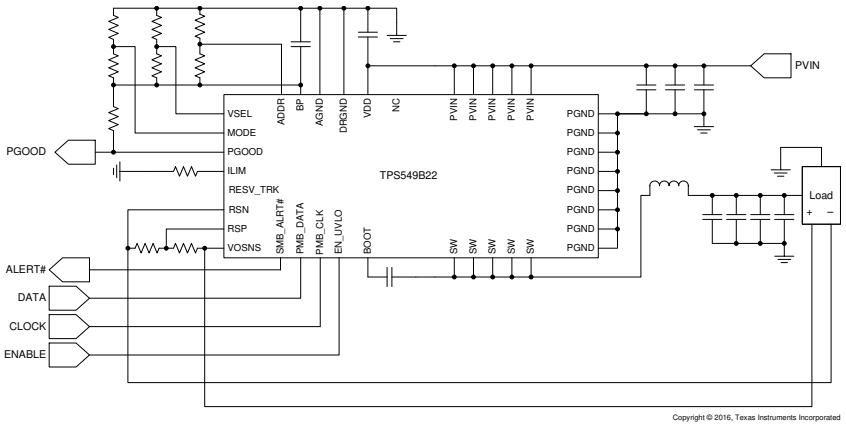
このデバイスには、完全な差動センスと、ハイサイド オン抵抗が 4.1mΩ、ローサイド オン抵抗が 1.9mΩ であるテキサス・インスツルメンツの統合 FET が搭載されています。また、0.5%、0.9V の高精度の基準電圧が搭載されており、-40℃～+125℃までの周囲温度に対応しています。競争優位性の高い特長として、外付け部品数が非常に少ないこと、正確な負荷レギュレーションおよびライン レギュレーション、オートスキップまたは FCCM モードでの動作、内部的なソフトスタート制御が挙げられます。

TPS549B22 デバイスは、7mm×5mm の 40 ピン LQFN-CLIP (RVF)パッケージで供給されます(RoHS 指令対象外)。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS549B22	RVF (LQFN-CLIP、40)	7.00mm × 5.00mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション概略図

Table of Contents

4 Pin Configuration and Functions

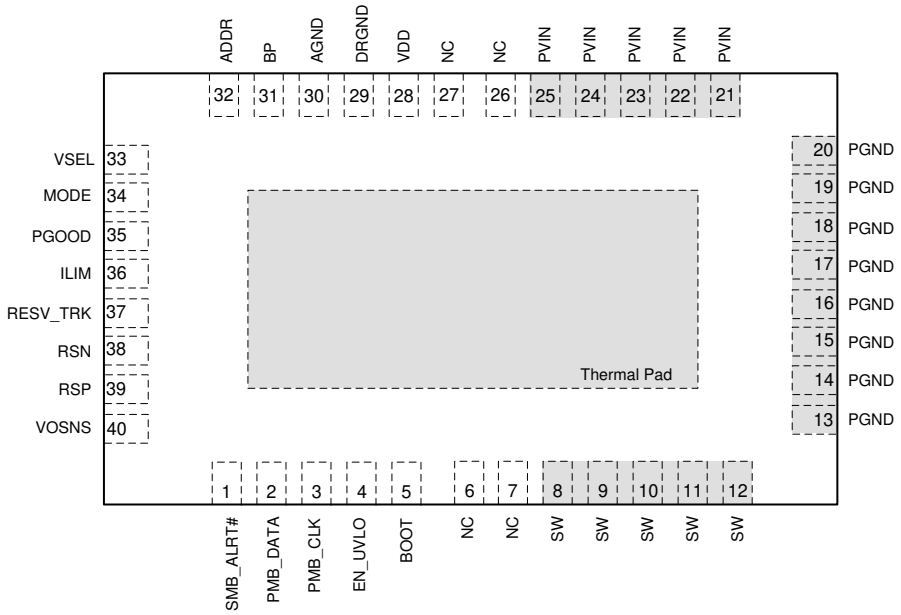


図 4-1. RVF Package 40-Pin LQFN-CLIP With Thermal Pad Top View

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
ADDR	32	I	Program device address and SKIP or FCCM mode.
AGND	30	G	Ground pin for internal analog circuits.
BOOT	5	P	Supply rail for high-side gate driver (boot terminal). Connect boot capacitor from this pin to SW node. Internally connected to BP via bootstrap PMOS switch.
BP	31	O	LDO output
DRGND	29	P	Internal gate driver return.
EN_UVLO	4	I	Enable pin that can turn on the DC/DC switching converter. Use also to program the required PVIN UVLO when PVIN and VDD are connected together.
ILIM	36	I/O	Program overcurrent limit by connecting a resistor to ground.
MODE	34	I	Mode selection pin. Select the control mode, and soft-start timing selection.
NC	6, 7, 26, 27		No connect.
PGND	13, 14, 15, 16, 17, 18, 19, 20	P	Power ground of internal FETs.
PGOOD	35	O	Open drain power-good status signal.
PMB_CLK	3	I	Clock input for the PMBus interface.
PMB_DATA	2	I/O	Data I/O for the PMBus interface.
PVIN	21, 22, 23, 24, 25	P	Power supply input for integrated power MOSFET pair.
RSN	38	I	Inverting input of the differential remote sense amplifier.
RSP	39	I	Non-inverting input of the differential remote sense amplifier.
RESV_TRK	37	I	Do not connect.
SMB_ALRT#	1	O	$\overline{\text{Alert}}$ output for the PMBus interface.
SW	8, 9, 10, 11, 12	I/O	Output switching terminal of power converter. Connect the pins to the output inductor.

表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VDD	28	P	Controller power supply input.
VOSNS	40	I	Output voltage monitor input pin.
VSEL	33	I	Program the initial start-up and or reference voltage without feedback resistor dividers (from 0.6 V to 1.2 V in 50-mV increments).

(1) I = input, O = output, G = GND

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
Input voltage	PVIN		–0.3	25	V
	VDD		–0.3	25	
	BOOT		–0.3	34	
	BOOT to SW	DC	–0.3	7.7	
		< 10 ns	–0.3	9	
	PMB_CLK, PMB_DATA		–0.3	6	
	EN_UVLO, VOSNS, MODE, ADDR, ILIM		–0.3	7.7	
	RSP, RESV_TRK, VSEL		–0.3	3.6	
	RSN		–0.3	0.3	
	PGND, AGND, DRGND		–0.3	0.3	
	SW	DC	–0.3	25	
		< 10 ns	–5	27	
Output voltage	PGOOD, BP		–0.3	7.7	V
Output voltage	SMB_ALRT#, PMB_DATA		–0.3	6	V
Junction temperature, T_J			–55	150	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Input voltage	PVIN with no snubber circuit: SW ringing peak voltage equals 23 V at 25-A output		1.5	14	V
	PVIN with snubber circuit: SW ringing peak voltage equals 23 V at 25-A output		1.5	18	
	VDD		4.5	22	
	BOOT		–0.1	24.5	
	BOOT to SW	DC	–0.1	6.5	
		< 10 ns	–0.1	7	
	PMB_CLK, PMB_DATA		–0.1	5.5	
	EN_UVLO, VOSNS, MODE, ADDR, ILIM		–0.1	5.5	
	RSP, RESV_TRK, VSEL		–0.1	3.3	
	RSN		–0.1	0.1	
	PGND, AGND, DRGND		–0.1	0.1	
	SW	DC	–0.1	18	
		< 10 ns	–5	27	
Output voltage	PGOOD, BP		–0.1	7	V
Output voltage	SMB_ALRT#, PMB_DATA		–0.1	5.5	V
Junction temperature, T_J			–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS549B22 RVF (LQFN-CLIP) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.96	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 12 V, V_{EN_UVLO} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
MOSFET ON-RESISTANCE ($R_{DS(on)}$)						
$R_{DS(on)}$	High-side FET	(V_{BOOT} – V_{SW}) = 5 V, I_D = 25 A, T_J = 25°C		4.1		mΩ
	Low-side FET	V_{VDD} = 5 V, I_D = 25 A, T_J = 25°C		1.9		mΩ
INPUT SUPPLY AND CURRENT						
V_{VDD}	VDD supply voltage	Nominal VDD voltage range	4.5		22	V
I_{VDD}	VDD bias current	No load, power conversion enabled (no switching), T_A = 25°C,		2		mA
$I_{VDDSTBY}$	VDD standby current	No load, power conversion disabled, T_A = 25°C		700		µA

5.5 Electrical Characteristics (続き)

over operating free-air temperature range, V_{VDD} = 12 V, V_{EN_UVLO} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT						
V_{VDD_UVLO}	VDD UVLO rising threshold		4.123	4.25	4.41	V
$V_{VDD\_UVLO(HYS)}$	VDD UVLO hysteresis			0.2		V
$V_{EN\_ON\_TH}$	EN_UVLO on threshold		1.45	1.6	1.75	V
V_{EN_HYS}	EN_UVLO hysteresis		270	300	340	mV
I_{EN_LKG}	EN_UVLO input leakage current	V_{EN_UVLO} = 5 V	–1	0	1	µA
INTERNAL REFERENCE VOLTAGE RANGE						
V_{INTREF}	Internal REF voltage			900.4		mV
$V_{INTREFTOL}$	Internal REF voltage tolerance	–40°C ≤ T_J ≤ 125°C	–0.5%		0.5%	
V_{INTREF}	Internal REF voltage range		0.6		1.2	V
OUTPUT VOLTAGE						
V_{IOS_LPCMP}	Loop comparator input offset voltage(1)		–2.5		2.5	mV
I_{RSP}	RSP input current	V_{RSP} = 600 mV	–1		1	µA
$I_{VO(dis)}$	VO discharge current	V_{VO} = 0.5 V, power conversion disabled	8	12		mA
DIFFERENTIAL REMOTE SENSE AMPLIFIER						
f_{UGBW}	Unity gain bandwidth(1)		5	7		MHz
A_0	Open loop gain(1)		75			dB
SR	Slew rate(1)			±4.7		V/µsec
V_{IRNG}	Input range(1)		–0.2		1.8	V
V_{OFFSET}	Input offset voltage(1)		–3.5		3.5	mV
INTERNAL BOOT STRAP SWITCH						
V_F	Forward voltage	$V_{BP-BOOT}$, I_F = 10 mA, T_A = 25°C		0.1	0.2	V
I_{BOOT}	VBST leakage current	V_{BOOT} = 30 V, V_{SW} = 25 V, T_A = 25°C		0.01	1.5	µA
SWITCHING FREQUENCY						
f_{SW}	VO switching frequency(2)	V_{IN} = 12 V, V_{VO} = 1 V, T_A = 25°C	275	315	350	kHz
			380	425	475	
			490	550	615	
			585	650	740	
			740	825	930	
			790	900	995	
			920	1025	1160	
			950	1125	1250	
$t_{ON(min)}$	Minimum on-time(1)			60		ns
$t_{OFF(min)}$	Minimum off-time(1)	DRVH falling to rising			300	ns

5.5 Electrical Characteristics (続き)

over operating free-air temperature range, V_{VDD} = 12 V, V_{EN_UVLO} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
MODE, VSEL, ADDR DETECTION							
V_{DETECT_TH}	MODE, VSEL, and ADDR detection voltage	V_{BP} = 2.93 V, R_{HIGH} = 100 kΩ	Open		V_{BP}		V
			R_{LOW} = 187 kΩ		1.9091		
			R_{LOW} = 165 kΩ		1.8243		
			R_{LOW} = 147 kΩ		1.7438		
			R_{LOW} = 133 kΩ		1.6725		
			R_{LOW} = 121 kΩ		1.6042		
			R_{LOW} = 110 kΩ		1.5348		
			R_{LOW} = 100 kΩ		1.465		
			R_{LOW} = 90.9 kΩ		1.3952		
			R_{LOW} = 82.5 kΩ		1.3245		
			R_{LOW} = 75 kΩ		1.2557		
			R_{LOW} = 68.1 kΩ		1.187		
			R_{LOW} = 60.4 kΩ		1.1033		
			R_{LOW} = 53.6 kΩ		1.0224		
			R_{LOW} = 47.5 kΩ		0.9436		
			R_{LOW} = 42.2 kΩ		0.8695		
			R_{LOW} = 37.4 kΩ		0.7975		
			R_{LOW} = 33.2 kΩ		0.7303		
			R_{LOW} = 29.4 kΩ		0.6657		
			R_{LOW} = 25.5 kΩ		0.5953		
			R_{LO}W = 22.1 kΩ		0.5303		
			R_{LOW} = 19.1 kΩ		0.4699		
			R_{LOW} = 16.5 kΩ		0.415		
			R_{LOW} = 14.3 kΩ		0.3666		
			R_{LOW} = 12.1 kΩ		0.3163		
			R_{LOW} = 10 kΩ		0.2664		
			R_{LOW} = 7.87 kΩ		0.2138		
			R_{LOW} = 6.19 kΩ		0.1708		
			R_{LOW} = 4.64 kΩ		0.1299		
			R_{LOW} = 3.16 kΩ		0.0898		
			R_{LOW} = 1.78 kΩ		0.0512		
			R_{LOW} = 0 Ω		GND		

5.5 Electrical Characteristics (続き)

over operating free-air temperature range, V_{VDD} = 12 V, V_{EN_UVLO} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
SOFT-START							
t_{SS}	Soft-start time	V_{OUT} rising from 0 V to 95% of final set point, R_{MODE_HIGH} = 100 kΩ	R_{MODE_LOW} = 60.4 kΩ	7	8[4]	10	ms
			R_{MODE_LOW} = 53.6 kΩ	3.6	4[5]	5.2	
			R_{MODE_LOW} = 47.5 kΩ	1.6	2	2.8	
			R_{MODE_LOW} = 42.2 kΩ	0.8	1	1.6	
POWER-ON DELAY							
t_{PODLY}	Power-on delay time	Delay from enable to switching POD[2:0] = 000			256		µs
		Delay from enable to switching POD[2:0] = 001			512		
		Delay from enable to switching POD[2:0] = 010			1.024		ms
		Delay from enable to switching POD[2:0] = 011			2.048		
		Delay from enable to switching POD[2:0] = 100			4.096		
		Delay from enable to switching POD[2:0] = 101			8.192		
		Delay from enable to switching POD[2:0] = 110			16.384		
		Delay from enable to switching POD[2:0] = 111			32.768		
PGOOD COMPARATOR							
V_{PGTH}	PGOOD threshold	PGOOD in from higher		105	108	111	%V_{REF}
		PGOOD in from lower		89	92	95	
		PGOOD out to higher			120		
		PGOOD out to lower			68		
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5 V			6.9		mA
t_{PGDLY}	PGOOD delay time	Delay for PGOOD going in, PGD[2:0] = 000			256		µs
		Delay for PGOOD going in, PGD[2:0] = 001			512		
		Delay for PGOOD going in, PGD[2:0] = 010			1.024		ms
		Delay for PGOOD going in, PGD[2:0] = 011			2.048		
		Delay for PGOOD going in, PGD[2:0] = 100			4.096		
		Delay for PGOOD going in, PGD[2:0] = 101			8.192		
		Delay for PGOOD going in, PGD[2:0] = 110			16.384		
		Delay for PGOOD going in, PGD[2:0] = 111			131		
		Delay for PGOOD coming out				2	µs
I_{PGLK}	PGOOD leakage current	V_{PGOOD} = 5 V		–1	0	1	µA
CURRENT DETECTION							
I_{OCL_VA}	Valley current limit threshold	R_{LIM} = 61.9 kΩ			30		A
		OC tolerance			±15%[3]		
		R_{LIM} = 51.1 kΩ			25		A
		OC tolerance			±15%[3]		
		R_{LIM} = 40.2 kΩ		17	20	23	A
$I_{OCL\_VA\_N}$	Negative valley current limit threshold	R_{LIM} = 61.9 kΩ			–30		A
		R_{LIM} = 51.1 kΩ			–25		
		R_{LIM} = 40.2 kΩ			–20		
I_{CLMP_LO}	Clamp current at V_{LIM} clamp at lowest	V_{ILIM_CLMP} = 0.1 V, T_A = 25°C			5		A
I_{CLMP_HI}	Clamp current at V_{LIM} clamp at highest	V_{ILIM_CLMP} = 1.2 V, T_A = 25°C			50		A

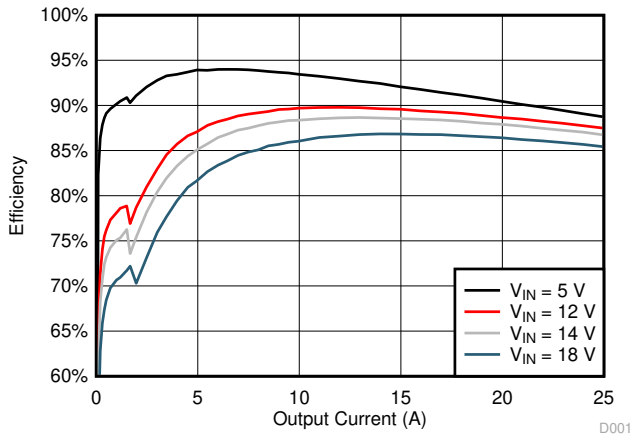
5.5 Electrical Characteristics (続き)

over operating free-air temperature range, V_{VDD} = 12 V, V_{EN_UVLO} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PROTECTIONS AND OOB						
V_{BPUVLO}	BP UVLO threshold voltage	Wake-up		3.32		V
		Shutdown		3.11		
V_{OVP}	OVP threshold voltage	OVP detect voltage	117%	120%	123%	V_{REF}
t_{OVPDLY}	OVP response time	100-mV over drive			1	µs
V_{UVP}	UVP threshold voltage	UVP detect voltage	65%	68%	71%	V_{REF}
t_{UVPDLY}	UVP delay filter delay time			1		ms
V_{OOB}	OOB threshold voltage			8%		V_{REF}
t_{HICDLY}	Hiccup blanking time	t_{SS} = 1 ms		16		ms
		t_{SS} = 2 ms		24		ms
		t_{SS} = 4 ms		38		ms
		t_{SS} = 8 ms		67		ms
BP VOLTAGE						
V_{BP}	BP LDO output voltage	V_{IN} = 12 V, 0 A ≤ I_{LOAD} ≤ 10 mA,		5.07		V
V_{BPDO}	BP LDO dropout voltage	V_{IN} = 4.5 V, I_{LOAD} = 30 mA, T_A = 25°C			365	mV
I_{BPMAX}	BP LDO overcurrent limit	V_{IN} = 12 V, T_A = 25°C		100		mA
PMB_CLK and PMB_DATA INPUT BUFFER LOGIC THRESHOLDS						
$V_{IL\text{-}PMBUS}$	PMB_CLK and PMB_DATA low-level input voltage(1)				0.8	V
$V_{IH\text{-}PMBUS}$	PMB_CLK and PMB_DATA high-level input voltage(1)		1.35			V
$V_{HY\text{-}PMBUS}$	PMB_CLK and PMB_DATA hysteresis voltage(1)			150		mV
PMB_CLK and SMB_ALRT OUTPUT PULLDOWN						
$V_{OL\text{-}PMBUS}$	PMB_DATA and SMB_ALRT low-level output voltage(1)	I_{SINK} = 20 mA			0.4	V
THERMAL SHUTDOWN						
T_{SDN}	Built-In thermal shutdown threshold(1)	Shutdown temperature	155	165		°C
		Hysteresis			30	

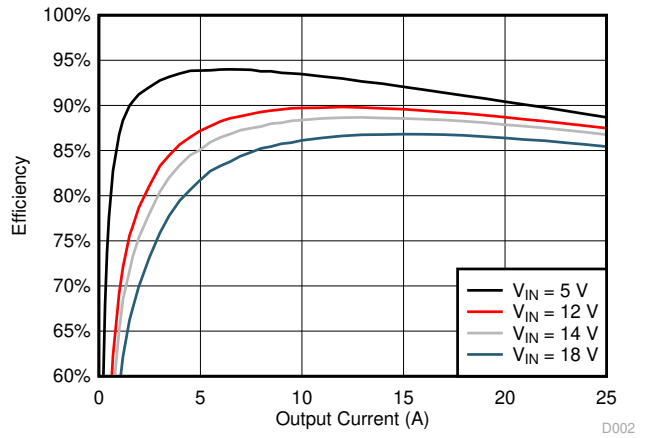
(1) Specified by design. Not production tested.
(2) Correlated with close-loop EVM measurement at load current of 30 A.
(3) Calculated from 20-A test data. Not production tested.
(4) To use the 8-ms SS setting, follow the steps outlined in *セクション 6.5.1.4*.
(5) To use the 4-ms SS setting, follow the steps outlined in *セクション 6.5.1.4*.

5.6 Typical Characteristics



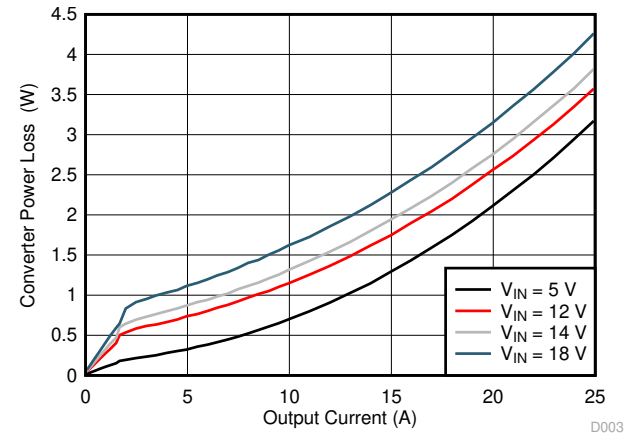
V_{OUT} = 1 V　　V_{DD} = V_{IN}　　SKIP Mode
f_{SW} = 650 kHz

図 5-1. Efficiency vs Output Current



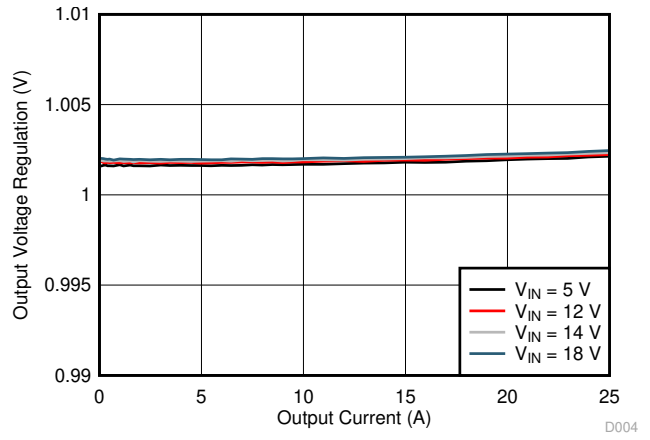
V_{OUT} = 1 V　　V_{DD} = V_{IN}　　FCCM Mode
f_{SW} = 650 kHz

図 5-2. Efficiency vs Output Current



V_{OUT} = 1 V　　V_{DD}= V_{IN}　　SKIP Mode
f_{SW} = 650 kHz

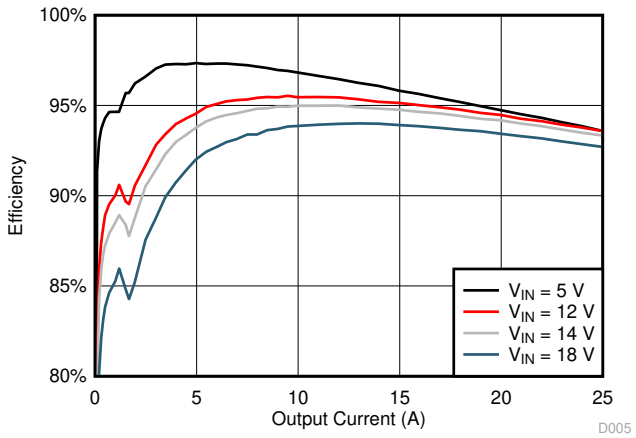
図 5-3. Converter Power Loss vs Output Current



V_{OUT} = 1 V　　V_{DD} = V_{IN}　　FCCM Mode
f_{SW} = 650 kHz

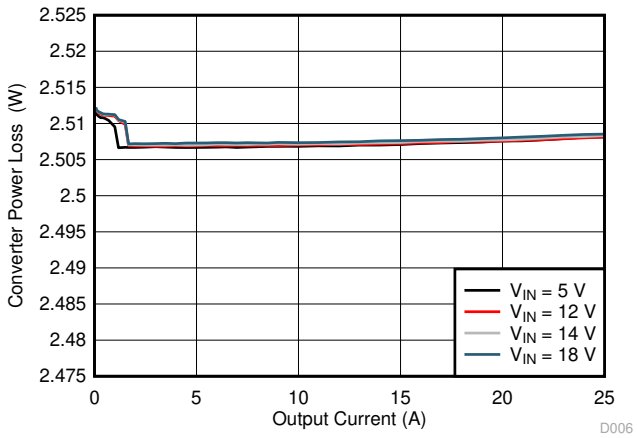
図 5-4. Output Voltage Regulation vs Output Current

5.6 Typical Characteristics (continued)



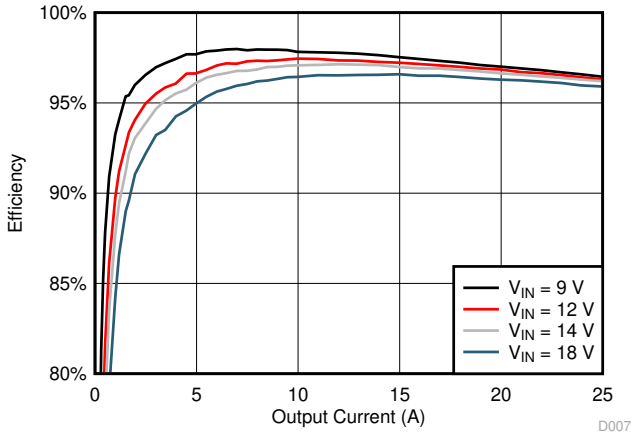
V_{DD} = V_{IN} f_{SW} = 650 kHz SKIP Mode
V_{OUT} = 2.5 V L= 820 nH, 0.9 mΩ

図 5-5. Efficiency vs Output Current



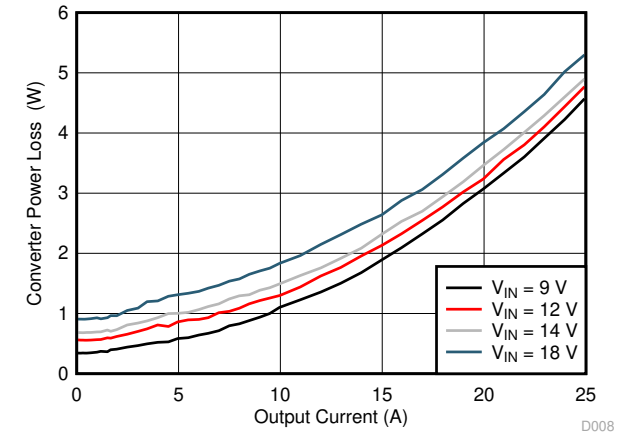
V_{DD} = V_{IN} f_{SW} = 650 kHz SKIP Mode
V_{OUT} = 2.5 V L= 820 nH, 0.9 mΩ

図 5-6. Output Voltage Regulation vs Output Current



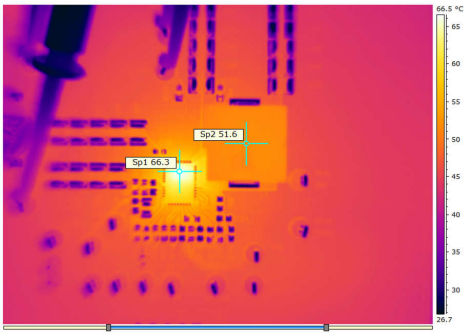
V_{DD} = V_{IN} f_{SW} = 650 kHz FCCM Mode
V_{OUT} = 5 V L= 820 nH, 0.9 mΩ

図 5-7. Efficiency vs Output Current



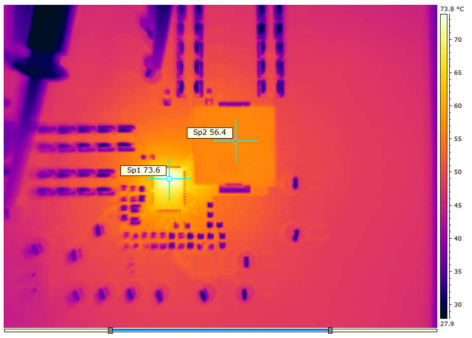
V_{DD} = V_{IN} f_{SW} = 650 kHz FCCM Mode
V_{OUT} = 5 V L= 820 nH, 0.9 mΩ

図 5-8. Power Loss vs Output Current



V_{DD} = V_{IN} = 12 V f_{SW} = 650 kHz I_{OUT} = 25 A
V_{OUT} = 1 V Natural convection at room temperature

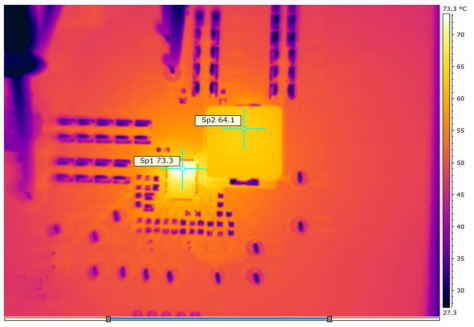
図 5-9. Thermal Image



V_{DD} = V_{IN} = 12 V f_{SW} = 650 kHz I_{OUT} = 25 A
V_{OUT} = 1 V Natural convection at room temperature

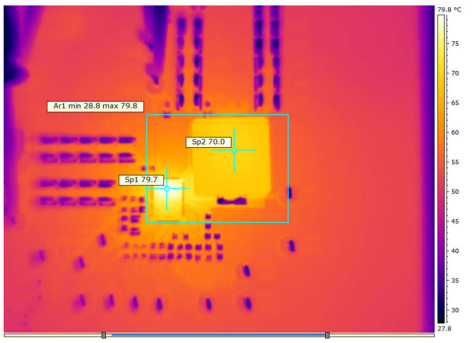
図 5-10. Thermal Image

5.6 Typical Characteristics (continued)



V_{DD} = V_{IN} = 12 V
V_{OUT} = 2.5 V
f_{SW} = 650 kHz
Natural convection at room temperature
I_{OUT} = 25 A

図 5-11. Thermal Image



V_{DD} = V_{IN} = 12 V
V_{OUT} = 5 V
f_{SW} = 650 kHz
Natural convection at room temperature
I_{OUT} = 25 A

図 5-12. Thermal Image

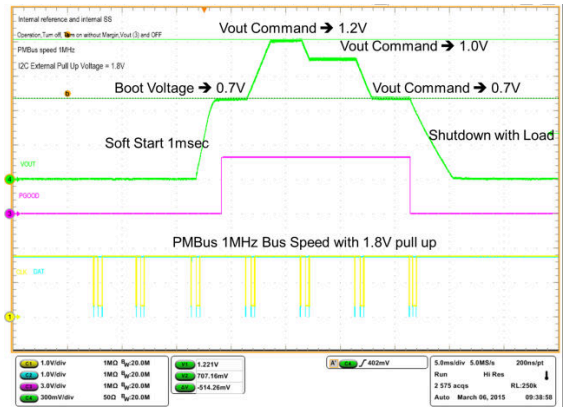
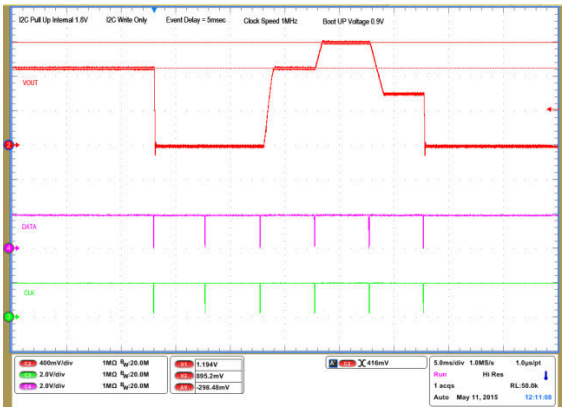


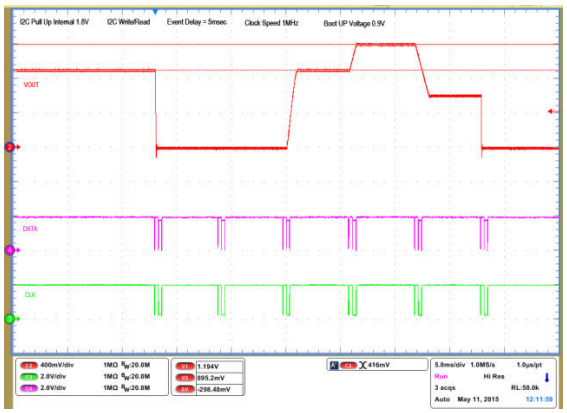
図 5-13. PMBus 1-MHz Bus Speed with 1.8-V Pullup



1 – Operation only
2 – Turnoff
3 – Turnon without Margin
4 – V_{OUT} Command up to 1.2 V
5 – V_{OUT} Command down to 0.6 V
6 – Turnoff

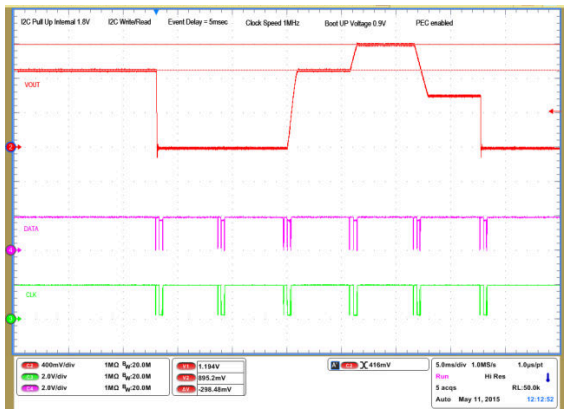
図 5-14. 6 Sequenced Events – I2C Write

5.6 Typical Characteristics (continued)



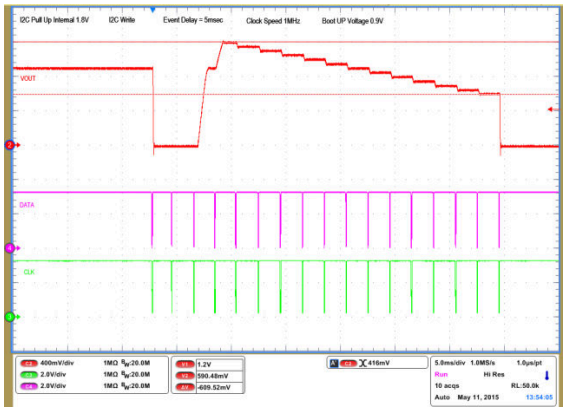
1 – Operation only
2 – Turnoff
3 – Turnon without Margin
4 – V_{OUT} Command up to 1.2 V
5 – V_{OUT} Command down to 0.6 V
6 – Turnoff

図 5-15. 6 Sequenced Events – I2C Write/Read



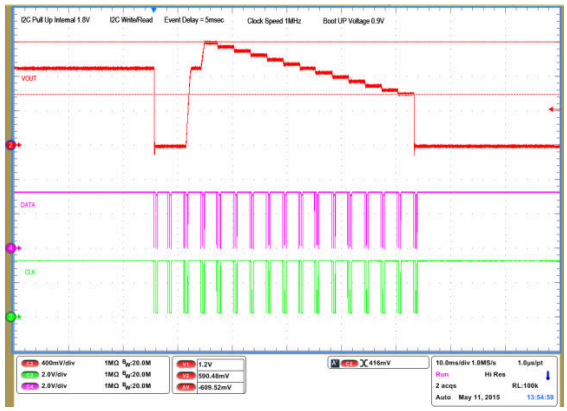
1 – Operation only
2 – Turnoff
3 – Turnon without Margin
4 – V_{OUT} Command up to 1.2 V
5 – V_{OUT} Command down to 0.6 V
6 – Turnoff

図 5-16. 6 Sequenced Events – I2C Write/Read with PEC



1 – Operation only
2 – Turnoff
3 – Turnon without Margin
4 – 16 V_{OUT} Command up to 1.2 V,
50 mV per step down to 0.6 V
17 – Turnoff

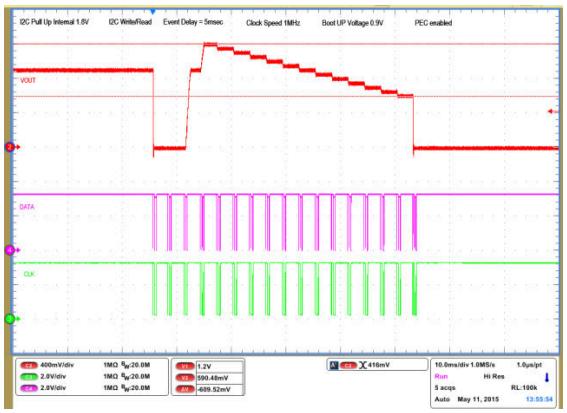
図 5-17. 17 Sequenced Events – I2C Write



1 – Operation only
2 – Turnoff
3 – Turnon without Margin
4 – 16 V_{OUT} Command up to 1.2 V,
50 mV per step down to 0.6 V
17 – Turnoff

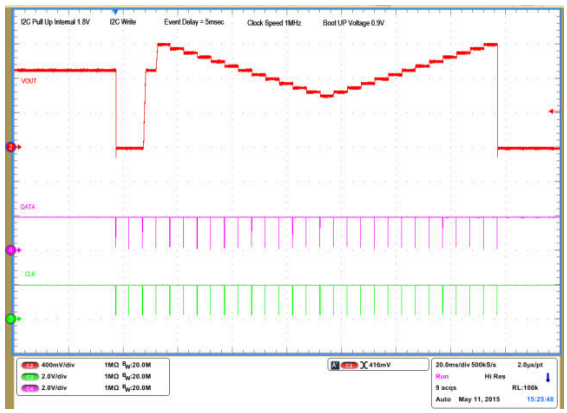
図 5-18. 17 Sequenced Events – I2C Write/Read

5.6 Typical Characteristics (continued)



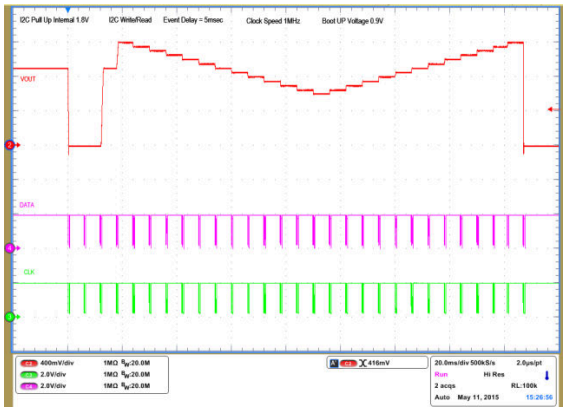
1 – Operation only
2 – Turnoff
3 – Turnon without Margin
4 – 16 V_{OUT} Command up to 1.2 V, 50 mV per step down to 0.6 V
17 – Turnoff

図 5-19. 17 Sequenced Events – I2C Write/Read with PEC



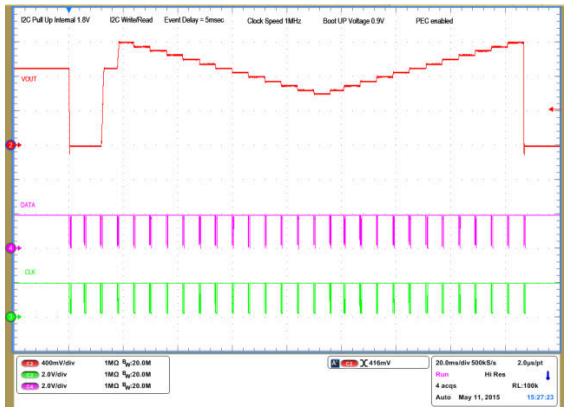
1 – Operation only
2 – Turnoff
3 – Turnon without Margin
4 – 16 V_{OUT} Command up to 1.2 V, 50 mV per step down to 0.6 V
17 – 28 V_{OUT} Command from 0.6 V to 1.2 V, 50 mV per step
29 – Turnoff

図 5-20. 29 Sequenced Events – I2C Write



1 – Operation only
2 – Turnoff
3 – Turnon without Margin
4 – 16 V_{OUT} Command up to 1.2 V, 50 mV per step down to 0.6 V
17 – 28 Vout Command from 0.6 V to 1.2 V, 50 mV per step
29 – Turnoff

図 5-21. 29 Sequenced Events – I2C Write/Read



1 – Operation only
2 – Turnoff
3 – Turnon without Margin
4 – 16 Vout Command up to 1.2 V, 50 mV per step down to 0.6 V
17 – 28 Vout Command from 0.6 V to 1.2 V, 50 mV per step
29 – Turnoff

図 5-22. 29 Sequenced Events – I2C Write/Read with PEC

6 Detailed Description

6.1 Overview

The TPS549B22 device is a high-efficiency, single-channel, FET-integrated, synchronous buck converter. The device is designed for point-of-load applications with 25 A or lower output current in storage, telecom and similar digital applications. The device features proprietary D-CAP3 control mode combined with adaptive on-time architecture. This combination is designed for building modern high/low duty ratio, ultra-fast load step response DC-DC converters.

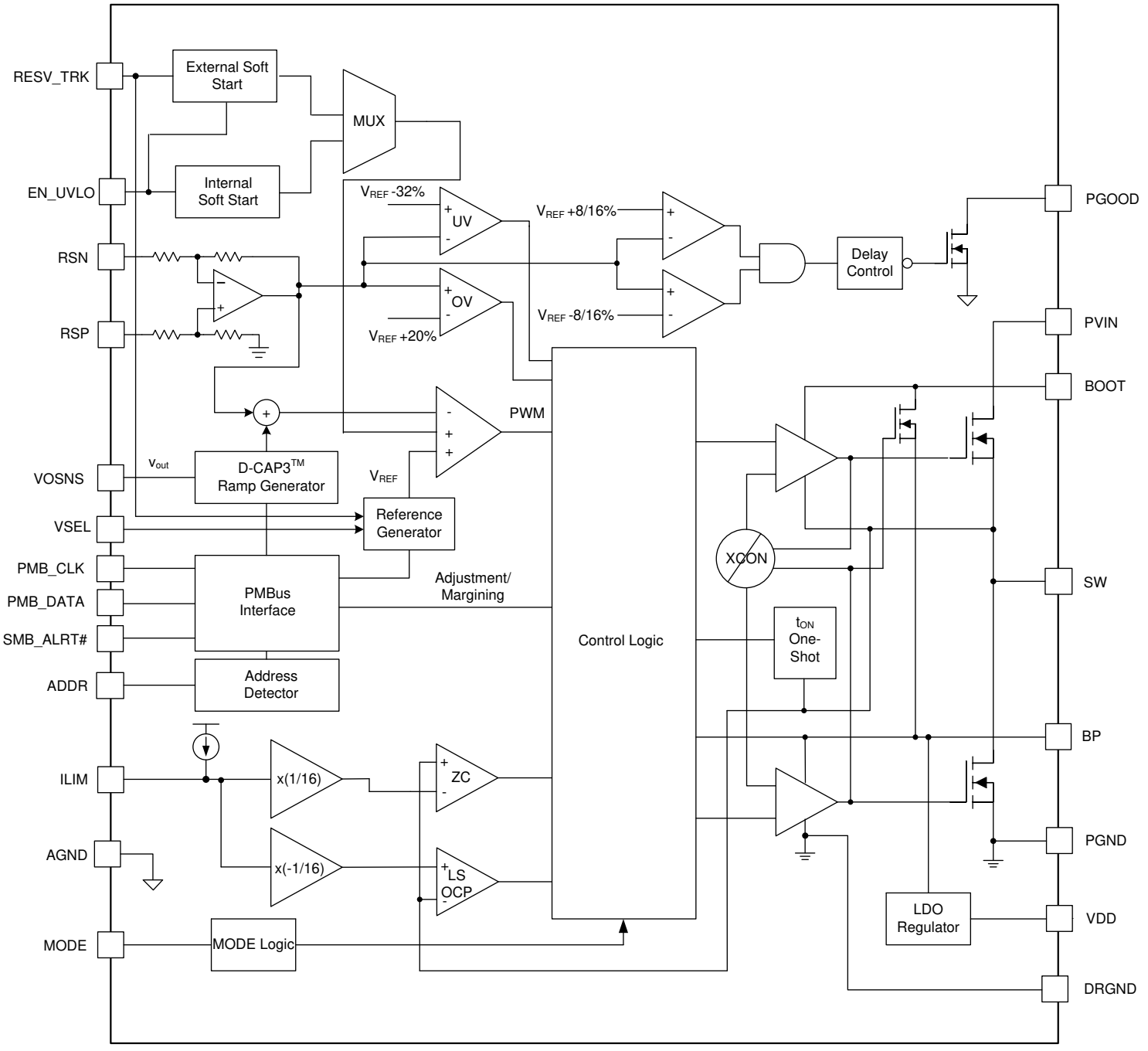
The TPS549B22 device has integrated MOSFETs rated at 25-A TDC.

The converter input voltage range is from 1.5 V up to 18 V, and the V_{DD} input voltage range is from 4.5 V to 22 V. The output voltage ranges from 0.6 V to 5.5 V.

Stable operation with all ceramic output capacitors is supported as the D-CAP3 control mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require phase compensation network outside, which makes the control scheme easy to use and also enables low external component count. . Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during load step transient.

The default preset switching frequency for this device is 650 kHz. Switching frequency is also programmable from 8 preset values through PMBus interface. supports digital communication via PMBus using standard interfacing pins, PMB_CLK, PMB_DATA and SMB_ALRT#. The detailed PMBus features, capabilities and command sets of the TPS549B22 can be found in *PMBus Programming*.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 25-A FET

The TPS549B22 device is a high-performance, integrated FET converter supporting current rating up to 25 A thermally. It integrates two N-channel NexFET™ power MOSFETs, enabling high power density and small PCB layout area. The drain-to-source breakdown voltage for these FETs is 25-V DC and 27-V transient for 10 ns. Avalanche breakdown occurs if the absolute maximum voltage rating exceeds 27 V. To limit the switch node

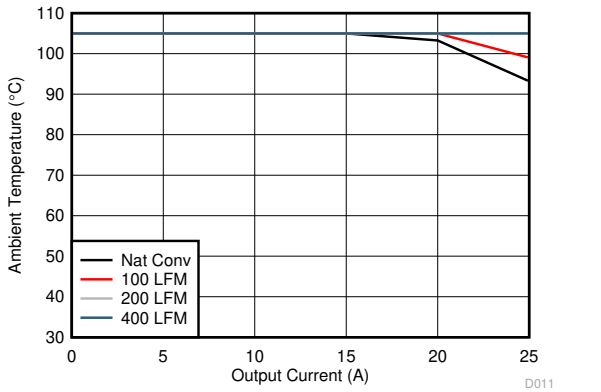
ringing of the device, TI recommends adding an R-C snubber from the SW node to the PGND pins. Refer to *セクション 8.4.1* for the detailed recommendations.

6.3.2 On-Resistance

The typical on-resistance ($R_{DS(on)}$) for the high-side MOSFET is 4.1 mΩ, and typical on-resistance for the low-side MOSFET is 1.9 mΩ with a nominal gate voltage (V_{GS}) of 5 V.

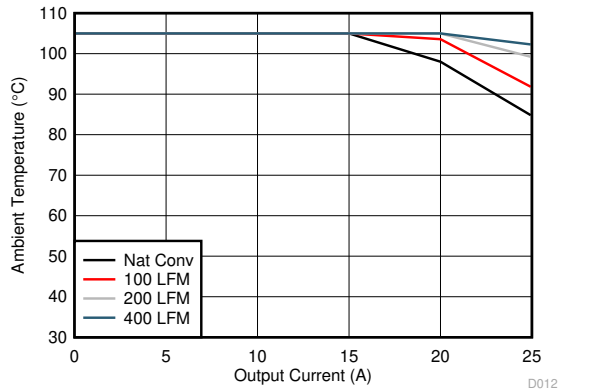
6.3.3 Package Size, Efficiency and Thermal Performance

The TPS549B22 device is available in a 7 mm × 5 mm QFN package with 40 power and I/O pins. The device employs TI proprietary MCM packaging technology with thermal pad. With a properly designed system layout, applications achieve optimized safe operating area (SOA) performance. The curves shown in 図 6-1 and 図 6-2 are based on the orderable evaluation module design. (See www.ti.com to order the EVM.)



V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 650 kHz

図 6-1. Safe Operating Area



V_{IN} = 12 V V_{OUT} = 5.5 V f_{SW} = 650 kHz

図 6-2. Safe Operating Area

6.3.4 Soft-Start Operation

In the TPS549B22 device the soft-start time controls the inrush current required to charge the output capacitor bank during start-up. The device offers selectable soft-start options of 1 ms, 2 ms, 4 ms and 8 ms. When the device is enabled (either by EN or V_{DD} UVLO), the reference voltage ramps from 0 V to the final level defined by VSEL pin-strap configuration, in a given soft-start time. The TPS549B22 device supports several soft-start times between 1 ms and 8 ms selected by MODE pin configuration. Refer to MODE definition table for details.

6.3.5 V_{DD} Supply Undervoltage Lockout (UVLO) Protection

The TPS549B22 device provides fixed V_{DD} undervoltage lockout threshold and hysteresis. The typical V_{DD} turnon threshold is 4.25 V, and hysteresis is 0.2 V. The V_{DD} UVLO can be used in conjunction with the EN_UVLO signal to provide proper power sequence to the converter design. UVLO is a non-latched protection.

6.3.6 EN_UVLO Pin Functionality

The EN_UVLO pin drives an input buffer with accurate threshold and can be used to program the exact required turnon and turnoff thresholds for switcher enable, V_{DD} UVLO or VIN UVLO (if VIN and VDD are tied together). If desired, an external resistor divider can be used to set and program the turnon threshold for V_{DD} or VIN UVLO.

図 6-3 shows how to program the input voltage UVLO using the EN_UVLO pin.

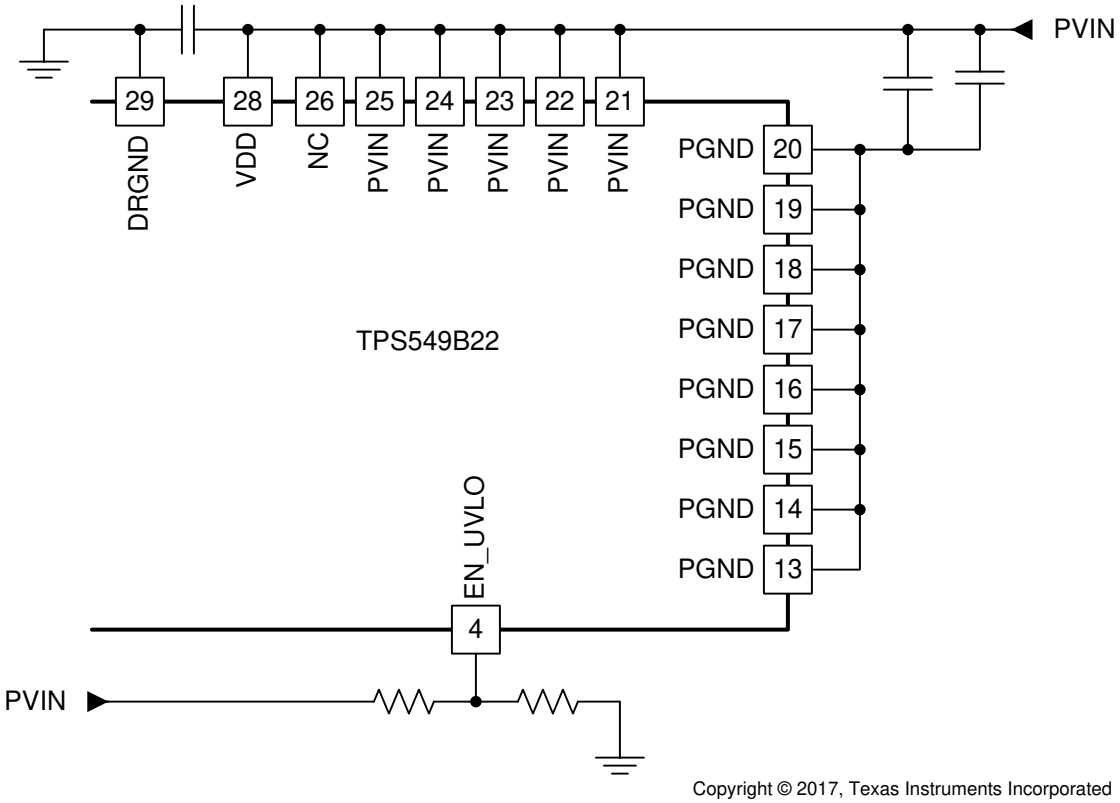


図 6-3. Programming the UVLO Voltage

6.3.7 Fault Protections

This section describes positive and negative overcurrent limits, overvoltage protections, out-of-bounds limits, undervoltage protections, and overtemperature protections.

6.3.7.1 Current Limit (ILIM) Functionality

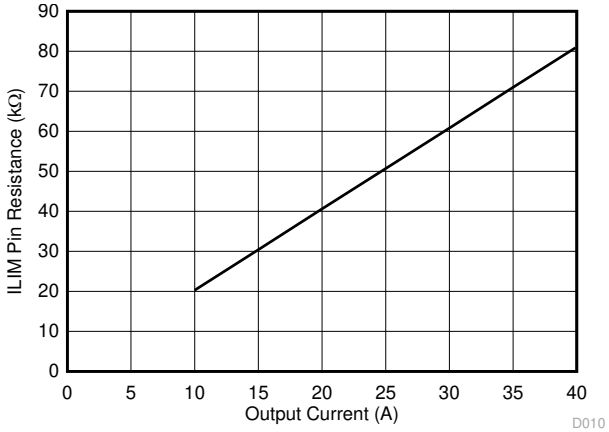


図 6-4. Current Limit Resistance vs OCP Valley Overcurrent Limit

The ILIM pin sets the OCP level. Connect the ILIM pin to GND through the voltage setting resistor, R_{ILIM}. To provide both good accuracy and a cost-effective solution, the TPS549B22 device supports temperature compensated internal MOSFET $R_{DS(on)}$ sensing.

Also, the TPS549B22 device performs both positive and negative inductor current limiting with the same magnitudes. The positive current limit normally protects the inductor from saturation that causes damage to the high-side FET and low-side FET. The negative current limit protects the low-side FET during OVP discharge.

The voltage between GND pin and SW pin during the OFF time monitors the inductor current. The current limit has 1200 ppm/°C temperature slope to compensate the temperature dependency of the on-resistance ($R_{DS(on)}$). The GND pin is used as the positive current sensing node.

The TPS549B22 device uses cycle-by-cycle over-current limiting control. The inductor current is monitored during the *OFF*-state and the controller maintains the OFF-state during the period that the inductor current is larger than the overcurrent I_{LIM} level. V_{ILIM} sets the valley level of the inductor current.

6.3.7.2 V_{DD} Undervoltage Lockout (UVLO)

The TPS549B22 device has an UVLO protection function for the V_{DD} supply input. The on-threshold voltage is 4.25 V with 200 mV of hysteresis. During a UVLO condition, the device is disabled regardless of the EN_UVLO pin voltage. The supply voltage (V_{VDD}) must be above the on-threshold to begin the pin strap detection.

6.3.7.3 Overvoltage Protection (OVP) and Undervoltage Protection (UVP)

The device monitors a feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 68% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the device latches OFF both high-side and low-side MOSFETs drivers. The UVP function enables after soft-start is complete.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit. Upon reaching the negative current limit, the low-side FET is turned off and the high-side FET is turned on again for a minimum on-time. The TPS549B22 device operates in this cycle until the output voltage is pulled down under the UVP threshold voltage for 1 ms. The fault is cleared with a reset of VDD or by retoggling the EN pin.

表 6-1. Overvoltage Protection Details

REFERENCE VOLTAGE (V_{REF})	SOFT-START RAMP	START-UP OVP THRESHOLD	OPERATING OVP THRESHOLD	OVP DELAY 100 mV OD (µs)	OVP RESET
Internal	Internal	1.2 × Internal V_{REF}	1.2 × Internal V_{REF}	1	UVP

6.3.7.4 Out-of-Bounds Operation

The device has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, so the device is not latched off after an OOB event. OOB protection operates as an early no-fault overvoltage-protection mechanism. During the OOB operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly toward the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to make sure of the safe operation of the internal FETs.

6.3.7.5 Overtemperature Protection

TPS549B22 device has overtemperature protection (OTP) by monitoring the die temperature. If the temperature exceeds the threshold value (default value 165°C), TPS549B22 device is shut off. When the temperature falls about 25°C below the threshold value, the device turns on again. The OTP is a non-latch protection.

6.4 Device Functional Modes

6.4.1 D-CAP3™ Control Mode Topology

The TPS549B22 employs an artificial ramp generator that stabilizes the loop. The ramp amplitude is automatically adjusted as a function of selected switching frequency (f_{SW}) The ramp amplitude is a function of

duty cycle (V_{OUT}-to-V_{IN} ratio). Consequently, two additional pin-strap bits are provided for fine tuning the internal ramp amplitude. The device uses an improved D-CAP3 control mode architecture that incorporates a steady-state error integrator. The slow integrator improves the output voltage DC accuracy greatly and presents minimal impact to small signal transient response. To further enhance the small signal stability of the control loop, the device uses a modified ramp generator that supports a wider range of output LC stage.

6.4.2 DCAP Control Topology

For advanced users of this device, the internal D-CAP3 control mode ramp can be disabled using the MODE[4] pin-strap bit. This situation requires an external RCC network to make sure of control loop stability. Place this RCC network across the output inductor. Use a range between 10 mV and 15 mV of injected RSP pin ripple. If no feedback resistor divider network is used, insert a 10-kΩ resistor between the VOUT pin and the RSP pin.

6.5 Programming

6.5.1 Programmable Pin-Strap Settings

ADDR, VSEL and MODE. Description: a 1% or better 100kΩ resistor is needed from BP to each of the three pins. The bottom resistor from each pin to ground (see **MODE, VSEL, ADDR DETECTION** section of the *セクション 5.5* table) in conjunction with the top resistor defines each pin strap selection. The pin detection checks for external resistor divider ratio during initial power up (VDD is brought down below approximately 3 V) when BP LDO output is at approximately 2.9 V.

6.5.1.1 Address Selection (ADDR) Pin

The TPS549B22 allows up to 16 different chip addresses for PMBus communication with the first 3 bits fixed as 001. The address selection process is defined by resistor divider ratio from BP pin to ADDR pin, and the address detection circuit starts to work only after the initial power up when V_{DD} has risen above the UVLO threshold. 表 6-4 lists all combinations of the address selections. The 1% or better tolerance resistors with typical temperature coefficient of ±100ppm/°C are recommended.

ADDR pin-strap configuration also programs the light load conduction mode.

6.5.1.2 VSEL Pin

VSEL pin strap configuration is used to program initial boot voltage value, hiccup mode and latch off mode. The initial boot voltage is used to program the main loop voltage reference point. VSEL voltage settings provide TI designated discrete internal reference voltages. 表 6-2 lists internal reference voltage selections.

表 6-2. Internal Reference Voltage Selections

VSEL[4]	VSEL[3]	VSEL[2]	VSEL[1]	VSEL[0]	R_{VSEL} (kΩ) (1)
1111: **0.975 V**				1: Latch-Off	Open
				0: Hiccup	187
1110: 1.1992 V				1: Latch-Off	165
				0: Hiccup	147
1101: 1.1504 V				1: Latch-Off	133
				0: Hiccup	121
1100: 1.0996 V				1: Latch-Off	110
				0: Hiccup	100
1011: 1.0508 V				1: Latch-Off	90.9
				0: Hiccup	82.5
1010: 1.0000 V				1: Latch-Off	75
				0: Hiccup	68.1
1001: 0.9492 V				1: Latch-Off	60.4
				0: Hiccup	53.6
1000: 0.9023 V				1: Latch-Off	47.5
				0: Hiccup	42.2
0111: 0.9004 V				1: Latch-Off	37.4
				0: Hiccup	33.2
0110: 0.8496 V				1: Latch-Off	29.4
				0: Hiccup	25.5
0101: 0.8008 V				1: Latch-Off	22.1
				0: Hiccup	19.1
0100: 0.7500 V				1: Latch-Off	16.5
				0: Hiccup	14.3
0011: 0.6992 V				1: Latch-Off	12.1
				0: Hiccup	10
0010: 0.6504 V				1: Latch-Off	7.87
				0: Hiccup	6.19
0001: 0.5996 V				1: Latch-Off	4.64
				0: Hiccup	3.16
0000: **0.975 V**				1: Latch-Off	1.78
				0: Hiccup	0

(1) 1% or better and connect to ground

6.5.1.3 D-CAP3™ Control Mode Selection

The MODE pinstrap configuration programs the control topology and internal soft-start timing selections. The TPS549B22 device supports both D-CAP3 control mode and DCAP operation

MODE[4] selection bit is used to set the control topology. If MODE[4] bit is 0, it selects DCAP operation. If MODE[4] bit is 1, it selects D-CAP3 control mode operation.

MODE[1] and MODE[0] selection bits are used to set the internal soft-start timing.

表 6-3. Allowable MODE Pin Selections

MODE[4]	MODE[3]	MODE[2]	MODE[1]	MODE[0]	R_{MODE} (kΩ) (1)
1: D-CAP3	0: Internal Reference	0: Internal SS	11: 8 ms(2)		60.4
			10: 4 ms(2)		53.6
			01: 2 ms		47.5
			00: 1 ms		42.2
0: DCAP	0: Internal Reference	0: Internal SS	11: 8 ms(2)		4.64
			10: 4 ms(2)		3.16
			01: 2 ms		1.78
			00: 1 ms		0

(1) R_{MODE} settings in lighter shade are not permitted (24 settings).
(2) See セクション 6.5.1.4.

6.5.1.4 Application Workaround to Support 4-ms and 8-ms SS Settings

To properly design for 4 ms and 8 ms SS settings, additional application consideration is needed. The recommended application workaround to support the 4-ms and 8-ms soft-start settings is to ensure sufficient time delay between the V_{DD} and EN_UVLO signals. The minimum delay between the rising maximum V_{DD} UVLO level and the minimum turn on threshold of EN_UVLO is at least T_{DELAY_MIN}.

$$T_{DELAY\_MIN} = K \times V_{REF} \quad (1)$$

where

- K = 9 ms/V for SS setting of 4 ms
- K = 18 ms/V for SS setting of 8 ms
- V_{REF} is the internal reference voltage programmed by VSEL pin strap

For example, if SS setting is 4 ms and V_{REF} = 1 V, program the minimum delay at least 9 ms; if SS setting is 8 ms, the minimum delay must be programmed at least 18 ms. See 図 6-5 and 図 6-6 for detailed timing requirement. Because TPS549B22 is a PMBus device, the end user has the option of programming power-on delay (POD) as another workaround. Be sure to follow the same calculation to determine the needed POD (see セクション 7.18 and 表 7-17 for detailed information).

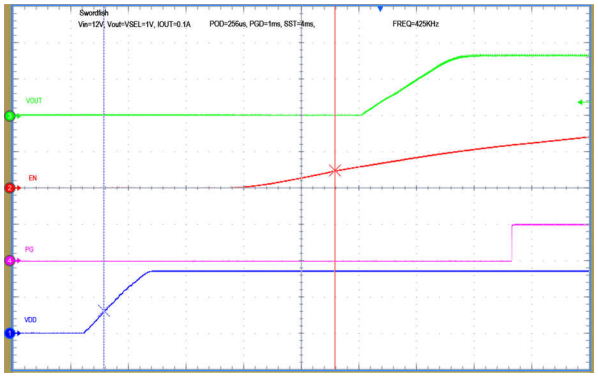


図 6-5. Proper Sequencing of V_{DD} and EN_UVLO to Support the use of 4-ms SS Setting

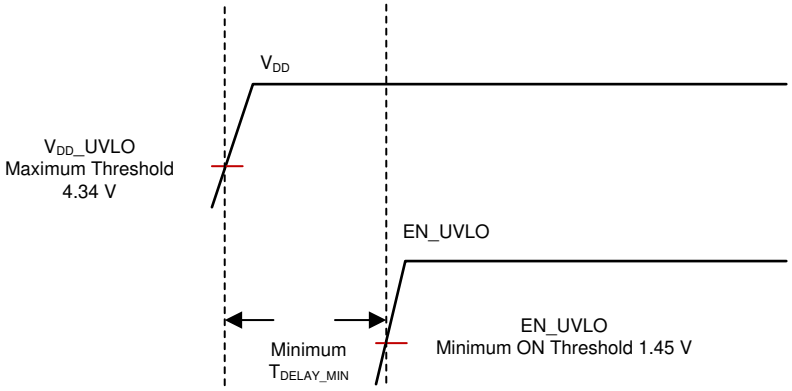


図 6-6. Minimum Delay Between V_{DD} and EN_UVLO to Support the use of 4-ms and 8-ms SS settings

The workaround/consideration described previously is not required for SS settings of 1 ms and 2 ms.

6.5.2 Programmable Analog Configurations

6.5.2.1 RSP/RSN Remote Sensing Functionality

RSP and RSN pins are used for remote sensing purpose. In the case where feedback resistors are required for output voltage programming, connect the RSP pin to the mid-point of the resistor divider, and connect the RSN pin to the load return. In the case where feedback resistors are not required as when the VSEL programs the output-voltage setpoint, connect the RSP pin to the positive sensing point of the load, and the RSN pin must always be connected to the load return.

RSP and RSN pins are extremely high-impedance input terminals of the true differential remote sense amplifier. The feedback resistor divider must use resistor values much less than 100 kΩ.

6.5.2.1.1 Output Differential Remote Sensing Amplifier

The examples in this section show simplified remote sensing circuitry where each example uses an internal reference of 1 V. 図 6-7 shows remote sensing without feedback resistors, with an output voltage setpoint of 1 V. 図 6-8 shows remote sensing using feedback resistors, with an output voltage setpoint of 5 V.

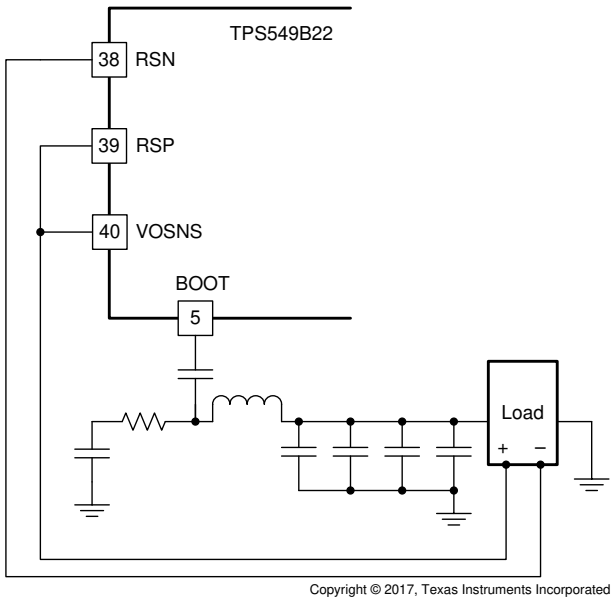


図 6-7. Remote Sensing Without Feedback Resistors

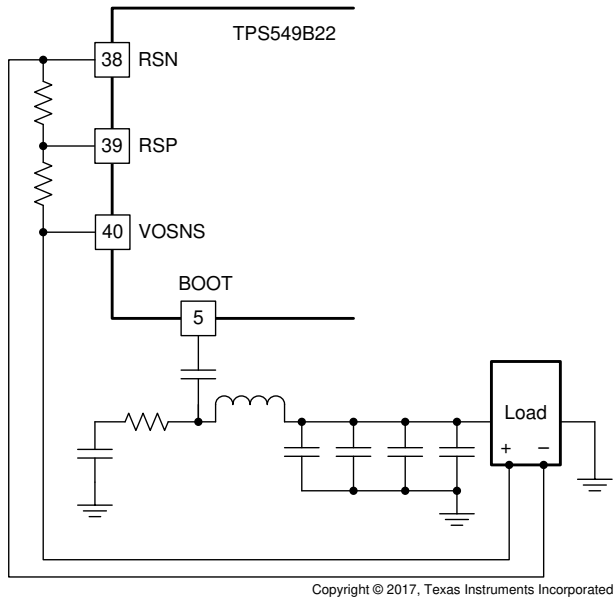


図 6-8. Remote Sensing With Feedback Resistors

6.5.2.2 Power Good (PGOOD Pin) Functionality

The TPS549B22 device has power-good output that registers high when switcher output is within the target. The power-good function is activated after soft start has finished. When the soft-start ramp reaches 300 mV above the internal reference voltage, SS end signal goes high to enable the PGOOD detection function. If the output voltage becomes within ±8% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1 ms programmable delay. If the output voltage goes outside of ±16% of the target value, the power-good signal becomes low after two microsecond (2-µs) internal delay. The open-drain power-good output must be pulled up externally. The internal N-channel MOSFET does not pull down until the V_{DD} supply is above 1.2 V.

6.5.3 PMBus Programming

TPS549B22 has seven internal custom user-accessible 8-bit registers. The PMBus interface has been designed for program flexibility, supporting direct format for write operation. Read operations are supported for both combined format and stop separated format. While there is no auto increment/decrement capability in the TPS549B22 PMBus logic, a tight software loop can be designed to randomly access the next register independent of which register was accessed first. The start and stop commands frame the data packet and the repeat start condition is allowed when necessary.

6.5.3.1 TPS549B22 Limitations to the PMBUS Specifications

TPS549B22 only recognizes seven bit addressing. This means TPS549B22 is not compatible with ten bit addressing and CBUS communication. The device can operate in standard mode (100 kbit/s), fast mode (400 kbit/s) or faster mode (1000 kbit/s).

6.5.3.2 Target Address Assignment

The seven bit target address is $001A_3A_2A_1A_0x$, where $A_3A_2A_1A_0$ is set by the ADDR pin on the device. Bit 0 is the data direction bit, i.e. $001A_3A_2A_1A_00$ is used for write operation and $001A_3A_2A_1A_01$ is used for read operation.

6.5.3.3 PMBUS Address Selection

TPS549B22 allows up to 16 different chip addresses for PMBus communication, with the first three bits fixed as 001. The address selection process is defined by the resistor divider ratio from BP pin to ADDR pin, and the

address detection circuit will start to work only after V_{DD} input supply has risen above the UVLO threshold. 表 6-4 lists the divider ratio and some example resistor values. The 1% tolerance resistors with typical temperature coefficient of ±100 ppm/°C are recommended. Higher performance resistors can be used if tighter noise margin is required for more reliable address detection.

6.5.3.4 Supported Formats

The supported formats are described in the following subsections.

6.5.3.4.1 Direct Format — Write

The simplest format for a PMBus write is direct format. After the start condition [S], the target chip address is sent, followed by an eighth bit indicating a write. TPS549B22 then acknowledges that it is being addressed, and the controller responds with an 8 bit register address byte. The target acknowledges and the controller sends the appropriate 8-bit data byte. Once again the target acknowledges and the controller terminates the transfer with the stop condition [P].

6.5.3.4.2 Combined Format — Read

After the start condition [S], the target chip address is sent, followed by an eighth bit indicating a write. TPS549B22 then acknowledges that it is being addressed, and the controller responds with an 8-bit register address byte. The target acknowledges and the controller sends the repeated start condition [Sr]. Once again, the target chip address is sent, followed by an eighth bit indicating a read. The target responds with an acknowledge followed by previously addressed 8-bit data byte. The controller then sends a non-acknowledge (NACK) and finally terminates the transfer with the stop condition [P].

6.5.3.5 Stop Separated Reads

Stop-separated reads can also be used. This format allows a controller to set up the register address pointer for a read and return to that target at a later time to read the data. In this format the target chip address followed by a write bit are sent after a start [S] condition. TPS549B22 then acknowledges it is being addressed, and the controller responds with the 8-bit register address byte. The controller then sends a stop or restart condition and can then address another target. After performing other tasks, the controller can send a start or restart condition to the TPS549B22 with a read command. The device acknowledges this request and returns the data from the register location that had been set up previously.

表 6-4. ADDR Pin Selection Table

PMBus_Address<3:0>				CM	RADDR (kΩ) (1% or better and connect to ground)
1	1	1	1	1: FCCM	Open
				0: SKIP	187
1	1	1	0	1: FCCM	165
				0: SKIP	147
1	1	0	1	1: FCCM	133
				0: SKIP	121
1	1	0	0	1: FCCM	110
				0: SKIP	100
1	0	1	1	1: FCCM	90.9
				0: SKIP	82.5
1	0	1	0	1: FCCM	75
				0: SKIP	68.1
1	0	0	1	1: FCCM	60.4
				0: SKIP	53.6
1	0	0	0	1: FCCM	47.5
				0: SKIP	42.2
0	1	1	1	1: FCCM	37.4
				0: SKIP	33.2
0	1	1	0	1: FCCM	29.4
				0: SKIP	25.5
0	1	0	1	1: FCCM	22.1
				0: SKIP	19.1
0	1	0	0	1: FCCM	16.5
				0: SKIP	14.3
0	0	1	1	1: FCCM	12.1
				0: SKIP	10
0	0	1	0	1: FCCM	7.87
				0: SKIP	6.19
0	0	0	1	1: FCCM	4.64
				0: SKIP	3.16
0	0	0	0	1: FCCM	1.78
				0: SKIP	0

6.5.3.6 Supported PMBUS Commands and Registers

Only the following PMBus commands are supported by TPS549B22, and not all parts of each command are supported.

表 6-5. PMBUS Command and Register Table

CMD CODE	COMMAND NAME	DESCRIPTION	NVM?	TYPE	No. of DATA BYTES	BIT PATTERN
1h	OPERATION	The OPERATION command is used to turn the unit on and off in conjunction with the input from the EN pin. It is also used to cause the device to set the output voltage to the upper or lower margin voltages.	no	R/W Byte	1	00XX XX00 = Turn Off 1000 XX00 = Turn on (VOUT Margin off) 1001 0100 = Turn on (VOUT Margin Low, Ignore Fault) 1001 1000 = Turn on (VOUT Margin Low, Act on Fault) 1010 0100 = Turn on (VOUT Margin High, Ignore Fault) 1010 1000 = Turn on (VOUT Margin High, Act on Fault)
2h	ON_OFF_CONFIG	Configures the combination of EN pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.	yes	R/W Byte	1	0001 0011 = Act on neither OPERATION nor EN pin 0001 0111 = Act on EN pin and ignore OPERATION 0001 1011 = Act on OPERATION and ignore EN pin 0001 1111 = Act on OPERATION and Act on EN pin (requires both)
3h	CLEAR_FAULTS	Clears all fault status registers to 0x00 and deasserts SMBAlert. The "Unit is Off" bit in the status byte and "PGOOD# de-assertion" bit in the status word are not cleared when this command is issued.	no	Send Byte	0	No data. Write only.
10h	WRITE_PROTECT	Prevents unwanted writes to the device. This register can be over-written. This is not a permanent lock.	yes	R/W Byte	1	1000 0000 Only allow WRITE_PROTECT 0100 0000 Only allow WRITE_PROTECT and OPERATION 0010 0000 Only allow WRITE_PROTECT, OPERATION, ON_OFF_CONFIG and VOUT_COMMAND 0000 0000 Allow all writes
11h	STORE_DEFAULT_ALL	Copies Operating Memory to matching non-volatile Default Store Memory.	no	Send Byte	0	No data. Write only.
12h	RESTORE_DEFAULT_ALL	Restores all parameters from non-volatile Default Store Memory to Operating Memory	no	Send Byte	0	No data. Write only.
19h	CAPABILITY	This command provides a way for a host system to determine some key capabilities of a PMBus device, including PEC, Alert and Speed.	no	Read Byte	1	1101 0000 = PEC, 1-MHz bus speed, ALERT
20h	VOUT_MODE	Hard coded to linear mode with exponent of –9.	no	Read Byte	1	000x xxxx = Linear format. 0001 0111 = Exponent value of –9 (1.953 mV resolution)
21h	VOUT_COMMAND	Output voltage setpoint. DAC resolution is 1.9531 mV and range is ~0.6 V to ~1.200 V	yes	R/W Word	2	0000 0001 0011 0011 = 0.5996 V 0000 0010 0110 0110 = 1.1992 V
25h	VOUT_MARGIN_HIGH	Sets the voltage to which the output is to be changed when the OPERATION command is set to "MARGIN HIGH".	no	R/W Word	2	0000 0001 0011 0011 = 0.5996 V 0000 0010 0110 0110 = 1.1992 V
26h	VOUT_MARGIN_LOW	Sets the voltage to which the output is to be changed when the OPERATION command is set to "MARGIN LOW".	no	R/W Word	2	0000 0001 0011 0011 = 0.5996 V 0000 0010 0110 0110 = 1.1992 V
78h	STATUS_BYTE	Status of all fault conditions in a data byte.	no	Read Byte	1	See 表 6-6
79h	STATUS_WORD	Status of all fault conditions in two data bytes.	no	Read Word	2	See 表 6-6
7Ah	STATUS_VOUT	Returns one byte of information relating to the status of the output voltage related faults.	no	Read Byte	1	See 表 6-8
7Bh	STATUS_OUT	Returns one byte of information relating to the status of the output current related faults.	no	Read Byte	1	See 表 6-8

表 6-5. PMBUS Command and Register Table (続き)

CMD CODE	COMMAND NAME	DESCRIPTION	NVM?	TYPE	No. of DATA BYTES	BIT PATTERN
7Eh	STATUS_CML	Status of communications, logic and memory in a data byte	no	Read Byte	1	XXX0 0000 0XX0 0000 = A valid or supported command has been received 1XX0 0000 = An invalid or unsupported command has been received X0X0 0000 = A valid or supported data has been received X1X0 0000 = An invalid or unsupported data has been received XX00 0000 = Packet error check has failed XX10 0000 = Packet error check has succeeded
D0h	MFR_SPECIFIC_00	Customer programmable byte that does not affect chip functionality	yes	R/W Byte	1	Free format
D1h	MFR_SPECIFIC_01	Program PGOOD delay and Power-On delay	yes	R/W Byte	1	
D2h	MFR_SPECIFIC_02	Read SST, CM, HICLOFF, TRK and SEQ. Program Forced SKIP Soft Start.	yes	R/W Byte	1	
D3h	MFR_SPECIFIC_03	Program Fsw and control mode, Read RC ramp	yes	R/W Byte	1	
D4h	MFR_SPECIFIC_04	Program the D-CAP3 control mode offset	yes	R/W Byte	1	
D6h	MFR_SPECIFIC_06	Program the V_{DD} UVLO level	yes	R/W Byte	1	
D7h	MFR_SPECIFIC_07	Program the final tracking set point and select pseudo/ external tracking	yes	R/W Byte	1	
FCh	MFR_SPECIFIC_44	Read TI PMBUS GUI Devcie ID and IC revision code	no	Read Word	2	

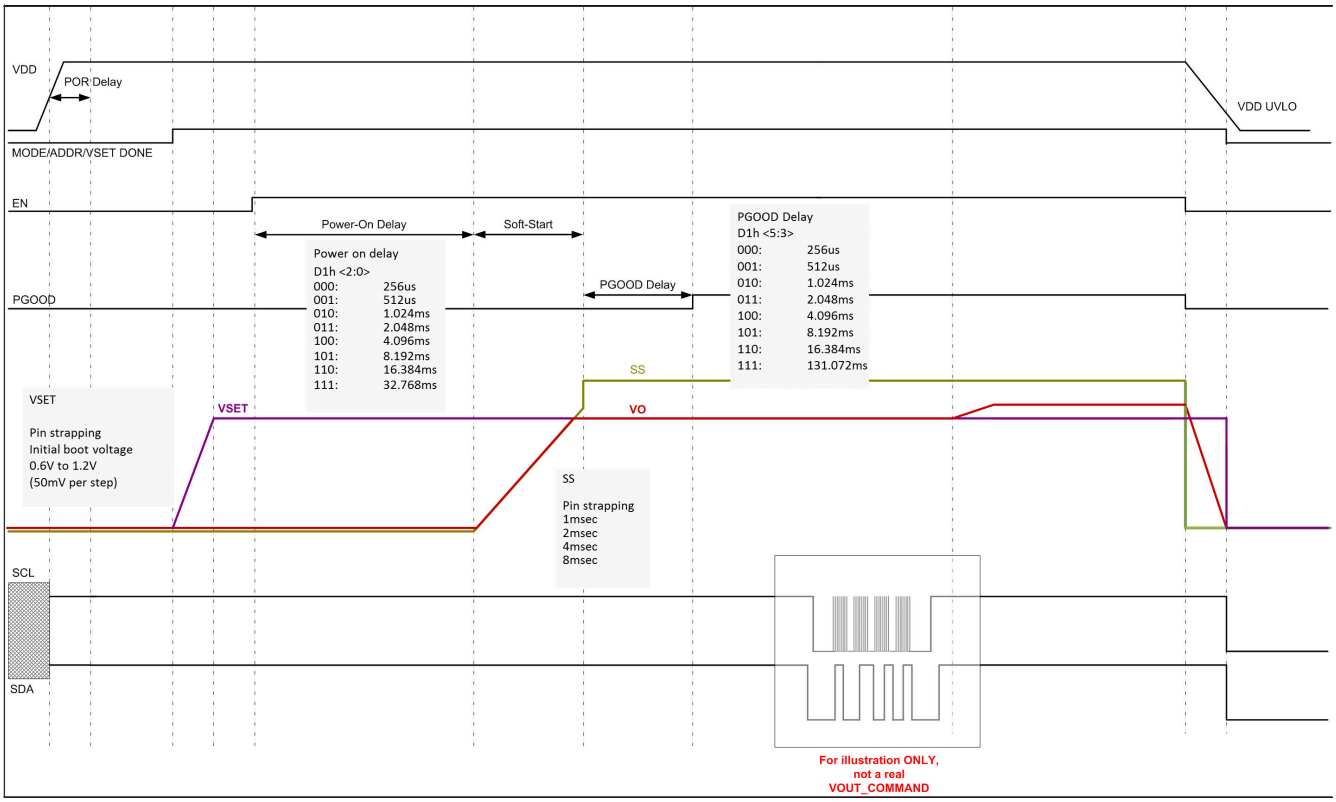


図 6-9. Start-up and VOUT_COMMAND Timing Diagram

表 6-6. Status Word Summary Table

BITS	NAME	MEANING
Low 7	not used	not used
Low 6	OFF	Unit is not providing power to the output
Low 5	VOUT_OV_FAULT	Output overvoltage
Low 4	IOUT_OC_FAULT	Output overcurremt
Low 3	VDD_UV_FAULT	Input V_{DD} undervoltage
Low 2	TEMP	Internal die temperature. Overtemperature fault
Low 1	CML	Communications, logic or memory fault
Low 0	OTHER	None of the above in the PMBUS spec
High 7	VOUT	Any output voltage fault or warning
High 6	IOUT	Any output current fault or warning
High 5	VDD_UV_FAULT	Input V_{DD} undervoltage
High 4	not used	Not used
High 3	PGOOD#	Power good de-asserted
High 2	not used	not used
High 1	not used	not used
High 0	not used	not used

表 6-7. Status V_{OUT} Summary Table

BITS	NAME	MEANING
7	OVF	Overvoltage fault
6	OVW	Overvoltage warning
5	UVW	Undervoltage warning
4	UVF	Undervoltage fault
3	not used	not used
2	not used	not used
1	not used	not used

表 6-8. Status I_{OUT} Summary Table

BITS	NAME	MEANING
7	OCF	Overcurrent fault
6	OCUVF	Overcurrent and output undervoltage fault
5	not used	not used
4	UCF	Negative overcurrent limit
3	not used	not used
2	not used	not used
1	not used	not used
0	not used	not used

7 Register Maps

7.1 OPERATION Register (address = 1h)

図 7-1. OPERATION

7	6	5	4	3	2	1	0
On_OFF	0	OPMARGIN<3:0>				0	0
R/W	R/W	R/W				R	R

RLEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-1. OPERATION

Bit	Field	Type	Reset	Description
7	ON_OFF	R/W	0	0: Turn off switching converter (if CMD=1) 1: Turn on switching converter (if CMD=1), and also enable VOUT Margin function
6		R	0	
5:2	OPMARGIN<3:0>	R/W	0	00xx: Turn off VOUT Margin function 0101: Turn on VOUT Margin Low and Ignore Fault 0110: Turn on VOUT Margin Low and Act On Fault 1001: Turn on VOUT Margin High and Ignore Fault 1010: Turn on VOUT Margin High and Act On Fault
1		R	0	
0		R	0	

7.2 ON_OFF_CONFIG Register (address = 2h)

図 7-2. ON_OFF_CONFIG

7	6	5	4	3	2	1	0
0	0	0	1	CMD	CP	1	1
R	R	R	R	R/W	R/W	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-2. ON_OFF_CONFIG

Bit	Field	Type	Reset	Description
7		R	0	
6		R	0	
5		R	0	
4		R	1	
3	CMD	R/W	0	0: Ignore ON_OFF bit 1: Act on ON_OFF bit
2	CP	R/W	1	0: Ignore ON_OFF bit 1: Act on ON_OFF bit
1		R	1	
0		R	1	

7.3 CLEAR FAULTS (address = 3h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command simultaneously clears all bits in all status registers. At the same time, the device clears the SMB_ALERT# signal output if the device is asserting the SMB_ALERT# signal.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means.

7.4 WRITE PROTECT (address = 10h)

図 7-3. WRITE PROTECT

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-3. WRITE PROTECT

Bit	Field	Type	Reset	Description
7:0	WRITE_PROTECT	R/W	0	00000000: Enable writes to ALL commands 00100000: Enable writes to only WRITE_PROTECT, OPERATION and ON_OFF_CONFIG and VOUT_COMMAND commands 01000000: Enable writes to only WRITE_PROTECT and OPERATION 10000000: Enable writes to only WRITE_PROTECT

7.5 STORE_DEFAULT_ALL (address = 11h)

Store all of the current storable register settings in the EEPROM memory as the new defaults on power up.

It is permitted to use the STORE_DEFAULT_ALL command while the device is operating. However, the device can be unresponsive during the write operation with unpredictable memory storage results. TI recommends to turn the device output off before issuing this command.

EEPROM programming faults will set the ‘CML’ bit in the STATUS_BYTE and the ‘MEM’ bit in the STATUS_CML registers.

7.6 RESTORE_DEFAULT_ALL (address = 12h)

Write EEPROM data to those CSRs that: (1) have EEPROM support, and; (2) are unprotected according to current setting of WRITE_PROTECT.

It is permitted to use the RESTORE_DEFAULT_ALL command while the device is operating. However, the device can be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. TI recommends turning the device output off before issuing this command.

No data bytes are sent, just the command code is sent.

7.7 CAPABILITY (address = 19h)

This command provides a way for a host system to determine some key capabilities of this PMBus device.

図 7-4. CAPABILITY

7	6	5	4	3	2	1	0
PEC=1	SPEED <1:0>		ALRT=1	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-4. CAPABILITY

Bit	Field	Type	Reset	Description
7	PEC=1	R	1	1: Packet Error Checking is supported
6:5	SPEED <1:0>	R	10b	10: Maximum supported bus speed is 1 MHz
4	ALRT=1	R	1	TPS549B22 has an ALERT# pin and it supports SMBus Alert Response protocol
3		R	0	

表 7-4. CAPABILITY (続き)

Bit	Field	Type	Reset	Description
2		R	0	
1		R	0	
0		R	0	

7.8 VOUT_MODE (address = 20h)

図 7-5. VOUT_MODE

7	6	5	4	3	2	1	0
MODE = 000			Exponent = 10111				
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-5. VOUT_MODE

Bit	Field	Type	Reset	Description
7:5	MODE = 000	R	0	000: Linear Format
4:0	Exponent	R	17h	10111: Exponent = −9 (equivalent of 1.9531 mV/LSB)

7.9 VOUT_COMMAND (address = 21h)

The VOUT_COMMAND command sets the output voltage in volts. The exponent is set be VOUT_MODE at –9 (equivalent of 1.9531 mV/LSB). The programmed V_{OUT} is computed as:

$$V_{OUT} = \text{VOUT\_COMMAND} \times \text{VOUT\_MODE volts} = \text{VOUT\_COMMAND} \times 2^{-9}\ \text{V} \quad (2)$$

The support range for TPS549B22 is: 0.5996 V to 1.1992 V. It is effectively 9 bits limited to 307 to 614 decimal. Slew-rate control is provided through MODE pin.

V_{OUT} changes 1 step per t_{slew}, where t_{slew} is programmable by MODE pin: 4, 8, 16, or 32 µs.

図 7-6. VOUT_COMMAND

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mantissa															
R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-6. VOUT_COMMAND

Bit	Field	Type	Reset	Description
7:4	Mantissa	R	0000	
3:0	Mantissa	R/W	00xx	x = pin strap
7:0	Mantissa	R/W	xxxx xxxx	

7.10 VOUT_MARGIN_HIGH (address = 25h) ®

The VOUT_MARGIN_HIGH command loads the TPS549B22 with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

The data bytes are two bytes formatted according to the setting of the VOUT_MODE command.

The support margin range for TPS549B22 is: 0.5996 V to 1.1992 V. It is effectively 9 bits limited to 307 to 614 decimal. Slew-rate control is provided through MODE pin.

図 7-7. VOUT_MARGIN_HIGH

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mantissa															
R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-7. VOUT_MARGIN_HIGH

Bit	Field	Type	Reset	Description
7:4	Mantissa	R	0000	
3:0	Mantissa	R/W	00xx	x = pin strap
7:0	Mantissa	R/W	xxxx xxxx	

7.11 VOUT_MARGIN_LOW (address = 26h)

The VOUT_MARGIN_LOW command loads the TPS549B22 with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

The data bytes are two bytes formatted according to the setting of the VOUT_MODE command.

The support margin range for TPS549B22 is: 0.5996 V to 1.1992 V. It is effectively 9-bits limited to 307 to 614 decimal. Slew-rate control is provided through MODE pin.

図 7-8. VOUT_MARGIN_LOW:

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mantissa															
R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-8. VOUT_MARGIN_LOW:

Bit	Field	Type	Reset	Description
7:4	Mantissa	R	0000	
3:0	Mantissa	R/W	00xx	x = pin strap
7:0	Mantissa	R/W	xxxx xxxx	

7.12 STATUS_BYTE (address = 78h)

図 7-9. STATUS_BYTE

7	6	5	4	3	2	1	0
Not used	OFF	VOUT_OV	IOUT_OC	VDD_UV	TEMP	CML	OTHER
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-9. STATUS_BYTE

Bit	Field	Type	Reset	Description
7	Not Used	R	N/A	Not used
6	OFF	R	N/A	0: IC is on. This includes the following fault response conditions where the output is still being actively driven, such as OVP and OCF. 1: IC is off. This includes two conditions. One is unit is commanded off via OPERATION/ON_OFF _CONFIG and the other is unit is commanded on via OPERATION/ ON_OFF_CONFIG; but, due to fault response the output has been tri-stated by UVF, OT and UVLO.

表 7-9. STATUS_BYTE (続き)

Bit	Field	Type	Reset	Description
5	VOUT_OV	R	N/A	0: An output overvoltage fault has not occurred 1: An output overvoltage fault has occurred
4	IOUT_OC	R	N/A	0: An output overcurrent fault has not occurred 1: An output overcurrent fault has occurred
3	VDD_UV	R	N/A	0: An input undervoltage fault has not occurred 1: An input undervoltage fault has occurred
2	TEMP	R	N/A	0: A temperature fault or warning has not occurred 1: A temperature fault or warning has occurred
1	CML	R	N/A	0: A communications, memory or logic fault has not occurred 1: A communications, memory or logic fault has occurred
0	OTHER	R	N/A	0: A fault or warning not listed above has not occurred 1: A fault of warning not listed above has occurred

7.13 STATUS_WORD (High Byte) (address = 79h)

図 7-10. STATUS_WORD (High Byte)

7	6	5	4	3	2	1	0
VOUT	IOUT	VDD	Not Used	PGOOD#	Not Used		
R	R	R	R	R	R		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-10. STATUS_WORD (High Byte)

Bit	Field	Type	Reset	Description
7	VOUT	R	N/A	0: An output voltage fault or warning has not occurred 1: An output voltage fault or warning has occurred
6	IOUT	R	N/A	0: An output current fault has not occurred 1:An output current fault has occurred
5	VDD	R	N/A	A VDD voltage fault has not occurred 1: A VDD voltage fault has occurred
4	Not Used	R	N/A	Not Used
3	PGOOD#	R	N/A	0: PGOOD pin is at logic high 1: PGOOD pin is at logic high
2:0	Not Used	R	N/A	Not used

7.14 STATUS_VOUT (address = 7Ah)

図 7-11. STATUS_VOUT

7	6	5	4	3	2	1	0
OVF	OVW	UVW	UVF	Not Used			
R	R	R	R	R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-11. STATUS_VOUT

Bit	Field	Type	Reset	Description
7	OVF	R	N/A	0: An output overvoltage fault has not occurred 1: An output overvoltage fault has occurred
6	OVW	R	N/A	0: An output overvoltage warning has not occurred 1: An output overvoltage warning has occurred
5	UVW	R	N/A	0: An output undervoltage warning has not occurred 1: An output undervoltage warning has occurred
4	UVF	R	N/A	0: An output undervoltage fault has not occurred 1: An output undervoltage fault has occurred
3:0	Not Used	R	N/A	Not Used

7.15 STATUS_IOUT (address = 7Bh)

図 7-12. STATUS_IOUT

7	6	5	4	3	2	1	0
OCF	OCUVF	Not Used	UCF	Not Used			
R	R	R	R	R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-12. STATUS_IOUT

Bit	Field	Type	Reset	Description
7	OCF	R	N/A	0: An output positive overcurrent fault has not occurred 1: An output positive overcurrent fault has occurred
6	OCUVF	R	N/A	0: A simultaneous output positive overcurrent and undervoltage fault has not occurred 1: A simultaneous output positive overcurrent and undervoltage fault has occurred
5	Not Used	R	N/A	Not Used
4	UCF	R	N/A	0: An output negative overcurrent fault has not occurred 1: An output negative overcurrent fault has occurred
3:0	Not Used	R	N/A	Not Used

7.16 STATUS_CML (address = 7Eh)

図 7-13. STATUS_CML

7	6	5	4	3	2	1	0
COMM	DATA	PEC	Not Used			OTH	Not Used
R	R	R	R			R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-13. STATUS_CML

Bit	Field	Type	Reset	Description
7	COMM	R	N/A	0: A valid or supported command has been received 1: An invalid or unsupported command has been received
6	DATA	R	N/A	0: A valid or supported data has been received 1: An invalid or unsupported data has been received
5	PEC	R	N/A	0: Packet Error Check has failed 1: Packet Error Check has succeeded
4:2	Not Used	R	N/A	Not Used
1	OTH	R	N/A	0: A communication fault other than the ones listed in this table has not occurred 1: A communication fault other than the ones listed in this table has occurred. Currently, this bit is only set for too many data bytes
0	Not Used	R	N/A	Not Used

7.17 MFR_SPECIFIC_00 (address = D0h)

図 7-14. MFR_SPECIFIC_00

7	6	5	4	3	2	1	0
USER SCRATCH PAD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-14. MFR_SPECIFIC_00

Bit	Field	Type	Reset	Description
7:0	USER SCRATCH PAD	R/W	0	The MFR_SPECIFIC_00 is a user-accessible register dedicated as a user scratch pad.

7.18 MFR_SPECIFIC_01 (address = D1h)

図 7-15. MFR_SPECIFIC_01

7	6	5	4	3	2	1	0
0	0	PGD			POD		
R	R	R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-15. MFR_SPECIFIC_01

Bit	Field	Type	Reset	Description
7:6		R	00b	The MFR_SPECIFIC_01 is a user-accessible register dedicated for configuring the PGOOD delay and Power-On Delay functions. (Refer to 表 7-16 and 表 7-17)
5:3	PGD	R/W	010b	
2:0	POD	R/W	010b	

表 7-16. PGD[2:0]

PGD[2]	PGD[1]	PGD[0]	PGood Delay
0	0	0	256 µs
0	0	1	512 µs
0	1	0	1.024 ms
0	1	1	2.048 ms
1	0	0	4.096 ms
1	0	1	8.192 ms
1	1	0	16.384 ms
1	1	1	131.072 ms

表 7-17. POD[2:0]

POD[2]	POD[1]	POD[0]	Power-On Delay
0	0	0	256 µs
0	0	1	512 µs
0	1	0	1.024 ms
0	1	1	2.048 ms
1	0	0	4.096 ms
1	0	1	8.192 ms
1	1	0	16.384 ms
1	1	1	32.768 ms

7.19 MFR_SPECIFIC_02 (address = D2h)

The MFR_SPECIFIC_02 register allows the user to read the configuration of various pin-strap features and/or overwrite them. Note that any overwritten values here are only good until the next power-on-reset, when all parameters revert back to their pin-strap configurations.

図 7-16. MFR_SPECIFIC_02

7	6	5	4	3	2	1	0
TRK	SEQ	0	FORCESKIPSS	SST		HICLOFF	CM
R/W	R/W	R	R/W	R/W		R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-18. MFR_SPECIFIC_02

Bit	Field	Type	Reset	Description
7	TRK	R/W	P	This bit indicates whether the device is using internal or external reference voltage tracking. It will initially be loaded and reflect the value of the pin strap; but, can also be overwritten by PMBus. 0: No tracking. The device will use internal reference voltage. 1: External tracking.
6	SEQ	R/W	P	This bit indicates whether the device is using internal or external soft-start ramp. It will initially be loaded and reflect the value of the pin strap; but, can also be overwritten by PMBus. 0: No sequencing. The device will use the internal soft start ramp. 1: Sequencing
5		R	0	
4	FORCESKIPSS	R/W	1	This bit (when set) allows the user to force Soft-start to always use SKIP mode; regardless of the CM pin strap. 0: CM bit controls whether to operate in SKIP or FCCM mode during and after soft start. 1: Soft start is forced to operate in SKIP mode, then CM bit controls the mode after soft start.
3:2	SST	R/W	P	These bits indicate the time the device takes to ramp the output voltage up to regulation (that is, soft-start). The field will initially be loaded and reflect the value of the pin strap; but, can also be overwritten by PMBus. (Refer to 表 7-19)
1	HICLOFF	R/W	P	This bit indicates the response the device will take upon an output undervoltage fault. There are two fault response options which are enforced by the analog circuits: Hiccup or Latch-off. The bit value will initially be loaded and reflect the value of the pin strap; but, can also be overwritten by PMBus. 0: Hiccup after UVP fault. 1: Latch off after UVP fault.
0	CM	R/W	P	This bit indicates the conduction mode for the device. The bit value will initially be loaded and reflect the value of the pin strap; but, can also be overwritten by PMBus. 0: SKIP 1: FCCM

表 7-19. SST

SST[1]	SST[0]	Soft-start time
0	0	1 ms
0	1	2 ms
1	0	4 ms
1	1	8 ms

7.20 MFR_SPECIFIC_03 (address = D3h)

The MFR_SPECIFIC_03 register allows the user to read the configuration of the pin-strap feature (and/or overwrite it), as well configure the Ramp Generator and the PWM switching frequency.

図 7-17. MFR_SPECIFIC_03

7	6	5	4	3	2	1	0
D-CAP3	0	RCSP		0	FS		
R/W	R	R/W		R	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-20. MFR_SPECIFIC_03 Field Descriptions

Bit	Field	Type	Reset	Description
7	D-CAP3	R/W	P	This bit allows the user to read/configure the device's internal DCAP-3 control mode. It is initially loaded and reflects the value of the pin strap, but can also be overwritten by PMBus. 0: Internal D-CAP3 is disabled (ramp injection is off). 1: Internal D-CAP3 is enabled (ramp injection is on)
6		R	0	
5:4	RCSP	R/W	P	These bits allow the user to read/configure the D-CAP3 ramp generator's resistor value selection. (Refer to 表 7-21.)
3		R	0	
2:0	FS	R/W	011b	These bits allow the user to read/configure the device's PWM switching frequency. (Refer to 表 7-22)

表 7-21. RCSP

RCSP[1]	RCSP[0]	Resistor Selection
0	0	Resistor ÷ 2
0	1	Resistor ÷ 1
1	0	Resistor × 2
1	1	Resistor × 3

表 7-22. FS

FS[2]	FS[1]	FS[0]	Switching Frequency
0	0	0	315 kHz
0	0	1	425 kHz
0	1	0	550 kHz
0	1	1	650 KHz
1	0	0	825 KHz
1	0	1	900 KHz
1	1	0	1.025 MHz
1	1	1	1.125 MHz

7.21 MFR_SPECIFIC_04 (address = D4h)

The MFR_SPECIFIC_04 register allows the user to configure the D-CAP control scheme offset reduction and fixed offset correction.

図 7-18. MFR_SPECIFIC_04

7	6	5	4	3	2	1	0
DCAP3OffsetSel	DCAP3Offset[1:0]		0	0	0	0	0
R/W	R/W		R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-23. MFR_SPECIFIC_04

Bit	Field	Type	Reset	Description
7	DCAP3OffsetSel	R/W	1	This bit allows the user to read/configure the D-CAP loop's offset reduction scheme. 0: Select DCAP loop manual offset reduction circuit. 1: Select DCAP loop automatic offset reduction circuit.
6:5	DCAP3Offset	R/W	0	These bits allow the user to read/configure the D-CAP3 offset correction if and only if DCAP3OffsetSel = 0 (refer to 表 7-24).
4:0		R	0	

表 7-24. DCAP3OFFSET

DCAP3Offset[1]	DCAP3Offset[0]	Additional Offset Correction Voltage Added
0	0	0 mV
0	1	+ 2 mV
1	0	+ 4 mV
1	1	+ 6 mV

7.22 MFR_SPECIFIC_06 (address = D6h)

The MFR_SPECIFIC_06 is a user-accessible register dedicated for configuring the V_{DD} UVLO threshold.

図 7-19. MFR_SPECIFIC_06

7	6	5	4	3	2	1	0
0	0	0	0	0	VDDUVLO[2:0]		
R	R	R	R	R	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-25. MFR_SPECIFIC_06

Bit	Field	Type	Reset	Description
7:3		R	0	
2:0	VDDUVLO	R/W	101b	These bits allow the user to read/configure the device V_{DD} ULVO threshold (refer to 表 7-26).

表 7-26. VDDUVLO

VDDUVLO[2]	VDDUVLO[1]	VDDUVLO[0]	VDD UVLO threshold
0	X	X	10.2 volts
1	0	0	2.8 volts
1	0	1	4.25 volts
1	1	0	6 volts
1	1	1	8.1 volts

7.23 MFR_SPECIFIC_07 (address = D7h)

The MFR_SPECIFIC_07 is a user-accessible register dedicated for configuring the device's PGOOD threshold and external tracking options.

図 7-20. MFR_SPECIFIC_07

7	6	5	4	3	2	1	0
VPBAD	SPARE	0	TRKOPTION	VTRKIN[3:0]			
R/W	R/W	R	R/W	R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-27. MFR_SPECIFIC_07

Bit	Field	Type	Reset	Description
7	VPBAD	R/W	1	This bit allows the user to read/configure the PGOOD high and low thresholds. 0: PGOOD high and low thresholds are +16% and -16%, respectively 1: PGOOD high and low thresholds are +20% and -32%, respectively
6	SPARE	R/W	0	This bit allows the user to read/configure an EEPROM backed SPARE bit and corresponding digital block output. 0: pSPARE = 0 1: pSPARE = 1
5		R	0	
4	TRKOPTION	R/W	0	This bit allows the user to read/control whether the external TRKIN is enabled by a 425 mV threshold, or not. 0: TRKIN voltage must be above 425mV (that is, TRKINOK = 1) before switcher can be enabled. 1: TRKIN voltage does **not** need to be above 425mV before switcher can be enabled.
3:0	VTRKIN	R/W	1111b	These bits allow the user to read/configure the device's final TRKIN target voltage for external tracking operation. (Refer to 表 7-28)

表 7-28. VTRKIN

VTRKIN[3]	VTRKIN[2]	VTRKIN[1]	VTRKIN[0]	Final TRKIN target voltage for external tracking operation
0	0	0	0	500 mV
0	0	0	1	550 mV
0	0	1	0	600 mV
0	0	1	1	650 mV
0	1	0	0	700 mV
0	1	0	1	750 mV
0	1	1	0	800 mV
0	1	1	1	850 mV
1	0	0	0	900 mV
1	0	0	1	950 mV
1	0	1	0	1.00 V
1	0	1	1	1.05 V
1	1	0	0	1.10 V
1	1	0	1	1.15 V
1	1	1	0	1.20 V
1	1	1	1	1.25 V

7.24 MFR_SPECIFIC_44 (address = FCh)

The DEVICE_CODE command returns a 12-bit unique identifier code for the device and a 4 bit device revision code.

図 7-21. MFR_SPECIFIC_44

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Identifier Code												Revision Code			
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-29. MFR_SPECIFIC_44

Bit	Field	Type	Reset	Description
7:0	Identifier Code	R	02h	0000 0010 0000b – Device ID Code Identifier for TPS549B22.
7:4		R	0	
3:0	Revision Code	R	0	1000b - Revision Code (first silicon starts at 0)

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS549B22 device is a highly-integrated synchronous step-down DC-DC converter with PMBus features and capabilities. This devices is used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 25 A. Use the following design procedure to select key component values for this family of devices.

8.2 Typical Applications

8.2.1 TPS549B22 1.5-V to 18-V Input, 1-V Output, 25-A Converter

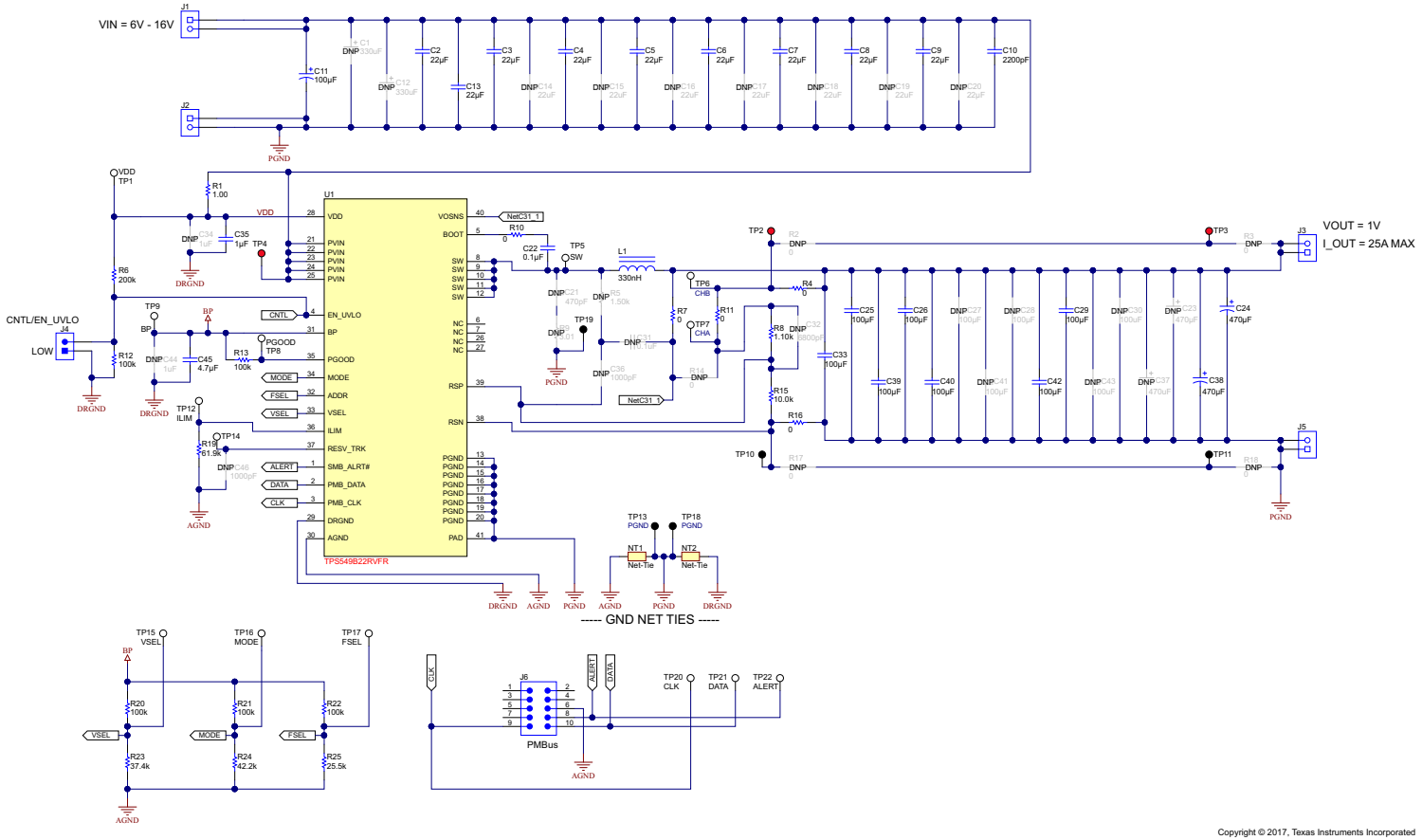


図 8-1. Typical Application Schematic

8.2.2 Design Requirements

For this design example, use the input parameters shown in 表 8-1.

表 8-1. Design Example Specifications

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		5	12	18	V
$V_{IN(ripple)}$	Input ripple voltage	I_{OUT} = 25 A			0.4	V
V_{OUT}	Output voltage			1		V
	Line regulation	5 V ≤ V_{IN} ≤ 18 V			0.5%	
	Load regulation	0 V ≤ I_{OUT} ≤ 25 A			0.5%	
V_{PP}	Output ripple voltage	I_{OUT} = 25 A		10		mV
V_{OVER}	Transient response overshoot	I_{STEP} = 15 A		30		mV
V_{UNDER}	Transient response undershoot	I_{STEP} = 15 A		30		mV
I_{OUT}	Output current	5 V ≤ V_{IN} ≤ 18 V			25	A
t_{SS}	Soft-start time			1		ms
I_{OC}	Overcurrent trip point			32		A
η	Peak efficiency	I_{OUT} = 7 A,		90%		
f_{SW}	Switching frequency			650		kHz

8.2.3 Detailed Design Procedure

8.2.3.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS549B22 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.3.2 Switching Frequency Selection

The default switching frequency of the TPS549B22 device is 650 kHz. There are a total of 8 switching frequency settings that can be programmed via PMBus interface. For each switching frequency setting, there are 4 internal ramp compensations (D-CAP3 control mode) to choose from, also via PMBus. When D-CAP3 control mode is selected (preferred), the internal ramp compensation is used for stabilizing the converter design. The ramp is a function of the switching frequency and duty cycle range (the output voltage to input voltage ratio). 表 8-2 summarizes the ramp choices using these functions.

表 8-2. Switching Frequency Selection

SWITCHING FREQUENCY SETTING (f_{SW}) (kHz)	RAMP SELECT OPTION	TIME CONSTANT t (µs)	V_{OUT} RANGE (FIXED V_{IN} = 12 V)		DUTY CYCLE RANGE (V_{OUT}/V_{IN}) (%)	
			MIN	MAX	MIN	MAX
315, 425	R/2	9	0.6	0.9	5	7.5
	R × 1	16.8	0.9	1.5	7.5	12.5
	R × 2	32.3	1.5	2.5	12.5	21
	R × 3	55.6	2.5	5.5	>21	
550, 650	R/2	7	0.6	0.9	5	7.5
	R × 1	13.5	0.9	1.5	7.5	12.5
	R × 2	25.9	1.5	2.5	12.5	21
	R × 3	44.5	2.5	5.5	>21	
825, 900	R/2	5.6	0.6	0.9	5	7.5
	R × 1	10.4	0.9	1.5	7.5	12.5
	R × 2	20	1.5	2.5	12.5	21
	R × 3	34.4	2.5	5.5	>21	
1.025, 1.225 MHz	R/2	3.8	0.6	0.9	5	7.5
	R × 1	7.1	0.9	1.5	7.5	12.5
	R × 2	13.6	1.5	2.5	12.5	21
	R × 3	23.3	2.5	5.5	>21	

8.2.3.3 Inductor Selection

To calculate the value of the output inductor, use 式 3. The coefficient K_{IND} represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing a high inductor ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, maintain a K_{IND} coefficient between 0 and 40 for balanced performance. Using this target ripple current, the required inductor size can be calculated as shown in 式 3

$$L1 = \frac{V_{OUT}}{\left(V_{IN(max)} \times f_{SW}\right)} \times \frac{V_{IN} - V_{OUT}}{\left(I_{OUT(max)} \times K_{IND}\right)} = \frac{1\,V \times (18\,V - 1\,V)}{(18\,V \times 650\,kHz \times 25\,A \times 0.2)} = 0.29\,\mu H \quad (3)$$

Selecting a K_{IND} of 0.2, the target inductance L_1 = 290 nH. Using the next standard value, the 330 nH is chosen in this application for the high current rating, low DCR, and small size. The inductor ripple current, RMS current, and peak current can be calculated using 式 4, 式 5 and 式 6. Use these values to select an inductor with approximately the target inductance value, and current ratings that allow normal operation with some margin.

$$I_{RIPPLE} = \frac{V_{OUT}}{\left(V_{IN(max)} \times f_{SW}\right)} \times \frac{V_{IN(max)} - V_{OUT}}{L1} = \frac{1\,V \times (18\,V - 1\,V)}{18\,V \times 650\,kHz \times 330\,nH} = 4.4\,A \quad (4)$$

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times (I_{RIPPLE})^2} = 25\,A \quad (5)$$

$$I_{L(peak)} = (I_{OUT}) + \frac{1}{2} \times (I_{RIPPLE}) = 27.2\,A \quad (6)$$

8.2.3.4 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- Stability
- Regulator response to a change in load current or load transient
- Output voltage ripple

These three considerations are important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

8.2.3.4.1 Minimum Output Capacitance to Make Sure of Stability

To prevent sub-harmonic multiple pulsing behavior, TPS549B22 application designs must strictly follow the small signal stability considerations described in 式 7.

$$C_{OUT(min)} > \frac{t_{ON}}{2} \times \frac{8\tau}{L_{OUT}} \times \frac{V_{REF}}{V_{OUT}} \tag{7}$$

where

- $C_{OUT(min)}$ is the minimum output capacitance needed to meet the stability requirement of the design
- t_{ON} is the on-time information based on the switching frequency and duty cycle (in this design, 128 ns)
- τ is the ramp compensation time constant of the design based on the switching frequency and duty cycle, (in this design, 25.9 µs, refer to 表 8-2)
- L_{OUT} is the output inductance (in the design, 0.33 µH)
- V_{REF} is the user-selected reference voltage level (in this design, 1 V)
- V_{OUT} is the output voltage (in this design, 1 V)

The minimum output capacitance calculated from 式 7 is 40 µF. The stability is ensured when the amount of the output capacitance is 40 µF or greater. And when all MLCCs (multi-layer ceramic capacitors) are used, both DC- and AC-derating effects must be considered to make sure that the minimum output capacitance requirement is met with sufficient margin.

8.2.3.4.2 Response to a Load Transient

The output capacitance must supply the load with the required current when current is not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation (such as undershoot and overshoot) during the transient.

Use 式 8 and 式 9 to estimate the amount of capacitance needed for a given dynamic load step and release.

注

There are other factors that can impact the amount of output capacitance for a specific design, such as ripple and stability.

$$C_{OUT(min\_under)} = \frac{L_{OUT} \times \left(\Delta I_{LOAD(max)}\right)^2 \times \left(\frac{V_{OUT} \times t_{SW}}{V_{IN(min)}} + t_{OFF(min)}\right)}{2 \times \Delta V_{LOAD(insert)} \times \left(\left(\frac{V_{IN(min)} - V_{OUT}}{V_{IN(min)}}\right) \times t_{SW} - t_{OFF(min)}\right) \times V_{OUT}} \tag{8}$$

$$C_{OUT(min\_over)} = \frac{L_{OUT} \times \left(\Delta I_{LOAD(max)}\right)^2}{2 \times \Delta V_{LOAD(release)} \times V_{OUT}} \quad (9)$$

where

- $C_{OUT(min\_under)}$ is the minimum output capacitance to meet the undershoot requirement
- $C_{OUT(min_over)}$is the minimum output capacitance to meet the overshoot requirement
- L is the output inductance value (0.33 µH)
- $\Delta I_{LOAD(max)}$ is the maximum transient step (15 A)
- V_{OUT} is the output voltage value (1 V)
- t_{SW} is the switching period (1.54 µs)
- $V_{IN(min)}$ is the minimum input voltage for the design (10.8 V)
- $t_{OFF(min)}$ is the minimum off time of the device (300 ns)
- $\Delta V_{LOAD(insert)}$ is the undershoot requirement (30 mV)
- $\Delta V_{LOAD(release)}$ is the overshoot requirement (30 mV)

Most of the above parameters can be found in 表 8-1.

The minimum output capacitance to meet the undershoot requirement is 516 µF. The minimum output capacitance to meet the overshoot requirement is 1238 µF. This example uses a combination of POSCAP and MLCC capacitors to meet the overshoot requirement.

- POSCAP bank 1: 2 x 470 µF, 2.5 V, 6 mΩ per capacitor
- MLCC bank 2: 7 × 100 µF, 2.5 V, 1 mΩ per capacitor with DC+AC derating factor of 60%

Recalculating the worst case overshoot using the described capacitor bank design, the overshoot is 29.0 mV which meets the 30-mV overshoot specification requirement.

8.2.3.4.3 Output Voltage Ripple

The output voltage ripple is another important design consideration. 式 10 calculates the minimum output capacitance required to meet the output voltage ripple specification. This criterion is the requirement when the impedance of the output capacitance is dominated by ESR.

$$C_{OUT(min)RIPPLE} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times V_{OUT(ripple)}} = 82\ \mu F \quad (10)$$

In this case, the maximum output voltage ripple is 10 mV. For this requirement, the minimum capacitance for ripple requirement yields 82 µF. Because this capacitance value is significantly lower compared to that of transient requirement, determine the capacitance bank from steps in the previous section *セクション 8.2.3.4.2*. Because the output capacitor bank consists of both POSCAP and MLCC type capacitors, it is important to consider the ripple effect at the switching frequency due to effective ESR. Use 式 11 to determine the maximum ESR of the output capacitor bank for the switching frequency.

$$ESR_{MAX} = \frac{V_{OUT(ripple)} - \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}}}{I_{RIPPLE}} = 2.2\ m\Omega \quad (11)$$

Estimate the effective ESR at the switching frequency by obtaining the impedance vs frequency characteristics of the output capacitors. The parallel impedance of capacitor bank 1 and capacitor bank 2 at the switching frequency of the design example is estimated to be 1.2 mΩ, which is less than that of the maximum ESR value. Therefore, the output voltage ripple requirement (10 mV) can be met. For detailed calculation on the effective ESR please contact the factory to obtain a user-friendly Excel based design tool.

8.2.3.5 Input Capacitor Selection

The TPS549B22 devices require a high-quality, ceramic, type X5R or X7R, input decoupling capacitor with a value of at least 1 µF of effective capacitance on the VDD pin, relative to AGND. The power stage input decoupling capacitance (effective capacitance at the PVIN and PGND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using 式 12.

$$I_{CIN(rms)} = I_{OUT(max)} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} = 10 \text{ Arms} \quad (12)$$

The minimum input capacitance and ESR values for a given input voltage ripple specification, $V_{IN(ripple)}$, are shown in 式 13 and 式 14. The input ripple is composed of a capacitive portion, $V_{RIPPLE(cap)}$, and a resistive portion, $V_{RIPPLE(esr)}$.

$$C_{IN(min)} = \frac{I_{OUT(max)} \times V_{OUT}}{V_{RIPPLE(cap)} \times V_{IN(max)} \times f_{SW}} = 21.4 \text{ µF} \quad (13)$$

$$ESR_{CIN(max)} = \frac{V_{RIPPLE(ESR)}}{I_{OUT(max)} + \left(\frac{I_{RIPPLE}}{2}\right)} = 3.4 \text{ m}\Omega \quad (14)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into account. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this design, allow 0.1-V input ripple for $V_{RIPPLE(cap)}$, and 0.1-V input ripple for $V_{RIPPLE(esr)}$. Using 式 13 and 式 14, the minimum input capacitance for this design is 21.4 µF, and the maximum ESR is 3.4 mΩ. For this example, four 22-µF, 25-V ceramic capacitors and one additional 100-µF, 25-V low-ESR polymer capacitors in parallel were selected for the power stage.

8.2.3.6 Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 µF must be connected between the BOOT and SW pins for proper operation. TI recommends using a ceramic capacitor with X5R or better grade dielectric. Use a capacitor with a voltage rating of 25 V or higher.

8.2.3.7 BP Pin

Bypass the BP pin to DRGND with 4.7 µF of capacitance. In order for the regulator to function properly, it is important that these capacitors be localized to the TPS549B22 , with low-impedance return paths. See *セクション 8.4.1* for more information.

8.2.3.8 R-C Snubber and VIN Pin High-Frequency Bypass

Though operating the TPS549B22 within absolute maximum ratings without ringing reduction techniques is possible, some designs can require external components to further reduce ringing levels. This example uses two approaches: a high frequency power stage bypass capacitor on the VIN pins, and an R-C snubber between the SW area and GND.

The high-frequency VIN bypass capacitor is a lossless ringing reduction technique which helps minimizes the outboard parasitic inductances in the power stage, which store energy during the low-side MOSFET on-time, and discharge after the high-side MOSFET is turned on. For this example two 2.2-nF, 25-V, 0603-sized high-frequency capacitors are used. The placement of these capacitors is critical to the effectiveness. The excellent placement is shown in 図 8-1.

Additionally, an R-C snubber circuit is added to this example. To balance efficiency and spike levels, a 1-nF capacitor and a 1-Ω resistor are chosen. In this example a 0805-sized resistor is chosen, which is rated for 0.125 W, nearly twice the estimated power dissipation. See *Snubber Circuits: Theory, Design and Application* for more information about snubber circuits.

8.2.3.9 Optimize Reference Voltage (VSEL)

Optimize the reference voltage by choosing a value for R_{VSEL}. The TPS549B22 device is designed with a wide range of precision reference voltage support from 0.6 V to 1.2 V with an available step change of 50 mV. Program these reference voltages using the VSEL pin-strap configurations. See 表 6-2 for internal reference voltage selections. In addition to providing initial boot voltage value, use the VSEL pin to program hiccup and latch-off mode.

There are two ways to program the output voltage set point. If the output voltage set point is one of the 16 available reference and boot voltage options, no feedback resistors are required for output voltage programming. In the case where feedback resistors are not needed, connect the RSP pin to the positive sensing point of the load. Always connect the RSN pin to the load return sensing point.

In this design example, because the output voltage set point is 1 V, select $R_{VSEL(LS)}$ of either 75 kΩ (latch off) or 68.1 kΩ (hiccup) as shown in 表 6-3. If the output voltage set point is NOT one of the 16 available reference or boot voltage options, feedback resistors are required for output voltage programming. Connect the RSP pin to the mid-point of the resistor divider. Always connect the RSN pin to the load return sensing point as shown in Figure 23 and Figure 24.

The general guideline to select boot and internal reference voltage is to select the reference voltage closest to the output voltage set point. In addition, because the RSP and RSN pins are extremely high-impedance input terminals of the true differential remote sense amplifier, use a feedback resistor divider with values much less than 100 kΩ.

8.2.3.10 MODE Pin Selection

MODE pin strap configuration is used to program control topology and internal soft-start timing selections. TPS549B22 supports both D-CAP3 and DCAP control modes. For general POL applications, TI strongly recommends configuring the D-CAP3 control mode due to the simple to use and no external compensation features. In the rare instance where DCAP control scheme is needed, an RCC network across the output inductor is needed to generate sufficient ripple voltage on the RSP pin. In this design example, $R_{MODE(LS)}$ of 42.2 kΩ is selected for D-CAP3 control mode and soft start time of 1 ms.

8.2.3.11 ADDR Pin Selection

ADDR pin strap configuration is used to program device address and light load conduction mode selection. The TPS549B22 allows up to 16 different chip addresses for PMBus communication with the first 3 bits fixed as 001. The address selection process is defined by resistor divider ratio from BP pin to ADDR pin, and the address detection circuit will start to work only after the initial power up when V_{DD} has risen above the UVLO threshold.

For this application example, a device address of 16d is desired. We select the low side RADDR to be 0 Ω considering the SKIP operation and device address of 16d. Table 4 lists all combinations of the address selections. The 1% or better tolerance resistors with typical temperature coefficient of ±100 ppm/°C are recommended

8.2.3.12 Overcurrent Limit Design

The TPS549B22 device uses the ILIM pin to set the OCP level. Connect the ILIM pin to GND through the voltage setting resistor, R_{ILIM}. To provide both good accuracy and cost effective solution, this device supports

temperature compensated MOSFET on-resistance ($R_{DS(on)}$) sensing. Also, this device performs both positive and negative inductor current limiting with the same magnitudes. Positive current limit is normally used to protect the inductor from saturation therefore causing damage to the high-side and low-side FETs. Negative current limit is used to protect the low-side FET during OVP discharge.

The inductor current is monitored by the voltage between PGND pin and SW pin during the OFF time. The ILIM pin has 1200 ppm/°C temperature slope to compensate the temperature dependency of the on-resistance. The PGND pin is used as the positive current sensing node.

TPS549B22 has cycle-by-cycle over-current limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period that the inductor current is larger than the overcurrent ILIM level. The voltage on the ILIM pin (V_{ILIM}) sets the valley level of the inductor current. The range of value of the R_{ILIM} resistor is between 9.53 kΩ and 105 kΩ. The range of valley OCL is between 5 A and 50 A (typical). If the R_{ILIM} resistance is outside of the recommended range, OCL accuracy and function cannot be ensured. (see 表 8-3)

表 8-3. Closed Loop EVM Measurement of OCP Settings

1% R_{ILIM} (kΩ)	OVERCURRENT PROTECTION VALLEY (A)
82.1	40
71.5	35
61.9	30
51.1	25
40.2	20
30.1	15
20.5	10

Use 式 15 to relate the valley OCL to the R_{ILIM} resistance.

$$R_{ILIM} = 2.0664 \times OCL_{VALLEY} - 0.6036 \quad (15)$$

where

- R_{ILIM} is in kΩ
- OCL_{VALLEY} is in A

In this design example, the desired valley OCL is 43 A, the calculated R_{ILIM} is 61.9 kΩ. Use 式 16 to calculate the DC OCL to be 32.1 A.

$$OCL_{DC} = OCL_{VALLEY} + 0.5 \times I_{RIPPLE} \quad (16)$$

where

- R_{ILIM} is in kΩ
- OCL_{DC} is in A

In an overcurrent condition, the current to the load exceeds the inductor current and the output voltage falls. When the output voltage crosses the under-voltage fault threshold for at least 1 ms, the behavior of the device depends on the VSEL pin strap setting. If hiccup mode is selected, the device restarts after a 16-ms delay (1-ms soft-start option). If the overcurrent condition persists, the OC hiccup behavior repeats. During latch-off mode operation the device shuts down until the EN pin is toggled or VDD pin is power cycled.

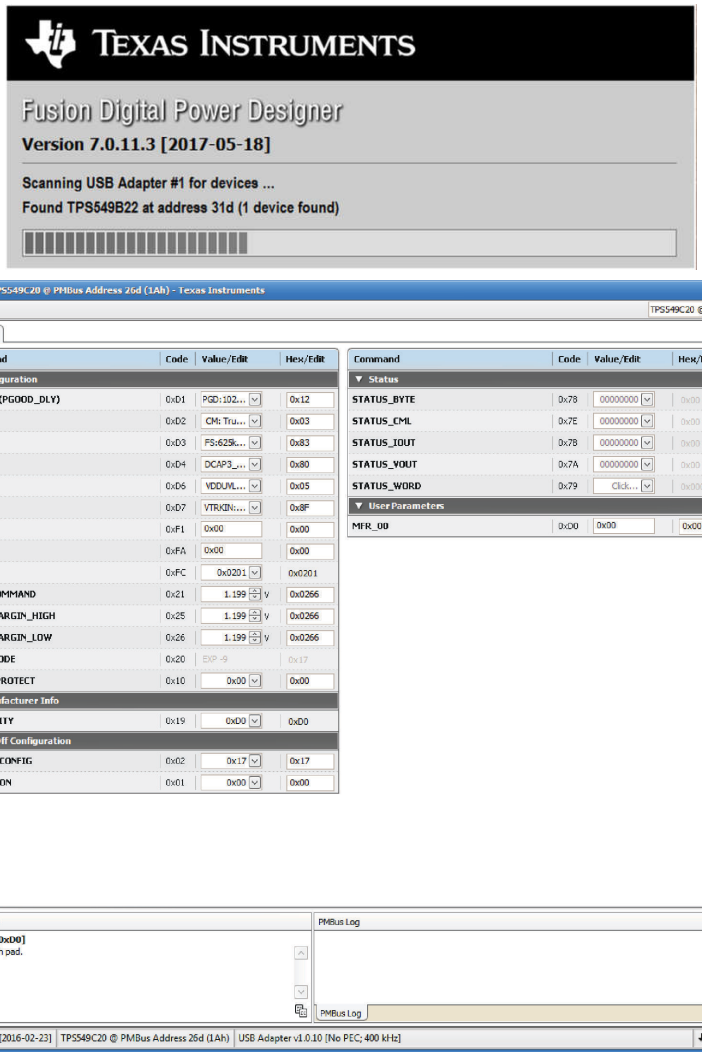
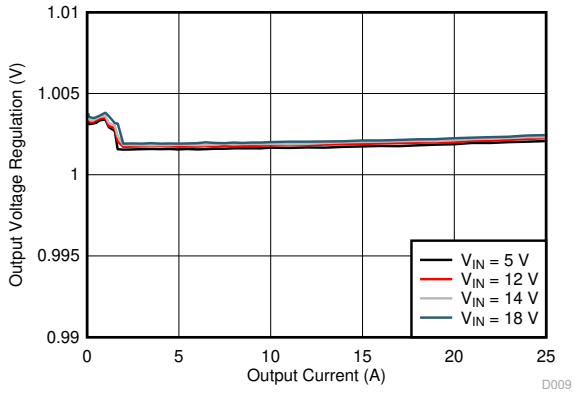


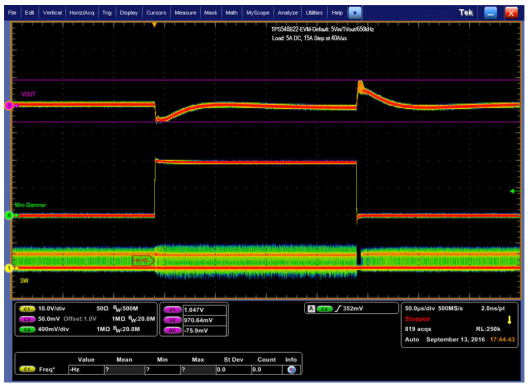
図 8-2. VOUT Command Graphic User Interface

8.2.4 Application Curves



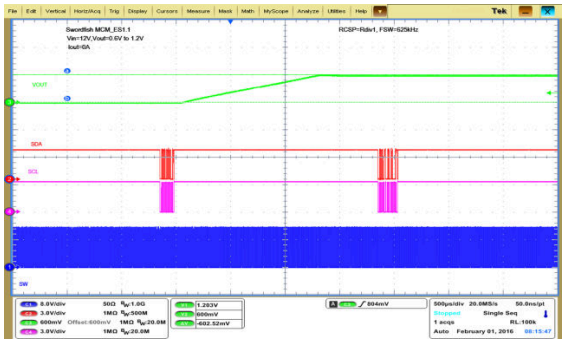
$V_{DD} = V_{IN}$
V_{OUT} = 1 V
f_{SW} = 650 kHz
SKIP Mode

図 8-3. Output Voltage Regulation vs. Output Current



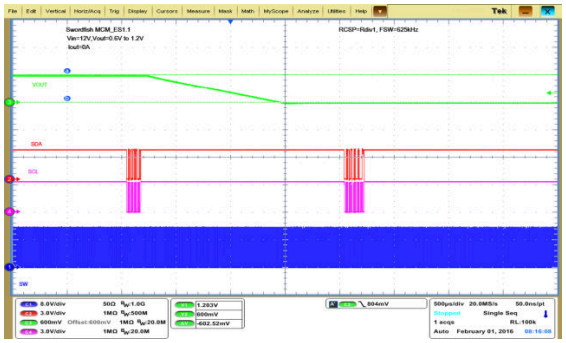
$V_{DD} = V_{IN}$ = 5 V
V_{OUT} = 1 V
5-A DC with 15-A step at 40A/µs
f_{SW} = 650 kHz
FCCM mode

図 8-4. Transient Response Peak-to-Peak



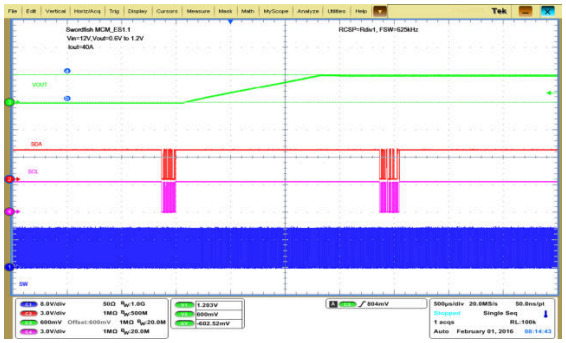
V_{IN} = 12 V
I_{OUT} = 0 A
V_{OUT} = 0.6 V to 1.2 V

図 8-5. VOUT Command



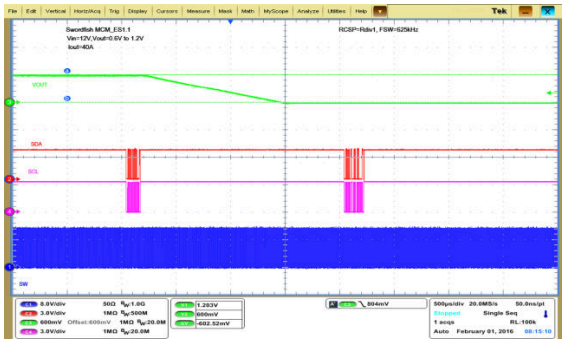
V_{IN} = 12 V
I_{OUT} = 0 A
V_{OUT} = 1.2 V to 0.6 V

図 8-6. VOUT Command



V_{IN} = 12 V
I_{OUT} = 40 A
V_{OUT} = 0.6 V to 1.2 V

図 8-7. VOUT Command



V_{IN} = 12 V
I_{OUT} = 40 A
V_{OUT} = 1.2 V to 0.6 V

図 8-8. VOUT Command

8.3 Power Supply Recommendations

This device is designed to operate from an input voltage supply between 1.5 V and 18 V. Ensure the supply is well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance,

as is the quality of the PCB layout and grounding scheme. See the recommendations in the セクション 8.4 section.

8.4 Layout

8.4.1 Layout Guidelines

Consider these layout guidelines before starting a layout work using TPS549B22.

- Making sure that all GND pins, including AGND (pin 30), DRGND (pin 29), and PGND (pins 13, 14, 15, 16, 17, 18, 19, and 20) are connected directly to the thermal pad underneath the device via traces or plane is absolutely ciritical.
- Include as many thermal vias as possible to support a 25-A thermal operation. For example, a total of 35 thermal vias are used (outer diameter of 20 mil) in the TPS49B22EVM-847, which is available for purchase at www.ti.com.
- Placed the power components (including input/output capacitors, output inductor and TPS549B22 device) on one side of the PCB (solder side). Insert at least two inner layers (or planes) connected to the power ground, to shield and isolate the small signal traces from noisy power lines.
- Place the VIN pin decoupling capacitors as close as possible to the PVIN and PGND pins to minimize the input AC current loop. Place a high-frequency decoupling capacitor (with a value between 1 nF and 0.1 µF) as close to the PVIN pin and PGND pin as the spacing rule allows. This placement helps suppress the switch node ringing.
- Place VDD and BP decoupling capacitors as close as possible to the device pins. Do not use PVIN plane connection for the VDD pin. Separate the VDD signal from the PVIN signal by using separate trace connections. Provide GND vias for each decoupling capacitor and make the loop as small as possible.
- Make sure that the PCB trace defined as switch node (which connects the SW pins and up-stream of the output inductor) are as short and wide as possible. In the TPS49B22EVM-847 design, the SW trace width is 200 mil. Use a separate via or trace to connect SW node to snubber and bootstrap capacitor. Do not combine these connections.
- Place all sensitive analog traces and components (including VOSNS, RSP, RSN, ILIM, MODE, VSEL and ADDR) far away from any high voltage switch node (itself and others), such as SW and BOOT to avoid noise coupling. In addition, place MODE, VSEL and ADDR programming resistors near the device pins.
- The RSP and RSN pins operate as inputs to a differential remote sense amplifier that operates with very high impedance. It is essential to route the RSP and RSN pins as a pair of diff-traces in Kelvin-sense fashion. Route them directly to either the load sense points (+ and –) or the output bulk capacitors. The internal circuit uses the VOSNS pin for on-time adjustment. It is critical to tie the VOSNS pin directly tied to VOUT (load sense point) for accurate output voltage result.
- Pins 6, 7, and 26 are not connected in the 25-A TPS549B22 device, while pins 6, and 7 connect to SW and pins 26 connects to PVIN in the 40-A TPS549D22 device.

8.4.2 Layout Examples

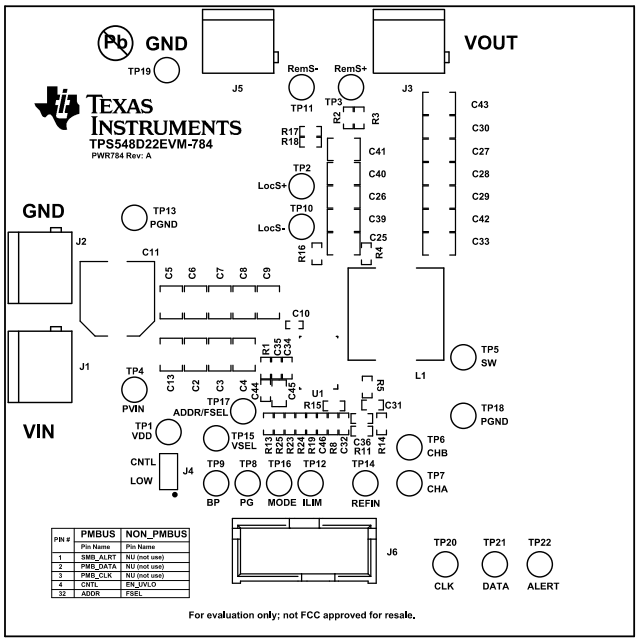


図 8-9. EVM Top View

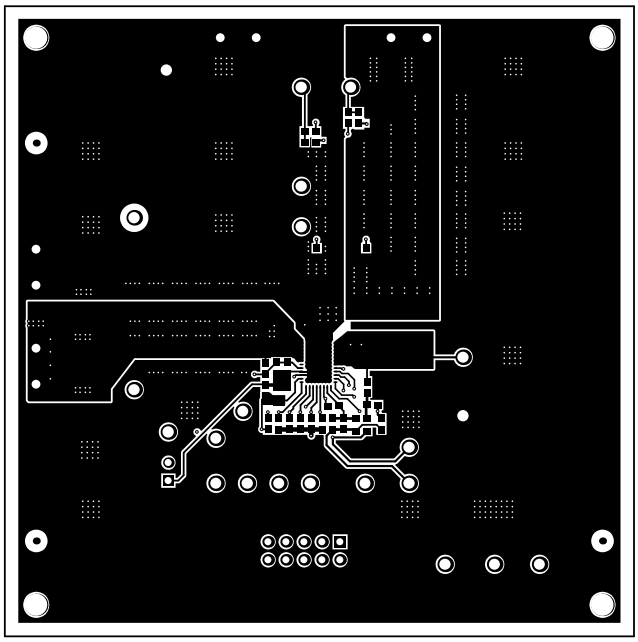


図 8-10. EVM Top Layer

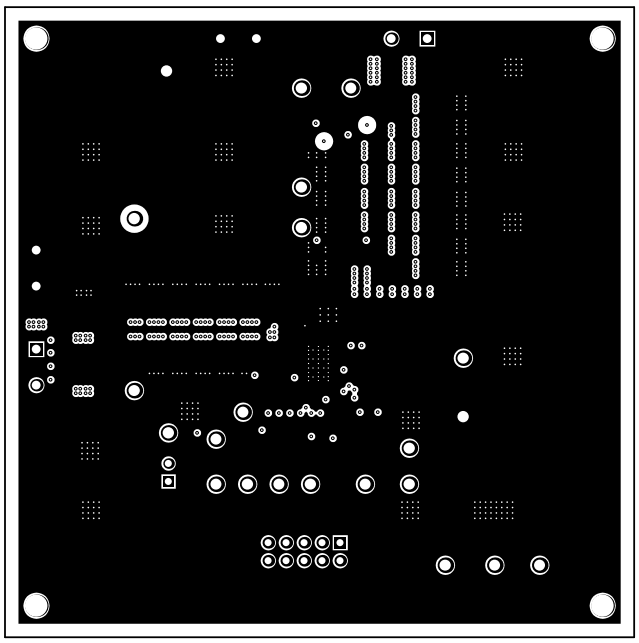


図 8-11. EVM Inner Layer 1

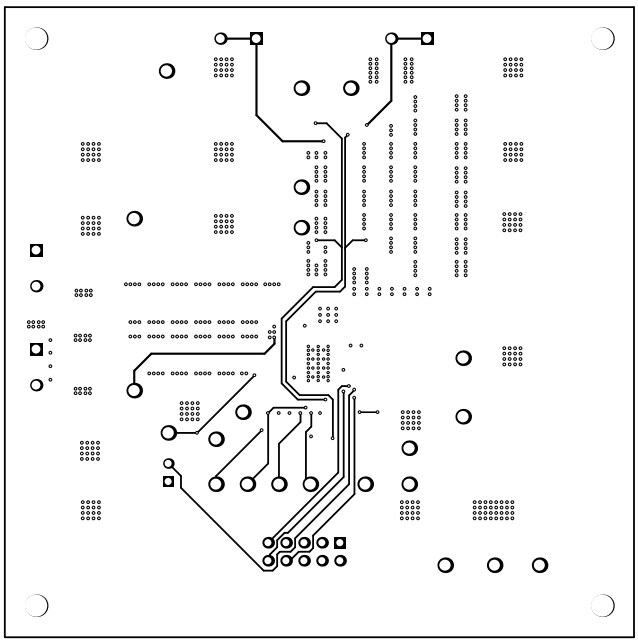


図 8-12. EVM Inner Layer 2

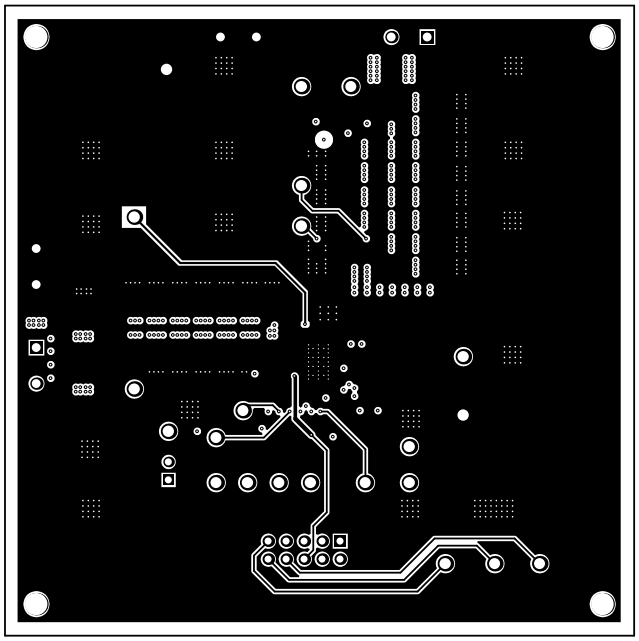


図 8-13. EVM Inner Layer 3

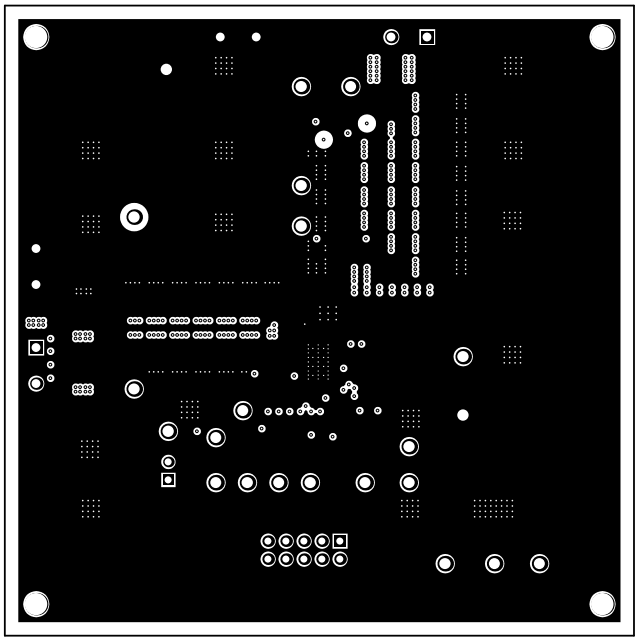


図 8-14. EVM Inner Layer 4

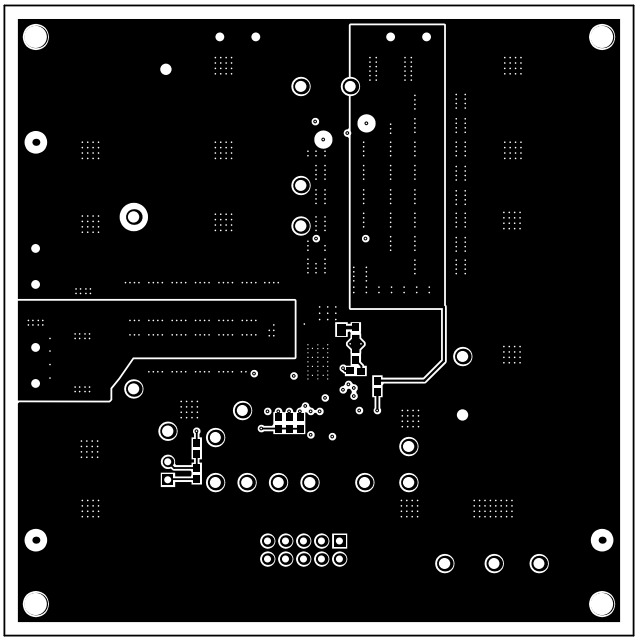


図 8-15. EVM Bottom Layer

8.4.3 Mounting and Thermal Profile Recommendation

Proper mounting technique adequately covers the exposed thermal tab with solder. Excessive heat during the reflow process can affect electrical performance. 図 8-16 shows the recommended reflow oven thermal profile. Proper post-assembly cleaning is also critical to device performance. See

QFN/SON PCB Attachment for more information.

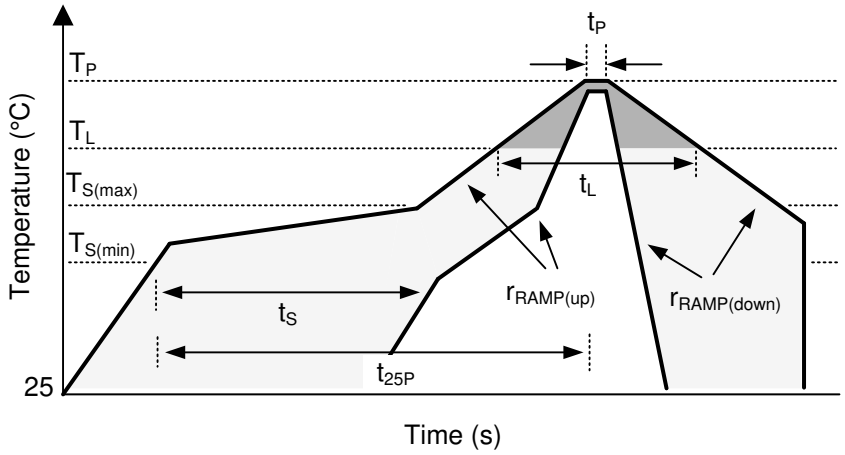


図 8-16. Recommended Reflow Oven Thermal Profile

表 8-4. Recommended Thermal Profile Parameters

PARAMETER		MIN	TYP	MAX	UNIT
RAMP UP AND RAMP DOWN					
$r_{RAMP(up)}$	Average ramp-up rate, $T_{S(max)}$ to T_P			3	°C/s
$r_{RAMP(down)}$	Average ramp-down rate, T_P to $T_{S(max)}$			6	°C/s
PRE-HEAT					
T_S	Pre-heat temperature	150		200	°C
t_S	Pre-heat time, $T_{S(min)}$ to $T_{S(max)}$	60		180	s
REFLOW					
T_L	Liquids temperature		217		°C
T_P	Peak temperature			260	°C
t_L	Time maintained above liquidus temperature, T_L	60		150	s
t_P	Time maintained within 5°C of peak temperature, T_P	20		40	s
t_{25P}	Total time from 25°C to peak temperature, T_P			480	s

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS549B22 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Snubber Circuits: Theory, Design and Application* seminar

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.5 Trademarks

SWIFT™, D-CAP3™, NexFET™, and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.
PMBus® is a registered trademark of SMIF, Inc..
WEBENCH® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (June 2017) to Revision A (February 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 古い用語を使用している部分のすべてをコントローラとターゲットに変更	1
• 商標の情報を更新	1
• Updated parameters in the *Electrical Characteristics* table	6

11 Mechanical, Packaging, and Orderable Information

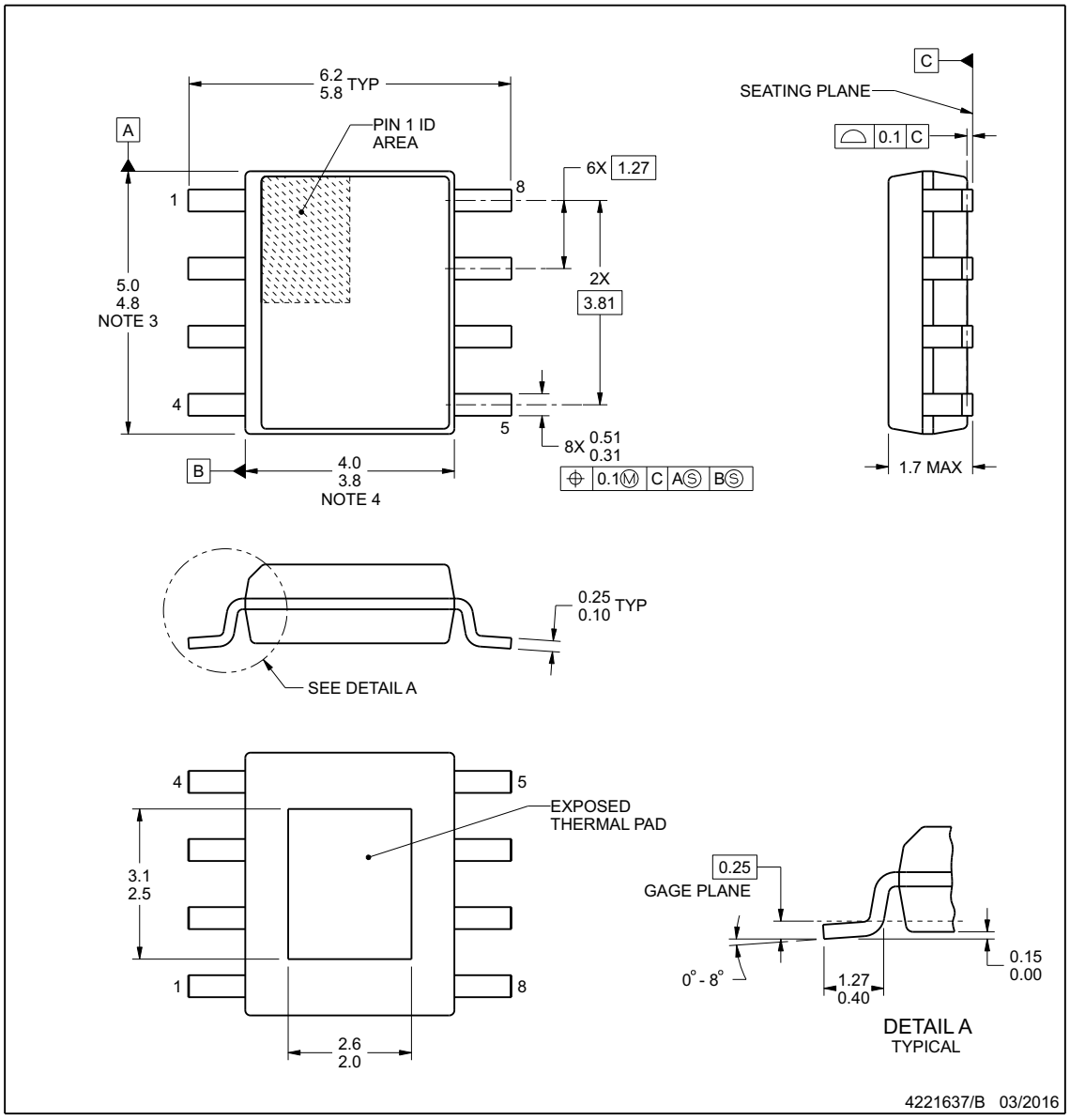
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

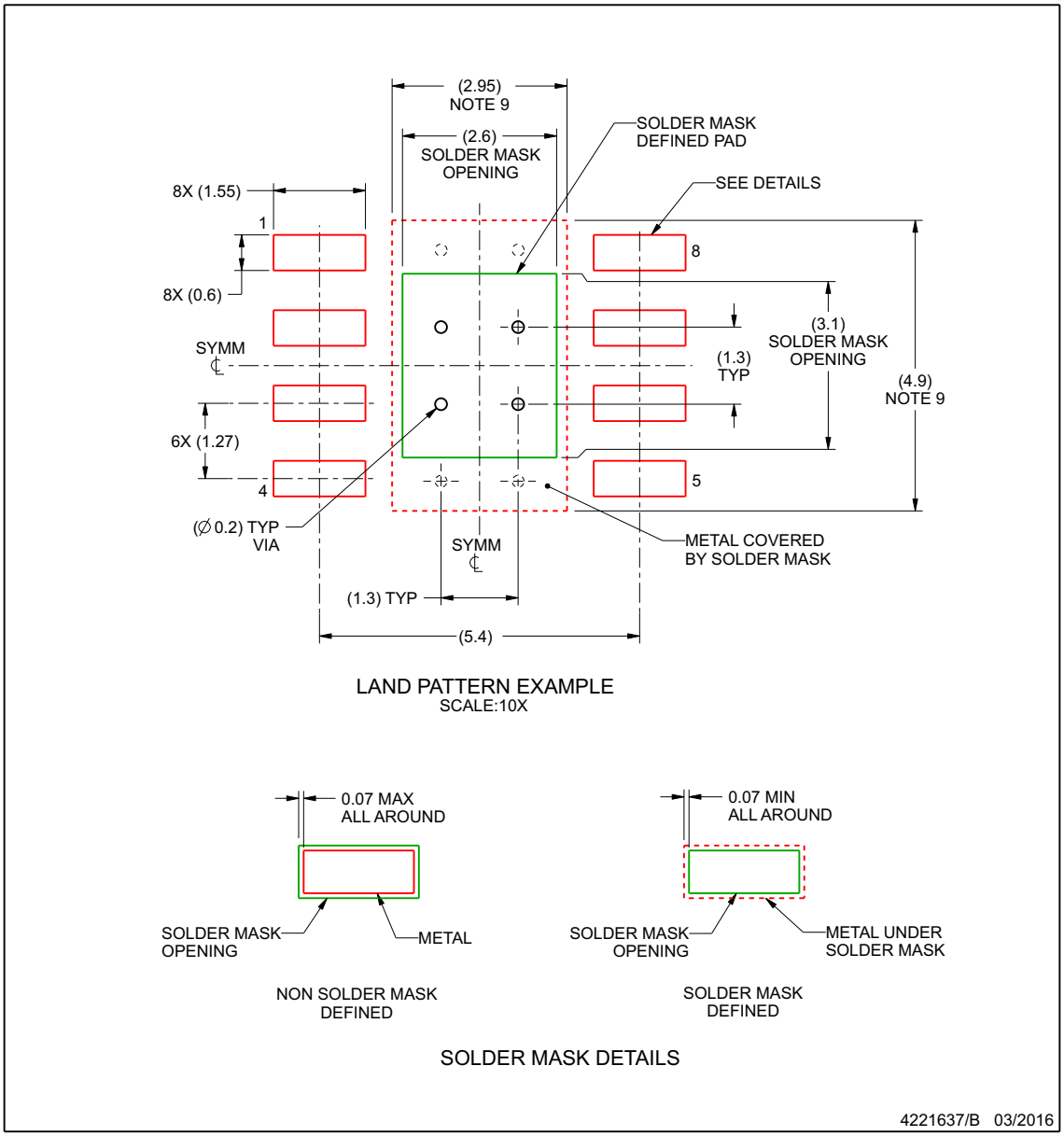
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

EXAMPLE BOARD LAYOUT

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

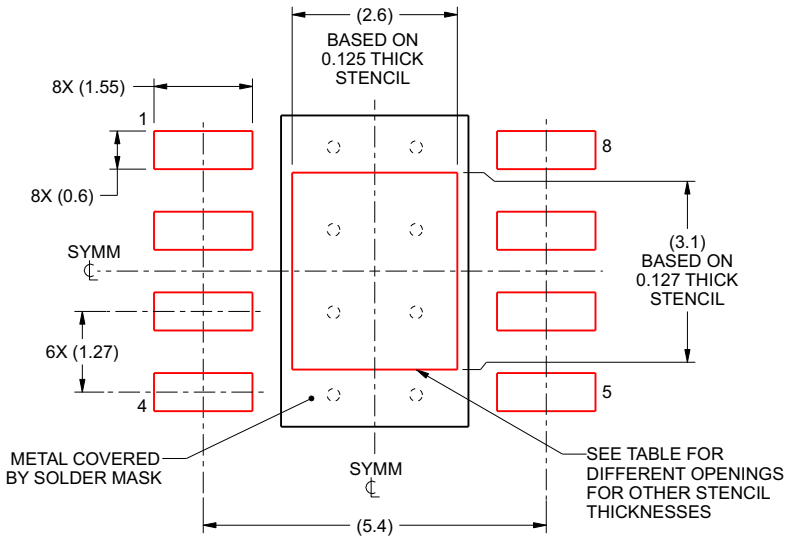
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS549B22RVFR	Active	Production	LQFN-CLIP (RVF) | 40	2500 | LARGE T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	(549B22, 549B22A1)
TPS549B22RVFR.A	Active	Production	LQFN-CLIP (RVF) | 40	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(549B22, 549B22A1)
TPS549B22RVFR.B	Active	Production	LQFN-CLIP (RVF) | 40	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS549B22RVFT	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	(549B22, 549B22A1)
TPS549B22RVFT.A	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(549B22, 549B22A1)
TPS549B22RVFT.B	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
TPS549B22RVFTG4	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	549B22
TPS549B22RVFTG4.A	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	549B22
TPS549B22RVFTG4.B	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

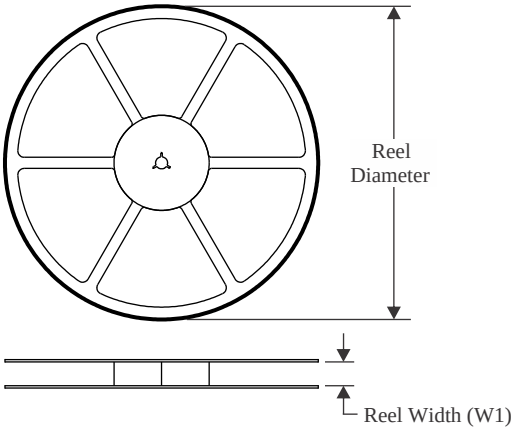
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

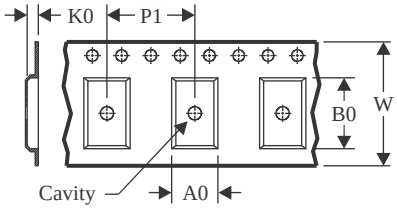
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

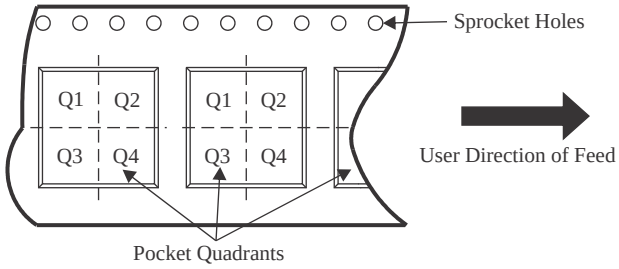


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

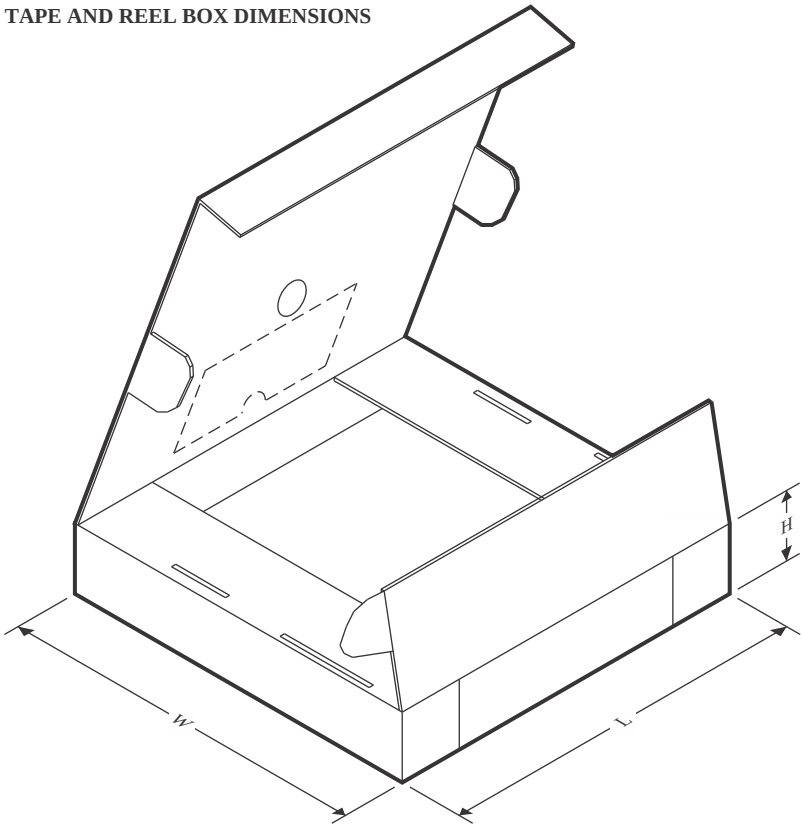
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS549B22RVFR	LQFN-CLIP	RVF	40	2500	330.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1
TPS549B22RVFT	LQFN-CLIP	RVF	40	250	180.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1
TPS549B22RVFTG4	LQFN-CLIP	RVF	40	250	180.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

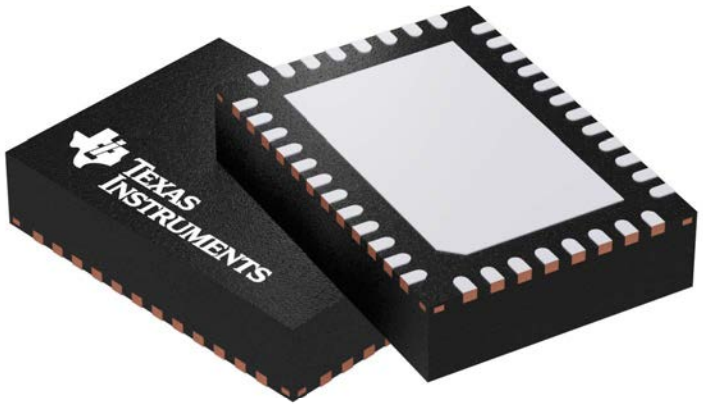


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS549B22RVFR	LQFN-CLIP	RVF	40	2500	367.0	367.0	38.0
TPS549B22RVFT	LQFN-CLIP	RVF	40	250	210.0	185.0	35.0
TPS549B22RVFTG4	LQFN-CLIP	RVF	40	250	210.0	185.0	35.0

RVF 40 LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



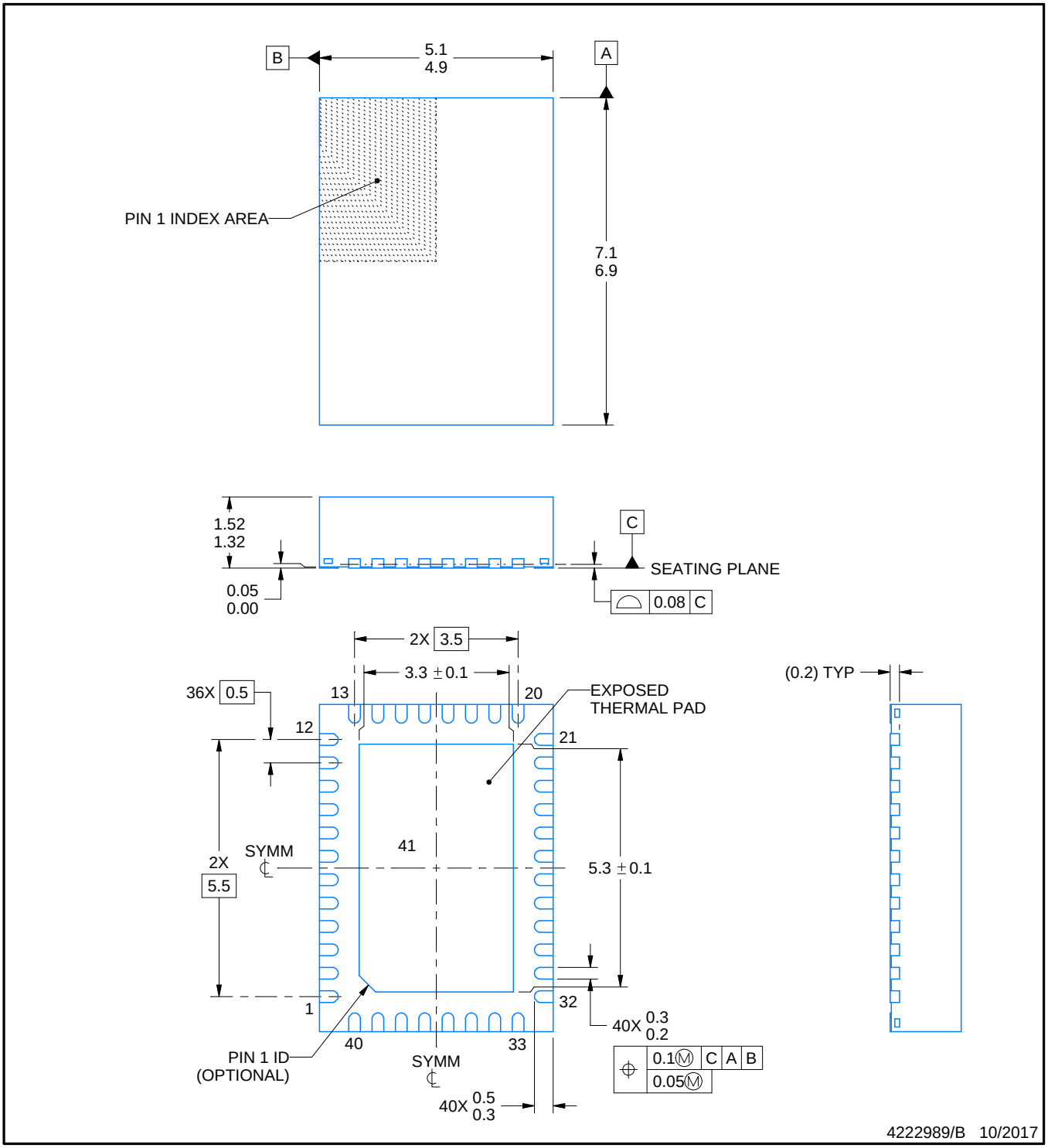
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RVF0040A

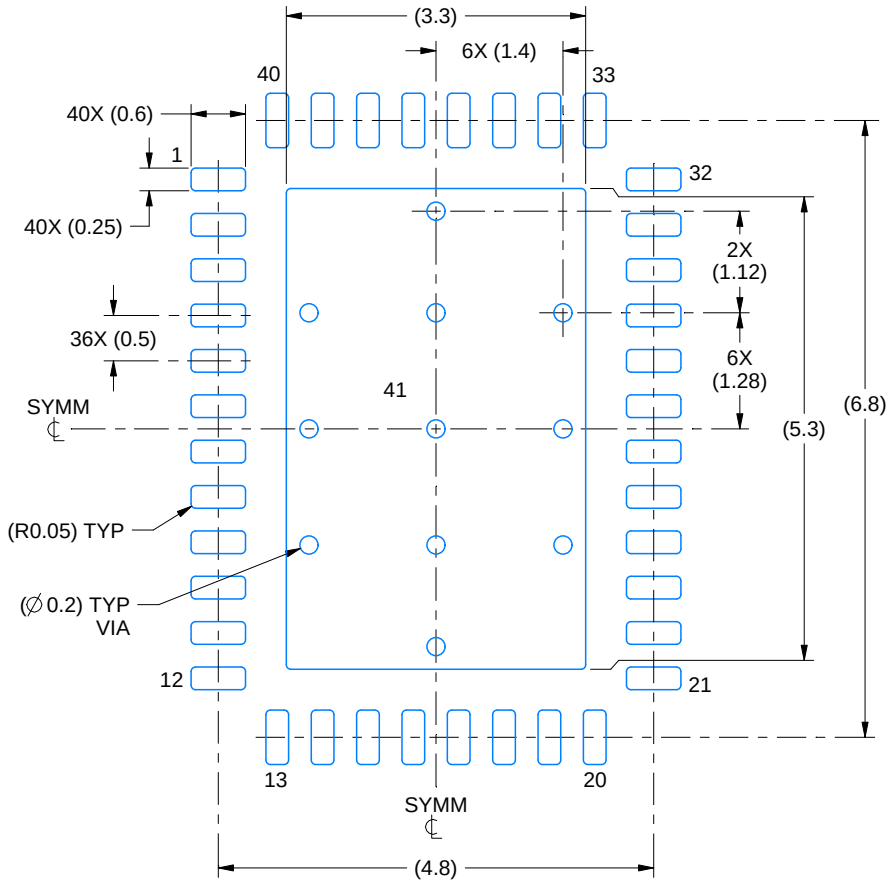
LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

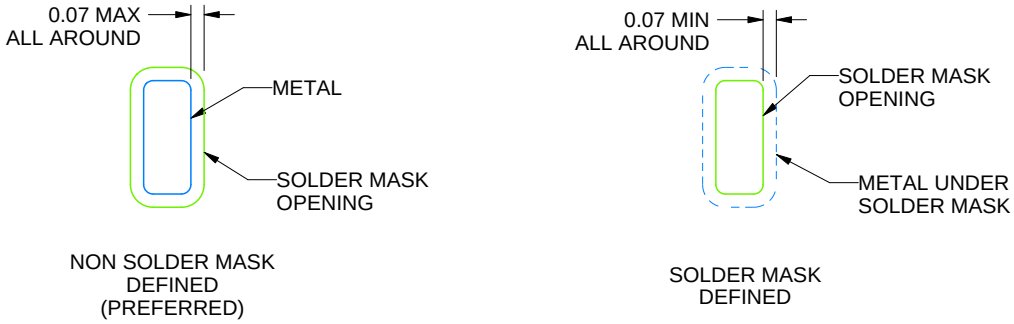


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
SCALE:12X

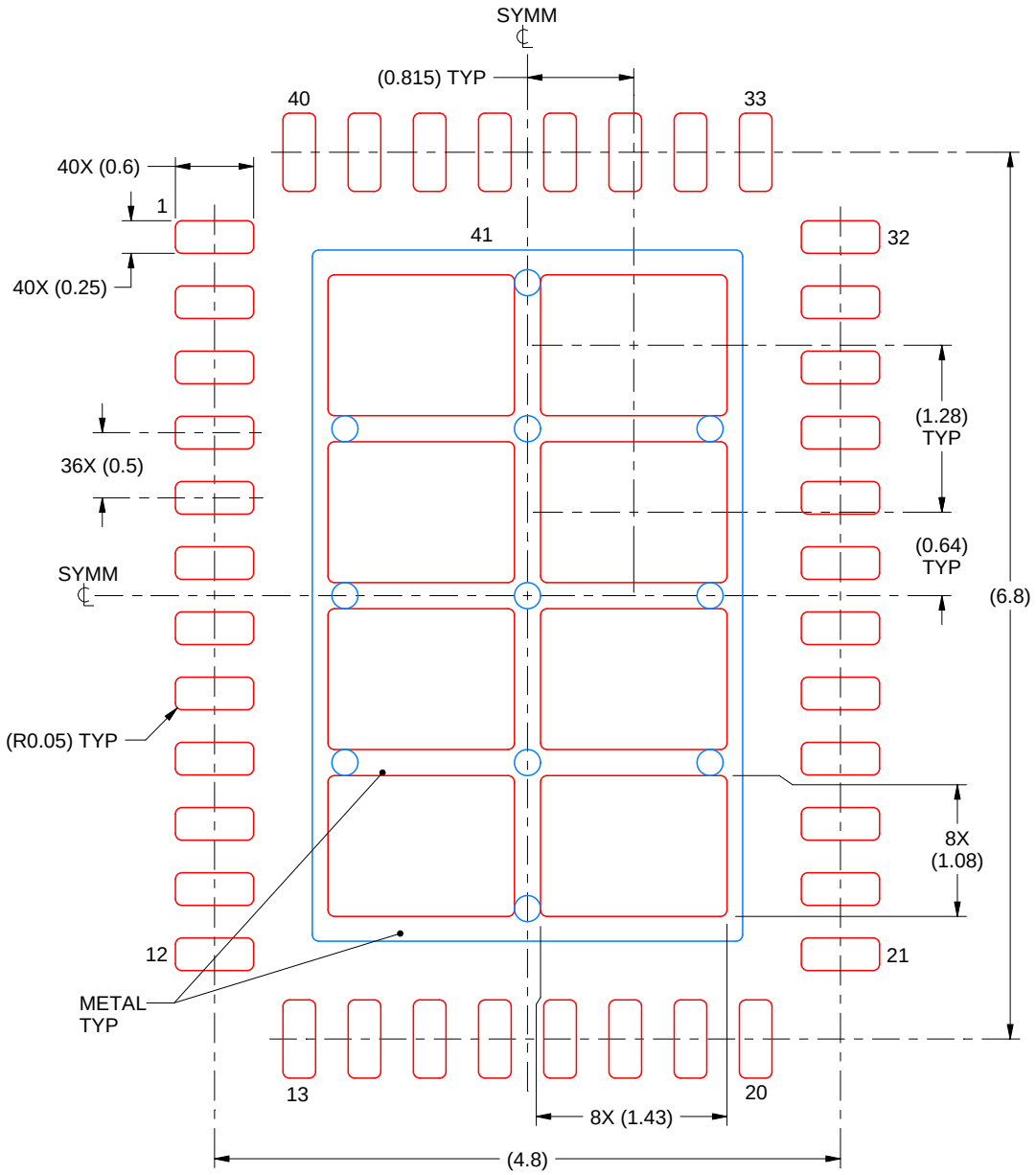


SOLDER MASK DETAILS

4222989/B 10/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
71% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222989/B 10/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265