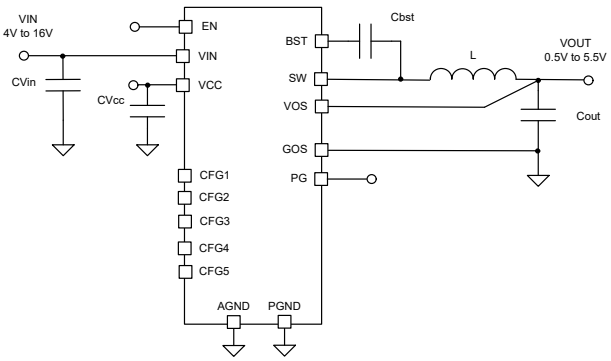
TPS548B23 4V～16V 入力、20A、リモート センス、D-CAP4、同期整流降圧コンバータ

1 特長

- 入力電圧範囲:4V～16V
- 3.13V～5.3V の外部 VCC バイアスをサポート
- 10mΩ および 3.3mΩ MOSFET (V_{VCC} = 3.3V)
- 連続出力電流:20A
- 効率と放熱性能向けに最適化された 19 ピン WQFN-HR パッケージ
- T_J = -40℃～+125℃で ±1.0% の基準電圧 (VREF)
- 出力電圧範囲:0.5V～5.5V
- 差動リモート センス
- D-CAP4 による超高速負荷ステップ応答
- すべての出力コンデンサでセラミック コンデンサの使用をサポート
- 軽負荷時の高効率を実現する自動スキップ Eco モードを選択可能
- バレー電流制限を でプログラム可能
- 600kHz、800kHz、1.0MHz、1.2MHz、で選択可能なスイッチング周波数:
- ソフトスタート時間をプログラム可能
- プリバイアス付きスタートアップ機能
- オープン ドレインのパワー グッド出力
- 過電圧および低電圧フォルト保護
- 3mm × 3mm (0.4mm ピン ピッチ)、19 ピン QFN パッケージ
- 12A の TPS548A23 および 6A の TPS548623 とピン互換

2 アプリケーション

- ラック サーバーとブレード サーバー
- データ センター向けスイッチ



概略回路図

3 概要

TPS548B23 デバイスは、適応型オン時間 D-CAP4 制御モードを備えた小型で高効率の同期整流降圧コンバータです。この制御方式により、外部補償ネットワークを必要とせずに、出力電圧範囲全体にわたって低い最小オン時間と高速負荷過渡応答を実現できます。外部補償が不要のため、本デバイスは使いやすく、外付け部品をほとんど必要としません。 このデバイスは、スペースに制約のあるデータ センター アプリケーションに適した設計になっています。

TPS548B23 デバイスには差動リモート センス、高性能の内蔵 MOSFET、高精度の内蔵 ±1.0% 基準が搭載されています。このデバイスの特長は、正確な負荷およびライン レギュレーションと、Eco モードまたは強制連続導通モード (FCCM) 動作です。複数のピンストラップ オプションを使用して、過電流制限、フォルト応答、内部または外部のフィードバック、出力電圧の選択、スイッチング周波数、ソフト スタート時間を設定できます。

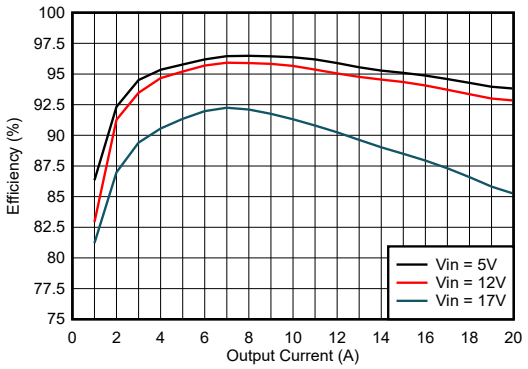
内蔵の 3.0V LDO は、VCC ピンを介して 3.3V～5V の外部電源でオーバードライブできるため、効率向上と消費電力低減を実現できます。

TPS548B23 デバイスは鉛フリー デバイスです。RoHS に準拠しています (適用除外なし)。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS548B23	VAN (WQFN-HR、19)	3mm × 3mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション効率 (V_{IN} = 12V、外部 VCC = 3.3V、FCCM、Fsw = 800kHz、, DCR = 1.4mΩ)

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4 Device Comparison Table

Device Number	Maximum Output Current	V_O Adjust	Pin Strap Configurability	Digital Interface	Telemetry
TPS548B23	20A	0.5V – 5.5V	Internal, External FB, F_{SW}, FCCM/PFM, OCP, Hiccup.Latch-off, SS time	NA	No
TPS548A23	12A				
TPS548623	6A				
TPS544B28	20A	0.4V – 5.5V	Internal, External FB, F_{SW}, FCCM/PFM, RAMP, OCP, Hiccup.Latch-off	PMBus	Yes
TPS544A28	12A				
TPS544628	6A				
TPS544B26	20A			I^2C	
TPS544A26	12A				
TPS544626	6A				

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5 Pin Configuration and Functions

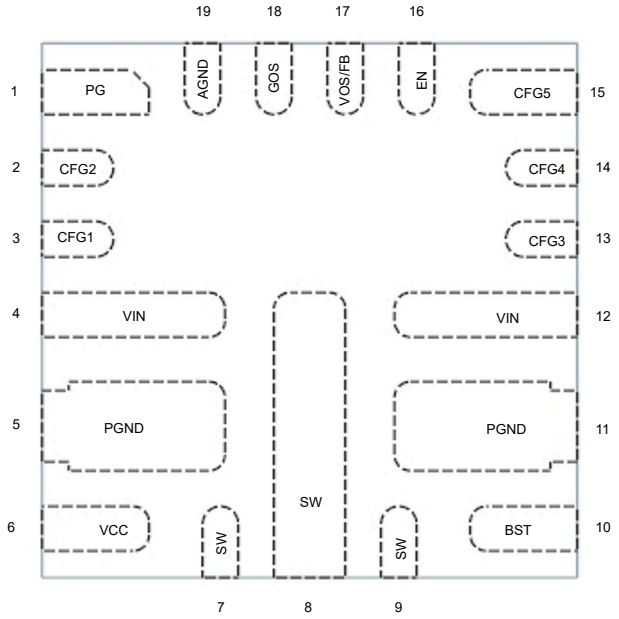

図 5-1. VAN Package, 19-Pin, 3mm × 3mm (0.4mm Pin Pitch) WQFN-HR (Top View)

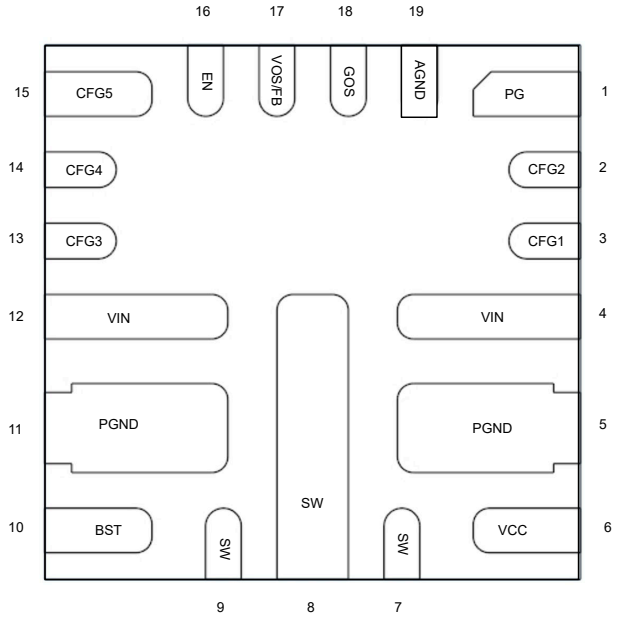

図 5-2. VAN Package, 19-Pin, 3mm × 3mm (0.4mm Pin Pitch) WQFN-HR (Bottom View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO		
PG	1	O	Open-drain power-good status signal. Connect an external pullup resistor to a voltage source. When the FB voltage moves outside the specified limits, PG goes low after the specified delay.
CFG2	2	I	Multi-function select pin. Connection to AGND, VCC, or floating this pin selects between the operating frequency, and the overcurrent limit. When configured for external FB operation, connecting a resistor between this pin and AGND sets the OCP limit.
CFG1	3	I	Multi-function select pin. Connection to AGND, VCC, or floating this pin selects between the operating frequency, and the over current limit. When configured for external FB operation, connecting a resistor between this pin and AGND selects switching frequency, SS time, and fault recovery (hiccup or latch-off) mode.
VIN	4, 12	P	Power-supply input pins for both the power stage MOSFETs and the internal LDO. Place the decoupling input capacitors from VIN pins to PGND pins as close as possible. A capacitor from each VIN to PGND close to IC is required.
PGND	5, 11	G	Ground return for the power stage. This pin is internally connected to the source of the low-side MOSFET. Place as many vias as possible beneath the PGND pins and as close as possible to the PGND pins. This action minimizes parasitic impedance and also lowers thermal resistance.
VCC	6	P	Internal 3V LDO output. A 3.3V or 5V external bias can be connected to this pin to save the power losses on the internal LDO. The voltage source on this pin powers both the internal circuitry and gate driver. Bypass with a 1µF, > 6.3V rating, ceramic capacitor from VCC pin to PGND. Place this capacitor as close to the VCC and PGND pins as possible.
SW	7, 8, 9	O	Output switching terminal of the power converter. Connect this pin to the output inductor.
BST	10	I/O	Supply for the internal high-side MOSFET gate driver (boost terminal). Connect the bootstrap capacitor from this pin to SW node.
CFG3	13	I	Multi-function select pins. Connection CFGx to AGND, VCC, or floating this pin selects the output voltage setting/configuration (internal or external FB) and forced continuous conduction mode (FCCM) or skip-mode operation, .
CFG4	14	I	
CFG5	15	I	
EN	16	I	Enable pin. The enable pin turns the DC/DC switching converter on or off. Floating EN pin before start-up disables the converter. The recommended maximum voltage applied to the EN pin is 5.5V. TI *does not* recommend connecting the EN pin to VIN pin directly.
VOS/FB	17	I	Output voltage feedback input. Positive input of the differential remote sense circuit, connect to the Vout sense point on the load side. When configured for external feedback, a resistor divider from the VOUT to GOS (tapped to FB pin) sets the output voltage.
GOS	18	I	Negative input of the differential remote sense circuit. Connect to a ground sense point near the load.
AGND	19	G	Analog ground return and reference for the internal control circuits.

(1) I = Input, O = Output, P = Supply, G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	19	V
Pin voltage	SW - PGND, DC	–0.3	19	V
Pin voltage	VIN – SW, DC	–0.3	19	V
Pin voltage	VIN – SW, transient < 10ns	–3	25	V
Pin voltage	BOOT - PGND	–0.3	24.5	V
Pin voltage	BOOT – SW	–0.3	5.5	V
Pin voltage	EN	–0.3	7	V
Pin voltage	VOS/FB, PG, CFGx, VCC	–0.3	6	V
Pin voltage	GOS, PGND	–0.3	0.3	V
Sink current	PG		15	mA
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	VIN	4		16	V
Pin voltage		V_{GOS} versus V_{AGND}	–0.1		0.1	V
		EN, PG	–0.1		5.5	V
V_{VCC}	External bias range	VCC, V_{VIN} ≤ 16V	–0.1		5.3	V
V_{OUT}	Output voltage range	VOUT	0.5		5.5	V
I_{PG}	Power-good sinking current	PG			10	mA
I_{OUT}	Output current	SW			20	A
IL_{PEAK}	Maximum peak inductor current	SW			31	A
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS548B23		UNIT
		VAN (QFN, JEDEC layout)	VAN (QFN, application layout, 6-layer PCB)	
		19 PINS	19 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	21.0[2]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	Not applicable [3]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	Not applicable [3]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD		°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD		°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD		°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Measured on 4 layer, 2oz copper, 3 inch × 3 inch layout with 1.9W dissipated in the device.
(3) The thermal test or simulation setup is not applicable to an application layout.

6.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VCC} = 3.3V (external), V_{VIN} = 4V to 16V. Typical values are at T_J = 25°C and V_{VIN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{EN} = 2V, V_{FB} = V_{FB_REG} + 50mV, no external bias on VCC pin		970		µA
$I_{Q(VIN)}$	VIN quiescent current with external VCC bias	T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, V_{FB} = V_{FB_REG} + 10mV (non-switching), 3.3V external bias on VCC pin		230	290	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{IN} = 12 V, V_{EN} = 0 V, no external bias on VCC pin		9.5	20	µA
$I_{Q(VCC)}$	VCC quiescent current	T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, V_{FB} = V_{FB_REG} + 10mV (non-switching), 3.3 V external bias on VCC pin		860		µA
$I_{SD(VCC)}$	VCC shutdown current	V_{EN} = 0V, V_{IN} = 0V, 3.3V external bias on VCC pin		90		µA
I_{VCC}	VCC external bias current	T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, regular switching, f_{SW} = 600kHz, 3.3V external bias on VCC pin		10		mA
I_{VCC}	VCC external bias current	T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, regular switching, f_{SW} = 1200kHz, 3.3V external bias on VCC pin		16		mA
INTERNAL LDO (VCC)						
V_{VCC}	Internal LDO output voltage		2.85	3.0	3.1	V
I_{VCC}	Internal LDO short-circuit current limit	V_{VIN} = 12V	50	180		mA
$VCC_{UVLO(R)}$	VCC UVLO rising threshold	V_{VIN} = 4V		2.8	2.85	V
$VCC_{UVLO(F)}$	VCC UVLO falling threshold	V_{VIN} = 4V		2.65		V
$VCC_{UVLO(H)}$	VCC UVLO hysteresis	V_{VIN} = 4V		0.15		V
	FB threshold to turn off VCC LDO	V_{FB} falling, EN = 0V		50	85	mV
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising		3.92	3.99	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling		3.77	3.83	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.15		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.15	1.2	1.25	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	1.06	1.12	1.18	V
$V_{EN(H)}$	EN voltage hysteresis			80		mV
$I_{EN(Hys)}$	EN pin hysteresis current	EN > $V_{EN(R)}$		5		µA

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6.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VCC} = 3.3V (external), V_{VIN} = 4V to 16V. Typical values are at T_J = 25°C and V_{VIN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	EN internal pulldown resistance	EN pin to AGND	0.74	1	1.27	MΩ
$V_{ENSTB(R)}$	EN standby rising threshold	EN rising, enable internal LDO, no switching		0.7		V
$V_{ENSTB(F)}$	EN standby falling threshold	EN Falling, disable internal LDO	0.3	0.6		V
PINSTRAP						
CFGx_high	CFGx logic high voltage level	VCC = 5.0V	3.6	4.2		V
		VCC = 3.3V	2.0	2.4		V
CFGx_low	CFGx logic low voltage level	VCC = 5.0V		0.7	1.0	V
		VCC = 3.3V		1.0	1.3	V
R_{CFG1_TRIP}	CFG2 resistor step range accuracy	External feedback configuration (CFG3-5 = GND)	– 4%		+ 4%	
STARTUP						
t_{SS}	Soft-start time	From start of switching to V_{FB} = 0.5V, t_{SS} = 1ms setting	0.5	1	1.5	ms
		From start of switching to V_{FB} = 0.5V, t_{SS} = 2ms setting	1.4	2	2.6	ms
		From start of switching to V_{FB} = 0.5V, t_{SS} = 3ms setting	2	3	4	ms
	EN HIGH to start of switching delay			800		µs
REFERENCE VOLTAGE (FB)						
V_{VOS_REG}	Output volatge regulation accuracy	Internal feedabck configuration, T_J = 0°C to +85°C	– 0.75 %		+ 0.75 %	
		Internal feedback configuration	– 1.25 %		+1.25 %	
V_{FB_REG}	Feedback regulation voltage	External Feedback Configuration, T_J = 0°C to +85°C	497.5	500	502.5	mV
		External Feedback Configuration	495	500	505	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = V_{FB_REG}			160	nA
DIFFERENTIAL REMOTE SENSE AMPLIFIER						
I_{GOSNS}	Leakage current out of GOS pin	V_{GOS} - V_{AGND} = 100mV			80	µA
V_{ICM}	GOS common mode voltage for regulation	V_{GOS} versus V_{AGND}	– 0.1		0.1	V
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 600kHz, No load	510	600	690	kHz
		V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 800kHz, No load	680	800	920	kHz
		V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 1.0MHz, No load	850	1000	1150	kHz
		V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 1.2MHz, No load	1020	1200	1380	kHz
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	$V_{BOOT-SW}$ = 5.0V		8		mΩ
		$V_{BOOT-SW}$ = 3.3V		9.9		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{VCC} = 5.0V		2.5		mΩ
		V_{VCC} = 3.3V		3		mΩ
$t_{ON(min)}$	Minimum ON pulse width			25		ns
$t_{OFF(min)}$	Minimum OFF pulse width				150	ns
	Output discharge resistor on SW pin	V_{IN} = 12V, V_{SW} = 1V, power conversion disabled		100		Ω
$I_{BOOT(LKG)}$	Leakage current into BOOT pin	$V_{BOOT-SW}$ = 3.3V, enabled, not switching.		30		µA
POWER GOOD						
$V_{PGTH(RISE\_OV)}$	Power-Good threshold	FB rising, PG high to low	113%	116%	119%	
$V_{PGTH(RISE\_UV)}$	Power-Good threshold	FB rising, PG low to high	89%	92.5%	95%	

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6.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VCC} = 3.3V (external), V_{VIN} = 4V to 16V. Typical values are at T_J = 25°C and V_{VIN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PGTH(FALL\_UV)}$	Power-Good threshold	FB falling, PG high to low	77%	80%	83%	
	PG delay going from low to high during startup			1.1	1.5	ms
	PG delay going from high to low			4	6.2	µs
$I_{PG(LKG)}$	PG pin leakage current when open drain output is high	V_{PG} = 4.5V			5	µA
	PG pin output low-level voltage	I_{PG} = 7\mA			500	mV
OVERCURRENT PROTECTION						
	OC limit high clamp	Valley current on LS FET, CFG3-5 = GND, 0Ω ≤ R_{ILIM} ≤ 4.32kΩ	19	21	23	A
$I_{LS(OC)}$	Low-side valley current limit	Valley current on LS FET, R_{ILIM} = 5.25kΩ	14.5	16	17.5	A
		Valley current on LS FET, R_{ILIM} = 10.5kΩ	7	8	9	A
		Valley current on LS FET, R_{ILIM} = 20.0kΩ	3.5	4.2	4.9	A
R_{ILIM}	ILIM pin resistance range		0		20	kΩ
	Low-side valley current limit	Valley current on LS FET, CFG3-5 = VCC, CFG1 = VCC	19	21	23	A
		Valley current on LS FET, CFG3-5 = VCC, CFG1 = Float	16	18	20	A
		Valley current on LS FET, CFG3-5 = VCC, CFG1 = GND	13	15	17	A
$I_{LS(NOC)}$	Low-side negative current limit	Sinking current limit on LS FET		–10	–8	A
I_{ZC}	Zero-cross detection current threshold to enter DCM, open loop	V_{IN} = 12V		–750		mA
$I_{ZC(HYS)}$	Zero-cross detection current threshold hysteresis after entering DCM, open loop	V_{IN} = 12V		1000		mA
OUTPUT OVP AND UVP						
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	V_{FB} rising	113%	116%	119%	
t_{OVPDLY}	OVP delay	With 100mV overdrive		650		ns
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	V_{FB} falling	77%	80%	83%	
t_{UVPDLY}	UVP filter delay			70		µs
	Hiccup wait time	Hiccup mode enabled		7 x t_{SS}		ms
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising	150	165		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			15		°C

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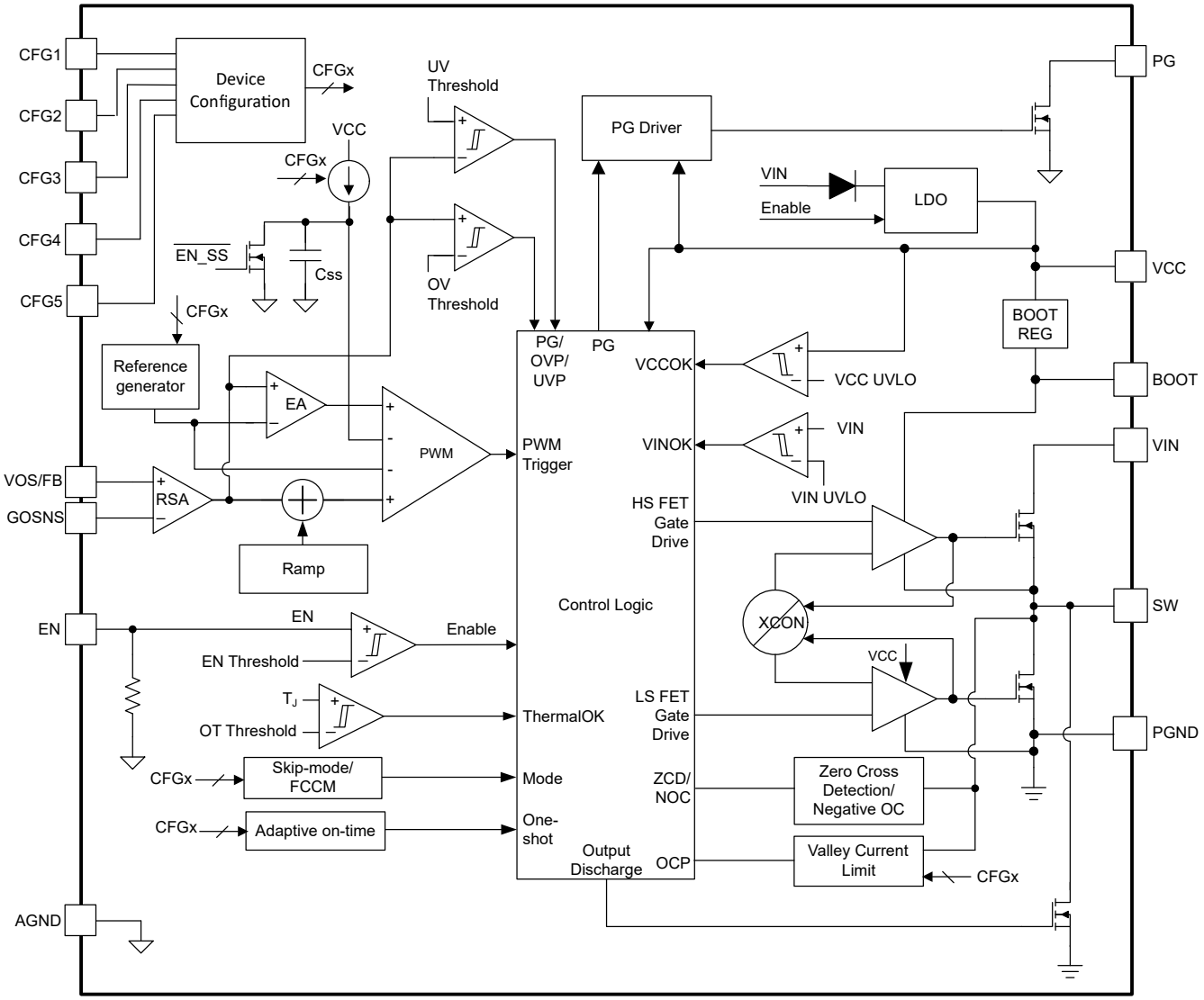
7 Detailed Description

7.1 Overview

The TPS548B23 device is a high-efficiency, single-channel, small-sized, synchronous buck converter. The device is designed for low output voltage point-of-load applications with 20A or lower output current in server, storage, and similar computing applications. The TPS548B23 features proprietary D-CAP4 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an ideal fashion. The output voltage set by the feedback voltage divider ranges from the internal voltage reference to 5.5V. The conversion input voltage ranges from 4V to 16V, and the VCC input voltage ranges from 3.13V to 5.3V. The D-CAP4 modulator uses emulated current information to control the modulation. The D-CAP4 modulator reduces loop gain variation with different output voltages providing better transient response in higher output voltage applications. An advantage of this control scheme is that this control scheme does not require a phase-compensation network outside which makes the device easy-to-use and also allows low external component count. Another advantage of this control scheme is that this control scheme supports stable operation with all low ESR output capacitors (such as ceramic capacitors and low ESR polymer capacitors). Lastly, adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during load-step transients.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 D-CAP4 Control

The device uses D-CAP4 control to achieve a fast load transient response while maintaining ease-of-use. The D-CAP4 control architecture includes an internal ripple generation network enabling the use of very low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC) and low ESR polymer capacitors. No external current sensing network or voltage compensators are required with D-CAP4 control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine with the voltage feedback signal to regulate the loop operation.

D-CAP4 control architecture reduces loop gain variation across V_{OUT}, enabling a fast load transient response across the entire output voltage range with one ramp setting. The R-C time-constant of the internal ramp circuit sets the zero frequency of the ramp, similar to other R-C based internal ramp generation architectures. The reduced variation in loop gain also mitigates the need for a feedforward capacitor to optimize the transient response. The ramp amplitude varies with V_{IN} to minimize variation in loop gain across input voltage, commonly referred to as input voltage feedforward. Lastly, the device uses internal circuitry to correct for the dc offset caused by the injected ramp, and significantly reduces the dc offset caused by the output ripple voltage, especially with light load current.

For any control topologies supporting no external compensation, there is a minimum range, maximum range, or both, for the output filter it can support. The output filter used for a typical buck converter is a low-pass L-C circuit. This L-C filter has double pole that is described in 式 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency L-C double pole has a 180-degree drop in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase by 90 degrees per decade above the zero frequency.

After identifying the application requirements, the output inductance is typically designed so the inductor peak-to-peak ripple current is approximately between 15% and 40% of the maximum output current in the application.

The inductor and capacitor selected for the output filter must be such that the double pole of 式 1 is located no higher than 1/30th of the steady-state operating frequency. Choosing very small output capacitance leads to a high frequency L-C double pole which causes the overall loop gain to stay high until the L-C double frequency. Given the zero from the internal ripple generation network is a relatively high frequency as well, the loop with very small output capacitance can have too high of a crossover frequency which can cause instability. The internal zero is selected by the resistor at the MSEL pin, as described earlier.

In general, where reasonable (or smaller) output capacitance is desired, output ripple requirement and load transient requirement can be used to determine the necessary output capacitance for stable operation.

For the maximum output capacitance recommendation, select the inductor and capacitor values so that the L-C double pole frequency is no less than 1/100th of the operating frequency. With this starting point, verify the small signal response on the board using the following criteria: The phase margin at the loop crossover is greater than 50 degrees. The actual maximum output capacitance can go higher as long as phase margin is greater than 50 degrees. However, small signal measurement (Bode plot) must be done to confirm the design.

If MLCCs are used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10µF, X5R and 6.3V, the derating by DC bias and AC bias are 80% and 50%, respectively. The effective derating is the product of these two factors, which in this case is 40% and 4µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the application.

For large output filters with an L-C double pole near 1/100th of the operating frequency, additional phase boost can be required. A feedforward capacitor placed in parallel with R_{FB_HS} can boost the phase. Refer to the *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* application note for details.

Besides boosting the phase, a feedforward capacitor feeds more V_{OUT} node information into the FB node through AC coupling. This feedforward during load transient event enables faster response of the control loop to a V_{OUT} deviation. However, this feedforward during steady state operation also feeds more V_{OUT} ripple and noise into FB. High ripple and noise on FB usually leads to more jitter, or even double-pulse behavior. To determine the final feedforward capacitor value impacts to phase margin, load transient performance, ripple, and noise on FB must all be considered. TI recommends using frequency analysis equipment to measure the crossover frequency and the phase margin.

7.3.2 Internal VCC LDO and Using External Bias On the VCC Pin

The TPS548B23 has an internal 3.0V LDO featuring input from VIN and output to VCC. When the EN voltage rises above the enable threshold ($V_{EN(R)}$), the internal LDO is enabled and starts regulating output voltage on the VCC pin. The VCC voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drivers.

Bypass the VCC pin with a 1µF, at least 6.3V rating ceramic capacitor. An external bias that is above the output voltage of the internal LDO can override the internal LDO. This enhances the efficiency of the converter because the VCC current now runs off this external bias instead of the internal linear regulator. An external bias of 5.0V can be used to provide additional efficiency enhancement by reducing the R_{DSON} of the integrated power MOSFETs.

The VCC UVLO circuit monitors the VCC pin voltage and disables the whole converter when VCC falls below the VCC UVLO falling threshold. Maintaining a stable and clean VCC voltage is required for a smooth operation of the device.

Considerations when using an external bias on the VCC pin are as follows:

- When the external bias is applied on the VCC pin early enough (for example, before EN signal comes in), the internal LDO pass device is always off and the internal analog circuits have a stable power supply rail at the power enable.
- This consideration is not recommended. When the external bias is applied on the VCC pin late (for example, after EN signal comes in), any power-up and power-down sequencing can be applied as long as there is no excess current pulled out of the VCC pin. With this sequence, be cautious of external discharge paths on the VCC pin which can pull a current higher than the current limit of the internal VCC LDO. A load exceeding the current limit of the internal VCC LDO can potentially pull the VCC voltage low and turn off the VCC LDO through the UVLO, thereby shutting down the converter output.
- A good power-up sequence is when at least one of VIN UVLO rising threshold or EN rising threshold is satisfied later than VCC UVLO rising threshold. For example, a practical power-up sequence is: VIN applied first, then the external bias applied, and then EN signal goes high.

7.3.2.1 Powering the Device From a Single Bus

The device works well when powered by a single V_{IN} configuration. In a single V_{IN} configuration, the internal LDO is typically powered by a 5V or 12V bus and generates a 3V output to bias the internal analog circuitry and power MOSFET gate drivers. The V_{IN} input range under this configuration is 4V to 16V for up to 20A load current. 図 7-1 shows an example for this single V_{IN} configuration.

V_{IN} and EN are the two signals to enable the part. For start-up sequence, any sequence between the V_{IN} and EN signals can power the device up correctly.

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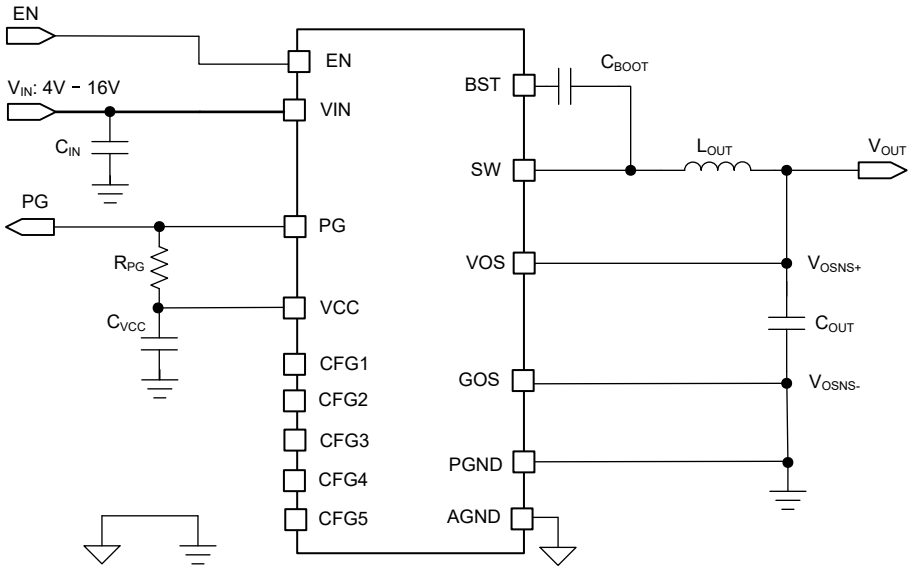

図 7-1. Single V_{IN} Configuration for a 12V Bus

7.3.2.2 Powering the Device From a Split-Rail Configuration

When an external bias, which is at a different level from main V_{IN} bus, is applied onto the VCC pin the device can be configured to split-rail by using both the main V_{IN} bus and VCC bias. Connecting a valid VCC bias to VCC pin overrides the internal LDO, thus saves power loss on the internal LDO. This configuration helps to improve overall system level efficiency but requires a valid VCC bias. A 3.3V or 5.0V rail is the common choice as VCC bias. With a stable VCC bias, the recommended V_{IN} input range under this configuration remains the same, from 4.0V to 16V.

The noise of the external bias affects the internal analog circuitry. To make sure of a proper operation, a clean, low-noise external bias and good local decoupling capacitor from VCC pin to PGND pin are required. 図 7-2 shows an example for this split rail configuration.

The VCC external bias current during nominal operation varies with the bias voltage level and also the operating frequency. For example, by setting the device to skip-mode, the VCC pin draws less current from the external bias when the frequency decreases under a light load condition. The typical VCC external bias current under FCCM operation is listed in *Electrical Characteristics.* The external bias must be capable of supplying this current or the external bias voltage can drop and the internal LDO can no longer be overridden.

Under split rail configuration, V_{IN}, VCC bias, and EN are the signals to enable the part. For start-up sequence, TI recommends that at least one of VIN UVLO rising threshold or EN rising threshold is satisfied later than VCC UVLO rising threshold. A practical start-up sequence example is:

1. V_{IN} applied
2. External VCC bias applied
3. EN signal goes high

Similarly, for power-down sequence, TI recommends that at least one of the VIN UVLO falling threshold or the EN falling threshold is satisfied before the external VCC bias supply turns off. If the external VCC bias supply turns off first, the internal LDO of the device prevents the VCC voltage from dropping below 3.0V and be loaded by other circuits powered by the external VCC bias supply.

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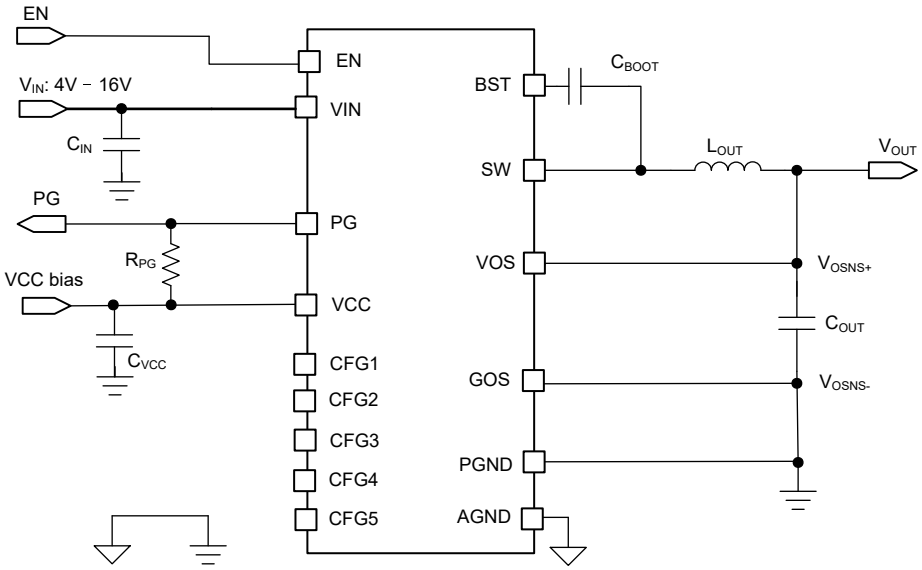

図 7-2. Split-Rail Configuration With External VCC Bias

7.3.3 Multifunction Configuration (CFG1-5) Pins

Through the multifunction configuration pins (CFG 1-5), the device can be configure for a variety of different operating modes. The CFG1-2 pins are used to set the device switching frequency, overcurrent threshold, soft-start time, and either hiccup or latch-up fault recovery operation, while the CFG3-5 pins provide select ability for either internal or external feedback, as well as FCCM or PFM operation.

注

The selection of either internal or external feedback operation through the CFG3-5 pins changes the functions of the CFG1-2 pins. Please see セクション 7.3.3.1 and セクション 7.3.3.2 for more information.

The CFGx states are set and latched during the internal power-on delay period. Changing the CFGx pins after the power-on delay does not change the status of the device.

7.3.3.1 Multifunction Configuration (CFG1-2) Pins (Internal Feedback)

When the device is configured for internal feedback operation with the CFG 3-5 pins (See 表 7-3), the switching frequency and current limit are programmed by tying the CFG1-2 pins either high (VCC), low (GND) or left floating based on the table below:

注

When the device is configured for internal feedback operation, the soft start time is set to 2ms, and the fault recovery is configured for hiccup.

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表 7-1. CFG 1-2 Pin Selection (Internal Feedback Configuration)

CFG1	VALLEY OCP (A)	CFG2	SWITCHING FREQUENCY (f_{SW}) (kHz)(1)
VCC	21	VCC	600
GND	18	GND	800
Float	15	Float	1200

(1) Switching frequency is based on 3.3V output voltage. Frequency varies with output voltage.

7.3.3.2 Multifunction Configuration (CFG1-2) Pins (External Feedback)

When the device is configured for external feedback operation with the CFG 3-5 pins (See 表 7-3), the switching frequency, fault recovery mode, overcurrent threshold, and soft-start time are programmed by connecting resistors between the CFG1-2 pins and AGND.

The switching frequency, fault recovery mode, and soft-start time are programmed by connecting a resistor between the CFG1 pin and AGND based on 表 7-2 below:

表 7-2. CFG1 Pin Selection Table (External Feedback Configuration)

CFG1 PIN RESISTANCE TO AGND (kΩ)	SWITCHING FREQUENCY (f_{SW}) (kHz)(1)	FAULT RECOVERY MODE	SOFT-START TIME (ms)
0 (GND)	600	Hiccup	1
4.99	800	Hiccup	1
7.50	1000	Hiccup	1
10.5	1200	Hiccup	1
13.3	600	Latch Off	1
16.9	800	Latch Off	1
21.0	1000	Latch Off	1
24.9	1200	Latch Off	1
30.1	600	Hiccup	2
35.7	800	Hiccup	2
42.2	1000	Hiccup	2
48.7	1200	Hiccup	2
56.2	600	Latch Off	2
64.9	800	Latch Off	2
75.0	1000	Latch Off	2
86.6	1200	Latch Off	2
102	600	Hiccup	3
118	800	Hiccup	3
137	1000	Hiccup	3
158	1200	Hiccup	3
182	600	Latch Off	3
210	800	Latch Off	3
243	1000	Latch Off	3
≥280 (FLOAT)	1200	Latch Off	3

(1) Switching frequency is based on 3.3V output voltage. Frequency varies with output voltage.

The valley overcurrent protection is programmed with resistor (R_{ILIM}) between CFG2 and AGND using based on 式 2

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$$R_{ILIM} = \frac{K_{OCL}}{I_{OCLIM} - \frac{1}{2} \times \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}}} \quad (2)$$

where

- I_{OCLIM} is overcurrent limit threshold for load current in A
- R_{ILIM} is ILIM resistor value in Ω
- K_{OCL} is a constant of 84 × 10^3 for the calculation
- V_{IN} is input voltage value in V
- V_O is output voltage value in V
- L is output inductor value in µH
- f_{SW} is switching frequency in MHz

$$I_{OCLIM} = \frac{K_{OCL}}{R_{ILIM}} + \frac{1}{2} \times \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}} \quad (3)$$

注

TI recommends a ±1% tolerance resistor because a worse tolerance resistor provides less accurate OCL threshold.

To protect the device from an unexpected connection to the ILIM pin, an internal fixed OCL clamp is implemented. This internal OCL clamp limits the maximum valley current on the low-side MOSFET to 21A when the ILIM pin has too small of a resistance to AGND, or is accidentally shorted to ground.

7.3.3.3 Multifunction Configuration (CFG3-5) Pins

The CFG3-5 pins select the device output voltage configuration as well as FCCM or PFM operation based on 表 7-3 below:

表 7-3. CFG 3-5 Pin Selection Table

CFG3	CFG4	CFG5	V_{FB} Config	V_{OUT}(V)	F_{SW} Mode
VCC	VCC	VCC	internal	5.0	FCCM
VCC	GND	VCC	internal	3.3	FCCM
VCC	Float	VCC	internal	2.5	FCCM
VCC	VCC	GND	internal	1.8	FCCM
VCC	GND	GND	internal	1.5	FCCM
VCC	Float	GND	internal	1.2	FCCM
VCC	VCC	Float	internal	1.1	FCCM
VCC	GND	Float	internal	1.05	FCCM
VCC	Float	Float	internal	1.0	FCCM
GND	VCC	VCC	internal	0.95	FCCM
GND	GND	VCC	internal	0.9	FCCM
GND	Float	VCC	internal	0.85	FCCM
GND	VCC	GND	internal	0.8	FCCM
GND	GND	GND	external	0.5	FCCM
GND	Float	GND	internal	5.0	PFM
GND	VCC	Float	internal	3.3	PFM
GND	GND	Float	internal	2.5	PFM
GND	Float	Float	internal	1.8	PFM
Float	VCC	VCC	internal	1.5	PFM
Float	GND	VCC	internal	1.2	PFM

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表 7-3. CFG 3-5 Pin Selection Table (続き)

CFG3	CFG4	CFG5	V_{FB} Config	V_{OUT}(V)	F_{SW} Mode
Float	Float	VCC	internal	1.1	PFM
Float	VCC	GND	internal	1.0	PFM
Float	GND	GND	internal	0.95	PFM
Float	Float	GND	internal	0.9	PFM
Float	VCC	Float	internal	0.85	PFM
Float	GND	Float	internal	0.8	PFM
Float	Float	Float	external	0.5	PFM

7.3.4 Enable

When the EN pin voltage rises above the enable threshold voltage ($V_{EN(R)}$) and VIN rises above the VIN UVLO rising threshold, the device enters the internal power-up sequence.

The EN pin has an internal filter to avoid unexpected ON or OFF due to small glitches. The time constant of this RC filter is 2µs. For example, when applying 3.3V voltage source on the EN pin that jumps from 0V to 3.3V with an ideal rising edge, the internal EN signal will reach 2.1V after 2µs, which is 63.2% of applied 3.3V voltage level.

An internal pulldown resistor is implemented between the EN pin and AGND pin. With this pulldown resistor, floating the EN pin before start-up keeps the device in the disabled state. A resistor divider to the EN pin can be used to increase the input voltage the device begins the start-up sequence. The internal pulldown resistor must be accounted for when using an external resistor divider. To reduce impact to the EN rising and falling threshold, this internal pulldown resistor is 1MΩ. During nominal operation when the power stage switches, this large internal pulldown resistor can not have enough noise immunity to hold EN pin low for the device to enter the disabled state.

If an external resistor divider is connected to the EN pin, an additional 5µA current source is activated when the EN voltage exceeds the rising threshold to provide a programmable hysteresis based on the enable falling threshold voltage ($V_{EN(F)}$) and external resistors.

The recommended operating condition for the EN pin is a maximum of 5.5V. *Do not* connect the EN pin to the VIN pin directly if VIN can exceed 5.5V.

7.3.5 Soft Start

The device implements an internally fixed 2ms soft-start time when configured for internal feedback operation and a selectable (1ms, 2ms, or 3ms) soft-start time when configured for external feedback operation.

If hiccup mode is enabled, the SS time also sets the hiccup wait-time before a restart attempt. After a fault triggers the hiccup response an internal timer sets the hiccup wait time to 7 × t_{SS}.

7.3.6 Power Good

The device has a power-good (PG or PGOOD) output that goes high to indicate when the converter output is in regulation. The power-good output is an open-drain output and must be pulled up to the VCC pin or an external voltage source (< 5.5V) through a pullup resistor (typically 30.1kΩ) to go high. The recommended power-good pullup resistor value is 1kΩ to 100kΩ.

After the soft-start ramp finishes, the power-good signal becomes high after a 1ms internal delay. An internal soft-start done signal goes high when the SS pin voltage reaches $V_{SS(DONE)}$ to indicate the soft-start ramp has finished. If the FB voltage drops to 80% of the V_{REF} voltage or exceeds 116% of the V_{REF} voltage, the power-good signal latches low after a 3µs internal delay. The power-good signal can only be pulled high again after re-toggling EN or a reset of VIN.

If an OV event causes the FB voltage to exceed the OV threshold during soft start, but the FB voltage drops below the OV threshold before soft-start is completed, the power-good signal does not latch low until FB

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exceeds the OV threshold or drops below UV threshold. The OV or UV event must occur after the soft-start ramp finishes for the power-good signal to latch low. FB exceeding the OV threshold during soft start does, however, trigger the OV fault, and the devices response to OV (described in セクション 7.3.7) typically pulls the output voltage below the UV threshold.

If the input supply fails to power up the device (for example, VIN and VCC both stay at zero volts) and this pin is pulled up through an external resistor, the power-good pin clamps low to the low-level specified in the POWER GOOD section in the *Electrical Characteristics.*

7.3.7 Overvoltage and Undervoltage Protection

The device monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage events. The OVP function enables when the output is enabled. The UVP function enables after the soft-start period is complete.

After soft-start is complete, if the FB voltage becomes lower than 80% of the V_{REF} voltage, the UVP comparator trips and an internal UVP delay counter begins counting. After the 70µs UVP delay time, depending on the selected fault recovery mode, the device either hiccups and re-starts after a sleep time of 7 × the soft-start period or latches off both high-side and low-side MOSFETs. The latch-off fault can be cleared with a reset of VIN or by toggling the EN pin.

When the output is enabled, the FB voltage must rise above the 92.5% PG low-to-high threshold to clear the UVP comparator. If the FB voltage does not exceed the 92.5% threshold by the end of the soft-start period, the device responds to the undervoltage event.

During the UVP delay time, if the FB voltage becomes higher than the 92.5% PG low-to-high threshold, the undervoltage event is cleared and the timer is reset to zero. When the output voltage falls below the 80% UVP threshold again, the 70-µs timer re-starts.

When the FB voltage becomes higher than 116% of the V_{REF} voltage, the OVP comparator trips and the circuit latches the fault condition and drives the PG pin low. The high-side MOSFET turns off and the low-side MOSFET turns on until reaching a negative current limit I_{NOCL}. Upon reaching the negative current limit, the low-side MOSFET is turned off, and the high-side MOSFET is turned on again, for a proper on-time (determined by $V_O/V_{IN}/f_{SW}$). The device operates in this mode until the output voltage is pulled down under the UVP threshold. The device then responds to the undervoltage event as described above.

If there is an overvoltage condition prior to the output being enabled (such as a high prebiased output), the device responds to the overvoltage event as described above at the beginning of the soft-start period. The device waits until the completion of the soft-start period for UVP to be enabled, and depending on the selected fault recovery mode, the device either hiccups and re-starts after a sleep time of 7 × the soft-start period or latches off .

7.3.8 Remote Sense

The device integrates a remote sense amplifier across the VOS/FB and GOS pins. The remote sense function compensates for voltage drop on the PCB traces helping to maintain V_{OUT} accuracy under steady state operation and load transient events.

The FB voltage divider resistors (if used) must be kept near the device to minimize the trace length connected to the FB pin. The connections from the FB voltage divider resistors and the GOS pin to the remote location must be a pair of PCB traces with Kelvin sensing across a bypass capacitor of 0.1µF or higher. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below.

Single-ended V_{OUT} sensing is often used for local sensing. For this configuration, connect the higher FB resistor, R_{FB_HS}, to a high-frequency local bypass capacitor of 0.1µF or higher, and short GOS to AGND.

The recommended GOS operating range (relative to the AGND pin) is –100mV to +100mV.

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7.3.9 Low-side MOSFET Zero-Crossing

The device uses a zero-crossing (ZC) circuit to perform the zero inductor current detection during skip-mode operation. The ZC threshold is set to a small negative value before the low-side MOSFET is turned off, entering discontinuous conduction mode (DCM) operation. After entering DCM, the ZC threshold hysteresis increases the threshold to a small positive value after entering DCM. As a result, the device delivers better light-load efficiency.

When the load current increases enough such that the device exits DCM, the ZC circuit must detect 16 consecutive cycles of negative inductor current below the ZC threshold before returning to DCM. Only one cycle without ZC detection is required to exit DCM.

When the output is enabled, the ZC circuit is also enabled during the first 32 switching cycles while the device is in soft start. If the MSEL resistor value is for FCCM, ZC is disabled and the device transitions to FCCM when soft start is complete. See *Adjustable Soft Start* for a description on soft-start completion. If there are not at least 32 switching cycles before soft-start is done, such as during start-up with a high output prebias, the ZC is not disabled until the first high-side MOSFET on-time after soft-start done is complete.

7.3.10 Current Sense and Positive Overcurrent Protection

For a buck converter, during the on-time of the high-side MOSFET, the switch current increases at a linear rate determined by the input voltage, output voltage, on-time, and output inductor value. During the on-time of the low-side MOSFET, the current decreases linearly. The average value of the switch current equals the load current.

The output overcurrent limit (OCL) in the device is implemented using a cycle-by-cycle valley current detect control circuit. The inductor current is monitored during the on-time of the low-side MOSFET by measuring the low-side MOSFET drain-to-source current. If the measured drain-to-source current of the low-side MOSFET is above the current limit threshold, the low-side MOSFET stays ON until the current level becomes lower than the current limit threshold. This type of behavior reduces the average output current sourced by the device.

During an overcurrent condition, the current to the load exceeds the current to the output capacitors. Thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the undervoltage-protection threshold (80%), the UVP comparator detects the fall and shuts down the device after a wait time of 70 µs. Depending on the fault recovery configuration, the device either hiccups or latches off, as described in *Overvoltage and Undervoltage Protection.*

注

If an OCL condition happens during start-up, the device still has cycle-by-cycle current limit based on low-side valley current, but the UVP comparator does not shut down the device until after soft start has completed.

Please see セクション 7.3.3 for more information on setting the currently limit protection threshold.

7.3.11 Low-side MOSFET Negative Current Limit

The device has a fixed, cycle-by-cycle negative overcurrent limit ($I_{LS(NOC)}$). Similar with the positive overcurrent limit, the inductor current is monitored during the on-time of the low-side MOSFET. To prevent too large negative current flowing through the low-side MOSFET, when the device detects a -10-A current (typical threshold) through the low-side MOSFET, the device turns off the low-side MOSFET and then turns on the high-side MOSFET for the on-time set by the one-shot timer (determined by $V_{IN}/V_{OUT}/f_{SW}$). After the high-side MOSFET on-time expires, the low-side MOSFET turns on again.

The device must not trigger the -10-A negative current limit threshold during nominal operation, unless a small inductor value that is too small is chosen or the inductor becomes saturated. This negative current limit is used to discharge output capacitors after an output OVP event. See *Overvoltage and Undervoltage* for details.

7.3.12 Output Voltage Discharge

When the device is disabled through EN, the device enables the output voltage discharge mode. This mode forces both high-side and low-side MOSFETs to latch off, but turns on the internal discharge MOSFET, which is

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connected from SW to PGND, to discharge the output voltage. After the FB voltage drops below 50mV, the discharge MOSFET and the internal VCC LDO is turned off.

When the EN pin goes low to disable the converter and while the VCC voltage is sufficient to turn on the discharge switch, the output voltage discharge mode is activated.

7.3.13 UVLO Protection

The device monitors the voltage on both the VIN and the VCC pins. If the VCC pin voltage is lower than the VCC_{UVLO} falling threshold voltage, the device shuts off. If the VCC voltage increases beyond the VCC_{UVLO} rising threshold voltage, the device turns back on. VCC UVLO is a non-latch protection.

When the VIN pin voltage is lower than the VIN_{UVLO} falling threshold voltage but the VCC pin voltage is still higher than VCC_{UVLO} rising threshold voltage, the device stops switching and discharges the SS pin. After the VIN voltage increases beyond the VIN_{UVLO} rising threshold voltage, the device re-initiates the soft start and switches again. VIN UVLO is a non-latch protection.

7.3.14 Thermal Shutdown

The device monitors internal junction temperature. If the temperature exceeds the threshold value (typically 165°C), the device stops switching and discharges the SS pin. When the temperature falls approximately 15°C below the threshold value, the device turns back on with a re-initiated soft start. Thermal shutdown is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Auto-Skip (PFM) Eco-mode Light Load Operation

If Skip (PFM)-mode is selected through the CFG3-5 pins, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. See the *Multifunction Configuration (CFG3-5) Pins* section on how to select the PFM mode.

As the output current decreases from heavy load condition, the inductor current also decreases until the valley of the inductor ripple current touches the zero-crossing threshold (*Low-side MOSFET Zero-Crossing*). The zero-crossing threshold sets the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero-crossing threshold is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to light-load operation $I_{OUT(LL)}$ (for example: the boundary between continuous- and discontinuous-conduction mode) is calculated as shown in Equation 5.

For low output ripple, TI recommends using only ceramic output capacitors for designs that operate in skip-mode.

$$I_{OUT(LL)} = \frac{1}{2} \times \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}} \quad (4)$$

7.4.2 Forced Continuous-Conduction Mode

If FCCM mode is selected through the CFG3-5 pins, the controller operates in continuous-conduction mode (CCM) during light-load conditions. See the *Multifunction Configuration (CFG3-5) Pins* section on how to select the FCCM mode.

During FCCM, the switching frequency is maintained to an almost constant level over the entire load range, which is designed for applications requiring tight control of the switching frequency and output ripple at the cost of reduced light-load efficiency. Use Equation 5 to calculate the typical light-load operation boundary. Below this calculated load current, the device operates in FCCM.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS548B23 device is a high-efficiency, single-channel, small-sized, synchronous buck converter. The device is designed for low output voltage point-of-load applications with 20A or lower output current in server, storage, and similar computing applications. The TPS548B23 features proprietary D-CAP4 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an excellent fashion. The output voltage ranges from 0.5V to 5.5V. The conversion input voltage ranges from 4V to 16V, and the VCC input voltage ranges from 3.0 to 5.3V. The D-CAP4 mode uses emulated current information to control the modulation. An advantage of this control scheme is that this control scheme does not require an external phase-compensation network, which makes the device easy-to-use and also allows for a low external component count. Another advantage of this control scheme is that the control scheme supports stable operation with all low ESR output capacitors (such as ceramic capacitor and low ESR polymer capacitor). Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during a load-step transient.

8.2 Typical Application

The schematic shows a typical application for the TPS548B23. This example describes the design procedure of converting an input voltage range of 8V to 16V down to 3.3V with a maximum output current of 20A.

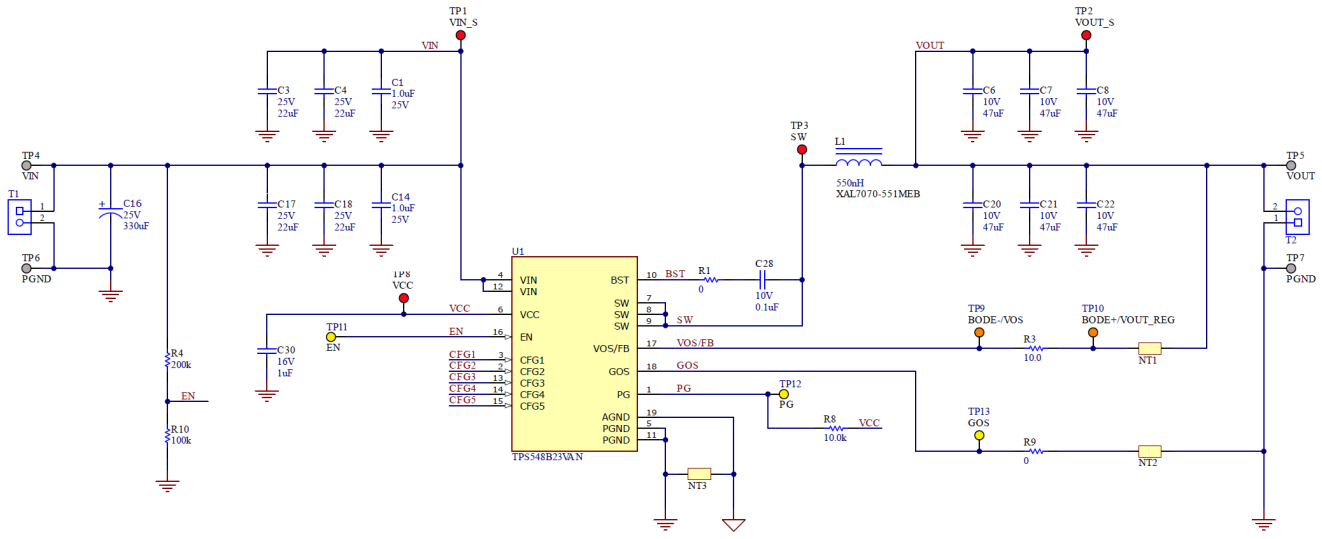

図 8-1. Application Circuit Diagram

ADVANCE INFORMATION

8.2.1 Design Requirements

This design uses the parameters listed in the following table.

表 8-1. Design Example Specifications

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			8	12	16	V
Input current	V_{IN} = 8V, I_{OUT} = 20A			9		A
Output voltage setpoint				3.3		V
Output current range	V_{IN} = 8V to 16V		0		20	A
Load transient response	I_{OUT} = 5A to 15A	Voltage change		–99		mV
	I_{OUT} = 15A to 5A	Voltage change		99		mV
Output ripple voltage	I_{OUT} = 20A			16		mVPP
Soft-start time	From start of switching to V_{FB} = 0.5V, t_{SS} = 2ms setting		1.4	2	2.6	ms
Current limit	OCP = 21A setting by CFG pin selection		19	21	23	A
Switching frequency (f_{SW})	f_{SW} = 800kHz setting by CFG1-5 pin selection			800		kHz

8.2.2 Detailed Design Procedure

The external component selection is a simple process using D-CAP4 mode. Select the external components using the following steps.

8.2.2.1 Output Voltage Setting Point

The CFG3-5 pins select the device output voltage configuration as well as FCCM or PFM operation based on 表 7-3. For this design, use the internal FB configuration option.

If an output voltage other than those is available in 表 7-3, the external feedback configuration allows the output voltage to be programmed by a voltage-divider resistors, R1 and R2. Connect R1 between the FB pin and the output, and connect R2 between the FB pin and GOS. The recommended R2 value is 10kΩ, but the value can also be set to another value between the range of 1kΩ to 20kΩ. Determine R1 by using 式 5.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.5V} - 1 \right) \quad (5)$$

8.2.2.2 Choose the Switching Frequency

For this design we use the internal feedback mode and the switching frequency is configured by tying the CFG2 pin to VCC (600kHz), GND (800kHz), or by leaving it floating (1.2MHz). Refer to 表 7-1.

If the external feedback configuration is being used, the CFG1 pin is used to select between four switching frequencies (600kHz, 800kHz, 1MHz, or 1.2MHz) Refer to 表 7-2 for more information using the CFG1 pin configuration in external feedback mode.

Switching frequency selection is a tradeoff between higher efficiency and smaller system design size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses which impact efficiency and thermal performance. For this design, connect CFG2 pin to AGND to set the switching frequency to 800kHz

When selecting the switching frequency of a buck converter, the minimum on-time and minimum off-time must be considered. 式 6 calculates the maximum f_{SW} before being limited by the minimum on-time. When hitting the minimum on-time limits of a converter with D-CAP4 control, the effective switching frequency changes to keep the output voltage regulated. This calculation ignores resistive drops in the converter to give a worst case estimation.

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$$f_{SW}(max) = \frac{V_{OUT}}{V_{IN}(max)} \times \frac{1}{t_{ON\_MIN}(max)} = \frac{3.3\ V}{16\ V} \times \frac{1}{25\ ns} = 8250\ kHz \quad (6)$$

式 6 calculates the maximum f_{SW} before being limited by the minimum off-time. When hitting the minimum off-time limits of a converter with D-CAP4 control, the operating duty cycle maxes out and the output voltage begins to drop with the input voltage. This equation requires the DC resistance of the inductor, R_{DCR}, selected in the following step so this preliminary calculation assumes a resistance of 1.4mΩ. If operating near the maximum f_{SW} limited by the minimum off-time, the variation in resistance across temperature must be considered when using 式 8. The selected f_{SW} of 800kHz is below the two calculated maximum values.

$$f_{SW}(max) = \frac{V_{IN}(min) - V_{OUT} - I_{OUT}(max) \times \left(R_{DCR} + R_{DS(ON)\_HS}\right)}{t_{OFF\_MIN}(max) \times \left(V_{IN}(min) - I_{OUT}(max) \times \left(R_{DS(ON)\_HS} - R_{DS(ON)\_LS}\right)\right)} \quad (7)$$

$$f_{SW}(max) = \frac{8\ V - 3.3\ V - 20\ A \times (1.4\ m\Omega + 9.5\ m\Omega)}{150\ ns \times (8\ V - 20\ A \times (9.5\ m\Omega - 3.3\ m\Omega))} = 3.8\ MHz \quad (8)$$

8.2.2.3 Choose the Inductor

To calculate the value of the output inductor (L_{OUT}), use 式 9. The output capacitor filters the inductor-ripple current ($I_{IND(ripple)}$). Therefore, selecting a high inductor-ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal to or greater than the inductor-ripple current. On the other hand, larger ripple current increases output ripple voltage, but improves signal-to-noise ratio and helps to stabilize operation. Generally speaking, the inductance value must set the ripple current at approximately 15% to 40% of the maximum output current for a balanced performance.

For this design, the inductor-ripple current is set to 30% of 20A output current. With a 800klHz switching frequency, 16V as maximum V_{IN}, and 3.3V as the output voltage, Based on these parmaters, 式 9 calculates an inductance of 0.546µH . A nearest standard value of 0.55µH is chosen.

$$L = \frac{(V_{IN}(max) - V_{OUT}) \times V_{OUT}}{I_{RIPPLE} \times V_{IN}(max) \times f_{SW}} = \frac{(16\ V - 3.3\ V) \times 3.3\ V}{0.3 \times 20A \times 16\ V \times 800\ kHz} = 0.546\ \mu H \quad (9)$$

The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough room above peak inductor current before saturation. The inductor current ripple is estimated using 式 10. For this design, by tying the CFG1 pin to VCC, $I_{OC(valley)}$ is set to 21A, thus peak inductor current under maximum V_{IN} is calculated as 22.98A with 式 11.

$$I_{RIPPLE} = \frac{(V_{IN}(max) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(max) \times f_{SW}} = \frac{(16\ V - 3.3\ V) \times 3.3\ V}{0.55\mu H \times 16\ V \times 800\ kHz} = 5.95\ A \quad (10)$$

$$I_{L(PEAK)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 20\ A + \frac{5.95\ A}{2} = 22.98\ A \quad (11)$$

$$I_{L(RMS)} = \sqrt{{I_{OUT}}^2 + \frac{{I_{RIPPLE}}^2}{12}} = \sqrt{{20\ A}^2 + \frac{{5.95\ A}^2}{12}} = 20.07\ A \quad (12)$$

The selected inductance is a Coilcraft XAL7070-551MEB. This has a saturation current rating of 43 A , RMS current rating of 29-A and a DCR of 1.6 mΩ max. This inductor was selected for its low DCR to get high efficiency.

8.2.2.4 Choose the Output Capacitor

There are three considerations for selecting the value of the output capacitor:

1. Stability
2. Steady state output voltage ripple
3. Regulator transient response to a change load current

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First, calculate the minimum output capacitance based on these three requirements. 式 13 calculates the minimum capacitance to keep the LC double pole below 1/30th the f_{SW} to meet stability requirements. This requirement helps to keep the LC double pole close to the internal zero. 式 14 calculates the minimum capacitance to meet the steady state output voltage ripple requirement of 16mV. These calculations are for CCM operation and does not include the portion of the output voltage ripple caused by the ESR or ESL of the output capacitors.

$$C_{OUT\_STABILITY} > \left(\frac{30}{2\pi \times f_{SW}}\right)^2 \times \frac{1}{L} = \left(\frac{30}{2\pi \times 800kHz}\right)^2 \times \frac{1}{0.55\mu H} = 64.8\mu F \quad (13)$$

$$C_{OUT\_RIPPLE} > \frac{I_{RIPPLE}}{8 \times V_{RIPPLE} \times f_{SW}} = \frac{5.95A}{8 \times 16mV \times 800kHz} = 58.1\mu F \quad (14)$$

式 16 and 式 17 calculate the minimum capacitance to meet the transient response requirement of 99mV with a 10A step. These equations calculate the necessary output capacitance to hold the output voltage steady while the inductor current ramps up or ramps down after a load step.

$$C_{OUT\_UNDERSHOOT} > \frac{L \times {I_{STEP}}^2 \times \left(\frac{V_{OUT}}{V_{IN}(min) \times f_{SW}} + t_{OFF\_MIN}(max)\right)}{2 \times V_{TRANS} \times V_{OUT} \times \left(\frac{V_{IN}(min) - V_{OUT}}{V_{IN}(min) \times f_{SW}} - t_{OFF\_MIN}(max)\right)} \quad (15)$$

$$C_{OUT\_UNDERSHOOT} > \frac{0.55\mu H \times {10A}^2 \times \left(\frac{3.3V}{8V \times 800kHz} + 150ns\right)}{2 \times 99mV \times 3.3V \times \left(\frac{8V - 3.3V}{8V \times 800kHz} - 150ns\right)} = 732\mu F \quad (16)$$

$$C_{OUT\_OVERSHOOT} > \frac{L \times {I_{STEP}}^2}{2 \times V_{TRANS} \times V_{OUT}} = \frac{0.55\mu H \times {10A}^2}{2 \times 99mV \times 3.3V} = 84.2\mu F \quad (17)$$

The output capacitance needed to meet the overshoot requirement is the highest value, so this sets the required minimum output capacitance for this example. Stability requirements can also limit the maximum output capacitance. 式 18 calculates the recommended maximum output capacitance. This calculation keeps the LC double pole above 1/100th the f_{SW}.

$$C_{OUT\_STABILITY} < \left(\frac{50}{\pi \times f_{SW}}\right)^2 \times \frac{1}{L} = \left(\frac{50}{\pi \times 800kHz}\right)^2 \times \frac{1}{0.55\mu H} = 720\mu F \quad (18)$$

Using more output capacitance is possible, but the stability must be checked through a bode plot or transient response measurement. The selected output capacitance is 6 × 47µF, 10V ceramic capacitors. When using ceramic capacitors, the capacitance must be derated due to DC and AC bias effects. The selected capacitors derate to 48% the nominal value giving an effective total capacitance of 135µF. This effective capacitance meets the minimum and maximum requirements.

This application uses all ceramic capacitors so the effects of ESR on the ripple and transient were ignored. If using non ceramic capacitors, as a starting point, the ESR must be below the values calculated in 式 19 to meet the ripple requirement and 式 20 to meet the transient requirement. For more accurate calculations or if using mixed output capacitors, the impedance of the output capacitors must be used to determine if the ripple and transient requirements can be met.

$$R_{ESR\_RIPPLE} < \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{26mV}{5.95A} = 4.4m\Omega \quad (19)$$

$$R_{ESR\_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{99mV}{10A} = 9.9m\Omega \quad (20)$$

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8.2.2.5 Choose the Input Capacitors (C_{IN})

The device requires input bypass capacitors between both pairs of VIN and PGND pins to bypass the power-stage. The bypass capacitors must be placed as close as possible to the pins of the IC as the layout allows. At least 20µF nominal of ceramic capacitance and two high frequency ceramic bypass capacitors are required. A 0.1µF to 1µF capacitor must be placed as close as possible to both VIN pins 4 and 12 on the same side of the board of the device to provide the required high frequency bypass, to reduce the high frequency overshoot and undershoot on across the power-stage on the VIN and SW pins. TI recommends at least 1µF of bypass capacitance as close as possible to each VIN pin to minimize the input voltage ripple. The ceramic capacitors must be a high-quality dielectric of X6S or better for the high capacitance-to-volume ratio and stable characteristics across temperature. In addition to this, more bulk capacitance can be needed on the input depending on the application to minimize variations on the input voltage during transient conditions.

The input capacitance required to meet a specific input ripple target can be calculated with 式 21. A recommended target input voltage ripple is 5% the minimum input voltage, 780 mV in this example. The calculated input capacitance is 5.5µF. This example meets these two requirements with 2 × 10µF ceramic capacitors.

$$C_{IN} > \frac{V_{OUT} \times I_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}(min)}\right)}{f_{SW} \times V_{IN}(min) \times V_{IN\_RIPPLE}} = \frac{3.3V \times 20A \times \left(1 - \frac{3.3V}{8V}\right)}{800\,kHz \times 8V \times 780mV} = 7.8\mu F \quad (21)$$

The capacitor must also have an RMS current rating greater than the maximum input RMS current in the application. The input RMS current the input capacitors must support is calculated by 式 23 and is 12.4A in this example. The ceramic input capacitors have a current rating greater than this value.

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}(min)} \times \left(\frac{(V_{IN}(min) - V_{OUT})}{V_{IN}(min)} \times {I_{OUT}}^2 + \frac{{I_{RIPPLE}}^2}{12}\right)} \quad (22)$$

$$I_{CIN(RMS)} = \sqrt{\frac{3.3V}{8V} \times \left(\frac{(8V - 3.3V)}{8V} \times 20^2 + \frac{5.95^2}{12}\right)} = 16.9A \quad (23)$$

For applications requiring bulk capacitance on the input, such as ones with low input voltage and high current, TI recommends the selection process in *How to select input capacitors for a buck converter*.

8.2.2.6 VCC Bypass Capacitor

At a minimum, a 1.0µF, at least 6.3V rating, X5R ceramic bypass capacitor is needed on VCC pin located as close to the pin as the layout allows. Use the smallest sized capacitor possible, such as an 0402 package, to minimize the loop from the VCC pin to the PGND pin.

8.2.2.7 BOOT Capacitor

At a minimum, a 0.1µF, 10V, X5R ceramic bypass capacitor is needed between the BOOT and SW pins located as close to the pin as the layout allows.

8.2.2.8 PG Pullup Resistor

The PG pin is open-drain, so a pullup resistor is required when using this pin. The recommended value is between 1kΩ and 100kΩ.

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4V and 16V. Both input supplies (VIN and VCC bias) must be well regulated. Proper bypassing of input supplies (VIN and VCC bias) is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendations in *Layout.*

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8.4 Layout

8.4.1 Layout Guidelines

Before beginning a design using the device, consider the following:

- Make VIN, PGND, and SW traces as wide as possible to reduce trace impedance and improve heat dissipation.
- Place the power components (including input and output capacitors, the inductor, and the IC) on the top side of the PCB. To shield and isolate the small signal traces from noisy power lines, insert at least one solid ground inner plane.
- Placement of the VIN decoupling capacitors are important for the power MOSFET robustness. A 1µF/25V/ 0402 ceramic high-frequency bypass capacitor on each VIN pin (pins 4 and 12) is required, connected to the adjacent PGND pins (pins 5 and 11 respectively). Place the remaining ceramic input capacitance next to these high frequency bypass capacitors. The remaining input capacitance can be placed on the other side of the board, but use as many vias as possible to minimize impedance between the capacitors and the pins of the IC.
- Place as many vias as possible below and near the PGND pins . This action minimizes parasitic impedance and also lowers thermal resistance.
- Use vias near both VIN pins and provide a low impedance connection between them through an internal layer. A via can also be placed below each of the VIN pins.
- Place the VCC decoupling capacitor as close as possible to the device, with a short return to PGND (pin 5). Make sure the VCC decoupling loop is small and use traces with a width of 12 mil or wider to route the connection.
- Place the BOOT capacitor as close as possible to the BOOT and SW pins. Use traces with a width of 12 mil or wider to route the connection.
- The PCB trace, which connects the SW pin and high-voltage side of the inductor, is defined as switch node. The switch node must be as short and wide as possible.
- If using external feedback, always place the feedback resistors near the device to minimize the FB trace distance, no matter single-end sensing or remote sensing.
  - For remote sensing, the connections from the FB voltage divider resistors to the remote location must be a differential pair of PCB traces, and must implement Kelvin sensing across a bypass capacitor of 0.1µF or higher. The ground connection of the remote sensing signal must be connected to GOS pin. The V_{OUT} connection of the remote sensing signal must be connected to the feedback resistor divider with the bottom feedback resistor terminated to the GOS pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below.
  - For single-end sensing, connect the top feedback resistor between the FB pin and the output voltage to a high-frequency local output bypass capacitor of 0.1µF or higher, and short GOS to AGND with a short trace.
- Connect the AGND pin (pin 19) to the PGND pins (pins 5 and 11) beneath the device.
- Avoid routing the PG signal and any other noisy signals in the application near noise sensitive signals, such as VOS/FB and GOS to limit coupling.
- See *Layout Example* for the layout recommendation.

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8.4.2 Layout Example

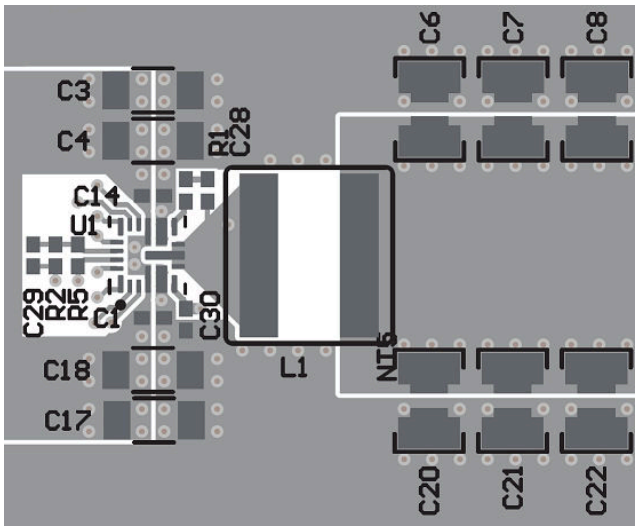

図 8-2. Layout Recommendation

For a more detailed layout example, please reference the *TPS548B23 Step-Down Converter Evaluation Module* EVM user's guide.

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application report
- Texas Instruments, *Non-isolated Point-of-load Solutions for VR13.HC in Rack Server and Datacenter Applications* application note
- Texas Instruments, *TPS548B23 Step-Down Converter Evaluation Module* EVM user's guide

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2024	*	Initial Release

ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

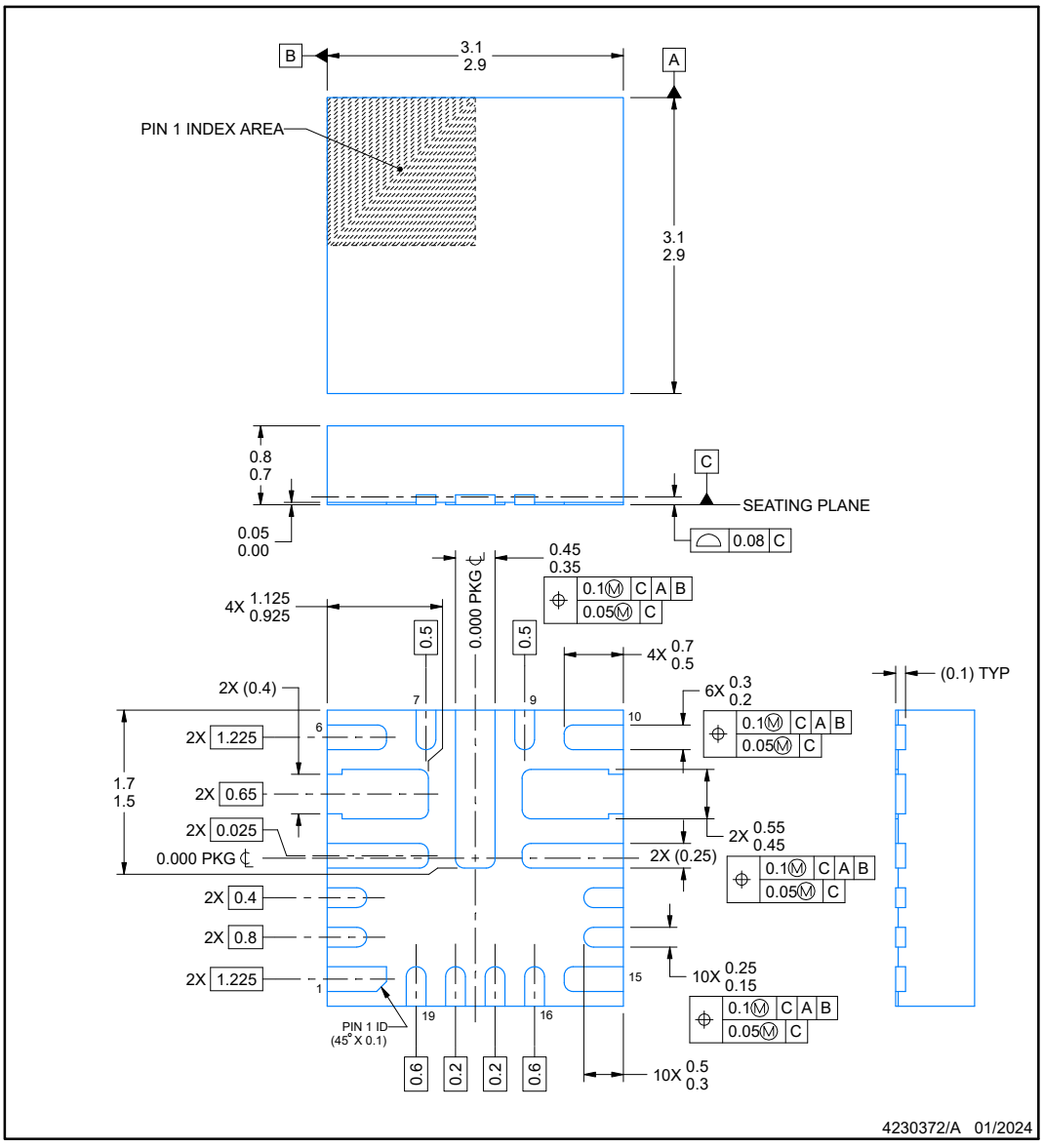
ADVANCE INFORMATION

PACKAGE OUTLINE

VAN0019A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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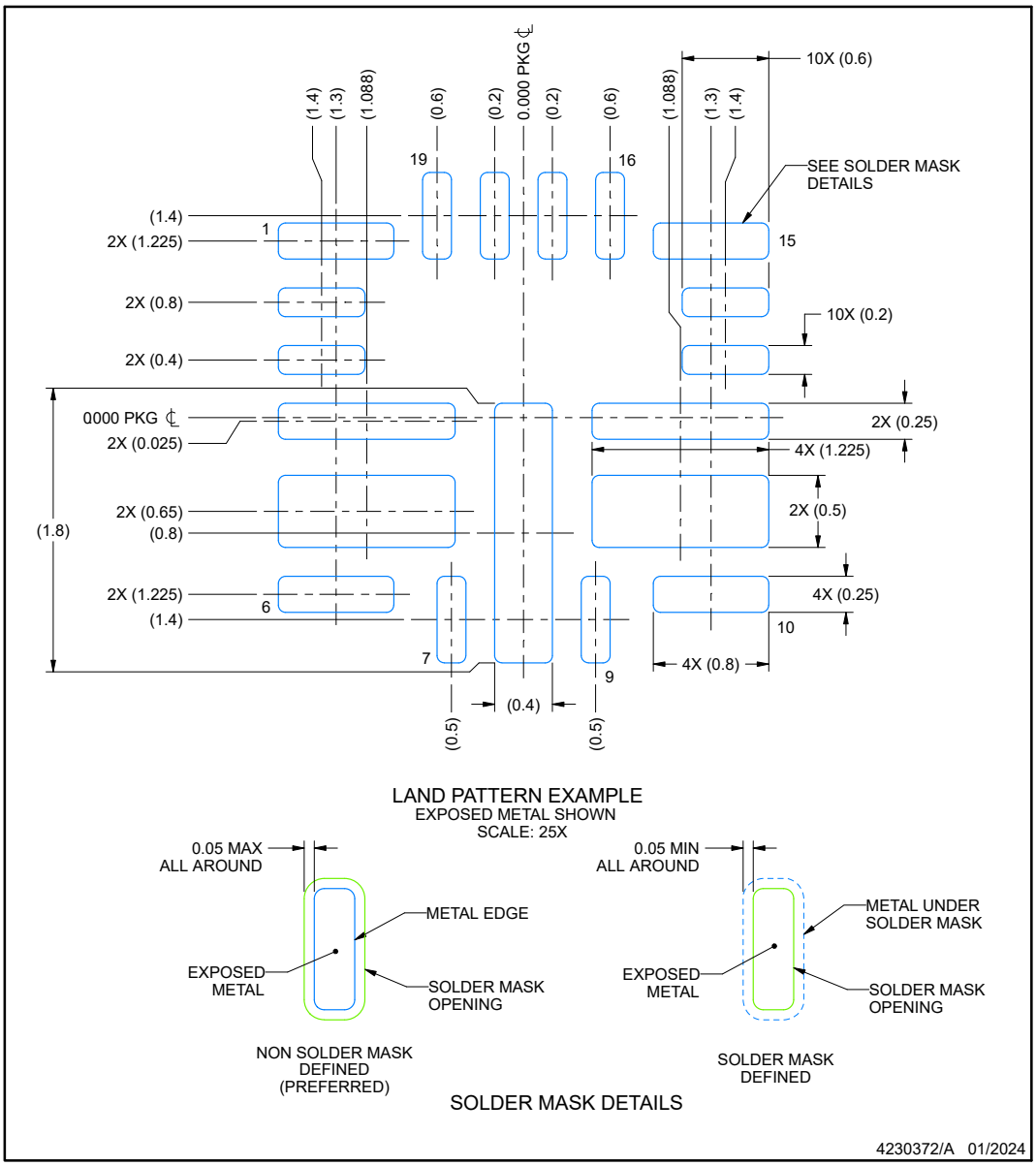
EXAMPLE BOARD LAYOUT

VAN0019A — **WQFN-HR - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

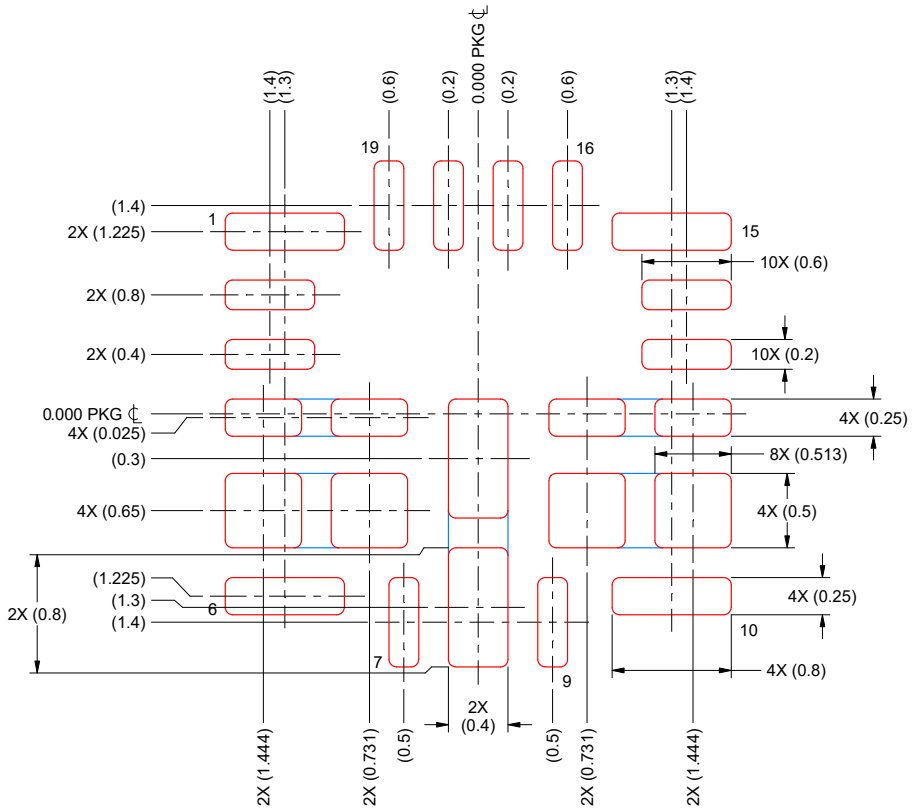
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

VAN0019A **WQFN-HR - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 4, 5, 11 & 12: 84%
PAD 8: 89%

4230372/A 01/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS548B23VANR	Active	Preproduction	WQFN-HR (VAN) | 19	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS548B23VANR.A	Active	Preproduction	WQFN-HR (VAN) | 19	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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