TEXAS INSTRUMENTS
TPS54618C-Q1
JAJSJP2A – SEPTEMBER 2020 – REVISED AUGUST 2021

TPS54618C-Q1 車載用 2.95V～6V、6A、同期整流降圧コンバータ

1 特長

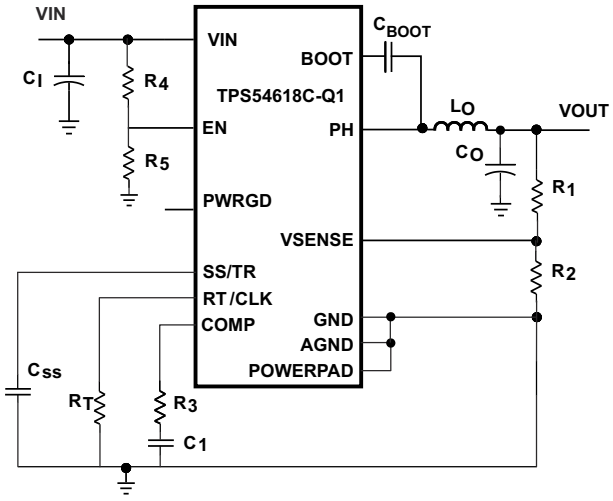
- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40°C～+125°C、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 2 つの 12mΩ (標準値) MOSFET により 6A の負荷で高効率を実現
- 300kHz～2MHz のスイッチング周波数
- -40℃～+150℃の温度範囲全体で 0.8V ±1% の基準電圧
- 外部クロックに同期
- 調整可能なスロー・スタートとシーケンシング
- UV および OV のパワー・グッド出力
- 新製品を入手可能:TPS62810-Q1、6V 降圧コンバータ、2mm × 3mm ウェッタブル・フランク付き QFN パッケージ
- 熱的に強化された 3mm × 3mm の 16 ピン WQFN パッケージ

2 アプリケーション

- 車載用ヘッド・ユニット
- 車載用インストルメント・クラスタ
- 車載用 ADAS カメラ

3 概要

TPS54618C-Q1 デバイスは、2 つの MOSFET を内蔵したフル機能の 6V、6A 同期整流降圧型電流モード・コンバータです。



概略回路図

TPS54618C-Q1 は、MOSFET を内蔵し、電流モード制御の実装により外付け部品数が少なく、スイッチング周波数が最大 2MHz と高いためインダクタのサイズを小さくでき、熱的に強化された小型 (3mm × 3mm) WQFN パッケージにより IC のフットプリントを最小化できるため、小型の設計を実現できます。

TPS54618C-Q1 は、温度範囲全体で ±1% の高精度基準電圧 (VREF) により、各種の負荷について正確なレギュレーションを行います。

内蔵の 12mΩ MOSFET と 515μA (標準値) の消費電流により、効率を最大化できます。
イネーブル・ピンを使用してシャットダウン・モードに移行すると、シャットダウン時の消費電流を 5.5μA に低減できます。

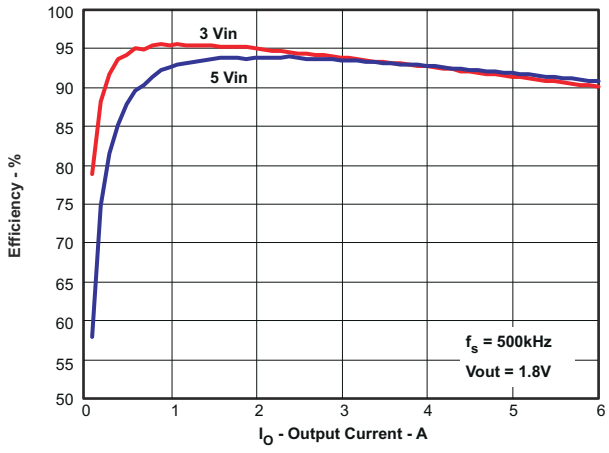
低電圧誤動作防止は内部で 2.6V に設定されていますが、イネーブル・ピンの抵抗回路でスレッショルドをプログラムすることにより、さらに高い電圧に設定できます。出力電圧のスタートアップ・ランプは、スロースタート・ピンにより制御されます。出力が公称電圧の 93%～107% の範囲内にあるとき、オープン・ドレインのパワー・グッド信号が通知されます。

周波数のフォールドバックとサーマル・シャットダウンにより、過電流時にデバイスが保護されます。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
TPS54618C-Q1	WQFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力電流との関係

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
Pin Functions ... 3
6 Specifications ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Timing Requirements ... 7
6.7 Typical Characteristics ... 8
7 Detailed Description ... 12
7.1 Overview ... 12
7.2 Functional Block Diagram ... 13
7.3 Feature Description ... 13
7.4 Device Functional Modes ... 20
8 Application and Implementation ... 24
8.1 Application Information ... 24
8.2 Typical Application ... 24
9 Power Supply Recommendations ... 32
10 Layout ... 33
10.1 Layout Guidelines ... 33
10.2 Layout Example ... 34
10.3 Power Dissipation Estimate ... 34
11 Device and Documentation Support ... 36
11.1 Device Support ... 36
11.2 Receiving Notification of Documentation Updates ... 36
11.3 Support Resources ... 36
11.4 Trademarks ... 36
11.5 静電気放電に関する注意事項 ... 36
11.6 Glossary ... 36
12 Mechanical, Packaging, and Orderable Information ... 36

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2020) to Revision A (August 2021)	Page
• TPS62816-Q1 のプロモーション項目を追加	1
• Changed "Start with 100 kΩ for the R1 resistor and use equation 1..." to "Pick a suitable value for R1 and use equation 1..."	14

5 Pin Configuration and Functions

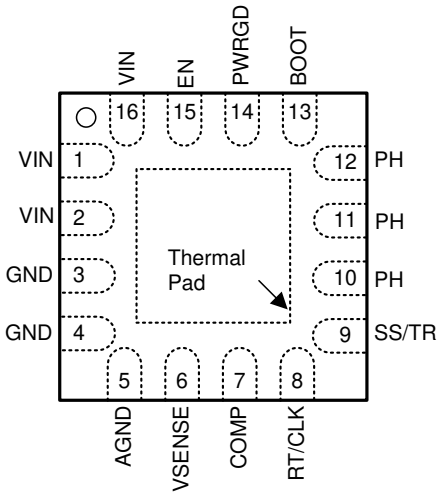


図 5-1. 16-Pin WQFN With Exposed Thermal Pad RTE Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AGND	5	G	Analog ground must be electrically connected to GND close to the device.
BOOT	13	I	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the BOOT UVLO, the output is forced to switch off until the capacitor is refreshed.
COMP	7	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	15	I	Enable pin and internal pullup current source. Pull below 1.2 V to disable. Float to enable. Can be used to set the on/off threshold (adjust UVLO) with two additional resistors.
GND	3	G	Power ground. This pin must be electrically connected directly to the power pad under the device.
	4		
PH	10	O	The source of the internal high-side power MOSFET, and drain of the internal low-side (synchronous) rectifier MOSFET.
	11		
	12		
PWRGD	14	O	An open-drain output, asserts low if output voltage is low due to thermal shutdown, overcurrent, overvoltage and undervoltage, or EN shutdown.
RT/CLK	8	I/O	Resistor timing or external clock input pin
SS/TR	9	I/O	Slow start and tracking. An external capacitor connected to this pin sets the output voltage rise time. This pin can also be used for tracking.
VIN	1	I	Input supply voltage: 2.95 V to 6 V
	2		
	16		
VSENSE	6	I	Inverting node of the transconductance (gm) error amplifier
Thermal Pad	—	G	GND pin must be connected to the exposed power pad for proper operation. This power pad must be connected to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = Input, O = Output, G = Ground

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AGND	5	G	Analog ground must be electrically connected to GND close to the device.

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BOOT	13	I	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the BOOT UVLO, the output is forced to switch off until the capacitor is refreshed.
COMP	7	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	15	I	Enable pin and internal pullup current source. Pull below 1.2 V to disable. Float to enable. Can be used to set the on/off threshold (adjust UVLO) with two additional resistors.
GND	3	G	Power ground. This pin must be electrically connected directly to the power pad under the device.
	4		
PH	10	O	The source of the internal high-side power MOSFET, and drain of the internal low-side (synchronous) rectifier MOSFET.
	11		
	12		
PWRGD	14	O	An open-drain output, asserts low if output voltage is low due to thermal shutdown, overcurrent, overvoltage and undervoltage, or EN shutdown.
RT/CLK	8	I/O	Resistor timing or external clock input pin
SS/TR	9	I/O	Slow start and tracking. An external capacitor connected to this pin sets the output voltage rise time. This pin can also be used for tracking.
VIN	1	I	Input supply voltage: 2.95 V to 6 V
	2		
	16		
VSENSE	6	I	Inverting node of the transconductance (gm) error amplifier
Thermal Pad	—	G	GND pin must be connected to the exposed power pad for proper operation. This power pad must be connected to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = Input, O = Output, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	PWRGD, VIN	–0.3	7	V
	EN, RT/CLK	–0.3	4	
	COMP, SS, VSENSE	–0.3	3	
	BOOT		V_{PH}+ 7	
Output voltage	BOOT-PH		7	V
	PH	–0.6	7	
	PH (10-ns transient)	–2	10	
Source current	EN, RT/CLK		100	µA
Sink current	COMP, SS		100	µA
	PWRGD		10	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under セクション 6.3. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) **HBM ESD classification level XX**	±2000	V
		Charged-device model (CDM), per AEC Q100-011 **CDM ESD classification level XX**	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VIN}	Input voltage	3	6	V
T_A	Operating ambient temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(2) (1)		TPS54618C-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.38	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.09	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.96	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.69	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.91	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.55	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Unless otherwise specified, metrics listed in this table refer to JEDEC high-K board measurements

6.5 Electrical Characteristics

at T_J = –40°C to +125°C, V_{IN} = 2.95 to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		2.95		6	V
Internal undervoltage lockout threshold	VIN UVLO STOP		2.28	2.5	V
	VIN UVLO START		2.45	2.6	
Shutdown supply current	EN = 0 V, 25°C, 2.95 V ≤ V_{IN} ≤ 6 V		5.5	15	µA
Quiescent current, I_Q	V_{SENSE} = 0.9 V, V_{IN} = 5 V, 25°C, RT = 400 kΩ		515	650	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.25		V
	Falling		1.18		
Input current	Enable threshold + 50 mV		–3.5		µA
	Enable threshold – 50 mV		–1.9		
VOLTAGE REFERENCE (VSENSE PIN)					
Voltage reference	2.95 V ≤ V_{IN} ≤ 6 V, –40°C <T_J < 150°C	0.791	0.799	0.807	V
MOSFET					
High-side switch resistance	BOOT-PH = 5 V		12	25	mΩ
	BOOT-PH = 2.95 V		16	33	
Low-side switch resistance	VIN = 5 V		13	25	mΩ
	VIN = 2.95 V		17	33	
ERROR AMPLIFIER					
Input current			2		nA
Error amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		245		µmhos
Error amplifier transconductance (gm) during slow start	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V, V_{SENSE} = 0.4 V		79		µmhos
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±20		µA
COMP to I_{switch} gm			25		A/V
CURRENT LIMIT					
Current limit threshold	V_{IN} = 6 V, 25°C < T_J < 150°C	7.46	10.6	15.3	A
	V_{IN} = 2.95 V, 25°C < T_J < 150°C	7.68	10.2	13.5	
THERMAL SHUTDOWN					
Thermal shutdown			168		°C
Hysteresis			20		°C
BOOT (BOOT PIN)					
BOOT charge resistance	V_{IN} = 5 V		16		Ω
BOOT-PH UVLO	V_{IN}= 2.95 V		2.1		V
SLOW-START AND TRACKING (SS/TR PIN)					
Charge current	$V_{(SS/TR)}$ = 0.4 V		2		µA
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.4 V		54		mV
SS/TR to reference crossover	98% normal		1.1		V
SS/TR discharge voltage (overload)	V_{SENSE} = 0 V		61		mV
SS/TR discharge current (overload)	V_{SENSE} = 0 V, $V_{(SS/TR)}$ = 0.4 V		350		µA
SS discharge current (UVLO, EN, Thermal fault)	V_{IN} = 5 V, V(SS) = 0.5 V		1.9		mA

at T_J = –40°C to +125°C, V_{IN} = 2.95 to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		91%		Vre
	VSENSE rising (Good)		93%		
	VSENSE rising (Fault)		109%		
	VSENSE falling (Good)		107%		
Hysteresis	VSENSE falling		2%		Vref
Output high leakage	VSENSE = VREF, $V_{(PWRGD)}$ = 5.5 V		7		nA
ON-resistance			56	100	Ω
Output low	$I_{(PWRGD)}$ = 3 mA		0.2	0.3	V
Minimum V_{IN} for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		0.65	1.5	V

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Switching frequency range using RT mode		200		2000	kHz
Switching frequency	R_t = 400 kΩ	400	500	600	kHz
Switching frequency range using CLK mode		300		2000	kHz
Minimum CLK pulse width		75			ns
RT/CLK voltage	$R_{(RT/CLK)}$ = 400 kΩ		0.5		V
RT/CLK high threshold			1.6	2.2	V
RT/CLK low threshold		0.4	0.6		V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		90		ns
PLL lock in time	Measure at 500 kHz		42		µs
PH (PH PIN)					
Minimum ON-time	Measured at 50% points on PH, I_{OUT} = 3 A		75		ns
	Measured at 50% points on PH, VIN = 6 V, I_{OUT} = 0 A		120		
Minimum OFF-time	Prior to skipping off pulses, BOOT-PH = 2.95 V, I_{OUT} = 3 A		60		ns
Rise time	V_{IN} = 6 V, 6 A		2.25		V/ns
Fall time	V_{IN} = 6 V, 6 A		2		

6.7 Typical Characteristics

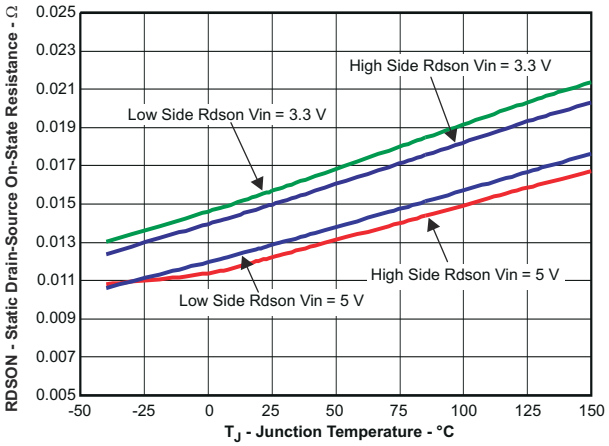


図 6-1. High-Side and Low-Side ON-Resistance vs Junction Temperature

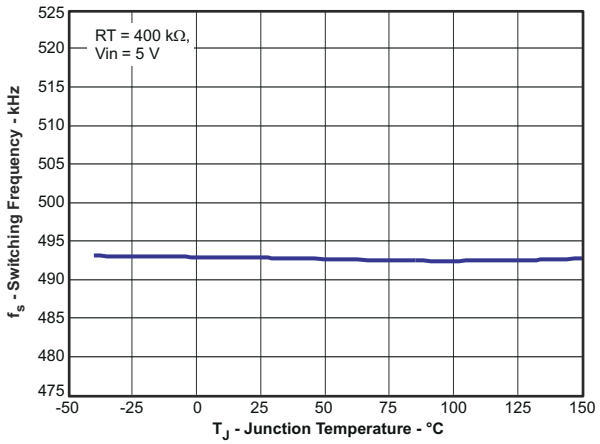


図 6-2. Switching Frequency vs Junction Temperature

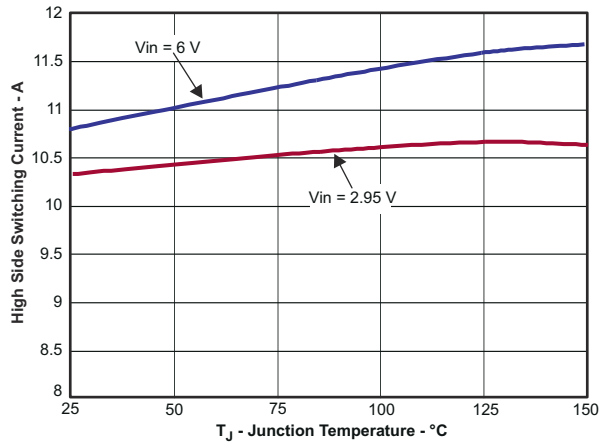


図 6-3. High-Side Current Limit vs Junction Temperature

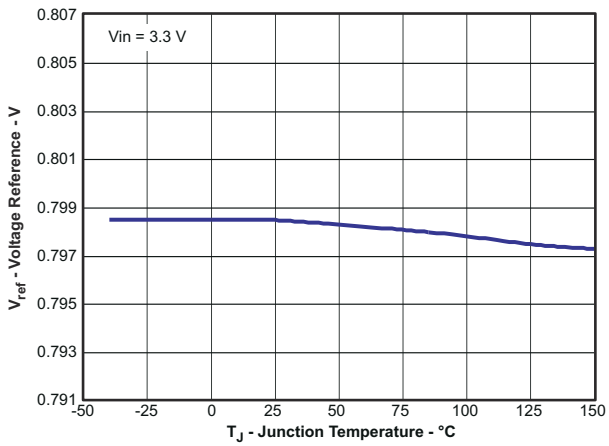


図 6-4. Voltage Reference vs Junction Temperature

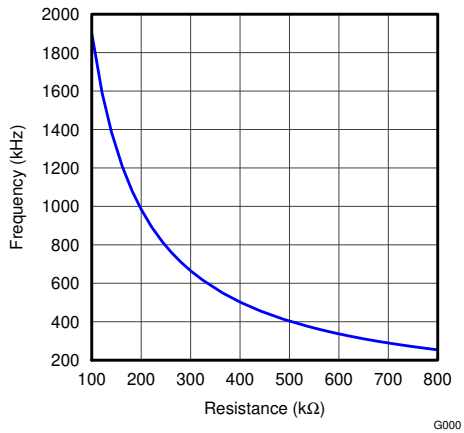


図 6-5. Switching Frequency vs RT Resistance Low Frequency Range

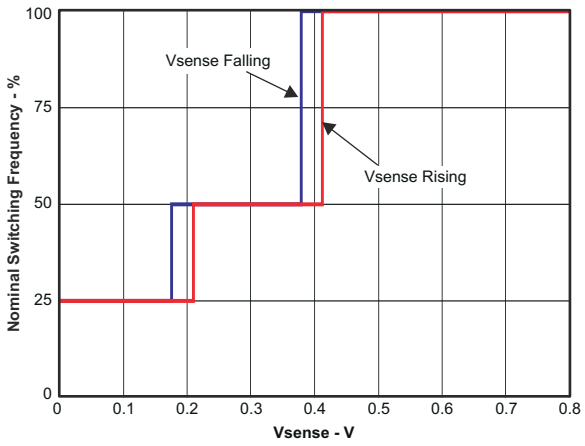


図 6-6. Switching Frequency vs Vsense

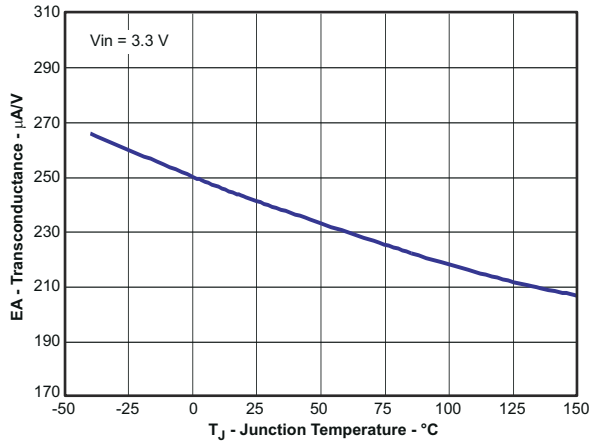


図 6-7. Transconductance vs Junction Temperature

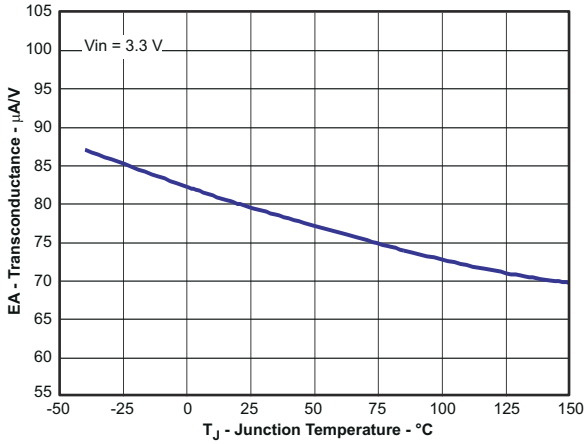


図 6-8. Transconductance (Soft-Start) vs Junction Temperature

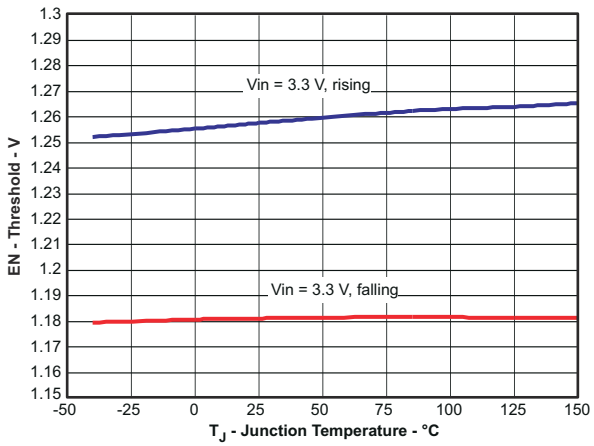


図 6-9. Enable Pin Voltage vs Junction Temperature

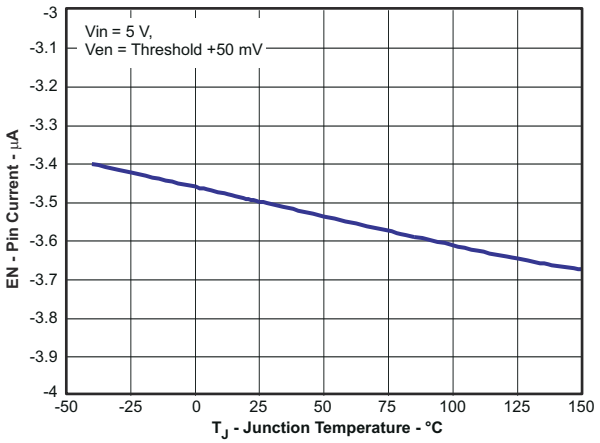


図 6-10. EN Pin Current vs Junction Temperature

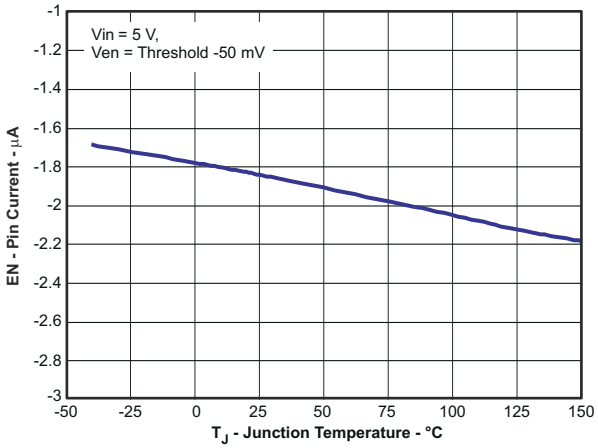


図 6-11. EN Pin Current vs Junction Temperature

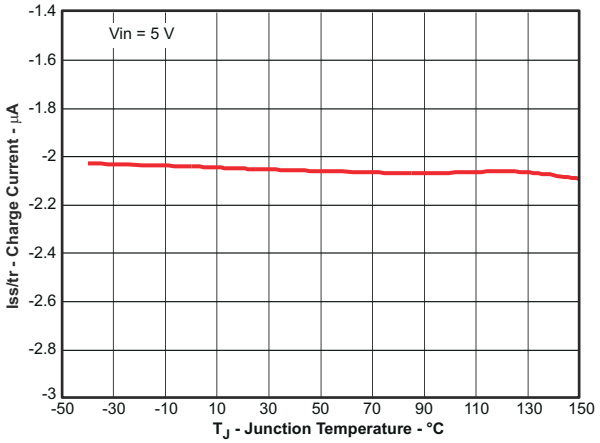


図 6-12. Charge Current vs Junction Temperature

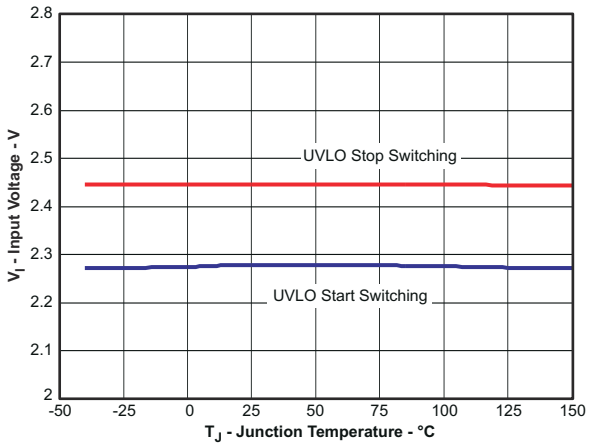


図 6-13. Input Voltage vs Junction Temperature

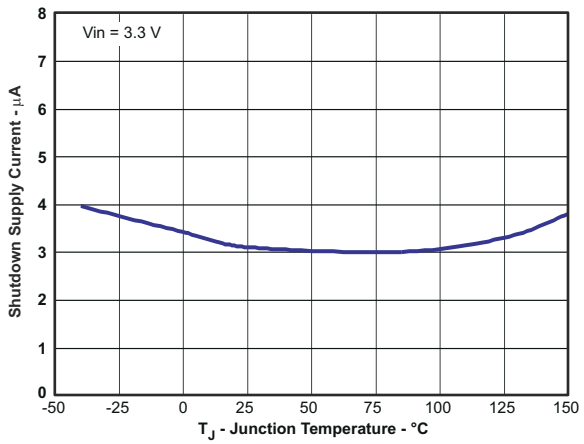


図 6-14. Shutdown Supply Current vs Junction Temperature

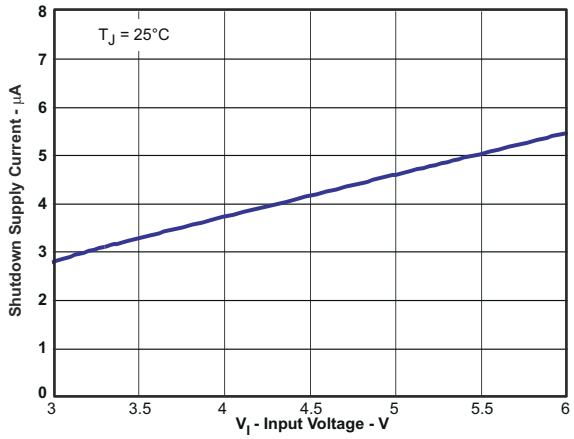


図 6-15. Shutdown Supply Current vs Input Voltage

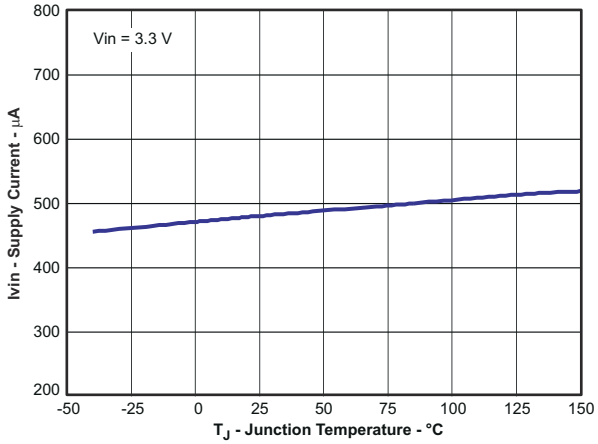


図 6-16. Supply Current vs Junction Temperature

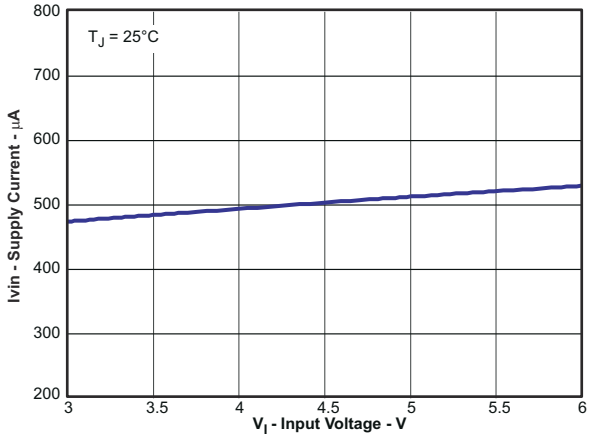


図 6-17. Supply Current vs Input Voltage

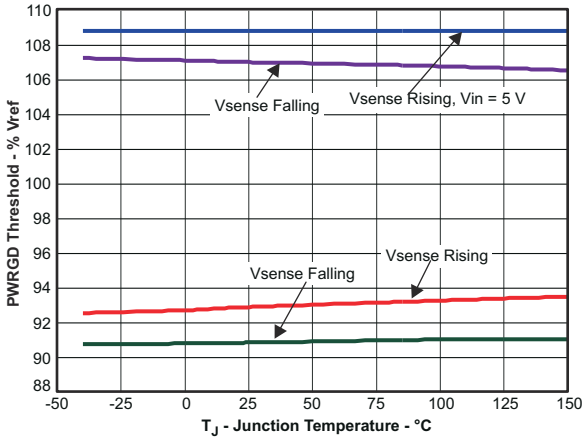


図 6-18. PWRGD Threshold vs Junction Temperature

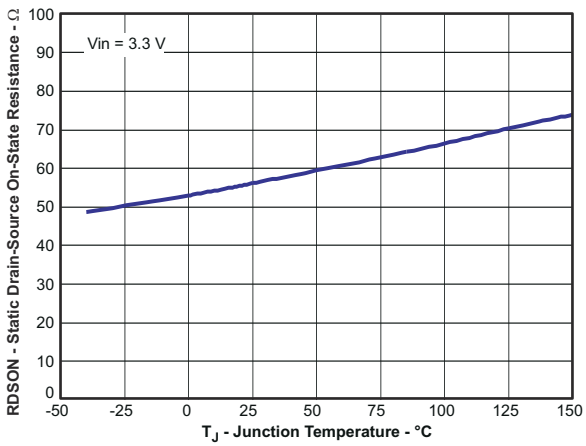


図 6-19. PWRGD ON-Resistance vs Junction Temperature

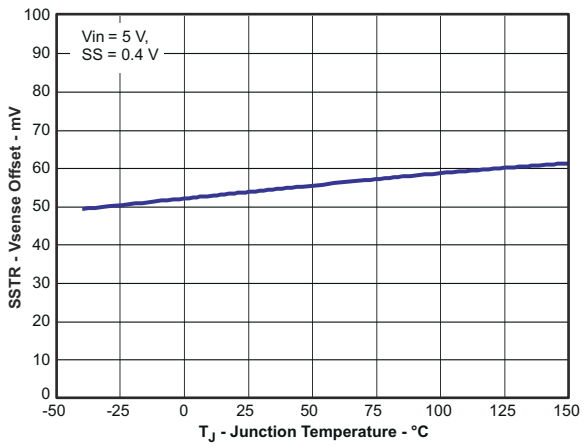


図 6-20. SS/TR to VSENSE Offset vs Junction Temperature

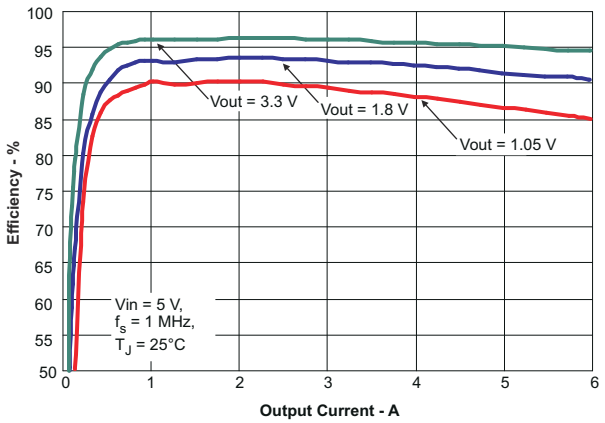


図 6-21. Efficiency vs Load Current

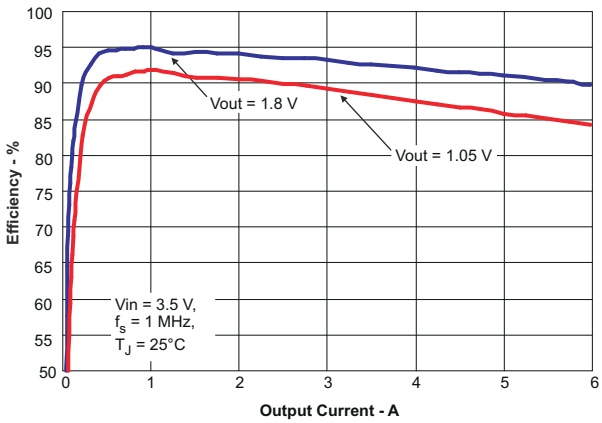


図 6-22. Efficiency vs Load Current

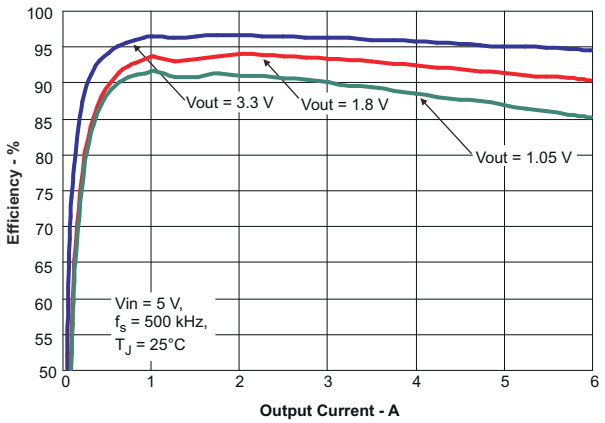


図 6-23. Efficiency vs Load Current

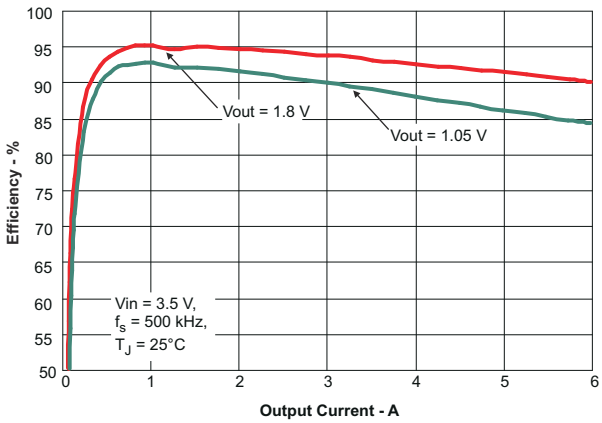


図 6-24. Efficiency vs Load Current

7 Detailed Description

7.1 Overview

The TPS54618C-Q1 is a 6-V, 6-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency range of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turnon to a falling edge of an external system clock.

The TPS54618C-Q1 has a typical default start-up voltage of 2.45 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the TPS54618C-Q1 is typically 515 µA when not switching and under no load. When the device is disabled, the supply current is less than 5.5 µA.

The integrated 12-mΩ MOSFETs allow for high efficiency power supply designs with continuous output currents up to 6 A.

The TPS54618C-Q1 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high-side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS54618C-Q1 to operate approaching 100%. The output voltage can be stepped down to as low as the 0.799-V reference.

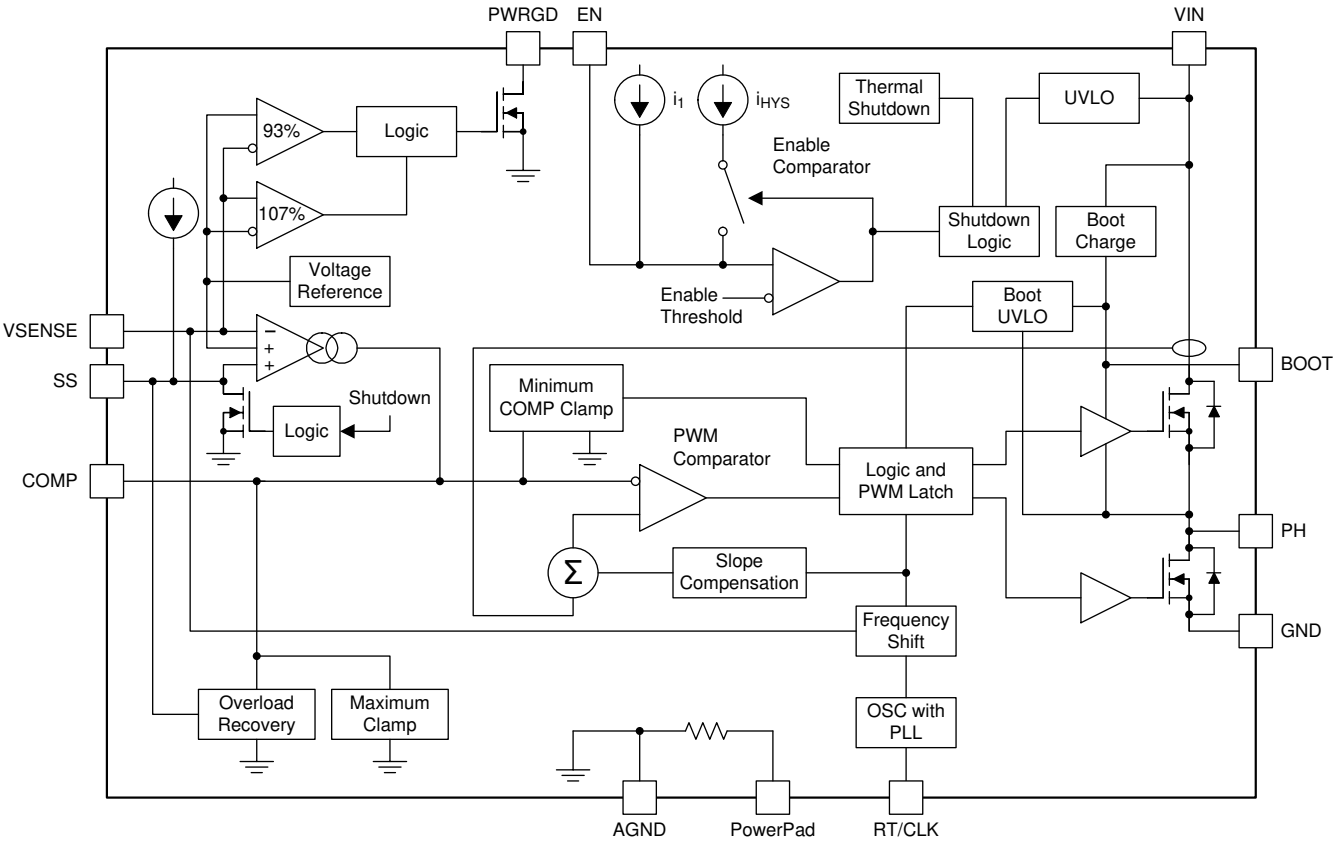
The TPS54618C-Q1 has a power-good comparator (PWRGD) with 2% hysteresis.

The TPS54618C-Q1 minimizes excessive output overvoltage transients by taking advantage of the overvoltage power-good comparator. When the regulated output voltage is greater than 109% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 107%.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor must be coupled to the pin for slow start. The SS/TR pin is discharged before the output power up to ensure a repeatable restart after an overtemperature fault, UVLO fault, or disabled condition.

The use of a frequency foldback circuit reduces the switching frequency during start-up and over current fault conditions to help limit the inductor current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS54618C-Q1 uses an adjustable, fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turnon of the high-side power switch. The error amplifier output is compared to the high-side power switch current. When the power switch current reaches the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient response performance.

7.3.2 Slope Compensation and Output Current

The TPS54618C-Q1 adds a compensating ramp to the switch current signal. This slope compensation prevents subharmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty cycle range.

7.3.3 Bootstrap Voltage (Boot) and Low Dropout Operation

The TPS54618C-Q1 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor must be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve dropout, the TPS54618C-Q1 is designed to operate at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.2 V. The high-side MOSFET is turned off using a UVLO circuit, allowing for the low-side MOSFET to conduct when the voltage from BOOT to PH drops below 2.2 V. Because the supply current

sourced from the BOOT pin is very low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is very high.

7.3.4 Error Amplifier

The TPS54618C-Q1 has a transconductance amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.799-V voltage reference. The transconductance of the error amplifier is 245 µA/V during normal operation. When the voltage of VSENSE pin is below 0.799 V and the device is regulating using the SS/TR voltage, the gm is typically greater than 79 µA/V, but less than 245 µA/V. The frequency compensation components are placed between the COMP pin and ground.

7.3.5 Voltage Reference

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature-stable bandgap circuit. The bandgap and scaling circuits produce 0.799 V at the noninverting input of the error amplifier.

7.3.6 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. TI recommends using divider resistors with 1% tolerance or better. Pick a suitable value for the R1 resistor and use 式 1 to calculate R2. To improve efficiency at very light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = R1 \times \left(\frac{0.799\ V}{V_O - 0.799\ V} \right) \quad (1)$$

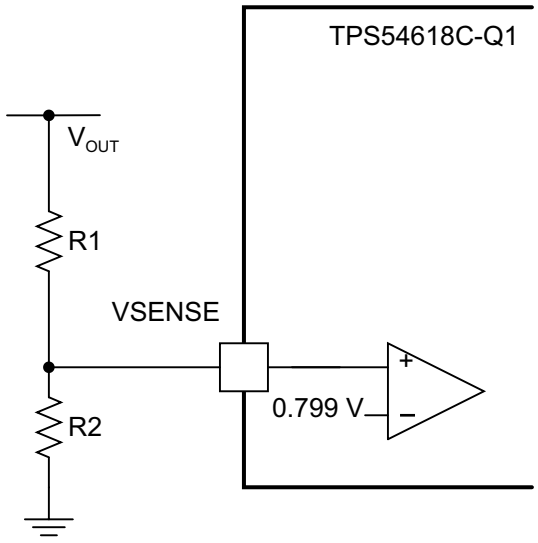


図 7-1. Voltage Divider Circuit

7.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54618C-Q1 is disabled when the VIN pin voltage falls below 2.28 V. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in 図 7-2 to adjust the input voltage UVLO by using two external resistors. TI recommends using the EN resistors to set the UVLO falling threshold (V_{STOP}) above 2.6 V. The rising threshold (V_{START}) must be set to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pullup current source that provides the default condition of the TPS54618C-Q1 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 1.6 µA of hysteresis is added. When the EN pin is pulled below 1.18 V, the 1.6 µA is removed. This additional current facilitates input voltage hysteresis.

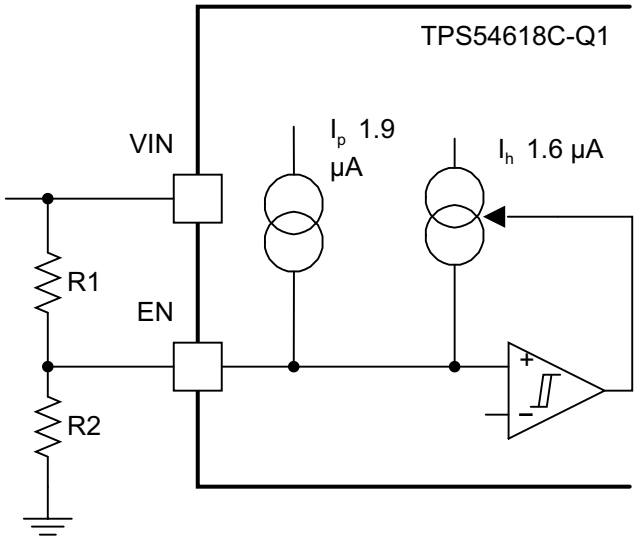


図 7-2. Adjustable Undervoltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (3)$$

where

- R1 and R2 are in Ω
- I_h = 1.6 µA
- I_p = 1.9 µA
- $V_{ENRISING}$ = 1.25 V
- $V_{ENFALLING}$ = 1.18 V

7.3.8 Soft-Start Pin

The TPS54618C-Q1 regulates to the lower of the SS/TR pin and the internal reference voltage. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS54618C-Q1 has an internal pullup current source of 2 µA, which charges the external slow-start capacitor. 式 4 calculates the required slow-start capacitor value.

$$Css(nF) = \frac{Tss(mS) \times Iss(\mu A)}{Vref(V)} \quad (4)$$

where

- Tss is the desired slow-start time in ms
- Iss is the internal slow-start charging current of 2 µA
- Vref is the internal voltage reference of 0.799 V

If, during normal operation, the VIN goes below UVLO, the EN pin pulls below 1.2 V, or a thermal shutdown event occurs, the TPS54618C-Q1 stops switching. When the VIN goes above UVLO, EN is released or pulled high, or a thermal shutdown is exited, then SS/TR is discharged to below 40 mV before reinitiating a powering-

up sequence. The VSENSE voltage follows the SS/TR pin voltage with a 54-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage, the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference.

7.3.9 Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins. The sequential method can be implemented using an open-drain or collector output of a power-on reset pin of another device. 図 7-3 shows the sequential method. The power good is coupled to the EN pin on the TPS54618C-Q1 which enables the second power supply once the primary supply reaches regulation.

Ratio-metric start-up can be accomplished by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, the pullup current source must be doubled in 式 4. The ratio-metric method is shown in 図 7-5.

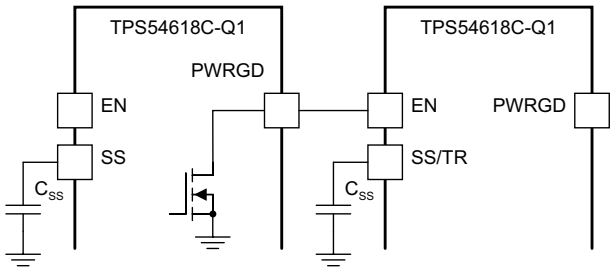


図 7-3. Sequential Start-Up Sequence

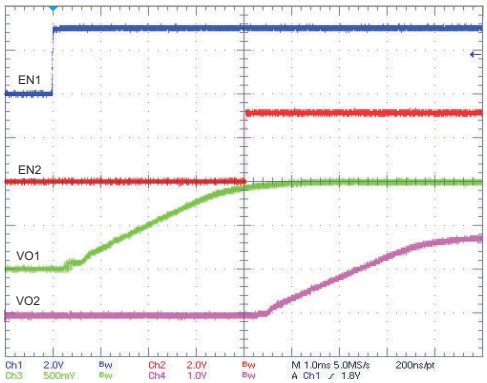


図 7-4. Sequential Start-Up Using EN and PWRGD

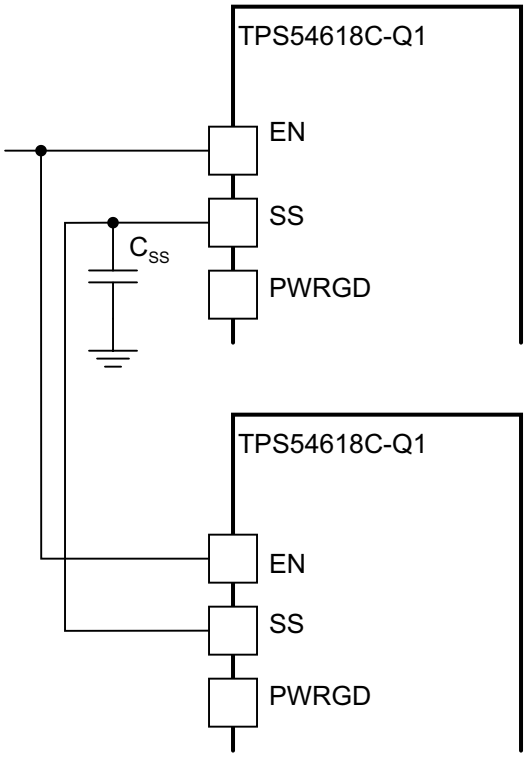


図 7-5. Schematic for Ratio-Metric Start-Up Sequence

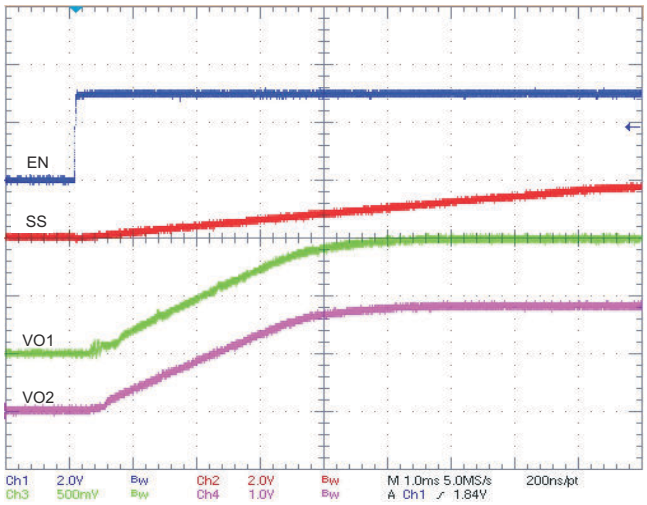


図 7-6. Ratio-Metric Start-Up

Ratio-metric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in 図 7-7 to the output of the power supply that needs to be tracked or another voltage reference source. Using 式 5 and 式 6, the tracking resistors can be calculated to initiate the Vout2 slightly before, after, or at the same time as Vout1. 式 7 is the voltage difference between Vout1 and Vout2. The ΔV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset (Vssoffset) in the slow-start circuit and the offset created by the pullup current source (I_{ss}) and tracking resistors, the Vssoffset and I_{ss} are included as variables in the equations. To design a ratio-metric start-up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in 式 5 through 式 7 for ΔV. 式 7 results in a positive number for applications which the Vout2 is slightly lower than Vout1 when Vout2 regulation is achieved. Because the SS/TR pin must be pulled below 40 mV before starting after an EN, UVLO, or thermal shutdown fault, careful selection of the tracking resistors is needed to ensure the device restarts after a fault. Make sure the calculated R1 value from 式 5 is greater than the value calculated in 式 8 to ensure the device can recover from a fault. As the SS/TR voltage becomes more than 85% of the nominal reference voltage the Vssoffset becomes larger as the slow-start circuits gradually handoff the regulation reference to the internal voltage reference. The SS/TR pin voltage needs to be greater than 1.1 V for a complete hand off to the internal voltage reference as shown in 図 7-6.

$$R1 = \frac{Vout2 + \Delta V}{Vref} \times \frac{Vssoffset}{Iss} \quad (5)$$

$$R2 = \frac{Vref \times R1}{Vout2 + \Delta V - Vref} \quad (6)$$

$$\Delta V = Vout1 - Vout2 \quad (7)$$

$$R1 > 2930 \times Vout1 - 145 \times \Delta V \quad (8)$$

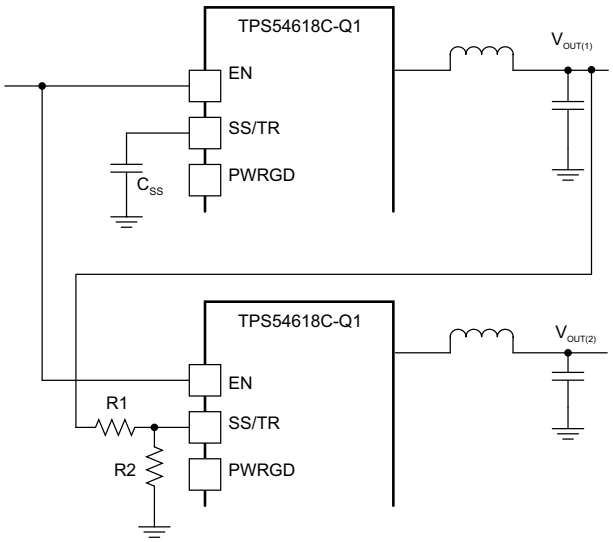


図 7-7. Ratio-Metric and Simultaneous Start-Up Sequence

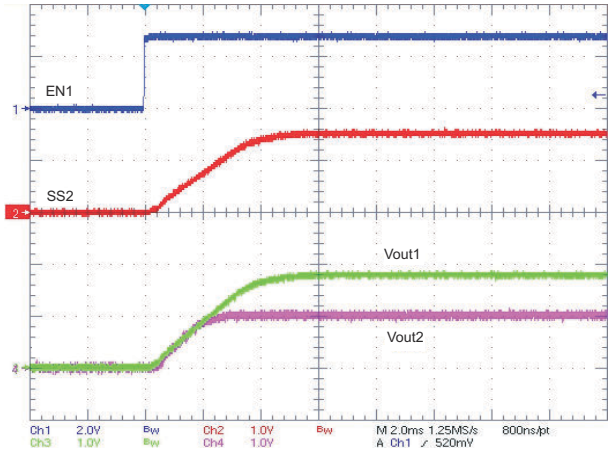


図 7-8. Ratio-Metric Start-Up Using Coupled SS/TR Pins

7.3.10 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54618C-Q1 is adjustable over a wide range from 300 kHz to 2000 kHz by placing a maximum of 700 kΩ and minimum of 85 kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in 式 9 or 式 10.

$$RT\left(k\Omega\right) = \frac{235892}{f_{SW}\left(kHz\right)^{1.027}} \quad (9)$$

$$f_{SW}\left(kHz\right) = \frac{171032}{RT\left(k\Omega\right)^{0.974}} \quad (10)$$

To reduce the solution size, you would typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage, and minimum controllable ON-time must be considered.

The minimum controllable ON-time is typically 75 ns at full current load and 120 ns at no load, and limits the maximum operating input voltage or output voltage.

7.3.11 Overcurrent Protection

The TPS54618C-Q1 implements a cycle-by-cycle current limit. During each switching cycle, the high-side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit.

7.3.12 Frequency Shift

To operate at high switching frequencies and provide protection during overcurrent conditions, the TPS54618C-Q1 implements a frequency shift. If frequency shift was not implemented during an overcurrent condition, the low-side MOSFET may not be turned off long enough to reduce the current in the inductor, causing a current runaway. With frequency shift during an overcurrent condition, the switching frequency is reduced from 100%, then 50%, then 25%, as the voltage decreases from 0.799 to 0 V on VSENSE pin to allow the low-side MOSFET to be off long enough to decrease the current in the inductor. During start-up, the switching frequency increases as the voltage on VSENSE increases from 0 to 0.799 V.

7.3.13 Reverse Overcurrent Protection

The TPS54618C-Q1 implements low-side current protection by detecting the voltage across the low-side MOSFET. When the converter sinks current through its low-side FET, the control circuit turns off the low-side MOSFET if the reverse current is typically more than 4.5 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into prebiased outputs.

7.3.14 Synchronize Using the RT/CLK Pin

The RT/CLK pin is used to synchronize the converter to an external system clock. See 図 7-9. To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an ON-time of at least 75 ns. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to the frequency set by the resistor. The square wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V typically. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of the PH is synchronized to the falling edge of RT/CLK pin.

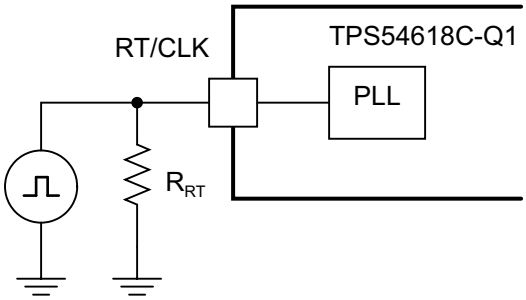


図 7-9. Synchronizing to a System Clock

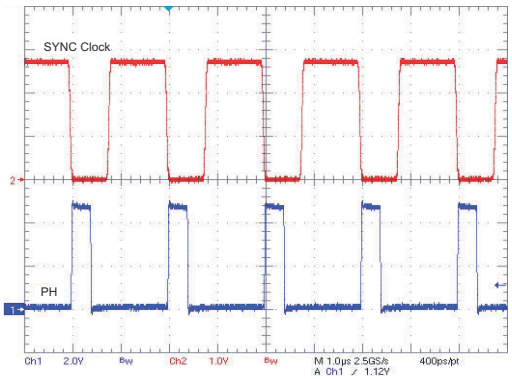


図 7-10. Plot of Synchronizing to System Clock

7.3.15 Power Good (PWRGD Pin)

The PWRGD pin output is an open-drain MOSFET. The output is pulled low when the VSENSE voltage enters the fault condition by falling below 91% or rising above 109% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the VSENSE voltage rises to the good condition above 93% or falls below 107% of the internal voltage reference, the PWRGD output MOSFET is turned off. TI recommends using a pullup resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 6 V or less. The PWRGD is in a valid state once the VIN input voltage is greater than 1.5 V.

7.3.16 Overvoltage Transient Protection

The TPS54618C-Q1 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to the OVTP threshold which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold, the high-side MOSFET is allowed to turn on the next clock cycle.

7.3.17 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 168°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 150°C, the device reinitiates the power-up sequence by discharging the SS pin to below 40 mV. The thermal shutdown hysteresis is 20°C.

7.4 Device Functional Modes

7.4.1 Simple Small Signal Model for Peak Current Mode Control

図 7-11 shows an equivalent model for the TPS54618C-Q1 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm of 245 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R0 and capacitor Co model the open loop gain and frequency response of the amplifier. The 1-mV AC voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

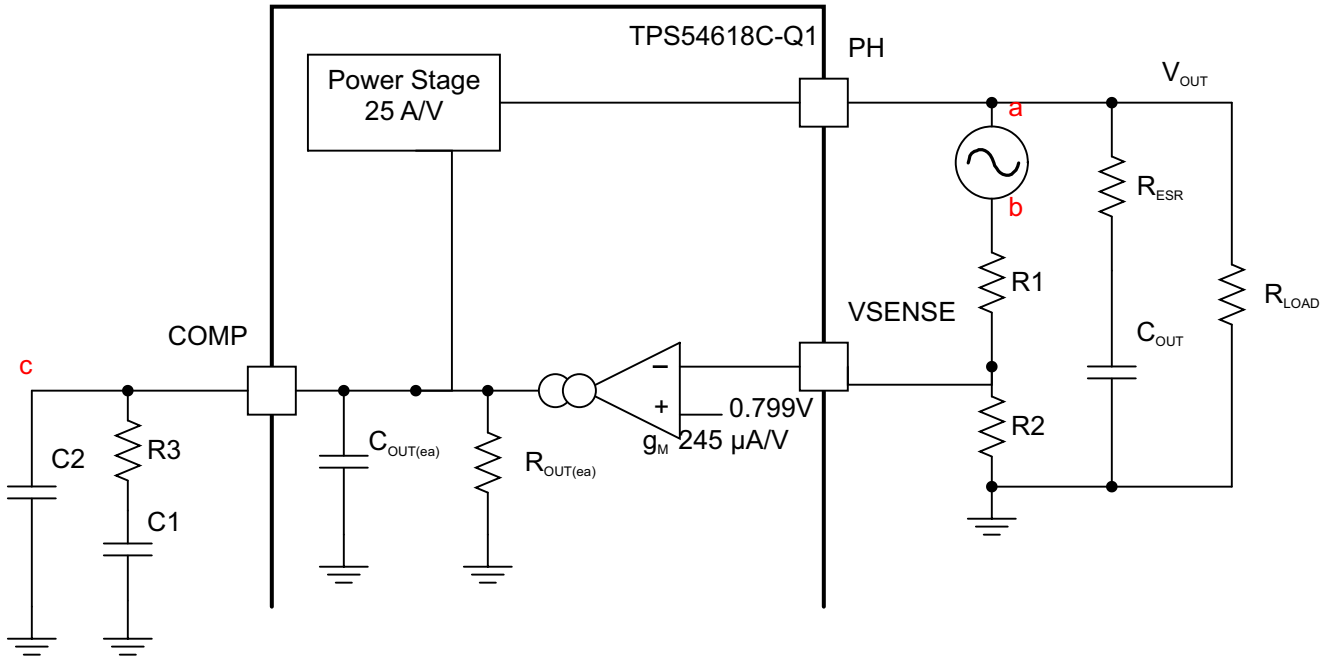


図 7-11. Small Signal Model for Loop Response

図 7-11 is a simple, small-signal model that can be used to understand how to design the frequency compensation. The TPS54618C-Q1 power stage can be approximated to a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in 式 11 and consists of a DC gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in 図 7-11) is the power stage transconductance. The gm for the TPS54618C-Q1 is 25 A/V. The low frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in 式 12. As the load current increases and decreases, the low frequency gain decreases and increases, respectively. This variation with load can seem problematic at first glance, but the dominant pole moves with load current. The combined effect is highlighted by the dashed line in the right half of 図 7-13. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

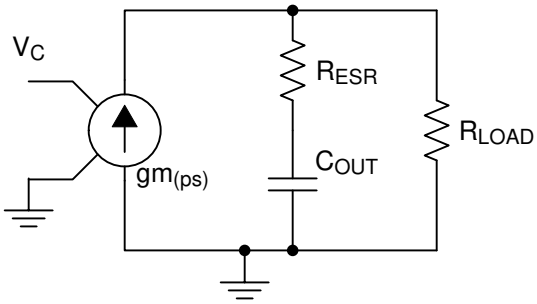


図 7-12. Small Signal Model for Peak Current Mode Control

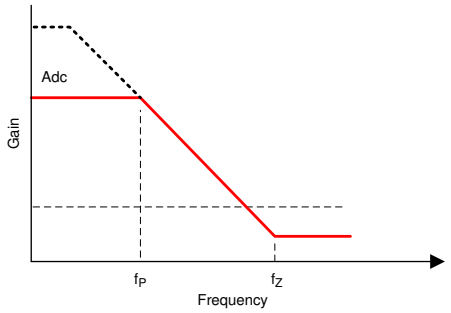


図 7-13. Frequency Response Model for Peak Current Mode Control

$$\frac{vo}{vc} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (11)$$

$$Adc = gm_{ps} \times R_L \quad (12)$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (13)$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (14)$$

7.4.2 Small Signal Model for Frequency Compensation

The TPS54618C-Q1 uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits. The compensation circuits are shown in 図 7-14. The Type-2 circuits are most likely implemented in high-bandwidth power supply designs using low-ESR output capacitors. In Type 2A, one additional high-frequency pole is added to attenuate high-frequency noise.

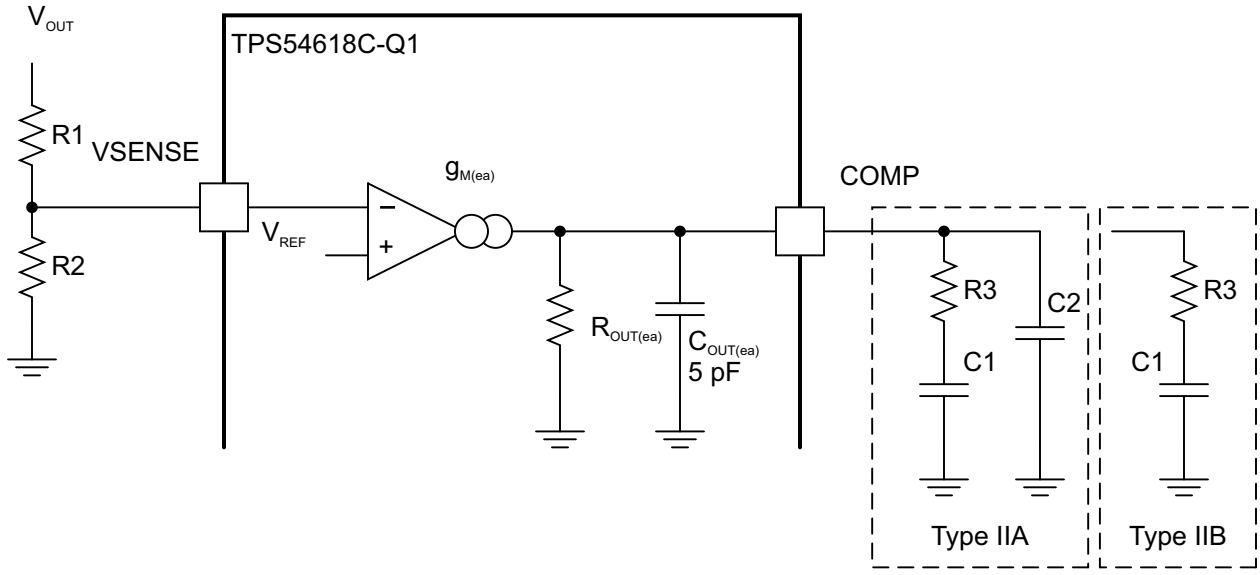


図 7-14. Types of Frequency Compensation

The design guidelines for TPS54618C-Q1 loop compensation are as follows:

1. The modulator pole, fpmod, and the esr zero, fz1, must be calculated using 式 15 and 式 16. Derating the output capacitor (C_{OUT}) can be needed if the output voltage is a high percentage of the capacitor rating. Use the capacitor manufacturer information to derate the capacitor value. Use 式 17 and 式 18 to estimate a starting point for the crossover frequency, fc. 式 17 is the geometric mean of the modulator pole and the esr zero and 式 18 is the mean of modulator pole and the switching frequency. Use the lower value of 式 17 or 式 18 as the maximum crossover frequency.

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \quad (15)$$

$$fz\ mod = \frac{1}{2\pi \times Resr \times Cout} \quad (16)$$

$$f_C = \sqrt{fp\ mod \times fz\ mod} \quad (17)$$

$$f_C = \sqrt{fp\ mod \times \frac{fsw}{2}} \quad (18)$$

2. R3 can be determined by 式 19:

$$R3 = \frac{2\pi \times fc \times Vo \times C_{OUT}}{gm_{ea} \times Vref \times gm_{ps}} \quad (19)$$

where

- the gm_{ea} amplifier gain (245 µA/V)
- gm_{ps} is the power stage gain (25 A/V)

3. Place a compensation zero at the dominant pole:

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi}$$

C1 can be determined by 式 20:

$$C1 = \frac{R_L \times C_{OUT}}{R3} \quad (20)$$

4. C2 is optional. It can be used to cancel the zero from the ESR of C_{OUT}.

$$C2 = \frac{Resr \times C_{OUT}}{R3} \quad (21)$$

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

This design example describes a high-frequency switching regulator design using ceramic output capacitors. This design is available as the HPA606 evaluation module (EVM).

8.2 Typical Application

This section details a high-frequency, 1.8-V output power supply design application with adjusted UVLO.

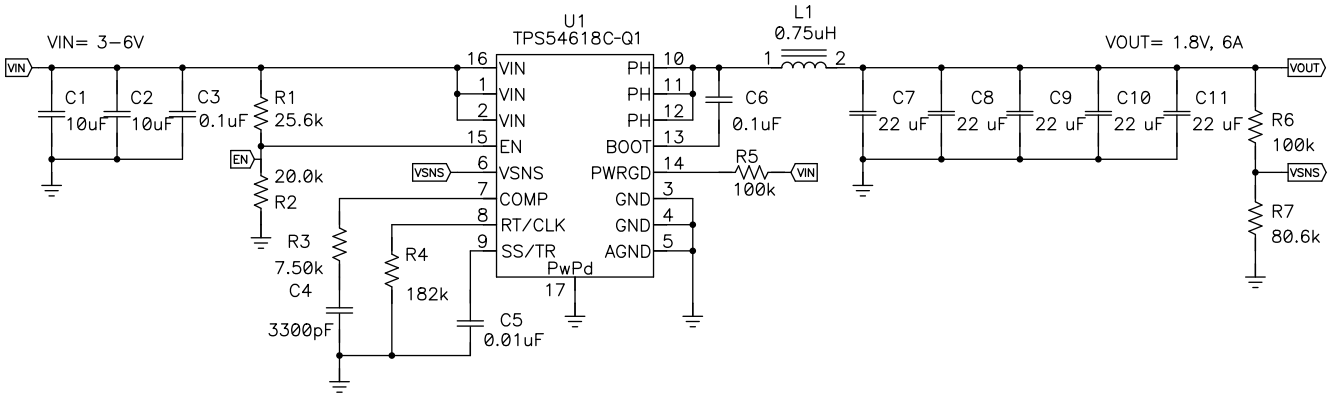


図 8-1. Typical Application Schematic TPS54618C-Q1

8.2.1 Design Requirements

The design parameters for the TPS54618C-Q1 are listed in 表 8-1.

表 8-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	Operating	3	3.3	6	V
V_{OUT}	Output voltage			1.8		V
ΔV_{OUT}	Transient response	1.5-A to 4.5-A load step		4%		
$I_{OUT(max)}$	Maximum output current				6	A
$V_{OUT(ripple)}$	Output voltage ripple				30	mV_{P-P}
f_{SW}	Switching frequency			1000		kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Step One: Select the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, you want to choose the highest switching frequency possible because this produces the smallest solution size. The high-switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the performance of the converter. The converter is capable of running from 300 kHz to 2 MHz. Unless a small solution size is an ultimate goal, a moderate switching frequency of 1 MHz is selected to achieve both a small solution size and a high-efficiency operation. Using 式 9, R4 is calculated to be 180 kΩ. A standard 1% 182-kΩ value was chosen in the design.

8.2.2.2 Step Two: Select the Output Inductor

The inductor selected works for the entire TPS54618C-Q1 input voltage range. To calculate the value of the output inductor, use 式 22. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use K_{IND} = 0.3 and the inductor value is calculated to be 0.7 µH. For this design, a nearest standard value was chosen: 0.75 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from 式 24 and 式 25.

For this design, the RMS inductor current is 6.01 A and the peak inductor current is 6.84 A. The chosen inductor is a Toko FDV0630-R75M. It has a saturation current rating of 10 A and a RMS current rating of 8.9 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \tag{22}$$

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw} \tag{23}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw} \right)^2} \tag{24}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{25}$$

8.2.2.3 Step Three: Choose the Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired holdup times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The

output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. 式 26 shows the minimum output capacitance necessary to accomplish this.

For this example, the transient load response is specified as a 3% change in Vout for a load step from 1.5 A (25% load) to 4.5 A (75% load). For this example, ΔIout = 4.5 – 1.5 = 3.0 A and ΔVout = 0.04 × 1.8 = 0.072 V. Using these numbers gives a minimum capacitance of 83 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

式 27 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, 式 27 yields 7 µF.

$$Co > \frac{2 \times \Delta Iout}{fsw \times \Delta Vout} \tag{26}$$

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \tag{27}$$

where

- ΔIout is the change in output current
- *f*sw is the regulators switching frequency
- and ΔVout is the allowable change in the output voltage

式 28 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. 式 28 indicates the ESR should be less than 18 mΩ. In this case, the ESR of the ceramic capacitor is much less than 18 mΩ.

Additional capacitance de-ratings for aging, temperature and DC bias must be factored in which increases this minimum value. For this example, five 22-µF, 10-V X5R ceramic capacitors with 3 mΩ of ESR are used. The estimated capacitance after derating by a factor 0.75 is 82.5 µF.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. 式 29 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, 式 29 yields 520 mA.

$$Resr < \frac{Voripple}{Iripple} \tag{28}$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \tag{29}$$

8.2.2.4 Step Four: Select the Input Capacitor

The TPS54618C-Q1 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance and in some applications, a bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54618C-Q1. The input ripple current can be calculated using 式 30.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 10-V voltage rating is required to support the maximum input voltage. For this example, two 10-µF and one 0.1-µF 10-V capacitors in parallel have been selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 式 31. Using the design example values (Ioutmax = 6 A, Cin = 20 µF, Fsw = 1 MHz) yields an input voltage ripple of 149 mV and an RMS input ripple current of 2.94 A.

$$Icirms = Iout \times \sqrt{\frac{Vout}{Vinmin} \times \frac{(Vinmin - Vout)}{Vinmin}} \tag{30}$$

$$\Delta Vin = \frac{Ioutmax \times 0.25}{Cin \times fsw} \tag{31}$$

8.2.2.5 Step Five: Choose the Soft-Start Capacitor

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54618C-Q1 reach the current limit or excessive current draw from the input power supply can cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow-start capacitor value can be calculated using 式 32. For the example circuit, the slow-start time is not too critical because the output capacitor value is 110 µF which does not require much current to charge to 1.8 V. The example circuit has the slow-start time set to an arbitrary value of 4 ms which requires a 10-nF capacitor. In TPS54618C-Q1, I_{ss} is 2.2 µA and Vref is 0.799 V.

$$Css(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \tag{32}$$

8.2.2.6 Step Six: Select the Bootstrap Capacitor

A 0.1-µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. TI recommends using a ceramic capacitor with X5R or better grade dielectric. The capacitor must have 10-V or higher voltage rating.

8.2.2.7 Step Eight: Select Output Voltage and Feedback Resistors

For the example design, 100 kΩ was selected for R6. Using 式 33, R7 is calculated as 80 kΩ. The nearest standard 1% resistor is 80.6 kΩ.

$$R7 = \frac{Vref}{Vo - Vref} R6 \quad (33)$$

8.2.2.7.1 Output Voltage Limitations

Due to the internal design of the TPS54618C-Q1, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.799 V. Above 0.799 V, the output voltage can be limited by the minimum controllable ON-time. The minimum output voltage in this case is given by 式 34.

$$Voutmin = Ontimemin \times Fsmax \times (Vinmax - Ioutmin \times RDSmin) - Ioutmin \times (RL + RDSmin) \quad (34)$$

where

- Voutmin = minimum achievable output voltage
- Ontimemin = minimum controllable ON-time (75 ns typical. 120 ns no load)
- Fsmax = maximum switching frequency including tolerance
- Vinmax = maximum input voltage
- Ioutmin = minimum load current
- RDSmin = minimum high-side MOSFET ON-resistance (see *セクション 6.5*)
- RL = series resistance of output inductor

There is also a maximum achievable output voltage which is limited by the minimum OFF-time. The maximum output voltage is given by 式 35.

$$Voutmax = Vin \times \left(1 - \frac{Offtimemax}{ts}\right) - Ioutmax \times (RDSmax + RI) - (0.7 - Ioutmax \times RDSmax) \times \left(\frac{tdead}{ts}\right) \quad (35)$$

where

- Voutmax = maximum achievable output voltage
- Vin = minimum input voltage
- Offtimemax = maximum OFF-time (90 ns typical for adequate margin)
- ts = 1/Fs
- Ioutmax = maximum current
- RDSmax = maximum high-side MOSFET ON-resistance (see *セクション 6.5*)
- RI = DCR of the inductor
- tdead = dead time (60 ns)

8.2.2.8 Step Nine: Select Loop Compensation Components

There are several industry techniques used to compensate DC–DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54618C-Q1. Because the slope compensation is ignored, the actual cross over frequency is usually lower than the cross over frequency used in the calculations. Use SwitcherPro™ software for a more accurate design.

To get started, the modulator pole, fpmod, and the esr zero, fz1, must be calculated using 式 36 and 式 37. For C_{OUT}, the derated capacitance value is 82.5 µF. Use 式 38 and 式 39 to estimate a starting point for the crossover frequency, fc. For the example design, fpmod is 6.43 kHz and fzmod is 643 kHz. 式 38 is the geometric mean of the modulator pole and the esr zero and 式 39 is the mean of modulator pole and the switching frequency. 式 38 yields 64.3 kHz and 式 39 gives 56.7 kHz. The lower value of 式 38 or 式 39 is the maximum recommended crossover frequency. For this example, a lower fc value of 40 kHz is specified. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole (if needed).

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \quad (36)$$

$$fz\ mod = \frac{1}{2\pi \times Resr \times Cout} \quad (37)$$

$$f_C = \sqrt{fp\ mod \times fz\ mod} \quad (38)$$

$$f_C = \sqrt{fp\ mod \times \frac{fsw}{2}} \quad (39)$$

The compensation design takes the following steps:

1. Set up the anticipated crossover frequency. Use 式 40 to calculate the resistor value of the compensation network. In this example, the anticipated crossover frequency (fc) is 40 kHz. The power stage gain (gm_{ps}) is 25 A/V and the error amplifier gain (gm_{ea}) is 245 µA/V.

$$R3 = \frac{2\pi \times fc \times Vo \times Co}{Gm \times Vref \times Vl_{gm}} \quad (40)$$

2. Place compensation zero at the pole formed by the load resistor and the output capacitor. The capacitor of the compensation network can be calculated from 式 41.

$$C4 = \frac{Ro \times Co}{R3} \quad (41)$$

3. An additional pole can be added to attenuate high-frequency noise. In this application, it is not necessary to add it.

From the previously listed procedures, the compensation network includes a 7.50-kΩ resistor and a 3300-pF capacitor.

8.2.3 Application Curves

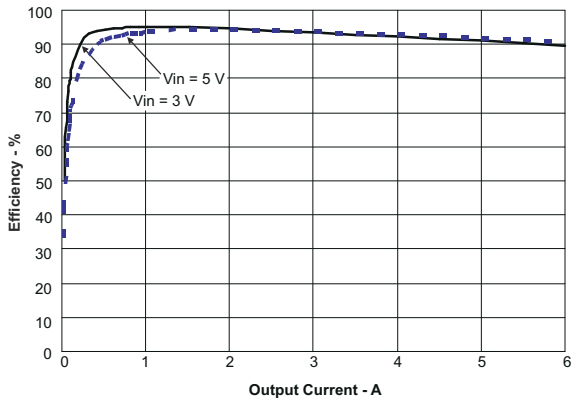


図 8-2. Efficiency vs Load Current

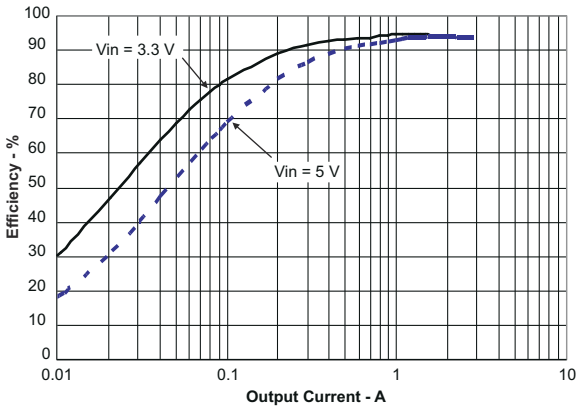


図 8-3. Efficiency vs Load Current

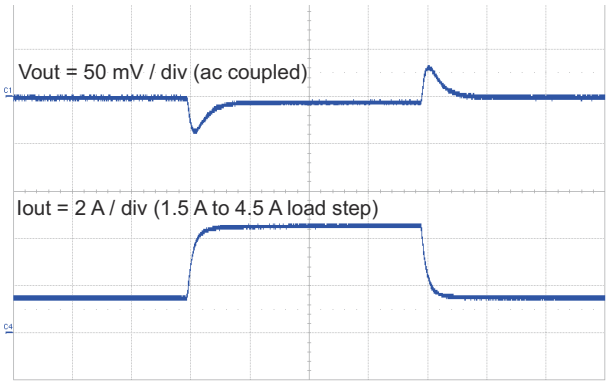


図 8-4. Transient Response

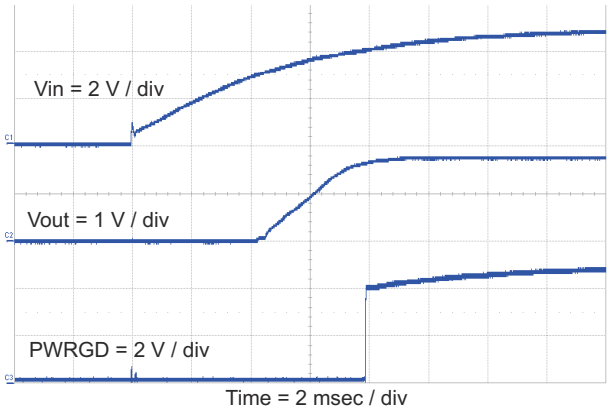


図 8-5. Power Up, V_{OUT}, V_{IN}

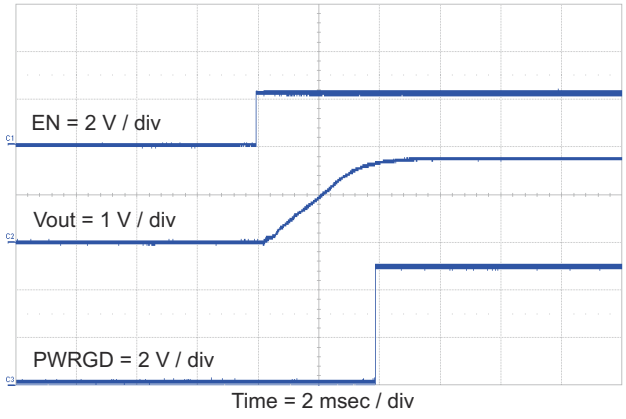


図 8-6. Power Up, V_{OUT}, EN

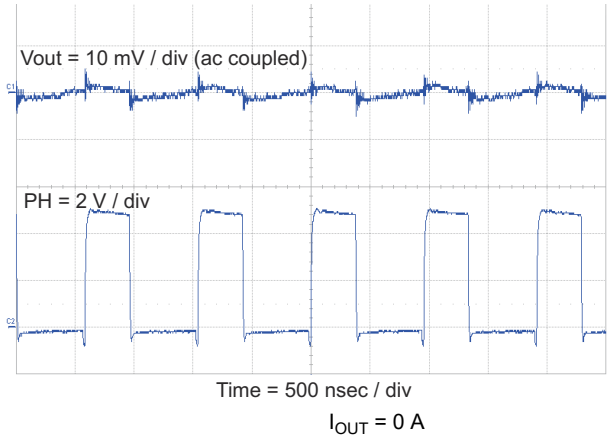
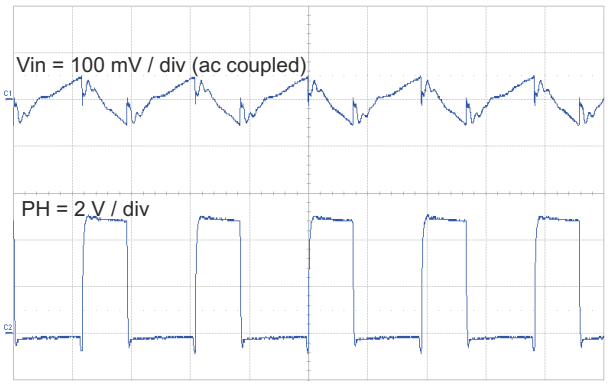
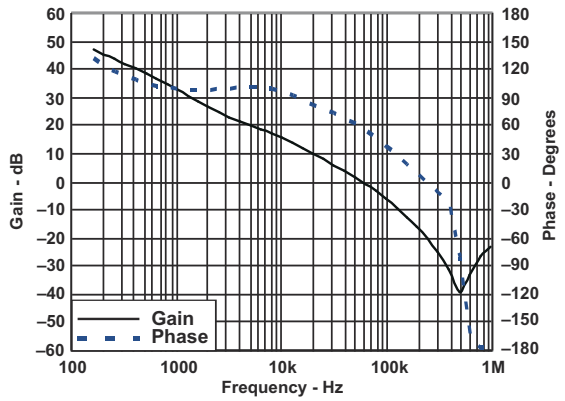


図 8-7. Output Ripple



I_{OUT} = 2A

図 8-8. Input Ripple



V_{IN} = 3.3. V I_{OUT} = 2 A

図 8-9. Closed-Loop Response

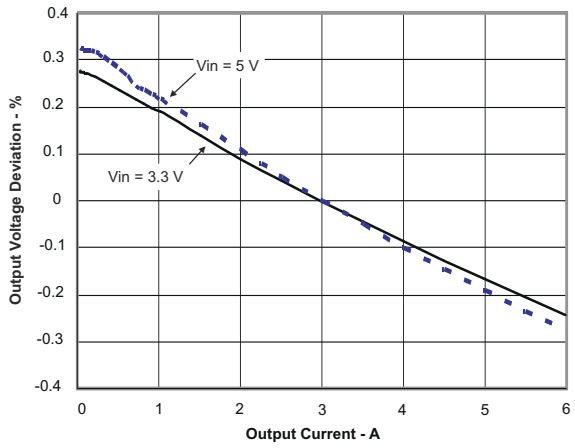


図 8-10. Load Regulation vs Load Current

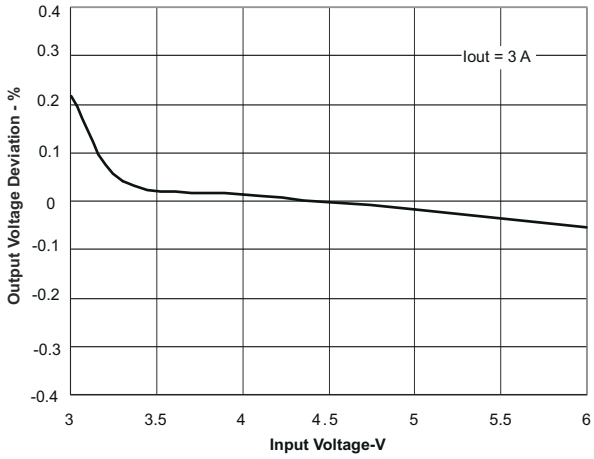


図 8-11. Regulation vs Input Voltage

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply between 2.95 V and 6 V. This supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in セクション *10.1*.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.

- Minimize the loop area formed by the bypass capacitor connections and the VIN pins. See 図 10-1 for a PCB layout example.
- The GND pins and AGND pin should be tied directly to the power pad under the TPS54618C-Q1 device. The power pad must be connected to any internal PCB ground planes using multiple vias directly under the device. Additional vias can be used to connect the top-side ground area to the internal planes near the input and output capacitors. For operation at full rated load, the top-side ground area along with any additional internal ground planes must provide adequate heat dissipating area.
- Place the input bypass capacitor as close to the device as possible.
- Route the PH pin to the output inductor. Because the PH connection is the switching node, place the output inductor close to the PH pins. Minimize the area of the PCB conductor to prevent excessive capacitive coupling.
- The boot capacitor must also be located close to the device.
- The sensitive analog ground connections for the feedback voltage divider, compensation components, soft-start capacitor, and frequency set resistor must be connected to a separate analog ground trace as shown in 図 10-1.
- The RT/CLK pin is particularly sensitive to noise so the RT resistor must be located as close as possible to the device and routed with minimal trace lengths.
- The additional external components can be placed approximately as shown. It is possible to obtain acceptable performance with alternate PCB layouts, however, this layout has been shown to produce good results and can be used as a guide.

10.2 Layout Example

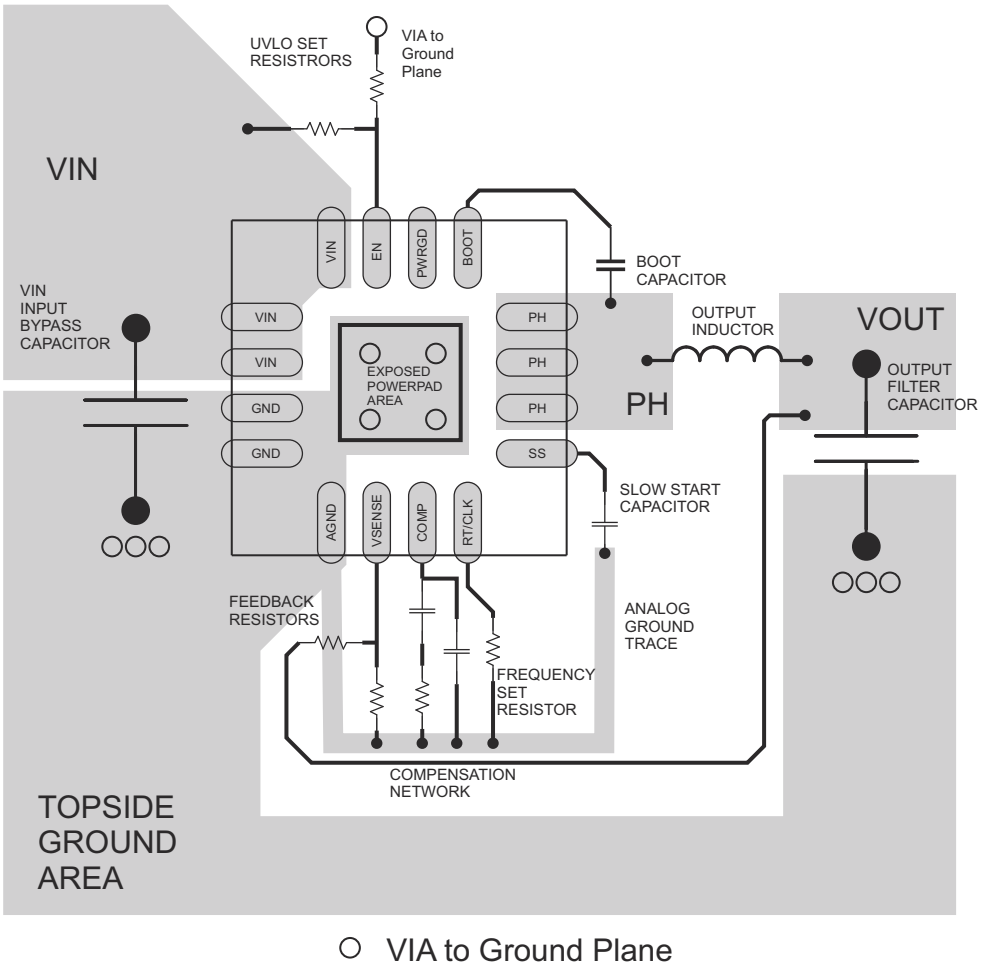


図 10-1. PCB Layout Example

10.3 Power Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous conduction mode (CCM) operation. The power dissipation of the IC (Ptot) includes conduction loss (Pcon), dead time loss (Pd), switching loss (Psw), gate drive loss (Pgd), and supply current loss (Pq).

$$Pcon = Io^2 \times R_{DS\_on\_Temp} \quad (42)$$

where

- I_O is the output current (A)
- $R_{DS\_on\_Temp}$ is the ON-resistance of the high-side MOSFET with given temperature (Ω)

$$Pd = f_{sw} \times Io \times 0.7 \times 40 \times 10^{-9} \quad (43)$$

where

- I_O is the output current (A)
- f_{sw} is the switching frequency (Hz)

$$Psw = 1/2 \times V_{in} \times Io \times f_{sw} \times 13 \times 10^{-9} \quad (44)$$

where

- I_O is the output current (A)
- V_{in} is the input voltage (V)
- f_{sw} is the switching frequency (Hz)

$$Pgd = 2 \times V_{in} \times f_{sw} \times 10 \times 10^{-9} \quad (45)$$

where

- V_{in} is the input voltage (V)
- f_{sw} is the switching frequency (Hz)

$$Pq = V_{in} \times 515 \times 10^{-6} \quad (46)$$

where

- V_{in} is the input voltage (V)

$$Ptot = Pcon + Pd + Psw + Pgd + Pq \quad (47)$$

where

- Ptot is the total device power dissipation (W)

For given T_A:

$$T_J = T_A + Rth \times Ptot \quad (48)$$

where

- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- Rth is the thermal resistance of the package (°C/W)

For given T_{Jmax} = 150°C:

$$T_{Amax} = T_{Jmax} – Rth \times Ptot \quad (49)$$

where

- Ptot is the total device power dissipation (W)
- Rth is the thermal resistance of the package (°C/W)
- T_{Jmax} is maximum junction temperature (°C)
- T_{Amax} is maximum ambient temperature (°C)

There are additional power losses in the regulator circuit due to the inductor AC and DC losses and trace resistance that impact the overall efficiency of the regulator.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Developmental Support

For developmental support, see the following:

- Evaluation Module for TPS54618C-Q1 Synchronous Step-Down SWIFT™ DC/DC Converter, HPA606

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

SwitcherPro™ and TI E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54618CQRTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	618CQ
TPS54618CQRTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	618CQ
TPS54618CQRTERQ1.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	618CQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

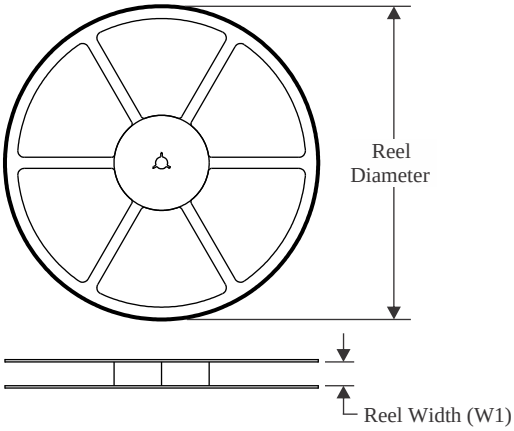
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

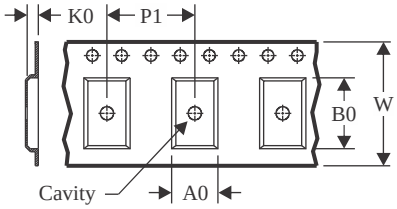
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

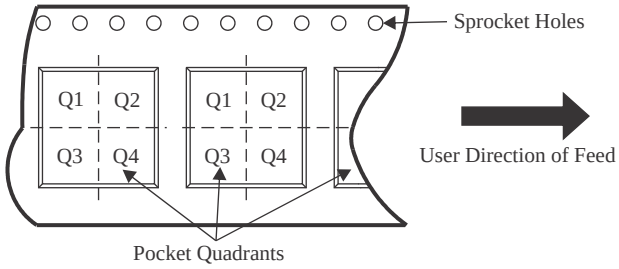


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

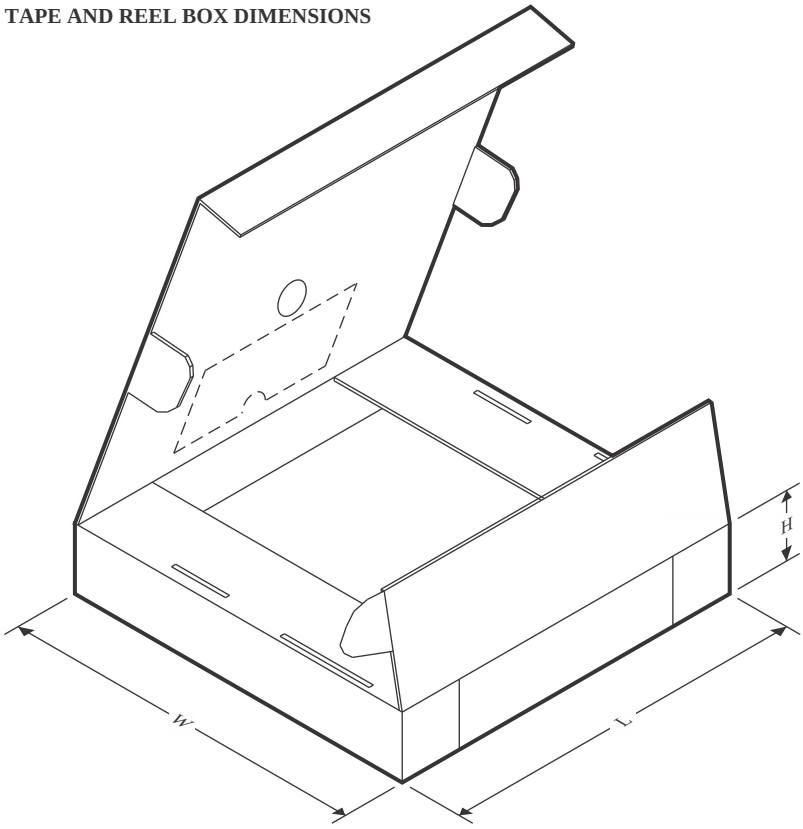
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54618CQRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54618CQRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

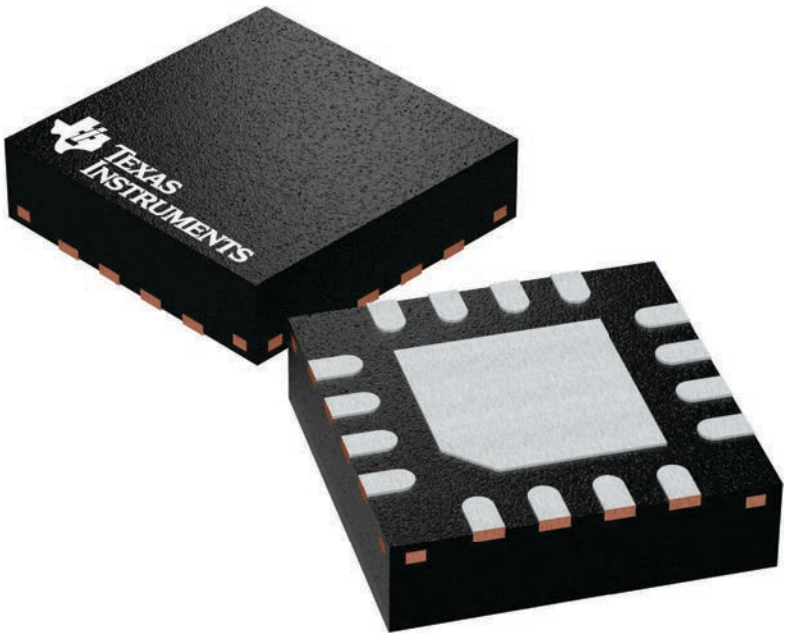
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

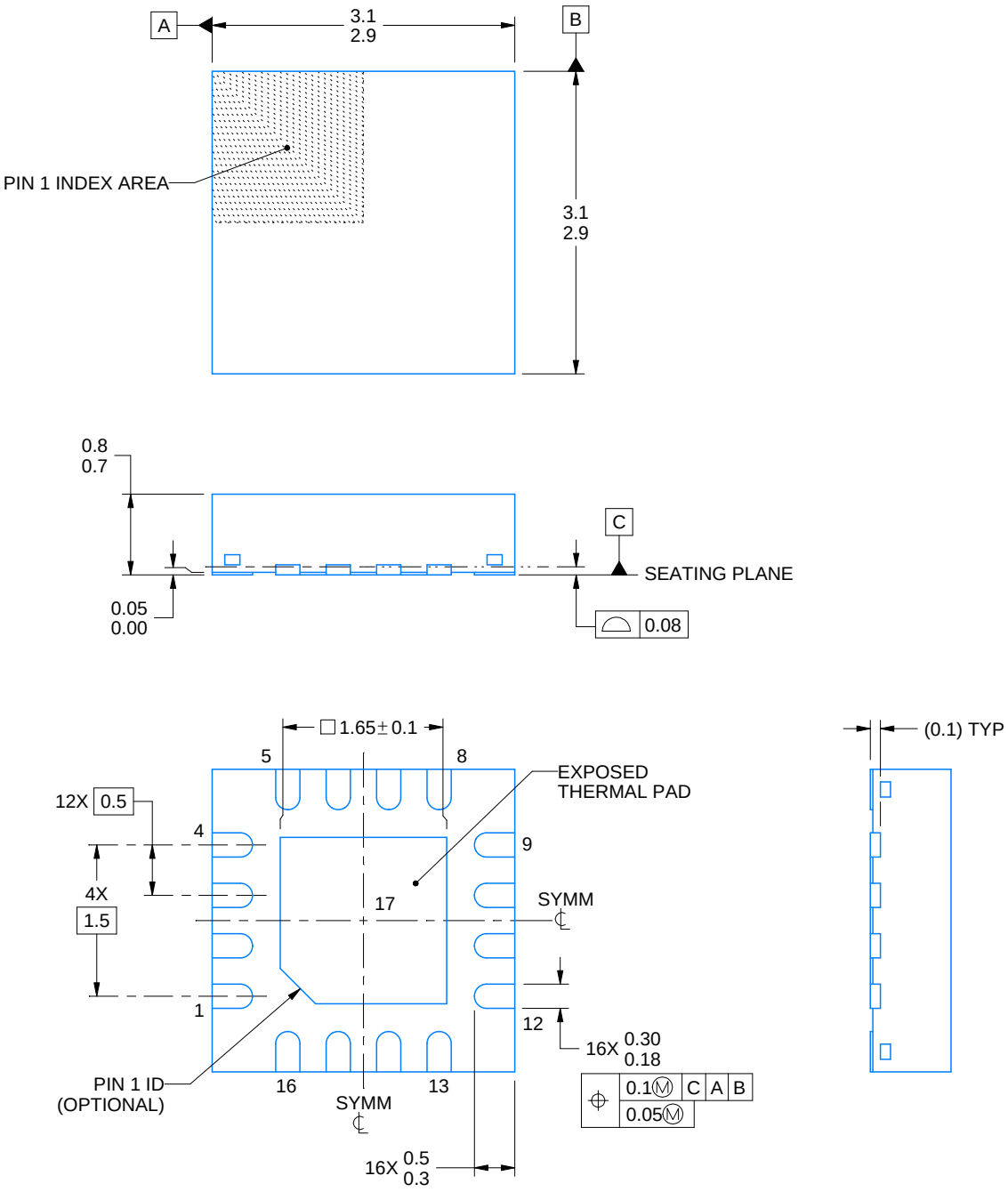


RTE0016F

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

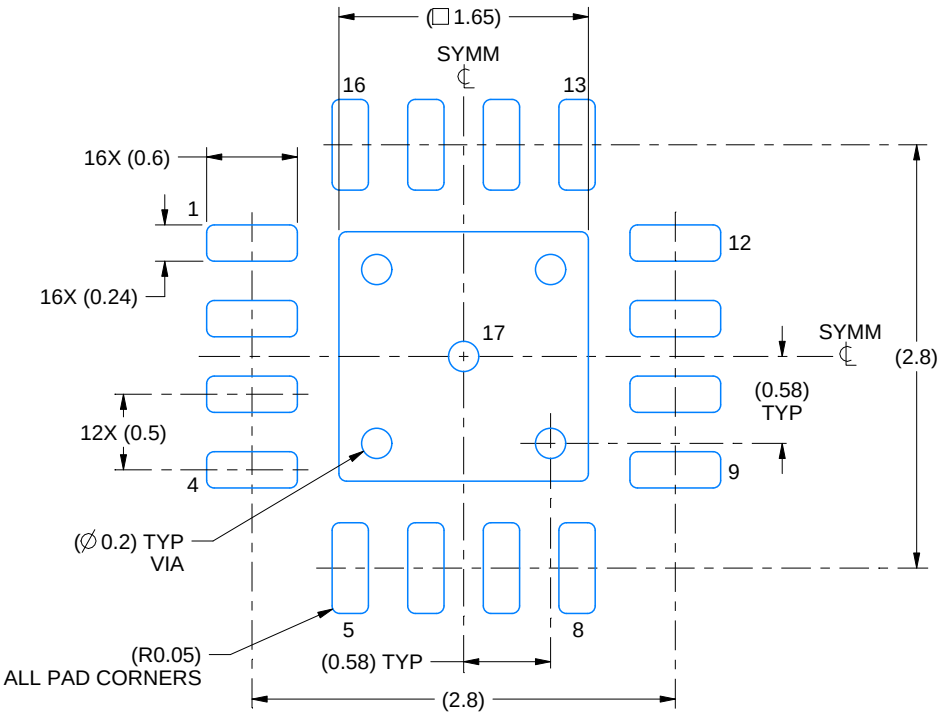
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

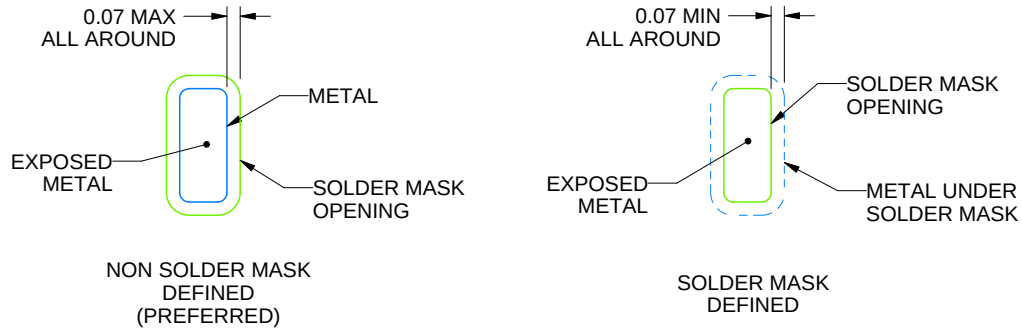
RTE0016F

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

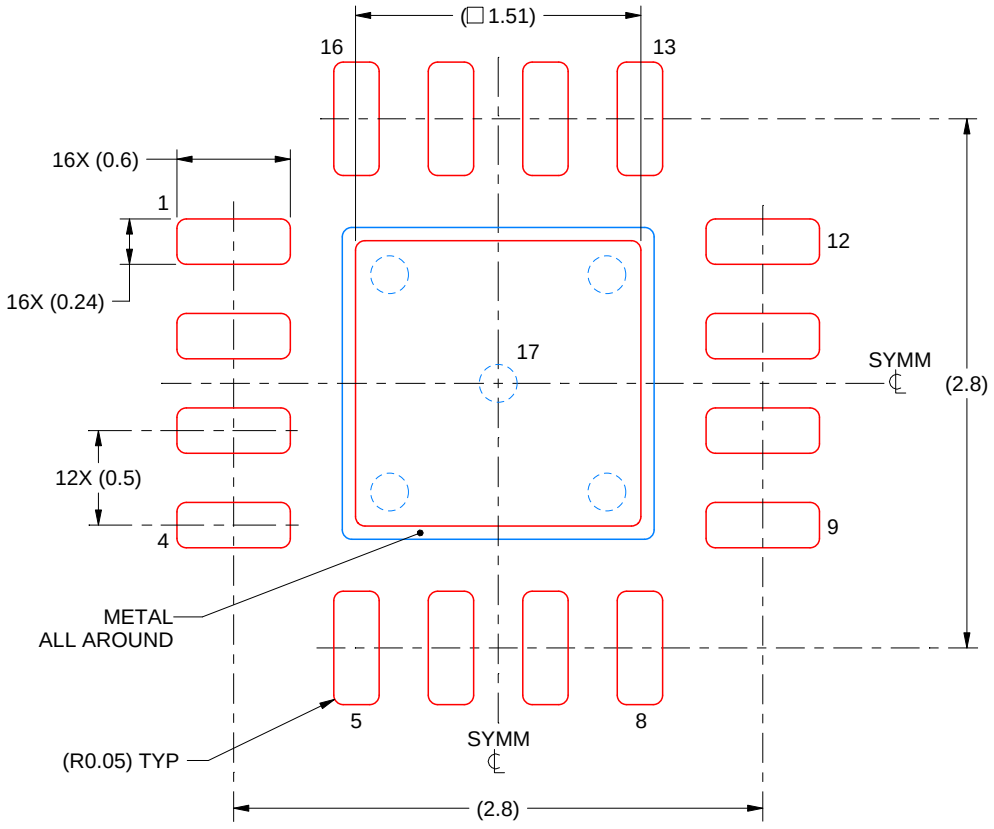


SOLDER MASK DETAILS

4219119/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219119/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265