TEXAS INSTRUMENTS

TPS544C25, TPS544B25

SLUSC81 – MAY 2015

TPS544x25 4.5-V to 18-V, 20-A and 30-A SWIFT™ Synchronous Buck Converters with PMBus™ and Frequency Synchronization

1 Features

- PMBus 1.2 Compliant Converters: 20 A and 30 A
- Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.5 V to 5.5 V
- 5 mm × 7 mm LQFN Package
- Single Thermal Pad
- Integrated 5.5-mΩ and 2.0-mΩ Stacked NexFET™ Power Stage
- 500-mV to 1500-mV Reference for Adapative Voltage Scaling (AVS) and Margining through PMBus
- 0.5% Reference Accuracy at 600 mV and Above
- Lossless Low-Side MOSFET Current Sensing
- Voltage Mode Control with Input Feed-Forward
- Differential Remote Sensing
- Monotonic Start-Up into Pre-Biased Output
- Output Voltage and Output Current Reporting
- External Temperature Monitoring with 2N3904 Transistor
- Programmable via the PMBus interface
  - VOUT_COMMAND and AVS VOUT Transition Rate
  - Overcurrent Protection with Thermal Compensation
  - UVLO, Soft-Start and Soft-Stop
  - PGOOD, OV, UV, OT Levels
  - Fault Responses
  - Turn-On and Turn-Off Delays
- Thermal Shutdown
- Pin Strapping for Switching Frequency: 200 kHz to 1 MHz
- Frequency Synchronization to an External Clock
- Footprint Compatible 20-A, 30-A Converters

2 Applications

- Test and Instrumentation
- Ethernet Switches, Optical Switches, Routers, Base Stations
- Servers
- Enterprise Storage SSD
- High-Density Power Solutions

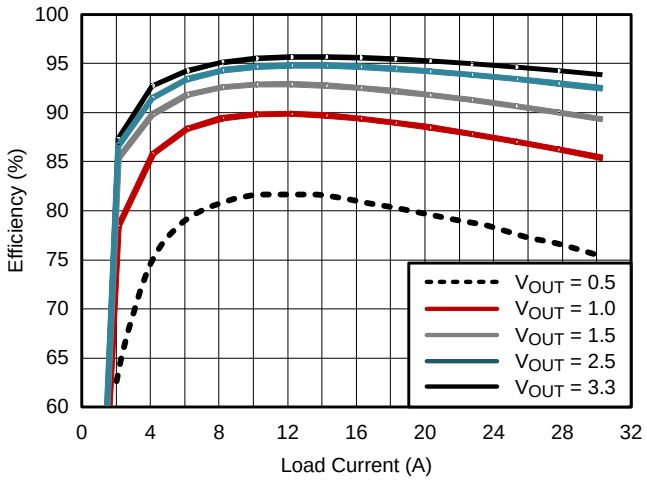
3 Description

The TPS544x25 devices are PMBus 1.2 Compliant, non-isolated DC-DC converters with integrated FETs, capable of high-frequency operation and 20-A or 30-A current output from a 5 mm × 7 mm package. High-frequency, low-loss switching, provided by an integrated NexFET™ power stage and optimized drivers, allows for very high-density power solutions. The PMBus interface enables the AVS through VOUT_COMMAND, flexible converter configuration, as well as key parameters monitoring including output voltage, current and an optional external temperature. Response to fault conditions can be set to either restart, latch-off or ignore depending on system requirements.

Device Information

DEVICE NAME	PACKAGE	BODY SIZE
TPS544B25RVFT	LQFN (40)	5.00 mm × 7.00 mm
TPS544C25RVFT	LQFN (40)	5.00 mm × 7.00 mm

Efficiency



V_{IN} = 12 V | No Snubber | L = 470 nH

f_{SW} = 500 kHz | R_{DCR} = 0.3mΩ | R_{BOOT} = 0 Ω

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4 Revision History

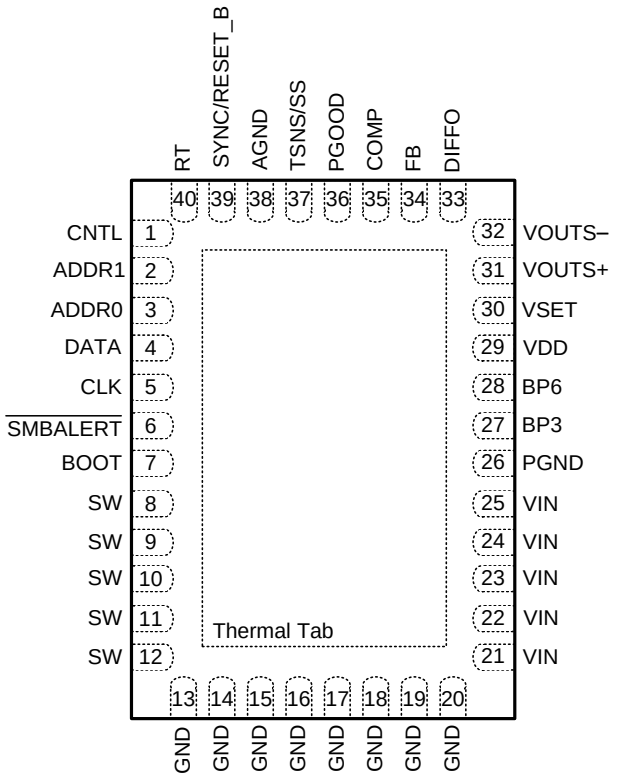
DATE	REVISION	NOTES
May 2015	*	Initial release.

5 Device Comparison Table

DEVICE NAME	CURRENT OPTION (A)
TPS544B25RVFR	20
TPS544B25RVFT	
TPS544C25RVFR	30
TPS544C25RVFT	

6 Pin Configuration and Functions

RVF Package
40-Pin LQFN
(Top View)



Pin Functions

NAME	NO.	DESCRIPTION
ADDR0	3	Sets low-order 3-bits of the PMBus address. Connect a resistor between this pin and AGND.
ADDR1	2	Sets high-order 3-bits of the PMBus address. Connect a resistor between this pin and AGND.
AGND	38	Analog ground return for controller device. Connect to GND at the thermal tab.
BP3	27	Output of the 3.3-V on-board regulator. This regulator powers the controller and should be bypassed with a minimum of 2.2 µF to AGND. BP3 is not designed to power external circuit.
BP6	28	Output of the 6.5-V on-board regulator. This regulator powers the driver stage of the controller and should be bypassed with a minimum of 2.2 µF to GND. TI recommends using an additional 100-nF typical bypass capacitor for reduce ripple on BP6.
BOOT	7	Bootstrap pin for the internal flying high-side driver. Connect a typical 100-nF capacitor from this pin to the SW pin.
CLK	5	PMBus CLK pin. See *Supported PMBus Commands* section.
CNTL	1	PMBus CNTL pin. See *Supported PMBus Commands* section. The CNTL pin has an internal pull-up and floats high when left floating.

Pin Functions (continued)

NAME	NO.	DESCRIPTION
COMP	35	Output of the error amplifier. Connect compensator network from this pin to the FB pin.
DATA	4	PMBus DATA pin. See *Supported PMBus Commands* section.
DIFFO	33	Output of the differential remote sense amplifier.
FB	34	Feedback pin for the control loop. Negative input of the error amplifier.
GND	13 14 15 16 17 18 19 20	Power stage ground return.
PGND	26	Power ground return for controller device. Connect to GND at the thermal tab.
PGOOD	36	Power good output. Open drain output that floats up when the device is operating and in regulation. Any fault condition causes this pin to pull low. Please refer to Table 6 for the possible sources to pull down PGOOD pin.
RT	40	Frequency-setting resistor. Connect a resistor from this pin to AGND to program the switching frequency. Do not leave this pin floating.
$\overline{\text{SMBALERT}}$	6	SMBus alert pin. See SMBus specification.
SW	8 9 10 11 12	Switched power output of the device. Connect the output averaging filter and bootstrap capacitor to this group of pins.
SYNC/RESET_B	39	For switching frequency synchronization or output voltage reset. The SYNC function allows synchronizing the oscillator to an external source that is either slower or faster than the nominal free running oscillator frequency. To use the SYNC function, VSET pin should be pulled up to BP3 or set the FORCE_SYNC bit in register MISC_CONFIG_OPTIONS (MFR_SPECIFIC_32) (F0h) if VSET function is used; if synchronization is not required, pull the SYNC pin to BP3. If the VSET pin is connected to AGND through a valid resistor to configure default output voltage, SYNC/RESET_B is configured as RESET_B function when FORCE_SYNC is not set. Then the logic low on the SYNC/RESET_B pin restores the output voltage to default value set by VSET without power cycling. When SYNC/RESET_B is configured as RESET_B function, there is an internal 200kΩ pull-up resistor to BP3.
TSNS/SS	37	External temperature sense signal input or alternatively used to set default soft-start time by connecting a resistor from this pin to AGND. Do not leave this pin floating. Disable TSNS by pulling TSNS to AGND and unsetting SS_DET_DIS in OPTIONS (MFR_SPECIFIC_21) (E5h) in applications where neither is needed.
VDD	29	Input power to the controller. Connect a low impedance bypass with a minimum of 1 µF to AGND. The VDD voltage is also used for input feed-forward. VIN and VDD must be the same potential for accurate short circuit protection.
VIN	21 22 23 24 25	Input power to the power stage. Low impedance bypassing of these pins to GND is critical.
VOUTS+	31	Load voltage sensing, positive side. This sensing provides remote sensing for the PMBus interface reporting and the voltage control loop.
VOUTS–	32	Load voltage sensing, negative or common side. This sensing provides remote sensing for the PMBus interface reporting and the voltage control loop.
VSET	30	Optionally configures default output voltage setting by connecting a resistor from this pin to AGND. See Set Default Output Voltage by VSET for details. If VSET is not used, pull this pin up to BP3. Do not leave this pin floating.
Thermal tab		Package thermal tab. Connect to GND. The thermal tab must have adequate solder coverage for proper operation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage range	VIN, VDD	–0.3	18	V
	VIN, VDD <2 ms transient	–0.3	19	
	VIN – SW (VIN to SW differential)	–0.3	25	
	VIN – SW (VIN to SW differential, <10 ns transient due to SW ringing)	–5	25	
	BOOT	–0.3	37	
	BOOT – SW (BOOT to SW differential)	–0.3	7	
	BOOT – SW (BOOT to SW differential, <10 ns transient)	–0.3	7.5	
	CLK, DATA	–0.3	5.5	
	VSET, ADDR0, ADDR1, TSNS/SS	–0.3	3.6	
	FB, SYNC/RESET_B, CNTL, VOUTS–, VOUTS+, RT	–0.3	7	
Output voltage range	SW	–1	25	V
	SW <100 ns transient	–5	25	
	BP6, COMP, DIFFO, PGOOD	–0.3	7	
	$\overline{\text{SMBALERT}}$	–0.3	5.5	
	BP3	–0.3	3.6	
Operating junction temperature range, T_J		–40	150	°C
Storage temperature range, T_{stg}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	Controller input voltage	4.5	12	18	V
V_{IN}	Power stage input voltage	4.5	12	18	V
T_J	Junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS544x25 PQFN (RVF) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	4.2	
ψ_{JT}	Junction-to-top characterization parameter	1.4	
ψ_{JB}	Junction-to-board characterization parameter	4.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{VIN} = V_{VDD}= 12 V, R_{RT} = 40.2 kΩ; zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VDD}	Input supply voltage range		4.5		18	V
V_{VIN}	Power stage voltage range		4.5		18	
I_{VDD}	Input operating current	Not switching		9.5	12	mA
UVLO						
VIN_ON	Input turn on voltage	Factory default setting		4.5		V
		Programmable range, 15 different settings	4.25		7.75	
		Accuracy	–5%		5%	
VIN_OFF	Input turn off voltage	Factory default setting		4		V
		Programmable range, 15 different settings	4		7.5	
		Accuracy	–5%		5%	
ERROR AMPLIFIER AND FEEDBACK VOLTAGE						
V_{FB}	Feedback pin voltage	Default setting	940.5	950	959.5	mV
		Setpoint range(1)	0.5		1.5	V
$V_{FB(ACC)}$	Feedback pin voltage accuracy	V_{FB} = 600 mV, 0°C ≤ T_J ≤ 85°C(2)	–0.5%		0.5%	%
		0.6 V ≤ V_{FB} ≤ 1.5 V(1)	–1.0%		1.0%	
		0.5 V ≤ V_{FB} < 0.6 V(1)	–1.5%		1.5%	
A_{OL}	Open-loop gain(1)		80			dB
G_{BWP}	Gain bandwidth product(1)		15			MHz
I_{FB}	FB pin input bias current	V_{FB} = 0.95 V	–75		75	nA
I_{COMP}	Sourcing	V_{FB} = 0 V	1			mA
	Sinking	V_{FB} = 1.2 V	1			
VSET						
I_{Vset}	VSET pin current		9.5	10.5	12	µA
V_{Vset}	Initial VOUT setting	R_{Vset} = 34.8 kΩ		950		mV
$V_{Vset(dis)}$	VSET disable threshold		2.41			V
OSCILLATOR						
F_{SW}	Adjustment range(2)		200		1000	kHz
	Switching frequency	R_{RT} = 40.2 kΩ	425	500	575	kHz
V_{RMP}	Ramp peak-to-peak(1)		V_{VDD}/9.3	V_{VDD}/8.5	V_{VDD}/7.6	V
V_{VLY}	Valley voltage(1)			0.75		
SYNCHRONIZATION						
$V_{IH(sync)}$	High-level input voltage		2.0			V
$V_{IL(sync)}$	Low-level input voltage				0.80	
$T_{pw(sync)}$	Sync input minimum pulse width				100	ns
f_{SYNC}	Synchronization frequency		200		1200	kHz
Δf_{SYNC}	SYNC pin frequency range from free running frequency(1)		-20%		20%	
RESET_B						
$V_{IH(reset)}$	High-level input voltage(1)	3.3-V and 5-V logic	2.1			V
		1.8-V logic (factory default)	1.2			
$V_{IL(reset)}$	Low-level input voltage	3.3-V and 5-V logic			0.8	
		1.8-V logic (factory default)			0.5	
$t_{PW(reset)}$	Minimum RESET_B pulse width	R_{VSET} = 34.8 kΩ	200			ns
$V_{vout\_command(reset)}$	Output voltage after reset triggered	R_{VSET} = 34.8 kΩ		950		mV

(1) Specified by design. Not production tested.
(2) The parameter covers 4.5 V to 18 V of VDD.

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{VIN} = V_{VDD}= 12 V, R_{RT} = 40.2 kΩ; zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BP6 REGULATOR						
V_{BP6}	Regulator output voltage	I_{BP6} = 10 mA	5.85	6.4	6.9	V
$V_{BP6(do)}$	Regulator dropout voltage	V_{VIN} – V_{BP6}, V_{VDD} = 4.5 V, I_{BP6} = 25 mA	50	200	400	mV
I_{BP6SC}	Regulator short-circuit current(1)	V_{VDD} = 12 V		150		mA
V_{BP6UV}	Regulator UVLO voltage(1)			3.73		V
$V_{BP6UV(hyst)}$	Regulator UVLO voltage hysteresis(1)			320		mV
BOOTSTRAP						
$V_{BOOT(drop)}$	Bootstrap voltage drop	I_{BOOT} = 5 mA			125	mV
BP3 REGULATOR						
V_{BP3}	3-V regulator output voltage	V_{VDD} ≥ 4.5 V, I_{BP3} = 5 mA	3.0	3.2	3.4	V
I_{BP3SC}	3-V regulator short-circuit current(1)			35		mA
PWM						
$t_{ON(min)}$	Minimum controllable pulse width(1)				100	ns
SOFT-START						
TON_RISE	Soft-start time	Factory default setting		5		ms
		Programmable range, 16 discrete settings(1)(3)	0		100	
		Accuracy, TON_RISE = 1 ms	-10		10	%
TON_MAX_FAULT_LIMIT	Upper limit on the time to power up the output	Factory default setting		100		ms
		Programmable range, 16 discrete settings(1)(4)	0		100	
		Accuracy(1)	–10		10	%
TON_DELAY	Turn-on delay	Factory default setting		0		ms
		Programmable range, 16 discrete settings(1)	0		100	
		Accuracy(1)	–10		10	%
SOFT-STOP						
TOFF_FALL	Soft-stop time	Factory default setting(5)		0		ms
		Programmable range, 16 discrete settings(1)(5)	0		100	
		Accuracy, TOFF_FALL = 1 ms	–10		10	%
TOFF_DELAY	Turn-off delay	Factory default setting		0		ms
		Programmable range, 16 discrete settings(1)	0		100	
		Accuracy(1)	–10		10	%
SS PIN FOR INITIAL SOFT-START PROGRAMMING						
I_{SS}	SS pin current		9.5	10.5	12	µA
$V_{SS(ivlow)}$	SS pin invalid low voltage				0.03	V
$V_{SS(ivhigh)}$	SS pin invalid high voltage		2.40			

(3) The setting of TON_RISE of 0 ms means the unit to bring its output voltage to the programmed regulation value as quickly as possible, which results in an effective TON_RISE time of 1 ms (fastest time supported).
(4) The setting of TON_MAX_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT of 0 means disabling TON_MAX_FAULT and VOUT_UV_FAULT response and reporting, respectively.
(5) The setting of TOFF_FALL of 0 ms means the unit to bring its output voltage down to 0 as quickly as possible, which results in an effective TOFF_FALL time of 1 ms (fastest time supported).

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{VIN} = V_{VDD}= 12 V, R_{RT} = 40.2 kΩ; zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REMOTE SENSE AMPLIFIER							
$V_{DIFFO(err)}$	Error voltage from DIFFO to (V_{OUTS+} – $V_{OUTS–}$)	(V_{OUTS+} – $V_{OUTS–}$) = 0.6 V		–5		5	mV
		(V_{OUTS+} – $V_{OUTS–}$) = 1.2 V		–7		7	
		(V_{OUTS+} – $V_{OUTS–}$) = 3.0 V		–15		15	
A_{RSA}	Differential gain			0.995		1.005	V/V
BW_{RSA}	Closed-loop bandwidth(1)			2			MHz
$V_{DIFFO(max)}$	Maximum DIFFO output voltage					V_{BP6}–0.2	V
I_{DIFFO}	DIFFO sourcing current			1			mA
	DIFFO sinking current			1			
POWER STAGE							
R_{HS}	High-side power device on-resistance	V_{VDD} ≥ 12 V, T_J = 25°C			5.5		mΩ
R_{LS}	Low-side power device on-resistance	V_{VDD} ≥ 12 V, (BOOT - SW) = 6.5 V, T_J = 25°C			2.0		
CURRENT SENSE AMPLIFIER							
$t_{LS(minCS)}$	Minimum LDRV pulse width for valid overcurrent and current mornitoring(1)				400		ns
LOW-SIDE CURRENT LIMIT PROTECTION							
$t_{OFF(OC)}$	Off time between restart attempts(1)				7 × TON_RISE		ms
IOUT_OC_FAULT_LIMIT	Output current overcurrent fault threshold	Factory default setting	TPS544C25		36		A
		Programmable range		5		40	
		Factory default setting	TPS544B25		24		
		Programmable range		5		36	
IOUT_OC_WARN_LIMIT	Output current overcurrent warning threshold	Factory default setting	TPS544C25		34		
		Programmable range		4		39.5	
		Factory default setting	TPS544B25		22		
		Programmable range		4		35.5	
$I_{OC(acc)}$	Output current overcurrent fault accuracy	I_{OUT} ≥ 20 A		–10%		+10%	
	Output current overcurrent warning accuracy	I_{OUT} ≥ 20 A(1)		–10%		+10%	
HIGH-SIDE SHORT CIRCUIT PROTECTION							
I_{HSOC}	High-side short-circuit protection peak current threshold		TPS544C25	40		75	A
			TPS544B25	33		66	
POWER GOOD (PGOOD) AND OVERVOLTAGE/UNDERVOLTAGE WARNING							
$V_{PG(hyst)}$	PGOOD and over/under votlage warning threshold hysteresis at DIFFO pin	VOUT_SCALE_LOOP = 1.0		15		75	mV
R_{PGOOD}	PGOOD pull-down resistance	V_{DIFFO} = 0 V, I_{PGOOD} = 5 mA		30	45	60	Ω
$I_{PGOOD(lk)}$	PGOOD pin leakage current	V_{PGOOD} = 5 V				15	µA
VOUT_OV_WARN_LIMIT	Overvoltage warning threshold at DIFFO pin	VOUT_SCALE_LOOP = 1.0, factory default setting		1165	1201	1237	mV
		VOUT_SCALE_LOOP = 1.0, programmable range(1)		527		1797	
VOUT_UV_WARN_LIMIT	Undervoltage warning threshold at DIFFO pin	VOUT_SCALE_LOOP = 1.0, factory default setting		600	631	650	
		VOUT_SCALE_LOOP = 1.0, programmable range(1)		350		1428	
$V_{UVOV(warnhyst)}$	Over/under votlage warning threshold hysteresis at DIFFO pin	VOUT_SCALE_LOOP = 1.0(1)		15		75	

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{VIN} = V_{VDD}= 12 V, R_{RT} = 40.2 kΩ; zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE FAULT PROTECTION						
VOUT_OV_FAULT_LIMIT	Overvoltage fault threshold at DIFFO pin	VOUT_SCALE_LOOP = 1.0, factory default setting	1243	1281	1330	mV
		VOUT_SCALE_LOOP = 1.0, programmable range(1)	529		1799	
VOUT_UV_FAULT_LIMIT	Undervoltage fault threshold at DIFFO pin	VOUT_SCALE_LOOP = 1.0, factory default setting	550	594	610	
		VOUT_SCALE_LOOP = 1.0, programmable range(1)(4)	346		1426	
$V_{UVOV(flthyst)}$	Over/under votlage fault threshold hysteresis at DIFFO pin	VOUT_SCALE_LOOP = 1.0(1)	15		75	
OUTPUT VOLTAGE TRIMMING						
VOUT_TRANSITION_RATE	Output voltage transition rate	Factory default setting		1.0		mV/µs
		Programmable range, 8 discrete settings	0.067		1.5	
		Accuracy	–10%		10%	
VOUT_SCALE_LOOP	Feedback loop scaling factor	Factory default setting		1		
		Programmable range, 3 discrete settings	0.25		1	
VOUT_COMMAND	Output voltage programmable register value, multiply by 2^{-9} to get output voltage	Factor default setting		486		
		VOUT_SCALE_LOOP = 1.0, programmable range(1)	256		768	
		VOUT_SCALE_LOOP = 0.5, programmable range(1)	512		1536	
		VOUT_SCALE_LOOP = 0.25, programmable range(1)	1024		3072	
TEMPERATURE SENSE AND THERMAL SHUTDOWN						
T_{SD}	Junction thermal shutdown temperature(1)		135	145	155	°C
T_{HYST}	Junction thermal shutdown hysteresis(1)		15	20	25	
V_{TSNS}	Voltage range on TSNS/SS pin(1)		0		1.00	V
OT_FAULT_LIMIT	External overtemperature fault limit(1)	Factory default setting		125		°C
		Programmable range	120		165	
OT_WARN_LIMIT	External overtemperature warning limit(1)	Factory default setting		100		
		Programmable range	100		140	
$T_{OT(hys)}$	External overtemperature fault, warning hysteresis(1)		15	20	25	
MEASUREMENT SYSTEM						
$M_{VOUT(rng)}$	Output voltage measurement range		0.5		5.8	V
$M_{VOUT(acc)}$	Output voltage measurement accuracy		–2.0%		2.0%	
$M_{VOUT(lsb)}$	Output voltage measurement bit resolution(1)			1.953		mV
$M_{IOUT(rng)}$	Output current measurement range		0		40	A
$M_{IOUT(acc)}$	Output current measurement accuracy	I_{OUT} ≥ 20 A	–15%		15%	
		3 A ≤ I_{OUT} < 20 A(1)	–3		3	A
$M_{IOUT(lsb)}$	Output current measurement bit resolution(1)			62.5		mA
$M_{TSNS(rng)}$	External temperature sense range(1)		–40		165	°C
$M_{TSNS(acc)}$	External temperature sense accuracy(1)	-40°C ≤ $T_{J(sensor)}$ ≤ 165°C	–5		5	
$M_{TSNS(lsb)}$	External temperature sense bit resolution(1)			1		

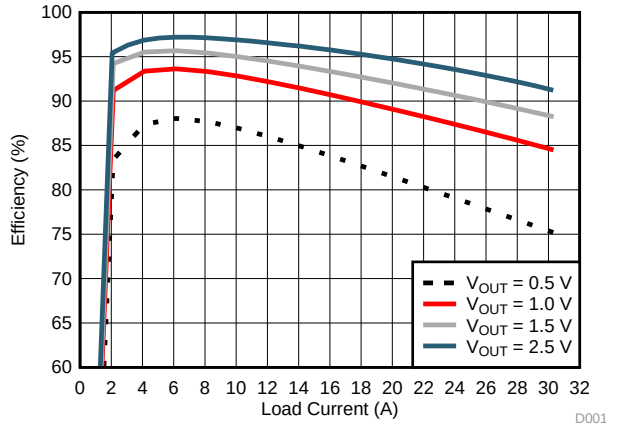
Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{VIN} = V_{VDD}= 12 V, R_{RT} = 40.2 kΩ; zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PMBus INTERFACE ADDRESSING						
I_{ADD}	Address pin bias current		9.5	10.5	12	µA
$V_{ADD(ivlow)}$	Address pin illegal low voltage				0.05	V
$V_{ADD(ivhigh)}$	Address pin illegal high voltage		2.40			
PMBus™ INTERFACE						
V_{IH}	Input high voltage, CLK, DATA, CNTL	3.3-V/5-V logic	2.1			V
		1.8-V logic (factory default)	1.2			
V_{IL}	Input low voltage, CLK, DATA, CNTL	3.3-V/5-V logic			0.8	V
		1.8-V logic (factory default)			0.5	
I_{IH}	Input high level current, CLK, DATA		-10		10	µA
I_{IL}	Input low level current, CLK, DATA		-10		10	µA
I_{CNTL}	CNTL pin pull-up current		5		10	µA
V_{OL}	Output low level voltage, DATA, $\overline{\text{SMBALERT}}$	V_{DD} > 4.5 V, input current to DATA, $\overline{\text{SMBALERT}}$ = 4mA			0.4	V
I_{OH}	Output high level open drain leakage current, DATA, $\overline{\text{SMBALERT}}$	Voltage on DATA, $\overline{\text{SMBALERT}}$ = 5.5V	-10		10	µA
I_{OL}	Output low level open drain leakage current, DATA, $\overline{\text{SMBALERT}}$	Voltage on DATA, $\overline{\text{SMBALERT}}$ = 0.4V	4.0			mA
I_{PMB}	PMBus operating frequency range	Slave mode	10		400	kHz

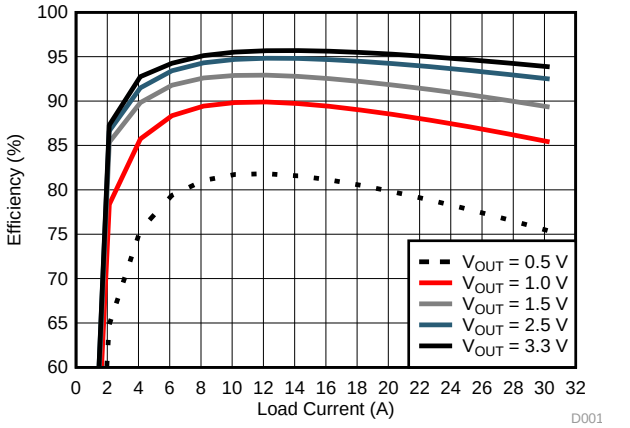
7.6 Typical Characteristics

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 40.2 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.



V_{IN} = 5 V | L = 470 nH | No Snubber
f_{SW} = 500 kHz | R_{DCR} = 0.3 mΩ | R_{BOOT} = 0 Ω

Figure 1. Efficiency vs. Output Current



V_{IN} = 12 V | L = 470 nH | No Snubber
f_{SW} = 500 kHz | R_{DCR} = 0.3 mΩ | R_{BOOT} = 0 Ω

Figure 2. Efficiency vs. Output Current

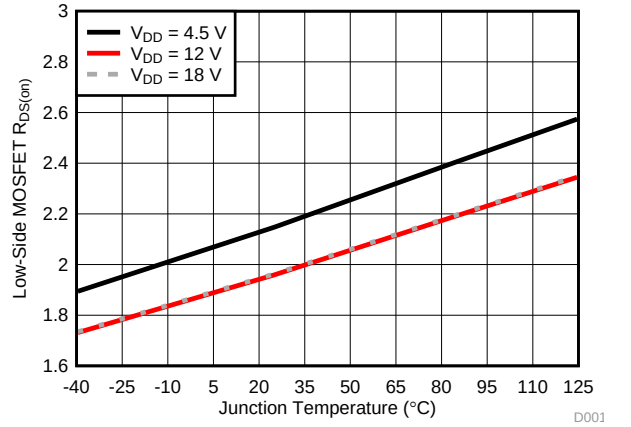


Figure 3. Low-Side MOSFET On-Resistance ($R_{DS(on)}$) vs. Junction Temperature

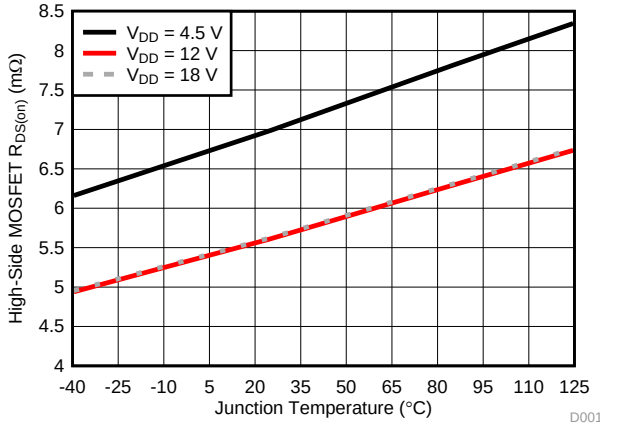
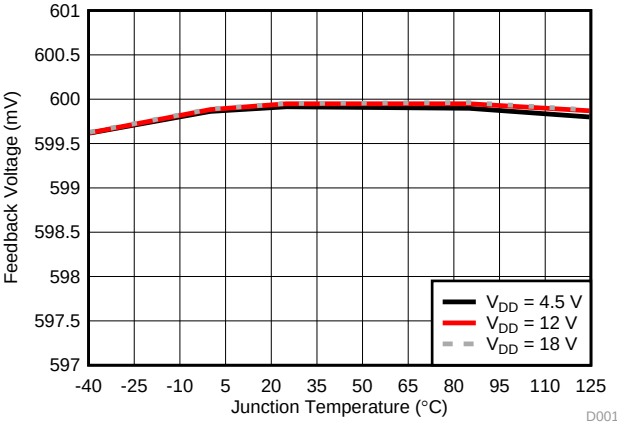
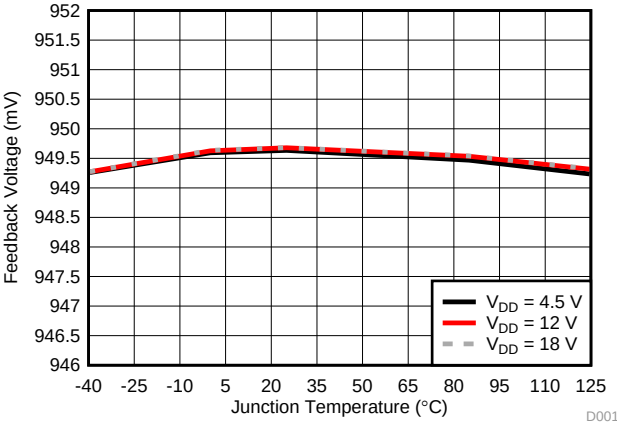


Figure 4. High-Side MOSFET On-Resistance ($R_{DS(on)}$) vs. Junction Temperature



V_{FB} = 600 mV

Figure 5. Feedback Voltage vs. Junction Temperature



V_{FB} = 950 mV

Figure 6. Feedback Voltage vs. Junction Temperature

Typical Characteristics (continued)

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 40.2 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.

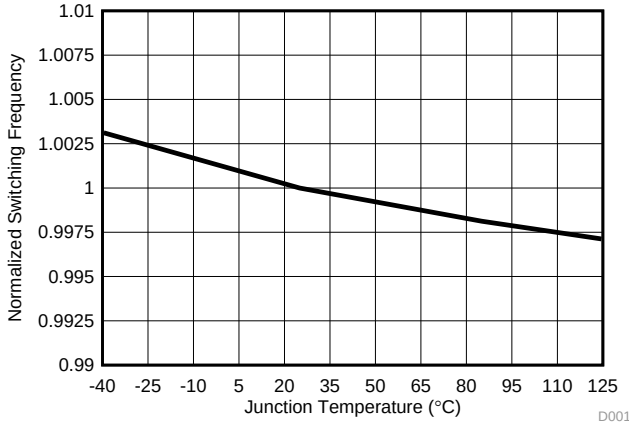


Figure 7. Normalized Switching Frequency vs. Junction Temperature

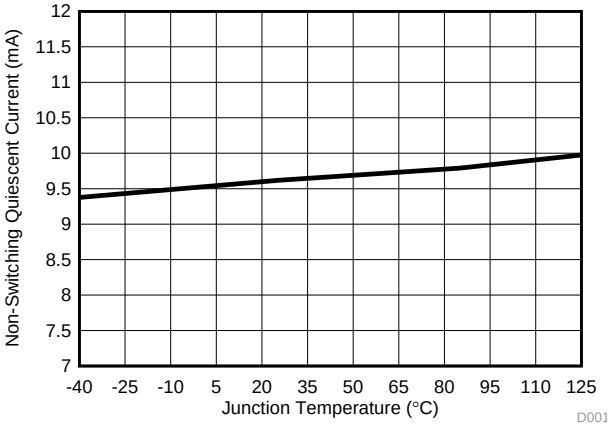
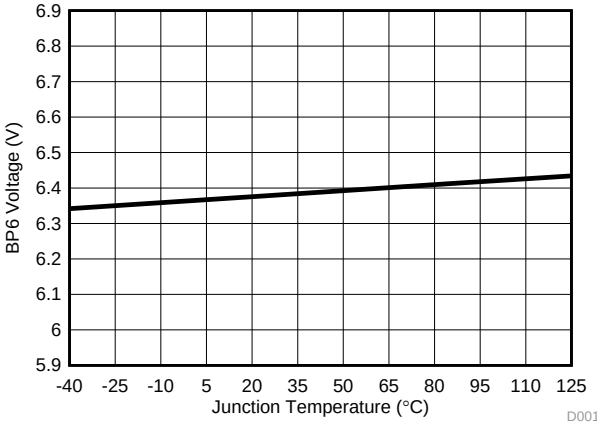
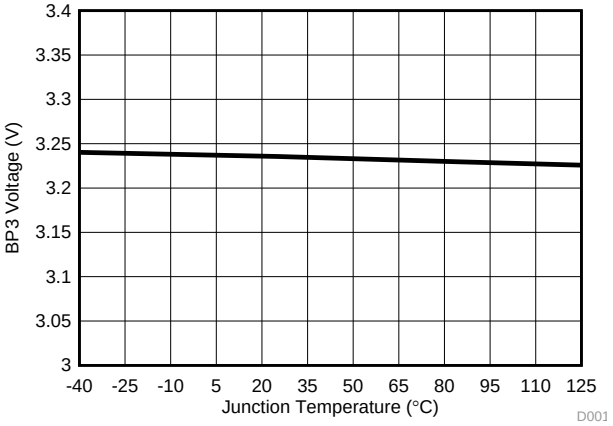


Figure 8. Non-Switching Input Current (I_{VDD}) vs. Junction Temperature



I_{BP6} = 10 mA V_{VIN} = V_{VDD}= 12 V

Figure 9. BP6 Voltage vs. Junction Temperature



I_{BP3} = 5 mA V_{VIN} = V_{VDD}= 12 V

Figure 10. BP3 Voltage vs. Junction Temperature

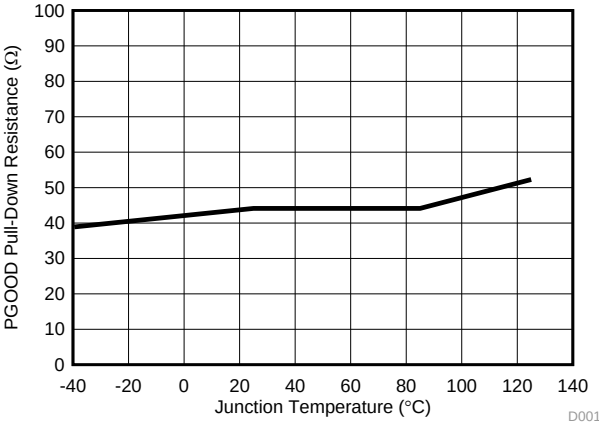
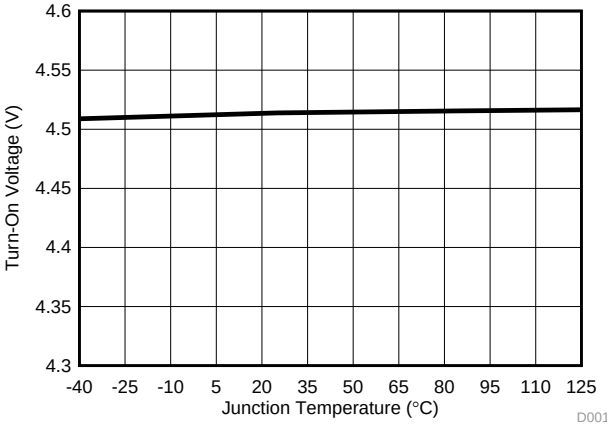


Figure 11. PGOOD Pull-Down Resistance vs. Junction Temperature

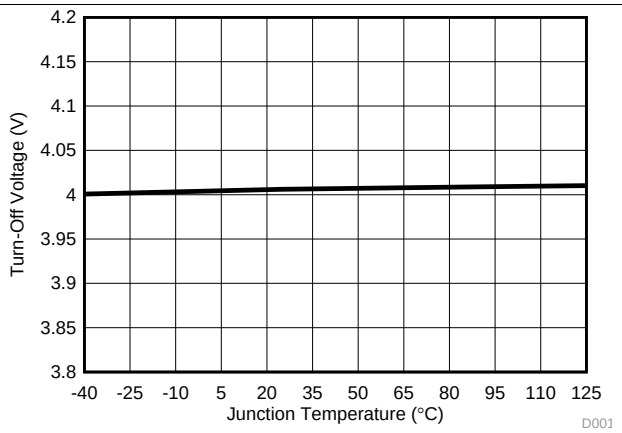


VIN_ON = 4.5 V

Figure 12. Turn-On Voltage vs. Junction Temperature

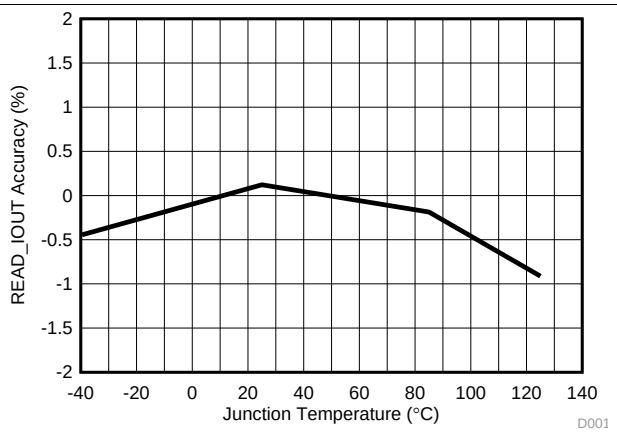
Typical Characteristics (continued)

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 40.2 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.



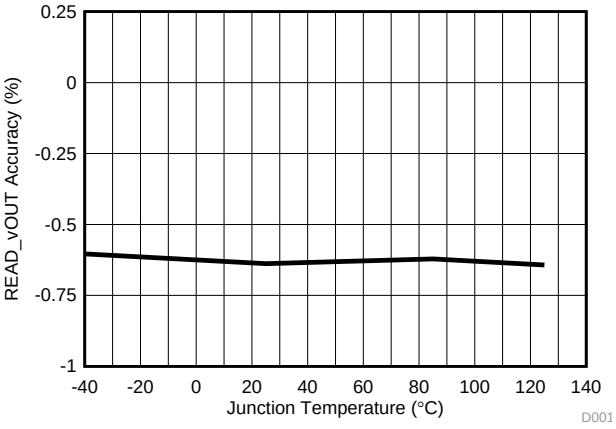
VIN_OFF = 4.0 V

Figure 13. Turn-Off Voltage vs. Junction Temperature



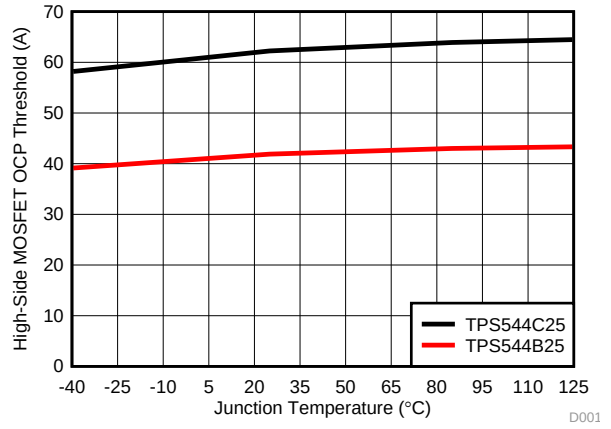
I_{OUT} = 20 A V_{VIN} = V_{VDD}= 12 V

Figure 14. READ_IOUT Accuracy vs. Junction Temperature



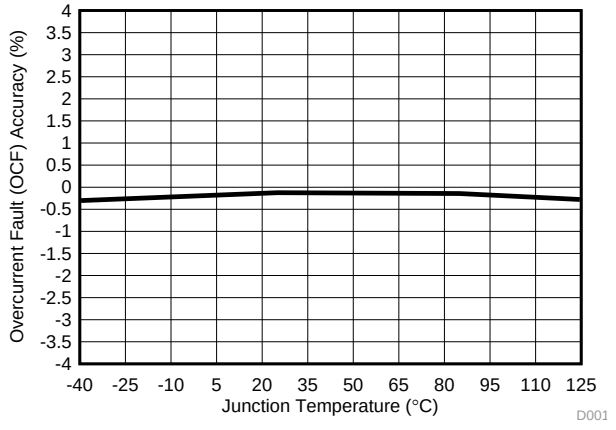
V_{VIN} = V_{VDD}= 12 V

Figure 15. READ_VOUT Accuracy vs. Junction Temperature



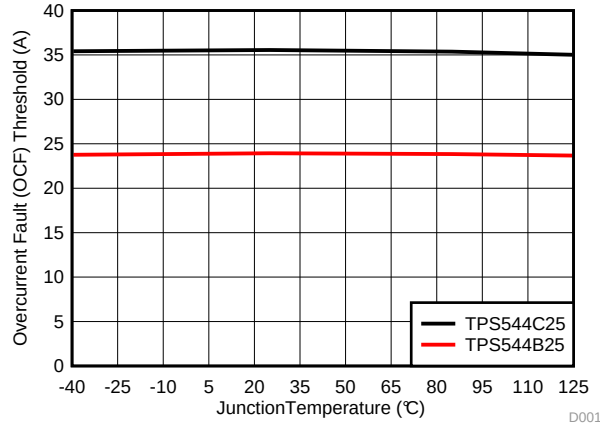
BOOT - SW = 6.5 V V_{VIN} = V_{VDD}= 12 V

Figure 16. High-Side Overcurrent Protection vs. Junction Temperature



OCF = 20 A V_{VIN} = V_{VDD}= 12 V

Figure 17. Overcurrent Fault Protection (OCF) Accuracy vs. Junction Temperature



V_{VIN} = V_{VDD}= 12 V OCF = 36 A (TPS544C25) OCF = 24 A (TPS544B25)

Figure 18. Overcurrent Fault Protection (OCF) vs. Junction Temperature

Typical Characteristics (continued)

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 40.2 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.

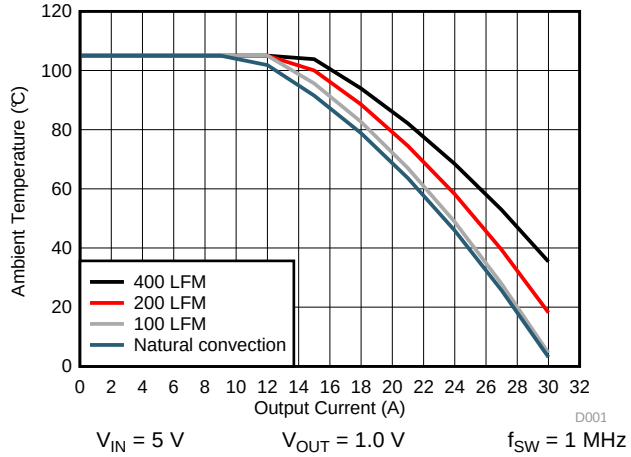


Figure 19. Safe Operating Area

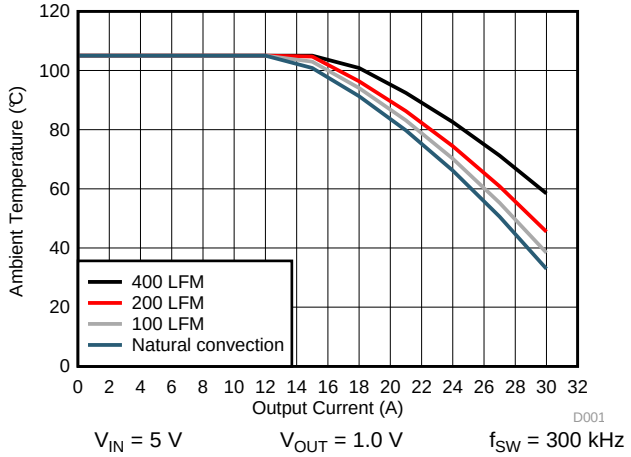


Figure 20. Safe Operating Area

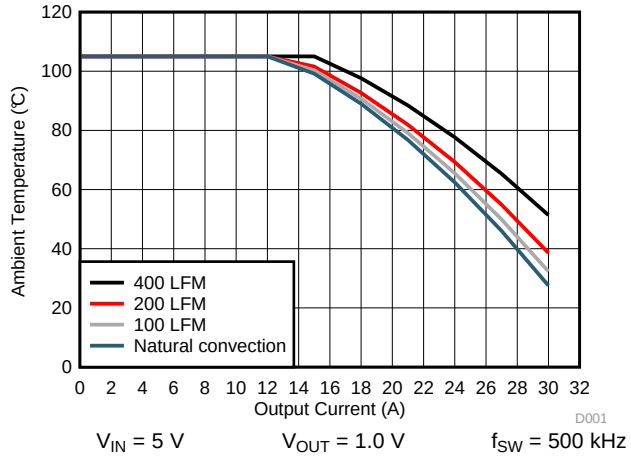


Figure 21. Safe Operating Area

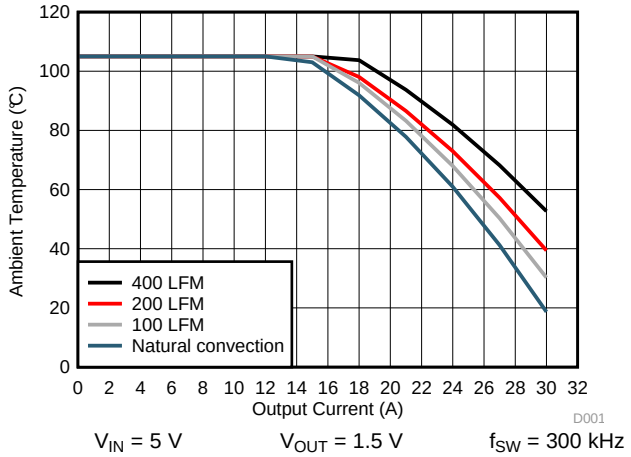


Figure 22. Safe Operating Area

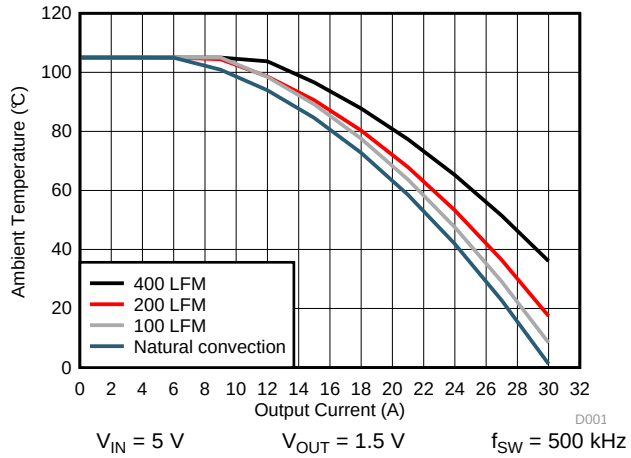


Figure 23. Safe Operating Area

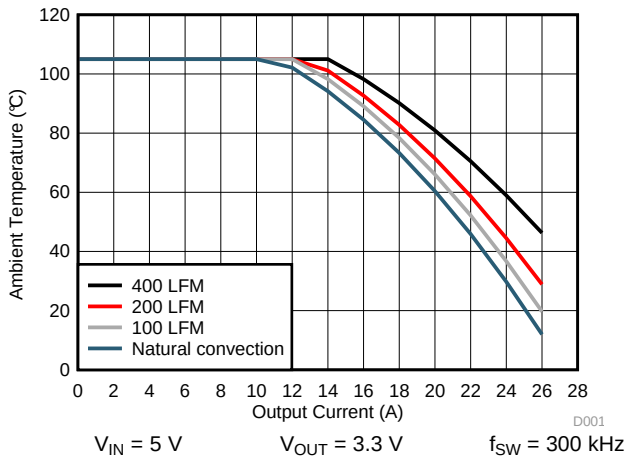
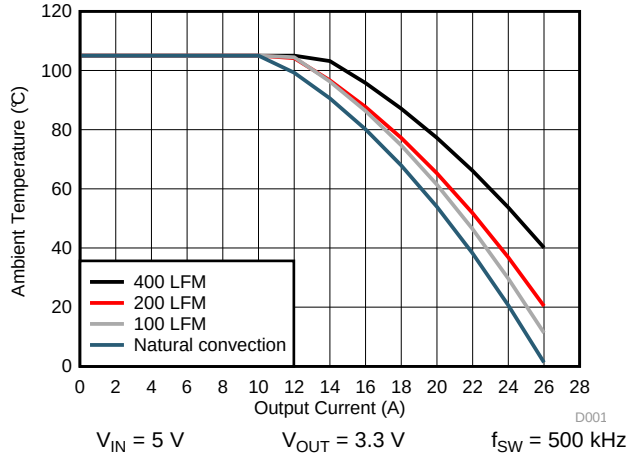


Figure 24. Safe Operating Area

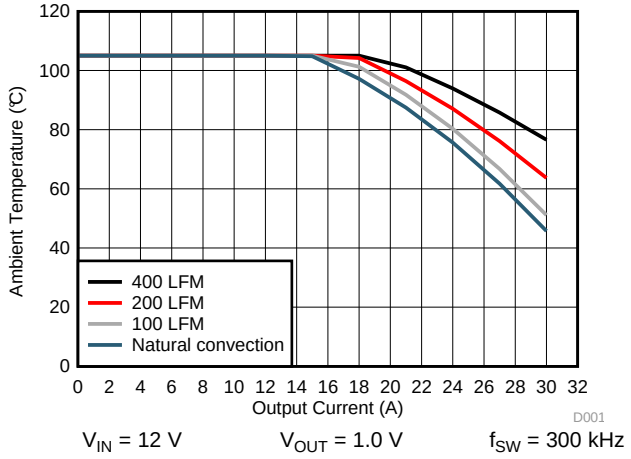
Typical Characteristics (continued)

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 40.2 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.



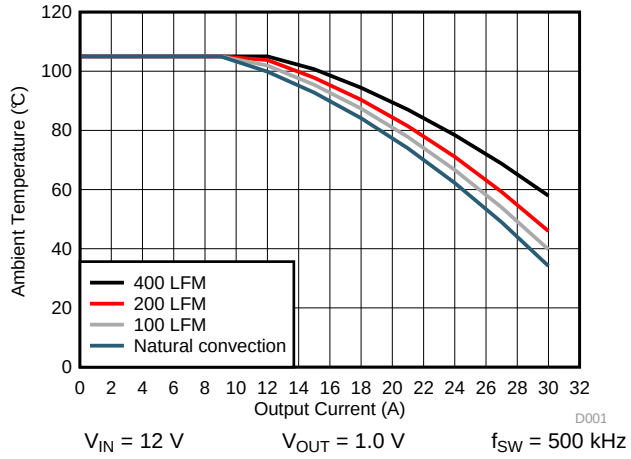
V_{IN} = 5 V V_{OUT} = 3.3 V f_{SW} = 500 kHz

Figure 25. Safe Operating Area



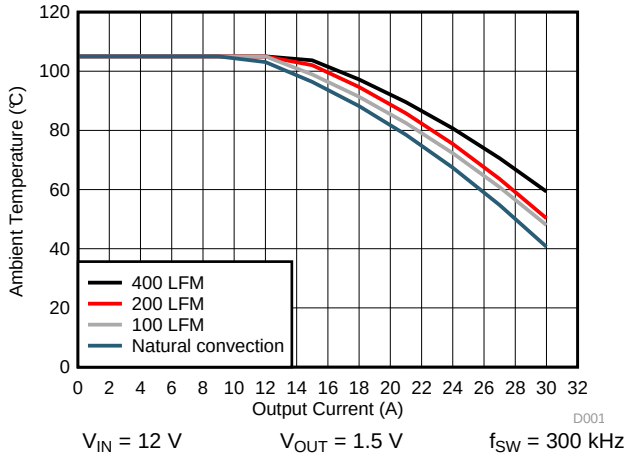
V_{IN} = 12 V V_{OUT} = 1.0 V f_{SW} = 300 kHz

Figure 26. Safe Operating Area



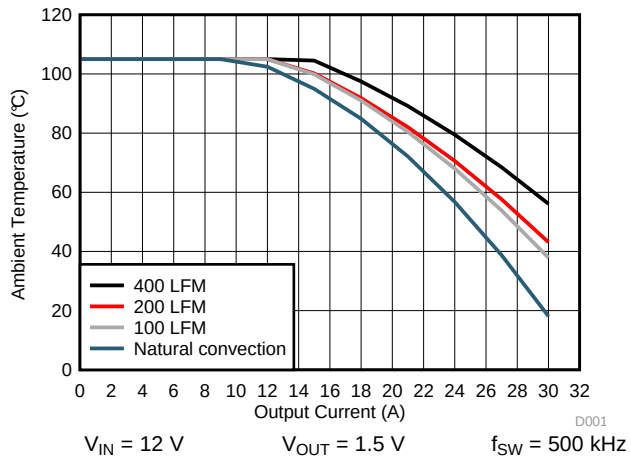
V_{IN} = 12 V V_{OUT} = 1.0 V f_{SW} = 500 kHz

Figure 27. Safe Operating Area



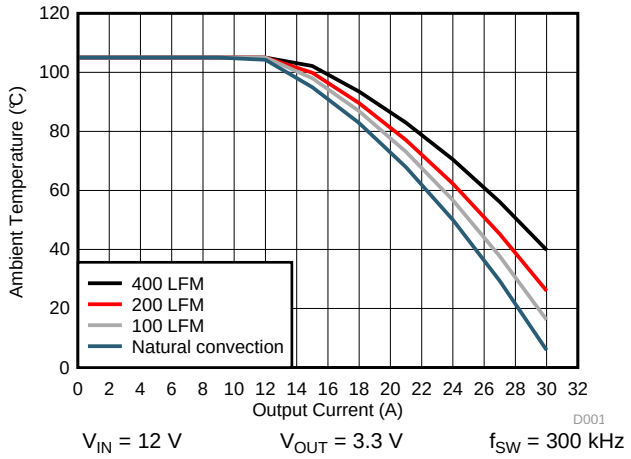
V_{IN} = 12 V V_{OUT} = 1.5 V f_{SW} = 300 kHz

Figure 28. Safe Operating Area



V_{IN} = 12 V V_{OUT} = 1.5 V f_{SW} = 500 kHz

Figure 29. Safe Operating Area

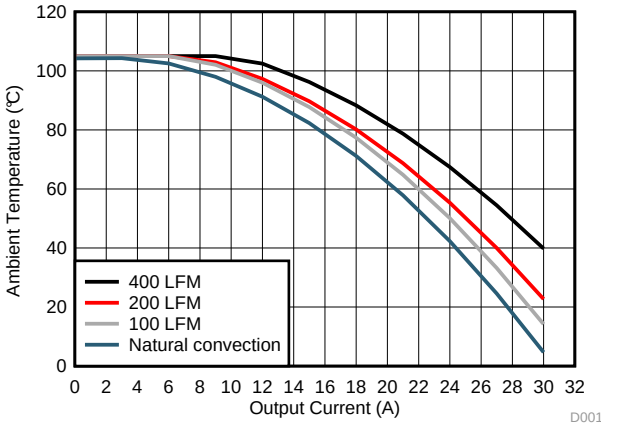


V_{IN} = 12 V V_{OUT} = 3.3 V f_{SW} = 300 kHz

Figure 30. Safe Operating Area

Typical Characteristics (continued)

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 40.2 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.



V_{IN} = 12 V V_{OUT} = 3.3 V f_{SW} = 500 kHz

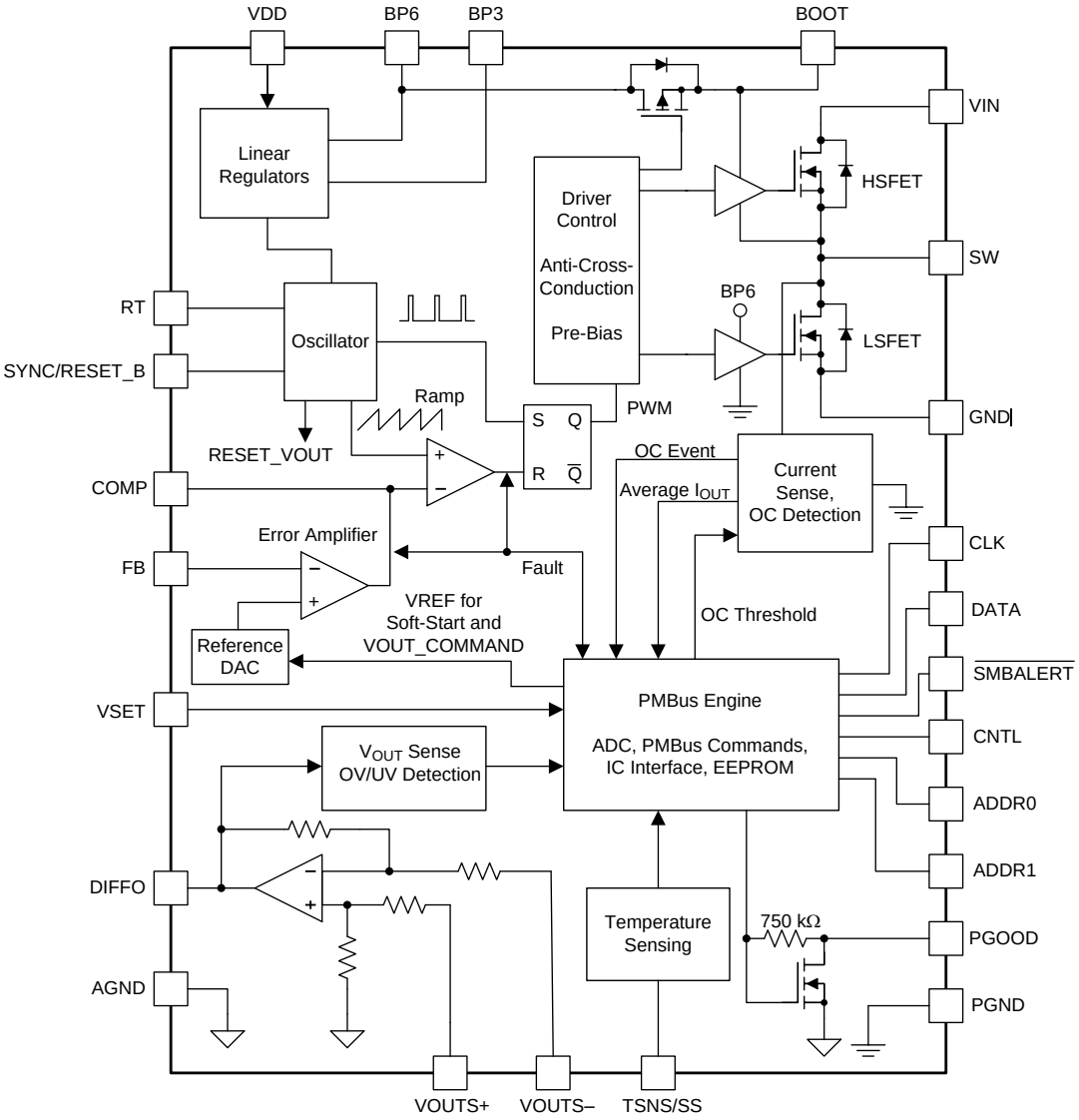
Figure 31. Safe Operating Area

8 Detailed Description

8.1 Overview

The TPS544x25 devices are PMBus 1.2 compliant 20-A and 30-A, high-performance, synchronous buck converters with two integrated N-channel NexFET™ power MOSFETs, enabling high power density and minimal PCB area. These devices implement the industry standard fixed switching frequency, voltage-mode control with input feed-forward topology that responds instantly to input voltage change. These devices can be synchronized to the external clock to eliminate beat noise and reduce EMI/EMC. The integrated PMBus interface capability provides precise current, voltage and on-board temperature monitoring, as well as many user-programmable configuration options including Adaptive Voltage Scaling (AVS) through standard VOUT_COMMAND.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Linear Regulators BP3 and BP6

The TPS544x25 devices have two on-board linear regulators to provide suitable power for the internal circuitry of the device. Externally bypass pins BP3 and BP6 for the converter to function properly. BP3 requires a minimum of 2.2 µF of capacitance connected to AGND. BP6 requires a minimum 2.2 µF of capacitance connected to GND. TI recommends using a 4.7-µF capacitor and an additional 100-nF to reduce the ripple on the BP6 pin.

NOTE

Place bypass capacitors as close as possible to the device pins, with a minimum return loop back to ground and the return loop should be kept away from fast switching voltage and main current path. Refer to Layout for details. Poor bypassing can degrade the performance of the regulator.

The use of the internal regulators to power other circuits are not recommended because the loads placed on the regulators might adversely affect operation of the controller.

8.3.2 Input Undervoltage Lockout (UVLO)

The TPS544x25 devices provide flexible user adjustment of the undervoltage lockout threshold and hysteresis. Two PMBus commands, VIN_ON (35h) and VIN_OFF (36h) allow the user to set these input voltage turn-on and turn-off thresholds independently, with a minimum of 4-V turn-off to a maximum 7.75-V turn-on. See the command descriptions for more details.

8.3.3 Turn-On and Turn-Off Delay and Sequencing

The TPS544x25 devices provide many sequencing options. Using the ON_OFF_CONFIG command, the device can be configured to start up whenever the input voltage is above the undervoltage lockout (UVLO) threshold, or to additionally require a signal on the CNTL pin and/or receive an update to the OPERATION command via the PMBus interface . When the gating signal as specified by ON_OFF_CONFIG is asserted, a programmable turn-on delay can be set with TON_DELAY to delay the start of regulation. Similarly, a programmable turn-off delay can be set with TOFF_DELAY to delay the stop of regulation once the gating signal is de-asserted. Delay times are specified in ms, from 0 to 100 ms.

Figure 32 shows control of the start-up and shutdown operations of the device, when the device is configured to respond to both CNTL and the OPERATION command. The device can also be configured to use either the CNTL signal, or the OPERATION command independently, or convert power whenever sufficient input voltage is present.

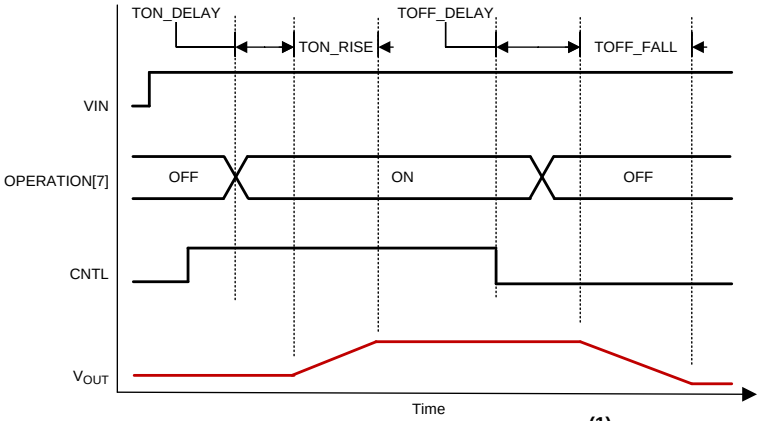


Figure 32. Turn-On Controlled By Both Operation(1) and Control (1)

8.3.4 Voltage Reference

A reference DAC (digital-to-analog converter) with 500 mV to 1500 mV range and 2^{-9} V (1.953 mV) resolution connects to the non-inverting input of the error amplifier. The tight tolerance on the reference voltage allows the user to design power supply with very high DC accuracy.

(1) Bit 7 of OPERATION is used to control power conversion.

Feature Description (continued)

8.3.5 Differential Remote Sense

The TPS544x25 devices implement a differential remote sense amplifier to provide excellent load regulation by cancelling IR-drop in high current applications. The VOUTS+ and VOUTS– pins should be kelvin-connected to the output capacitor bank directly at the load, and routed back to the device as a tightly coupled differential pair. Ensure that these traces are isolated from fast switching signals and high current paths on the final PCB layout, as these can add differential-mode noise. Optionally, use a small coupling capacitor (1-nF typical) between the VOUTS+ and VOUTS– pins to improve noise immunity. The output of the differential remote sense amplifier (DIFFO) is used for output voltage setting and error amplifier frequency compensation local to the device as shown in Figure 33.

Additionally, the voltage at the DIFFO pin is digitized, averaged to reduce measurement noise and continually stored in the READ_VOUT register, enabling output voltage telemetry.

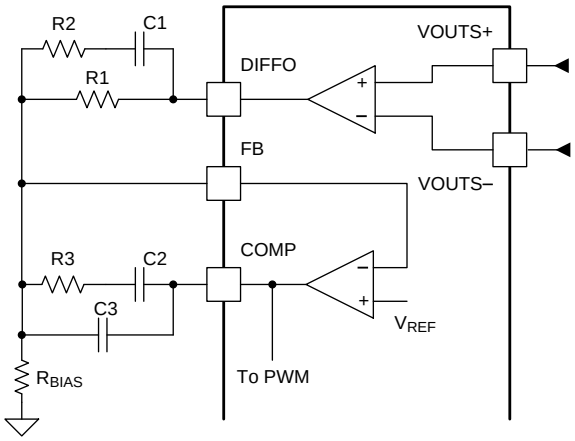


Figure 33. Output Voltage Setting

8.3.6 Set Output Voltage and Adapative Voltage Scaling (AVS)

A voltage divider from the DIFFO pin to the FB pin is typically required to set the nominal output voltage like the one formed by R1 and R_{BIAS} resistors shown in Figure 33. To allow PMBus devices to map between the commanded voltage and the voltage at the control circuit input (V_{OUT} divided down to match a reference voltage), the device uses the VOUT_SCALE_LOOP command.

VREF = VOUT_COMMAND × VOUT_MODE × VOUT_SCALE_LOOP (V)

where

- VOUT_SCALE_LOOP = $R_{BIAS}/(R_{BIAS}+R1)$ (as shown in Figure 33) (1)

VOUT = VOUT_COMMAND × VOUT_MODE = VOUT_COMMAND × 2^{-9} V. (2)

The output voltage can be set and adjusted dynamically using the VOUT_COMMAND through the PMBus interface. See the PMBus command description for full details on the implementation.

NOTE

- The VOUT_SCALE_LOOP is limited to only 3 possible options: 1 (default, no bottom resistor required for the divider), 0.5, and 0.25.
- When VOUT_SCALE_LOOP = 1 (default), no bottom resistor R_{BIAS} is needed. The reference voltage is equal to the output voltage, which allows tighter system DC accuracy by removing the resistor divider tolerance.
- It is required that the user make sure the divider ratio R_{BIAS} /(R_{BIAS} +R1) matches the programed VOUT_SCALE_LOOP and the user should program VOUT_SCALE_LOOP prior to any other VOUT related commands in order for the proper range checking to work and to avoid Invalid Data and output overvoltage and undervoltage scenarios.

Feature Description (continued)

The range of valid VOUT_COMMAND values is dependent upon the configured VOUT_SCALE_LOOP as shows in Table 1.

Table 1. FB Resistor Divider Ratio and VOUT_COMMAND Data Valid Range

VOUT_SCALE_LOOP	RESISTOR DIVIDER R_{BIAS}: R1 (IN Figure 33)	OUTPUT VOLTAGE RANGE (V)		VOUT_COMMAND DATA VALID RANGE	
		MIN	MAX	MIN	MAX
1	Unnecessary	0.5	1.5	256	768
0.5	1:1	1	3	512	1536
0.25	1:3	2	6	1024	3072

There are several commands that are used in commanding the output voltage of a device with a PMBus interface. These include:

- VOUT_MODE
- VOUT_COMMAND
- VOUT_MAX
- MFR_VOUT_MIN
- VOUT_SCALE_LOOP
- VOUT_OV_FAULT_LIMIT
- VOUT_OV_WARN_LIMIT
- VOUT_UV_WARN_LIMIT
- VOUT_UV_FAULT_LIMIT

Figure 34 shows how the output voltage related commands are applied. The TPS544x25 devices implement relational check to make sure the VOUT_COMMAND is not programmed to exceed the VOUT_MAX, MFR_VOUT_MIN, VOUT_OV_WARN_LIMIT , and VOUT_UV_WARN_LIMIT. The VOUT_OV_WARN_LIMIT should also be smaller than VOUT_OV_FAULT_LIMIT and the VOUT_UV_WARN_LIMIT should be greater than VOUT_UV_FAULT_LIMIT. Violation of these relational check rules will set corresponding status bits and trigger $\overline{\text{SMBALERT}}$. See the PMBus command description for full details.

In order for the relational checking to operate properly and to avoid error flagging, the VOUT_SCALE_LOOP should be changed first, if needed. Any changes to other registers should be made such that the values in all the registers conform to the limits for the current VOUT_SCALE_LOOP setting.

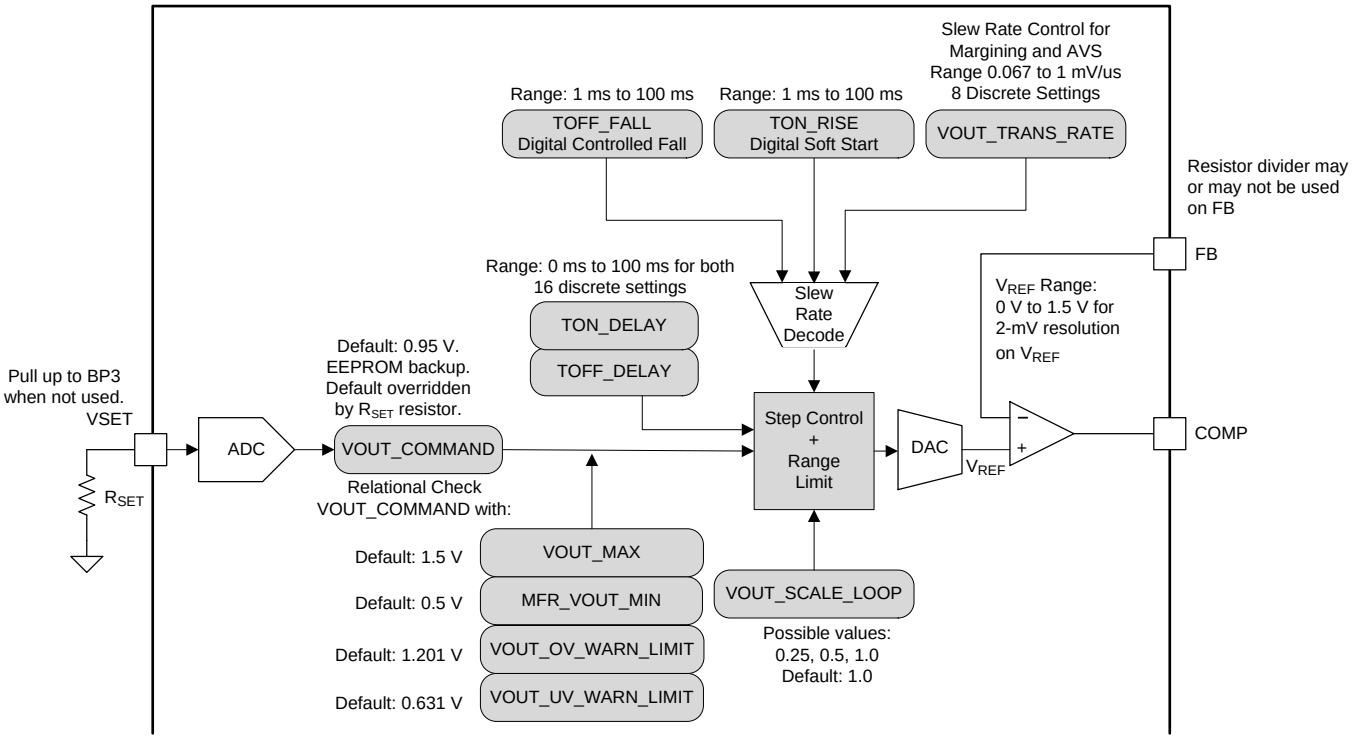


Figure 34. Conceptual View Of How Output Voltage Related Commands Are Applied

8.3.6.1 Increasing the Output Voltage

The order below is optimum for programming the output voltage upwards (not all commands may be necessary).

- (40h) VOUT_OV_FAULT_LIMIT
- (42h) VOUT_OV_WARN_LIMIT
- (24h) VOUT_MAX (ordering with respect to VOUT_OV_FAULT_LIMIT and VOUT_OV_WARN_LIMIT is irrelevant. Just set VOUT_MAX prior to VOUT_COMMAND)
- (21h) VOUT_COMMAND
- (A4h) MFR_VOUT_MIN (ordering with respect to VOUT_UV_FAULT_LIMIT and VOUT_UV_WARN_LIMIT is irrelevant. Just set MFR_VOUT_MIN after VOUT_COMMAND)
- (43h) VOUT_UV_WARN_LIMIT
- (44h) VOUT_UV_FAULT_LIMIT

8.3.6.2 Decreasing the Output Voltage

The order below is optimum for programming the output voltage downwards (not all commands may be necessary).

- (44h) VOUT_UV_FAULT_LIMIT
- (43h) VOUT_UV_WARN_LIMIT
- (A4h) MFR_VOUT_MIN (ordering with respect to VOUT_UV_FAULT_LIMIT and VOUT_UV_WARN_LIMIT is irrelevant. Just set MFR_VOUT_MIN prior to VOUT_COMMAND)
- (21h) VOUT_COMMAND
- (24h) VOUT_MAX (ordering with respect to VOUT_OV_FAULT_LIMIT and VOUT_OV_WARN_LIMIT is irrelevant. Just set VOUT_MAX after VOUT_COMMAND)
- (42h) VOUT_OV_WARN_LIMIT
- (40h) VOUT_OV_FAULT_LIMIT

8.3.6.3 Set Default Output Voltage by VSET

In order to power up the converter to a default VOUT_COMMAND rather than that stored in EEPROM without reprogramming, the initial boot-up output voltage can also be set by the resistor connected from VSET pin to AGND. The E48 series resistors with no worse than 1% tolerance suggested for setting the output votlage are shown in Table 2. VOUT_SCALE_LOOP can be set only at a value of 1 (no bottom resistor is needed in the feedback resistor divider) if the VSET pin is used. If VSET pin is not used, pull it up to BP3. If TPS544x25 devices re-start after losing power completely, the VOUT_COMMAND value set by external resistor overwrites any value stored from previous VOUT_COMMAND operation.

Table 2. VSET Resistors for Boot-up VOUT_COMMAND Value

BOOT-UP DEFAULT VOUT_COMMAND (V)	RESISTOR VALUE (kΩ)
0.95	Short to AGND
0.80	8.66
0.85	15.4
0.90	23.7
0.95	34.8
1.00	51.1
1.05	78.7
1.10	121
1.20	187
VOUT_COMMAND value stored in EEPROM	(VSET pin pulled up to BP3)(1)

(1) sets iv_vset bit in STATUS_MFR_SPECIFIC (80h)

If the resistor connected from VSET pin to AGND is used to set the output voltage, the SYNC/RESET_B pin is configured as RESET_B pin on default. Reset the output voltage to the boot-up voltage when SYNC/RESET_B is logic low. See Reset VOUT for more details.

If the VSET pin voltage higher than the VSET disable threshold (2.41 V minimum), the VSET function is disabled, the boot-up default VOUT_COMMAND are restored from the internal EEPROM of the TPS544x25 devices. When VSET is not used, the SYNC/RESET_B pin is configured as SYNC pin on default and the switching frequency synchronizes to the external clock applied to SYNC/RESET_B pin. In order to use both VSET and SYNC function, the FORCE_SYNC bit in register MISC_CONFIG_OPTIONS (MFR_SPECIFIC_32) (F0h) should be set to 1. The aforementioned interaction between VSET and SYNC/RESET_B pin funcationality is listed in Table 3. See Switching Frequency and Synchronization for more details.

The VSET pin configuration also affects the PMBus logic threshold in the TPS544x25 devices. See OPTIONS (MFR_SPECIFIC_21) (E5h) for details.

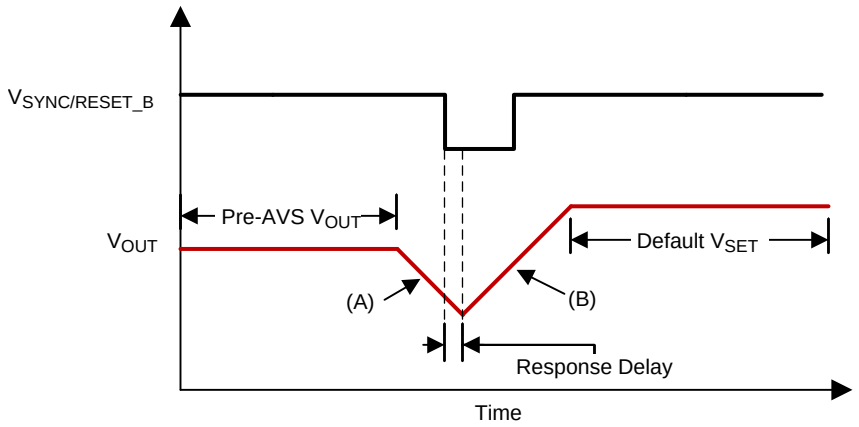
Table 3. Interaction between VSET and SYNC/RSET_B Pin Funcationality

VSET Used(1)	FORCE_SYNC	SYNC/RSET_B FUNCTIONALITY
No	0	SYNC
No	1	SYNC
Yes	0	RESET_B
Yes	1	SYNC

(1) VSET pin voltage < 2.41 V

8.3.7 Reset VOUT

Without power cycling, the VOUT_COMMAND value and the corresponding output voltage can be reset to the default value set by VSET. To reset VOUT_COMMAND, the VSET pin should be used in combination with SYNC/RESET_B pin. The default VOUT_COMMAND value is set by the resistor connected between VSET and AGND and latched when the TPS544x25 devices are powered up from VDD. When the SYNC/RESET_B pin is pulled low, the digital core sets VOUT_COMMAND value back to the default value. The Figure 35 shows the timing diagram for resetting the output voltage. When RESET_B is asserted low, after a short delay (less than 2 µs), the output voltage begins transitioning from its current value to the default value configured by VSET per the slew-rate set in VOUT_TRANSITION_RATE. The VOUT_COMMAND value is not updated to any VOUT_COMMAND programming while SYNC/RESET_B is held low.



(A) VOUT_COMMAND adjustment through the PMBus interface ;

(B) Reset back to default VOUT_COMMAND value determined by VSET resistor at power up. The slew rate is defined by VOUT_TRANSITION_RATE.

Figure 35. Output Voltage Reset

8.3.8 Switching Frequency and Synchronization

A resistor from the RT pin to AGND sets the switching frequency. Equation 3 calculates the R_{RT} resistor value.

$$R_{RT} = \frac{2.01 \times 10^{10}}{f_{SW}} \quad (3)$$

where

- R_{RT} is the timing resistor in Ω
- f_{SW} is the switching frequency in Hz

The TPS544x25 devices are designed to operate between 200 kHz and 1 MHz.

The TPS544x25 devices can also synchronize to an external clock which is ±20% of the free-running frequency. The external clock should be applied to the SYNC/RESET_B pin. A sudden change in synchronization clock frequency causes an associated control loop response, resulting in an overshoot or undershoot on the output voltage.

If a resistor is connected from VSET pin to AGND to program the initial boot-up voltage, the clock synchronization function is disabled on default, the SYNC/RESET_B pin is configured to RESET function which can reset VOUT when SYNC/RESET_B is logic low.

In order to use both VSET and SYNC function, the FORCE_SYNC bit in register MISC_CONFIG_OPTIONS (MFR_SPECIFIC_32) (F0h) should be set to 1, as shown in Table 3. While the output in regulation and an external clock being applied to SYNC/RESET_B pin, set the FORCE_SYNC bit on the fly causes a sudden change in switching frequency and results in an overshoot or undershoot on the output voltage.

8.3.9 Soft-Start and TON_RISE Command

To control the inrush current needed to charge the output capacitor bank during start up, the TPS544x25 devices implement a soft-start time. When the device is enabled, the feedback reference voltage, V_{REF}, ramps from 0 V to the final level defined by VOUT_COMMAND and VOUT_SCALE_LOOP at a slew rate defined by the TON_RISE command. The rise times specified are defined by the slew rate needed to ramp the reference voltage from 0 V to its final value at each given rise time.

The actual rise time of the converter output is slightly less than the rise time defined by TON_RISE. This difference occurs because switching does not occur until the error amplifier output reaches the valley of the PWM ramp. During soft-start, the error amplifier output voltage starts at 0 V, and must reach the valley of the PWM ramp, 0.75 V typical, before switching can begin. As soons as it reaches the valley of the PWM ramp, the converter output voltage rises quickly until the feedback voltage, V_{FB}, reaches the reference voltage V_{REF}, from which point they track through the end of the soft-start period.

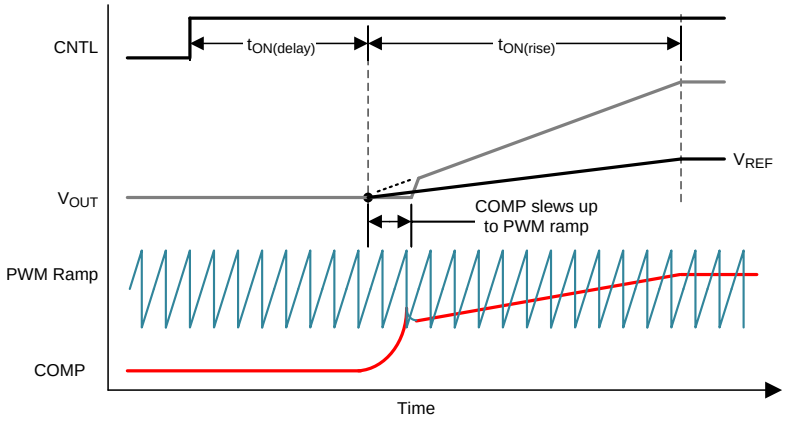


Figure 36. Soft-Start Timing

The TPS544x25 devices support several soft-start times between 1 ms and 100 ms selected by the TON_RISE command. The value of TON_RISE can be set through the PMBus interface or alternatively by the resistor connected from TSNS/SS pin to AGND. To use the TSNS/SS pin for TON_RISE setting, the SS_DET_DIS bit in OPTIONS (MFR_SPECIFIC_21) (E5h) register should be set to 0 to enable the soft-start time detection.

Table 4. TSNS/SS Pin Configuration

SS_DET_DIS	TSNS/SS FUNCTIONALITY
0	SS
1	TSNS

The E48 series resistors with no worse than 1% tolerance suggested for TON_RISE setting are shown in Table 5. Issuing TON_RISE command after start-up overwrites the TON_RISE value set by external resistor. If TPS544x25 re-starts after losing power completely, the TON_RISE value set by external resistor overwrites any value stored from previous TON_RISE operation.

Table 5. Soft-Start Resistors

TON_RISE (ms)	RESISTOR VALUE (kΩ)
5	Short to AGND (sets iv_ss bit in STATUS_MFR_SPECIFIC (80h))
1	8.25
2	14.7
3	22.6
5	34.8
7	51.1
10	78.7

Table 5. Soft-Start Resistors (continued)

TON_RISE (ms)	RESISTOR VALUE (kΩ)
27	121
52	187
5	TSNS/SS pin pulled up to BP3 (sets iv_ss bit in STATUS_MFR_SPECIFIC (80h))

8.3.10 Pre-Biased Output Start-Up

The TPS544x25 devices prevent current from being discharged from the output during start-up, when a pre-biased output condition exists. No SW pulses occur until the internal soft-start voltage rises above the error amplifier input voltage (FB pin), if the output is pre-biased. As soon as the soft-start voltage exceeds the error amplifier input, and SW pulses start, the device limits synchronous rectification after each SW pulse with a narrow on-time. The low-side MOSFET on-time slowly increases on a cycle-by-cycle basis until 128 pulses have been generated and the synchronous rectifier runs fully complementary to the high-side MOSFET. This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage start-up and ramp-to-regulation sequences are smooth and monotonic. These devices respond to a pre-biased output over-voltage condition immediately upon VDD powered up and BP6 regulator voltage above its own UVLO of 3.73 V typical.

8.3.11 Soft-Stop and TOFF_FALL Command

As shown in Figure 32, the TPS544x25 devices implement TOFF_FALL command to define the time for the output voltage to drop from regulation to 0. There might be negative current in the TPS544x25 devices during the TOFF_FALL time in order to discharge the output voltage. The setting of TOFF_FALL of 0 ms means the unit to bring its output voltage down to 0 as quickly as possible, which results in an effective TOFF_FALL time of 1 ms (fastest time supported). This feature can be disabled in ON_OFF_CONFIG for the turn-off controlled by CNTL pin or bit 6 of OPERATION if the regulator is turned off by OPERATION command, in that case, both high-side and low-side FET drivers are turned off immediately and the output voltage will be discharged by the load.

8.3.12 Current Monitoring and Low-Side MOSFET Overcurrent Protection

The TPS544x25 devices sense average output current using an internal sense FET. A sense FET conducts a scaled-down version of the power-stage current. Sampling this current in the middle of the low-side drive signal determines the average output current. This architecture achieves excellent current monitoring and better overcurrent threshold accuracy than inductor DCR current sensing with minimal temperature variation and no dependence on power loss in a higher DCR inductor. Use the IOUT_CAL_OFFSET command to improve current sensing and overcurrent accuracy by removing board layout-related systematic errors post assembly. The devices continually digitize the sensed output current, and average it to reduce measurement noise. The devices then store the current value in the read-only READ_IOUT register, enabling output current telemetry.

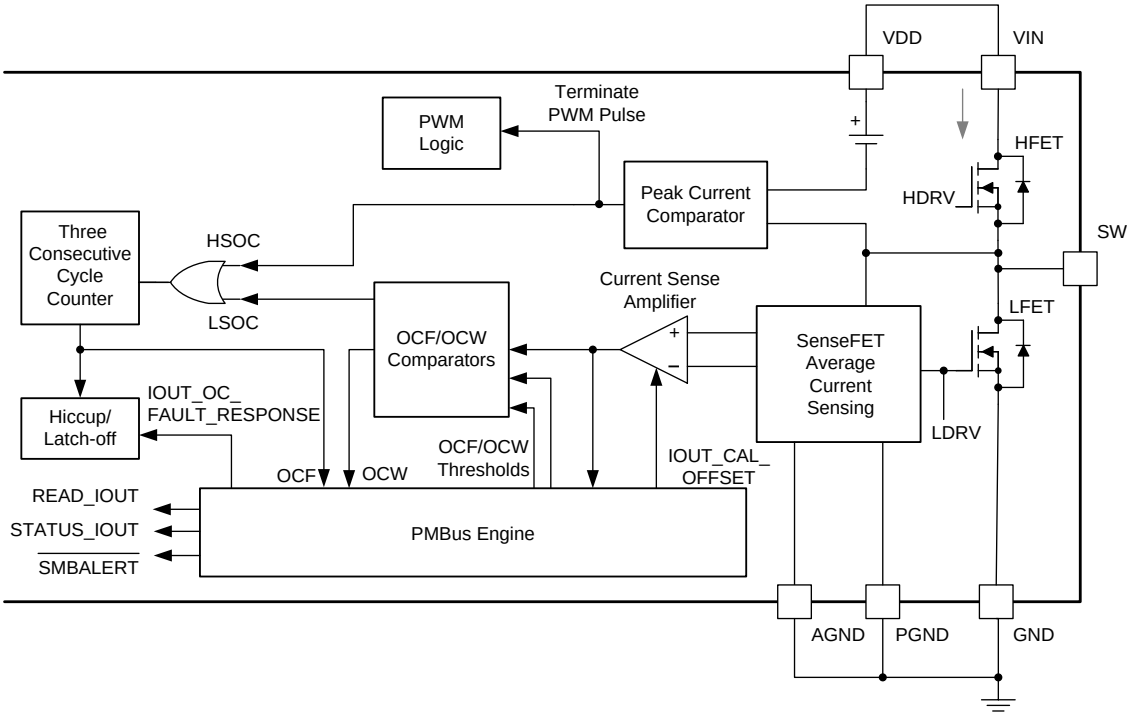


Figure 37. SenseFET Average Current Sensing and Overcurrent Protection

The TPS544x25 devices also implement low-side MOSFET overcurrent protection with programmable fault and warning thresholds. The IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT commands set the low-side overcurrent thresholds.

As shown in Figure 37, if an overcurrent event is detected in a given switching cycle, the device increments an overcurrent counter. When the device detects three consecutive overcurrent (either high-side or low-side) events, the converter responds, flagging the appropriate status registers, triggering SMBALERT if it is not masked, and entering either continuous restart hiccup, or latch-off according to the IOUT_OC_FAULT_RESPONSE command. In continuous restart hiccup mode, the devices implement a seven soft-start cycle time-out, followed by a normal soft-start attempt. When the overcurrent fault clears, normal operation resumes, otherwise, the device detects overcurrent and the process repeats. The IOUT_OC_FAULT_RESPONSE can also be set to ignore the OC fault for debug purpose. The fault response scheme is summarized in Table 6.

8.3.13 High-Side MOSFET Short-Circuit Protection

The TPS544x25 devices also implement a fixed high-side MOSFET overcurrent (HSOC) protection to limit peak current, and prevent inductor saturation in the event of a short circuit. The devices detect an overcurrent event by sensing the voltage drop across the high-side MOSFET when it is on. If the peak current reaches the I_{HOSC} level on any given cycle, the cycle terminates to prevent the current from increasing any further. High-side MOSFET overcurrent events are counted using the method shown in Figure 37. If the devices detect three consecutive overcurrent events (high-side or low-side), the converter responds, by flagging the appropriate status registers; triggering SMBALERT if it is not masked; and entering either continuous restart hiccup, or latch-off according to the IOUT_OC_FAULT_RESPONSE command. For accurate high-side MOSFET overcurrent protection, the VIN and VDD pins must be the same potential; split rail operation is not supported. The IOUT_OC_FAULT_RESPONSE can also be set to ignore the OC fault for debug purpose. When the IOUT_OC_FAULT_RESPONSE is set to ignore, the device continues to have cycle-by-cycle HSOC protection. The fault response scheme is summarized in Table 6.

8.3.14 Over-Temperature Protection

An internal temperature sensor protects theTPS544x25 devices from thermal runaway. The internal thermal shutdown threshold, T_{SD}, is fixed at 145°C typical. When the devices sense a temperature above T_{SD}, an over-temperature fault internal (OTFI) bit in STATUS_MFR_SPECIFIC is flagged, and power conversion stops until the sensed junction temperature falls by the thermal shutdown hysteresis amount, T_{HYST}, (20°C typical). The SMBALERT will be triggered if it is not masked.

The TPS544x25 devices also provide programmable external over-temperature fault and warning thresholds using measurements from an external temperature sensor connected on the TSNS/SS pin as shown in Figure 38. The temperature sensor circuit applies two bias currents to an external NPN transistor, and measures ΔV_{BE} to infer the junction temperature of the sensor. The TPS544x25 devices are designed to use a standard 2N3904 NPN transistor as a temperature sensor. Other sensors may be used, but the devices assume an ideality factor, *n*, of 1.008 for use with the 2N3904 transistor. The devices then digitize the result and compare it to the user-configured over-temperature fault and warning thresholds. When an external over-temperature fault (OTF) is detected, power conversion stops until the sensed temperature falls by 20°C. The READ_TEMPERATURE_2 (8Eh) register is continually updated with the digitized temperature measurement, enabling temperature telemetry. The OT_FAULT_LIMIT (4Fh) and OT_WARN_LIMIT (51h) commands set over-temperature fault and warning thresholds via the PMBus interface. When an overtemperature event is detected, the device sets the appropriate flags in STATUS_TEMPERATURE (7Dh) and triggers SMBALERT if it is not masked.

TI recommends including a 1-nF capacitor between the TSNS/SS pin and AGND to reduce temperature measurement noise. Optionally, external temperature sensing can be disabled by terminating TSNS/SS to AGND with a 0-Ω resistor. This termination forces the external temperature measurement to –40°C, and prevents external over-temperature faults tripping. The internal temperature sensor, and internal over-temperature fault remain enabled regardless of the TSNS/SS pin termination.

NOTE

The READ_TEMPERATURE_2 (8Eh) value remains at 25°C when SS_DET_DIS in OPTIONS (MFR_SPECIFIC_21) (E5h) is set to 0 since the TSNS/SS pin is configured to set TON_RISE time and not used for external temperature sensing (see Table 4).

The device response upon over-temperature fault can be set to Latch-off, Restart and Ignore in OT_FAULT_RESPONSE. The fault response scheme is summarized in Table 6.

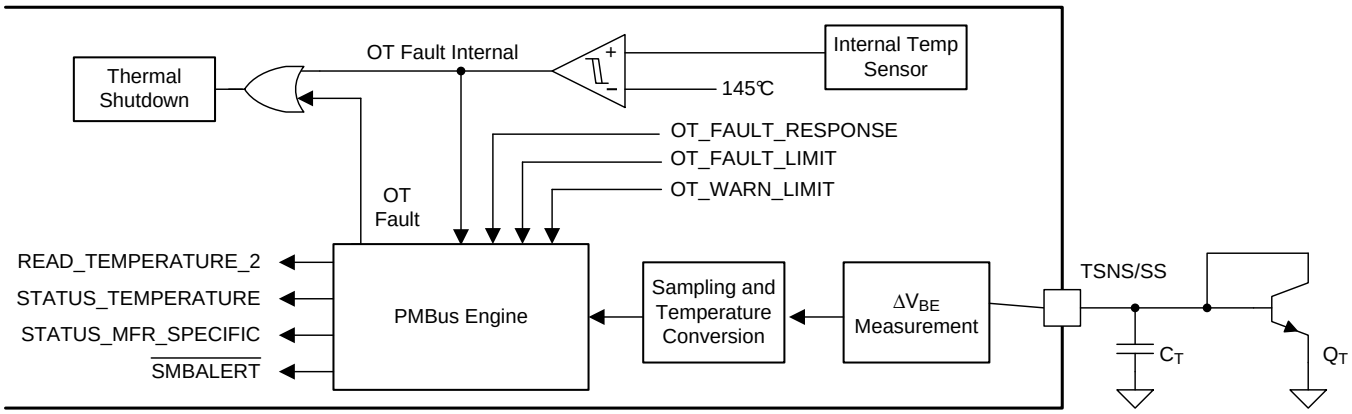


Figure 38. Over-Temperature Protection

8.3.15 Output Overvoltage and Undervoltage Protection

The TPS544x25 devices include both output overvoltage protection and output undervoltage protection capability. The devices compare the DIFFO pin voltage to internal selectable pre-set voltages, as defined by the VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT command . As the output voltage rises or falls from the nominal voltage, the DIFFO voltage tracks the output voltage.

If the DIFFO pin voltage rises above the output overvoltage protection threshold VOUT_OV_FAULT_LIMIT, the device terminates normal switching and turns on the low-side MOSFET to discharge the output capacitor and prevent further increases in the output voltage. The device also declares an OV fault, flagging the appropriate status registers, triggering SMBALERT if it is not masked. Then the device enters continuous restart hiccup, or latch-off according to the VOUT_OV_FAULT_RESPONSE command. The TPS544x25 devices respond to the output over-voltage condition immediately upon VDD powered up and BP6 regulator voltage above its own UVLO of 3.73 V typical. The VOUT_OV_FAULT_RESPONSE can also be set to ignore the output overvotlage fault and continue without interruption. Under this configuration, the control loop continues to respond and adjust PWM duty cycle in order to keep output voltage within regulation.

If the DIFFO pin voltage falls below the undervoltage protection level defined by VOUT_UV_FAULT_LIMIT after soft-start has completed, the device terminates normal switching and forces both the high-side and low-side MOSFETs off, and awaits an external reset or begins a hiccup time-out delay prior to restart, depending on the value of the VOUT_UV_FAULT_RESPONSE command. The device also declares a UV fault, flagging the appropriate status registers, triggering SMBALERT if it is not masked. The VOUT_UV_FAULT_RESPONSE can also be set to ignore the output undervotlage fault and continue without interruption for debug purpose.

The fault response scheme is summarized in Table 6.

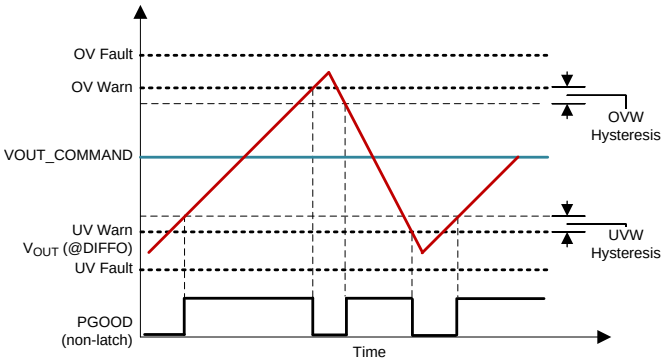
8.3.16 TON_MAX Fault

The TON_MAX_FAULT_LIMIT command sets an upper limit, in ms, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. The TPS544x25 devices differentiate a startup UV fault and a regulation UV fault by implementing the TON_MAX_FAULT_LIMIT . The TON_MAX_FAULT_LIMIT can allow the TPS544x25 devices more time than the soft-start time defined by TON_RISE to come into regulation and the UV detection is essentially delayed up to the TON_MAX_FAULT_LIMIT time. Refer to PMBus command section TON_MAX_FAULT_LIMIT for more details.

8.3.17 Power Good (PGOOD) Indicator

When the output voltage remains within the PGOOD window after the start-up period, PGOOD as an open-drain output is released, and rises to an externally supplied logic level. The PGOOD window is defined by VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT, which can be programmed through the PMBus interface, as shown in Figure 39. The PGOOD hystersis window scales with respect to VOUT_SCALE_LOOP, i.e. the OVW and UVW hystersis window of VOUT_SCALE_LOOP = 0.5 is twice the size of VOUT_SCALE_LOOP = 1 and just half of the size of VOUT_SCALE_LOOP = 0.25. The The PGOOD pin pulls low upon any fault condition on default. Please refer to Table 6 for the possible sources to pull down PGOOD pin.

The PGOOD signal can be connected to the CNTL pin of another device to provide additional controlled turn-on and turn-off sequencing.



(1) V_{OUT} is measured at the DIFFO pin.

Figure 39. PGOOD Threshold and Hysteresis

NOTE

Pulling PGOOD pin high before the TPS544x25 devices gets input power could cause PGOOD pin going high due to the limited pull-down capability in un-powered condition. If this is not desired, increase the pull-up resistance or reduce the external pull-up supply voltage.

8.3.18 Fault Protection Responses

Table 6 Summarizes the various fault protections and associated responses.

Table 6. Fault Protection Summary

FAULT or WARN	PROGRAMMING	FAULT RESPONSE SETTING	FET BEHAVIOR	ACTIVE DURING TON_RISE	SOURCE OF SMBALERT	SMBALERT MASKABLE	PGOOD
External Over Temp Fault	OT_FAULT_LIMIT (4Fh)	Latch-off	Both FETs off	Yes	Yes	Yes	Low
		Restart	Both FETs off, then restart after cooling down (1)				Low
		Ignore	FETs still controlled by PWM				High
External Over Temp Warn	OT_WARN_LIMIT (51h)	Latch-off or Restart on Fault	PWM maintains control of FETs	Yes	Yes	Yes	Low
		Ignore Fault					High
Internal Over Temp Fault (Junction Thermal Shutdown)	Threshold fixed internally	Latch-off	Both FETs off	Yes	Yes	Yes	Low
		Restart	Both FETs off, then restart after cooling down (1)				
		Ignore	Both FETs off, then restart after cooling down (2)				
Low-Side OC Fault	IOUT_OC_FAULT_LIMIT (46h)	Latch-off	3 PWM counts, then both FETs off	Yes	Yes	Yes	Low
		Restart	3 PWM counts, then both FETs off, restart after 7×TON_RISE				Low
		Ignore	FETs still controlled by PWM				High
Low-Side OC Warn	IOUT_OC_WARN_LIMIT	Latch-off or Restart on Fault	PWM maintains control of FETs	Yes	Yes	Yes	Low
		Ignore Fault					High
High-Side OC Fault	HSOC_USER_TRIM[1:0]	Latch-off	3 PWM counts, then both FETs off	Yes	Yes	Yes	Low
		Restart	3 PWM counts, then both FETs off, restart after 7×TON_RISE				Low
		Ignore	Cycle-by-cycle peak current limit				High
V_{OUT} OV Fault	VOUT_OV_FAULT_LIMIT	Latch-off	High-side FET OFF, low-side FET response configured byOV_RESP_SEL: latch ON or turn on till Vout reach VOUT_UV_FAULT_LIMIT	Yes	Yes	Yes	Low
		Restart	High-side FET OFF, low-side FET response configured by OV_RESP_SEL: latch ON or turn on till Vout reach VOUT_UV_FAULT_LIMIT. Then restart after 7×TON_RISE				
		Ignore	PWM maintains control of FETs				
V_{OUT} OV Warn	VOUT_OV_WARN_LIMIT	Latch-off or Restart on Fault	PWM maintains control of FETs	Yes	Yes	Yes	Low
		Ignore Fault					

(1) Once the external over-temperature fault is tripped, the device shuts off both FETs and restarts until the external sensed temperature falls 20°C from the OT_FAULT_LIMIT.
(2) The internal Over Temperature Fault (Junction Thermal Shutdown) cannot be ignored, the device shuts off both FETs and restarts after the internal die temperature drops below the threshold.

Table 6. Fault Protection Summary (continued)

FAULT or WARN	PROGRAMMING	FAULT RESPONSE SETTING	FET BEHAVIOR	ACTIVE DURING TON_RISE	SOURCE OF SMBALERT	SMBALERT MASKABLE	PGOOD
V_{OUT} UV Fault	VOUT_UV_FAULT_LIMIT	Latch-off	Both FETs off	No	Yes	Yes	Low
		Restart	Both FETs off, then restart after 7×TON_RISE				
		Ignore	PWM maintains control of FETs				
V_{OUT} UV Warn	VOUT_UV_WARN_LIMIT	Latch-off or Restart on Fault	PWM maintains control of FETs	No	Yes	Yes	Low
		Ignore Fault					
t_{ON} Max Fault	TON_MAX_FAULT_LIMIT	Latch-off	Both FETs off	No	Yes	Yes	Low
		Restart	Both FETs off, then restart after 7×TON_RISE				
		Ignore	PWM maintains control of FETs				
VIN UVLO	VIN_ON, VIN_OFF	Shut down	Both FETs off	Yes	Yes	Yes	Low

8.3.19 Switching Node

The SW pin connects to the switching node of the power conversion stage and acts as the return path for the high-side gate driver. When configured as a synchronous buck stage, the voltage swing on SW normally traverses from below ground to well above the input voltage. Parasitic inductance in the high-side FET and the output capacitance (C_{OSS}) of both power FETs form a resonant circuit that can produce high frequency (> 100 MHz) ringing on this node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Ensure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the pin.

In many cases, a series resistor and capacitor snubber network connected from the switching node to GND can be helpful in damping the ringing and decreasing the peak amplitude. Provide provisions for snubber network components in the layout of the printed circuit board. If testing reveals that the ringing amplitude at the SW pin exceeds the limit, then include snubber components. See SLUP100 for more information about snubber circuits design.

Placing a BOOT resistor in series with the BOOT capacitor slows down the turn-on of the high-side FET and can help to reduce the peak ringing at the switching node as well.

8.3.20 PMBus General Description

Timing and electrical characteristics of the PMBus interface specification can be found in the *PMB Power Management Protocol Specification, Part 1, revision 1.2* available at http://pmbus.org. The TPS544x25 devices support both the 100-kHz and 400-kHz bus timing requirements. The devices do not stretch pulses when communicating with the master device.

Communication over the PMBus interface can support the Packet Error Checking (PEC) scheme if desired. If the master supplies clock (CLK pin) pulses for the PEC byte, PEC is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The devices support a subset of the commands in the PMBus 1.2 Power Management Protocol Specification. See Supported PMBus Commands for more information

The devices also support the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave device (such as the TPS544x25 devices) can alert the bus master that it is available for communication. The master processes this event and simultaneously accesses all slaves on the bus (that support the protocol) through the alert response address (ARA). Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to ascertain the slave address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. By default these devices implement the *auto alert response*, a manufacturer specific improvement to the SMBALERT response protocol, intended to mitigate the issue of *bus hogging*. See Auto ARA Response for more information. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The devices contain non-volatile memory that stores configuration settings and scale factors. However, the device does not save the settings programmed into this non-volatile memory. The STORE_DEFAULT_ALL (11h) command must be used to commit the current settings to non-volatile memory as device defaults. The settings that are capable of being stored in non-volatile memory are noted in their detailed descriptions.

8.3.21 PMBus Address

The PMBus specification requires that each device connected to the PMBus have a unique address on the bus. The TPS544x25 devices each have 64 possible addresses (0 through 63 in decimal) that can be assigned by connecting resistors from the ADDR0 and ADDR1 pins to AGND. The address is set in the form of two octal (0-7) digits, one digit for each pin. ADDR1 is the high order digit and ADDR0 is the low-order digit. These address selection resistors must be 1% tolerance or better. Using resistors other than the recommended values can result in devices responding to adjacent addresses.

The E48 series resistors with no worse than 1% tolerance suggested for each digit value are shown in Table 7.

Table 7. Required Address Resistors

DIGIT	RESISTOR VALUE (kΩ)
0	8.66
1	15.4
2	23.7
3	34.8
4	51.1
5	78.7
6	121
7	187

The TPS544x25 devices also detect values that are out of range on the ADDR0 and ADDR1 pins. If the device detects that either pin has an out-of-range resistance connected to it, the device continues to respond to PMBus interface commands, but does so at address 127 decimal, which is outside of the possible programmed addresses. It is possible but not recommended to use the device in this condition, especially if other devices are present on the bus or if another device could possibly occupy the 127 decimal address.

Certain addresses in the I^2C address space are reserved for special functions and it is possible to set the address of the devices to respond to these addresses. The user is responsible for knowing which of these reserved addresses are in use in a system and for setting the address of the devices accordingly so as not to interfere with other system operations. The devices can be set to respond to the global call address or 0. It is recommended not to set the devices to this address unless the user is certain that no other devices respond to this address and that the overall bus is not affected by having such an address present.

8.3.22 PMBus Connections

The TPS544x25 devices support both the 100-kHz and 400-kHz bus speeds, 1.8-V or 3.3-V and 5-V PMBus interface logic level. See the *PMBus Interface* section of the Electrical Characteristics and PMBus command OPTIONS (MFR_SPECIFIC_21) (E5h) for more information.

8.3.23 Auto ARA (Alert Response Address) Response

By default, the TPS544x25 devices implement the *auto alert response*, a manufacturer specific improvement to the standard SMBALERT response protocol defined in the SMBus specification. The auto alert response is designed to prevent SMBALERT monopolizing in the case of a persistent fault condition on the bus. The user can choose to disable the auto ARA response, and use the standard SMBALERT response as defined in the SMBus specification, by using bit EN_AUTO_ARA of the OPTIONS (MFR_SPECIFIC_21) (E5h) register.

In the case of a fault condition, the slave device experiencing the fault pulls down the shared SMBALERT line, to alert the host that a fault condition has occurred. To establish which slave device has experienced the fault, the host issues a modified receive byte operation to the alert response address (ARA), to which only the slave pulling down on SMBALERT should respond. The SMBus protocol provides a method for address arbitration in the case that multiple slaves on the same bus are experiencing fault conditions. Once the host has established the address of the offending device, it must take any necessary action to release the SMBALERT line. For more information on the standard SMBus alert response protocol, see the System Management Bus (SMBus) specification.

In the case of a non-persistent fault (a single-time event, such as an invalid command or data byte), the host can ascertain the address of the slave experiencing a fault using the standard ARA response, and simply issue CLEAR_FAULTS (03h) to release the SMBALERT line, and resume normal operation. However, in the case of a persistent fault (one which remains active for some time, such as a short-circuit, or thermal shutdown), once the device issues a CLEAR_FAULTS (03h) command, the fault immediately re-triggers, and SMBALERT continues to be pulled low. In this case, the device holds low the SMBALERT line until the host masks the SMBALERT line using SMBALERT_MASK and then issues the CLEAR_FAULTS (03h) command. Because the SMBALERT line remains low, the host cannot be alerted to other fault conditions on the bus until it clears SMBALERT. Figure 40 and Figure 41 illustrate this response.

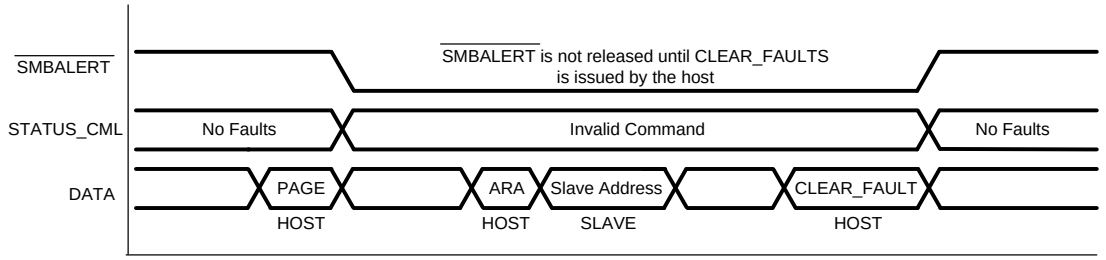


Figure 40. Example Standard ARA Response to Non-Persistent Fault

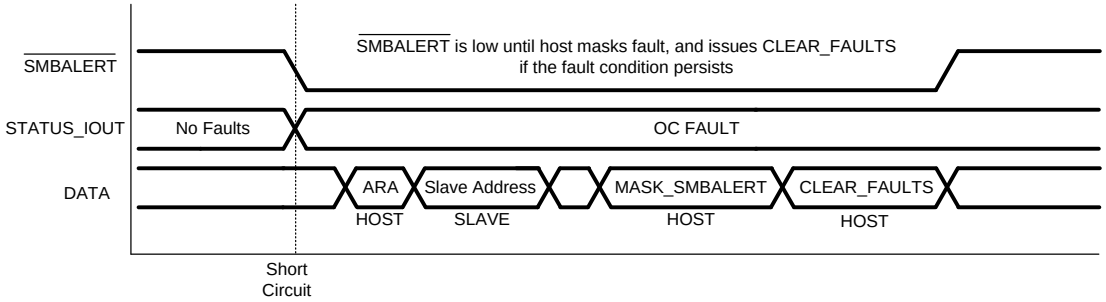


Figure 41. Example Standard ARA Response to a Persistent Fault

In order to mitigate the problem of SMBALERT *bus hogging* described previously, the devices implement the Auto ARA response. When Auto ARA is enabled, the devices releases SMBALERT automatically after successfully responding to access from the host at the alert response address. In this case, even when the device is experiencing a persistent fault, it does not hold the SMBALERT line low following successful notification of the host, and the host can be alerted to other faults on the bus in the normal manner. Examples of the auto ARA response are illustrated in Figure 42 and Figure 43.

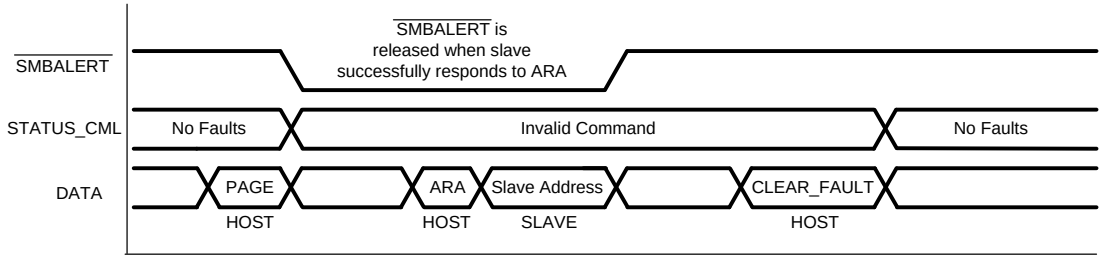


Figure 42. Example Auto ARA Response to Non-Persistent Fault

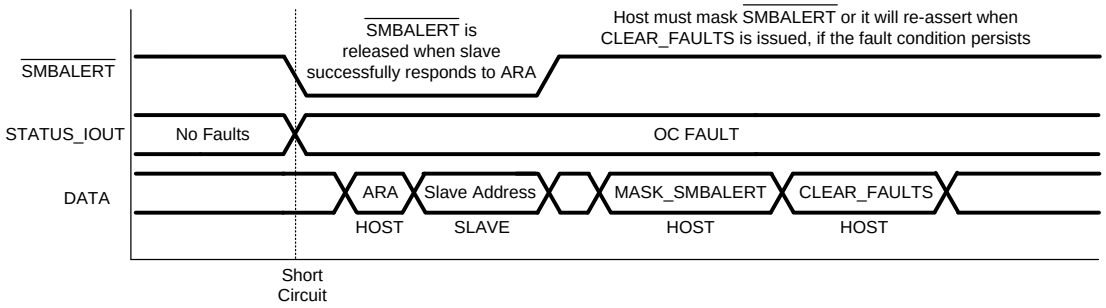


Figure 43. Example Auto ARA Response to Persistent Fault

8.4 Device Functional Modes

8.4.1 Continuous Conduction Mode

The TPS544x25 devices operate in continuous conduction mode (CCM) at a fixed frequency, regardless of the output current. For the first 128 switching cycles, the low-side MOSFET on-time is slowly increased to prevent excessive current sinking in the event the device is started with a pre-biased output. Following the first 128 clock cycles, the low-side MOSFET and the high-side MOSFET on-times are fully complementary.

8.4.2 Operation with CNTL Signal Control

According to the value in the ON_OFF_CONFIG register, the TPS544x25 devices can be commanded to use the CNTL pin to enable or disable regulation, regardless of the state of the OPERATION command. The CNTL pin can be configured as either active high or active low (inverted) logic.

8.4.3 Operation with OPERATION Control

According to the value in the ON_OFF_CONFIG register, the TPS544x25 devices can be commanded to use the OPERATION command to enable or disable regulation, regardless of the state of the CNTL signal.

8.4.4 Operation with CNTL and OPERATION Control

According to the value in the ON_OFF_CONFIG register, the TPS544x25 devices can be commanded to require both a signal on the CNTL pin, and the OPERATION command to enable or disable regulation.

8.5 Supported PMBus Commands

The commands listed in Table 8 are implemented as described to conform to the PMBus 1.2 specification. Default behavior and register values are also shown.

Table 8. Supported PMBus Commands and Default Values

CMD CODE	PMBus 1.2 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE	NVM
01h	OPERATION	Can be configured via ON_OFF_CONFIG to be used to turn the output on and off with or without input from the CTRL pin.	OPERATION is not used to enable regulation	00h	No
02h	ON_OFF_CONFIG	Configures the combination of CNTL pin input and OPERATION command for turning output on and off.	CNTL only. Active High	16h	Yes
03h	CLEAR_FAULTS	Clears all fault status registers to 0x00 and releases SMBALERT.	Write-only	n/a	No
10h	WRITE_PROTECT	Used to control writing to the volaile operating memory (PMBus and restore from EEPROM).	Allow writes to all registers	00h	Yes
11h	STORE_DEFAULT_ALL	Stores all current storable register settings into EEPROM as new defaults.	Write-only	n/a	No
12h	RESTORE_DEFAULT_ALL	Restores all storable register settings from EEPROM.	Write-only	n/a	No
19h	CAPABILITY	Provides a way for a host system to determine key PMBus capabilities of the device.	Read only. PMBus v1.2, 400 kHz, PEC enabled	B0h	No
1Bh	SMBALERT_MASK	Mask Warn or Fault status bits	Mask PGOODz only	n/a	Yes
20h	VOUT_MODE	Read-only output mode indicator.	Linear, exponent = –9	17h	No
21h	VOUT_COMMAND	Default Regulation Setpoint	950mV	01E6h	Yes

Supported PMBus Commands (continued)

Table 8. Supported PMBus Commands and Default Values (continued)

CMD CODE	PMBus 1.2 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE	NVM
24h	VOUT_MAX	Sets the maximum output voltage. VOUT_MAX imposes a higher bound to any attempted V_{OUT} setting from VOUT_COMMAND and VSET pin default.	1.5V	0300h	No
27h	VOUT_TRANSITION_RATE	Sets the rate at which the output should change voltage.	1 mV/us	D03Ch	No
29h	VOUT_SCALE_LOOP	Sets output sense scaling ratio for main control loop.	1	F004h	Yes
35h	VIN_ON	Sets value of input voltage at which the device should start power conversion.	4.5 V	F012h	Yes
36h	VIN_OFF	Sets value of input voltage at which the device should stop power conversion.	4.0V	F010h	Yes
39h	IOUT_CAL_OFFSET	Can be set to null out offsets in the current sensing circuit.	0.0000 A	E000h	Yes
40h	VOUT_OV_FAULT_LIMIT	Sets output overvoltage fault threshold.	1.281 V	0290h	Yes
41h	VOUT_OV_FAULT_RESPONSE	Sets output overvoltage fault response.	Restart	BFh	Yes
42h	VOUT_OV_WARN_LIMIT	Sets output overvoltage warning threshold.	1.201 V	0267h	No
43h	VOUT_UV_WARN_LIMIT	Sets output undervoltage warning threshold.	0.631 V	0143h	No
44h	VOUT_UV_FAULT_LIMIT	Sets output undervoltage fault threshold.	0.594 V	0130h	Yes
45h	VOUT_UV_FAULT_RESPONSE	Sets output undervoltage fault response.	Restart	BFh	Yes
46h	IOUT_OC_FAULT_LIMIT	Sets the value of the output current that causes an overcurrent fault condition.	36 A (TPS544C25)	F848h	Yes
			24 A (TPS544B25)	F830h	
47h	IOUT_OC_FAULT_RESPONSE	Sets response to output overcurrent faults to latch-off, hiccup mode or ignore.	Restart	BFh	Yes
4Ah	IOUT_OC_WARN_LIMIT	Sets the value of the output current that causes an overcurrent warning condition.	34 A (TPS544C25)	F844h	No
			22 A (TPS544B25)	F82Ch	
4Fh	OT_FAULT_LIMIT	Sets the value of the sensed temperature that causes an overtemperature fault condition.	125 °C	007Dh	Yes
50h	OT_FAULT_RESPONSE	Sets response to over temperature faults to latch-off, hiccup mode or ignore.	Restart	BFh	Yes
51h	OT_WARN_LIMIT	Sets the value of the sensed temperature that causes an overtemperature warning condition.	100 °C	0064h	No
60h	TON_DELAY	Sets the turn-on delay.	0 ms	0000h	Yes
61h	TON_RISE	Sets the time from when the output starts to rise until the voltage has entered the regulation band.	5 ms	0005h	Yes

Supported PMBus Commands (continued)

Table 8. Supported PMBus Commands and Default Values (continued)

CMD CODE	PMBus 1.2 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE	NVM
62h	TON_MAX_FAULT_LIMIT	Sets an UPPER limt in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. The time begins counting as the device enters the soft-start period.	100 ms	0064h	No
63h	TON_MAX_FAULT_RESPONSE	Sets the soft start timeout fault response.	Restart	BFh	Yes
64h	TOFF_DELAY	Sets the turn-off delay.	0 ms	0000h	Yes
65h	TOFF_FALL	Sets the soft stop fall time.	0 ms	0000h	Yes
78h	STATUS_BYTE	Returns one byte summarizing the most critical faults.	Read only	Current status	No
79h	STATUS_WORD	Returns two bytes summarizing fault and warning conditions.	Read only	Current status	No
7Ah	STATUS_VOUT	Returns one byte detailing if an output fault or warning has occurred	Read only	Current status	No
7Bh	STATUS_IOUT	Retyrns one byte detailing if an overcurrent fault or warning has occurred	Read only	Current status	No
7Ch	STATUS_INPUT	Returns one byte of information relating to the status of the converter's input related faults.	Read only	Current status	No
7Dh	STATUS_TEMPERATURE	Returns one byte detailing if a sensed temperature fault or warning has occurred.	Read only	Current status	No
7Eh	STATUS_CML	Returns one byte containing PMBus serial communication faults.	Read only	Current status	No
80h	STATUS_MFR_SPECIFIC	Returns one byte detailing if internal overtemperature or address detection fault has occurred.	Read only	Current status	No
8Bh	READ_VOUT	Returns the output voltage in volts.	Read only	Current status	No
8Ch	READ_IOUT	Returns the output current in amps.	Read only	Current status	No
8Eh	READ_TEMPERATURE_2	Returns the sensed temperature in degrees Celsius.	Read-only, 25 C whenSS_DET_DIS in OPTIONS (MFR_SPECIFIC_21) (E5h) = 0.	0019h	No
98h	PMBUS_REVISION	Returns PMBus revision to which the device is compliant.	Read only	12h	No
A4h	MFR_VOUT_MIN	Sets the minimum output voltage. MFR_VOUT_MIN imposes a lower bound to any attempted V_{OUT} setting from VOUT_COMMAND and VSET pin default.	0.5 V	0100h	No

Supported PMBus Commands (continued)

Table 8. Supported PMBus Commands and Default Values (continued)

CMD CODE	PMBus 1.2 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE	NVM
ADh	IC_DEVICE_ID	This Read-only Block Read command returns a single word (16 bits) with the unique Device Code identifier for each device for which this IC can be configured. The BYTE_COUNT field in the Block Read command is 2 (indicating 2 bytes follow): Low Byte first, then High Byte.	TPS544C25	0027h	No
			TPS544B25	0028h	
AEh	IC_DEVICE_REV	This Read-only Block Read command returns a single word (16 bits) with the unique Device revision identifier. The BYTE_COUNT field in the Block Read command is 2 (indicating 2 bytes follow): Low Byte first, then High Byte.	Read only	0000h	No
D0h	MFR_SPECIFIC_00	User scratch pad.		0000h	Yes
E5h	OPTIONS (MFR_SPECIFIC_21)	Sets user selectable options. Options register: Disable SS detection, Enable Auto Alert Response Address response (ARA), ADC averaging, Enable Data limit override, Enable ADC, Enable Vout Scan Mode, Enable auto PMBus rail logic level detection and Force PMBus rail logic level.	Enable SS detection, auto ARA, ADC conversion, PMBus auto detection, 8x average for V/I/T reporting, and force 1.8V logic	00C7h	Yes
F0h	MISC_CONFIG_OPTIONS (MFR_SPECIFIC_32)	Sets miscellaneous user selectable options. Options register: Force SYNC, HSOC user trim, OVP response options.	The SYNC/RESET_B pin operates as RESET_B if VSET detection is valid; default trim for HS OC; for OVP response, the LS FET latches on when an OV fault is detected, and turns off as soon as the sensed output (at DIFFO pin) drops below the UV fault threshold.	0001h	Yes

8.6 Register Maps

This family of devices supports the following commands from the PMBus 1.2 specification.

Register Access Legend:

- r- read
- w - write
- superscript E – the bit is backed up with Non-volatile EEPROM

8.6.1 OPERATION (01h)

The OPERATION command turns the device output on or off in conjunction with input from the CNTL signal. It is also used to set the output voltage to the upper or lower margin voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CNTL pin instructs the device to change to another mode.

COMMAND	OPERATION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r	r	r	r	r	r
Function	ON	OFF	X	X	X	X	X	X
Default Value	0	0	X	X	X	X	X	X

8.6.1.1 On

This bit is an enable command to the converter.

- 0: output switching is disabled. Both drivers placed in an off or low state.
- 1: output switching is enabled if the input voltage is above undervoltage lockout, OPERATION is configured as a gating signal in ON_OFF_CONFIG, and no fault conditions exist.

8.6.1.2 Off

This bit sets the turn-off behavior when commanding the unit to turn off via OPERATION[7] (the " On" bit).

- 0: Immediately turn off the output (not honoring the programmed turn-off delay (TOFF_DELAY) and ramp down (TOFF_FALL)) when commanded off via OPERATION[7] (the " On" bit).
- 1: Use the programmed turn-off delay (TOFF_DELAY) and ramp down (TOFF_FALL) when commanded off via OPERATION[7] – aka "soft off".

NOTE

The device ignores any values written to read-only bits. Additionally, both "on" and "off" bits being set at the same time is not allowed and considered invalid data per section 12.1 of the PMBus Specification Part II; any attempt to do so causes the device to set the 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the STATUS_CML registers, and triggers SMBALERT signal.

8.6.2 ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CNTL pin input and serial bus commands needed to turn the unit on and off. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL (11h) command. The default value in ON_OFF_CONFIG register is to have the device power up by CNTL pin only with the active high polarity and use the programmed turn-off delay (TOFF_DELAY) and ramp down (TOFF_FALL) for powering off the converter.

COMMAND	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	X	X	X	pu	cmd	cpr	pol	cpa
Default Value	X	X	X	1	0	1	1	0

8.6.2.1 pu

The pu bit sets the default to either operate any time power is present or for power conversion to be controlled by CNTL pin and PMBus OPERATION command. This bit is used in conjunction with the 'cpr', 'cmd', and 'on' bits to determine start up.

BIT VALUE	ACTION
0	Device powers up any time power is present regardless of state of the CNTL pin.
1	Device does not power up until commanded by the CNTL pin and/or OPERATION command as programmed in bits [3:0] of the ON_OFF_CONFIG register.

8.6.2.2 cmd

The cmd bit controls how the device responds to the OPERATION **co**m**m**an**d**. This bit is used in conjunction with the 'cpr', 'pu', and 'on' bits to determine start up.

BIT VALUE	ACTION
0	Device ignores the “on” bit in the OPERATION command.
1	Device responds to the “on” bit in the OPERATION command.

8.6.2.3 cpr

The cpr bit sets the **C**NTL **p**in **r**esponse. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up.

BIT VALUE	ACTION
0	Device ignores the CNTL pin. Power conversion is controlled only by the OPERATION command.
1	Device requires the CNTL pin to be asserted to start the unit.

8.6.2.4 pol

The pol bit controls the **pol**arity of the CNTL pin. For a change to become effective, the contents of the ON_OFF_CONFIG register must be stored to non-volatile memory using the STORE_DEFAULT_ALL command and the device power cycled. Simply writing a new value to this bit does not change the polarity of the CNTL pin.

BIT VALUE	ACTION
0	CNTL pin is active low.
1	CNTL pin is active high.

8.6.2.5 cpa

The cpa bit sets the **C**NTL **p**in **a**ction when turning the converter off.

BIT VALUE	ACTION
0	Use the programmed turn-off delay (TOFF_DELAY) and ramp down (TOFF_FALL).
1	Immediately turn off the output (**not** honoring the programmed turn-off delay (TOFF_DELAY) and ramp down (TOFF_FALL)).

8.6.3 CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT signal output if the device is asserting the SMBALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately reset and the host notified by the usual means.

NOTE

- To get a reliable clear fault result, the clear_fault command should be issued (8 × TON_RISE + TON_DELAY) after the switcher shuts down.
- In the case of OV fault with “latch off” response, the LS FET latches on when the fault is detected. If the OV_RESP_SEL bit in (F0h) MFR_SPECIFIC_32 is set to 1, then the LS FET releases when the output voltage falls below the VOUT_UV_FAULT_LIMIT. Otherwise, it remains on until the CLEAR_FAULTS command is issued. The CLEAR FAULTS command causes the LS FET to turn off.
- To clear an OV fault, two CLEAR_FAULTS commands need to be issued and the OVF cannot be cleared the first time, but the second time.

8.6.4 WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the device configuration or operation. All supported command parameters may have their parameters read, regardless of the WRITE_PROTECT settings. Write protection also prevents protected registers from being updated in the event of a RESTORE_DEFAULT_ALL. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

COMMAND	WRITE_PROTECT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r/w^E	r/w^E	X	X	X	X	X
Function	bit7	bit6	bit5	X	X	X	X	X
Default Value	0	0	0	X	X	X	X	X

8.6.4.1 bit5

BIT VALUE	ACTION
0	Enable all writes as permitted in bit6 or bit7
1	Disable all writes except the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND. (bit6 and bit7 must be 0 to be valid data)

8.6.4.2 bit6

BIT VALUE	ACTION
0	Enable all writes as permitted in bit5 or bit7
1	Disable all writes except for the WRITE_PROTECT, and OPERATION commands. (bit5 and bit7 must be 0 to be valid data)

8.6.4.3 bit7

BIT VALUE	ACTION
0	Enable all writes as permitted in bit5 or bit6
1	Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)

In any case, only one of the three bits may be set at any one time. Attempting to set more than one bit results in an alert being generated and the cml bit is STATUS_WORD being set. An invalid setting of the WRITE_PROTECT command results in no write protection.

Data Byte Value	ACTION
1000 0000	Disables all WRITES except to the WRITE_PROTECT command.
0100 0000	Disables all WRITES except to the WRITE_PROTECT, and OPERATION commands.
0010 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND commands.

8.6.5 STORE_DEFAULT_ALL (11h)

The STORE_DEFAULT_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed. Issuing STORE_DEFAULT_ALL also causes the device to be unresponsive via PMBus for a period of ~100ms.

EEPROM programming faults cause the device to NACK and set the 'cml' bit in the STATUS_BYTE and the 'mem' bit in the STATUS_CML registers.

8.6.6 RESTORE_DEFAULT_ALL (12h)

The RESTORE_DEFAULT_ALL command restores all of the storable register settings from EEPROM memory to those registers which are unprotected according to current setting of WRITE_PROTECT. Issuing STORE_DEFAULT_ALL also causes the device to be unresponsive via PMBus for a period of ~100ms.

NOTE

Do not use this command while the device is actively switching, this causes the device to stop switching and the output voltage to fall during the restore event. Depending on loading conditions, the output voltage could reach an undervoltage level and trigger an undervoltage fault response if programmed to do so. The command can be used while the device is switching, but it is not recommended as it results in a restart that could disrupt power sequencing requirements in more complex systems. It is strongly recommended that the device be stopped before issuing this command.

8.6.7 CAPABILITY (19h)

The CAPABILITY command provides a way for a host system to determine some key capabilities of this PMBus device.

COMMAND	CAPABILITY							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	PEC	SPD		ALRT	Reserved			
Default Value	1	0	1	1	0	0	0	0

The default values indicate that the device supports Packet Error Checking (PEC), a maximum bus speed of 400 kHz (SPD) and the SMBus Alert Response Protocol using SMBALERT.

8.6.8 SMBALERT_MASK (1Bh)

The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SMBALERT signal.

NOTE

The command uses the SMBus Write Word command protocol to overlay a “mask byte” with an associated/designated status register. It uses the SMBus Block Write/Block Read protocol – with a block size = 1, to read the mask settings for any given status register. If the host in the Block_Count field of the Block Write portion sends a block size unequal to 1 the device returns a NACK. The device always returns a Block Count of 1 upon reads of SMBALERT_MASK.

The bits in the mask byte align with the bits in the corresponding status register. For example, if the STATUS_TEMPERATURE command were sent with the mask byte 01000000b, then an Over Temperature Warning condition would be blocked from asserting SMBALERT. Please refer to the PMBus v1.2 specification - section 15.38 (SMBALERT_MASK Command) and the SMBus specification Block Write/Block Read protocol for further details.

There are 19 maskable SMBALERT sources in the TPS544x25. Each of these 19 status conditions has an associated EEPROM backed mask bit. These sources are represnted and identified in the status register command descriptions by a particular status bit denoted as having EEPROM backup (e.g. a bit access of r/w^{E}). Writes and reads to SMBALERT_MASK command code accepts only the following as valid STATUS_x command codes:

- STATUS_WORD
- STATUS_VOUT
- STATUS_IOUT
- STATUS_INPUT

- STATUS_TEMPERATURE
- STATUS_CML
- STATUS_MFR_SPECIFIC

Attempting to write a mask byte for any STATUS_X command code other than this list causes the device to set the 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the STATUS_CML registers, and triggers SMBALERT. Attempting to read a mask byte for any STATUS_x command code other than this list returns 00h for the mask byte. Refer to these individual command descriptions for further details on their specific smbalert masking capabilities.

There is 1 unique status bit in the TPS544x25 that warrants special clarification: PGOOD_Z (STATUS_WORD[10]) is maskable as an SMBALERT source via SMBALERT_MASK commands to STATUS_WORD. If the user wants to write, or read, the mask bit for PGOOD_Z, they must put '79h' in the STATUS_x COMMAND_CODE field of the SMBALERT_MASK command. PGOOD_Z SMBALERT_MASK bit default to 1.

8.6.9 VOUT_MODE (20h)

The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit mode and 5-bit exponent parameter, as shown below. The 3-bit mode sets whether the device uses the Linear or Direct modes for output voltage related commands. The 5-bit parameter sets the exponent value for the linear data mode. The mode and exponent parameters are fixed and do not permit the user to change the values.

COMMAND	VOUT_MODE							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Mode			Exponent				
Default Value	0	0	0	1	0	1	1	1

8.6.9.1 Mode:

Value fixed at 000, linear mode.

8.6.9.2 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95mV/count).

8.6.10 VOUT_COMMAND (21h)

The VOUT_COMMAND command sets the output voltage in volts. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command. The exponent is set be VOUT_MODE at –9 (equivalent of 1.953 mV/count). The programmed the output voltage is computed as:

$$V_{OUT} = \text{VOUT\_COMMAND} \times \text{VOUT\_MODE (V)} = \text{VOUT\_COMMAND} \times 2^{-9} \text{ (V)} \quad (4)$$

The range of valid VOUT_COMMAND values is dependent upon the configured VOUT_SCALE_LOOP (29h) as follows:

VOUT_SCALE_LOOP	Vout Range (volts)	VOUT_COMMAND data valid range
1	0.5 – 1.5	256 - 768
0.5	1 – 3	512 - 1536
0.25	2 – 6	1024 - 3072

There are 2 "invalid data" situations that are possible and checked in hardware. They are handled differently:

- The first case is if the value programmed to VOUT_COMMAND exceeds the value stored in either MFR_VOUT_MIN (A4h) or VOUT_MAX (24h). In this case, VOUT_COMMAND is set to the appropriate MFR_VOUT_MIN or VOUT_MAX value (which ever was violated). See the command descriptions for MFR_VOUT_MIN (A4h) or VOUT_MAX (24h) for the specific status bits set in either case.
- The second case is if VOUT_COMMAND is attempted to be programmed outside the OV and UV warn limits.

In this case, the VOUT_COMMAND value remains unchanged. Specifically, the following relationships must be maintained:

- VOUT_COMMAND < VOUT_OV_WARN_LIMIT
- VOUT_COMMAND > VOUT_UV_WARN_LIMIT

In this second case where VOUT_COMMAND is attempted to be programmed outside the OV or UV Warn limits, it causes the device to set the 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the STATUS_CML registers, and triggers SMBALERT signal.

When using the VSET function, at initial power-up. the Mantissa value decoded according to the appropriate VSET resistor is written into the VOUT_COMMAND register as the initial default. Note this overwrites any value restored from EEPROM when the device VDD is powered up.

COMMAND	VOUT_COMMAND															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0

8.6.10.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95mV/count, specified in VOUT_MODE command).

8.6.10.2 Mantissa

This is the Mantissa for the linear format. Default value is: 0000 0001 1110 0110 (bin) 486 (dec) (equivalent Vout default = 0.95V).

8.6.11 VOUT_MAX (24h)

The VOUT_MAX command sets the maximum output voltage. The purpose is to protect the device(s) on the output rail supplied by this device from a higher than acceptable output voltage. VOUT_MAX imposes an upper bound to any attempted output voltage setting:

a) programmed VOUT_COMMAND

b) VSET pin default

If any attempt is made to program the output voltage (using the VOUT_COMMAND) in excess of the value in VOUT_MAX, the device also:

- Clamps the output voltage at the programmed VOUT_MAX value
- Sets the OTH (other) bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the VOUT_MAX_Warning bit in the STATUS_VOUTregister
- Notifies the host via the SMBALERT pin

The exponent is set be VOUT_MODE at –9 (equivalent of 1.953 mV/count). The programmed output voltage is computed as:

$$\text{MAXIMUM VOUT allowed} = \text{VOUT\_MAX} \times \text{VOUT\_MODE (V)} = \text{VOUT\_MAX} \times 2^{-9}\ \text{(V)} \quad (5)$$

There are 2 "invalid data" situations that are possible and checked in hardware. They are handled differently:

- If the commanded VOUT_MAX is outside the valid data range for the VOUT_SCALE_LOOP configured, but, is still relationally correct (above VOUT_COMMAND). In this case, that value is not accepted; but, VOUT_MAX is set to the highest allowed value.
- The second case is the opposite, where the attempted write value is within the absolute range of VOUT_MAX; but, is not relationally correct (it is below VOUT_COMMAND). In this case, VOUT_MAX remains unchanged.

Both cases equally cause the device to set the 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the STATUS_CML registers, and triggers SMBALERT signal.

COMMAND	VOUT_MAX															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															

8.6.11.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95 mV/count, specified in VOUT_MODE command).

8.6.11.2 Mantissa

The range of valid VOUT_MAX values is dependent upon the configured (29h) VOUT_SCALE_LOOP as follows.

If VOUT_SCALE_LOOP = 1:

- default: 0000 0011 0000 0000 (bin) 768 (dec) (equivalent output voltage default = 1.5V)
- Minimum : 0000 0001 0001 1010 (bin) 282 (dec) (equivalent VOUT_MAX = 0.55V)
- Maximum: 0000 0011 0000 0000 (bin) 768 (dec) (equivalent VOUT_MAX = 1.5V)

If VOUT_SCALE_LOOP = 0.5:

- default: 0000 0110 0000 0000 (bin) 1536 (dec) (equivalent output voltage default = 3V)
- Minimum : 0000 0010 0011 0100 (bin) 564 (dec) (equivalent VOUT_MAX = 1.1V)
- Maximum: 0000 0110 0000 0000 (bin) 1536 (dec) (equivalent VOUT_MAX = 3V)

If VOUT_SCALE_LOOP = 0.25:

- default: 0000 1100 0000 0000 (bin) 3072 (dec) (equivalent output voltage default = 6V)
- Minimum : 0000 0100 0110 1000 (bin) 1128 (dec) (equivalent VOUT_MAX = 2.2V)
- Maximum: 0000 1100 0000 0000 (bin) 3072 (dec) (equivalent VOUT_MAX = 6V)

8.6.12 VOUT_TRANSITION_RATE (27h)

The VOUT_TRANSITION_RATE command sets the rate of change in mV/µs of any output voltage change during normal operation (also includes vout changes in TOFF_DELAY state. In contrast Soft Start transition rate is controlled by TON_RISE and the TOFF_FALL transition rate is controlled by TOFF_FALL command).

Only 8 fixed output voltage transition rates are available in the device. As such, the range of programmed vout_transition rates are sub-divided into 8 "buckets" that then selects one of the 8 fixed V_{OUT} transition rates. Programmed values are rounded to the nearest "bucket/transition rate" as outlined in the table below.

COMMAND	VOUT_TRANSITION_RATE															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	0	1	0	0	0	0	0	0	1	1	1	1	0	0

8.6.12.1 Exponent

default: 11010 (bin) -6 (dec) (0.015625)

These default settings are not programmable.

8.6.12.2 Mantissa

default: 000 0011 1100 (bin) 60 (dec) (equivalent VOUT_TRANSITION_RATE = 1mV/µs)

NOTE

It is possible to use VOUT_TRANSITION_RATE to slew Vref faster than the voltage loop can track. This causes a control related overshoot/undershoot response on the output voltage.

VOUT_TRANSITION rate (mV/µs)	VOUT_TRANSITION Mantissa (d)	
	Greater than	Less than or equal to
0.067		5
0.1	5	7
0.143	7	12
0.222	12	17
0.333	17	25
0.5	25	47
1	47	79
1.5	79	

8.6.13 VOUT_SCALE_LOOP (29h)

VOUT_SCALE_LOOP is equal to the feedback resistor ratio (R_{BIAS} /(R_{BIAS} +R1) in the configuration shown in Figure 33). It is limited to only 3 possible options/ratios: 1 (default, no R_{BIAS} needed), 0.5, and 0.25. Attempting to write a value unequal to one of these three options cause the device to set the 'cml' bit in the STATUS_BYTE, and the 'ivd' bit in the STATUS_CML registers. Additionally, SMBALERT is asserted and the value of VOUT_SCALE_LOOP remains unchanged. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

NOTE

Construct the feedback resistor ratio appropriately (see Table 1).

Program the VOUT_SCALE_LOOP setting before the output is turned on.

In order for the range checking to work properly and to avoid Invalid Data scenarios:

- VOUT_SCALE_LOOP should be changed first, if needed.
- Any changes to these registers should be made such that:
  - The values in all the registers conform to the limits for the current VOUT_SCALE_LOOP setting
  - The order below is optimum for programming the output voltage upwards (not all commands may be necessary)
    - (40h) VOUT_OV_FAULT_LIMIT
    - (42h) VOUT_OV_WARN_LIMIT
    - (24h) VOUT_MAX (ordering with respect to VOUT_OV_FAULT_LIMIT and VOUT_OV_WARN_LIMIT is irrelevant. Just set VOUT_MAX prior to VOUT_COMMAND)
    - (21h) VOUT_COMMAND
    - (A4h) MFR_VOUT_MIN (ordering with respect to VOUT_UV_FAULT_LIMIT and VOUT_UV_WARN_LIMIT is irrelevant. Just set MFR_VOUT_MIN after VOUT_COMMAND)
    - (43h) VOUT_UV_WARN_LIMIT
    - (44h) VOUT_UV_FAULT_LIMIT
  - The order below is optimum for programming the output voltage downwards (not all commands may be necessary)
    - (44h) VOUT_UV_FAULT_LIMIT
    - (43h) VOUT_UV_WARN_LIMIT
    - (A4h) MFR_VOUT_MIN (ordering with respect to VOUT_UV_FAULT_LIMIT and VOUT_UV_WARN_LIMIT is irrelevant. Simply set MFR_VOUT_MIN prior to VOUT_COMMAND)
    - (21h) VOUT_COMMAND

- (24h) VOUT_MAX (ordering with respect to VOUT_OV_FAULT_LIMIT and VOUT_OV_WARN_LIMIT is irrelevant. Simply set VOUT_MAX after VOUT_COMMAND)
- (42h) VOUT_OV_WARN_LIMIT
- (40h) VOUT_OV_FAULT_LIMIT

COMMAND	VOUT_SCALE_LOOP															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0

8.6.13.1 Exponent

default: 11110 (bin) -2 (dec) (equivalent LSB=0.25)

These default settings are not programmable.

8.6.13.2 Mantissa

default: 000 0000 0100 (bin) 4 (dec) (equivalent VOUT_SCALE_LOOP voltage = 1)

For VOUT_SCALE_LOOP = 1.00, mantissa = 004h. ($4 \times 2^{-2} = 1.00$)

For VOUT_SCALE_LOOP = 0.50, mantissa = 002h. ($2 \times 2^{-2} = 0.50$)

For VOUT_SCALE_LOOP = 0.25, mantissa = 001h. ($1 \times 2^{-2} = 0.25$)

8.6.14 VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start operation assuming all other required startup conditions are met. Values are mapped to the nearest supported increment. Values outside the supported range are treated as invalid data and cause the device set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers, and trigger SMBALERT signal. The value of VIN_ON remains unchanged on an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

The supported VIN_ON values are shown in Table 9:

Table 9. Supported VIN_ON Values

VIN_ON Values (V)				
4.25	4.5 (default)	4.75	5	5.25
5.5	5.75	6	6.25	6.5
6.75	7	7.25	7.5	7.75

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT signal being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5-bit exponent and an 11-bit mantissa. The four most significant bits of the mantissa are fixed, while the lower 4 bits may be altered.

COMMAND	VIN_ON															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	1

8.6.14.1 Exponent

default: 11110 (bin) -2 (dec) (equivalent LSB=0.25V)

These default settings are not programmable.

8.6.14.2 Mantissa

default: 000 0001 0010 (bin) 18 (dec) (equivalent VIN_ON voltage = 4.5V)

Minimum : 000 0001 0001 (bin) 17 (dec) (equivalent VIN_ON voltage = 4.25V)

Maximum: 000 0001 1111 (bin) 31 (dec) (equivalent VIN_ON voltage = 7.75V)

8.6.15 VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop operation. Values are mapped to the nearest supported increment. Values outside the supported range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers, and trigger SMBALERT signal. The value of VIN_OFF remains unchanged during an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

The supported VIN_OFF values are shown in Table 10:

Table 10. Supported VIN_OFF Values

VIN_OFF Values (V)				
4 (default)	4.25	4.5	4.75	5
5.25	5.5	5.75	6	6.25
6.5	6.75	7	7.25	7.5

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT being asserted along with the cml bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5 bit exponent and an 11 bit mantissa. The 4 most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

COMMAND	VIN_OFF															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0

8.6.15.1 Exponent

default: 11110 (bin) -2 (dec) (equivalent LSB=0.25V)

These default settings are not programmable.

8.6.15.2 Mantissa

default: 000 0001 0000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 4.0V)

Minimum : 000 0001 0000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 4.0V)

Maximum: 000 0001 1110 (bin) 30 (dec) (equivalent VIN_OFF voltage = 7.50V)

8.6.16 IOUT_CAL_OFFSET (39h)

The IOUT_CAL_OFFSET is used to compensate for offset errors in the READ_IOUT results and the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT thresholds. The units are amperes. The default setting is 0 A. The resolution of the argument for this command is 62.5 mA and the range is +3.9375 A to -4.0 A. Values written outside of this range alias into the supported range. This occurs because the read-only bits are fixed. The exponent is always –4 and the 5 msb bits of the Mantissa are always equal to the sign bit. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

COMMAND	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w^{E}	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.16.1 Exponent

default: 11100 (bin) -4 (dec) (lsb=62.5mA)

These default settings are not programmable.

8.6.16.2 Mantissa

MSB is programmable with sign, next 4 bits are sign extend only.
Lower six bits are programmable with a default value of 0 (dec).

8.6.17 VOUT_OV_FAULT_LIMIT (40h)

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage that causes an output overvoltage fault. Attempts to write values outside of the acceptable range is treated as invalid data, causing the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALERT signal. Additionally, the value of VOUT_OV_FAULT_LIMIT remains unchanged. Maintaining values within “acceptable range” also means:

VOUT_OV_WARN_LIMIT < VOUT_OV_FAULT_LIMIT < (922d/VOUT_SCALE_LOOP)

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command. Note the lower 4 bits can not be backed up in EEPROM.

The VOUT_OV_FAULT_LIMIT takes a two-byte data word formatted as shown below:

COMMAND	VOUT_OV_FAULT_LIMIT															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w	r/w	r/w	r/w
Function	Mantissa															
Default Value	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0

8.6.17.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95mV/count, specified in VOUT_MODE command).

8.6.17.2 Mantissa

default: 0000 0010 1001 0000 (bin) 656 (dec) (equivalent OVF 1.281 V or 134.8% of 0.95 V default reference (VOUT_COMMAND))

NOTE

Changing the VOUT_OV_FAULT_LIMIT (or Warn, or UV Fault, or Warn limit) during regulation causes a brief overshoot/undershoot on the output voltage. This is due to the Vref DAC being shared with OVUV DAC.

8.6.18 VOUT_OV_FAULT_RESPONSE (41h)

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to a VOUT_OV_FAULT_LIMIT fault. The device also:

- Sets the OVF bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the OVF bit in the STATUS_VOUT register, and
- Notifies the host by asserting SMBALERT

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

Bits [2:0] are hard-wired to 0x7 (111b) to indicate the 7 × TON_RISE time delay in response to a output overvoltage fault.

The default response to a output overvoltage fault is to shut down and restart with 7 × TON_RISE time delay.

COMMAND	VOUT_OV_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r/w^E	r/w	r/w	r	r	r
Function	RSP[1]	0	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	1	0	1	1	1	1	1	1

8.6.18.1 RSP[1]

This bit sets the output voltage over voltage **r**e**sp**onse to either ignore or not. Default is 1.

0: The PMBus device continues operation without interruption. Note: In this “ignore” fault response mode, the associated fault status bits is set. Additionally, SMBALERT remains triggered if it is not masked.

1: The PMBus device shuts down and restarts according to RS[2:0].

8.6.18.2 RS[2:0]

These bits are output voltage over voltage **r**etry **s**etting. Default is 111b.

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert SMBALERT along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Note, that since all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

8.6.19 VOUT_OV_WARN_LIMIT (42h)

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage that causes an output overvoltage warning condtion. Attempts to write values outside of the acceptable range is treated as invalid data, causing the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALERT signal. Additionally, the value of VOUT_OV_WARN_LIMIT remains unchanged. Maintaining values within “acceptable range” also means:

- VOUT_COMMAND < VOUT_OV_WARN_LIMIT < VOUT_OV_FAULT_LIMIT
- 269d < VOUT_OV_WARN_LIMIT × VOUT_SCALE_LOOP

The device also:

- Sets the oth bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the OVW bit in the STATUS_VOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

The VOUT_OV_WARN_LIMIT takes a two-byte data word formatted as shown below:

COMMAND	VOUT_OV_WARN_LIMIT															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															
Default Value	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	1

8.6.19.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95mV/count, specified in VOUT_MODE command).

8.6.19.2 Mantissa

default: 0000 0010 0110 0111 (bin) 615(dec) (equivalent OVW 1.201 V or 126.4% of 0.95 V default reference (VOUT_COMMAND))

Note: The default VOUT_OV_WARN_LIMIT is calculated from the EEPROM backed OVF limit by:

VOUT_OV_WARN_LIMIT = VOUT_OV_FAULT_LIMIT - VOUT_OV_FAULT_LIMIT/16

If the calculated value for VOUT_OV_WARN_LIMIT violates the requirement that VOUT_COMMAND < VOUT_OV_WARN_LIMIT, then the VOUT_OV_WARN_LIMIT value is set to VOUT_OV_FAULT_LIMIT - 1 LSB.

NOTE

Changing the VOUT_OV_WARN_LIMIT (or Fault, or UV Fault, or Warn limit) during regulation causes a brief overshoot/undershoot on the output voltage. This is due to the Vref DAC being shared with OVUV DAC.

8.6.20 VOUT_UV_WARN_LIMIT (43h)

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage that causes an output undervoltage warning condtion. This warning is masked until the unit reaches the programmed output voltage. This warning is also masked when the unit is disabled. Attempts to write values outside of the acceptable range is treated as invalid data, causing the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALERT}}$ signal. Additionally, the value of VOUT_UV_WARN_LIMIT remains unchanged. Maintaining values within “acceptable range” also means:

- VOUT_UV_FAULT_LIMIT < VOUT_UV_WARN_LIMIT < VOUT_COMMAND
- 178d < VOUT_UV_WARN_LIMIT × VOUT_SCALE_LOOP < 732d

The device also:

- Sets the oth bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the UVW bit in the STATUS_VOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

The VOUT_UV_WARN_LIMIT takes a two-byte data word formatted as shown below:

COMMAND	VOUT_UV_WARN_LIMIT															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1

8.6.20.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95mV/count, specified in VOUT_MODE command).

8.6.20.2 Mantissa

default: 0000 0001 0100 0011 (bin) 323(dec) (equivalent UVW 0.631 V or 66.4% of 0.95 V default reference (VOUT_COMMAND))

Note: The default VOUT_UV_WARN_LIMIT is calculated from the EEPROM backed UVF limit by:

VOUT_UV_WARN_LIMIT = VOUT_UV_FAULT_LIMIT + VOUT_UV_FAULT_LIMIT/16

If the calculated value for VOUT_UV_WARN_LIMIT violates the requirement that VOUT_COMMAND > VOUT_UV_WARN_LIMIT, then the VOUT_UV_WARN_LIMIT value is set to VOUT_UV_FAULT_LIMIT (rounded) + 1 LSB.

For the case when VOUT_UV_FAULT_LIMIT = 0 (which indicates it is disabled), the VOUT_UV_WARN_LIMIT default shall be the minimum value for the configured VOUT_SCALE_LOOP (179d/VOUT_SCALE_LOOP).

NOTE

Changing the VOUT_UV_WARN_LIMIT (or Fault, or OV Fault, or Warn limit) during regulation causes a brief overshoot/undershoot on the output voltage. This is due to the Vref DAC being shared with OVUV DAC.

8.6.21 VOUT_UV_FAULT_LIMIT (44h)

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage that causes an output undervoltage fault. This fault is masked until the unit reaches the programmed output voltage. This fault is also masked when the unit is disabled. Attempts to write values outside of the acceptable range is treated as invalid data, causing the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALERT signal. Additionally, the value of VOUT_UV_FAULT_LIMIT remains unchanged. Maintaining values within “acceptable range” also means:

- 176d/VOUT_SCALE_LOOP < VOUT_UV_FAULT_LIMIT < VOUT_UV_WARN_LIMIT

A VOUT_UV_FAULT_LIMIT of 0000h shall be a means of disabling VOUT_UV_FAULT response and reporting completely and is the only exception to the above “acceptable range” requirements. Disabling means that the unit does not check for Vout_UVF faults; thus there is no setting of UVF status bits, nor associated SMBALERT triggering. Disabling VOUT_UV_FAULT_LIMIT (by setting it to 0000h) has no bearing on VOUT_UV_WARN_LIMIT checking – which is considered a completely separate function.

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command. Note the lower 4 bits can not be backed up in EEPROM.

The VOUT_UV_FAULT_LIMIT takes a two-byte data word formatted as shown below:

COMMAND	VOUT_UV_FAULT_LIMIT															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w	r/w	r/w	r/w
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0

8.6.21.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95mV/count, specified in VOUT_MODE command).

8.6.21.2 Mantissa

default: 0000 0001 0011 0000 (bin) 304(dec) (equivalent UVW 0.594 V or 62.5% of 0.95 V default reference (VOUT_COMMAND))

NOTE

- Changing the VOUT_UV_FAULT_LIMIT (or Warn, or OV Fault, or Warn limit) during regulation causes a brief overshoot/undershoot on the output voltage. This is due to the Vref DAC being shared with OVUV DAC.
- Since the output undervoltage fault detection is masked until the unit reaches the programmed output voltage, if the output voltage did not reach the programmed value during the soft start time UPPER limit required by TON_MAX_FAULT_LIMIT, the device asserts a TON_MAX fault and reponse according to TON_MAX_FAULT_RESPONSE instead of VOUT_UV_FAULT_RESPONSE

8.6.22 VOUT_UV_FAULT_RESPONSE (45h)

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to a VOUT_UV_FAULT_LIMIT fault. The device also:

- Sets the oth bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the UVF bit in the STATUS_VOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

Bits [2:0] are hard-wired to 0x7 (111b) to indicate the 7 × TON_RISE time delay in response to a output undervoltage fault.

The default response to a output undervoltage fault is to shut down and restart with 7 × TON_RISE time delay.

COMMAND	VOUT_UV_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r/w^E	r/w	r/w	r	r	r
Function	RSP[1]	0	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	1	0	1	1	1	1	1	1

8.6.22.1 RSP[1]

This bit sets the output voltage under voltage **r**e**sp**onse to either ignore or not. Default is 1.

0: The PMBus device continues operation without interruption. Note: In this “ignore” fault response mode, the associated fault status bits are set. Additionally, $\overline{\text{SMBALERT}}$ continues to be triggered if it is not masked.

1: The PMBus device shuts down and restarts according to RS[2:0].

8.6.22.2 RS[2:0]

These bits are output voltage under voltage **r**etry **s**etting. Default is 111b.

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert SMBALERT along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Note, that since all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

8.6.23 IOUT_OC_FAULT_LIMIT (46h)

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. The IOUT_OC_FAULT_LIMIT should be set equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALERT signal. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

The IOUT_OC_FAULT_LIMIT takes a two-byte data word formatted as shown below:

COMMAND	IOUT_OC_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	See Below															

8.6.23.1 Exponent

default: 11111 (bin) -1 (dec) (0.5 amps)

These default settings are not programmable.

8.6.23.2 Mantissa

The upper four bits are fixed at 0.

The lower seven bits are programmable.

The actual output current for a given mantissa and exponent is shown in Equation 6.

$$I_{OUT(oc)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (6)$$

The default values and allowable ranges for each device are summarized below:

DEVICE	OC_FAULT_LIMIT			UNIT
	MIN	DEFAULT	MAX	
TPS544C25	5	36	40	A
TPS544B25	5	24	36	A

8.6.24 IOUT_OC_FAULT_RESPONSE (47h)

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT or a VOUT undervoltage (UV) fault. The device also:

- Sets the OCF bit in the STATUS_BYTE
- Sets the OCFW bit in the STATUS_WORD
- Sets the OCF bit in the STATUS_IOUT register, and
- Notifies the host by asserting SMBALERT

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

Bits [2:0] are hard-wired to 0x7 (111b) to indicate the 7 × TON_RISE time delay in response to an over current fault.

The default response to an over current fault is to shut down and restart with 7 × TON_RISE time delay.

COMMAND	IOUT_OC_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r/w^E	r/w	r/w	r	r	r
Function	RSP[1]	0	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	1	0	1	1	1	1	1	1

8.6.24.1 RSP[1]

This bit sets the over current fault **re**s**p**onse to either ignore or not. Default is 1.

0: The PMBus device continues operation without interruption. Note: In this “ignore” fault response mode, the associated fault status bits are set. Additionally, $\overline{\text{SMBALERT}}$ continues to be triggered if it is not masked.

1: The PMBus device shuts down and restarts according to RS[2:0].

8.6.24.2 RS[2:0]

These bits are over current fault **r**etry **s**etting. Default is 111b.

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (soft-start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert $\overline{\text{SMBALERT}}$ along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Note, that since all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

8.6.25 IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning. When this current level is exceeded the device:

- Sets the oth bit in the STATUS_BYTE
- Sets the OCFW bit in the STATUS_WORD
- Sets the OCW bit in the STATUS_IOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

The IOUT_OC_WARN_LIMIT threshold should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALERT}}$ signal.

The default IOUT_OC_WARN_LIMIT is always set to fixed, relative IOUT_OC_FAULT_LIMIT - 2 A. Since the IOUT_OC_WARN_LIMIT is not stored in EEPROM, the IOUT_OC_WARN_LIMIT register is set to 2 A less than the stored IOUT_OC_FAULT_LIMIT upon any RESTORE from EEPROM.

The IOUT_OC_WARN_LIMIT takes a two byte data word formatted as shown below:

COMMAND	IOUT_OC_WARN_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

COMMAND	IOUT_OC_WARN_LIMIT															
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	See Below															

8.6.25.1 Exponent

default: 11111 (bin) -1 (dec) (0.5 amps)

These default settings are not programmable.

8.6.25.2 Mantissa

The upper four bits are fixed at 0.

Lower seven bits are programmable.

The actual output warning current level for a given mantissa and exponent is:

$$I_{OUT\,(OCW)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \tag{7}$$

The default values and allowable ranges for each device are summarized below:

DEVICE	OC_WARN_LIMIT			UNIT
	MIN	DEFAULT	MAX	
TPS544C25	4	34	39.5	A
TPS544B25	4	22	35.5	

8.6.26 OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command sets the value of the temperature, in degrees Celsius, that causes an over-temperature fault condition, when the sensed temperature from the external sensor exceeds this limit.

The OT_FAULT_LIMIT must always be greater than the OT_WARN_LIMIT. Writing a value to OT_FAULT_LIMIT less than or equal to OT_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as asserts the SMBALERT signal. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

The OT_FAULT_LIMIT takes a two byte data word formatted as shown below.

COMMAND	OT_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

8.6.26.1 Exponent

default: 00000 (bin) 0 (dec) (represents mantissa with steps of 1 degree Celcius)

These default settings are not programmable.

8.6.26.2 Mantissa

default: 000 0111 1101 (bin) 125 (dec) (125 °C)

Minimum : 000 0111 1000 (bin) (equivalent OTF = 120 °C)

Maximum: 000 1010 0101 (bin) (equivalent OTF = 165 °C)

8.6.27 OT_FAULT_RESPONSE (50h)

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an OT_FAULT_LIMIT. The device also:

- Sets the OTFW bit in the STATUS_BYTE
- Sets the OTF bit in the STATUS_TEMPERATURE
- Notifies the host by asserting SMBALERT

Once the over-temperature fault is tripped, the fault flag is latched until the external sensed temperature falls 20°C from the OT_FAULT_LIMIT.

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

Bits [2:0] are hard-wired to 0x7 (111b) to indicate the 7 × TON_RISE time delay in response to an over temperature fault.

The default response to an over current fault is to shut down and restart with 7 × TON_RISE time delay.

COMMAND	OT_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r/w^E	r/w	r/w	r	r	r
Function	RSP[1]	0	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	1	0	1	1	1	1	1	1

8.6.27.1 RSP[1]

This bit sets the over temperature fault **r**e**sp**onse to either ignore or not. Default is 1.

0: The PMBus device continues operation without interruption. Note: In this “ignore” fault response mode, the associated fault status bits are set. Additionally, SMBALERT continues to be triggered if it is not masked.

1: The PMBus device shuts down and restarts according to RS[2:0].

8.6.27.2 RS[2:0]

These bits are over temperature fault **r**etry **s**etting. Default is 111b.

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert SMBALERT along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Note, that since all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

NOTE

The programmed response here is also applied to internally detected Over Temperture faults – with the one exception of the “ignore” response. Internal OT faults are never ignored. Internal OT faults always respond in a shutdown and attempted re-start once the part cools.

8.6.28 OT_WARN_LIMIT (51h)

The OT_ WARN _LIMIT command sets the value of the temperature, in degrees Celsius, that causes an over-temperature warning condition, when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature warning, the device takes the following actions:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT Warning bit in the STATUS_TEMPERATURE
- Notifies the host by asserting SMBALERT

Once the over-temperature warning is tripped, the warning flag is latched until the external sensed temperature falls 20°C from the OT_WARN_LIMIT.

The OT_WARN_LIMIT must always be less than the OT_FAULT_LIMIT. Writing a value to OT_WARN_LIMIT greater than or equal to OT_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALERT signal.

The default OT_WARN_LIMIT is mathematically derived from the EEPROM backed OTF limit by subtracting 25 from (4Fh) OT_FAULT_LIMIT to reach the default OT_WARN_LIMIT. If the calculated OTW is less than 100 °C, then the default value is set to 100 °C. OTW=max(OTF-25, 100)

The OT_WARN_LIMIT takes a two byte data word formatted as shown below:

COMMAND	OT_WARN_LIMIT															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0

8.6.28.1 Exponent

default: 00000 (bin) 0 (dec) (represents mantissa with steps of 1 degree Celcius)

These default settings are not programmable.

8.6.28.2 Mantissa

default: 000 0110 0100 (bin) 100 (dec) (100 °C) 25°C less than default OTF

Minimum : 000 0110 0100 (bin) (equivalent OTF = 100°C)

Maximum: 000 1000 1100 (bin) (equivalent OTF = 140°C)

8.6.29 TON_DELAY (60h)

The TON_DELAY command sets the time in milliseconds, from when a start condition is received to when the output voltage starts to rise. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

The TON_DELAY command is formatted as a linear mode two's complement binary integer.

COMMAND	TON_DELAY															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.29.1 Exponent

default: 00000 (bin) 0 (dec) (1 millisecond)

These default settings are not programmable.

8.6.29.2 Mantissa

The upper four bits are fixed at 0. The lower seven bits are programmable with a default value of 000 0000 0000 (bin) (0 ms).

Only 16 fixed TON_DELAY times are available in the device. As such, the range of programmed TON_DELAY settings are sub-divided into 16 “buckets” that then selects one of the 16 supported times. Programmed values are rounded to the nearest “bucket/transition rate” as outlined in the table Supported TON_DELAY Values:

Table 11. Supported TON_DELAY Values

EFFECTIVE TON_DELAY (ms)	PROGRAMMED TON_DELAY MANTISSA (dec)	
	Greater than	Less than or equal to
0 (50 us)		0
1	0	1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22
27	22	32
37	32	44
52	44	62
72	62	86
100	86	

8.6.30 TON_RISE (61h)

The TON_RISE command sets the time in milliseconds, from when the reference starts to rise until the voltage has entered the regulation band. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

Programming a value of 0 instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible. For TPS544x25, this results in an effective TON_RISE time of 1ms (fastest time supported).

If the Soft-Start Detection feature is being used (bit in MFR_??), then the Mantissa value decoded or derived by from the appropriate SS resistor writes into the TON_RISE register as the initial default. Note: This write overwrites any value restored from the EEPROM restore operation at initial power-up.

TON_RISE should always be set less than the TON_MAX_FAULT_LIMIT. Attempting to write a value to TON_RISE greater than TON_MAX_FAULT_LIMIT is not accepted and causes the device to set the ’cml’ bit in the STATUS_BYTE and the ‘ivd’ bit in the STATUS_CML registers and asserts the SMBALERT signal.

There is one exception to this rule: when TON_MAX_FAULT_LIMIT is set to 0. This indicates that the TON_MAX_FAULT timer is disabled, which means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely. If TON_MAX_FAULT_LIMIT = 0 (disabled), the relational cross check against TON_MAX_FAULT_LIMIT is also disabled.

The TON_RISE command is formatted as a linear mode two’s complement binary integer.

COMMAND	TON_RISE															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

8.6.30.1 Exponent

default: 00000 (bin) 0 (dec) (1 millisecond)

These default settings are not programmable.

8.6.30.2 Mantissa

The upper four bits are fixed at 0. The lower seven bits are programmable with a default value of 000 0000 0101 (bin) (5 ms).

The supported TON_RISE times over PMBus are shown in Table 12:

Table 12. Supported TON_RISE Values

Effective TON_RISE (ms)	Programmed TON_RISE Mantissa (d)	
	Greater than	Less than or equal to
1		1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22
27	22	32
37	32	44
52	44	62
72	62	86
100	86	

8.6.31 TON_MAX_FAULT_LIMIT (62h)

The TON_MAX_FAULT_LIMIT command sets an UPPER limt in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. The time begins counting as soon as the device enters the soft-start state begins to ramp the output. In other words, the TON_MAX_FAULT_LIMIT timer starts at the beginning of the TON_RISE state.

The TON_MAX_FAULT_LIMIT should always be set greater than the TON_RISE. Attempting to write a value to TON_MAX_FAULT_LIMIT less than TON_RISE is not accepted and causes the device to set the 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the STATUS_CML registers and asserts the SMBALERT signal.

There is one exception to this rule: when TON_MAX_FAULT_LIMIT is set to 0. This setting indicates that the TON_MAX_FAULT timer is disabled, which means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely. If TON_MAX_FAULT_LIMIT = 0 (disabled), the relational cross check against TON_MAX_FAULT_LIMIT is also disabled.

The TON_MAX_FAULT_LIMIT command is formatted as a linear mode two's complement binary integer.

COMMAND	TON_MAX_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

8.6.31.1 Exponent

default: 00000 (bin) 0 (dec) (1 millisecond)

These default settings are not programmable.

8.6.31.2 Mantissa

The upper four bits are fixed at 0. The lower seven bits are programmable with a default value of 000 0110 0100 (bin) (100 ms).

Even though this register is not EEPROM backed, a RESTORE_DEFAULT_ALL command causes the TON_MAX_FAULT_LIMIT to restore to the default 100 ms value.

The supported TON_MAX_FAULT_LIMIT times over PMBus are shown in Supported TON_MAX_FAULT_LIMIT Values:

Table 13. Supported TON_MAX_FAULT_LIMIT Values

Effective TON_MAX_FAULT_LIMIT (ms)	Programmed TON_MAX_FAULT_LIMIT Mantissa (d)	
	Greater than	Less than or equal to
No Limit (timer disabled)		0
1	0	1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22
27	22	32
37	32	44
52	44	62
72	62	86
100	86	

8.6.32 TON_MAX_FAULT_RESPONSE (63h)

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to an TON_MAX_FAULT_LIMIT.

The device also:

- Sets the oth bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the TONMAXF bit in the STATUS_VOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

Bits [2:0] are hard-wired to 0x7 (111b) to indicate the 7 × TON_RISE time delay in response to a TON_MAX_FAULT.

The default response to a TON_MAX_FAULT is to shut down and restart with 7 × TON_RISE time delay.

COMMAND	TON_MAX_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r/w^E	r/w	r/w	r	r	r
Function	RSP[1]	0	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	1	0	1	1	1	1	1	1

8.6.32.1 RSP[1]

This bit sets the TON_MAX_FAULT **re**s**p**onse to either ignore or not. Default is 1.

0: The PMBus device continues operation without interruption. Note: In this “ignore” fault response mode, the associated fault status bits are set. Additionally, SMBALERT continues to be triggered if it is not masked.

1: The PMBus device shuts down and restarts according to RS[2:0].

8.6.32.2 RS[2:0]

These bits are TON_MAX_FAULT **r**etry **s**etting. Default is 111b.

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert SMBALERT along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Note, that since all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

8.6.33 TOFF_DELAY (64h)

The TOFF_DELAY command sets the time in milliseconds, from when a stop condition is received and when the output voltage starts to fall. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

The TOFF_DELAY command is formatted as a linear mode two’s complement binary integer.

COMMAND	TOFF_DELAY															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.33.1 Exponent

default: 00000 (bin) 0 (dec) (1 millisecond)

These default settings are not programmable.

8.6.33.2 Mantissa

The upper four bits are fixed at 0. The lower seven bits are programmable with a default value of 000 0000 0000 (bin) (0 ms).

Only 16 fixed TOFF_DELAY times are available in the device. As such, the range of programmed TOFF_DELAY settings are sub-divided into 16 “buckets” that then selects one of the 16 supported times. Programmed values are rounded to the nearest “bucket/transition rate” as outlined in the table Supported TOFF_DELAY Values:

Table 14. Supported TOFF_DELAY Values

EFFECTIVE TOFF_DELAY (ms)	PROGRAMMED TOFF_DELAY MANTISSA (dec)	
	Greater than	Less than or equal to
0		0
1	0	1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22
27	22	32
37	32	44
52	44	62
72	62	86
100	86	

8.6.34 TOFF_FALL (65h)

The TOFF_FALL command sets the time in ms, from the end of the TOFF_DELAY time until the voltage reaches 0 V. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

Programming a value of 0 instructs the unit to bring its output voltage down to 0 as quickly as possible. For TPS544x25, this results in actively ramping down the output voltage in 1 ms (the fastest supported ramp down).

The TOFF_FALL command is formatted as a linear mode two's complement binary integer.

COMMAND	TOFF_FALL															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.34.1 Exponent

default: 00000 (bin) 0 (dec) (1 millisecond)

These default settings are not programmable.

8.6.34.2 Mantissa

The upper four bits are fixed at 0. The lower seven bits are programmable with a default value of 000 0000 0000 (bin) (0 ms).

The supported TOFF_FALL times over PMBus are shown in Supported TOFF_FALL Values:

Table 15. Supported TOFF_FALL Values

Effective TOFF_FALL (ms)	Programmed TOFF_FALL Mantissa (d)	
	Greater than	Less than or equal to

Table 15. Supported TOFF_FALL Values (continued)

Effective TOFF_FALL (ms)	Programmed TOFF_FALL Mantissa (d)	
1		1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22
27	22	32
37	32	44
52	44	62
72	62	86
100	86	

8.6.35 STATUS_BYTE (78h)

The STATUS_BYTE command returns one byte of information with a summary of the most critical device faults.

COMMAND	STATUS_BYTE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	OVF	OCF	X	OTFW	CML	oth
Default Value	0	X	0	0	0	0	0	1

A "1" in any of these bit positions indicates that:

OFF:

The device is not providing power to the output, regardless of the reason. In this family of devices, this flag means that the converter is not enabled.

OVF:

An output overvoltage fault has occurred. This bit directly reflects the state of STATUS_VOUT[7] – OVF. If the user wants this fault sourc to be masked and not trigger $\overline{\text{SMBALERT}}$, they must do it by masking STATUS_VOUT[7]. Per the PMBus v1.2 spec sections 10.2.4 and 10.2.5, this bit is not clearable via a PMBus write. In contast, the bit is to be cleared by clearing the bit(s) in STATUS_VOUT that cause this bit to be set.

OCF:

An output over current fault has occurred. This bit directly reflect the state of STATUS_IOUT[7] – OCF. If the user wants this fault sourced to be masked and not trigger $\overline{\text{SMBALERT}}$, they must do it by masking STATUS_IOUT[7]. Per the PMBus v1.2 spec sections 10.2.4 and 10.2.5, this bit is not clearable via a PMBus write. In contrast, the bit is to be cleared by clearing the bit(s) in STATUS_IOUT that cause this bit to be set.

OTFW:

A temperature fault or warning has occurred. Check STATUS_TEMPERATURE. Per the PMBus v1.2 spec sections 10.2.4 and 10.2.5, this bit is not clearable via a PMBus write. In contast, the bit is to be cleared by clearing the bit(s) in STATUS_TEMPERATURE that cause this bit to be set.

CML:

A **C**ommunications, **M**emory or **L**ogic fault has occurred. Check STATUS_CML. Per the PMBus v1.2 spec sections 10.2.4 and 10.2.5, this bit is not clearable via a PMBus write. In contast, the bit is to be cleared by clearing the bit(s) in STATUS_CML that cause this bit to be set.

oth:

A fault or warning not listed through bits 1-7 has occurred, for example an undervoltage condition or an over current warning condition. Check other status registers. Per the PMBus v1.2 spec sections 10.2.4 and 10.2.5, this bit is not clearable via a PMBus write. In contast, the bit is to be cleared by clearing the bit(s) in STATUS_VOUT and STATUS_IOUT that cause this bit to be set. The default for this bit is 1 because the default of STATUS_INPUT[3] LOW_Vin defaulting to 1.

8.6.36 STATUS_WORD (79h)

The STATUS_WORD command returns two bytes of information with a summary of the device fault and warning conditions. The low byte is identical to the STATUS_BYTE above. The additional byte reports the warning conditions for output overvoltage and overcurrent, as well as the power good status of the converter.

COMMAND	STATUS_WORD (low byte) = STATUS_BYTE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	OVF	OCF	x	OTFW	CML	oth
Default Value	0	X	0	0	0	0	0	1

COMMAND	STATUS_WORD (high byte)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r^E	r	r	r
Function	VFW	OCFW	INPUT	MFR	PGOOD_Z	X	X	X
Default Value	0	0	X	0	X	0	0	0

A "1" in any of the high byte bit positions indicates that:

VFW:

An output voltage fault or warning has occurred (OVF or OVW or UVW or UVF or VOUT_MAX_Warning or TONMAXF). Check STATUS_VOUT. Per the PMBus v1.2 spec sections 10.2.4 and 10.2.5, this bit is not clearable via a PMBus write. In contast, the bit is to be cleared by clearing the bit(s) in STATUS_VOUT that cause this bit to be set.

OCFW:

An output current warning or fault has occurred (OCF or OCW). Check STATUS_IOUT. Per the PMBus v1.2 spec sections 10.2.4 and 10.2.5, this bit is not clearable via a PMBus write. In contast, the bit is to be cleared by clearing the bit(s) in STATUS_IOUT that cause this bit to be set.

INPUT:

INPUT fault or warning in STATUS_INPUT is present. Check STATUS_INPUT. Per the PMBus v1.2 spec sections 10.2.4 and 10.2.5, this bit is not clearable via a PMBus write. In contast, the bit is to be cleared by clearing the bit(s) in STATUS_INPUT that cause this bit to be set.

MFR:

An manufacturer specific fault/warning condition has occurred (Internal over temperature fault or VOUT_MIN_Warning). Check STATUS_MFR_SPECIFIC. Per the PMBus v1.2 spec sections 10.2.4 and 10.2.5, this bit is not clearable via a PMBus write. In contast, the bit is to be cleared by clearing the bit(s) in STATUS_MFR_SPECIFIC that cause this bit to be set.

PGOOD_Z:

Power is Not Good, and the following condition is present: output over or under voltage warning or fault, TON_MAX_FAULT, over temperature warning or fault, over current warning or fault, insufficient input voltage. Please refer to the FAULT RESPONSE table for the possible sources to trigger PGOOD_Z. The signal is unlatched and always represents the current state of the device. Unless masked, it triggers SMBALERT; however, the default for this mask bit is 1, indicating that PGOOD_z cannot trigger SMBALERT by default. The user must clear the associated SMBALERT_MASK bit if SMBALERT triggering is desired for this condition.

8.6.37 STATUS_VOUT (7Ah)

The STATUS_VOUT command returns one byte of information relating to the status of the output voltage related faults.

COMMAND	STATUS_VOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r	r
Function	OVF	OVW	UVW	UVF	VOUT_MAX_Warning	TONMAXF	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OVF:

The device has seen the output voltage rise above the output overvoltage fault threshold VOUT_OV_FAULT_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

OVW:

The device has seen the output voltage rise above the output overvoltage warn threshold VOUT_OV_WARN_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

UVW:

The device has seen the output voltage fall below the output undervoltage warn threshold VOUT_UV_WARN_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

UVF:

The device has seen the output voltage fall below the output undervoltage fault threshold VOUT_UV_FAULT_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

VOUT_MAX_Warning:

An attempt is made to program the VOUT_COMMAND in excess of the value in VOUT_MAX. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

TONMAXF:

A TON_MAX_FAULT has occurred. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

8.6.38 STATUS_IOUT (7Bh)

The STATUS_IOUT command returns one byte of information relating to the status of the output current related faults.

COMMAND	STATUS_IOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^{E}	r	r/w^{E}	r	r	r	r	r
Function	OCF	X	OCW	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OCF:

The device has seen the output current rise above the level set by IOUT_OC_FAULT_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

OCW:

The device has seen the output current rise above the level set by IOUT_OC_WARN_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

8.6.39 STATUS_INPUT (7Ch)

The STATUS_INPUT command returns one byte of information relating to the status of the converter's input related faults.

COMMAND	STATUS_INPUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w^{E}	r	r	r
Function	X	X	X	X	LOW_Vin	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

LOW_Vin:

The unit is Off due to insufficient input voltage. The bit sets when the unit powers up and stays set until the first time VIN exceeds VIN_ON. During the initial power up, LOW_Vin is not latched and does not trigger SMBALERT. Once VIN does exceed VIN_ON for the first time, any subsequent VIN < VIN_OFF events are latched, trigger SMBALERT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

8.6.40 STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the external temperature related faults.

COMMAND	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^{E}	r/w^{E}	r	r	r	r	r	r
Function	OTF	OTW	X	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OTF:

The measured external temperature value of READ_TEMPERATURE_2 is equal to or greater than the level set by OT_FAULT_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. However, once cleared, the bit is set again unless the value in READ_TEMPERATURE_2 has fallen 20°C from the OT_FAULT_LIMIT.

OTW:

The measured external temperature value of READ_TEMPERATURE_2 is equal to or greater than the level set by OT_WARN_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. However, once cleared, the bit is set again unless the value in READ_TEMPERATURE_2 has fallen 20°C from the OT_WARN_LIMIT.

8.6.41 STATUS_CML (7Eh)

The STATUS_CML command returns one byte of information relating to the status of the converter's communication related faults.

COMMAND	STATUS_CML							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r	r	r/w^{E}	r
Function	ivc	ivd	pec	mem	X	X	oth	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

ivc:

An invalid or unsupported command has been received. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

ivd:

An invalid or unsupported data has been received. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

pec:

A Packet Error Check failed. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

mem:

A fault has been detected with the internal memory. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

oth:

Some other communication fault or error has occurred. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

8.6.42 STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command returns one byte of information relating to the status of manufacturer-specific faults or warnings.

COMMAND	STATUS_MFR_SPECIFIC							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^{E}	r	r	r/w	r/w	r	r/w^{E}	r
Function	otfi	illzero	illmany1s	iv_vset	iv_ss	reset_vout	VOUT_MIN_Warning	X

COMMAND	STATUS_MFR_SPECIFIC							
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

otfi:

The internal temperature is above the thermal shutdown (TSD) fault threshold. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

illzero:

The operation FSM has hit an illegal “ZERO” state. The FSM is a one-hot implementation, so all zeros in the state is illegal and should never occur. This event is informational only and would not trigger SMBALERT.

illmany1s:

The operation FSM for has hit an illegal “more than one hot” state. The FSM is a one-hot implementation, so a state where multiple state bits are HI is illegal and should never occur. This event is informational only and would not trigger SMBALERT.

iv_vset:

the VSET detection results in an “illegal high”. This condition is intended as “information only” - and does not trigger SMBALERT. To avoid initial turn-on events from clearing this condition and the user not being aware why the default vset value was used, this bit is only clearable via the CLEAR_FAULTS command or writing a logic 1 to this bit. Off and on events do not clear it as with the other, standard status bits.

iv_ss:

the TON_RISE/SS detection results in an “illegal low” or an “illegal high”. This condition is intended as “information only” - and does not trigger SMBALERT. To avoid initial turn-on events from clearing this condition and the user not being aware why the default vset value was used, this bit is only clearable via the CLEAR_FAULTS command or writing a logic 1 to this bit. Off and on events do not clear it as with the other, standard status bits.

reset_vout:

The SYNC/RESET_B pin voltage is low and the device is requested to reset the output voltage to the initial boot-up voltage set by VSET resistor. This event is informational only and would not trigger SMBALERT.

VOUT_MIN_Warning:

an attempt is made to program the output voltage below the value in (A4h) MFR_VOUT_MIN. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

8.6.43 READ_VOUT (8Bh)

The READ_VOUT commands returns two bytes of data in the linear data format that represent the output voltage of the controller. The output voltage is sensed at the remote sense amplifier output pin so voltage drop to the load is not accounted for. The data format is as shown below:

COMMAND	READ_VOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.43.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95mV/count, specified in VOUT_MODE command).

8.6.43.2 Mantissa

The output voltage calculation is shown below.

$$V_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \quad (8)$$

8.6.44 READ_IOUT (8Ch)

The READ_IOUT commands returns two bytes of data in the linear data format that represent the output current of the converter. The average output current is sensed according to the method described in Low-Side MOSFET Current Sensing and Overcurrent Protection. The data format is as shown below:

COMMAND	READ_IOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

The device scales the output current before it reaches the internal analog to digital converter so that resolution of the output current read is 62.5 mA. The maximum value that can be reported is 40 A. The user must set the IOUT_CAL_OFFSET parameter correctly in order to obtain accurate results. Calculate the output current using Equation 9.

$$I_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \quad (9)$$

8.6.44.1 Exponent

default: 11100 (bin) -4 (dec) (62.5 mA lsb)

These default settings are not programmable.

8.6.44.2 Mantissa

The lower 10 bits are the result of the ADC conversion of the average output current, as indicated by the output of the internal current sense amplifier. The 11th bit is fixed at 0 because only positive numbers are considered valid. Any computed negative current is reported as 0 A.

8.6.45 READ_TEMPERATURE_2 (8Eh)

The READ_TEMPERATURE_2 command returns the external temperature in degrees Celsius.

COMMAND	READ_TEMPERATURE_2															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1

8.6.45.1 Exponent

default: 00000 (bin) 0 (dec)

These default settings are not programmable.

8.6.45.2 Mantissa

The lower 11 bits are the result of the ADC conversion of the external temperature.

The default reading is 000 00011001 (bin) 25 (dec), corresponding to a temperature of 25°C.

NOTE

The READ_TEMPERATURE_2 (8Eh) value remains at 25°C when SS_DET_DIS in OPTIONS (MFR_SPECIFIC_21) (E5h) is set to 0 since the TSNS/SS pin is configured to set TON_RISE time and not used for external temperature sensing.

8.6.46 PMBUS_REVISION (98h)

The PMBUS_REVISION command returns a single, unsigned binary byte that indicates that these devices are compatible with the 1.2 revision of the PMBus™ specification.

COMMAND	PMBUS_REVISION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Default Value	0	0	0	1	0	0	1	0

8.6.47 MFR_VOUT_MIN (A4h)

The MFR_VOUT_MIN command sets the minimum output voltage. The purpose is to protect the device(s) on the output rail supplied by this device from a lower than acceptable output voltage. MFR_VOUT_MIN imposes a lower bound to any attempted output voltage setting:

- programmed VOUT_COMMAND
- VSET pin default

If any attempt is made to program the output voltage (using the VOUT_COMMAND) below the value in MFR_VOUT_MIN, the device also:

- Clamps the output voltage at the programmed MFR_VOUT_MIN value
- Sets the oth (other) bit in the STATUS_BYTE
- Sets the MFR bit in the STATUS_WORD
- Sets the VOUT_MIN_Warning bit in the STATUS_MFR_SPECIFIC register, and
- Notifies the host via the SMBALERT pin.

The exponent is set by VOUT_MODE at –9 (equivalent of 1.953 mV/count). The programmed output voltage is computed as:

$$\text{Minimum } V_{OUT} \text{ allowed} = \text{MFR\_VOUT\_MIN} \times \text{VOUT\_MODE (V)} = \text{MFR\_VOUT\_MIN} \times 2\text{-}9 \text{ (V)} \quad (10)$$

There are 2 “invalid data” situations that are possible and checked in hardware. They are handled differently:

- If the commanded MFR_VOUT_MIN is outside the valid data range for the VOUT_SCALE_LOOP configured, but, is still relationally correct (below VOUT_COMMAND), then that value is not accepted; but, MFR_VOUT_MIN is set to the lowest allowed value.
- The second case is the opposite, where the attempted write value is within the absolute range of MFR_VOUT_MIN; but, is not relationally correct (it is above VOUT_COMMAND). In this case, the MFR_VOUT_MIN remains unchanged.

Both cases equally cause the device to set the ’cml’ bit in the STATUS_BYTE and the ‘ivd’ bit in the STATUS_CML registers, and triggers SMBALERT signal.

COMMAND	MFR_VOUT_MIN															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															

8.6.47.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95mV/count, specified in VOUT_MODE command).

8.6.47.2 Mantissa

The range of valid MFR_VOUT_MIN values is dependent upon the configured (29h) VOUT_SCALE_LOOP as follows.

If VOUT_SCALE_LOOP = 1:

- default: 0000 0001 0000 0000 (bin) 256 (dec) (equivalent Vout default = 0.5V)
- Minimum : 0000 0001 0000 0000 (bin) 256 (dec) (equivalent VOUT_MAX = 0.5V)
- Maximum: 0000 0010 1110 0110 (bin) 742 (dec) (equivalent VOUT_MAX = 1.45V)

If VOUT_SCALE_LOOP = 0.5:

- default: 0000 0010 0000 0000 (bin) 512 (dec) (equivalent Vout default = 1V)
- Minimum : 0000 0010 0000 0000 (bin) 512 (dec) (equivalent VOUT_MIN = 1V)
- Maximum: 0000 0101 1100 1100 (bin) 1484 (dec) (equivalent VOUT_MIN = 2.9V)

If VOUT_SCALE_LOOP = 0.25:

- default: 0000 0100 0000 0000 (bin) 1024 (dec) (equivalent Vout default = 2V)
- Minimum : 0000 0100 0000 0000 (bin) 1024 (dec) (equivalent VOUT_MIN = 2V)
- Maximum: 0000 1011 1001 1000 (bin) 2968 (dec) (equivalent VOUT_MIN = 2.9V)

8.6.48 IC_DEVICE_ID (ADh)

This Read-only Block Read command returns a single word (16 bits) with the unique Device Code identifier for each device for which this IC can be configured. The BYTE_COUNT field in the Block Read command is 2 (indicating 2 bytes follow): **Low Byte first, then High Byte**.

COMMAND	IC_DEVICE_ID															
Format	Linear, binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Default Value	See below															

Device Identifier Code default:

- 0027h – Code Identifier for TPS544C25 – 30A device
- 0028h – Code Identifier for TPS544B25 – 20A device

8.6.49 IC_DEVICE_REV (AEh)

This Read-only Block Read command returns a single word (16 bits) with the unique Device revision identifier. The DEVICE_REV starts at 0 with the first silicon and is incremented with each subsequent silicon revision. The BYTE_COUNT field in the Block Read command is 2 (indicating 2 bytes follow): **Low Byte first, then High Byte**.

COMMAND	IC_DEVICE_REV															
Format	Linear, tbinary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

COMMAND	IC_DEVICE_REV
Default Value	See below

Device Identifier Code default:

- 0000b

8.6.50 MFR_SPECIFIC_00 (D0h)

The MFR_SPECIFIC_00 register is dedicated as a user scratch pad. Only the lower 8 bits are writeable for users. This is a read word command, with only the lower 8 bits accessible. Note it's NOT a read byte command. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

COMMAND	MFR_SPECIFIC_00															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	User scratch pad															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.51 OPTIONS (MFR_SPECIFIC_21) (E5h)

The OPTIONS register can be used for setting user selectable options, as shown below. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

COMMAND	OPTIONS															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w	r/w	r/w^{E}	r/w^{E}	r/w^{E}
Function	X	X	X	X	X	X	X	SS_DET_DIS	EN_AUTO_ARA	AVG_PROG[1:0]		DLO	VSM	EN_ADC_CNTL	PMB_VTH	PMB_HI_LO
Default Value	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1

8.6.51.1 PMB_HI_LO

This bit forces PMB rail logic levels.

- 0: Force 3V/5V logic thresholds.
- 1: Force 1.8V logic thresholds.

8.6.51.2 PMB_VTH

This bit configures automatic PMBus logic level detection.

- 0: No automatic bus detection occurs.
- 1: Allow the automatic bus detection to occur – VTH can result in 3V/5V or 1.8V depending upon comparator output.

PMB_VTH	PMB_HI_LO	BUS DETECTION COMPARATOR (< 2.4 V)	VSET_USED	FINAL VTH
0	0	X	X	3V/5V
0	1	X	X	1.8V
1	X	0	0	3V/5V
1	X	0	1	1.8V
1	X	1	X	1.8V

8.6.51.3 EN_ADC_CNTL

This bit enables ADC operation used for voltage, current and temperature monitoring.

- 0: Disable ADC operation.
- 1: Enable ADC operation.

NOTE

The EN_ADC_CNTL bit must be set in order to enable output voltage, current and temperature telemetry. When the EN_ADC_CNTL bit is zero, the READ_VOUT, READ_IOUT and READ_TEMPERATURE_2 registers do not update continuously, and retain their previous values from the last time EN_ADC_CNTL was set.

8.6.51.4 VSM

This bit configures the measurement system for fast, vout-only measurement mode. Setting this bit disables READ_IOUT, and READ_TEMPERATURE_2, and insteasd allows the device to update READ_VOUT more frequently. This bit does not have EEPROM backup.

- 0: Measure Vout, Temperature, and Iout.
- 1: Measure only Vout.

8.6.51.5 DLO

This bit allows bypassing the normal valid data checks on register writes. This feature is included for flexibility during debug to quickly generate fault conditions and/or possibly work around any data limit protection mechanisms prohibiting output voltage programming. This bit does not have EEPROM backup.

- 0: Normal PMBus data write restrictions.
- 1: Data write restrictions are overridden for the following registers: SMBALERT_MASK, VOUT_COMMAND, VOUT_SCALE_LOOP, VOUT_OV_FAULT_LIMIT, VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT, IOUT_OC_FAULT_LIMIT, IOUT_OC_WARN_LIMIT, OT_FAULT_LIMIT, OT_WARN_LIMIT, TON_MAX_FAULT_LIMIT, TON_RISE, TOFF_FALL, MFR_VOUT_MIN, VOUT_MAX, VIN_ON, VIN_OFF, and OPERATION.

NOTE

CAUTION: Users should use this bit with extreme caution. Setting this bit allows invalid data conditions to be programmed into the device which can lead to damage. Invalid data written into any register when DLO is enabled does NOT set the IVD bit; nor trigger SMBALERT. The invalid data is simply allowed to be programmed. Furthermore, invalid data programmed into a command/status register while DLO is enabled, does not trigger SMBALERT upon de-assertion of DLO. So, it is possible to exit DLO mode with invalid data in command/status registers. Use with extreme caution.

8.6.51.6 AVG_PROG[1:0]

These bits configure programmable digital measurement averaging. Bits provide programmable averaging for current (READ_IOUT), temperature (READ_TEMPERATURE_2), and voltage (READ_VOUT). The default (10b) yields 8x averaging for all three parameters; however, this default can be changed and stored in EEPROM, if necessary. Programming options are:

AVG_PROG[1:0]	ACCUMULATING AVERAGING
00b	16x
01b	0x – this ‘bypasses’ the averagers – every sample from measurement system updates corresponding READ_XXX CSR.
10b	8x
11b	32x

8.6.51.7 EN_AUTO_ARA

This bit **E**nables auto **A**lert **R**esponse **A**ddress response. When this feature is enabled, and after the device has successfully responded to an ARA transaction, the hardware automatically masks any fault source currently set from re-asserting SMBALERT. This prevents PMBus “bus hogging” in the case of a persistent fault in a device that consistently wins ARA arbitration due to its device address. In contrast, when this bit is cleared, immediate re-assertion of SMBALERT is allowed in the event of a persistent fault and the responsibility is upon the host to mask each source individually.

8.6.51.8 SS_DET_DIS

This bit Disables Soft Start Detection when set. The READ_TEMPERATURE_2 value remains at 25°C when OPTIONS (MFR_SPECIFIC_21) (E5h) is set to 0 since the TSNS/SS pin is configured to set TON_RISE time and not used for external temperature sensing.

8.6.52 MISC_CONFIG_OPTIONS (MFR_SPECIFIC_32) (F0h)

This user-accessible register is used for miscellaneous options, as shown below. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

COMMAND	MISC_CONFIG_OPTIONS															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	X	X	X	X	X	X	X	X	X	X	X	X	FORCE_SYNC	HSOC_USER_TRIM[1:0]		OV_RESP_SEL
Default Value	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

8.6.52.1 OV_RESP_SEL

This bit selects between two options for low-side FET behavior after an output overvoltage fault condition. Regardless of the setting of this bit, the low-side FET latches on when an output OV fault is detected (if the OV_FAULT_RESPONSE is not programmed to “ignore”).

- 0: the low-side FET remains on until either the part initiates a new startup of the output voltage or the CLEAR_FAULTS command is given while the part is in the “DISABLE” operational state
- 1: the low-side FET turns off as soon as the sensed output (at DIFFO pin) drops below the VOUT_UV_FAULT_LIMIT.

8.6.52.2 HSOC_USER_TRIM[1:0]

This trim is provided so that the customers can adjust the high-side overcurrent (HSOC) threshold in order to account for their application specific Vin sensing parasitics and component current handling spec requirements.

HSOC_USER_TRIM[1:0]	HSOC Change from Default
00b	0
01b	+12.5%
10b	–25%
11b	–12.5%

8.6.52.3 FORCE_SYNC

This bit configures the SYNC/RESET_B pin functions in conjunction with VSET detection.

- 0: the pin operates as RESET_B if VSET detection is valid, and SYNC otherwise.
- 1: the SYNC/RESET_B pin operates as a SYNC pin regardless of the outcome of the VSET detection.

9 Applications and Implementation

9.1 Application Information

The TPS544x25 devices are highly-integrated synchronous step-down DC-DC converters. These devices are used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 20 A or 30 A. Use the following design procedure to select key component values for this family of devices, and set the appropriate behavioral options via the PMBus™ interface.

9.2 Typical Applications

9.2.1 TPS544C25 4.5-V to 18-V Input, 0.95-V Output, 30-A Converter

Typical Applications (continued)

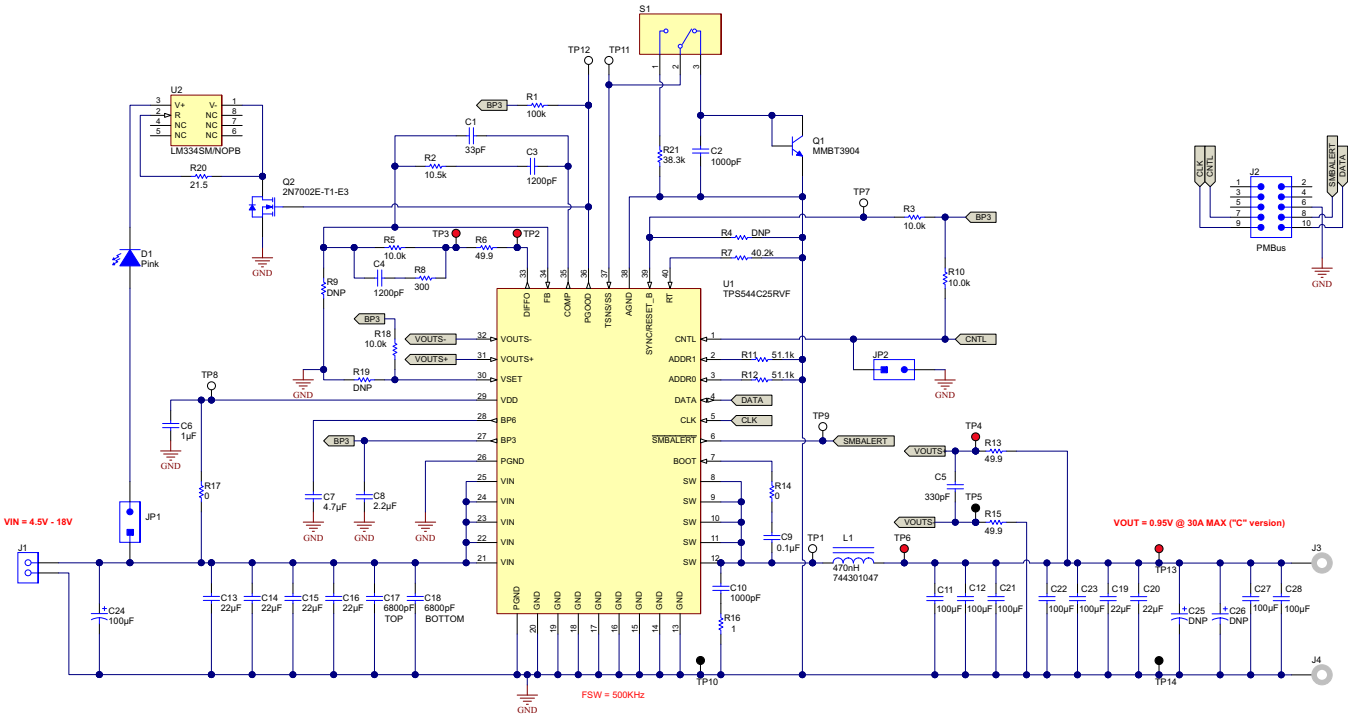


Figure 44. Typical Application Schematic

9.2.2 Design Requirements

For this design example, use the following input parameters.

Table 16. Design Example Specifications

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5	12.0	18.0	V
$V_{IN(ripple)}$	Input ripple voltage	I_{OUT} = 30 A			0.4	V
V_{OUT}	Output voltage			0.95		V
	Line regulation	4.5 V ≤ V_{IN} ≤ 18 V			0.5%	
	Load regulation	0 V ≤ I_{OUT} ≤ 30 A			0.5%	
V_{PP}	Output ripple voltage	I_{OUT} = 30 A		20		mV
V_{OVER}	Transient response overshoot	I_{STEP} = 10 A		90		mV
V_{UNDER}	Transient response undershoot	I_{STEP} = 10 A		90		mV
I_{OUT}	Output current	4.5 V ≤ V_{IN} ≤ 18 V	0	20	30	A
t_{SS}	Soft-start time	V_{IN} = 12 V		5		ms
I_{OC}	Overcurrent trip point			36	40	A
η	Peak Efficiency	I_{OUT} = 13 A, V_{IN} = 12 V		88%		
f_{SW}	Switching frequency			500		kHz

9.2.3 Design Procedure

9.2.3.1 Switching Frequency Selection

Select a switching frequency for the regulator. There is a trade off between higher and lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which decrease efficiency and impact thermal performance. In this design, a moderate switching frequency of 500 kHz achieves both a small solution size and a high-efficiency operation With the frequency selected, the timing resistor is calculated using Equation 11

$$R_T = \frac{2.01 \times 10^{10}}{f_{SW}} = \frac{2.01 \times 10^{10}}{500\ \text{kHz}} = 40.2\ \text{k}\Omega \tag{11}$$

9.2.3.2 Inductor Selection

To calculate the value of the output inductor, use Equation 12. The coefficient K_{IND} represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing a high inductor ripple current impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Generally, K_{IND} coefficient should be kept between 0.2 and 0.4 for balanced performance. Using this target ripple current, the required inductor size can be calculated as shown in Equation 12

$$L1 = \frac{V_{OUT}}{\left(V_{IN\,(max)} \times f_{SW}\right)} \times \frac{V_{IN} - V_{OUT}}{\left(I_{OUT\,(max)} \times K_{IND}\right)} = \frac{0.95\ \text{V} \times (18\ \text{V} - 0.95\ \text{V})}{(18\ \text{V} \times 500\ \text{kHz} \times 30\ \text{A} \times 0.3)} = 0.2\mu\text{H} \tag{12}$$

Selecting K_{IND} = 0.3, the target inductance L_1 = 200 nH. Using the next standard value, the 470 nH is chosen in this application for its high current rating, low DCR, and small size. The inductor ripple current, RMS current, and peak current can be calculated using Equation 13, Equation 14 and Equation 15. These values should be used to select an inductor with approximately the target inductance value, and current ratings that allow normal operation with some margin.

$$I_{RIPPLE} = \frac{V_{OUT}}{\left(V_{IN\,(max)} \times f_{SW}\right)} \times \frac{V_{IN\,(max)} - V_{OUT}}{L1} = \frac{0.95\ \text{V} \times (18\ \text{V} - 0.95\ \text{V})}{(18\ \text{V} \times 500\ \text{kHz} \times 470\ \text{nH})} = 3.83\ \text{A} \tag{13}$$

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12}(I_{RIPPLE})^2} = \sqrt{(30\ \text{A})^2 + \frac{1}{12} \times (3.83\ \text{A})^2} = 30.02\ \text{A} \tag{14}$$

$$I_{L(peak)} = (I_{OUT}) + \frac{1}{2}(I_{RIPPLE}) = 30\ \text{A} + \frac{1}{2}(3.83\ \text{A}) = 31.95\ \text{A} \tag{15}$$

The Pulse PG077.401NL is rated for 45 A_{RMS} current, and 48-A saturation. Using this inductor, the ripple current I_{RIPPLE}= 3.85 A, the RMS inductor current $I_{L(rms)}$= 30.02 A, and peak inductor current $I_{L(peak)}$= 31.92 A.

9.2.3.3 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- how the regulator responds to a change in load current or load transient
- the output voltage ripple
- the amount of capacitance on the output voltage bus

The last of these three considerations is important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

9.2.3.3.1 Response to a Load Transient

The desired response to a load transient is the first criterion. The output capacitor needs to supply the load with the required current when not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation during the transient.

In order to meet the requirements for control loop stability, the TPS544C25 requires the addition of compensation components in the design of the error amplifier. While these compensation components provide for a stable control loop, they often also reduce the speed with which the regulator can respond to load transients. The delay in the regulator response to load changes can be two or more clock cycles before the control loop reacts to the change. During that time the difference between the old and the new load current must be supplied (or absorbed) by the output capacitance. The output capacitor impedance must be designed to be able to supply or absorb the delta current while maintaining the output voltage within acceptable limits. Equation 16 and Equation 17 show the relationship between the transient response overshoot, V_{OVER}, the transient response undershoot, V_{UNDER}, and the required output capacitance, C_{OUT}.

$$V_{OVER} < \frac{(I_{TRAN})^2 \times L1}{V_{OUT} \times C_{OUT}} \qquad (16)$$

$$V_{UNDER} < \frac{(I_{TRAN})^2 \times L1}{(V_{IN} - V_{OUT}) \times C_{OUT}}$$

If

- $V_{IN(min)} > 2 \times V_{OUT}$, use overshoot to calculate minimum output capacitance.
- $V_{IN(min)} < 2 \times V_{OUT}$, use undershoot to calculate minimum output capacitance. (17)

In this case, the minimum designed input voltage $V_{IN(min)}$ is greater than $2 \times V_{OUT}$, so V_{OVER} dictates the minimum output capacitance. Therefore, using Equation 18, the minimum output capacitance required to meet the transient requirement is 285 µF.

$$C_{OUT\,(min)} = \frac{(I_{TRAN})^2 \times L1}{(V_{OUT} \times V_{OVER})} = \frac{(10\ A)^2 \times 470\ nH}{(0.95\ V \times 90\ mV)} = 550\ \mu F \qquad (18)$$

9.2.3.3.2 Output Voltage Ripple

The output voltage ripple is the second criterion. Equation 19 calculates the minimum output capacitance required to meet the output voltage ripple specification. This criterion is the requirement when the impedance of the output capacitance is dominated by ESR.

$$C_{OUT\,(min)} = \frac{I_{RIPPLE}}{(8 \times f_{SW} \times V_{OUT\,(ripple)})} = \frac{3.83\ A}{(8 \times 500\ kHz \times 20\ mV)} = 48\ \mu F \qquad (19)$$

In this case, the maximum output voltage ripple is 20 mV. Under this requirement, the minimum output capacitance for ripple (as calculated in Equation 19) yields 48 µF. Because this capacitance value is smaller than the output capacitance required to meet the transient response, select the output capacitance value based on the transient requirement. For this application, seven 100-µF low-ESR ceramic capacitors, and two 22-µF ceramic capacitors were selected to meet the transient specification with sufficient margin. Therefore C_{OUT} = 744 µF.

With the target output capacitance value chosen, Equation 20 calculates the maximum ESR the output capacitor bank can have to meet the output voltage ripple specification. Equation 20 indicates the ESR should be less than 4.9 mΩ. The ceramic capacitors each contribute approximately 3 mΩ, making the effective ESR of the output capacitor bank approximately 0.3 mΩ, meeting the specification with sufficient margin.

$$ESR_{MAX} = \frac{V_{OUT(ripple)} - \frac{I_{RIPPLE}}{(8 \times f_{SW} \times C_{OUT})}}{I_{RIPPLE}} = \frac{20mV - \frac{3.83\ A}{(8 \times 500\ kHz \times 744\ \mu F)}}{3.83\ A} = 4.9\ m\Omega \qquad (20)$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in, which increases the minimum required capacitance value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (root mean square) value of the maximum ripple current. Equation 21 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 21 yields 1.11 A.

$$I_{C(rms)} = \frac{V_{OUT} \times (V_{IN\,(max)} - V_{OUT})}{\sqrt{12} \times V_{IN\,(max)} \times f_{SW} \times L1} = \frac{0.95\ V \times (18\ V - 0.95\ V)}{\sqrt{12} \times 18\ V \times 500\ kHz \times 470\ nH} = 1.11\ A \qquad (21)$$

9.2.3.3.3 Bus Capacitance

The amount of bus capacitance is the third criterion. This requirement is optional. However, extra output bus capacitance should be considered in systems where the electrical environment is unpredictable, or not fully defined, or can be subject to severe events such as hot-plug events or even electrostatic discharge (ESD) events.

During a hot-plug event, when a discharged load capacitor is plugged into the output of the regulator, the instantaneous current demand required to charge this load capacitance is be far too rapid to be supplied by the control loop. Often the peak charging current can be multiple times higher than the current limit of the regulator. Additional output capacitance helps maintain the bus voltage within acceptable limits. For hot-plug events, the amount of required bus capacitance can be calculated if the load capacitance is known, based on the concept of conservation of charge.

An ESD event, or even non-direct lightning surges at the primary circuit level can cause glitches at this converter system level. A glitch of sufficient amplitude to falsely trip OVP or UVLO can cause several clock cycles of disturbance. In such cases it is beneficial to design in more bus capacitance than is required by the simpler load transient and ripple requirements. The amount of extra bus capacitance can be calculated based on maintaining the output voltage within acceptable limits during the disturbance. This capacitance can be as much as required to fully support the load for the duration of the interrupted converter operation.

9.2.3.4 Input Capacitor Selection

The TPS544x25 devices require a high-quality, ceramic, type X5R or X7R, input decoupling capacitor with a value of at least 0.1 µF of effective capacitance on the VDD pin, relative to AGND. The power stage input decoupling capacitance (effective capacitance at the VIN and GND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using Equation 22.

$$I_{CIN\,(rms)} = I_{OUT\,(max)} \times \sqrt{\frac{V_{OUT}}{V_{IN\,(min)}} \times \frac{\left(V_{IN\,(min)} - V_{OUT}\right)}{V_{IN\,(min)}}} = 30\ A \times \sqrt{\frac{0.95\ V}{4.5\ V} \times \frac{(4.5\ V\ -\ 0.95\ V)}{4.5\ V}}$$
$$= 12.2\ Arms \quad (22)$$

The minimum input capacitance and ESR values for a given input voltage ripple specification, $V_{IN(ripple)}$, are shown in Equation 23 and Equation 24. The input ripple is composed of a capacitive portion, $V_{RIPPLE(cap)}$, and a resistive portion, $V_{RIPPLE(esr)}$.

$$C_{IN\,(min)} = \frac{I_{OUT\,(max)} \times V_{OUT}}{V_{RIPPLE\ \ (cap)} \times V_{IN\,(max)} \times f_{SW}} = \frac{30\ A \times 0.95\ V}{100\ mV \times 18\ V \times 500\ KHz} = 32\ \mu F \quad (23)$$

$$ESR_{CIN\,(max)} = \frac{V_{RIPPLE\ (ESR)}}{I_{OUT\ \ (max)} + \frac{1}{2}(I_{RIPPLE})} = \frac{0.3\ V}{30\ A\ + \frac{1}{2}(3.83\ A)} = 9.4\ m\Omega \quad (24)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into account. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this design, allow 0.1-V input ripple for $V_{RIPPLE(cap)}$, and 0.3-V input ripple for $V_{RIPPLE(esr)}$. Using Equation 23 and Equation 24, the minimum input capacitance for this design is 32 µF, and the maximum ESR is 9.4 mΩ. For this example, four 22-µF, 25-V ceramic capacitors and one additional 100-µF, 25-V low-ESR polymer capacitors in parallel were selected for the power stage. For the VDD pin, one 1-µF, 25-V ceramic capacitor was selected. The input voltage (VDD) and power input voltage (VIN) pins must be tied together.

9.2.3.5 Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 μF must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have voltage rating of 25 V or higher.

9.2.3.6 BP6 and BP3

According to the recommendations in , BP3 is bypassed to AGND with 2.2 μF of capacitance, and BP6 is bypassed to PGND with 4.7-μF of capacitance. In order for the regulator to function properly, it is important that these capacitors be localized to the TPS544x25 , with low-impedance return paths. See for more information.

9.2.3.7 R-C Snubber and VIN Pin High-Frequency Bypass

Though it is possible to operate the TPS544x25 within absolute maximum ratings without ringing reduction techniques, some designs may require external components to further reduce ringing levels. This example uses two approaches: a high frequency power stage bypass capacitor on the VIN pins, and an R-C snubber between the SW area and GND.

The high-frequency VIN bypass capacitor is a lossless ringing reduction technique which helps minimizes the outboard parasitic inductances in the power stage, which store energy during the low-side MOSFET on-time, and discharge once the high-side MOSFET is turned on. For this example two 6.8-nF, 25-V, 0402 sized high-frequency capacitors are used. The placement of these capacitors is critical to its effectiveness. Its ideal placement is shown in .

Additionally, an R-C snubber circuit is added to this example. To balance efficiency and spike levels, a 1-nF capacitor and a 1-Ω resistor are chosen. In this example a 1206 resistor is chosen, which is rated for 0.25 W, nearly twice the estimated power dissipation. See SLUP100 for more information about snubber circuits.

9.2.3.8 Temperature Sensor

This application design uses a surface-mount MMBT3904 for the temperature sensor, Q1. In this example, the sensor monitors the PCB temperature where it is generally the highest, next to the power inductor. Placement of the temperature sensor and routing back to the TSNS pin are critical design features to reduce noise its temperature measurements. In this example, the temperature sensor is placed on the V_{OUT} side of the power inductor to avoid switching noise from the SW plane, and routed back to the TSNS and AGND pin. Additionally, a 1-nF capacitor, C2, is placed from TSNS to AGND near the TSNS pin. The READ_TEMPERATURE_2 (8Eh) register is continually updated with the digitized temperature measurement, enabling temperature telemetry.

Disable external temperature sensing by terminating TSNS to AGND with a 0 Ω resistor. This termination forces the temperature readings to –40 °C, and prevents external over-temperature fault trips.

The switch S1 in this example can be used to switch between temperature sensor and SS resistor. Note that the READ_TEMPERATURE_2 value will be kept at 25°C when SS_DET_DIS in (E5h) MFR_SPECIFIC_21 is set to 0 since the TSNS/SS pin is configured to set TON_RISE time and not used for external temperature sensing.

9.2.3.9 Key PMBus™ Parameter Selection

Several of the key design parameters for the TPS544x25 device can be configured via the PMBus interface, and stored to its non-volatile memory (NVM) for future use.

9.2.3.9.1 Enable, UVLO and Sequencing

The ON_OFF_CONFIG (02h) command is used to select the turn-on behavior of the converter. For this example, the CNTL pin was used to enable or disable the converter, regardless of the state of OPERATION (01h), as long as input voltage is present, and above the UVLO threshold.

The minimum input voltage, $V_{IN(min)}$, for this example is 4.5 V. The VIN_ON command was set to 4.5 V, and the VIN_OFF command was set to 4.0 V, giving 500 mV of hysteresis. If VIN falls below VIN_OFF, power conversion stops, until it is raised above VIN_ON.

The turn-on or turn-off delay time can be set by TON_DELAY and TOFF_DELAY. Accounting for the time during which the COMP signal rises to the valley of the PWM ramp, the delay between enabling power conversion, and the rise of the output voltage is approximately 200 μs. See *Soft-Start and TON_RISE Command* for more information.

9.2.3.9.2 Soft-Start Time

The TON_RISE command sets the soft-start time. When selecting the soft-start time, consider the charging current for the output capacitors. In some applications (e.g., those with large amounts of output capacitance) this current can lead to problems with nuisance tripping of the overcurrent protection circuitry. To avoid nuisance tripping, the output capacitor charging current should be included when choosing a soft-start time, and overcurrent threshold. The capacitor charging current can be calculated using Equation 25

$$I_{CAP} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{0.95\ V \times 744\ \mu F}{5\ ms} = 141.36\ mA \quad (25)$$

With the charging current calculated, the overcurrent threshold can then be calibrated to the sum of the maximum load current and the output capacitor charging current plus some margin.

In this example, the soft-start time is arbitrarily selected to be 5 ms. In this case, the charging current, I_{CAP} = 141.36 mA.

9.2.3.9.3 Overcurrent Threshold and Response

The IOUT_OC_FAULT_LIMIT command sets the overcurrent threshold. The current limit should be set to the maximum load current, plus the output capacitor charging current during start-up, plus some margin for load transients and component variation. The amount of margin required depends on the individual application, but a suggested starting point is between 25% and 30%. More or less may be required. For this application, the maximum load current is 30 A, the output capacitor charging current is 141 mA. This design allows some extra margin, so an overcurrent threshold of 36 A was selected.

The IOUT_OC_FAULT_RESPONSE command sets the desired response to an overcurrent event, which can be *hiccup* (continuously restart waiting for a 7 x soft-start time-out between re-trials) in the event of an overcurrent, latch-off, or continue without interruption (i.e. ignore the fault).

9.2.3.9.4 Power Good, Output Overvoltage and Undervoltage Protection

The VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT commands configure the PGOOD window, and VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT commands configure the output voltage fault limits.

The VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE command sets the desired response to an output overvoltage and undervoltage event respectively, which can be *hiccup* (continuously restart waiting for a 7 x soft-start time-out between re-trials) in the event of a fault, latch-off, or continue without interruption (i.e. ignore the fault).

Note that the VOUT_UV_FAULT_LIMIT is masked until the unit reaches the programmed output voltage. If the output voltage did not reach the programmed value during the soft start time UPPER limit required by TON_MAX_FAULT_LIMIT, the device will assert a TON_MAX fault and reponse according to TON_MAX_FAULT_RESPONSE.

9.2.3.10 Output Voltage Setting and Frequency Compensation Selection

The output voltage can be set by the resistor connected from VSET to AGND with 8 possible options to set initial boot-up output voltage ranging from 0.80 V to 1.20 V with VOUT_SCALE_LOOP = 1. The output voltage can also be set by VOUT_COMMAND through the PMBus interface .

It is required that the user program VOUT_SCALE_LOOP prior to any VOUT related commands in order for the proper range checking to work and to avoid Invalid Data scenarios. VOUT_SCALE_LOOP is equal to the feedback resistor ratio of (R9/(R5+R9)). It is limited to only 3 possible options/ratios: 1 (default, no bottom resistor required), 0.5, and 0.25.

In this design, the VSET pin is pulled up to BP3, so the VOUT_COMMAND goes to the default value of 0.95V stored in the EEPROM. No bottom feedback resistor is needed for the output voltage range of 0.5 V to 1.5V.

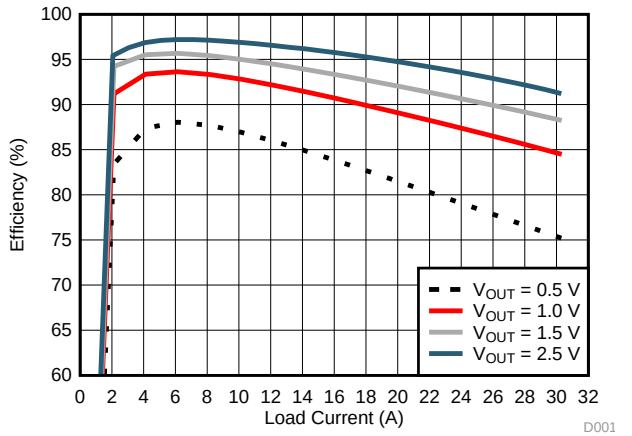
The TPS544x25 device uses voltage mode control, with input feedforward. See SLUP206 for an in-depth discussion of voltage-mode feedback and control. Frequency compensation can be accomplished using standard techniques. TI also provides a compensation calculator tool to streamline compensation design. Using the *TPS40k Loop Compensation Tool*, with 50 kHz of bandwidth, and 60 degrees of phase margin and optimizing based on measured results yields the following:

Table 17. Design Example Frequency Compensation Values

RESISTOR	VALUE (kΩ)	CAPACITOR	VALUE (pF)
R5	10.0	C4	1200
R8	0.3	C3	1200
R2	10.5	C1	33
R_{Bias}	Not Used		

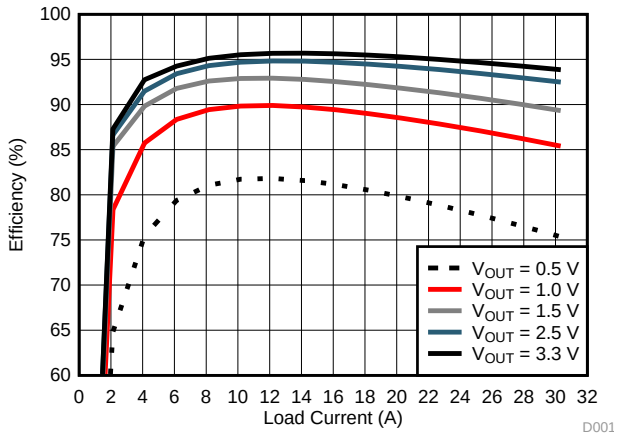
The tool provides the recommended compensation components, and approximate bode plots. As a starting point, the crossover frequency should be set to 1/10 f_{SW}, and the phase margin at crossover should be greater than 45°. The resulting plots should be reviewed for a few common issues. The error amplifier gain should not hit the error amplifier gain bandwidth product (GBWP), nor should its mid-band gain, A_{MID}, be greater than approximately 20 dB in general. Use the tool to calculate the system bode plot at different loading conditions to ensure that the phase does not drop below zero prior to crossover, as this condition is known as conditional stability.

9.2.4 Application Curves



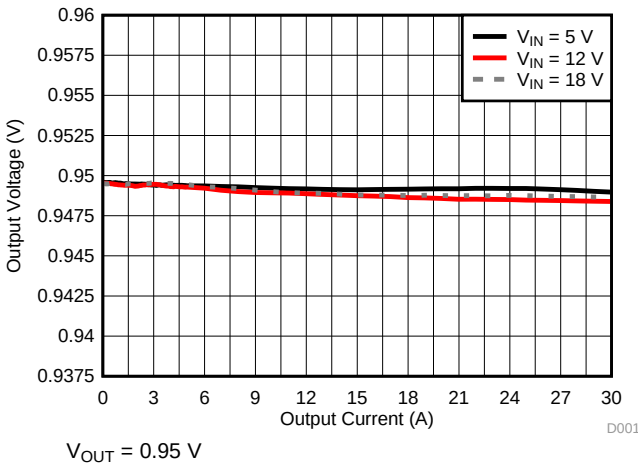
V_{IN} = 5 V f_{SW} = 500 kHz R_{BOOT} = 0 Ω
L = 470 nH No snubber R_{DCR} = 0.3 mΩ

Figure 45. Efficiency vs. Load Current



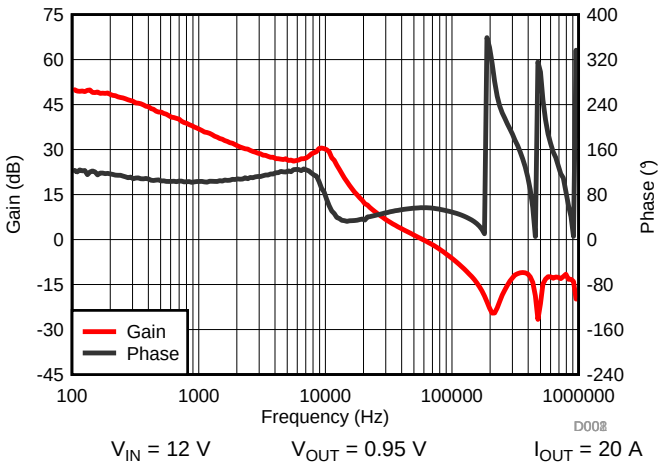
V_{IN} = 12 V f_{SW} = 500 kHz R_{BOOT} = 0 Ω
L = 470 nH No snubber R_{DCR} = 0.3 mΩ

Figure 46. Efficiency vs. Load Current



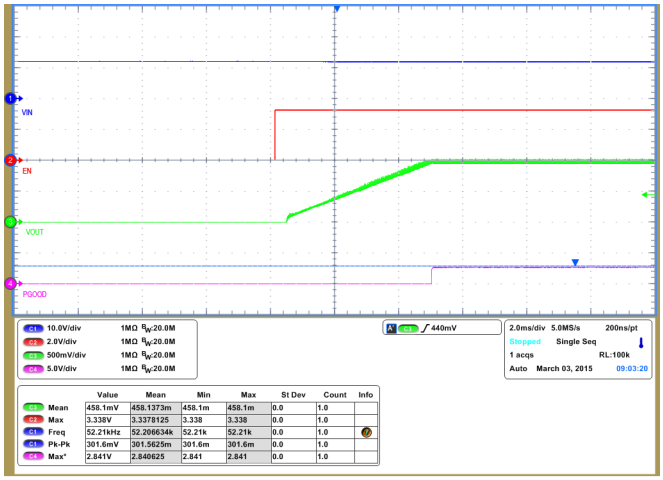
V_{OUT} = 0.95 V

Figure 47. Load Regulation



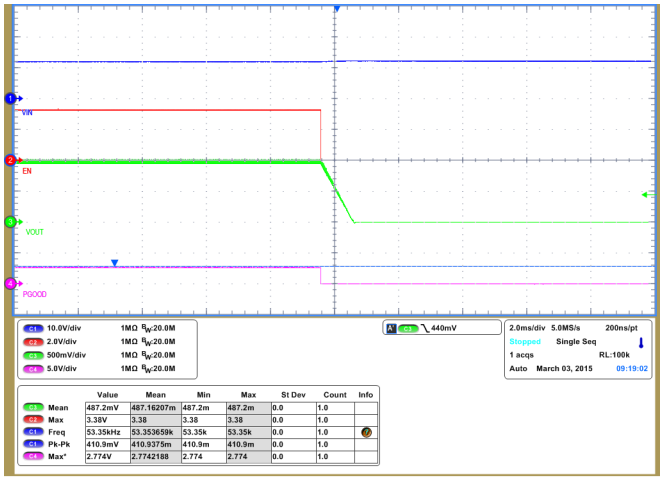
V_{IN} = 12 V V_{OUT} = 0.95 V I_{OUT} = 20 A

Figure 48. System Bode Plot



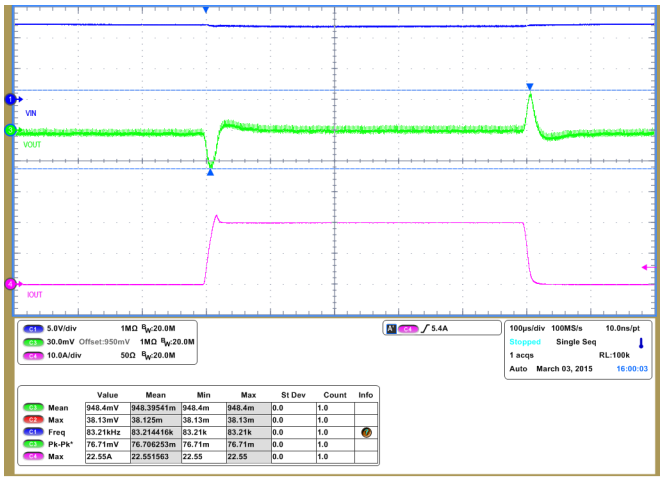
V_{IN} = 12 V V_{OUT} = 0.95 V I_{OUT} = 20 A

Figure 49. Startup from CNTL



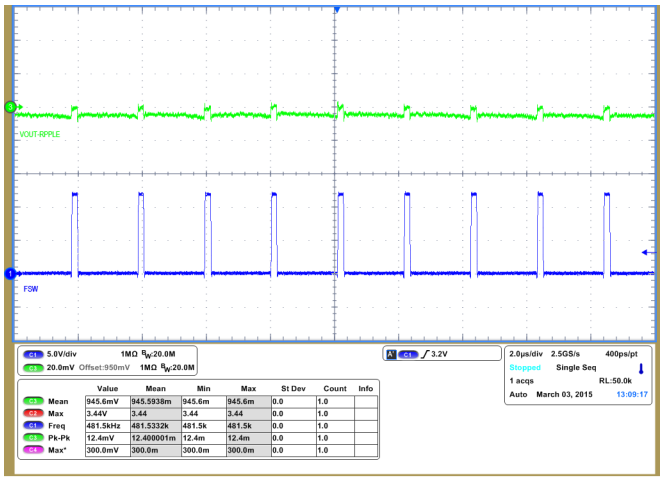
V_{IN} = 12 V V_{OUT} = 0.95 V I_{OUT} = 20 A

Figure 50. Shutdown from CNTL



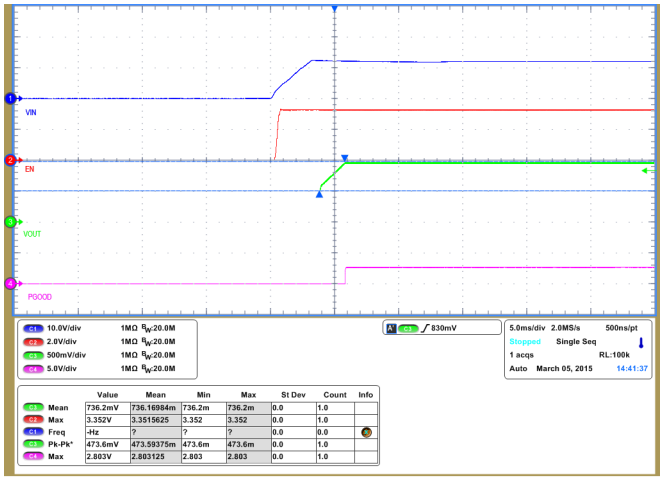
V_{IN} = 12 V V_{OUT} = 0.95 V I_{OUT} = 0 A to 20A , 2.5 A/µs

Figure 51. Transient Load



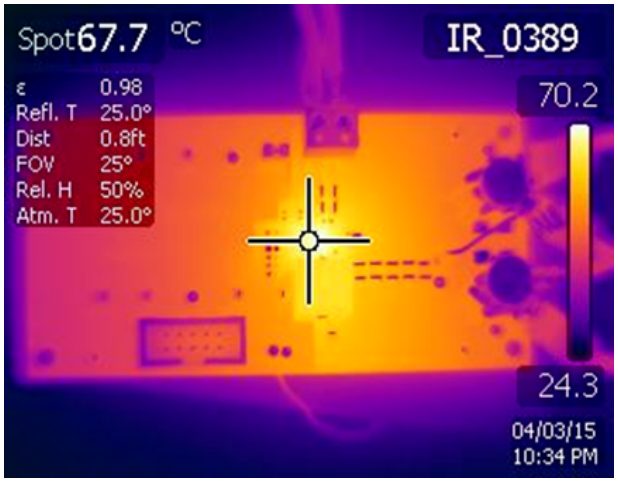
V_{IN} = 12 V V_{OUT} = 0.95 V I_{OUT} = 20 A

Figure 52. DC Ripple



V_{IN} = 12 V I_{OUT} = 0 A $V_{PRE-BIAS}$= 0.5 V

Figure 53. 50% Pre-Biased Start-Up



Natural Convection V_{OUT} = 0.95 V

V_{IN} = 12 V I_{OUT} = 20 A f_{SW} = 500 kHz

Figure 54. Thermal Image

10 Power Supply Recommendations

These devices are designed to operate from an input voltage supply between 4.5 V and 18 V. This supply must be well regulated. These devices are not designed for split-rail operation. The VIN and VDD pins must be the same potential for accurate high-side short circuit protection. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the *Layout* section.

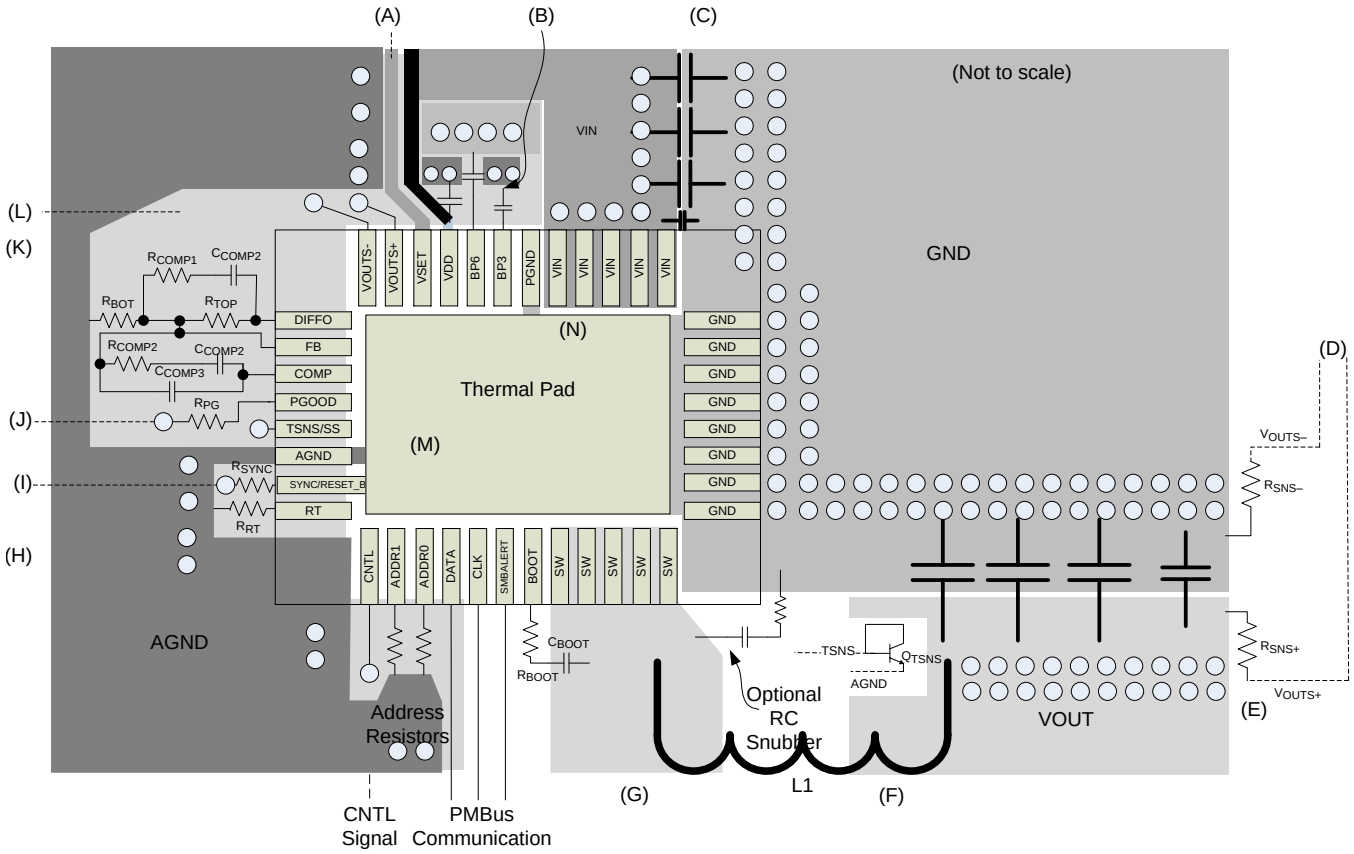
11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. Figure 55 shows the recommended PCB layout configuration. A list of PCB layout considerations using these devices are listed below.

- As with any switching regulator, there are several signal paths that conduct fast switching voltages or currents. Minimize the loop area formed by these paths and their bypass connections.
- Bypass the VIN pins to GND with a low-impedance path. Power-stage input bypass capacitors should be as close as physically possible to the VIN and GND pins. Additionally, a high-frequency bypass capacitor in 0402 package on the VIN pins can help to reduce switching spikes, which can be tucked right underneath the IC on the other side of the PCB to keep a minimum loop.
- BP6 bypass capacitor carries large switching current for gate driver. Bypassing the BP6 pin to GND with a low-impedance path is very critical to the stable operation of the TPS544x25 devices. Place BP6 high-frequency bypass capacitors as close as possible to the device pins, with a minimum return loop back to ground.
- The VDD and BP3 also require good local bypassing. Place bypass capacitors as close as possible to the device pins, with a minimum return loop back to ground and this return loop should be kept away from fast switching voltage and main current path, as well as BP6 current path. Poor bypassing on VDD and BP3 can degrade the performance of the regulator.
- Keep signal components local to the device, and place them as close as possible to the pins to which they are connected. These components include the feedback resistors, the RT resistor, the VSET resistor, the SS resistor, as well as ADDR0 and ADDR1 resistors. These components should also be kept away from fast switching voltage and current paths. Those components can be terminated to GND with minimum return loop or bypassed to a separate **low impedance** analog ground (AGND) copper area, which is isolated from fast switching voltage and current paths and has single connection to PGND on the thermal tab via AGND pin. See Figure 55 for placement recommendation.
- The PGND pin (pin 26) must be directly connected to the thermal pad of the device on the PCB, with a low-noise, low-impedance path to ensure accurate current monitoring.
- Minimize the SW copper area for best noise performance. Route sensitive traces away from SW and BOOT, as these nets contain fast switching voltages, and lend easily to capacitive coupling.
- Snubber component placement is critical to its effectiveness of ringing reduction. These components should be on the same layer as the TPS544x25 devices, and be kept as close as possible to the SW and GND copper areas.
- The VIN and VDD pins must be the same potential for accurate short circuit protection, but high frequency switching noise on the VDD pin can degrade performance. VDD should be connected to VIN through a trace from the input copper area. Optionally form a small low-pass R-C between VIN and VDD, with the VDD bypass capacitor (1 µF) and a 0-2 Ω resistor between VIN and VDD. See Figure 55.
- Route the VOUTS+ and VOUTS– lines from the output capacitor bank at the load back to the device pins as a tightly coupled differential pair. It is critical that these traces be kept away from switching or noisy areas which can add differential-mode noise.
- Routing of the temperature sensor traces is critical to the noise performance of temperature monitoring. Keep these traces away from switching areas or high current paths on the layout. It is also recommended to use a small 1-nF capacitor from TSNS/SS to AGND to improve the noise performance of temperature readings.

11.2 Layout Example



(A) Connect to AGND with setting resistor or pull up to BP3 if not used.
(B) Bypass for internal regulators BP3, BP6, VDD. Use multiple vias to reduce parasitic inductance
(C) Place VIN bypass capacitors as close as possible to device, with best high frequency capacitor closest to VIN and GND pins
(D) Kelvin connect to TPS544C25 VOUTS– and VOUTS+ pins
(E) Sense point should be directly at the load
(F) For best efficiency, use a heavy weight copper and place these planes on multiple PCB layers
(G) Minimize SW area for least noise. Keep sensitive traces away from SW and BOOT on all layers
(H) AGND and PGND are only connected together on Thermal Pad.
(I) Optional SYNC/RESET_B Signal. Pull up to BP3 if not used.
(J) Pull up to BP6 or external voltage to use PGOOD.
(K) Maintain feedback and compensation network components localized to the device.
(L) Internal AGND Plane to reduce the BP3 and VDD bypass parasitics.
(M) Connect AGND to Thermal Pad
(N) Connect PGND to Thermal Pad

Figure 55. PCB Layout Recommendation

11.2.1 Mounting and Thermal Profile Recommendation

Proper mounting technique adequately covers the exposed thermal tab with solder. Excessive heat during the reflow process can affect electrical performance. Figure 56 shows the recommended reflow oven thermal profile. Proper post-assembly cleaning is also critical to device performance. See SLUA271 for more information.

Layout Example (continued)

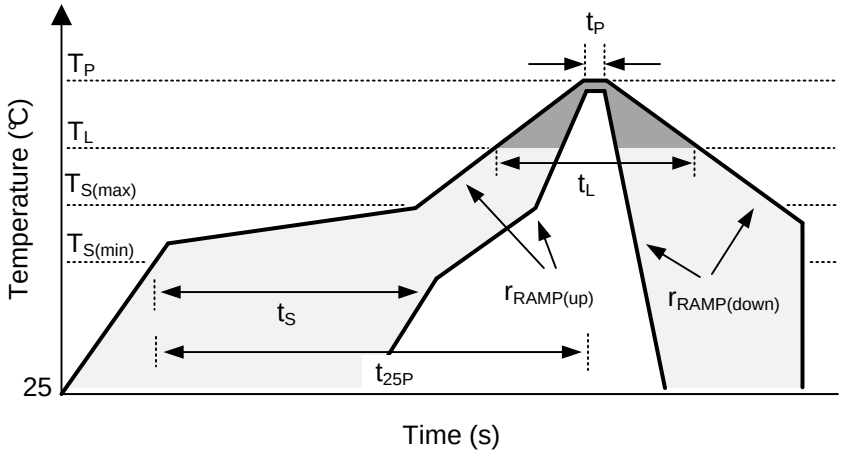


Figure 56. Recommended Reflow Oven Thermal Profile

Table 18. Recommended Thermal Profile Parameters

PARAMETER		MIN	TYP	MAX	UNIT
RAMP UP AND RAMP DOWN					
$r_{RAMP(up)}$	Average ramp-up rate, $T_{S(max)}$ to T_P			3	°C/s
$r_{RAMP(down)}$	Average ramp-down rate, T_P to $T_{S(max)}$			6	°C/s
PRE-HEAT					
T_S	Pre-heat temperature	150		200	°C
t_S	Pre-heat time, $T_{S(min)}$ to $T_{S(max)}$	60		180	s
REFLOW					
T_L	Liquidus temperature		217		°C
T_P	Peak temperature			260	°C
t_L	Time maintained above liquidus temperature, T_L	60		150	s
t_P	Time maintained within 5 °C of peak temperature, T_P	20		40	s
t_{25P}	Total time from 25 °C to peak temperature, T_P			480	s

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Texas Instruments Fusion Digital Power Designer

The TPS544x25 devices are fully supported by Texas Instruments Digital Power Designer. Fusion Digital Power Designer is a graphical user interface (GUI) which can be used to configure and monitor the devices via PMBus using a Texas Instruments USB-to-GPIO adapter.

Click this link to download the Texas Instruments Fusion Digital Power Designer software package.

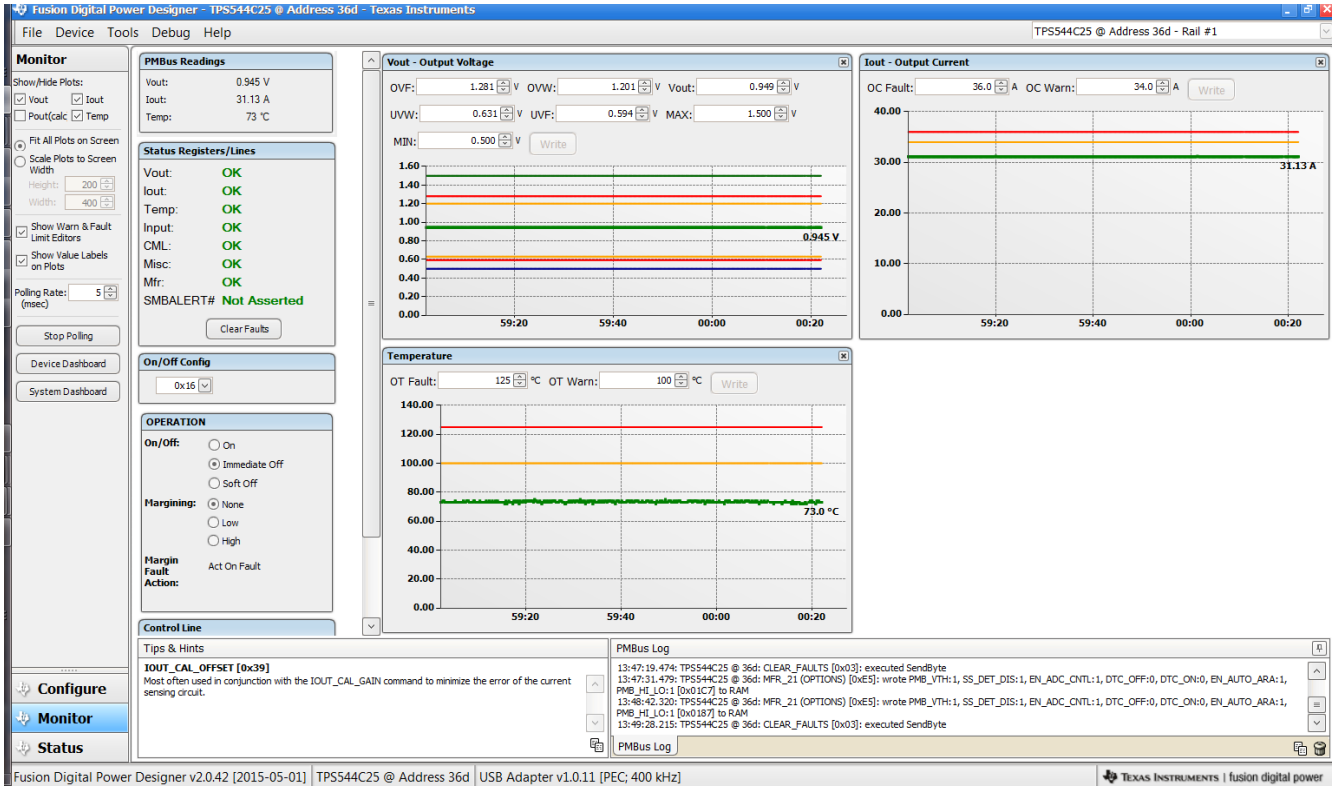


Figure 57. Device Monitoring with Fusion Digital Power Designer

Device Support (continued)

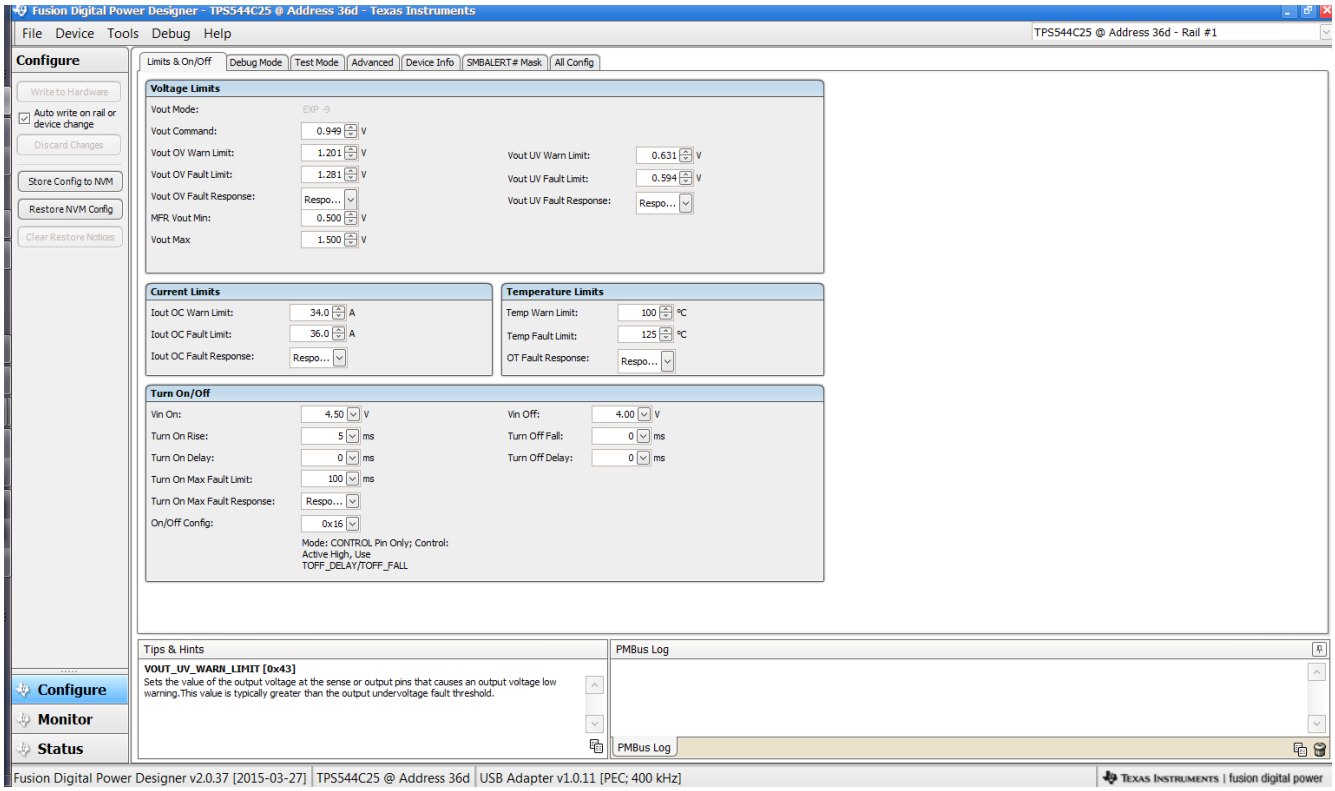


Figure 58. Device Configuration with Fusion Digital Power Designer

12.1.1.2 TPS40k Loop Compensation Tool

The TPS544x25 devices are supported by the Texas Instruments *TPS40k Loop Compensation Tool*. This spreadsheet tool can be used to calculate frequency compensation components for devices with voltage mode control.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 19. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS544C25	Click here	Click here	Click here	Click here	Click here
TPS544B25	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

SWIFT, NexFET, E2E are trademarks of Texas Instruments.
PMBus is a trademark of SMIF, Inc..
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. These data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS544B25RVFR	Active	Production	LQFN-CLIP (RVF) | 40	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544B25
TPS544B25RVFR.B	Active	Production	LQFN-CLIP (RVF) | 40	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544B25
TPS544B25RVFT	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544B25
TPS544B25RVFT.B	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544B25
TPS544B25RVFTG4.B	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544B25
TPS544C25RVFR	Active	Production	LQFN-CLIP (RVF) | 40	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544C25
TPS544C25RVFR.B	Active	Production	LQFN-CLIP (RVF) | 40	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544C25
TPS544C25RVFRG4.B	Active	Production	LQFN-CLIP (RVF) | 40	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544C25
TPS544C25RVFT	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544C25
TPS544C25RVFT.B	Active	Production	LQFN-CLIP (RVF) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS544C25

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

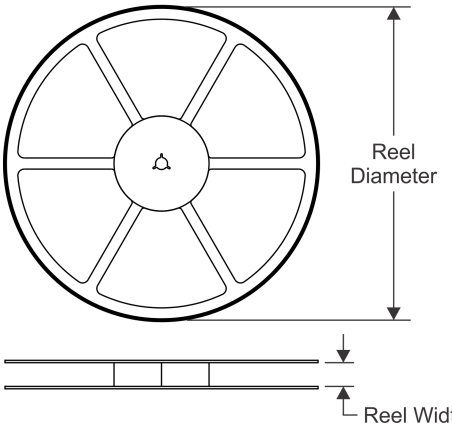
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

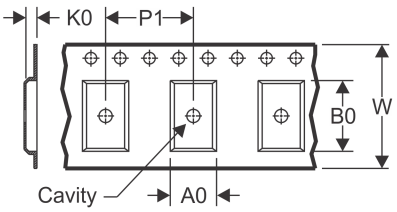
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

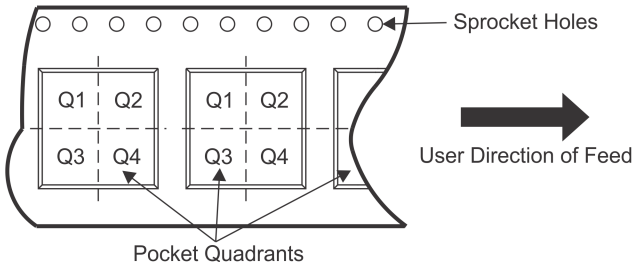


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

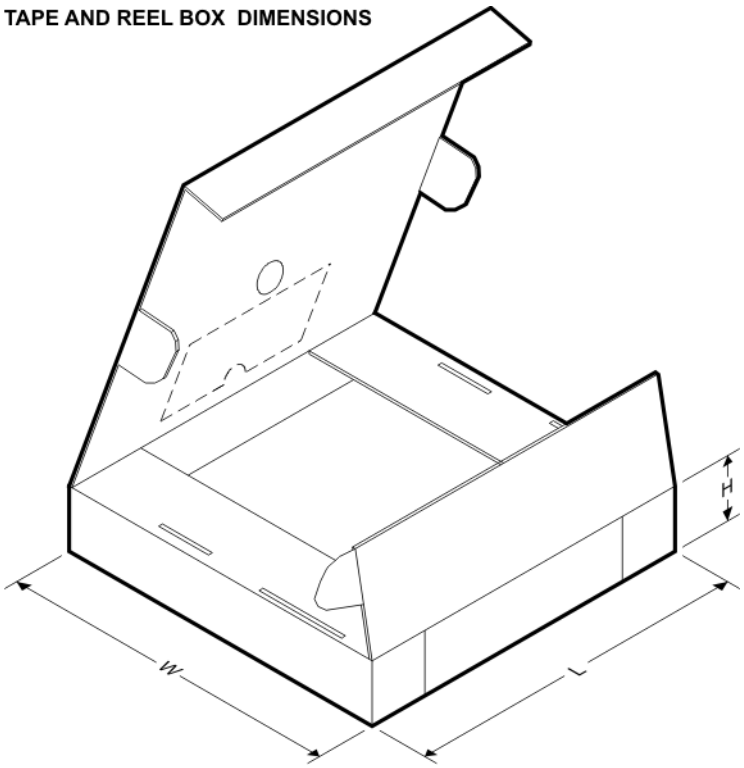
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS544B25RVFR	LQFN-CLIP	RVF	40	2500	330.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1
TPS544B25RVFT	LQFN-CLIP	RVF	40	250	180.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1
TPS544C25RVFR	LQFN-CLIP	RVF	40	2500	330.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1
TPS544C25RVFT	LQFN-CLIP	RVF	40	250	180.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

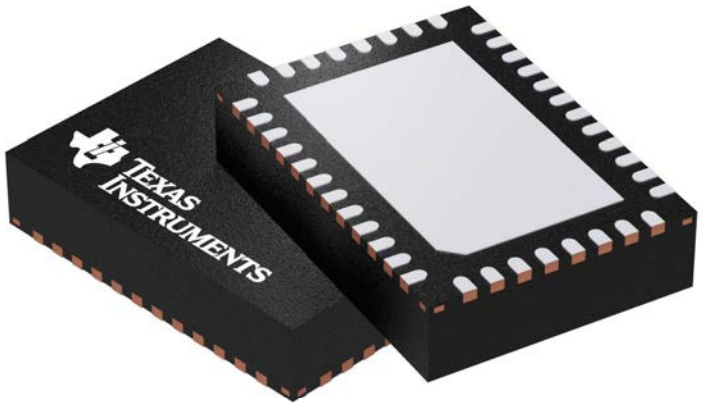


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS544B25RVFR	LQFN-CLIP	RVF	40	2500	367.0	367.0	38.0
TPS544B25RVFT	LQFN-CLIP	RVF	40	250	210.0	185.0	35.0
TPS544C25RVFR	LQFN-CLIP	RVF	40	2500	367.0	367.0	38.0
TPS544C25RVFT	LQFN-CLIP	RVF	40	250	210.0	185.0	35.0

RVF 40 LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



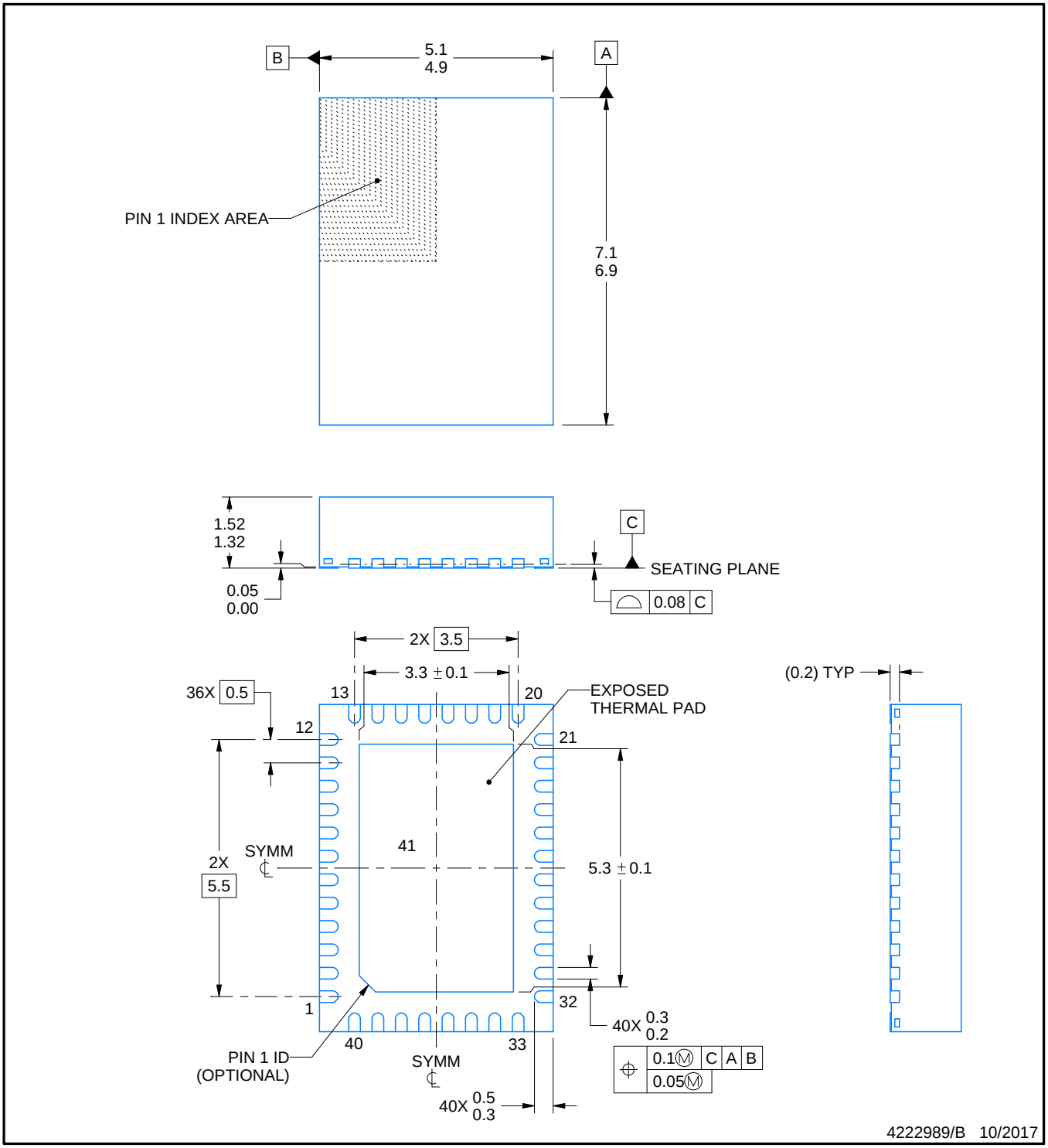
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RVF0040A

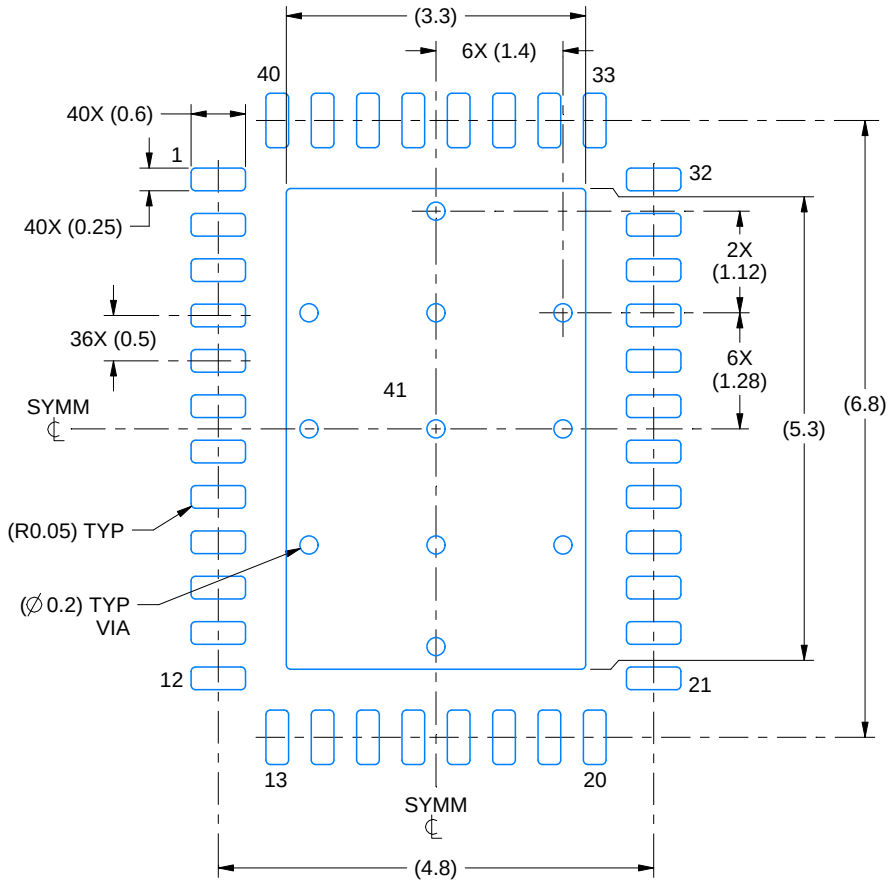
LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

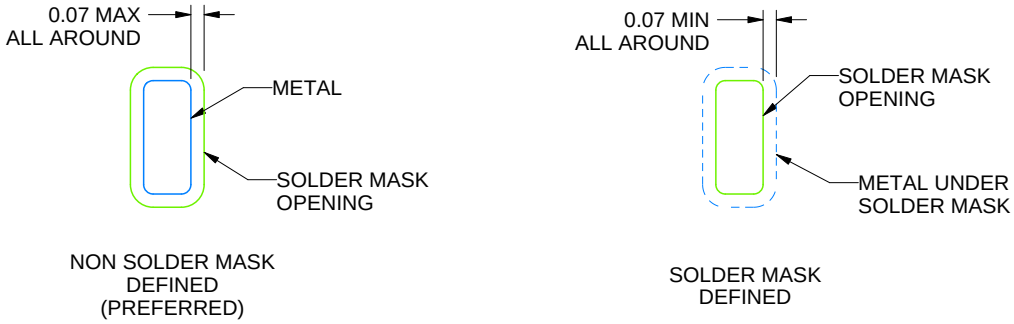


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

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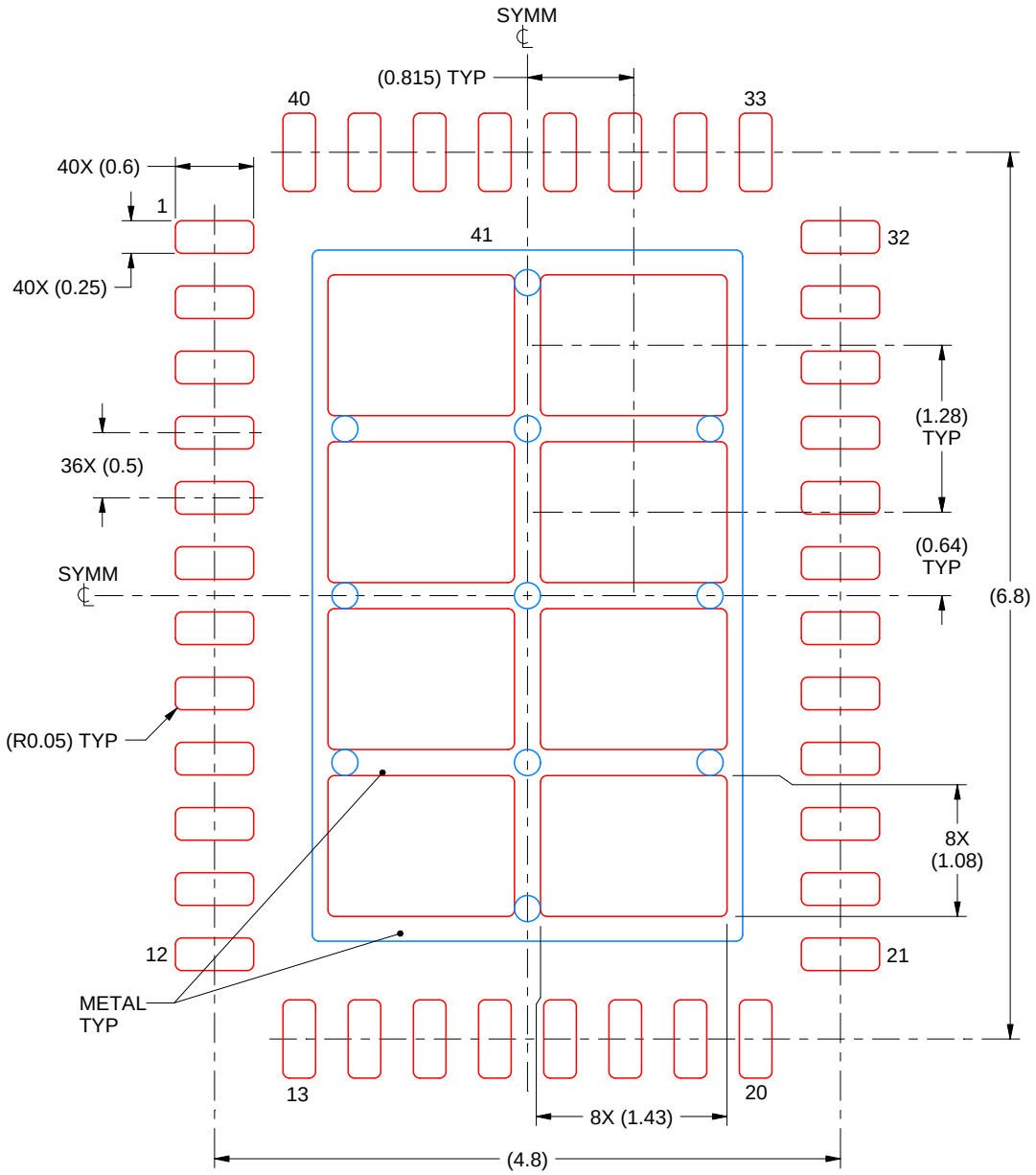
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
71% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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