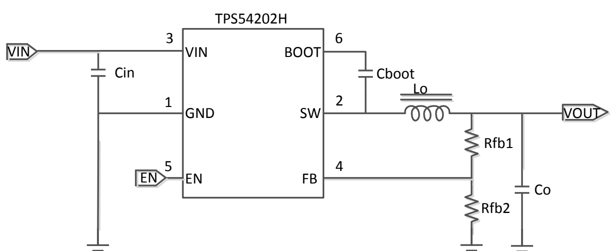
TPS54202H 4.5V～28V 入力、2A 出力、SWIFT™ 同期整流降圧型電圧コンバータ

1 特長

- 4.5V～28V の広い入力電圧範囲
- 148mΩ と 78mΩ の MOSFET を内蔵し、2A の連続出力電流に対応
- 低いシャットダウン時電流 (2μA) と静止電流 (45μA)
- 5ms のソフト・スタート内蔵
- 500kHz の固定スイッチング周波数
- 高度な Eco-mode™ パルス・スキップ
- ピーク電流モード制御
- ループ補償内蔵
- ヒカップ・モード保護機能付き、2 個の MOSFET の過電流保護
- 過電圧保護
- サーマル・シャットダウン
- SOT-23 (6) パッケージ

2 アプリケーション

- 12V、24V の分散パワー・バス電源
- 産業用アプリケーション
  - 白物家電
- 消費者向けアプリケーション
  - オーディオ
  - STB、DTV
  - プリンタ



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概略回路図

3 概要

TPS54202H は入力電圧範囲が 4.5V～28V で、2A の同期整流降圧型コンバータです。このデバイスには 2 つの内蔵スイッチング FET、内部的なループ補償、および 5ms の内部ソフトスタートが搭載されているため、部品数を減らすことができます。

TPS54202H には MOSFET が内蔵され、SOT-23 パッケージを採用しているため、高い電力密度を実現し、PCB 上でわずかな面積しか占有しません。

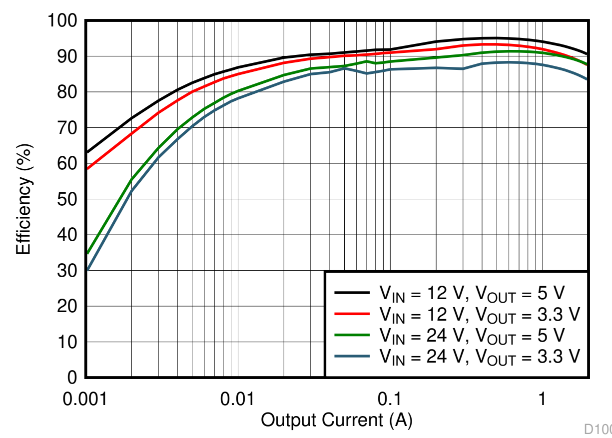
高度な Eco-mode の実装により、軽負荷時の効率が最大化され、電力損失が低減されています。

両方のハイサイド MOSFET でサイクル単位の電流制限を行い、過負荷の状況でコンバータを保護します。また、ローサイド MOSFET の電流制限を自由に設定でき、電流暴走を防止することで、さらに保護が強化されています。プリセット時間を上回る長さで過電流状態が続いた場合、ヒカップ・モード保護機能をトリガします。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS54202H	SOT-23 (6)	1.60mm × 2.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力電流との関係

English Data Sheet: SLVSDG7

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2016) to Revision A (April 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新........ 1
- Changed the max centre switching frequency from 590 kHz to 630 kHz........ 5
- Changed the max low-side source current limit from 4 A to 4.3 A........ 5

5 Pin Configuration and Functions

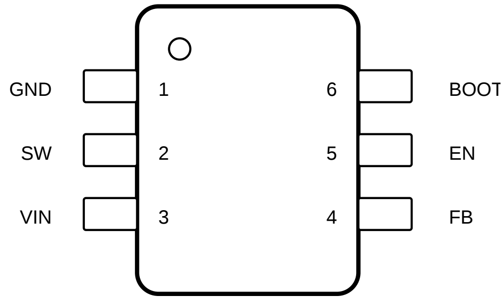


図 5-1. 6-Pin SOT-23 DDC Package (Top View)

表 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
BOOT	6	O	Supply input for the high-side NFET gate drive circuit. Connect a 0.1-µF capacitor between BOOT and SW pins.
EN	5	I	This pin is the enable pin. Float the EN pin to disable.
FB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
GND	1	–	Ground pin. Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	–	Input voltage supply pin. The drain terminal of high-side power NFET.

(1) O = Output; I = Input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Input voltage range, V_I	VIN	–0.3	30	V
	EN	–0.3	7	V
	FB	–0.3	7	V
Output voltage range, V_O	BOOT-SW	–0.3	7	V
	SW	–0.3	30	V
	SW (20 ns transient)	–5	30	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range	VIN	4.5	28	V
		EN	–0.1	7	V
		FB	–0.1	7	V
V_O	Output voltage range	BOOT-SW	–0.1	7	V
		SW	–0.1	28	V
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS54202H DDC (SOT23) 6 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	89.2	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	39.5	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	14.7	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	1.2	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	14.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, .

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_J = –40°C to +125°C, V_{IN} = 4.5 V to 28 V, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range		4.5		28	V
I_Q	Non switching quiescent current	EN =5 V, VFB = 1 V		45		µA
I_{OFF}	Shut down current	EN = GND		2		µA
$V_{IN(UVLO)}$	VIN under voltage lockout	Rising V_{IN}	3.9	4.2	4.4	V
		Falling V_{IN}	3.4	3.7	3.9	V
	Hysteresis		400	480	560	mV
ENABLE (EN PIN)						
$V_{(EN\_RISING)}$	Enable threshold	Rising		1.28	1.35	V
$V_{(EN\_FALLING)}$		Falling	1.16	1.25		V
$I_{(EN\_HYS)}$	Hysteresis current	V_{EN} = 1.5 V		1		µA
FEEDBACK AND ERROR AMPLIFIER						
V_{FB}	Feedback Voltage	V_{IN} = 12 V	0.581	0.596	0.611	V
PULSE SKIP MODE						
$I_{(SKIP)}$ (1)	Pulse skip mode peak inductor current threshold	V_{IN} = 24 V, V_{OUT} = 5 V, L = 15 µH		300		mA
POWER STAGE						
$R_{(HSD)}$	High-side FET on resistance	T_A = 25°C, V_{BST} – SW = 6 V		148		mΩ
$R_{(LSD)}$	Low-side FET on resistance	T_A = 25°C, V_{IN} = 12		78		mΩ
CURRENT LIMIT						
$I_{(LIM\_HS)}$	High side current limit	Inductor peak current	2.5	3.2	3.9	A
$I_{(LIM\_LS)}$	Low side source current limit	Inductor valley current	2	3	4.3	A
OSCILLATOR						
F_{sw}	Centre switching frequency		390	500	630	kHz
OVER TEMPERATURE PROTECTION						
Thermal Shutdown (1)	Rising temperature			155		°C
	Hysteresis			10		°C
	Hiccup time			32768		Cycles

(1) Not production tested

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
OVER CURRENT PROTECTION					
t_{HIC_WAIT}	Hiccup up wait time		512		Cycles
$t_{HIC\_RESTART}$	Hiccup up time before restart		16384		Cycles
t_{SS}	Soft-start time		5		mS
ON TIME CONTROL					
t_{MIN_ON} (1)	Minimum on time, measured at 90% to 90% and 1-A loading		110		ns

Typical Characteristics

V_{IN} = 12, unless otherwise specified

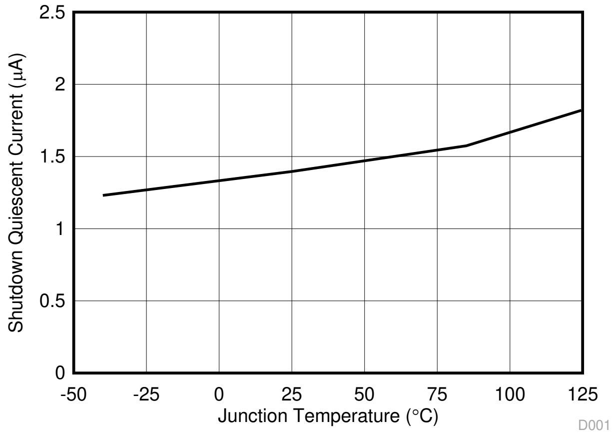


図 6-1. Shutdown Quiescent Current vs Junction Temperature

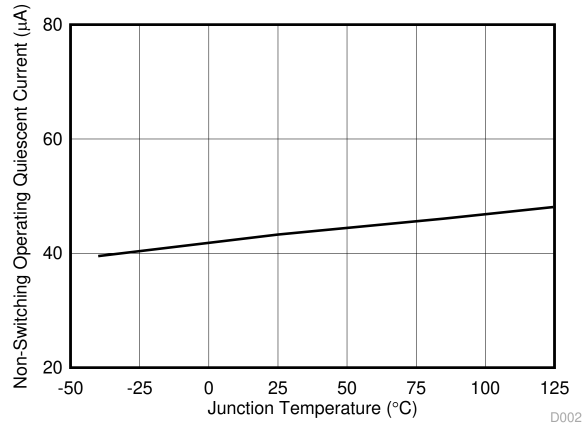


図 6-2. Non-Switching Operating Quiescent Current vs Junction Temperature

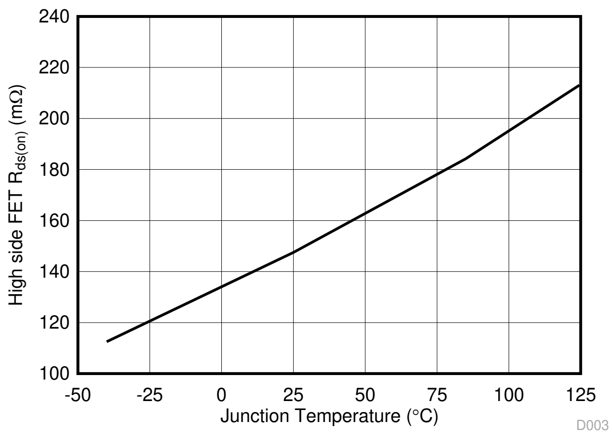


図 6-3. High-Side Resistance vs Junction Temperature

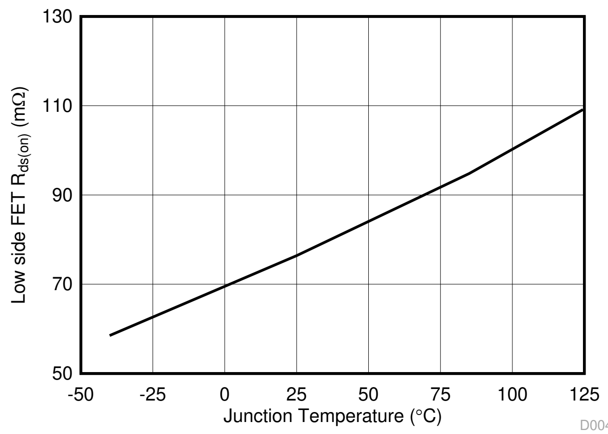


図 6-4. Low-Side FET On Resistance vs Junction Temperature

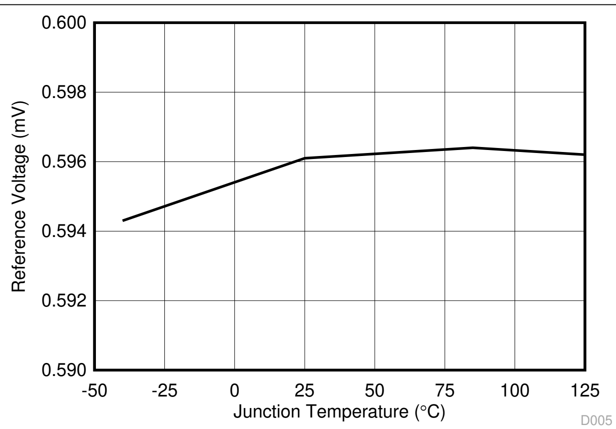


図 6-5. Reference Voltage vs Junction Temperature

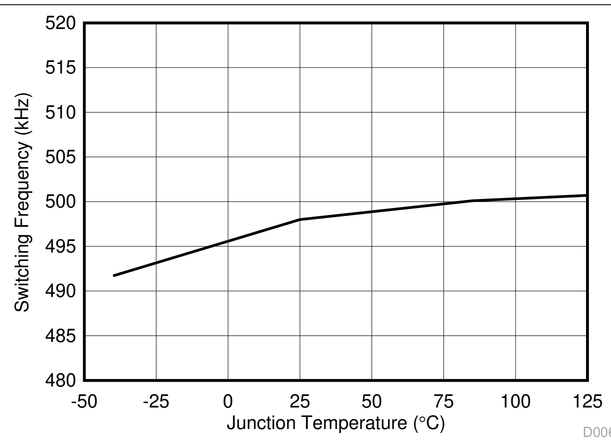


図 6-6. Centre Switching Frequency vs Junction Temperature

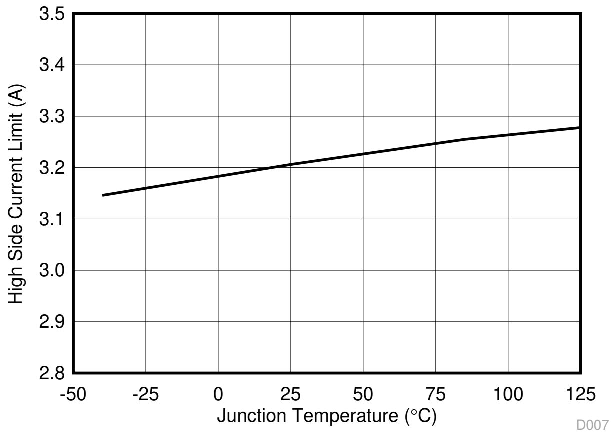


図 6-7. High-Side Current Limit Threshold vs Junction Temperature

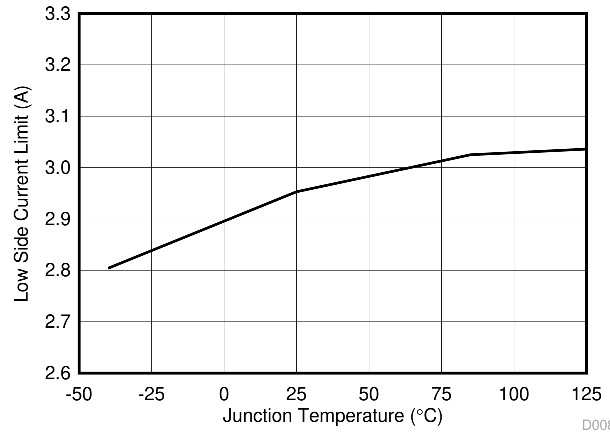


図 6-8. Low-Side Current Limit Threshold vs Junction Temperature

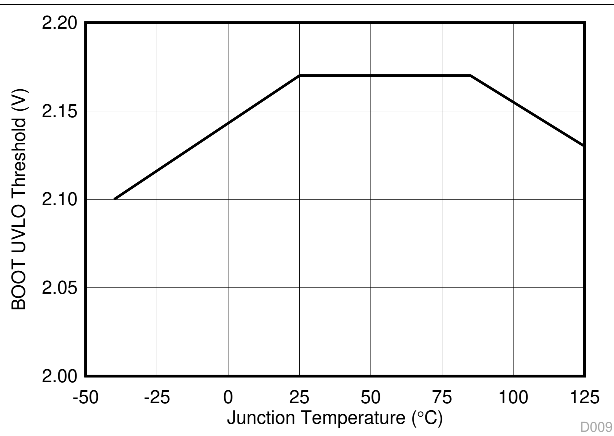


図 6-9. BOOT-SW UVLO Threshold vs Junction Temperature

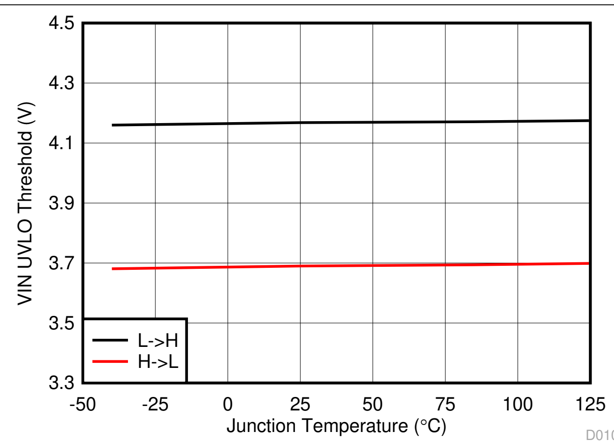


図 6-10. VIN UVLO Threshold vs Junction Temperature

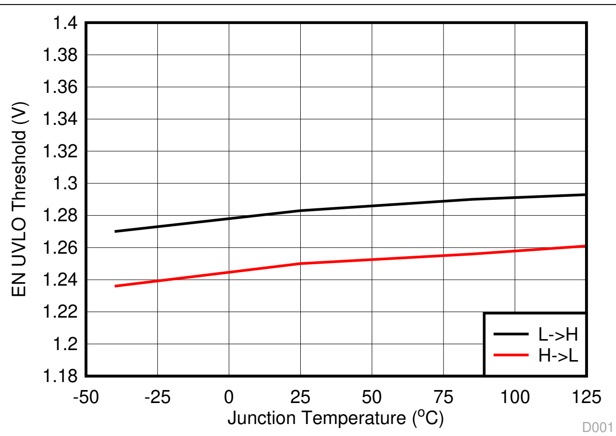


図 6-11. EN UVLO Threshold vs Junction Temperature

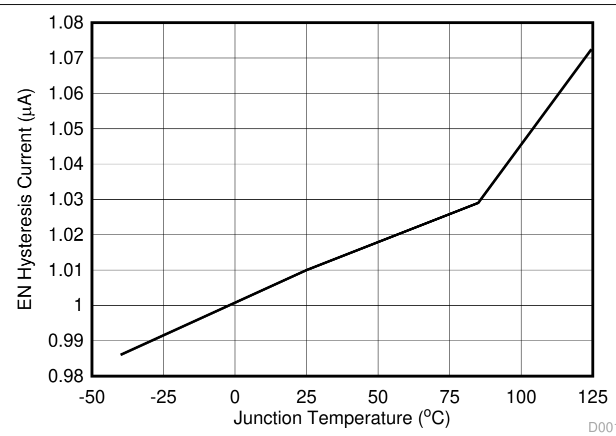


図 6-12. EN Hysteresis Current vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS54202H device is a 28-V, 2-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant-frequency, peak current mode control which reduces output capacitance. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

The switching frequency is fixed to 500 kHz.

The device begins switching at VIN equal to 4.5 V. The operating current is 45 μA typically when not switching and under no load. When the device is disabled, the supply current is 2 μA typically.

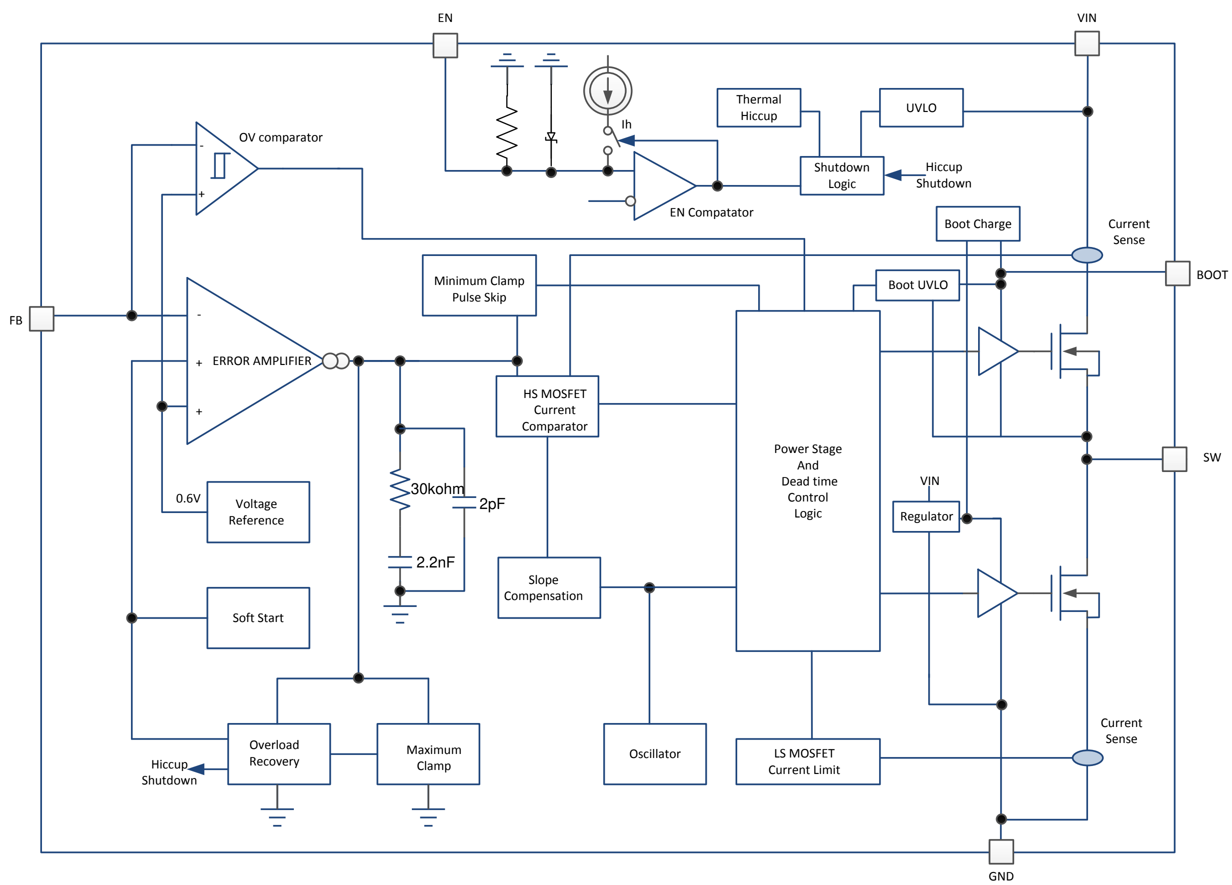
The integrated 148-mΩ high-side MOSFET and 78-mΩ allow for high efficiency power supply designs with continuous output currents up to 2 A.

The device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pins. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically.

The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage comparator. When the regulated output voltage is greater than 108% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 104%.

The device has internal 5-ms soft-start time to minimize inrush currents.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The device uses a fixed-frequency, peak current-mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the current of the high-side power switch. When the power-switch current reaches the error amplifier output voltage level, the high side power switch is turned off and the low-side power switch is turned on. The error amplifier output voltage increases and decreases as the output current increases and decreases. The device implements a current-limit by clamping the error amplifier voltage to a maximum level and also implements a minimum clamp for improved transient-response performance.

7.3.2 Pulse Skip Mode

The TPS54202H is designed to operate in pulse skipping mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 300 mA typically, the device enters pulse skipping mode. When the device is in pulse skipping mode, the error amplifier output voltage is clamped which prevents the high side integrated MOSFET from switching. The peak inductor current must rise above 300 mA and exit pulse skip mode. Since the integrated current comparator catches the peak inductor current only, the average load current entering pulse skipping mode varies with the applications and external output filters.

7.3.3 Error Amplifier

The device has a trans-conductance amplifier as the error amplifier. The error amplifier compares the FB voltage to the lower of the internal soft-start voltage or the internal 0.596-V voltage reference. The transconductance of the error amplifier is 240 μA/V typically. The frequency compensation components are placed internal between the output of the error amplifier and ground.

7.3.4 Slope Compensation and Output Current

The device adds a compensating ramp to the signal of the switch current. This slope compensation prevents sub-harmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

7.3.5 Device Enable

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent (IQ) state.

The EN pin has an internal pull down resistance Rpd (typical 1 MΩ) which allows the user to float the EN pin to disable the device, a Zener diode (typical break down voltage 6.9 V) is used to clamp the EN input voltage. To enable the device, connect a pull up resistor R4 (typical 510 KΩ) between EN and VIN, R4 is used to limit the quiet scent current of the device for light load efficiency improvement.

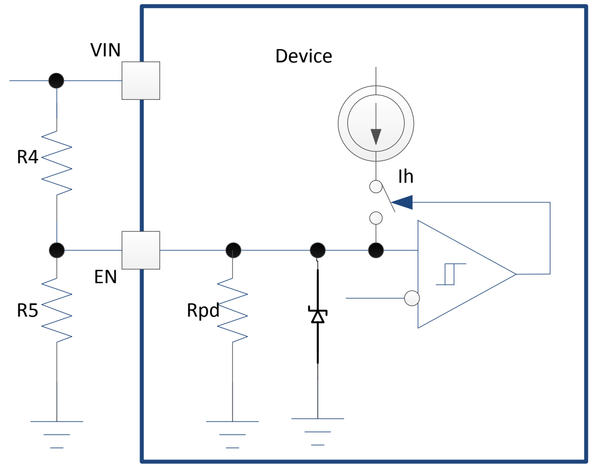


図 7-1. Adjustable VIN Undervoltage Lockout

7.3.6 Adjusting Under Voltage Lockout

The device implements internal under voltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 480 mV. To enable the device, connect a pull-up resistor R4 (typical 510 KΩ to limit the quiescent current) to the VIN pin.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in 図 7-1. When using the external UVLO function, setting the hysteresis at a value greater than 500 mV is recommended.

The EN pin has a pull-down resistance Rpd (typical 1 MΩ), which sets the default state of the pin to disable when no external components are connected. Use 式 1 and 式 2 to calculate the values of R4 and R5 for a specified UVLO threshold.

$$R4 = \left(\frac{V_{ENfalling}}{V_{ENrising}} \times V_{START} - V_{STOP} \right) / I_h \tag{1}$$

$$R5 = \frac{R4 \times Rpd}{\left(\frac{V_{START}}{V_{ENrising}} - 1 \right) \times Rpd - R4} \tag{2}$$

Where:

I_h = 1 μA
$V_{ENrising}$ = 1.28 V
$V_{ENfalling}$ = 1.25 V

7.3.7 Safe Startup into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than FB pin voltage.

7.3.8 Voltage Reference

The voltage reference system produces a precise ±2.5% voltage-reference over temperature by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.596 V.

7.3.9 Adjusting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 100 kΩ for the upper resistor divider, use 式 3 to calculate the output voltage. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$$V_{OUT} = V_{ref} \times \left[\frac{R2}{R3} + 1 \right] \quad (3)$$

7.3.10 Internal Soft-Start

The TTPS54202H device uses the internal soft-start function. The internal soft start time is set to 5 ms typically.

7.3.11 Bootstrap Voltage (BOOT)

The TPS54202H has an integrated boot regulator and requires a 0.1-μF ceramic capacitor between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1 V typically.

7.3.12 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

7.3.12.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the internal COMP voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference the high-side switch turns off.

7.3.12.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. If the low-side sourcing current-limit is exceeded, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the low-side current is below the low-side sourcing current-limit at the start of a cycle which is the inductor current valley value.

Furthermore, if an output overload condition occurs for more than the hiccup wait time, which is programmed for 512 switching cycles, the device shuts down and restarts after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

7.3.13 Output Overvoltage Protection (OVP)

The TPS54202H incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the FB pin voltage and internal thresholds. When the FB pin voltage goes above 108% × Vref, the high-side MOSFET will be forced off. When the FB pin voltage falls below 104% × Vref, the high-side MOSFET will be enabled again.

7.3.14 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 145°C typically, the internal thermal-hiccup timer begins to count. The device reinitiates the power-up sequence after the built-in thermal-shutdown hiccup time (32768 cycles) is over.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold, the TPS54202H can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when inductor peak current is above 0 A. In CCM, the device operates at a fixed frequency.

7.4.2 Eco-mode™ Operation

The devices are designed to operate in high-efficiency pulse-skipping mode under light load conditions. Pulse skipping initiates when the switch current falls to 0 A. During pulse skipping, the low-side FET turns off when the switch current falls to 0 A. The switching node (the SW pin) waveform takes on the characteristics of discontinuous conduction mode (DCM) operation and the apparent switching frequency decreases. As the output current decreases, the perceived time between switching pulses increases.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS54202H device is typically used as a step down converter, which convert an input voltage from 8 V to 28 V to fixed output voltage 5 V.

8.2 Typical Application

8.2.1 TPS54202H 8-V to 28-V Input, 5-V Output Converter

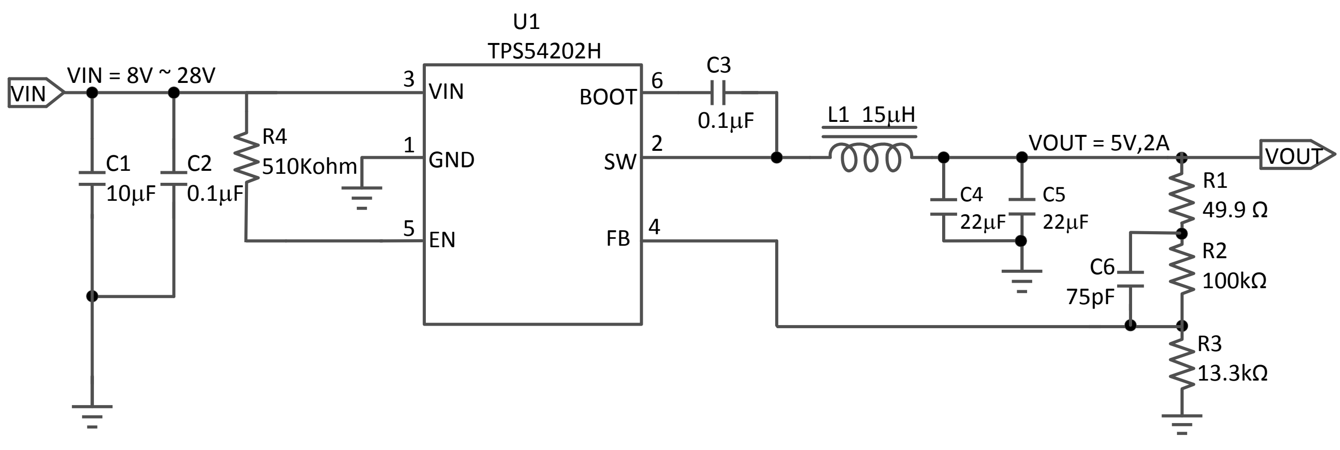


図 8-1. 5-V, 2-A Reference Design

8.2.2 Design Requirements

For this design example, use the parameters in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	8 V to 28 V
Output voltage	5 V
Output current	2 A
Transient response, 1.5 A load step	ΔV_{OUT} = ±5 %
Input ripple voltage	400 mV
Output voltage ripple	30 mVpp
Switching frequency	500 kHz

8.2.3 Detailed Design Procedure

8.2.3.1 Input Capacitor Selection

The device requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor (C2) from VIN to GND is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Use 式 4 to calculate the input ripple voltage (ΔV_{IN}).

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (4)$$

where:

- C_{BULK} is the bulk capacitor value
- f_{SW} is the switching frequency
- $I_{OUT(MAX)}$ is the maximum loading current
- ESR_{MAX} is maximum series resistance of the bulk capacitor

The maximum RMS (root mean square) ripple current must also be checked. For worst case conditions, use 式 5 to calculate $I_{CIN(RMS)}$.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{2} \quad (5)$$

The actual input-voltage ripple is greatly affected by parasitic associated with the layout and the output impedance of the voltage source. Design Requirements show the actual input voltage ripple for this circuit which is larger than the calculated value. This measured value is still below the specified input limit of 400 mV. The maximum voltage across the input capacitors is VIN (MAX) + ΔVIN/2. The selected bypass capacitor is rated for 35 V and the ripple current capacity is greater than 2 A. Both values provide ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

8.2.3.2 Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.3.3 Output Voltage Set Point

The output voltage of the TPS54202H device is externally adjustable using a resistor divider network. In the application circuit of , this divider network is comprised of R2 and R3. Use 式 6 and 式 7 to calculate the relationship of the output voltage to the resistor divider.

$$R3 = \frac{R2 \times V_{ref}}{V_{OUT} - V_{ref}} \quad (6)$$

$$V_{OUT} = V_{ref} \times \left[\frac{R2}{R3} + 1\right] \quad (7)$$

Select a value of R2 to be approximately 100 kΩ. Slightly increasing or decreasing R3 can result in closer output voltage matching when using standard value resistors. In this design, R2 = 100 kΩ and R3 = 13.3 kΩ which results in a 5-V output voltage. The 49.9-Ω resistor, R1, is provided as a convenient location to break the control loop for stability testing.

8.2.3.4 Enable Pin Setup

To enable the chip, a pull-up resistor R4 (typical 511 KΩ) connecting between VIN and EN R4 is used to limit the quiet scent current which should be less than 50 μA.

8.2.3.5 Output Filter Components

Two components must be selected for the output filter, the output inductor (L_O) and C_O.

8.2.3.5.1 Inductor Selection

Use 式 8 to calculate the minimum value of the output inductor (L_{MIN}).

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{sw}} \quad (8)$$

Where:

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

In general, the value of K_{IND} is at the discretion of the designer; however, the following guidelines may be used. For designs using low-ESR output capacitors, such as ceramics, a value as high as K_{IND} = 0.3 can be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3. The minimum inductor value is calculated as 13.7 μH. For this design, a close standard value of 15 μH was selected for L_{MIN}.

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use 式 9 to calculate the RMS inductor current ($I_{L(RMS)}$).

$$I_{L(MAX)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_O \times f_{SW} \times 0.8} \right)^2} \quad (9)$$

Use 式 10 to calculate the peak inductor current ($I_{L(PK)}$).

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_O \times f_{SW}} \quad (10)$$

Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple. Smaller inductor values increase AC current and output voltage ripple.

8.2.3.5.2 Output Capacitor Selection

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to notice the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change.

The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Use 式 11 to calculate the minimum required output capacitance.

$$C_O > \frac{2 \times \Delta I_{OUT}}{f_{sw} \times \Delta V_{OUT}} \tag{11}$$

where:

- ΔI_{OUT} is the change in output current
- f_{SW} is the switching frequency of the regulator
- $\Delta V_{(OUT\ )}$b is the allowable change in the output voltage

For this example, the transient load response is specified as a 5% change in the output voltage, V_{OUT}, for a load step of 1.5 A. For this example, ΔI_{OUT} = 1.5 A and ΔV_{OUT} = 0.05 × 5 = 0.25 V. Using these values results in a minimum capacitance of 24 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

式 12 calculates the minimum output capacitance required to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, 式 12 yields 4.56 µF.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{OUTripple}}{I_{ripple}}} \tag{12}$$

where:

- f_{SW} is the switching frequency
- $V_{(OUTripple)}$ is the maximum allowable output voltage ripple
- $I_{(ripple)}$ is the inductor ripple current

Use 式 13 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. 式 13 indicates the ESR should be less than 54.8 mΩ. In this case, the ESR of the ceramic capacitor is much smaller than 54.8 mΩ.

$$R_{ESR} < \frac{V_{OUTripple}}{I_{ripple}} \tag{13}$$

The output capacitor can affect the crossover frequency f_o. Considering to the loop stability and effect of the internal parasitic parameters, choose the crossover frequency less than 40 kHz without considering the feed forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor C6 is shown in 式 14, assuming C_{OUT} has small ESR.

$$f_o = \frac{3.95}{V_{OUT} \times C_{OUT}} \tag{14}$$

Additional capacitance deratings for aging, temperature, and DC bias should be considered which increases this minimum value. For this example, two 22-uF 25-V, X7R ceramic capacitors are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use 式 15 to calculate the RMS ripple current that the output capacitor must support. For this application, 式 15 yields 79 mA for each capacitor.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_O \times f_{SW} \times N_C} \right) \quad (15)$$

8.2.3.5.3 Feed-Forward Capacitor

The TPS54202H device is internally compensated and the internal compensation network is composed of two capacitors and one resister shown on the block diagram. Depending on the V_{OUT}, if the output capacitor C_{OUT} is dominated by low ESR (ceramic types) capacitors, it could result in low phase margin. To improve the phase boost an external feedforward capacitor C6 can be added in parallel with R2. C6 is chosen such that phase margin is boosted at the crossover frequency.

式 16 for C6 was tested:

$$C6 = \frac{1}{2\pi f_O} \times \frac{1}{R2} \quad (16)$$

For this design, C6 = 75 pF. C6 is not needed when C_{OUT} has high ESR, and C6 calculated from 式 16 should be reduced with medium ESR. 表 8-2 can be used as a starting point.

表 8-2. Recommended Component Values

V_{OUT} (V)	L (µH)	C_{OUT}(µF)	R2 (kΩ)	R3 (kΩ)	C6 (pF)
1.8	5.6	66	100	49.9	47
2.5	8.2	44	100	31.6	33
3.3	10	44	100	22.1	56
5	15	44	100	13.3	75
12	22	44	100	5.23	100

8.2.4 Application Curves

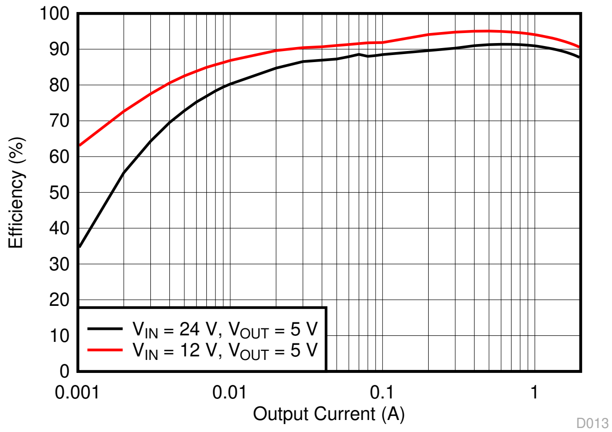


図 8-2. Efficiency

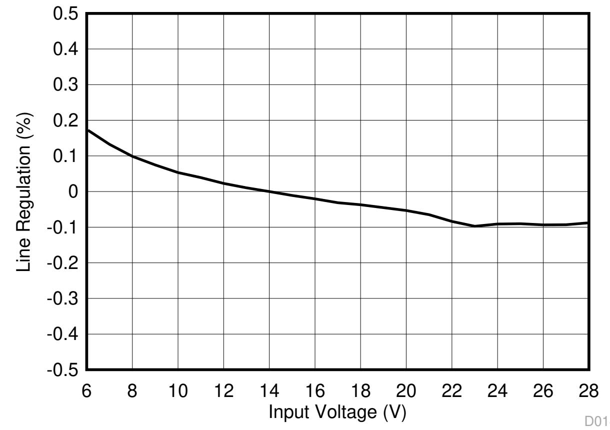


図 8-3. Line Regulation

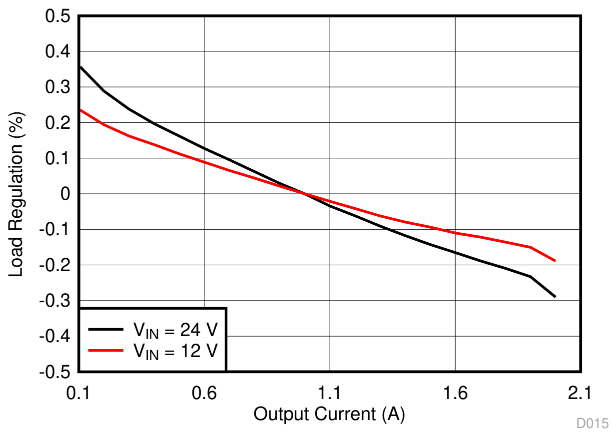
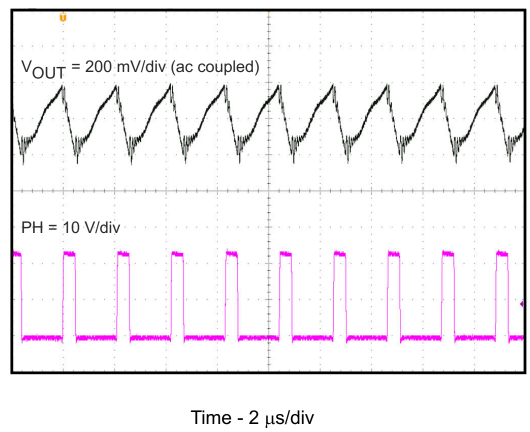
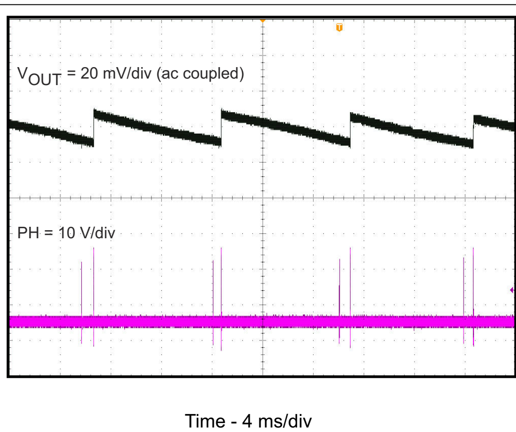


図 8-4. Load Regulation



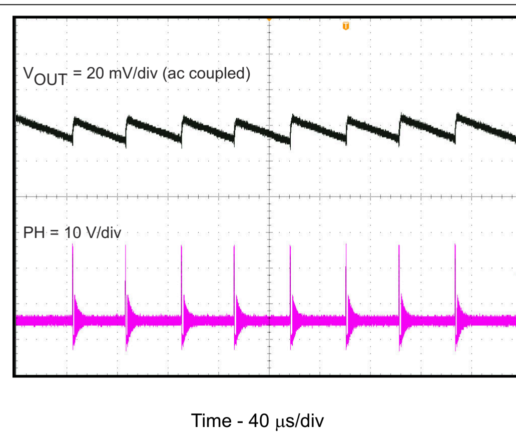
I_{OUT} = 2 A

図 8-5. Input Voltage Ripple



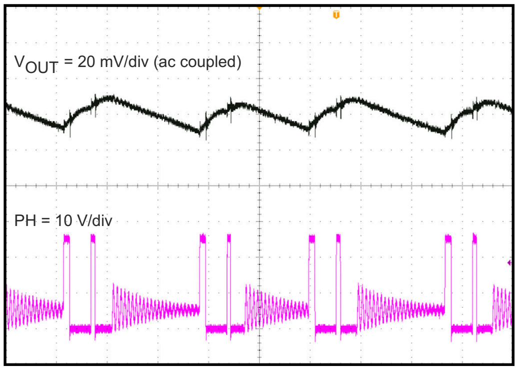
I_{OUT} = 0 A

図 8-6. Output Voltage Ripple



I_{OUT} = 10 mA

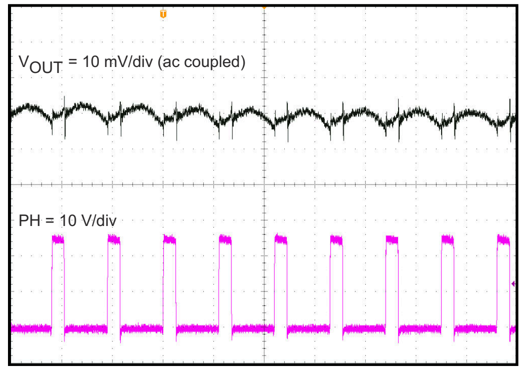
図 8-7. Output Voltage Ripple



Time - 4 µs/div

I_{OUT} = 100 mA

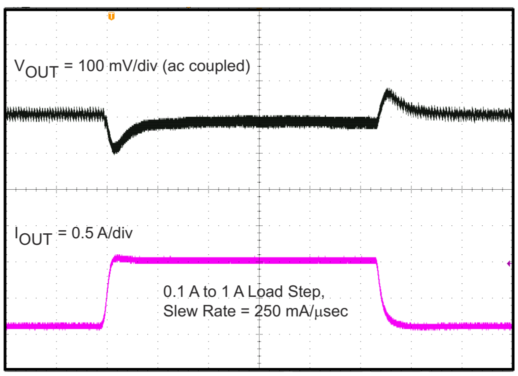
図 8-8. Output Voltage Ripple



Time - 2 µs/div

I_{OUT} = 2 A

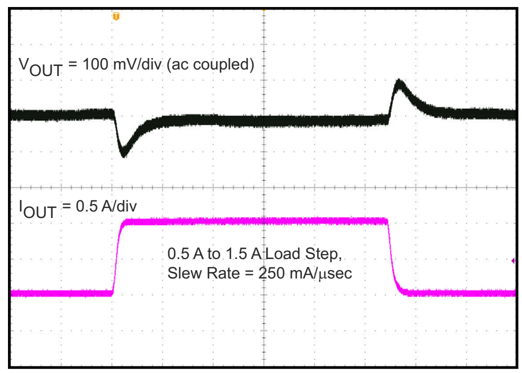
図 8-9. Output Voltage Ripple



Time - 200 µs/div

0.1 to 1 A

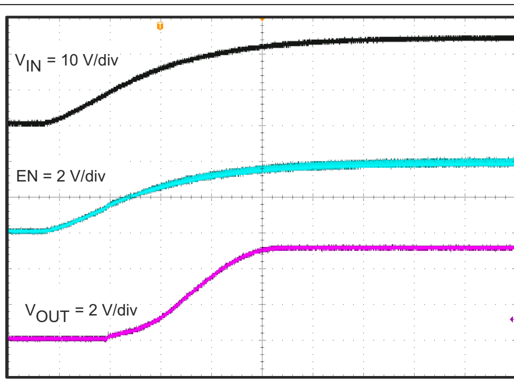
図 8-10. Transient Response



Time - 200 µs/div

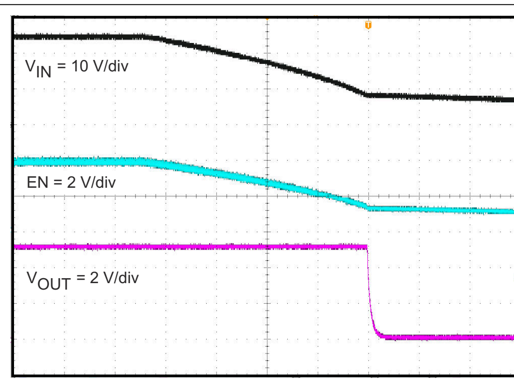
0.5 to 1.5 A

図 8-11. Transient Response



Time - 2 ms/div

図 8-12. Start-Up Relative to VIN



Time - 2 ms/div

図 8-13. Shutdown Relative to VIN

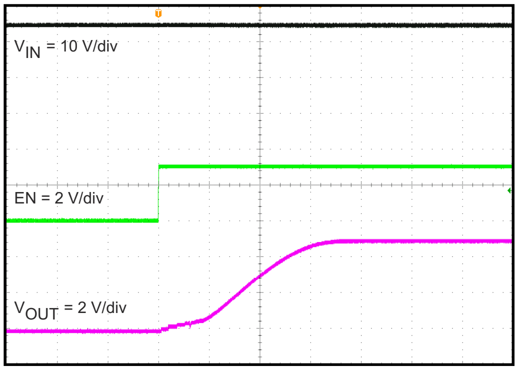


図 8-14. Start-Up Relative to EN

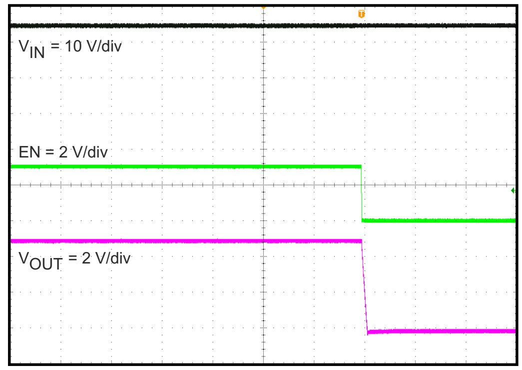


図 8-15. Shutdown Relative to EN

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

- VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
- The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- A separate VOUT path should be connected to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
- The trace of the VFB node should be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

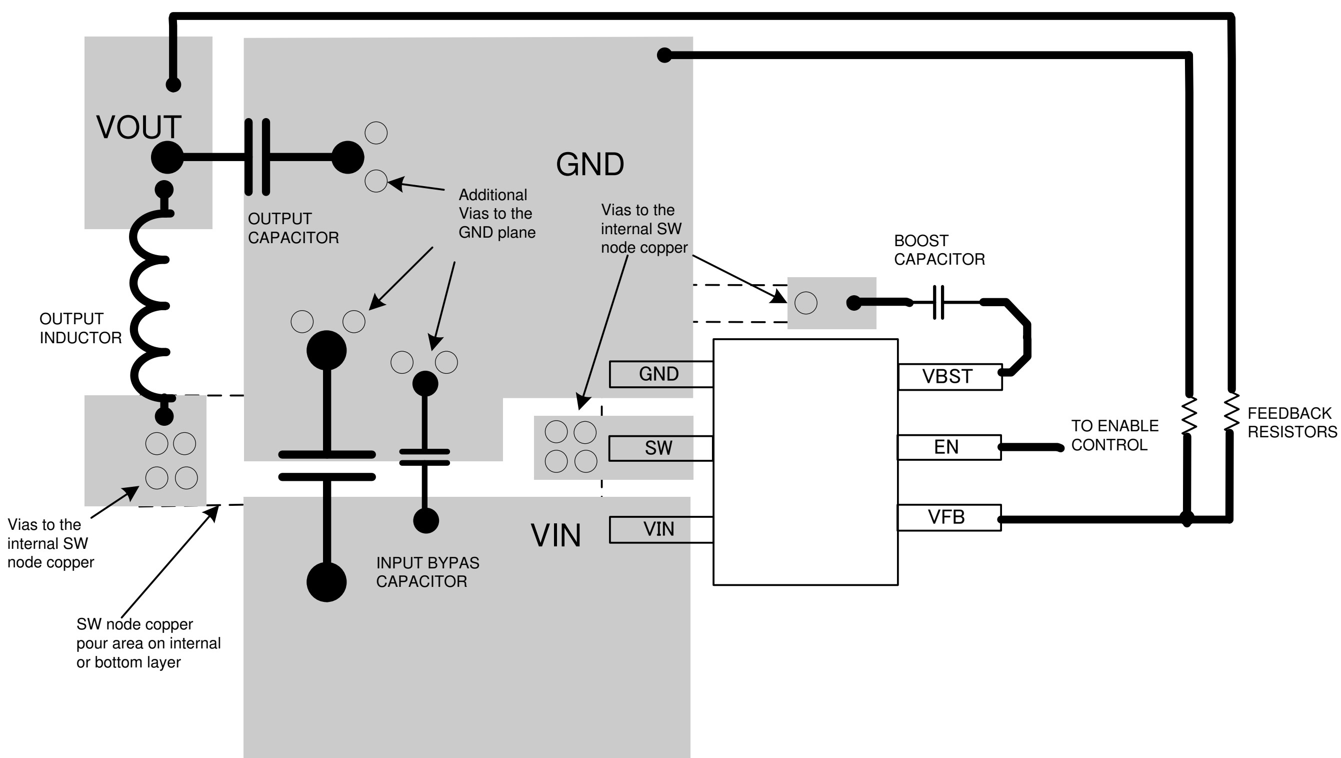


図 10-1. Board Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54202HDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	202H
TPS54202HDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	202H
TPS54202HDDCR.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	202H
TPS54202HDDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	202H
TPS54202HDDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	202H
TPS54202HDDCT.B	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	202H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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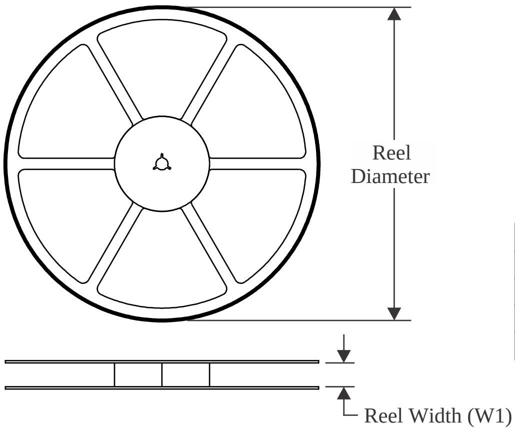
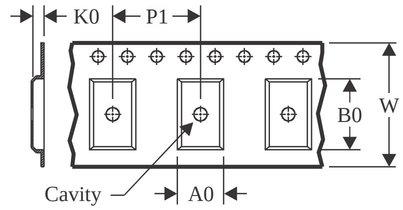
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

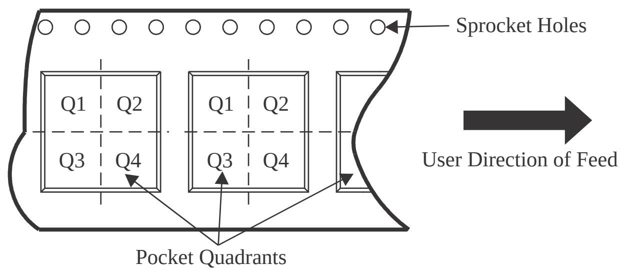


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

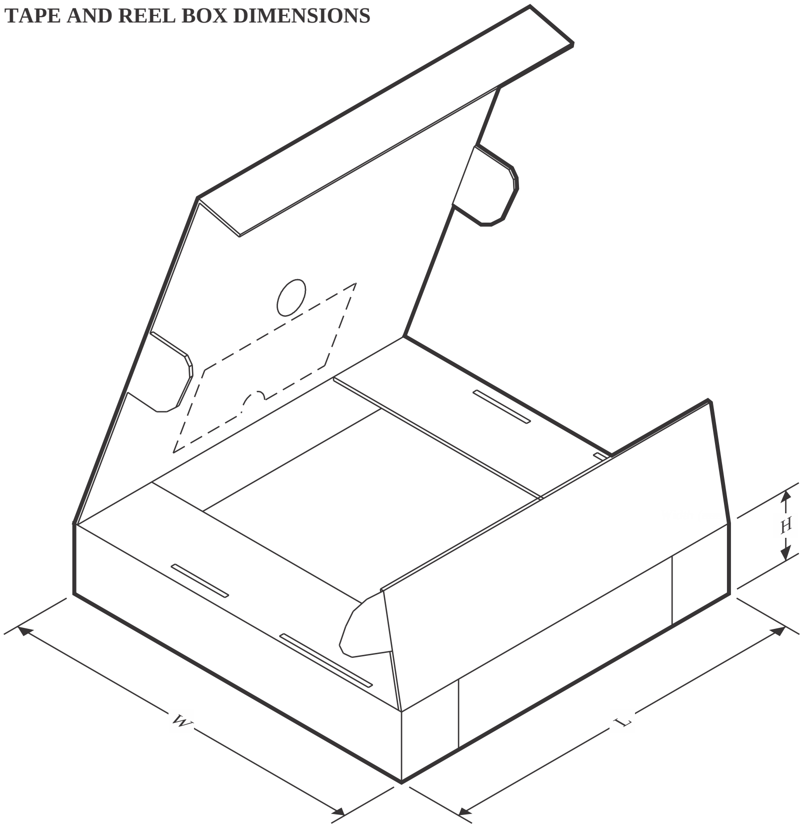
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

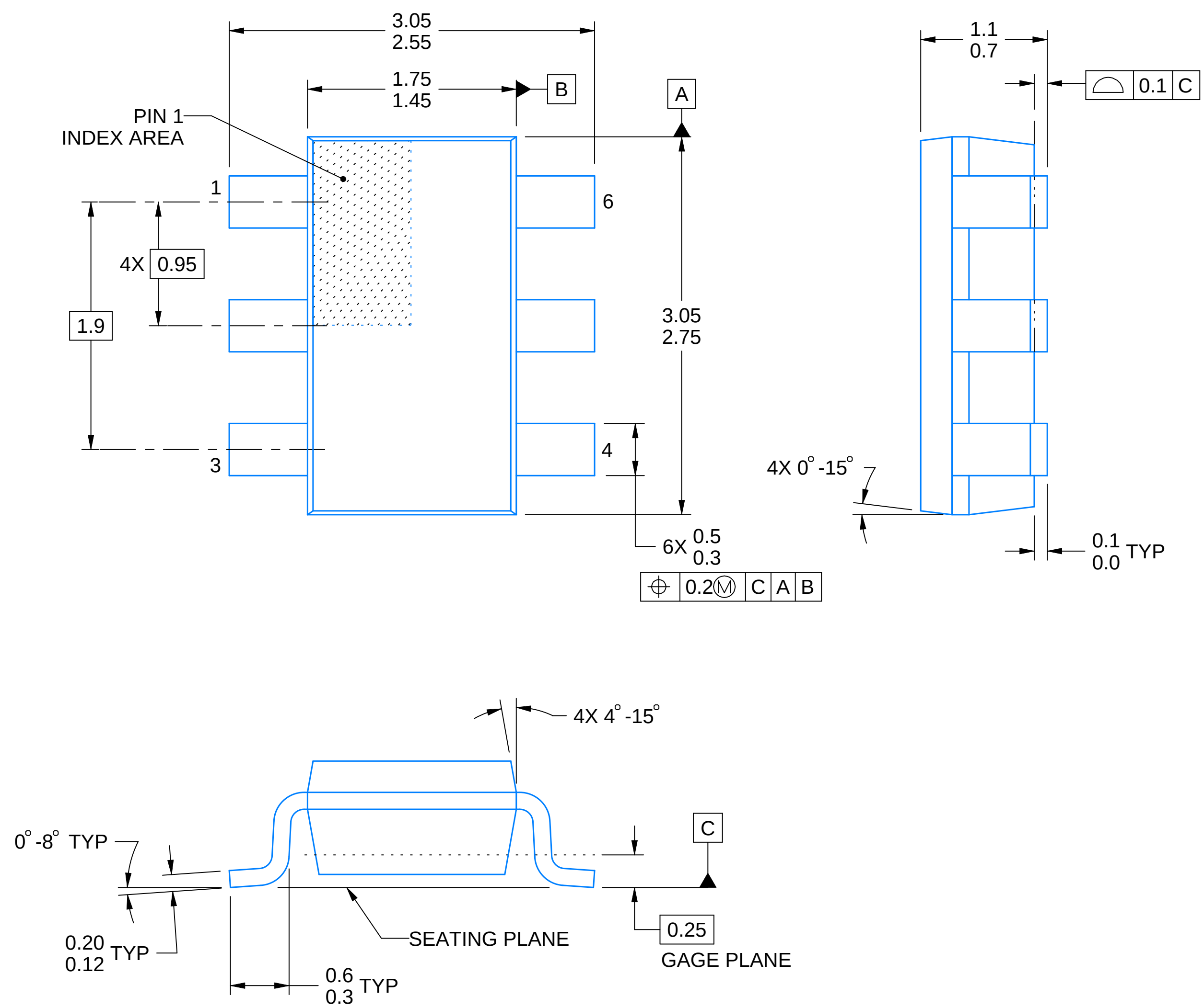
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54202HDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS54202HDDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54202HDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS54202HDDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0



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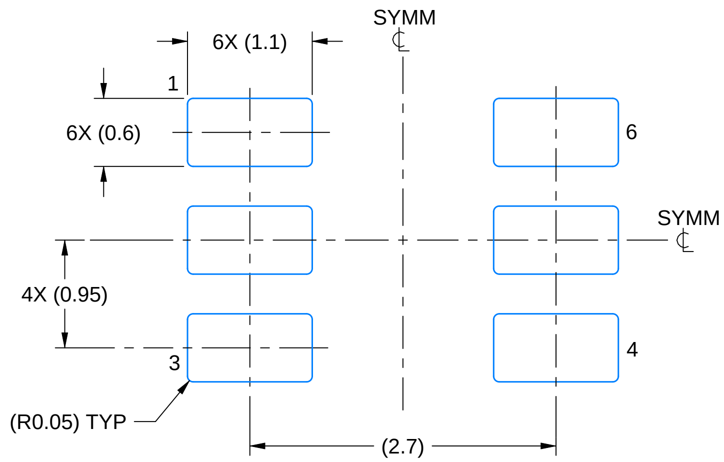
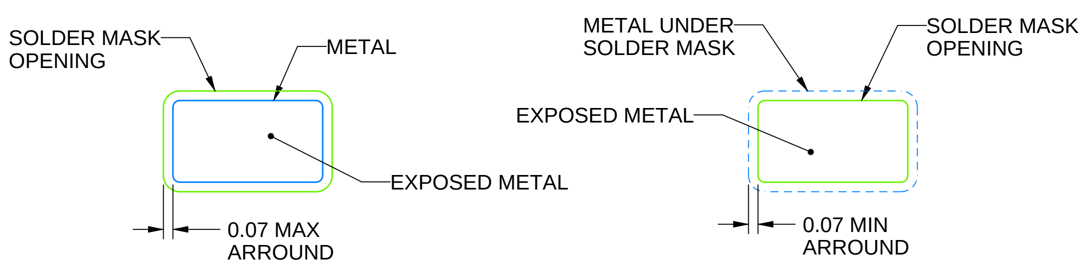
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDERMASK DETAILS

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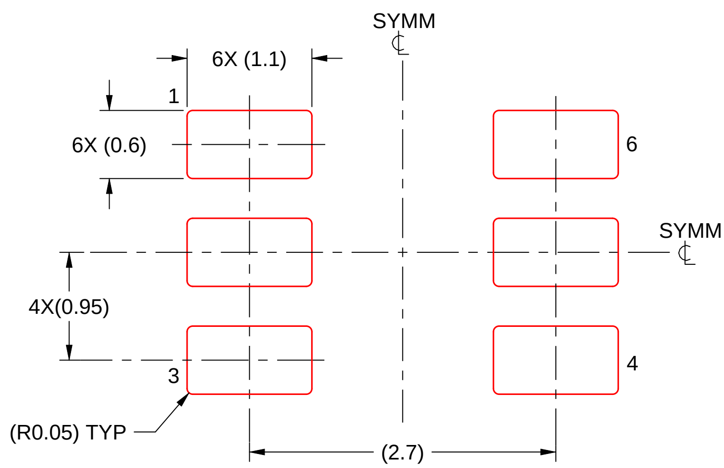
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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