

TPS5331x Eco-mode 制御搭載、 高効率 8A または 14A 同期整流式降圧コンバータ

1 特長

- 変換入力電圧範囲：1.5V ~ 22V
- VDD 入力電圧範囲：4.5V ~ 25V
- 14A において 12V から 1.5V への効率：91%
- 出力電圧範囲：0.6V ~ 5.5V
- 5V LDO 出力
- 単一レール入力のサポート
- パワー MOSFET を内蔵：連続出力電流 8A (TPS53318) または 14A (TPS53319)
- 自動スキップ Eco-mode™ により軽負荷時の効率を向上
- シャットダウン電流：110μA 未満
- 高速過渡応答の D-CAP™ モード
- 外付け抵抗によりスイッチング周波数を 250kHz ~ 1MHz の範囲で選択可能
- 自動スキップまたは PWM のみの動作を選択可能
- 1% 精度、0.6V の基準電圧を内蔵
- 内部電圧サーボ・ソフト・スタート：0.7ms、1.4ms、2.8ms、5.6ms から選択可能
- ブースト・スイッチ内蔵
- プリチャージ・スタートアップ機能
- 温度補償付きの調整可能な過電流制限
- 過電圧、低電圧、UVLO、過熱保護
- すべての出力コンデンサでセラミック・コンデンサの使用をサポート
- オープン・ドレインのパワー・グッド表示
- NexFET™ パワー・ブロック・テクノロジーを内蔵
- 22 ピン QFN (DQP) パッケージ、PowerPAD™ 付き

2 アプリケーション

- サーバーおよびストレージ
- ワークステーションおよびデスクトップ
- 通信インフラストラクチャ

3 概要

TPS53318 および TPS53319 デバイスは、D-CAP モードに対応し、MOSFET を内蔵した、8A または 14A の同期整流スイッチャです。使いやすさに重点を置き、外部部品数の少ない省スペースの電源システム用に設計されています。

精度 1% の 0.6V リファレンスに加え、ブースト・スイッチを内蔵しています。主な特徴として、1.5V ~ 22V の幅広い変換入力電圧範囲、非常に少ない外部部品数、D-CAP™ モード制御による超高速過渡応答、自動スキップ・モード動作、内部ソフト・スタート制御、選択可能な周波数、補償が不要、などが挙げられます。

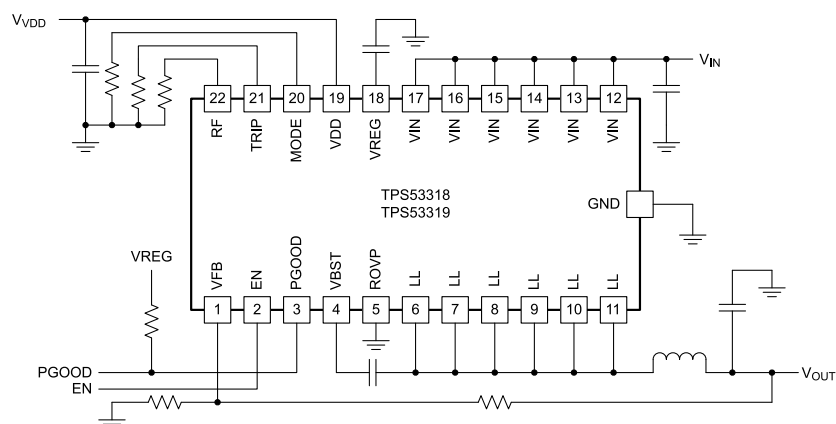
変換入力電圧範囲は 1.5V ~ 22V、電源電圧範囲は 4.5V ~ 25V、出力電圧範囲は 0.6V ~ 5.5V です。

これらのデバイスは 5mm × 6mm の 22 ピン QFN パッケージで供給され、-40°C ~ 85°C で仕様が規定されています。

製品情報 (1) (1 ページ)

型番	パッケージ	本体サイズ (公称)
TPS53318	LSON-CLIP (22)	6.00mm × 5.00mm
TPS53319		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。



アプリケーション概略



Table of Contents

1 特長	1	8.3 Feature Description.....	17
2 アプリケーション	1	8.4 Device Functional Modes.....	22
3 概要	1	9 Application and Implementation	24
4 Revision History	2	9.1 Application Information.....	24
5 Device Comparison Table	3	9.2 Typical Applications.....	24
6 Pin Configuration and Functions	4	10 Power Supply Recommendations	30
7 Specifications	6	11 Layout	31
7.1 Absolute Maximum Ratings.....	6	11.1 Layout Guidelines.....	31
7.2 ESD Ratings.....	6	11.2 Layout Example.....	32
7.3 Recommended Operating Conditions.....	6	12 Device and Documentation Support	33
7.4 Thermal Information.....	7	12.1 Device Support.....	33
7.5 Electrical Characteristics.....	7	12.2 Receiving Notification of Documentation Updates.....	33
7.6 Typical Characteristics.....	10	12.3 Support Resources.....	33
7.7 TPS53319 Typical Characteristics.....	14	12.4 Trademarks.....	33
7.8 TPS53318 Typical Characteristics.....	15	12.5 Electrostatic Discharge Caution.....	33
8 Detailed Description	16	12.6 Glossary.....	33
8.1 Overview.....	16	13 Mechanical, Packaging, and Orderable Information	33
8.2 Functional Block Diagram.....	16		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (November 2016) to Revision F (October 2020)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Added ROVP pin description.....	4
• Added additional ROVP pin information.	20
Changes from Revision D (February 2015) to Revision E (November 2016)	Page
• Changed Pin 19 From: ground To: V_{IN} 12 V in 図 9-1	24
Changes from Revision C (December 2014) to Revision D (February 2015)	Page
• Added recommendation for ROVP connection when ROVP function is not needed in <i>Pin Functions</i> table.....	4
• Corrected typographical error. Changed "when the VDD voltage rises above 1 V" to "when the VDD voltage rises above 2 V" in セクション 8.3.1	17
• Added <i>ROVP Pin Design Note</i> in セクション 8.3.9	20
Changes from Revision B (May 2013) to Revision C (OCTOBER 2014)	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• Added clarity to セクション 8.3.7	19
• Added 表 8-2	19
Changes from Revision A (JUNE 2012) to Revision B (MAY 2013)	Page
• Added clarity to セクション 8.3.8	20
• Updated 図 11-1	32

Changes from Revision * (JUNE 2012) to Revision A (AUGUST 2012)

Page

- [セクション 1](#) (1 ページ) の「シャットダウン電流 : 100 μ A 未満」を「シャットダウン電流 : 110 μ A 未満」に変更 [1](#)

5 Device Comparison Table

ORDER NUMBER ⁽¹⁾	OUTPUT CURRENT (A)
TPS53318DQP	8
TPS53319DQP	14

- (1) For detailed ordering information see the *Package Option Addendum* section at the end of this data sheet.

6 Pin Configuration and Functions

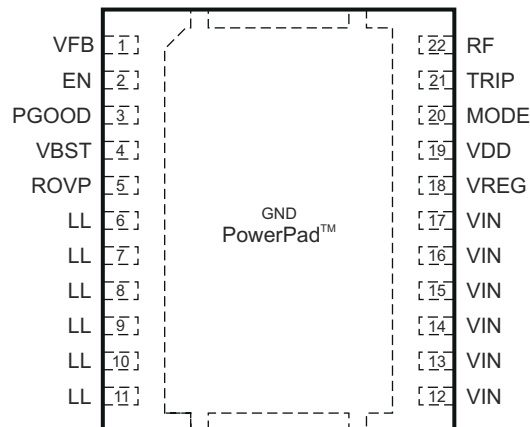


图 6-1. 22 Pins DQP (LSON-CLIP) Package (Top View)

表 6-1. Pin Functions

PIN		I/O/P ⁽¹⁾	DESCRIPTION
NAME	NO.		
EN	2	I	Enable pin. Typical turnon threshold voltage is 1.3 V. Typical turnoff threshold voltage is 1.0 V.
GND		G	Ground and thermal pad of the device. Use proper number of vias to connect to ground plane.
LL	6	B	Output of converted power. Connect this pin to the output inductor.
	7		
	8		
	9		
	10		
	11		
MODE	20	I	Soft start and mode selection. Connect a resistor to select soft-start time using 表 8-3. The soft-start time is detected and stored into internal register during start-up.
PGOOD	3	O	Open drain power-good flag. Provides 1-ms start-up delay after VFB falls in specified limits. When VFB goes out of the specified limits, PGOOD goes low after a 2-μs delay.
ROVP	5	I	Redundant overvoltage protection (OVP) input. Use a resistor divider to connect this pin to V _{OUT} . Internally pulled down to GND with a 1.5-MΩ resistor. If redundant OVP is not needed, connect this pin to GND. Do not leave ROVP pin floating (see セクション 8.3.9).
RF	22	I	Switching frequency selection. Connect a resistor to GND or VREG to select switching frequency using 表 8-1. The switching frequency is detected and stored during the start-up.
TRIP	21	I	OCL detection threshold setting pin. I _{TRIP} = 10 μA at room temperature. 3000 ppm/°C current is sourced and set the OCL trip voltage as follows.
			$V_{OCL} = V_{TRIP}/32$ ($V_{TRIP} \leq 2.4 \text{ V}$, $V_{OCL} \leq 75 \text{ mV}$)
VBST	4	P	Supply input for high-side FET gate driver (boost terminal). Connect capacitor from this pin to LL node. Internally connected to VREG via bootstrap MOSFET switch.
VDD	19	P	Controller power supply input. VDD input voltage range is from 4.5 V to 25 V.
VFB	1	I	Output feedback input. Connect this pin to V _{OUT} through a resistor divider.
VIN	12	P	Conversion power input. The conversion input voltage range is from 1.5 V to 22 V.
	13		
	14		
	15		
	16		
	17		
VREG	18	P	5-V low dropout (LDO) output. Supplies the internal analog circuitry and driver circuitry.

表 6-1. Pin Functions (continued)

PIN		I/O/P ⁽¹⁾	DESCRIPTION
NAME	NO.		
Thermal Pad		G	Ground and thermal pad of the device. Use a proper number of vias to connect to ground plane.

(1) I = Input, O = Output, B = Bidirectional, P = Supply, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

			VALUE ⁽¹⁾		UNIT
			MIN	MAX	
Input voltage range	VIN (main supply)		−0.3	30	V
	VDD		−0.3	28	
	VBST		−0.3	32	
	VBST (with respect to LL)		−0.3	7	
	EN, MODE, TRIP, RF, ROVP, VFB		−0.3	7	
Output voltage range	LL	DC	−2	30	V
		Pulse < 20ns, E = 5 μJ	−7	32	
	PGOOD, VREG		−0.3	7	
	GND		−0.3	0.3	
Source/Sink current	VBST		50		mA
Operating free-air temperature, T _A			−40	85	°C
Junction temperature range, T _J			−40	150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				300	
Storage temperature, T _{stg}			−55	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VIN (main supply)	1.5	22	V
	VDD	4.5	25	
	VBST	4.5	28	
	VBST (with respect to LL)	4.5	6.5	
	EN, MODE, TRIP, RF, ROVP, VFB	−0.1	6.5	
Output voltage range	LL	−1	27	V
	PGOOD, VREG	−0.1	6.5	
Junction temperature range, T _J		−40	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS53318 TPS53319	UNIT
		DQP	
		22 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	27.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	17.1	
R _{θJB}	Junction-to-board thermal resistance	5.9	
Ψ _{JT}	Junction-to-top characterization parameter	0.8	
Ψ _{JB}	Junction-to-board characterization parameter	5.8	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	1.2	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

Over recommended free-air temperature range, V_{VDD} = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V _{VIN}	VIN pin power conversion input voltage		1.5		22	V
V _{VDD}	Supply input voltage		4.5		25.0	V
I _{VIN(leak)}	VIN pin leakage current	V _{EN} = 0 V			1	μA
I _{VDD}	VDD supply current	T _A = 25°C, No load, V _{EN} = 5 V, V _{VFB} = 0.630 V		420	590	μA
I _{VDDSDN}	VDD shutdown current	T _A = 25°C, No load, V _{EN} = 0 V			110	μA
INTERNAL REFERENCE VOLTAGE						
V _{VFB}	VFB regulation voltage	CCM condition ⁽¹⁾		0.600		V
V _{VFB}	VFB regulation voltage	T _A = 25°C	0.597	0.600	0.603	V
		0°C ≤ T _A ≤ 85°C	0.5952	0.600	0.6048	
		–40°C ≤ T _A ≤ 85°C	0.594	0.600	0.606	
I _{VFB}	VFB input current	V _{VFB} = 0.630 V, T _A = 25°C		0.01	0.20	μA
LDO OUTPUT						
V _{VREG}	LDO output voltage	0 mA ≤ I _{VREG} ≤ 30 mA	4.77	5.00	5.36	V
I _{VREG}	LDO output current ⁽¹⁾	Maximum current allowed from LDO			30	mA
V _{DO}	Low drop out voltage	V _{VDD} = 4.5 V, I _{VREG} = 30 mA			250	mV
BOOT STRAP SWITCH						
V _{FBST}	Forward voltage	V _{VREG-VBST} , I _F = 10 mA, T _A = 25°C		0.1	0.2	V
I _{VBSTLK}	VBST leakage current	V _{VBST} = 23 V, V _{SW} = 17 V, T _A = 25°C		0.01	1.50	μA
DUTY AND FREQUENCY CONTROL						
t _{OFF(min)}	Minimum off-time	T _A = 25°C	150	260	400	ns
t _{ON(min)}	Minimum on-time	V _{IN} = 17 V, V _{OUT} = 0.6 V, f _{SW} = 1 MHz, T _A = 25 °C ⁽¹⁾		35		ns
SOFT-START TIMING						
t _{SS}	Internal soft-start time from V _{OUT} = 0 V to 95% of V _{OUT}	R _{MODE} = 39 kΩ		0.7		ms
		R _{MODE} = 100 kΩ		1.4		
		R _{MODE} = 200 kΩ		2.8		
		R _{MODE} = 470 kΩ		5.6		

Over recommended free-air temperature range, $V_{DD} = 12\text{ V}$ (unless otherwise noted)

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE DISCHARGE							
I _{DSCHG}	Output voltage discharge current		V _{EN} = 0 V, V _{SW} = 0.5 V	5.0	6.6	9.0	mA
POWERGOOD							
V _{THPG}	PG threshold		PG in from lower	92.5%	95.0%	98.5%	
			PG in from higher	107.5%	110.0%	112.5%	
			PG hysteresis	2.5%	5.0%	7.5%	
R _{PG}	PG transistor on-resistance			15	30	60	Ω
t _{PGDEL}	PG delay		Delay for PG in	0.8	1	1.2	ms
LOGIC THRESHOLD AND SETTING CONDITIONS							
V _{EN}	EN Voltage		Enable	1.0	1.3	1.6	V
			Disable	0.8	1.0	1.2	
I _{EN}	EN Input current		V _{EN} = 5 V			1.0	μA
f _{SW}	Switching frequency		R _{RF} = 0 Ω to GND, T _A = 25°C ⁽²⁾	200	250	300	kHz
			R _{RF} = 187 kΩ to GND, T _A = 25°C ⁽²⁾	250	300	350	
			R _{RF} = 619 kΩ, to GND, T _A = 25°C ⁽²⁾	350	400	450	
			R _{RF} = Open, T _A = 25°C ⁽²⁾	450	500	550	
			R _{RF} = 866 kΩ to VREG, T _A = 25°C ⁽²⁾	540	600	660	
			R _{RF} = 309 kΩ to VREG, T _A = 25°C ⁽²⁾	670	750	820	
			R _{RF} = 124 kΩ to VREG, T _A = 25°C ⁽²⁾	770	850	930	
			R _{RF} = 0 Ω to VREG, T _A = 25°C ⁽²⁾	880	970	1070	
PROTECTION: CURRENT SENSE							
I _{TRIP}	TRIP source current		V _{TRIP} = 1 V, T _A = 25°C	10			μA
TC _{ITRIP}	TRIP current temperature coefficient		On the basis of 25°C ⁽²⁾	3000			ppm/°C
V _{TRIP}	Current limit threshold setting range	TPS53318	V _{TRIP-GND}	0.4		1.5	V
		TPS53319		2.4			
V _{OCL}	Current limit threshold		V _{TRIP} = 1.2 V	37.5			mV
			V _{TRIP} = 0.4	12.5			
V _{OCLN}	Negative current limit threshold		V _{TRIP} = 1.2 V	−37.5			mV
			V _{TRIP} = 0.4 V	−12.5			
I _{OCP}	Valley current limit threshold		R _{TRIP} = 66.5 kΩ, 0°C ≤ T _A ≤ 125°C	4.6	5.4	6.3	A
			R _{TRIP} = 66.5 kΩ, −40°C ≤ T _A ≤ 125°C	4.4	5.4	6.3	
V _{AZCADJ}	Auto zero cross adjustable range		Positive	3	15		mV
			Negative		−15	−3	
PROTECTION: UVP and OVP							
V _{OVP}	OVP trip threshold		OVP detect	115%	120%	125%	
t _{OVPDEL}	OVP propagation delay		VFB delay with 50-mV overdrive	1			μs
V _{UVP}	Output UVP trip threshold		UVP detect	65%	70%	75%	
t _{UVPDEL}	Output UVP propagation delay			0.8	1.0	1.2	ms
t _{UVPEN}	Output UVP enable delay		From enable to UVP workable	1.5	2.3	3.0	ms
UVLO							
V _{UVVREG}	VREG UVLO threshold		Wake up	4.00	4.20	4.33	V
			Hysteresis	0.25			

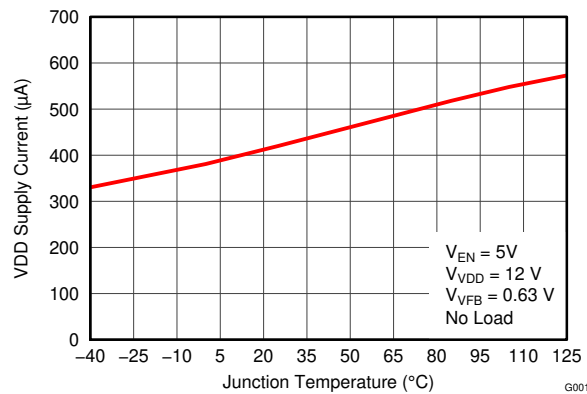
Over recommended free-air temperature range, $V_{DD} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION: UVP and OVP						
V _{OVP}	OVP trip threshold	OVP detect	115%	120%	125%	
t _{OVPDEL}	OVP propagation delay	VFB delay with 50-mV overdrive	1			μs
V _{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
t _{UVPDEL}	Output UVP propropagation delay		0.8	1.0	1.2	ms
t _{UVPEN}	Output UVP enable delay	From enable to UVP workable	1.5	2.3	3.0	ms
UVLO						
V _{UVVREG}	VREG UVLO threshold	Wake up	4.00	4.20	4.33	V
		Hysteresis	0.25			
THERMAL SHUTDOWN						
T _{SDN}	Thermal shutdown threshold	Shutdown temperature ⁽²⁾	145			°C
		Hysteresis ⁽²⁾	10			

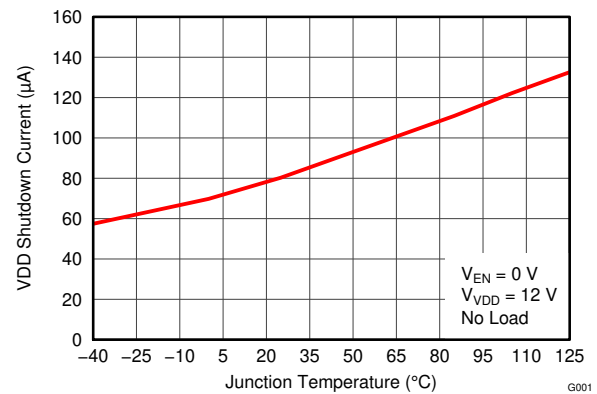
(1) Ensured by design. Not production tested.

(2) Not production tested. Test condition is $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 5\text{ A}$ using application circuit shown in [Figure 9-12](#).

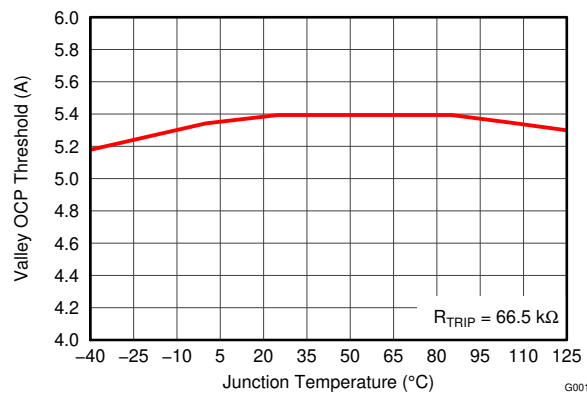
7.6 Typical Characteristics



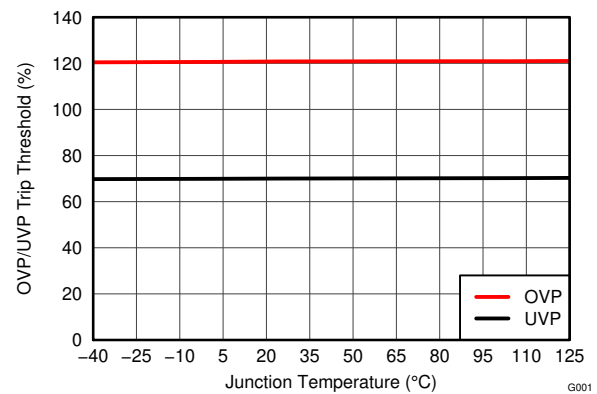
7-1. VDD Supply Current vs. Junction Temperature



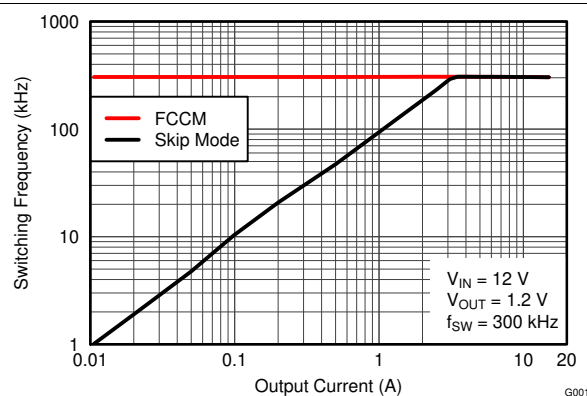
7-2. VDD Shutdown Current vs. Junction Temperature



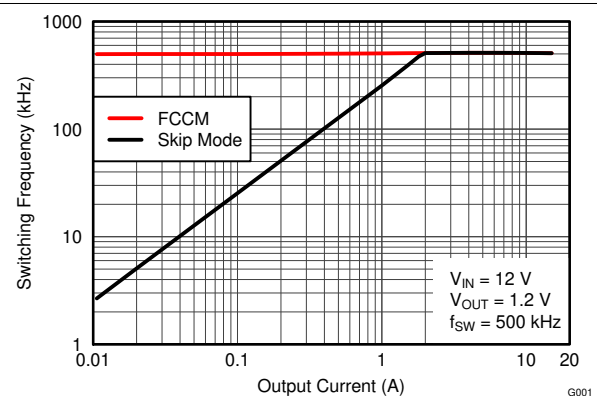
7-3. Valley OCP Threshold vs Temperature



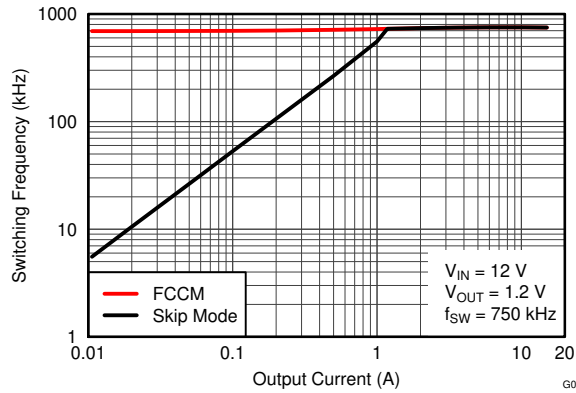
7-4. OVP/UVP Trip Threshold vs. Junction Temperature



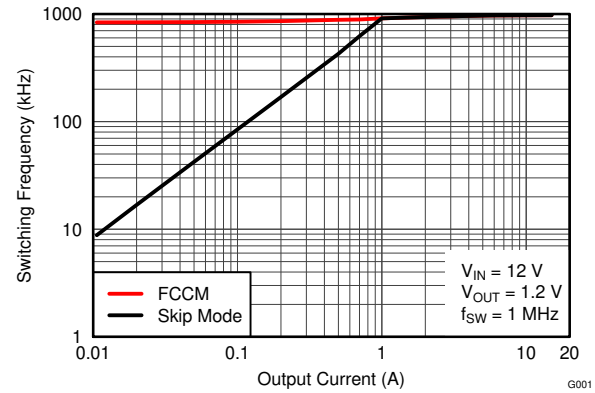
7-5. Switching Frequency vs. Output Current



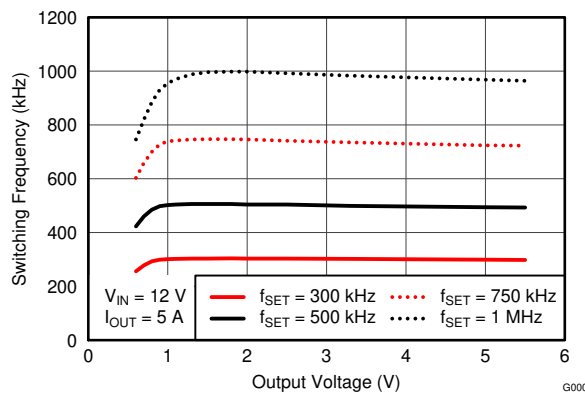
7-6. Switching Frequency vs. Output Current



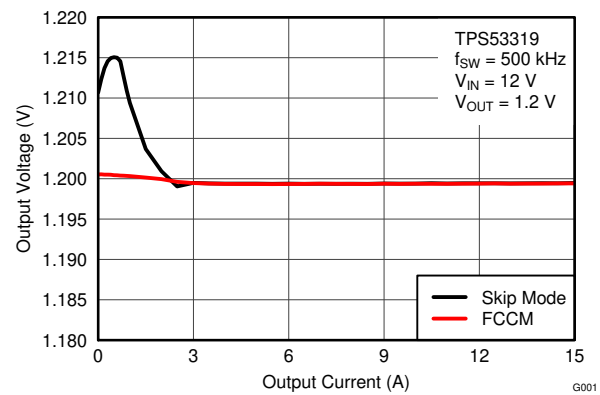
7-7. Switching Frequency vs. Output Current



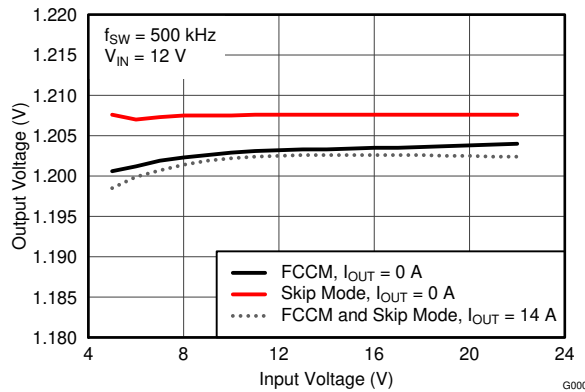
7-8. Switching Frequency vs. Output Current



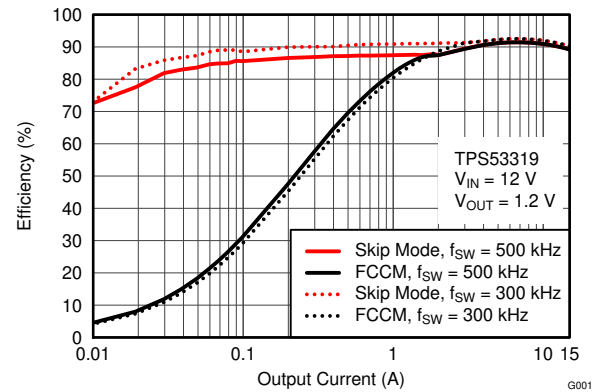
7-9. Switching Frequency vs. Output Voltage



7-10. Output Voltage vs. Output Current



7-11. Output Voltage vs. Input Voltage



7-12. Efficiency vs. Output Current

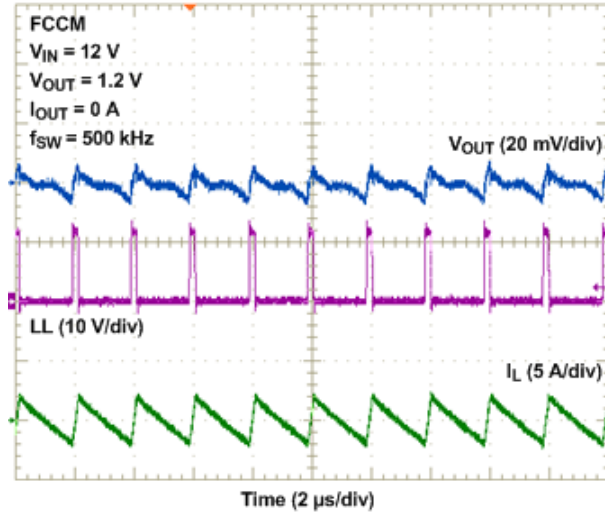


图 7-13. 1.2-V Output FCCM Mode Steady-State Operation

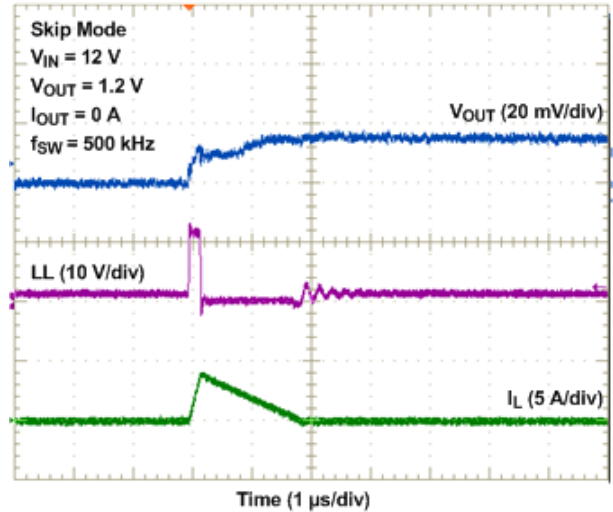


图 7-14. 1.2-V Output Skip Mode Steady-State Operation

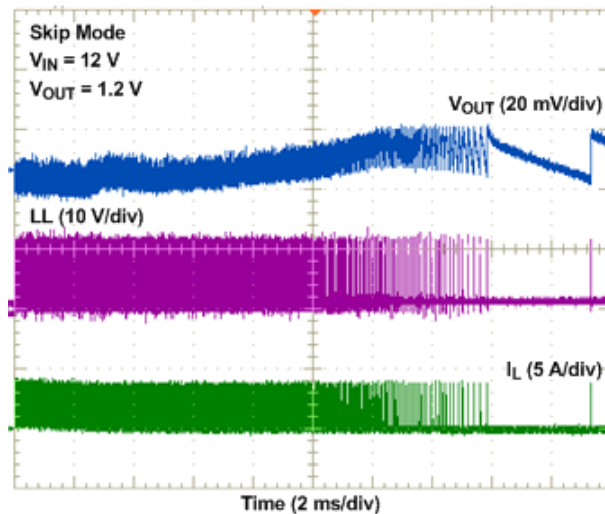


图 7-15. CCM to DCM Transition

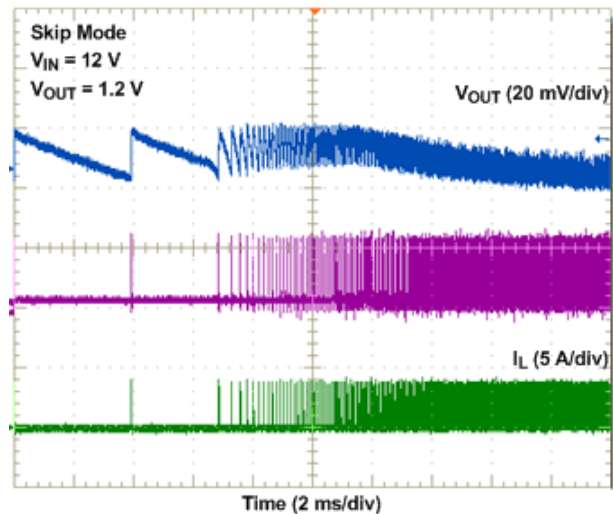
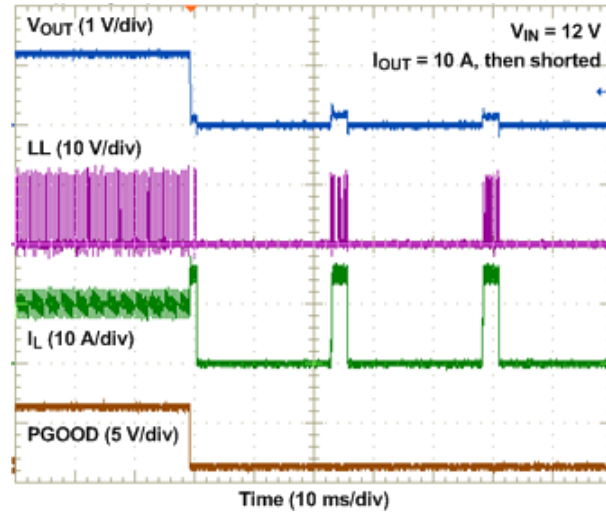
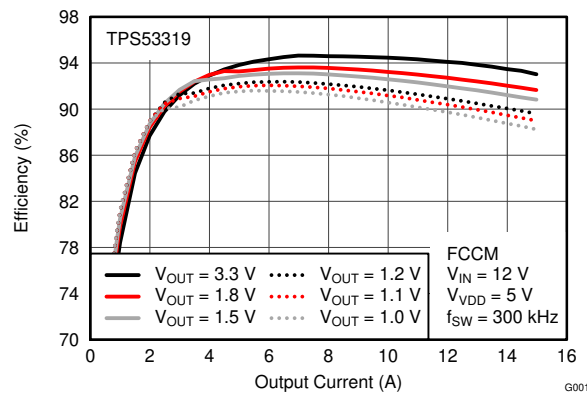


图 7-16. DCM to CCM Transition

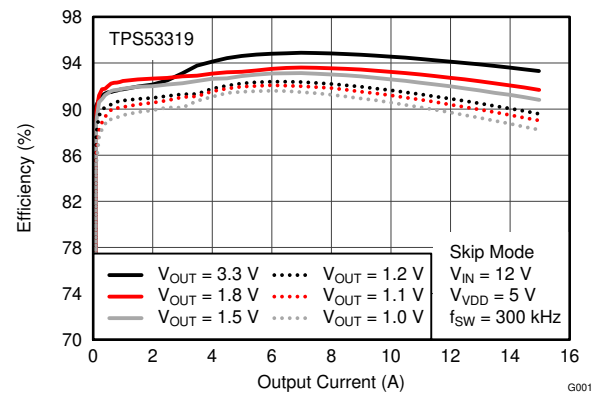



7-17. Short Circuit Protection

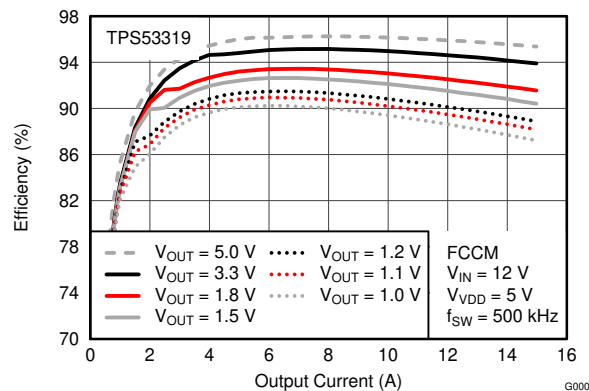
7.7 TPS53319 Typical Characteristics



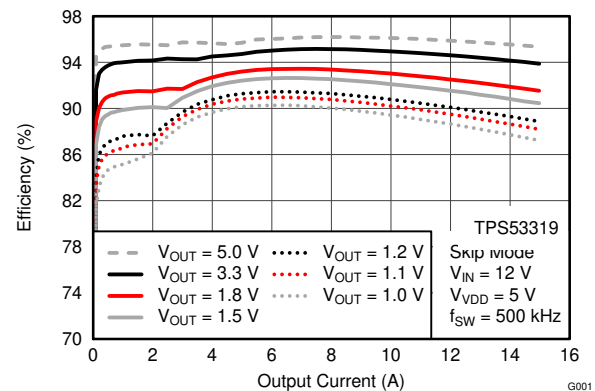
7-18. Efficiency vs Output Current



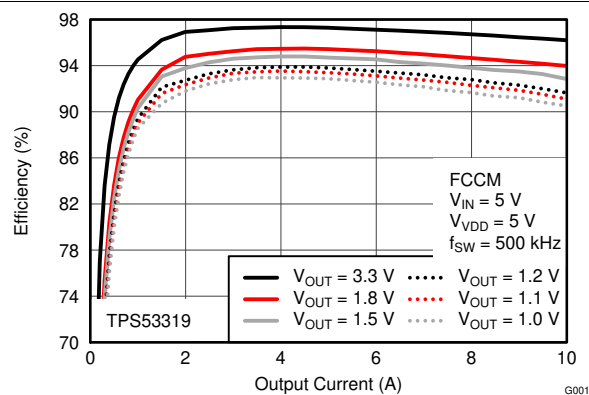
7-19. Efficiency vs Output Current



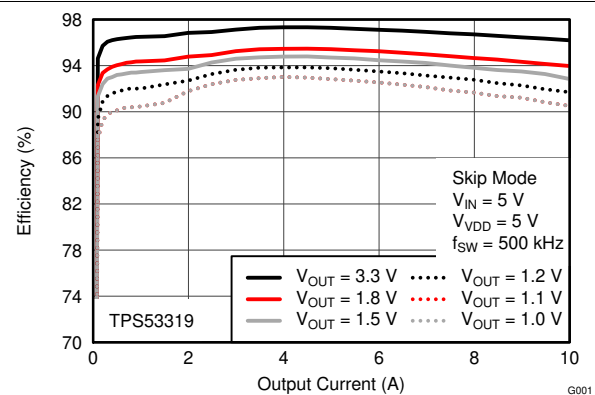
7-20. Efficiency vs Output Current



7-21. Efficiency vs Output Current

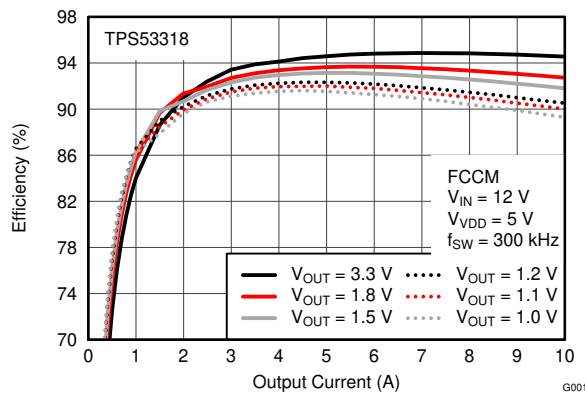


7-22. Efficiency vs Output Current

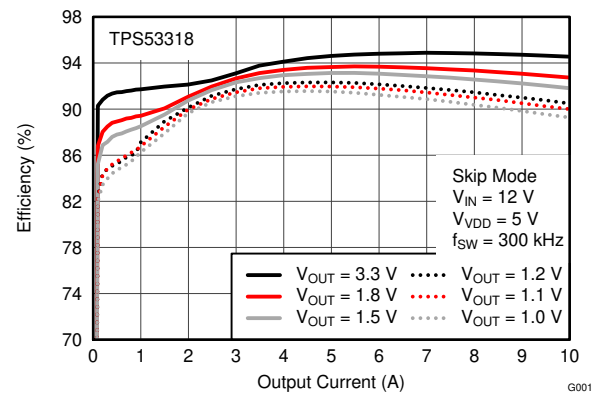


7-23. Efficiency vs Output Current

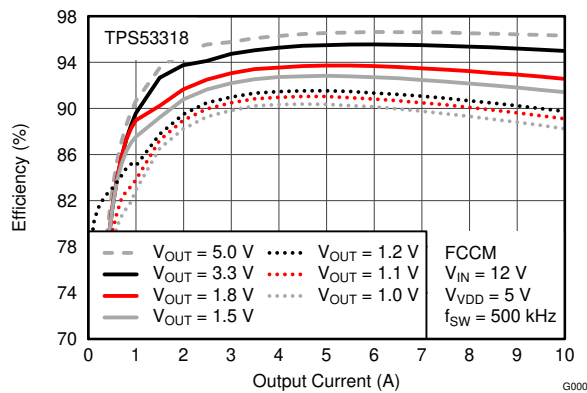
7.8 TPS53318 Typical Characteristics



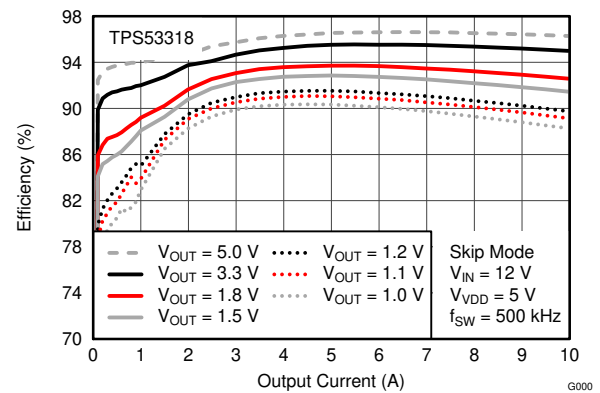
7-24. Efficiency vs Output Current



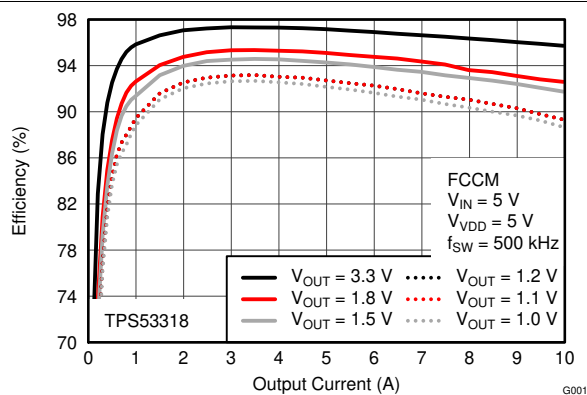
7-25. Efficiency vs Output Current



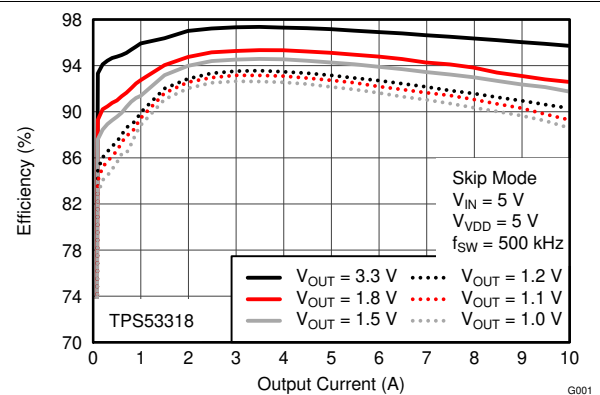
7-26. Efficiency vs Output Current



7-27. Efficiency vs Output Current



7-28. Efficiency vs Output Current



7-29. Efficiency vs Output Current

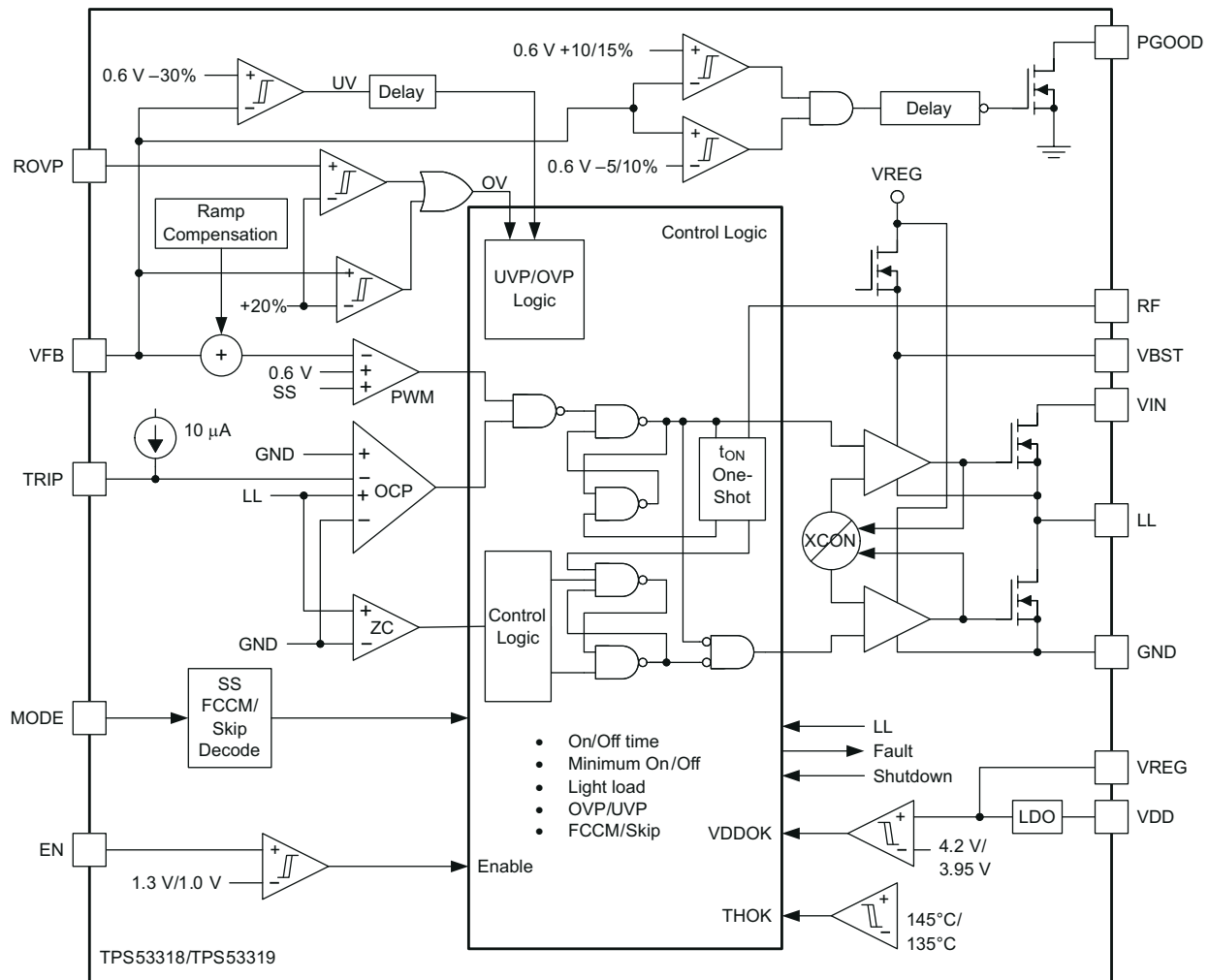
8 Detailed Description

8.1 Overview

The TPS53318 and TPS53319 devices are high-efficiency, single channel, synchronous buck converters suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V to 22 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP mode uses the equivalent series resistance (ESR) of the output capacitor or capacitors to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

These devices have a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms as shown in 表 8-3.

8.2 Functional Block Diagram



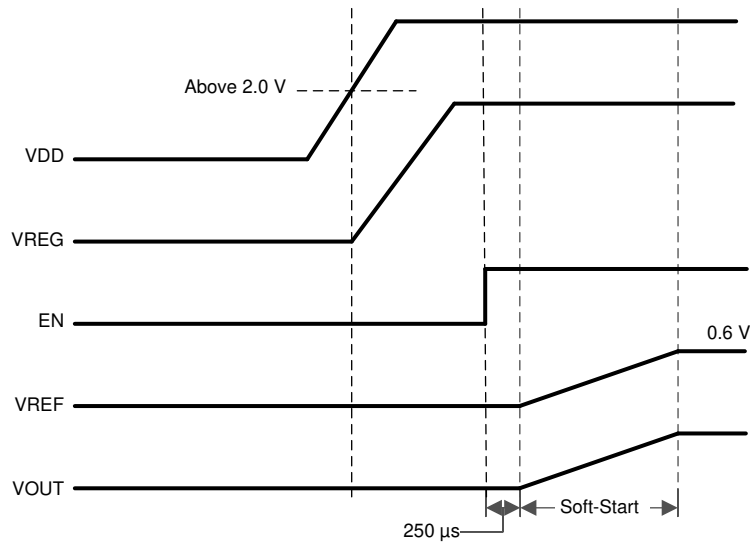
UDG-12041

A. The thresholds shown in [セクション 8.2](#) are typical values. Refer to [セクション 7.5](#) for threshold tolerance specifications.

8.3 Feature Description

8.3.1 5-V LDO and VREG Start-Up

Both the TPS53318 and TPS53319 devices provide an internal 5-V LDO function using input from VDD and output to VREG. When the VDD voltage rises above 2 V, the internal LDO is enabled and outputs voltage to the VREG pin. The VREG voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drives.



8-1. Power-Up Sequence Voltage Waveforms

Note

The 5-V LDO is not controlled by the EN pin. The LDO starts-up any time VDD rises to approximately 2 V (see [8-1](#)).

8.3.2 Adaptive On-Time D-CAP Control and Frequency Selection

Neither the TPS53318 nor the TPS53319 device have a dedicated oscillator to determine switching frequency. However, the device operates with pseudo-constant frequency by feedforwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage as shown in [式 1](#).

$$t_{ON} \propto \frac{V_{OUT}}{V_{IN}} \quad (1)$$

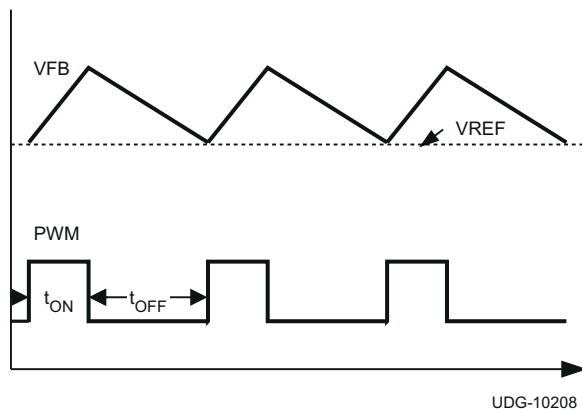
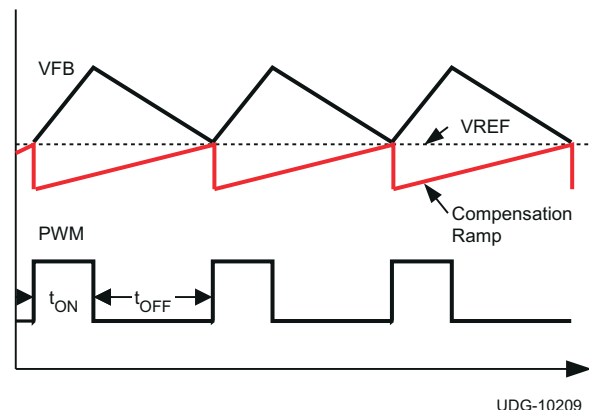
This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in [表 8-1](#). Maintaining open resistance sets the switching frequency to 500 kHz.

表 8-1. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS		SWITCHING FREQUENCY (f_{sw}) (kHz)
VALUE (k Ω)	CONNECT TO	
0	GND	250
187	GND	300
619	GND	400
OPEN	n/a	500
866	VREG	600
309	VREG	750
124	VREG	850
0	VREG	970

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a set signal to terminate the off-time (turn off the low-side MOSFET and turn on high-side the MOSFET). The set signal is valid if the inductor current level is below the OCP threshold, otherwise the off-time is extended until the current level falls below the threshold.

The waveforms shown in [Figure 8-2](#) show on-time control without ramp compensation. The waveforms shown in [Figure 8-3](#) show on-time control without ramp compensation.

**Figure 8-2. On-Time Control Without Ramp Compensation****Figure 8-3. On-Time Control With Ramp Compensation**

8.3.3 Ramp Signal

The TPS53318 and TPS53319 devices add a ramp signal to the 0.6-V reference in order to improve jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the signal-to-noise ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with -7 mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady state.

During skip mode operation, under discontinuous conduction mode (DCM), the switching frequency is lower than the nominal frequency and the off-time is longer than the off-time in CCM. Because of the longer off-time, the ramp signal extends after crossing 0 mV. However, it is clamped at 3 mV to minimize the DC offset.

8.3.4 Adaptive Zero Crossing

The TPS53318 and TPS53319 devices have an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off

timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

8.3.5 Output Discharge Control

When the EN pin becomes low, the TPS53318 and TPS53319 devices discharge the output capacitor using the internal MOSFET connected between the SW pin and the PGND pin while the high-side and low-side MOSFETs are maintained in the OFF state. The typical discharge resistance is 75 Ω. The soft discharge occurs only as EN becomes low. The discharge circuit is powered by VDD. While VDD remains high, the discharge circuit remains active.

8.3.6 Power-Good

The TPS53318 and TPS53319 devices have power-good output that indicates high when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within +10% and –5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-μs) internal delay. The power-good output is an open drain output and must be pulled up externally.

The power-good MOSFET is powered through the VDD pin. V_{VDD} must be >1 V in order to have a valid power-good logic. It is recommended to pull PGOOD up to VREG (or a voltage divided from VREG).

8.3.7 Current Sense, Overcurrent, and Short Circuit Protection

The TPS53318 and TPS53319 device offer cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the *OFF* state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, the TPS53319 device supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP} . The TRIP terminal sources current (I_{TRIP}) which is 10 μA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in 式 2.

$$V_{TRIP} (mV) = R_{TRIP} (k\Omega) \times I_{TRIP} (\mu A) \quad (2)$$

The inductor current is monitored by the LL pin. The GND pin is used as the positive current sensing node and the LL pin is used as the negative current sense node. The trip current, I_{TRIP} has a 3000ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. For each device, I_{TRIP} is also adjusted based on the device-specific on-resistance measurement in production tests to eliminate the any OCP variation from device to device. Duty-cycle should not be over 45% in order to provide the most accurate OCP.

As the comparison is made during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP} , can be calculated as shown in 式 3.

$$I_{OCP} = \frac{V_{TRIP}}{(32 \times R_{DS(on)})} + \frac{I_{IND(ripple)}}{2} = \frac{R_{TRIP}}{12.3 \times 10^3} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

where

- R_{TRIP} is in Ω

In an overcurrent or short-circuit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms plus 0.7 ms soft-start period), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

$$t_{HIC(wait)} = (2^n + 257) \times 4 \mu s \quad (4)$$

where

- $n = 8, 9, 10, \text{ or } 11$ depending on soft-start time selection

$$t_{\text{HIC(dly)}} = 7 \times (2^n + 257) \times 4 \mu\text{s} \quad (5)$$

表 8-2. Hiccup Timing

SELECTED SOFT-START TIME (t_{SS})(ms)	HICCUP WAIT TIME ($t_{\text{HIC(wait)}}$)(ms)	HICCUP DELAY TIME ($t_{\text{HIC(delay)}}$)(ms)
0.7	2.052	14.364
1.4	3.076	21.532
2.8	5.124	35.868
5.6	9.220	64.540

For the TPS53318 device, the OCP threshold is internally clamped to 10.5 A. The recommended R_{TRIP} value for the TPS53318 device is less than 150 k Ω .

8.3.8 Overvoltage and Undervoltage Protection

The TPS53318 and TPS53319 devices monitor the resistor divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the device latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (refer to 表 8-2). This function is enabled 1.5-ms after the soft start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. Before the latch-off action for both the high-side and low-side drivers, the output voltage must be pulled down below the UVP threshold voltage for a period of 1 ms. After the 1 ms period, the drivers are latched off.

8.3.9 Redundant Overvoltage Protection (OVP)

The TPS53318 and TPS53319 devices have a redundant input for OVP protection. The ROVP pin senses the voltage divided from output voltage and sends it to the OVP comparator. If this voltage is higher than 120% of the target voltage, the overvoltage protection engages and the low-side FET is turned on. When the output voltage is lower than the UVP threshold then the device latches off.

This redundant OVP function typically protects against a situation where the feedback loop is open or where a VFB pin short to GND exists. The ROVP pin has an internal 1.5-M Ω pulldown resistor.

Note

For an application that does not require a redundant OVP feature, tie the ROVP pin to GND. Do not leave ROVP pin floating.

8.3.10 UVLO Protection

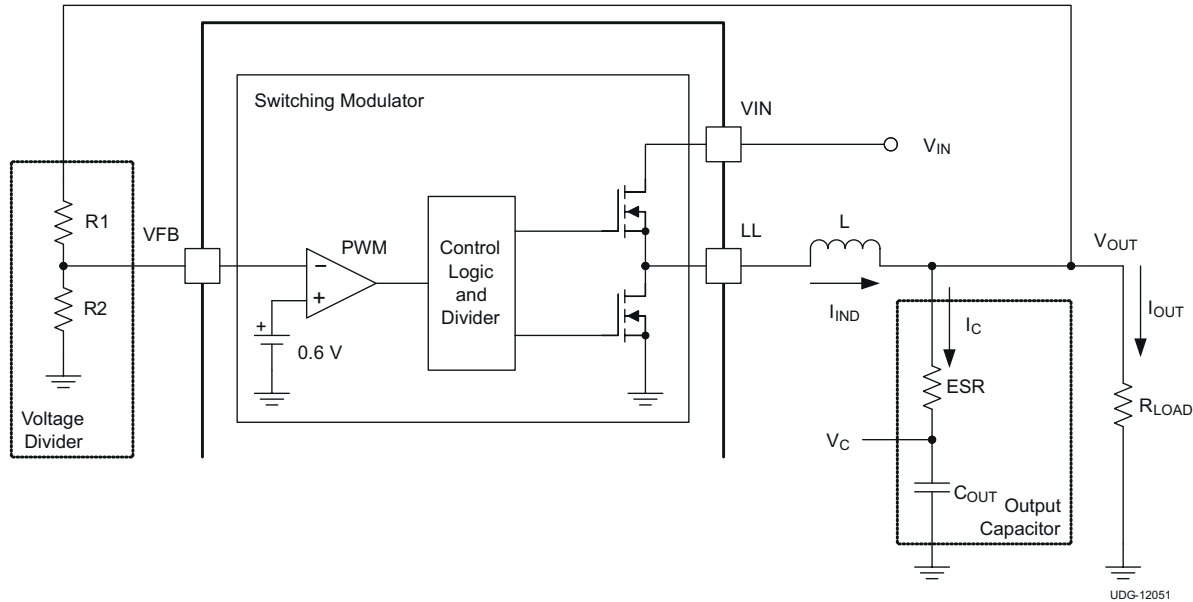
The TPS53318 and TPS53319 devices use VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than 3.95 V, the device shuts off. When the VREG voltage is higher than 4.2 V, the device restarts. This is a non-latch protection.

8.3.11 Thermal Shutdown

The TPS53318 and TPS53319 devices monitor the internal die temperature. If the temperature exceeds the threshold value (typically 145°C), the device shuts down. When the temperature falls about 10°C below the threshold value, the device will turn back on. This is a non-latch protection.

8.3.12 Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP mode can be simplified as shown in 图 8-4.



8-4. Simplified Modulator Model

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times ESR \times C_{OUT}} \quad (6)$$

For loop stability, the 0-dB frequency, f_0 , defined below needs to be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4} \quad (7)$$

According to 式 7, the loop stability of D-CAP mode modulator is mainly determined by the chemistry of the capacitor. For example, specialty polymer capacitors (SP-CAP) have an output capacitance in the order of several 100 μ F and ESR in range of 10 m Ω . These make f_0 on the order of 100 kHz or less, creating a stable loop. However, ceramic capacitors have an f_0 at more than 700 kHz, and need special care when used with this modulator. An application circuit for ceramic capacitor is described in セクション 8.3.13.

8.3.13 External Component Selection Using All Ceramic Output Capacitors

When a ceramic output capacitor is used, the stability criteria in 式 7 cannot be satisfied. The ripple injection approach as shown in 図 9-1 is implemented to increase the ripple on the VFB pin and make the system stable. In addition to the selections made using steps 1 through step 6 in セクション 9.2.1.2, the ripple injection components must be selected. The C2 value can be fixed at 1 nF. The value of C1 can be selected between 10 nF to 200 nF.

$$\frac{L \times C_{OUT}}{R7 \times C1} > N \times \frac{t_{ON}}{2} \quad (8)$$

where

- N is the coefficient to account for L and C_{OUT} variation

N is also used to provide enough margin for stability. It is recommended that $N = 2$ for $V_{OUT} \leq 1.8\text{ V}$ and $N = 4$ for $V_{OUT} \geq 3.3\text{ V}$ or when $L \leq 250\text{ nH}$. The higher V_{OUT} needs a higher N value because the effective output capacitance is reduced significantly with higher DC bias. For example, a 6.3-V, 22- μF ceramic capacitor may have only 8 μF of effective capacitance when biased at 5 V.

Because the VFB pin voltage is regulated at the valley, the increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from the VOUT pin and they can be calculated using 式 9 and 式 10 when neglecting the output voltage ripple caused by equivalent series inductance (ESL).

$$V_{INJ_SW} = \frac{V_{IN} - V_{OUT}}{R7 \times C1} \times \frac{D}{f_{SW}} \quad (9)$$

$$V_{INJ_OUT} = ESR \times I_{IND(ripple)} + \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (10)$$

It is recommended that V_{INJ_SW} to be less than 50 mV. If the calculated V_{INJ_SW} is higher than 50 mV, then other parameters need to be adjusted to reduce it. For example, C_{OUT} can be increased to satisfy 式 8 with a higher R7 value, thereby reducing V_{INJ_SW} .

The DC voltage at the VFB pin can be calculated by 式 11:

$$V_{VFB} = 0.6 + \frac{V_{INJ_SW} + V_{INJ_OUT}}{2} \quad (11)$$

And the resistor divider value can be determined by 式 12:

$$R1 = \frac{V_{OUT} - V_{VFB}}{V_{VFB}} \times R2 \quad (12)$$

8.4 Device Functional Modes

8.4.1 Enable, Soft Start, and Mode Selection

When the EN pin voltage rises above the enable threshold voltage (typically 1.3 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5 V at the VREG pin. The controller calibrates the switching frequency setting resistance attached to the RF pin during the first 250 μs . It then stores the switching frequency code in the internal registers. During this period, the MODE pin also senses the resistance attached to this pin and determines the soft-start time. Switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

Note

Enable voltage should not higher then VREG for 0.8 V.

表 8-3. Soft-Start and MODE Settings

MODE SELECTION	ACTION	SOFT-START TIME (t_{ss}) (ms)	R_{MODE} (k Ω)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475

表 8-3. Soft-Start and MODE Settings (continued)

MODE SELECTION	ACTION	SOFT-START TIME (t _{ss}) (ms)	R _{MODE} (kΩ)
Forced CCM ⁽¹⁾	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) Device enters FCCM after the PGOOD pin goes high when MODE is connected to PGOOD through the resistor R_{MODE}.

After the soft-start period begins, the MODE pin becomes the input of an internal comparator which determines auto skip or FCCM mode operation. If MODE voltage is higher than 1.3 V, the converter enters into FCCM mode. Otherwise it operates in auto skip mode at light-load condition. Typically, when FCCM mode is selected, the MODE pin connects to the PGOOD pin through the R_{MODE} resistor, so that before PGOOD goes high, the converter remains in auto skip mode.

8.4.2 Auto-Skip Eco-mode Light Load Operation

While R_{MODE} pulls the MODE pin low, the controller automatically reduces the switching frequency at light-load conditions to maintain high efficiency. More specifically, as the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light-load operation I_{OUT(LL)} (that is, the threshold between continuous and discontinuous conduction mode) can be calculated as shown in 式 13.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (13)$$

where

- f_{SW} is the PWM switching frequency

Switching frequency versus output current in the light-load condition is a function of L, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current from the I_{OUT(LL)} given in 式 13. For example, it is 60 kHz at I_{OUT(LL)}/5 if the frequency setting is 300 kHz.

8.4.3 Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency.

9 Application and Implementation

Note

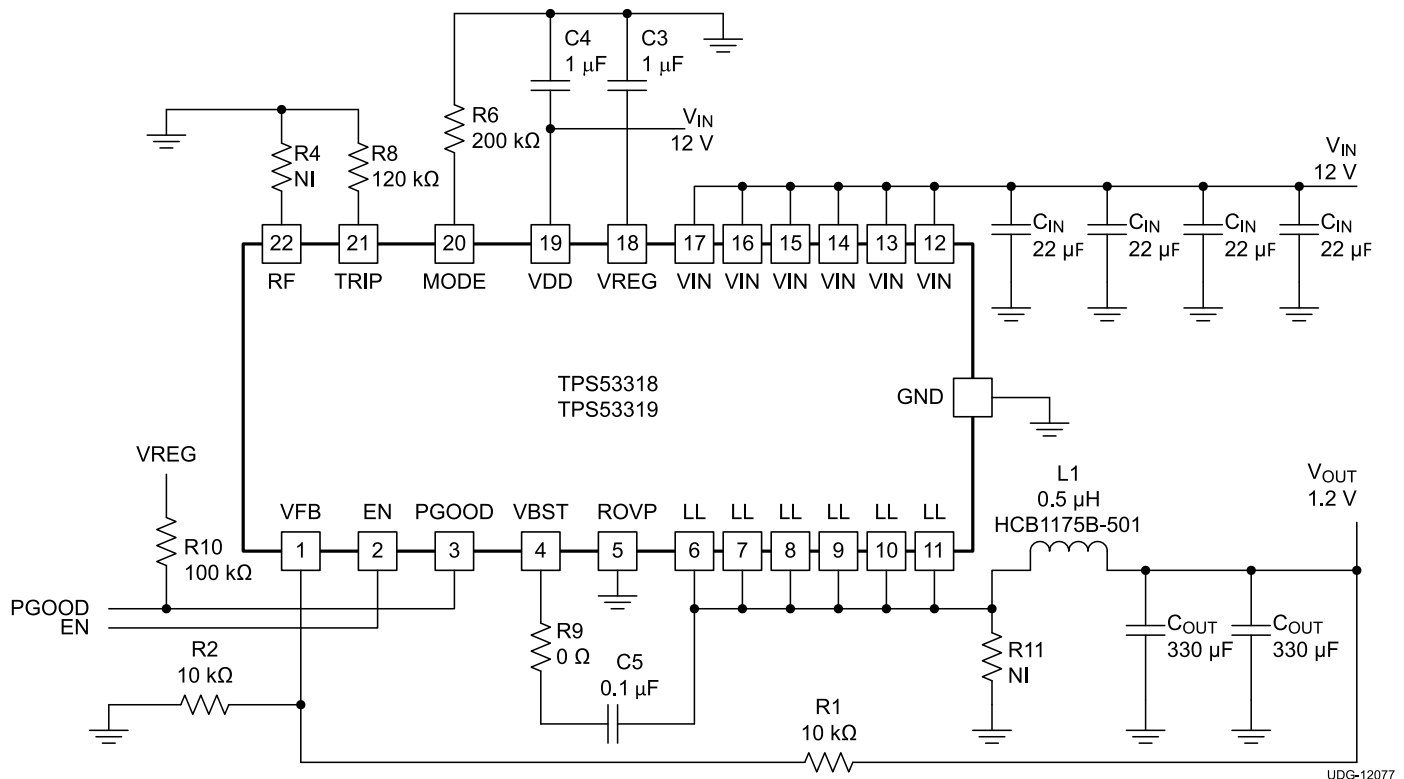
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS53318 and TPS53319 devices are high-efficiency, single channel, synchronous buck converters suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V to 22 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP mode uses the equivalent series resistance (ESR) of the output capacitor or capacitors to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network allowing for a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

9.2 Typical Applications

9.2.1 Application Using Bulk Output Capacitors, Redundant Overvoltage Protection Function (OVP) Disabled



9-1. Typical Application Circuit, Redundant Overvoltage Protection Disabled

9.2.1.1 Design Requirements

This design uses the parameters listed in [Table 9-1](#).

表 9-1. Design Specifications

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V _{IN}	Voltage range		5	12	18	V
I _{MAX}	Maximum input current	V _{IN} = 5 V, I _{OUT} = 8 A		2.5		A
	No load input current	V _{IN} = 12 V, I _{OUT} = 0 A with auto-skip mode		1		mA
OUTPUT CHARACTERISTICS						
V _{OUT}	Output voltage			1.2		V
	Output voltage regulation	Line regulation, 5 V ≤ V _{IN} ≤ 14 V with FCCM		0.2%		
		Load regulation, V _{IN} = 12 V, 0 A ≤ I _{OUT} ≤ 8 A with FCCM		0.5%		
V _{RIPPLE}	Output voltage ripple	V _{IN} = 12 V, I _{OUT} = 8 A with FCCM		10		mV _{pp}
I _{LOAD}	Output load current		0		8	A
I _{OVER}	Output overcurrent			11		
t _{SS}	Soft-start time			1		ms
SYSTEMS CHARACTERISTICS						
f _{SW}	Switching frequency			500	1000	kHz
η	Peak efficiency	V _{IN} = 12 V, V _{OUT} = 1.2 V, I _{OUT} = 4 A		91%		
	Full load efficiency	V _{IN} = 12 V, V _{OUT} = 1.2 V, I _{OUT} = 8 A		91.5%		
T _A	Operating temperature			25		°C

9.2.1.2 Detailed Design Procedure

The external components selection is a simple process when using organic semiconductors or special polymer output capacitors.

9.2.1.2.1 Step One: Select Operation Mode and Soft-Start Time

Select operation mode and soft-start time using [表 8-3](#).

9.2.1.2.2 Step Two: Select Switching Frequency

Select the switching frequency from 250 kHz to 1 MHz using [表 8-1](#).

9.2.1.2.3 Step Three: Choose the Inductor

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps ensure stable operation, but increases inductor core loss. Using 1/3 ripple current to maximum output current ratio, the inductance can be determined by [式 14](#).

$$L = \frac{1}{I_{\text{IND(ripple)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} = \frac{3}{I_{\text{OUT(max)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (14)$$

The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in [式 15](#).

$$I_{\text{IND(peak)}} = \frac{V_{\text{TRIP}}}{32 \times R_{\text{DS(on)}}} + \frac{1}{L \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (15)$$

9.2.1.2.4 Step Four: Choose the Output Capacitor or Capacitors

When organic semiconductor capacitor or capacitors or specialty polymer capacitor or capacitors are used, loop stability, capacitance, and ESR should satisfy 式 7. For jitter performance, 式 16 is a good starting point to determine ESR.

$$ESR = \frac{V_{OUT} \times 10\text{mV} \times (1-D)}{0.6\text{V} \times I_{IND(\text{ripple})}} = \frac{10\text{mV} \times L \times f_{SW}}{0.6\text{V}} = \frac{L \times f_{SW}}{60} (\Omega) \quad (16)$$

where

- D is the duty factor
- The required output ripple slope is approximately 10 mV per t_{SW} (switching period) in terms of VFB terminal voltage

9.2.1.2.5 Step Five: Determine the Value of R1 and R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in 图 8-4. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is from 10 kΩ to 20 kΩ. Determine R1 using 式 17.

$$R1 = \frac{V_{OUT} - \frac{I_{IND(\text{ripple})} \times ESR}{2} - 0.6}{0.6} \times R2 \quad (17)$$

9.2.1.2.6 Step Six: Choose the Overcurrent Setting Resistor

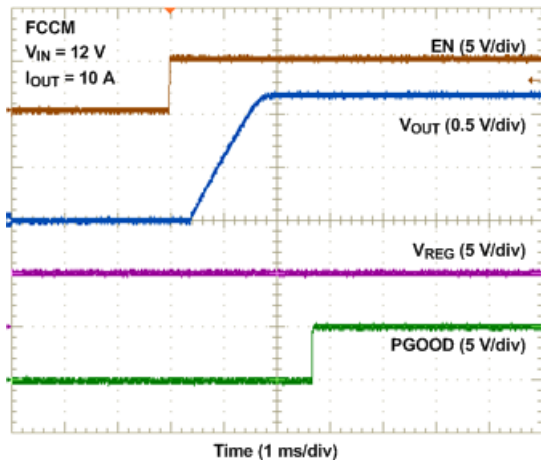
The overcurrent setting resistor, R_{TRIP} , can be determined by 式 18.

$$R_{TRIP} = \left(I_{OCP} - \left(\frac{1}{2 \times L \times f_{SW}} \right) \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \right) \times 12.3 \quad (18)$$

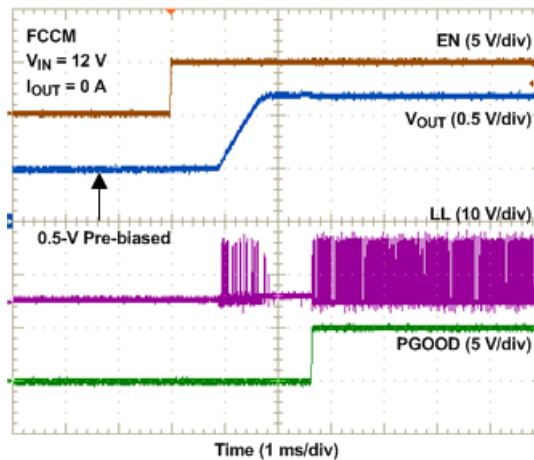
where

- R_{TRIP} is in kΩ

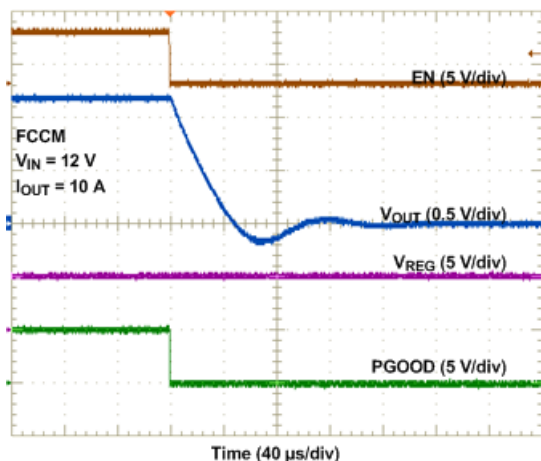
9.2.1.3 Application Curves



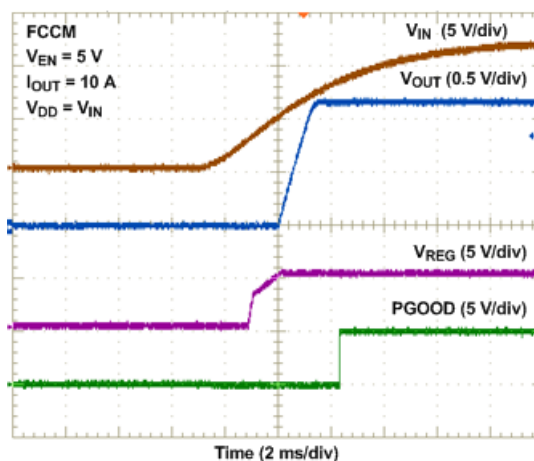
9-2. Start-Up



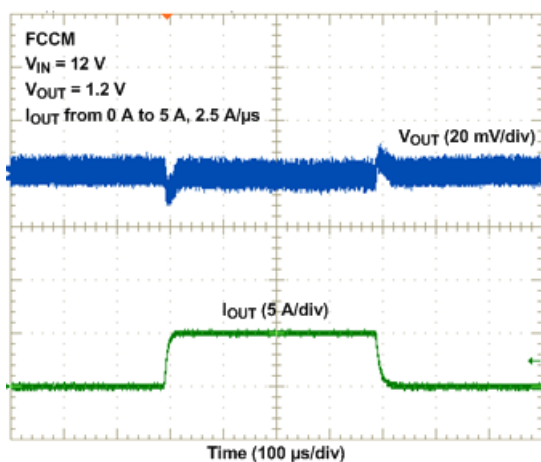
9-3. Pre-Bias Start-Up



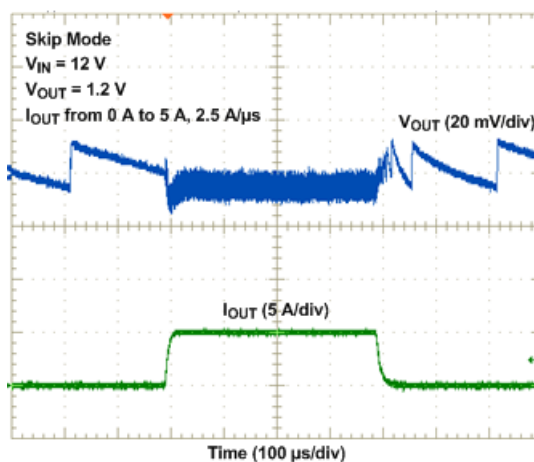
9-4. Shutdown



9-5. UVLO Start-Up



9-6. FCCM Load Transient



9-7. Skip Mode Load Transient

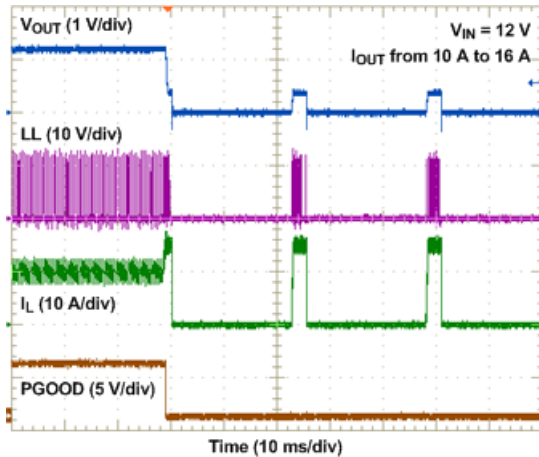


图 9-8. Overcurrent Protection

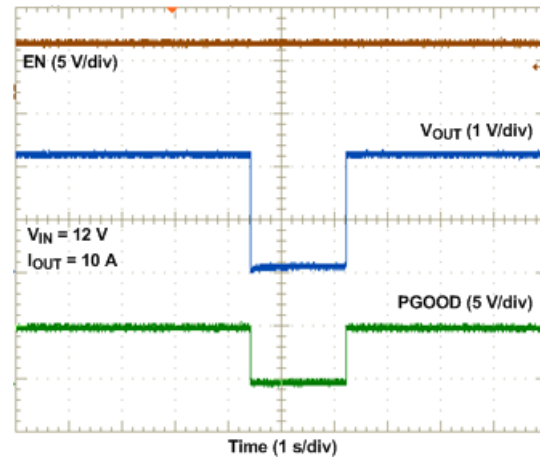
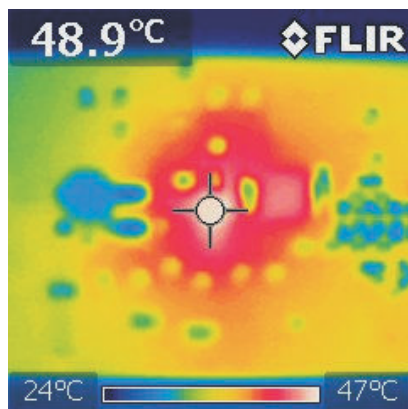
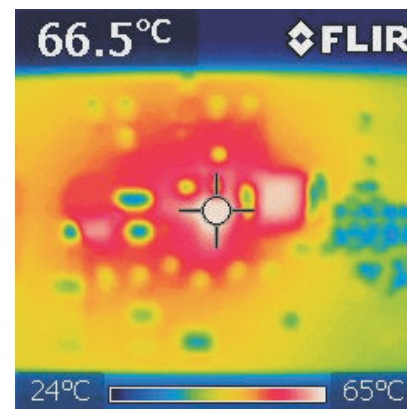


图 9-9. Overtemperature Protection



TPS53319 EVM $V_{IN} = 12\text{ V}$ $V_{OUT} = 1.2\text{ V}$
 $I_{OUT} = 14\text{ A}$ $f_{SW} = 500\text{ kHz}$ $T_A = 25^\circ\text{C}$
 No airflow

图 9-10. Thermal Signature



TPS53319 EVM $V_{IN} = 12\text{ V}$ $V_{OUT} = 5\text{ V}$
 $I_{OUT} = 14\text{ A}$ $f_{SW} = 500\text{ kHz}$ $T_A = 25^\circ\text{C}$
 No airflow

图 9-11. Thermal Signature

9.2.2 Application Using Ceramic Output Capacitors, Redundant Overvoltage Protection Function (OVP) Enabled



9-12. Typical Application Circuit, Redundant OVP Enabled

9.2.2.1 Design Requirements

This design uses the parameters listed in 表 9-1.

9.2.2.2 Detailed Design Procedure

The detailed design procedure for this design example is similar to the procedure for the previous design example. The differences are discussed in the following two sections.

9.2.2.2.1 External Component Selection Using All Ceramic Output Capacitors

Refer to [セクション 8.3.13](#) for guidelines for this design with all ceramic output capacitors.

9.2.2.2.2 Redundant Overvoltage Protection

The redundant overvoltage level is programmed according to the output voltage setting, it is controlled by resistors R11 and R12 as shown in [Figure 9-12](#). Connect resistor R11 between the ROVP pin and the output, and connect resistor R12 between the ROVP pin and GND. This design recommends that the value of resistor R11 match the value of resistor R1 (or slightly higher), and that the value of resistor R2 match the value of resistor R12.

9.2.2.3 Application Curves

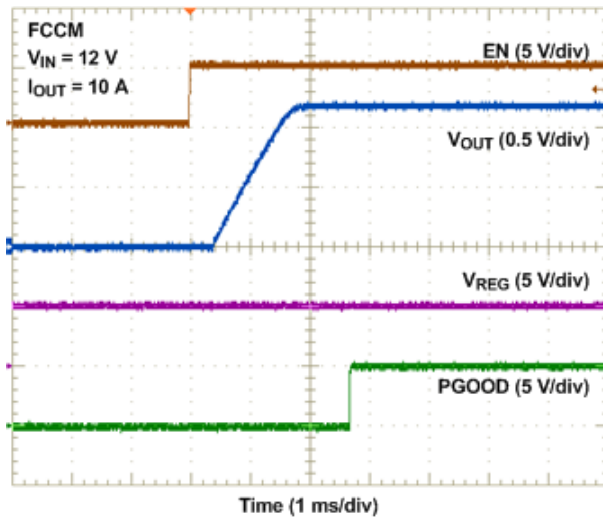


図 9-13. Start-Up

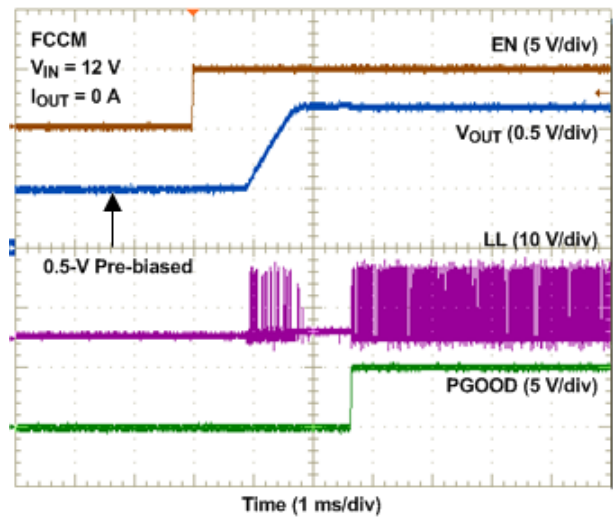


図 9-14. Pre-Bias Start-Up

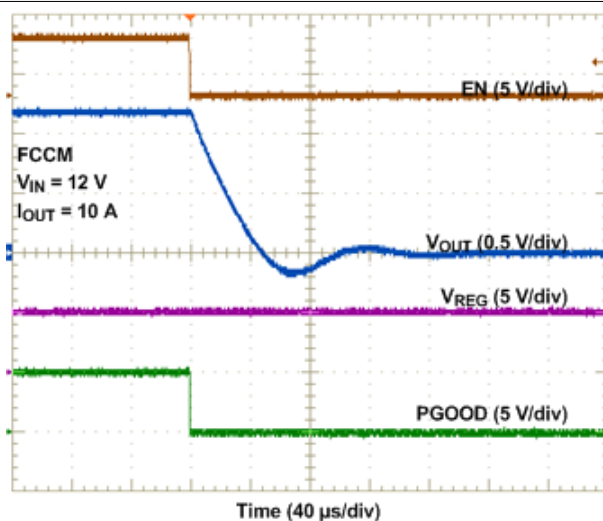


図 9-15. Shutdown

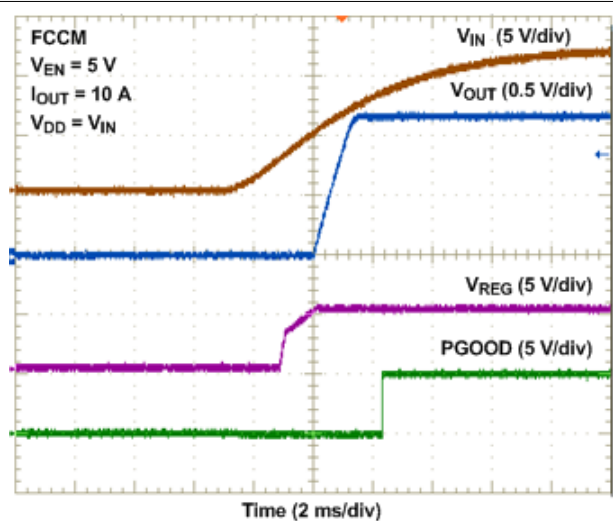


図 9-16. UVLO Start-Up

10 Power Supply Recommendations

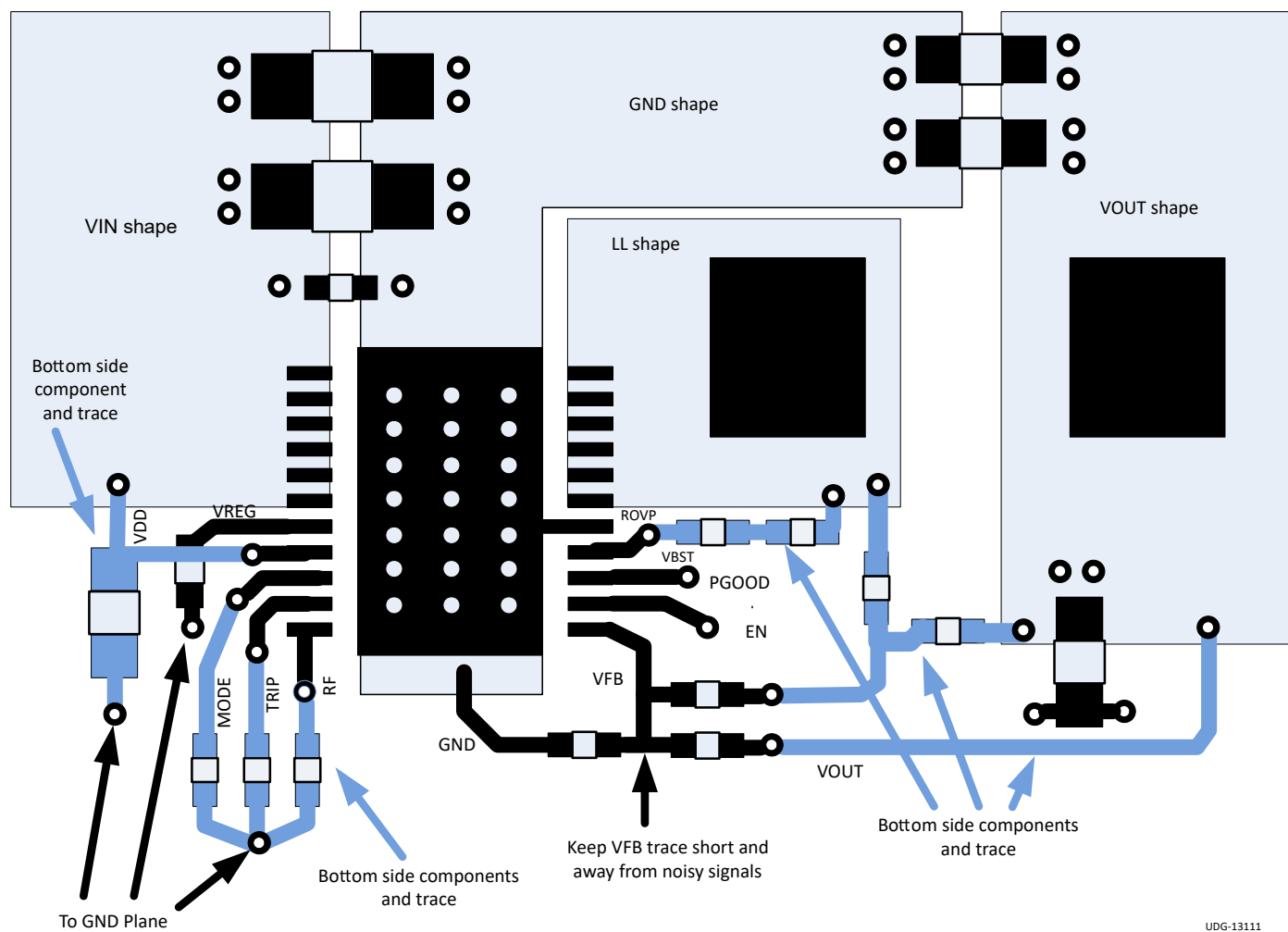
The devices are designed to operate from an input voltage supply range between 1.5 V and 22 V (4.5 V to 25 V biased). This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in [セクション 11](#).

11 Layout

11.1 Layout Guidelines

- The power components (including input/output capacitors, inductor, and TPS53318 or TPS53319 device) should be placed on one side of the PCB (solder side). At least one inner plane should be inserted, connected to ground, to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE, and RF should be placed away from high-voltage switching nodes such as LL, VBST to avoid coupling. Use internal layer or layers as ground plane or planes and shield feedback trace from power traces and components.
- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop.
- Because the TPS53319 device controls output voltage referring to voltage across the VOUT capacitor, the top-side resistor of the voltage divider should be connected to the positive node of the VOUT capacitor. The GND of the bottom side resistor should be connected to the GND pad of the device. The trace from these resistors to the VFB pin should be short and thin.
- Place the frequency setting resistor (R_F), OCP setting resistor (R_{TRIP}), and mode setting resistor (R_{MODE}) as close to the device as possible. Use the common GND via to connect them to GND plane if applicable.
- Place the VDD and VREG decoupling capacitors as close to the device as possible. Ensure to provide GND vias for each decoupling capacitor and make the loop as small as possible.
- For better noise filtering on VDD, a dedicated and localized decoupling support is strongly recommended.
- The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor, should be as short and wide as possible.
- Connect the ripple injection V_{OUT} signal (V_{OUT} side of the C1 capacitor in [Figure 9-12](#)) from the terminal of ceramic output capacitor. The AC coupling capacitor (C2 in [Figure 9-12](#)) should be placed near the device, and R7 and C1 can be placed near the power stage.
- Use separated vias or trace to connect LL node to snubber, boot strap capacitor, and ripple injection resistor. Do not combine these connections.

11.2 Layout Example



UDG-13111

✎ 11-1. Layout Recommendation

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- Reference Design: 7-V to 12-V Input, 1.2-V Output, 8-A Step-Down Converter for Powering Rails in Altera Arria V FPGA, [PMP8824](#)
- Evaluation Module: Synchronous Switcher with Integrated MOSFETs, [TPS53319EVM-136](#)
- TPS53318 TINA-TI Transient Spice Model, [SLUM381](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS53318DQPR	Active	Production	LSON-CLIP (DQP) 22	2500 LARGE T&R	ROHS Exempt	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	53318DQP
TPS53318DQPR.A	Active	Production	LSON-CLIP (DQP) 22	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53318DQP
TPS53318DQPR.B	Active	Production	LSON-CLIP (DQP) 22	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS53318DQPRG4	Active	Production	LSON-CLIP (DQP) 22	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53318DQP
TPS53318DQPRG4.A	Active	Production	LSON-CLIP (DQP) 22	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53318DQP
TPS53318DQPRG4.B	Active	Production	LSON-CLIP (DQP) 22	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS53318DQPT	Active	Production	LSON-CLIP (DQP) 22	250 SMALL T&R	ROHS Exempt	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	53318DQP
TPS53318DQPT.A	Active	Production	LSON-CLIP (DQP) 22	250 SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53318DQP
TPS53318DQPT.B	Active	Production	LSON-CLIP (DQP) 22	250 SMALL T&R	-	Call TI	Call TI	-40 to 125	
TPS53319DQPR	Active	Production	LSON-CLIP (DQP) 22	2500 LARGE T&R	ROHS Exempt	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	53319DQP
TPS53319DQPR.A	Active	Production	LSON-CLIP (DQP) 22	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53319DQP
TPS53319DQPR.B	Active	Production	LSON-CLIP (DQP) 22	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS53319DQPT	Active	Production	LSON-CLIP (DQP) 22	250 SMALL T&R	ROHS Exempt	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	53319DQP
TPS53319DQPT.A	Active	Production	LSON-CLIP (DQP) 22	250 SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53319DQP
TPS53319DQPT.B	Active	Production	LSON-CLIP (DQP) 22	250 SMALL T&R	-	Call TI	Call TI	-40 to 125	
TPS53319DQPTG4	Active	Production	LSON-CLIP (DQP) 22	250 SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53319DQP
TPS53319DQPTG4.A	Active	Production	LSON-CLIP (DQP) 22	250 SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53319DQP
TPS53319DQPTG4.B	Active	Production	LSON-CLIP (DQP) 22	250 SMALL T&R	-	Call TI	Call TI	-40 to 125	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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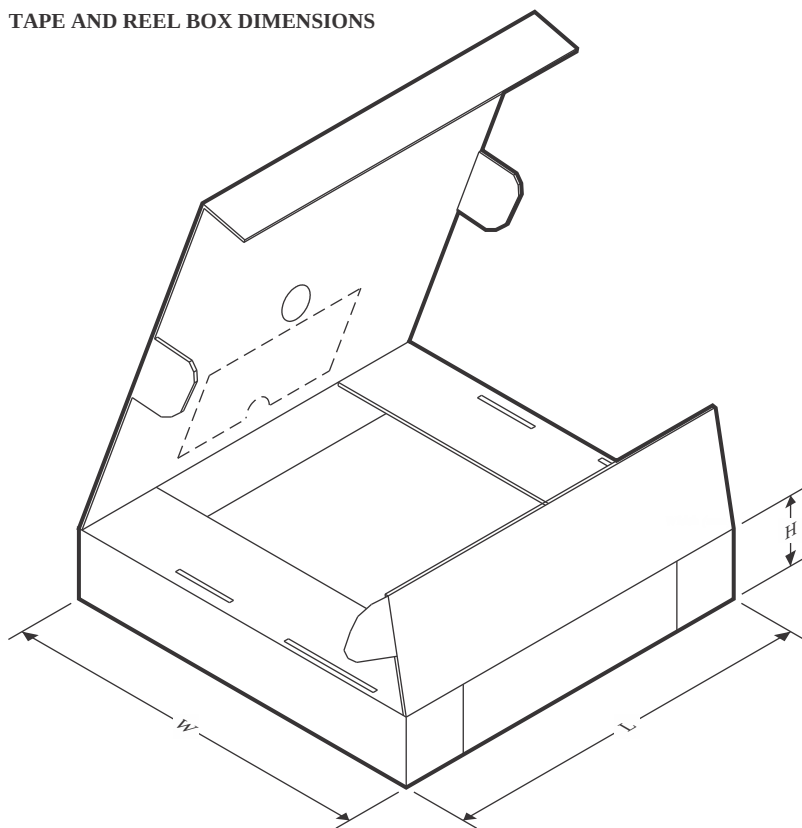
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53318DQPR	LSON-CLIP	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53318DQPRG4	LSON-CLIP	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53318DQPT	LSON-CLIP	DQP	22	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53319DQPR	LSON-CLIP	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53319DQPT	LSON-CLIP	DQP	22	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53319DQPTG4	LSON-CLIP	DQP	22	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

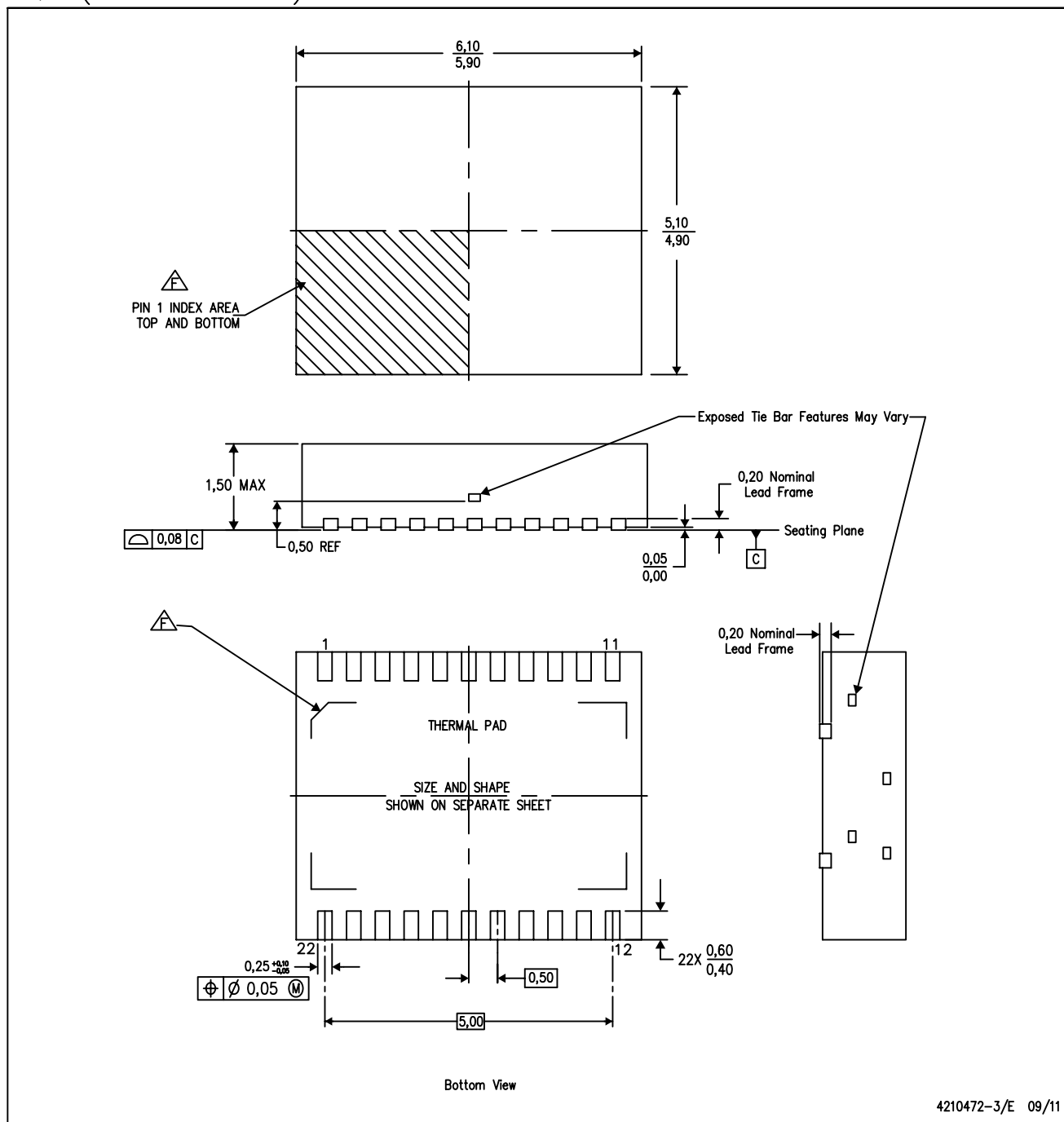


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53318DQPR	LSON-CLIP	DQP	22	2500	346.0	346.0	33.0
TPS53318DQPRG4	LSON-CLIP	DQP	22	2500	346.0	346.0	33.0
TPS53318DQPT	LSON-CLIP	DQP	22	250	210.0	185.0	35.0
TPS53319DQPR	LSON-CLIP	DQP	22	2500	346.0	346.0	33.0
TPS53319DQPT	LSON-CLIP	DQP	22	250	210.0	185.0	35.0
TPS53319DQPTG4	LSON-CLIP	DQP	22	250	210.0	185.0	35.0

DQP (R-PSON-N22)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

THERMAL PAD MECHANICAL DATA

DQP (R-PSON-N22)

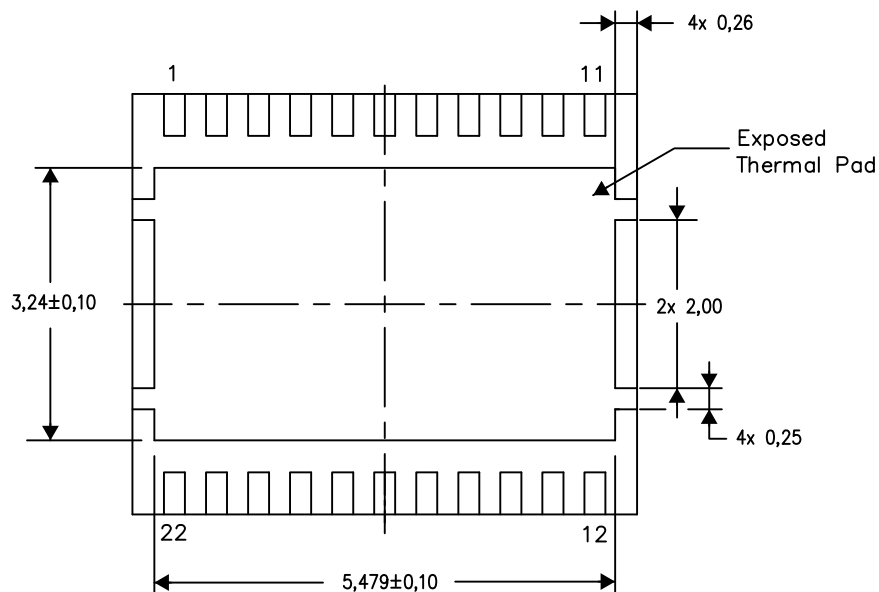
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

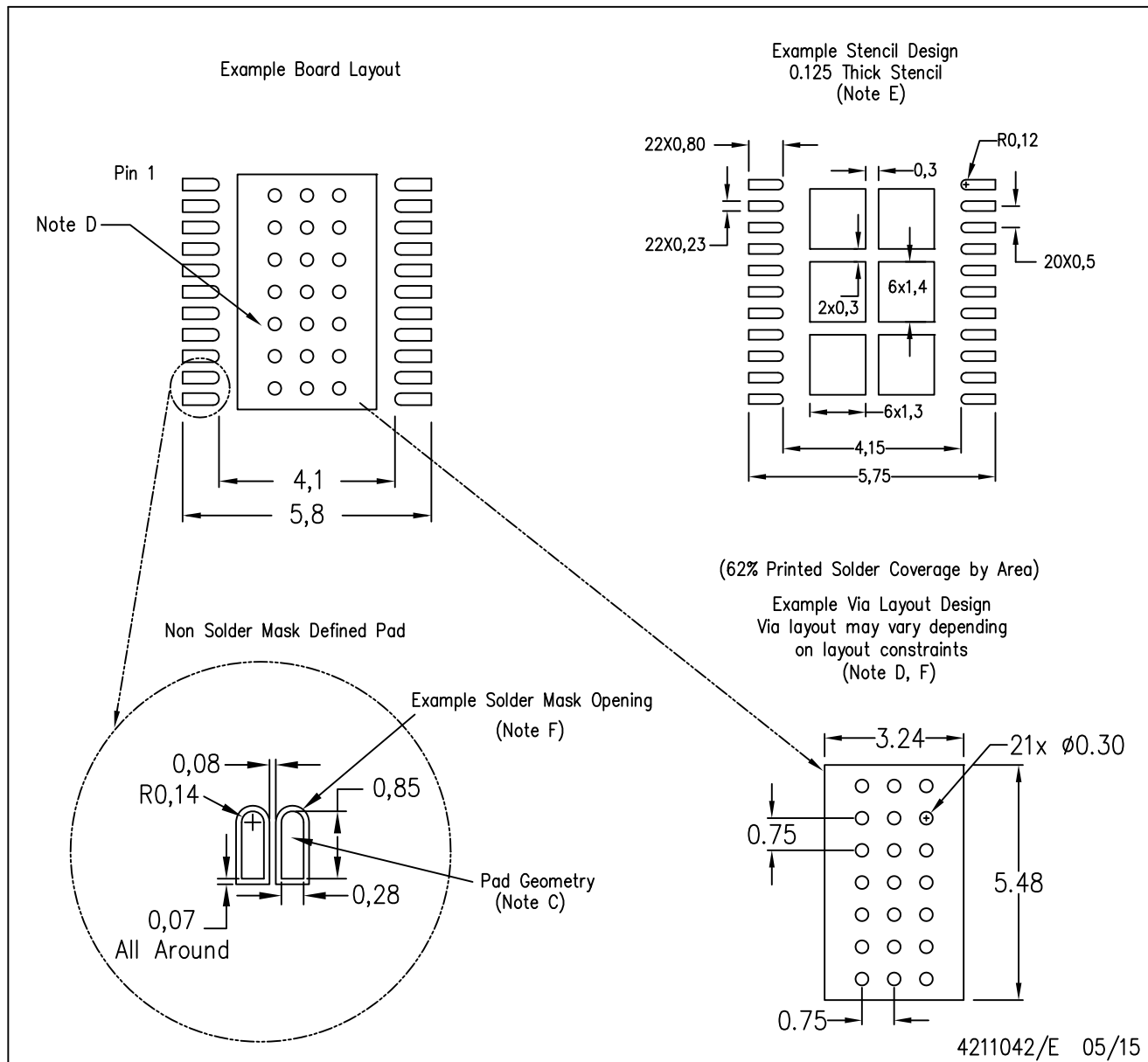
Exposed Thermal Pad Dimensions

4211024-3/H 08/15

NOTE: All linear dimensions are in millimeters

DQP (R-PSO-N22)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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