TPS482H85-Q1: 48V, 85mΩ Automotive Dual-Channel Smart High-Side Switch

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Functional safety capable
  - Documentation available to aid functional safety system design
- Dual-channel 85mΩ smart high-side switch with full diagnostics
- Wide operating voltage: 6V to 58V
- Ultra-low standby current, < 2µA per channel
- High-accuracy current sense: < ±10% for > 50mA
- Selectable current limit levels with external resistor
- Protection features:
  - Short-to-GND protection by current limit
  - Absolute and relative thermal shutdown
  - Inductive Load negative voltage clamp with optimized slew rate
  - Loss-of-ground, loss-of-battery, and reverse battery protection
- Diagnostics features:
  - Overcurrent and short-to-ground detection
  - Open-load and short-to-battery detection
  - Accurate current sense
- 3.5mm × 3mm small form factor 12-pin QFN package

2 Applications

- Body control module
- Zone control module
- ADAS modules
- Automotive lighting

3 Description

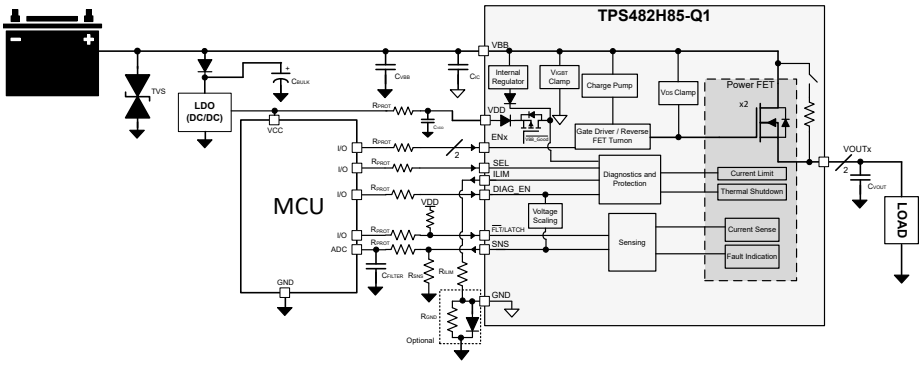
The TPS4H82H85-Q1 device is fully protected dual-channel smart high-side switch with two integrated 85mΩ NMOS power FETs, intended for 24V and 48V automotive systems. The low R_{ON} minimizes the device power dissipation when driving a wide range of output load current up to 2.2A when both channels are enabled or 3A when only one channel is enabled. Protection and diagnostic features include accurate current sense, selectable current limit levels, OFF-state open-load, short-to-battery detection, output clamp, and thermal shutdown.

The device provides an accurate load current sense that allows for improved load diagnostics such as overload and open-load detection, which enables better predictive maintenance, without further calibration. The device also implements a selectable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. The TPS4H82H85-Q1 device can be used as a high-side power switch for a wide variety of resistive, inductive, and capacitive loads, including low-wattage bulbs, LEDs, relays, solenoids, and heaters.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS482H85-Q1	CHU (VQFN-HR, 12)	3.5mm × 3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

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4 Device Comparison Table

PART NUMBER	UNIQUE PIN	NOTE	CLAMP STRUCTURE	VBB VOLTAGE TOLERANCE
TPS482H85A-Q1	LATCH	• User is able to configure the device behavior after a thermal fault (latch or auto-retry) using the LATCH pin. • Fault status can be reported through SNS pin.	Bi-directional clamp for clamping both positive VBB or negative VOUT voltage.	Max 65V steady state. Max 100µs transient up to 80V.
TPS482H85B-Q1	$\overline{\text{FLT}}$	• User is able to read the global fault status through $\overline{\text{FLT}}$ pin. • Device auto-retries after a thermal fault.	Bi-directional clamp for clamping both positive VBB or negative VOUT voltage.	Max 65V steady state. Max 100µs transient up to 80V.
TPS482H85C-Q1(1)	LATCH	• User is able to configure the device behavior after a thermal fault - latch or auto-retry using the LATCH pin. • Fault status can be reported through SNS pin.	Uni-directional clamp for clamping negative VOUT voltage.	Max 70V steady state. No transient beyond 70V.

(1) Device in preview. Please contact TI for more information.

5 Pin Configuration and Functions

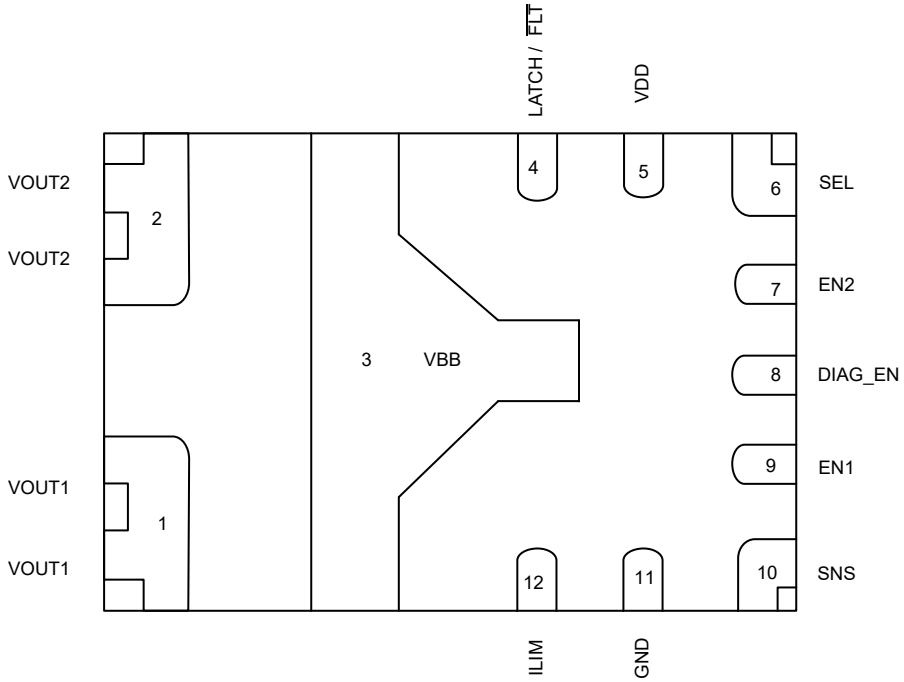


Figure 5-1. CHU Package 12-Pin VQFN-HR Top View

Table 5-1. Pin Functions

See Applications Section for full list of recommended components

PIN			TYPE	DESCRIPTION
NO.	NAME (Ver. A/C)	NAME (Ver. B)		
1	VOUT1	VOUT1	O	Channel 1 output.
2	VOUT2	VOUT2	O	Channel 2 output.
3	VBB	VBB	POWER	Input power supply.
4	LATCH	$\overline{FLT}$	I for LATCH, O for $\overline{FLT}$	• LATCH: High to latch OFF device after thermal shutdown; low to auto-retry. Internally pulled down. • $\overline{FLT}$: Open drain global fault pin.
5	VDD	VDD	POWER	Low voltage supply input. Float to enable the internal regulator.
6	SEL	SEL	I	Selects the channel for fault and current sense output on the SNS pin. Low to select channel 1; high to select channel 2. Internally pulled down.
7	EN2	EN2	I	Enable signal for channel 2. Internally pulled down.
8	DIAG_EN	DIAG_EN	I	High to enable ON state current sense and fault reporting through SNS pin, and OFF-state open load detection. Low to disable the diagnostics. Internally pulled down.
9	EN1	EN1	I	Enable signal for channel 1. Internally pulled down.
10	SNS	SNS	O	Outputs value based on sense ratio; also shows fault status by going high.

Table 5-1. Pin Functions (continued)

See Applications Section for full list of recommended components

PIN			TYPE	DESCRIPTION
NO.	NAME (Ver. A/C)	NAME (Ver. B)		
11	GND	GND	GND	Ground of device. Connect to resistor and diode ground network for reverse battery protection.
12	ILIM	ILIM	O	Adjustable current limit. Select the current limit by connecting a resistor from ILIM to IC GND. Leave the pin floating or short the pin to IC GND for two additional levels.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum continuous supply voltage, V_{BB} (Version A, B)			65	V
VBB transient overvoltage (Version A, B)	Maximum 100 µs duration		80	V
Maximum continuous supply voltage, V_{BB} (Version C)			70	V
Maximum continuous supply voltage, V_{DD}			7	V
Reverse Polarity Voltage, maximum duration of 3 minutes and with the application circuit		-28		V
Enable pin current, I_{ENx}		–1	20	mA
Enable pin voltage, V_{ENx}		–1	7	V
Diagnostic Enable pin current, I_{DIAG_EN}		–1	20	mA
Diagnostic Enable pin voltage, V_{DIAG_EN}		–1	7	V
LATCH pin voltage, V_{LATCH} (Version A, C)		–1	70 (2)	V
LATCH pin current, I_{LATCH} (Version A, C)		–1	20	mA
SEL pin voltage, V_{SEL}		–1	7	V
SEL pin current, I_{SEL}		–1	20	mA
Sense pin current, I_{SNS}		–100	10	mA
ILIM pin voltage, V_{ILIM}		–1	70 (2)	V
ILIM pin current, I_{ILIM}		–1	20	mA
Sense pin voltage, V_{SNS}		–1	5.5	V
FLT pin current, I_{FLT} (Version B)		-30	10	mA
FLT pin voltage, V_{FLT} (Version B)		–0.3	70 (2)	V
Reverse ground current, I_{GND}	V_{BB} < 0 V, Max 2ms negative supply transient		-50	mA
Energy dissipation during turnoff, E_{TOFF}	Singe pulse, one channel, L_{OUT} = 5 mH, VBB = 32 V, $T_{J,start}$ = 125°C		70(3)	mJ
Energy dissipation during turnoff, E_{TOFF}	Singe pulse, one channel, L_{OUT} = 5 mH, VBB = 54 V, $T_{J,start}$ = 125°C		85(3)	mJ
Energy dissipation during turnoff, E_{TOFF}	Repetitive pulse, one channel, L_{OUT} = 5 mH, VBB = 32 V, $T_{J,start}$ = 125°C		25(3)	mJ
Energy dissipation during turnoff, E_{TOFF}	Repetitive pulse, one channel, L_{OUT} = 5 mH, VBB = 54 V, $T_{J,start}$ = 125°C		28(3)	mJ
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) These pins are adjacent to pins that will handle high-voltages. In the event of a pin-to-pin short, there will not be device damage.
(3) For further details, see the section regarding switch-off of an inductive load.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per AEC Q100-002 Classification Level 2(2)	All pins except VBB and VOUT	±2000	V
			VBB and VOUT	±4000	
		Charged-device model (CDM), per AEC Q100-011 Classification Level C5	All pins	±750	

(1) All ESD strikes are with reference from the pin mentioned to GND

(2) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{VDD_NOM}	VDD Nominal supply voltage	4.5	5.5	V
V_{VBB_NOM}	VBB Nominal supply voltage	6	58	V
V_{VBB_SC}	VBB Short circuit supply voltage capability		58	V
V_{ENx}	Enable voltage	–1	5.5	V
V_{DIAG_EN}	Diagnostic Enable voltage	–1	5.5	V
V_{LATCH}	LATCH pin voltage (Version A,C)	–1	5.5	V
V_{SEL}	Select pin voltage	–1	5.5	V
V_{SNS}	Sense pin voltage	–1	5.5	V
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS482Hxx-Q1 Hotrod QFN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.8	°C/W

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{BB} = 8 V to 58 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
V_{Clamp}	VDS clamp voltage	VBB = 8V, Ids = 1A	T_J = –40°C to 150°C	55		67	V
		VBB = 48V, Ids = 1A	T_J = –40°C to 150°C	58		74	V
V_{UVLOR}	V_{BB} undervoltage lockout rising (not indicated on FLT or SNS pin)	Measured with respect to the GND pin of the device		6	6.2	6.5	V
V_{UVLOF}	V_{BB} undervoltage lockout falling (not indicated on FLT or SNS pin)			5.2	5.6	5.9	V
I_{SLEEP_VDD}	Standby current from VDD supply	VBB <= 54 V, VDD < 5.5V, V_{EN} = V_{DIAG_EN} = 0 V, V_{OUT} = 0 V	T_J = 85°C	-0.2		0.1	µA
I_{SLEEP}	Standby current (total device leakage including both MOSFET channels)	V_{BB} ≤ 54V, V_{EN} = V_{DIAG_EN} = 0V, V_{OUT} = 0V	T_J = 25°C			2	µA
			T_J = 85°C			4	µA
			T_J = 125°C			10	µA

6.5 Electrical Characteristics (continued)

V_{BB} = 8 V to 58 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{OUT(standby)}$	Output leakage current per channel	V_{BB} ≤ 54V, V_{EN} = V_{DIAG_EN} = 0V, V_{OUT} = 0V	T_J = 25°C		0.01	0.3	µA
			T_J = 85°C			0.8	µA
			T_J = 125°C			5	µA
I_{DIA}	Current consumption in diagnostic mode, channels OFF	I_{SNS} = 0 mA, VDD floating, V_{EN} = 0V, V_{DIAG_EN} = 5V, V_{OUT} = 0V			1.2	1.5	mA
		I_{SNS} = 0mA, VDD = 5V, V_{EN} = 0V, V_{DIAG_EN} = 5V, V_{OUT} = 0V			0.5	0.8	mA
$I_{Q\_1CH,DIAG}$	Quiescent current one channel enabled with external VDD	I_{SNS} = 0 mA, VOUT floating, VDD =5V, V_{EN1} = 5V, V_{DIAG_EN} = 5V			1.4	1.6	mA
	Quiescent current one channel enabled with internal VDD	I_{SNS} = 0mA, VOUT floating, VDD floating, V_{EN1} = 5V, V_{DIAG_EN} = 5V			1.4	1.8	mA
$I_{Q,DIAG}$	Quiescent current both channels enabled, diagnostic enabled	V_{EN} = V_{DIAG_EN} = 5V, I_{OUT} = 0A, VDD = 5V			1	1.3	mA
		V_{EN} = V_{DIAG_EN} = 5V, I_{OUT} = 0A, VDD not connected			1.7	2	mA
$I_{Q,\ VDD}$	VDD Quiescent current when both channels enabled, diagnostic enabled	V_{EN} = V_{DIAG_EN} = 5 V, I_{OUT} = 0 A, VDD = 5V			0.6	0.8	mA
t_{STBY}	Standby mode delay time	V_{ENx} = V_{DIAG_EN} = 0 V to standby			20	30	ms
RON CHARACTERISTICS							
R_{ON}	On-resistance per channel	8 V ≤ V_{BB} ≤ 54 V, I_{OUT}= 1 A	T_J = 25°C		85	95	mΩ
			T_J = 150°C			165	mΩ
R_{ON_par}	2-channels Paralleled On-resistance	8 V ≤ V_{BB} ≤ 54 V, I_{OUT}= 1 A	T_J = 25°C		42	47	mΩ
			T_J = 150°C			82	mΩ
R_{ON}	Reverse Polarity On-resistance	-28 V ≤ V_{BB} ≤ -8 V, I_{OUT}= 1 A, EN2 = 0V	T_J = 25°C		87		mΩ
			T_J = 150°C			174	mΩ
ΔR_{ON}	Delta On-resistance between channels	8 V ≤ V_{BB} ≤ 28 V, I_{OUT}= 1 A	T_J= -40°C to 150°C			5	%
IL_{NOM}	Continuous load current, per channel	Two channels enabled, T_A = 85°C, JEDEC 2s2p board with 4 thermal vias below VBB pad			2.2		A
		One channel enabled, T_A = 85°C, JEDEC 2s2p board with 4 thermal vias below VBB pad			3		A
V_F	Source-to-drain body diode voltage	V_{EN} = 0 V, I_{OUT} = –1 A		0.3	0.7	1	V
CURRENT SENSE CHARACTERISTICS							
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS}	I_{OUT} = 1A			2000		
I_{SNS_SAT}	Saturated sense current (Current clamp setting)			4	4.5		mA
I_{SNSI}	Current sense current	V_{EN} = V_{DIAG_EN} = 5 V	I_{OUT} = 4 A	1.93	2.03	2.13	mA
			I_{OUT} = 2 A	0.96	1.01	1.07	mA
			I_{OUT} = 1 A	0.48	0.5	0.54	mA
			I_{OUT} = 500 mA	0.24	0.252	0.266	mA
			I_{OUT} = 200 mA	0.095	0.102	0.107	mA
			I_{OUT} = 100 mA	0.047	0.051	0.054	mA
			I_{OUT} = 50 mA	0.023	0.0255	0.027	mA
			I_{OUT} = 10 mA	0.0039	0.005	0.0061	mA

6.5 Electrical Characteristics (continued)

V_{BB} = 8 V to 58 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SNS CHARACTERISTICS							
V_{SNSFH}	V_{SNS} fault high-level	V_{DIAG_EN} = 5V		4.4	4.7	5.1	V
		V_{DIAG_EN} = 3.3 V, V_{DIAG_EN} > $V_{IH,DIAG\_EN}$		3.0	3.3	3.5	V
I_{SNSFH}	I_{SNS} fault high-level	V_{DIAG_EN} > $V_{IH,DIAG\_EN}$		4.2		5.2	mA
$I_{SNSleak}$	I_{SNS} leakage with no load current	V_{DIAG_EN} = 5 V, IL = 0 mA	T_A = 25°C			1	µA
			T_A = 125°C			1.5	µA
V_{BB_ISNS}	V_{BB} headroom needed for full current sense and fault functionality	V_{DIAG_EN} = 3.3 V		6			V
		V_{DIAG_EN} = 5 V		6.5			V
CURRENT LIMIT CHARACTERISTICS							
$R_{ILIM,SHORT}$	RLIM Short Circuit Detection Range					0.3	kΩ
$R_{ILIM,OPEN}$	RLIM Open Detection Range			75			kΩ
I_{CLx}	CHx I_{CL} Current limit regulation level	Regulated current at short circuit R_L < 200 mΩ when Enabled. T_J = –40°C to 150°C	R_{ILIM} = Open	8.8	10	10.5	A
			R_{ILIM} = Short	8	9	10	A
			R_{ILIM} = 2.32 kΩ	7	8	9	A
			R_{ILIM} = 6.04 kΩ	6	7	8	A
			R_{ILIM} = 11.3 kΩ	4.9	6	7.1	A
			R_{ILIM} = 18.2 kΩ	4.2	5	5.8	A
			R_{ILIM} = 25.5 kΩ	3.3	4	4.8	A
			R_{ILIM} = 34.8 kΩ	2.4	3	3.6	A
			R_{ILIM} = 45.3 kΩ	1.6	2	2.4	A
			R_{ILIM} = 57.6 kΩ	0.75	1	1.1	A
I_{CLx_LINPK}	CHx I_{CL} current limit threshold before current limiting - overload condition. Ratio to the regulated current limit level.	dI/dt<0.01A/ms. T_J = –40°C to 150°C	all R_{ILIM}			1.25 x I_{CL}	
I_{ENPS}	Peak current enabling into permanent short. Ratio to the regulated current limit level.	Z_L = 100 mΩ + 5 µH. T_J = –40°C to 150°C	I_{ILIM} < 3A			1.8 x I_{CL}	
			I_{ILIM} >= 3A			1.6 x I_{CL}	
I_{OVCR}	OVCR Peak current threshold when short is applied while switch enabled	Z_L = 100 mΩ + 5 µH. T_J = –40°C to 150°C	all R_{ILIM}			40	A
FAULT CHARACTERISTICS							
$V_{OL,off}$	Open-load detection voltage (VDS voltage)	V_{EN} = 0 V, V_{DIAG_EN} = 5 V, measure VDS voltage		2.1	2.4	2.7	V
V_{OL_HYS}	Open-load detection voltage (VDS voltage) comparator hysteresis	V_{EN} = 0 V, V_{DIAG_EN} = 5 V			360		mV
R_{PU}	Open-load detection internal pull-up resistor per channel	V_{EN} = 0 V, V_{DIAG_EN} = 5 V		180	270	360	kΩ
t_{OL_OFF}	Open-load indication-time from EN falling	V_{EN} = 5 V to 0 V, V_{DIAG_EN} = 5 V, I_{OUT} = 0 mA, V_{OUT} = V_{BB} - V_{OL}			350		µs
t_{OL_OFF1}	Open-load detection deglitch time	V_{EN} = 0 V, V_{DIAG_EN} = 5 V, When V_{BB} – V_{OUT} < V_{OL}, duration longer than t_{OL}. Open load detected.				1.6	ms

6.5 Electrical Characteristics (continued)

V_{BB} = 8 V to 58 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{OL_OFF2}	Open-load indication-time from DIAG_EN rising	V_{EN} = 0 V, V_{DIAG_EN} = 0 V to 5 V, I_{OUT} = 0 mA, V_{OUT} = V_{BB} - V_{OL}				1.6	ms
T_{ABS}	Thermal shutdown			153	169	185	°C
T_{REL}	Relative thermal shutdown				60		°C
T_{HYS_ABS}	Thermal shutdown hysteresis				20		°C
t_{FLT}	Fault indication-time, Ver B	V_{DIAG_EN} = 5 V, Time between fault and $\overline{FLT}$ asserting				30	µs
t_{FLT_SNS}	Fault indication-time through SNS pin	V_{DIAG_EN} = 5 V, Time between fault and I_{SNS} settling at V_{SNSFH}				70	µs
t_{RETRY}	Retry time	Time from fault shutdown until switch re-enable (thermal shutdown).		1	2	3	ms
EN PIN CHARACTERISTICS							
$V_{IL,\ ENx}$	Input voltage low-level	Relative to IC GND				0.8	V
$V_{IH,\ ENx}$	Input voltage high-level	Relative to IC GND		1.5			V
$V_{IHYS,\ ENx}$	Input voltage hysteresis			150	280	400	mV
R_{ENx}	Internal pulldown resistor	V_{EN} = 0.8 V		600	1000	1400	kΩ
$I_{IL,\ ENx}$	Input current low-level	V_{EN} = 0.8 V				4	µA
$I_{IH,\ ENx}$	Input current high-level	V_{EN} = 5 V				20	µA
DIAG_EN PIN CHARACTERISTICS							
$V_{IL,\ DIAG\_EN}$	Input voltage low-level					0.8	V
$V_{IH,\ DIAG\_EN}$	Input voltage high-level			1.5			V
$V_{IHYS,\ DIAG\_EN}$	Input voltage hysteresis			150	280	400	mV
R_{DIAG_EN}	Internal pulldown resistor	V_{DIAG_EN} = 0.8 V		600	1000	1400	kΩ
$I_{IL\_DIAG\_EN}$	Input current low-level	V_{DIAG_EN} = -1 V		–10		0	µA
$I_{IL,\ DIAG\_EN}$	Input current low-level	V_{DIAG_EN} = 0.8 V				4	µA
$I_{IH,\ DIAG\_EN}$	Input current high-level	V_{DIAG_EN} = 5 V				20	µA
SEL PIN CHARACTERISTICS							
$V_{IL,\ SEL}$	Input voltage low-level					0.8	V
$V_{IH,\ SEL}$	Input voltage high-level			1.5			V
$V_{IHYS,\ SEL}$	Input voltage hysteresis			150	280	400	mV
R_{SEL}	Internal pulldown resistor	V_{SEL} = 0.8 V	V_{DIAG_EN} = 0.8 V	600	1000	1400	kΩ
$I_{IL,\ SEL}$	Input current low-level	V_{SEL} = 0.8 V	V_{DIAG_EN} = 0.8 V			1.1	µA
$I_{IH,\ SEL}$	Input current high-level	V_{SEL} = 5V	V_{DIAG_EN} = 5 V			7	µA
LATCH PIN CHARACTERISTICS							
$V_{IH,\ LATCH}$	Input voltage high-level			1.5			V
$V_{IL,\ LATCH}$	Input voltage low-level					0.8	V
$I_{IL,LATCH}$	Input current low-level	V_{LATCH} = 0.8 V	V_{DIAG_EN} = 0.8 V			2	µA
$I_{IH,LATCH}$	Input current high-level	V_{LATCH} = 5V	V_{DIAG_EN} = 5 V			12	µA
$V_{IHYS,LATCH}$	Input voltage hysteresis			150	280	400	mV
R_{LATCH}	Internal pulldown resistor	V_{LATCH} = 0.8 V	V_{DIAG_EN} = 0.8 V	400	500	600	kΩ

6.6 SNS Timing Characteristics

V_{BB} = 6 V to 18 V, T_J = –40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIAG_EN (50% of V_{DIAG_EN} to 90% of settled ISNS)	V_{ENx}= 5 V, V_{DIAG_EN} = 0 V to 5 V, R_{SNS} = 1 kΩ, I_L = 0.32A			20	µs
		V_{EN} = 5 V, V_{DIAG_EN} = 0 V to 5 V, R_{SNS} = 1 kΩ, I_L = 16mA			6	µs
$t_{SNSION2}$	Settling time from rising edge of EN and DIAG_EN (50% of V_{DIAG_EN} V_{EN} to 90% of settled ISNS)	V_{EN} = V_{DIAG_EN} = 0 V to 5 V, VBB = 48 V, R_{SNS} = 1 kΩ, I_L = 0.32A			160	µs
$t_{SNSION3}$	Settling time from rising edge of EN with DIAG_EN HI (50% of V_{DIAG_EN} V_{EN} to 90% of settled ISNS)	V_{EN} = 0 V to 5 V, V_{DIAG_EN} = 5 V, VBB = 48 V, R_{SNS} = 1 kΩ, I_L = 0.32A			160	µs
$t_{SNSIOFF}$	Settling time from falling edge of DIAG_EN (50% of V_{DIAG_EN} to 5% of settled ISNS)	V_{EN} = 5 V, V_{DIAG_EN} = 5 V to 0 V, VBB = 48 V, R_{SNS} = 1 kΩ, I_L = 0.32A			17	µs
$t_{SETTLEH}$	Settling time from rising edge of load step	V_{EN} = 5 V, V_{DIAG_EN} = 5 V, R_{SNS} = 1 kΩ, I_L = 16mA to 0.32A			3	µs
$t_{SETTLEL}$	Settling time from falling edge of load step	V_{EN} = 5 V, V_{DIAG_EN} = 5 V, R_{SNS} = 1 kΩ, I_L = 0.32A to 16mA			4	µs
t_{MUX}	Settling time from switching from CHx to CHy	V_{EN} = 5 V, V_{DIAG_EN} = 5 V, R_{SNS} = 1 kΩ, SEL = 0 V to 5 V, CH1 = 0.48A, CH2 = 3.2A			20	µs
t_{MUX}	Settling time from switching from CH2 to CH1	V_{EN1} = 5 V, V_{EN2} = 0 V, V_{DIAG_EN} = 5 V, R_{SNS} = 1 kΩ, SEL = 5 V to 0 V, CH1 = 0.48A, CH2 = Open			38	µs
t_{MUX}	Settling time from switching from CH1 to CH2	V_{EN1} = 5 V, V_{EN2} = 0 V, V_{DIAG_EN} = 5 V, R_{SNS} = 1 kΩ, SEL = 0 V to 5 V, CH1 = 0.48A, CH2 = Open			825	µs

6.7 Switching Characteristics_24V

V_{BB} = 24V, T_J = –40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Channel Turn-on delay time (from Standby)	R_L = 20 Ω (50% of EN to 20% of VOUT)			100	µs
t_{DR}	Channel Turn-on delay time (from Active)	R_L = 20 Ω (50% of EN to 20% of VOUT)			50	µs
t_{DF}	Channel Turn-off delay time	R_L = 20 Ω (50% of EN to 80% of VOUT)			50	µs
SR_R	VOUT rising slew rate	20% to 80% of V_{OUT}, R_L = 20 Ω	0.2		0.7	V/µs
SR_F	VOUT falling slew rate	80% to 20% of V_{OUT}, R_L = 20 Ω	0.25		0.7	V/µs
f_{PWM}	PWM frequency				1	kHz
t_{ON}	Channel Turn-on time	R_L = 20 Ω (50% of EN to 80% of VOUT)			140	µs
t_{OFF}	Channel Turn-off time	R_L = 20 Ω (50% of EN to 20% of VOUT)			86	µs
$t_{ON} – t_{OFF}$	Turn-on and off matching	1-ms enable pulse in Active state, R_L = 20 Ω, DIAG_EN high	–15		20	µs
		200-µs enable pulse in Active state, R_L = 20 Ω, DIAG_EN high	–30		30	µs
E_{ON}	Switching energy losses during turn-on	R_L = 50 Ω			0.15	mJ

6.7 Switching Characteristics_24V (continued)

V_{BB} = 24V, T_J = –40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_{OFF}	Switching energy losses during turn-off	R_L = 50 Ω			0.15	mJ

6.8 Switching Characteristics_48V

V_{BB} = 48V, T_J = –40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Channel Turn-on delay time (from Standby)	R_L = 20 Ω (50% of EN to 20% of VOUT)			105	µs
t_{DR}	Channel Turn-on delay time (from Active)	R_L = 20 Ω (50% of EN to 20% of VOUT)			56	µs
t_{DF}	Channel Turn-off delay time	R_L = 20 Ω (50% of EN to 80% of VOUT)			65	µs
SR_R	VOUT rising slew rate	20% to 80% of V_{OUT}, R_L = 20 Ω	0.3		0.85	V/µs
SR_F	VOUT falling slew rate	80% to 20% of V_{OUT}, R_L = 20 Ω	0.34		0.9	V/µs
f_{PWM}	PWM frequency				1	kHz
t_{ON}	Channel Turn-on time	R_L = 20 Ω (50% of EN to 80% of VOUT)			180	µs
t_{OFF}	Channel Turn-off time	R_L = 20 Ω (50% of EN to 20% of VOUT)			140	µs
$t_{ON} – t_{OFF}$	Turn-on and off matching	1-ms enable pulse in Active state, R_L = 20 Ω, DIAG_EN high	–30		30	µs
		200-µs enable pulse in Active state, R_L = 20 Ω, DIAG_EN high	–30		30	µs
Δ_{PWM}	PWM accuracy - average load current	400-µs enable pulse (2-ms period) in Active state, R_L = 20 Ω	–15		15	%
		≤500 Hz in Active state, 50% Duty cycle, R_L = 20 Ω	–10		10	%
E_{ON}	Switching energy losses during turn-on	R_L = 50 Ω			1	mJ
E_{OFF}	Switching energy losses during turn-off	R_L = 50 Ω			0.9	mJ

6.9 Typical Characteristics

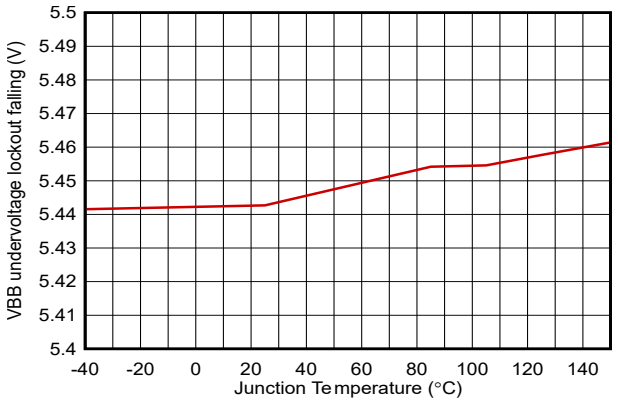


Figure 6-1. VBB Undervoltage Lockout Falling

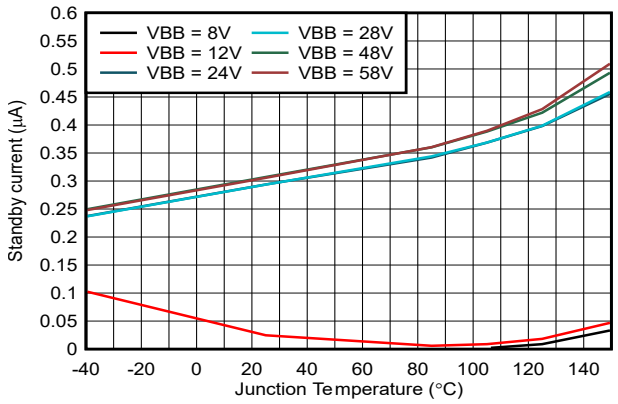


Figure 6-2. Standby Current

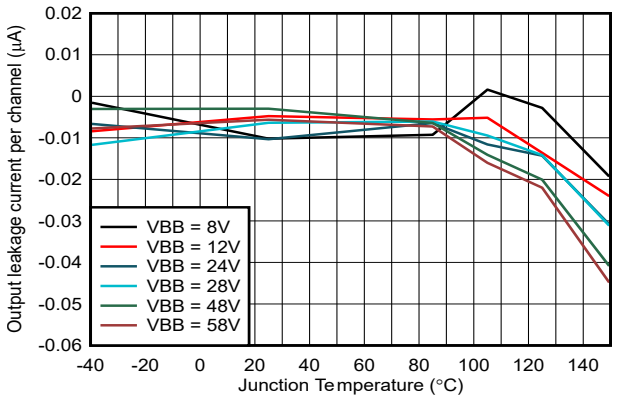


Figure 6-3. Output Leakage Current Per Channel

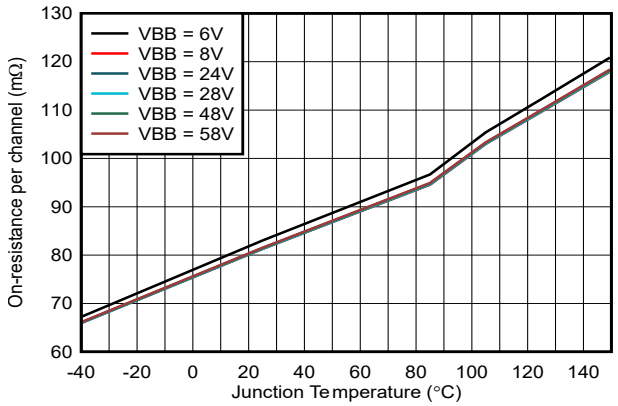


Figure 6-4. On-Resistance Per Channel

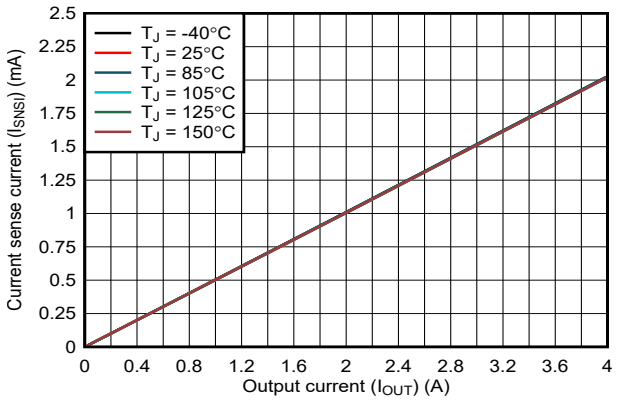


Figure 6-5. Current Sense Signal, VBB = 8V

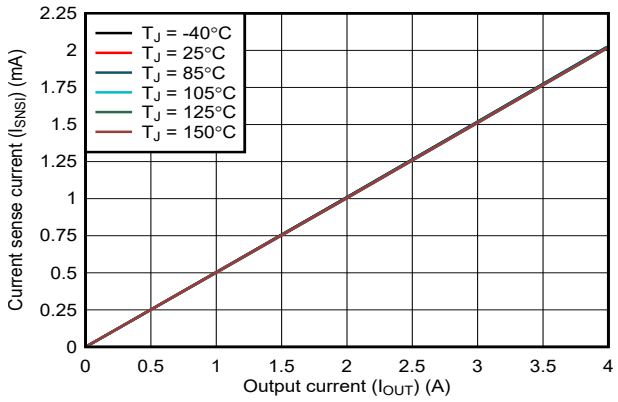


Figure 6-6. Current Sense Signal, VBB = 24V

6.9 Typical Characteristics (continued)

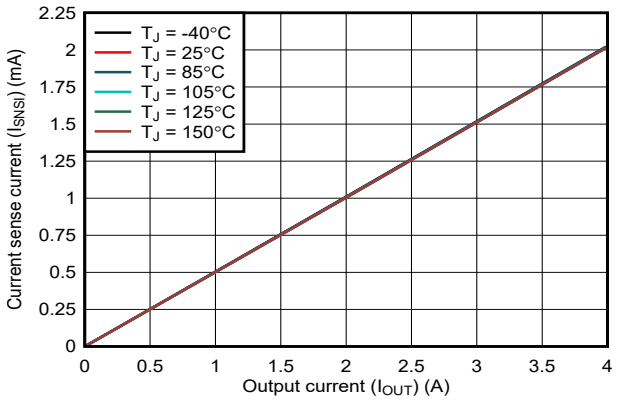


Figure 6-7. Current Sense Signal, VBB = 48V

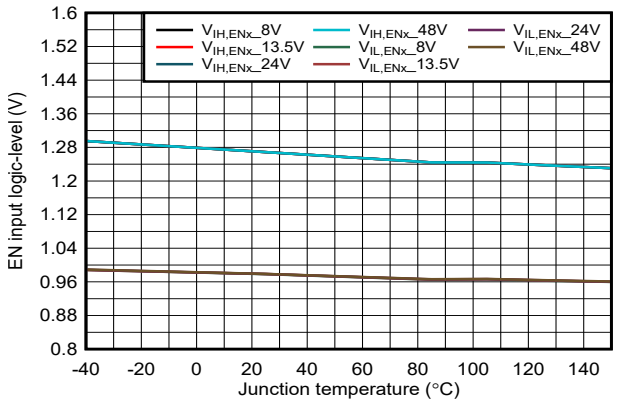


Figure 6-8. Input Voltage Low-Level and High-Level for EN Pins

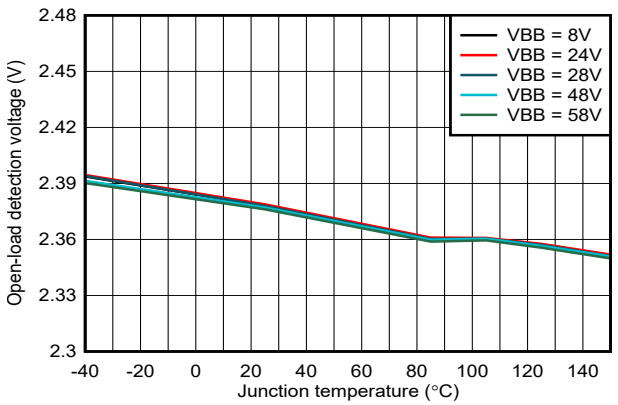


Figure 6-9. Open-Load Detection Voltage

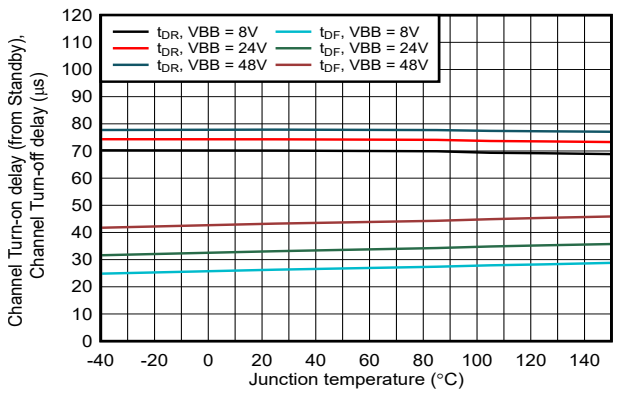


Figure 6-10. Channel Turn-On (t_{DR}) and Turn-Off (t_{DF}) Delay Time

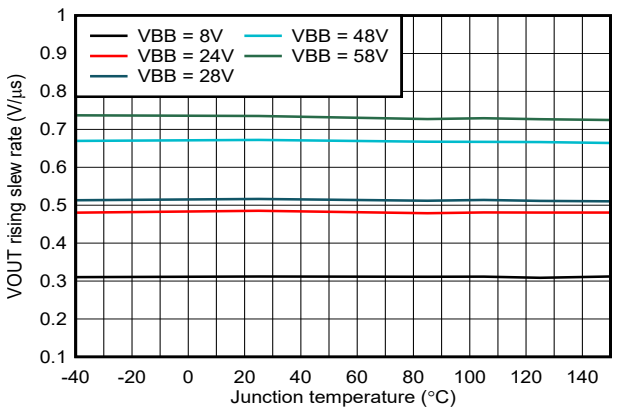


Figure 6-11. VOUT Rising Slew Rate

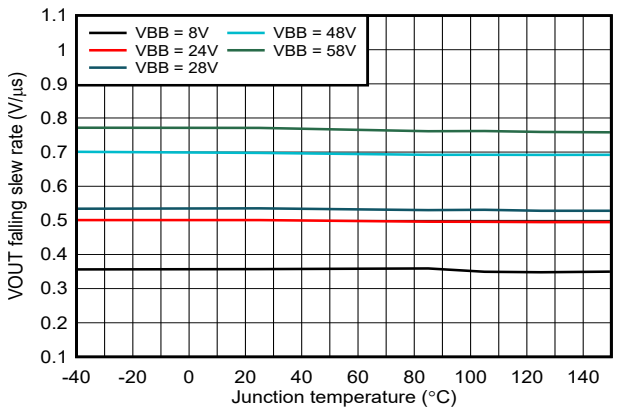


Figure 6-12. VOUT Falling Slew Rate

6.9 Typical Characteristics (continued)

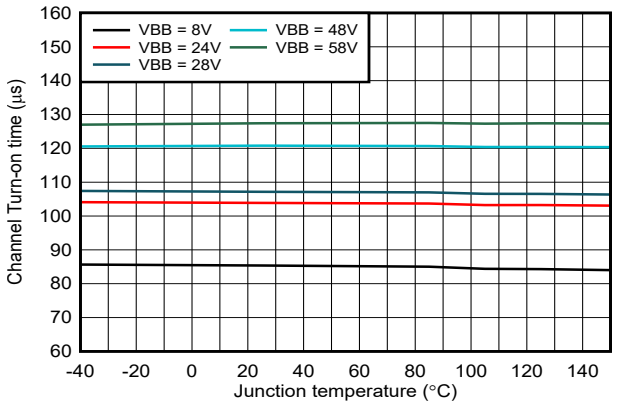


Figure 6-13. Channel Turn-On Time

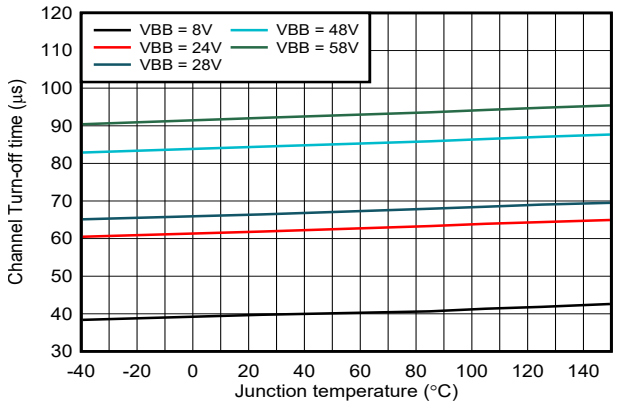


Figure 6-14. Channel Turn-Off Time

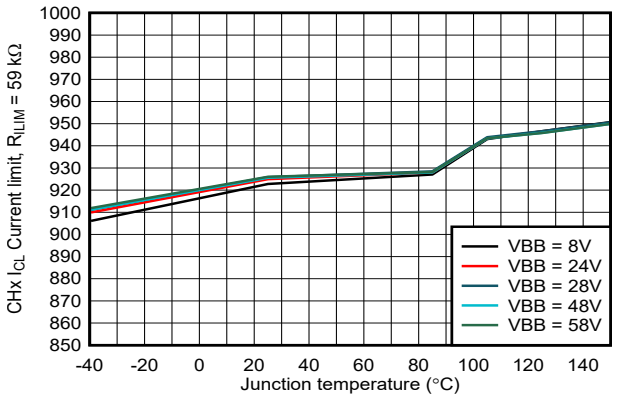


Figure 6-15. Current Limit Regulation Level: 1A

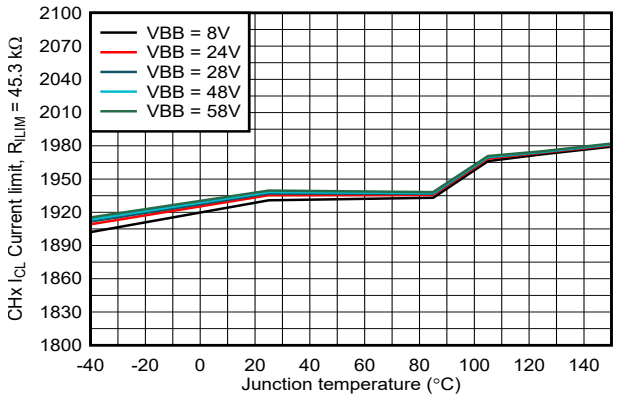


Figure 6-16. Current Limit Regulation Level: 2A

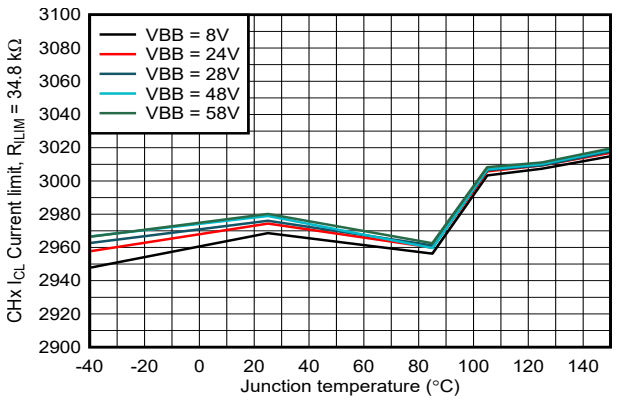


Figure 6-17. Current Limit Regulation Level: 3A

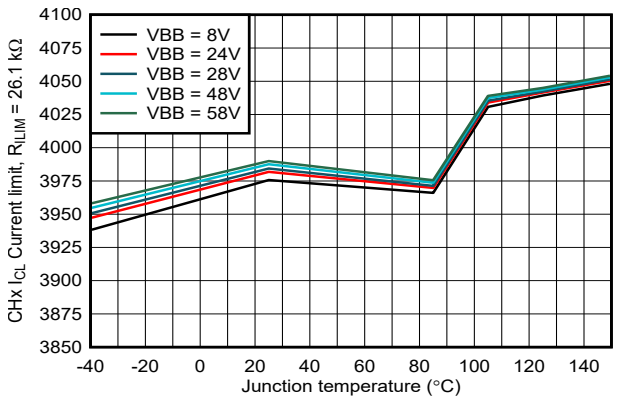


Figure 6-18. Current Limit Regulation Level: 4A

6.9 Typical Characteristics (continued)

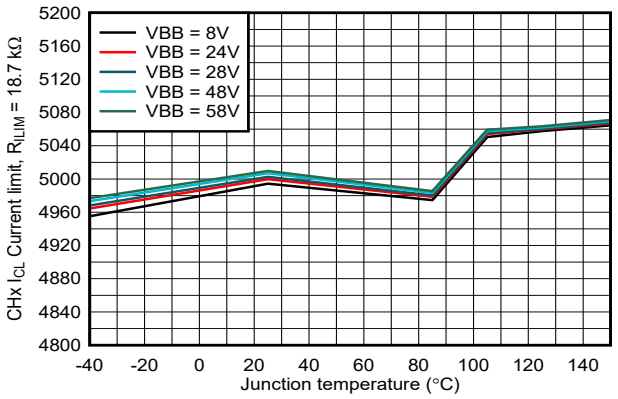


Figure 6-19. Current Limit Regulation Level: 5A

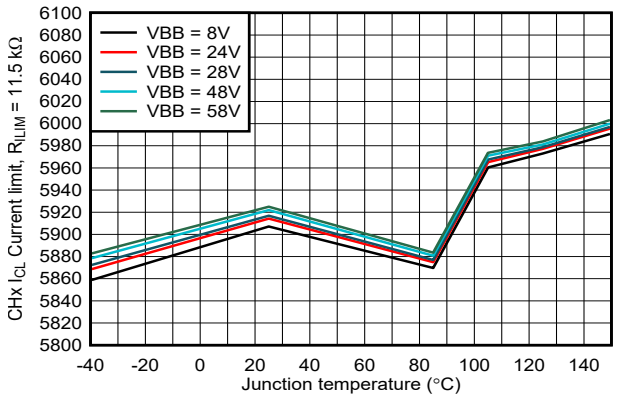


Figure 6-20. Current Limit Regulation Level: 6A

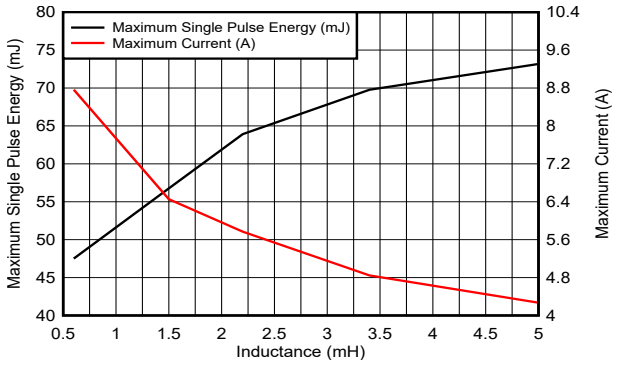


Figure 6-21. Single Pulse Energy, VBB = 32V, T_{J_start} = 125°C

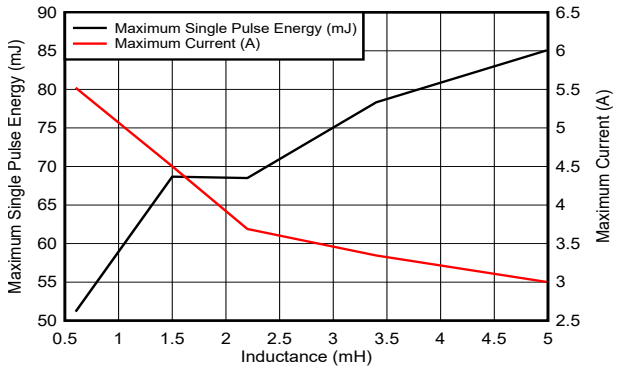


Figure 6-22. Single Pulse Energy, VBB = 54V, T_{J_start} = 125°C

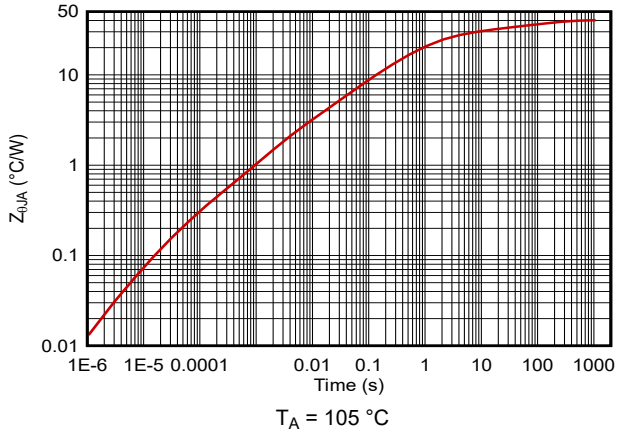


Figure 6-23. $Z_{\Theta JA}$ (transient thermal impedance) with JEDEC standard 2s2p PCB layout, 4 Vias below VBB Pad

7 Detailed Description

7.1 Overview

The TPS482H85-Q1 device is a smart high-side switch, with internal charge pump and dual-channel integrated NMOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of whole system.

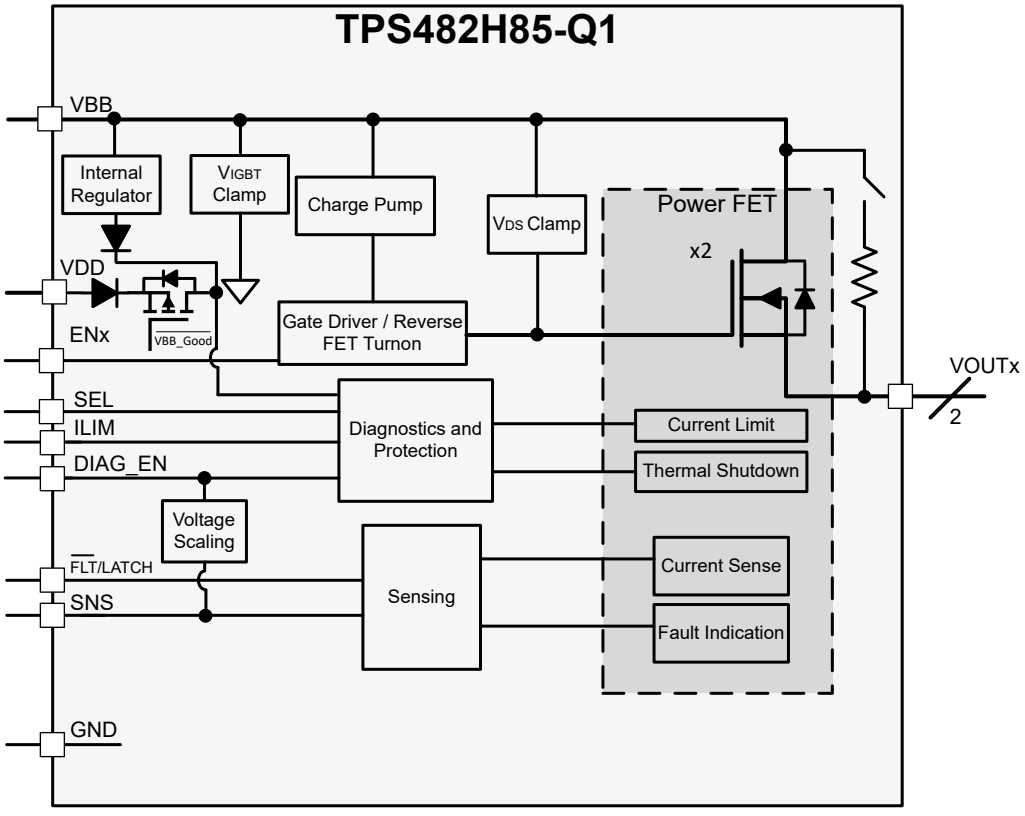
The device has logic pins to enable each of the two channels and a separate pin to enable the diagnostic output with SEL pin to select the channel to be output on the analog current SNS pin. A and C versions provide a LATCH pin to select between latch and auto-retry behavior after thermal shutdown, while B version provides a global $\overline{\text{FLT}}$ pin to indicate a fault in the device.

The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

For inductive loads (relays, solenoids, valves), the device implements an active clamp between drain and source to protect itself. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power and EMI to a minimum.

The TPS482H85-Q1 device is able to drive a wide variety of resistive, inductive, and capacitive loads, including low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pin Current and Voltage Conventions

For reference purposes throughout the data sheet, current directions on their respective pins are as shown by the arrows in Figure 7-1. The direction is used to indicate the polarities of current in Specifications, but not to represent the actual current flow direction of each pin. All voltages are measured relative to the ground plane.

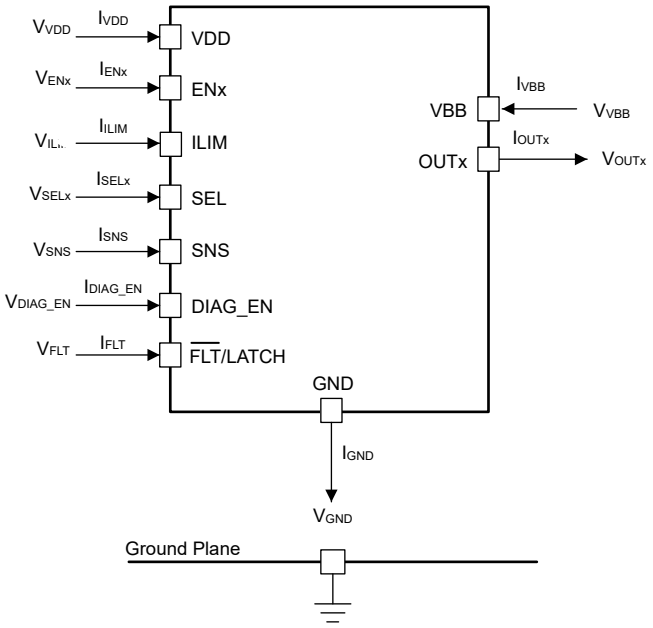


Figure 7-1. Voltage and Current Conventions

7.3.2 Accurate Current Sense

The high-accuracy current-sense function is internally implemented, which allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, flowing out to the external resistor between the SNS pin and GND, and reflected as voltage on the SNS pin.

K_{SNS} is the ratio of the output current and the sense current. The accuracy values of K_{SNS} quoted in the electrical characteristics do take into consideration temperature and supply voltage. Each device was internally calibrated while in production, so post-calibration by users is not required in most cases.

The maximum voltage out on the SNS pin is clamped to V_{SNSFH}, which is the fault voltage level. This voltage is made a function of the DIAG_EN voltage to ensure that it is not higher than what the system can tolerate. If DIAG_EN is between V_{IH} and 3.3V, the maximum output on the SNS pin is approximately 3.3V. However, if the voltage at DIAG_EN is above 3.3V, then the fault SNS voltage, V_{SNSFH}, tracks that voltage up to 5V. Tracking is done because the GPIO voltage output that is powering the diagnostics through DIAG_EN is close to the maximum acceptable ADC voltage within the same microcontroller.

Therefore, choose the sense resistor value, R_{SNS}, to maximize the range of currents needed to be measured by the system. The maximum usable R_{SNS} value is bounded by the ADC minimum acceptable voltage, $V_{ADC,min}$, for the smallest load current needed to be measured by the system, $I_{LOAD,min}$. Choose the minimum acceptable R_{SNS} value so that the V_{SNS} voltage is less than the V_{SNSFH} value, allowing for the system to correctly determine faults.

The clamp on the SNS pin is enabled when DIAG_EN in low as well. So, if the application has tied SNS pins of multiple devices together, external multiplexers can be used to read individual SNS pin voltages. The multiplexers can be controlled by the DIAG_EN signal of individual devices.

In case a GND network is used for reverse polarity protection, the voltage drop across the GND network has to be taken into account to ensure that the SNS pin voltage does not exceed the maximum acceptable ADC voltage. For example, if the microcontroller is running at 3.3V and a GND network is used, the effective DIAG_EN voltage seen by the device will be lowered by the amount of offset induced by the GND network, typically about 0.7V. As a result, the SNS pin will clamp to about 3.3V plus the GND offset. External clamp diodes can be used to restrict the SNS pin voltage in such cases.

The difference between the maximum readable current through the SNS pin, $I_{LOAD,max} \times R_{SNS} / K_{SNS}$, and the V_{SNSFH} is called the headroom voltage, V_{HR}. The headroom voltage is determined by the system, the supply voltage and whether a ground network is used. The current sensing output voltage limitation due to V_{HR} starts at VBB ~ 2.6V + V_{SNS} when a GND network is used. In the case of a fault level, the voltage drop is smaller (~1.5V), because when there is a fault, the internal SENSE FET is byapssed, which leads to lower headroom requirement. Without a ground network, the SNS pin voltage limitation due to V_{HR} starts at a lower VBB (by about 0.7V).

It is important to maintain a headroom so that there is a difference between the maximum readable current and a fault condition. Therefore, the minimum R_{SNS} value has to be the V_{SNSFH} minus the V_{HR} times the sense current ratio, K_{SNS} divided by the maximum load current the system must measure, $I_{LOAD,max}$. Use the following equation to set the boundary equation -

$$V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \leq R_{SNS} \leq (V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \quad (1)$$

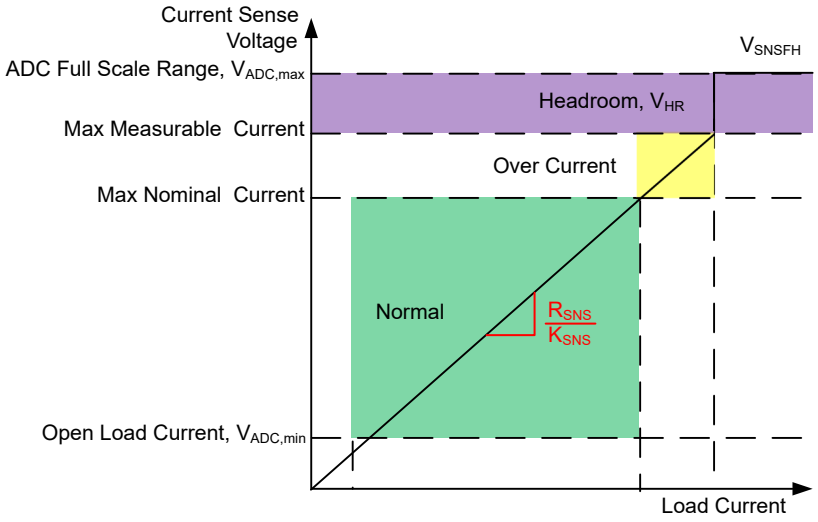


Figure 7-2. Voltage Indication on the Current-Sense Pin

The maximum current the system wants to read, $I_{LOAD,max}$, must be below the current-limit threshold because after the current-limit threshold is tripped the V_{SNS} value goes to V_{SNSFH}.

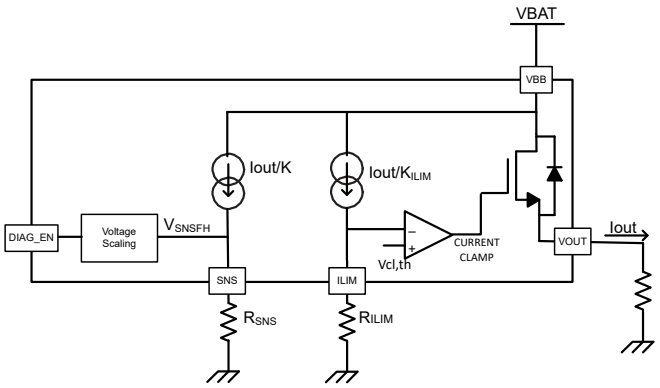


Figure 7-3. Current-Sense and Current-Limit Block Diagram

Because this scheme adapts based on the voltage coming in from the MCU, there is no need to have a Zener diode on the SNS pin to protect from high voltages.

7.3.3 Adjustable Current Limit

A high-accuracy adjustable current limit allows higher reliability, which protects the power supply and wires during short circuit or power up by being programed to an acceptable level. Also, current limiting can save system costs by reducing PCB traces, connector size, capacity of the preceding power stage and reducing wire gauge.

Current limit offers protection from over-stressing to the load and integrated power FET. the current limit regulates the output current to the set value, asserts the $\overline{FLT}$ pin, and pulls up the SNS pin to V_{SNSFH} if the device is set up to output that channel on the SNS pin.

- The device can be programmed to different current limit values through an external resistor on the ILIM pin. There are 10 current limit settings which can be set based on resistors values in Current Limit Setting Through External Resistor. ≤±1% tolerance resistors should be used for R_{ILIM} resistor.

Table 7-1. Current Limit Setting Through External Resistor

ALLOWED RESISTOR VALUE (1)	ILIM THRESHOLD
59 kΩ	1A
45.3 kΩ	2A
34.8 kΩ	3A
26.1 kΩ	4A
18.7 kΩ	5A
11.5 kΩ	6A
6.65 kΩ	7A
2.74 kΩ	8A
Short to GND (<1.1 kΩ)	9A
Open (> 60 kΩ)	10A

(1) Any resistor settings that are not listed in this table can be interpreted as one of the adjacent levels, which is not a recommended configuration.

To set a different inrush current limit and steady state current limit, change the current limit resistor dynamically when the device is ON. Adopt a MOSFET based control scheme for changing the current limit on the fly. However, carefully consider the components and the layout at ILIM pin to minimize the capacitance at the pin.

If switching the ILIM threshold on-the-fly, any capacitance ≥ 100pF at ILIM pin might affect the transition speed from one ILIM resistor to another, which can lead to unwanted shutdown. Select a MOSFET with low input capacitance for dynamic current limit change.

A current limit event occurs when I_{OUTx} reaches the regulation threshold level, I_{CL}. When I_{OUT} reaches the current limit threshold, I_{CL}, the device can remain enabled and limit I_{OUTx} to I_{CL}. When the device remains enabled (and limits I_{OUT}), thermal shutdown may be triggered due to the high amount of power dissipation in the FET. The regulation loop response when the device is enabled into a short circuit is shown in Enable Into Short Current Limit (auto-retry). The figure is showing the scenario with the auto-retry versions or LATCH pin version with LATCH = LOW listed in Device Comparison Table. The LATCH pin version with LATCH = HIGH will latch off after the first thermal shutdown. Please note that the current may peak at a higher value (I_{CL_ENPS}) than the regulation threshold (I_{CL}).

When an over-current event occurs, the current limit must respond quickly in order to limit the peak current seen on short circuits (both hot and enabling into a short). The peak has to be limited to ensure that the supply does not droop for a given amount of supply capacitance. This is especially important in applications where the device is powered from a DC/DC instead of car battery.

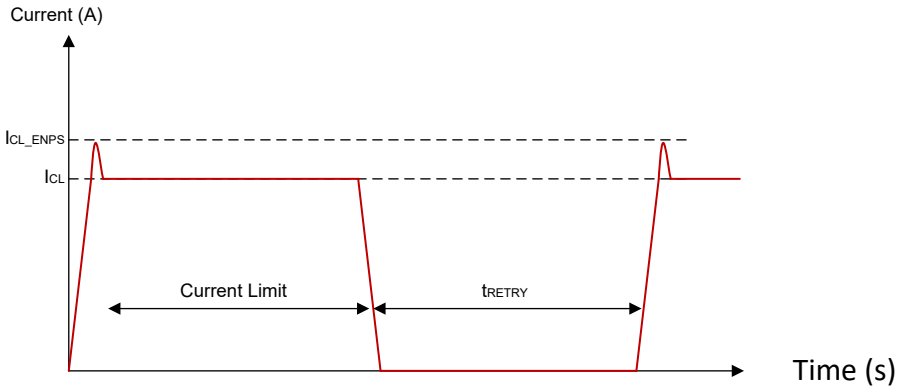


Figure 7-4. Enable Into Short Current Limit (auto-retry)

However, a higher (I_{CL_LINPK}) output current than the current limit regulation loop threshold (I_{CL}) may be available from the switch during an overload condition before the current limitation is applied.

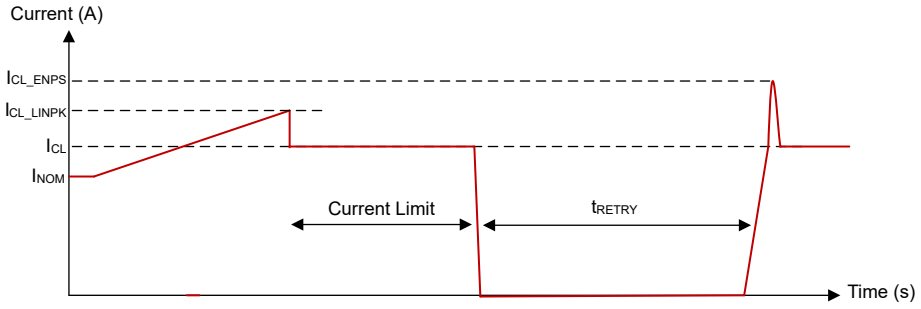


Figure 7-5. Linear Peak From Soft Short (auto-retry)

The device applies a strong pulldown to limit the current during the short circuit event while the switch is enabled. The current will then drop down to zero before the current limit regulation loop engages and the switch turn-on and the behavior will be similar to the enable into a short circuit case.

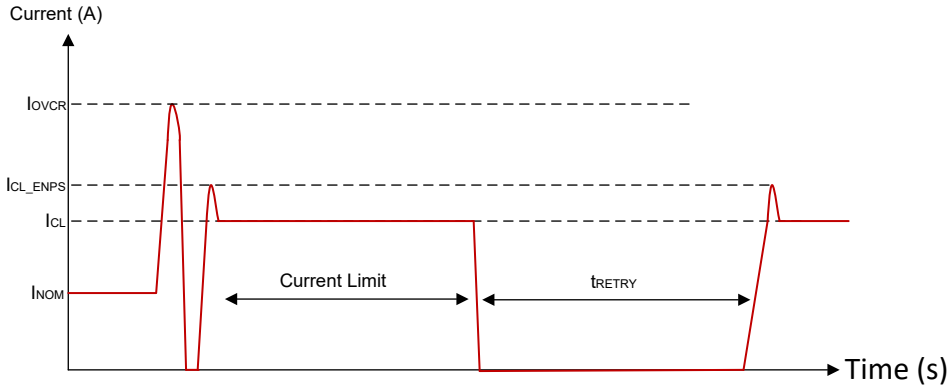


Figure 7-6. Hot Short Event (auto-retry)

7.3.4 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

$$V_{DS(clamp)} = V_{VS} - V_{OUT} \quad (2)$$

During the period of demagnetization (t_{decay}), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ($E_{(VS)}$) and the energy of the load ($E_{(load)}$). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \quad (3)$$

When an inductive load switches off, $E_{(HSS)}$ causes high thermal stressing on the device. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

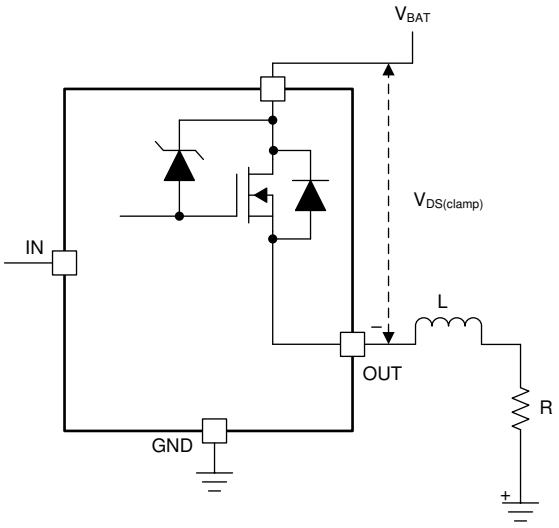


Figure 7-7. Drain-to-Source Clamping Structure

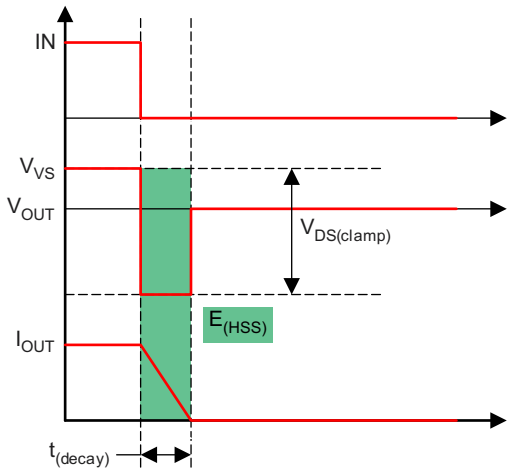


Figure 7-8. Inductive Load Switching-Off Diagram

From the perspective of the high-side switch, $E_{(HSS)}$ equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_0^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t)dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)$$

$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(max)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \quad (4)$$

When R approximately equals 0, $E_{(HSD)}$ can be given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I_{OUT(max)}^2 \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|} \quad (5)$$

The device optimizes the switching-off slew rate when the clamp is active. This optimization can help the system design by keeping the effects of transient power and EMI to a minimum. The controlled slew rate is around 0.7V/µs.

The recommendation for PWM-controlled inductive loads is to add the external freewheeling circuitry shown in Figure 7-9 to protect the device from repetitive power stressing. The TVS is used to achieve the fast decay. See Figure 7-9 for more details.

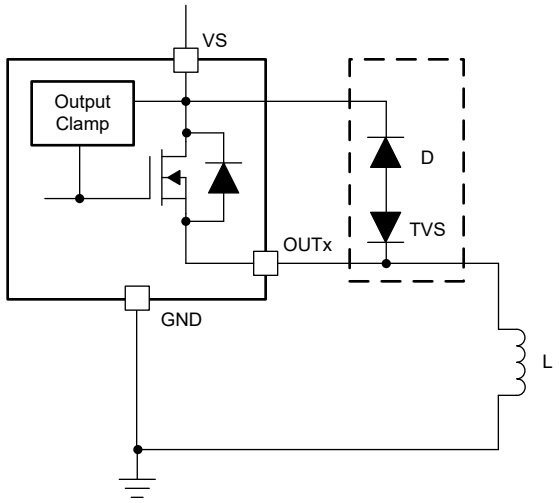


Figure 7-9. Protection With External Circuitry

7.3.5 Fault Detection and Reporting

7.3.5.1 Diagnostic Enable Function

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and ENx low.

7.3.5.2 Multiplexing of Current Sense

SEL pin is used to multiplex the shared current-sense function among the two channels within the same device. Pulling each pin high or low sets the corresponding channel to be output on the SNS pin if DIAG_EN is high. $\overline{\text{FLT}}$ pin in B variant represents a global interrupt that goes low if a fault occurs on any channel, except for open load and short-to-battery faults. For open load and short-to-battery faults, $\overline{\text{FLT}}$ goes low only if the selected channel has the fault.

If current sense information is multiplexed across different devices, do not directly tie the SNS pins together across multiple devices. When the DIAG_EN is LOW, there is an internal clamp at SNS pin that clamps the voltage to approximately 2V. One device SNS pin is able to affect the SNS readback of other devices if tied directly.

To use the SNS pin across multiple devices, connect individual SNS pin to different analog input pins of MCU; see Figure 7-10. Alternatively, use an external analog MUX to connect to a single MCU pin; see Figure 7-11.

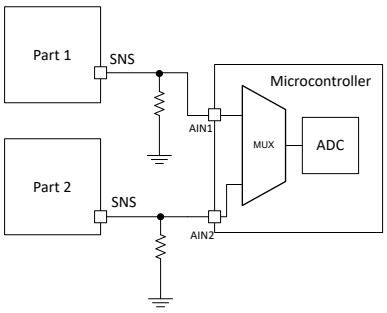


Figure 7-10. SNS Sharing Across Multiple Devices Method 1

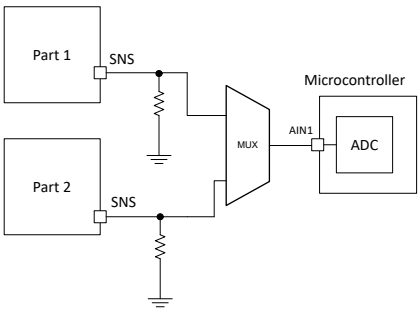


Figure 7-11. SNS Sharing Across Multiple Devices Method 2

Table 7-2. Diagnosis Configuration Table

DIAG_EN	ENx	SEL	SNS ACTIVATED CHANNEL	SNS	$\overline{FLT}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	0V. Clamp to 2V internally if external voltage is applied to the pin.	See Fault Table	SNS disabled, $\overline{FLT}$ reporting, full protection
	L				High-Z	Diagnostics disabled, no protection
H	—	0	Channel 1	Fault Table	See Fault Table	See Fault Table
		1	Channel 2			

7.3.5.3 $\overline{FLT}$ Reporting

For the B variant with the global $\overline{FLT}$ pin, the $\overline{FLT}$ output monitors the fault condition for both the channels. When a fault condition (except open load and short-to-battery faults) occurs on any channel, the $\overline{FLT}$ pin is pulled down to GND. A 3.3V or 5V external pullup is required to match the supply level of the microcontroller. The $\overline{FLT}$ pin reports faults on any channel as long as the device is not in the SLEEP mode. For open load and short-to-battery faults, $\overline{FLT}$ goes low only if the selected channel has the fault.

After the $\overline{FLT}$ report, the microcontroller can check and identify the channel in fault status by multiplexed current sensing. Alternately for the A and C variants, the SNS pin also works as a fault report with an internal pullup voltage, V_{SNSFH} if DIAG_EN is high.

7.3.5.4 Fault Table

Table 7-3. Fault Table

CONDITIONS	ENx	OUTx	SNS (If DIAG_EN is high)	$\overline{FLT}$ (1) (with external pull-up)	BEHAVIOR	FAULT RECOVERY
Normal	L	L	0	H	Normal	—
	H	V_{BB} - I_{LOAD} × R_{ON}	I_{LOAD} / K_{SNS}	H	Normal	—
Overcurrent	H	V_{BB} - I_{LIM} × R_{ON}	V_{SNSFH}	L	Holds the current at the current limit until thermal shutdown or when the overcurrent event is removed.	Auto
Open load, reverse polarity	L	H	V_{SNSFH}	L	Internal pull-up resistor is active. Fault is asserted when $V_{VS} - V_{OUTx} < V_{(ol,off)}$	Auto
	H	H	I_{LOAD} / K_{SNS}	H	Normal behavior. User can make judgement based on SNS pin output.	—
Hot short	H	L	V_{SNSFH}	L	Device will immediately shutdown, and re-enable into current limit.	Auto-retry into current limit until thermal shutdown. Auto-retry version will repeat until the fault goes away. Latch version will need toggle EN after first thermal shutdown.
Enable into permanent short	L → H	L	V_{SNSFH}	L	Device will enable into current limit until thermal shutdown.	Enable into current limit until thermal shutdown. Auto-retry version will repeat until the fault goes away. Latch version will need toggle EN after first thermal shutdown.

Table 7-3. Fault Table (continued)

CONDITIONS	ENx	OUTx	SNS (If DIAG_EN is high)	$\overline{FLT}$ (1) (with external pull-up)	BEHAVIOR	FAULT RECOVERY
Absolute thermal shutdown, Relative thermal shutdown	H	L	V_{SNSFH}	L	Shuts down when devices hits relative or absolute thermal shutdown.	For auto-retry version, output auto-retry after t_{RETRY}. Fault recovers when $T_J < T_{HYS}$ or when ENx toggles. Latch version can recover only when EN toggles.
Reverse polarity	X	X	X		X	Channel turns on to lower power dissipation. Limit current into ground pin by external ground network.

(1) $\overline{FLT}$ output only on the variants that include $\overline{FLT}$ pin.

7.3.6 Full Diagnostics

7.3.6.1 Short-to-GND and Overload Detection

When a channel is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device will clamp the current to I_{CL} until thermal shutdown. The device automatically recovers when the fault condition is removed.

In a hot short condition, when the short-circuit is applied when the EN is HIGH, the device will shutdown immediately and auto-retry the same as enable into permanent short condition, as shown in Figure 7-6.

7.3.6.2 Open-Load Detection

7.3.6.2.1 Channel On

When a channel is ON, benefiting from the high-accuracy current sense in the small current range, an open-load event can be detected as an ultra low V_{SNS} and handled by the microcontroller. Note that the detection is not reported on the $\overline{FLT}$ pin or the fault registers. The microcontroller must multiplex the SEL pin to output the correct channel out on the SNS pin.

7.3.6.2.2 Channel Off

In the OFF state, when DIAG_EN is high, there is an internal pull-up resistor R_{PU} that pulls up a channel to V_{BB}. The specific channel that gets pulled up is based on the selection of SEL, and the other channels do not have the pull-up resistor engaged.

If there is load present at the selected channel, then the output voltage is pulled to around 0V, as the load is much stronger than the R_{PU}. In the case of an open load, the output voltage will be pulled close to the supply voltage by the R_{PU}. If $V_{BB} - V_{OUT} < V_{OL,off}$ for the selected channel, the $\overline{FLT}$ pin goes low to indicate the fault to the MCU, and the SNS pin is pulled up to I_{SNSFH}.

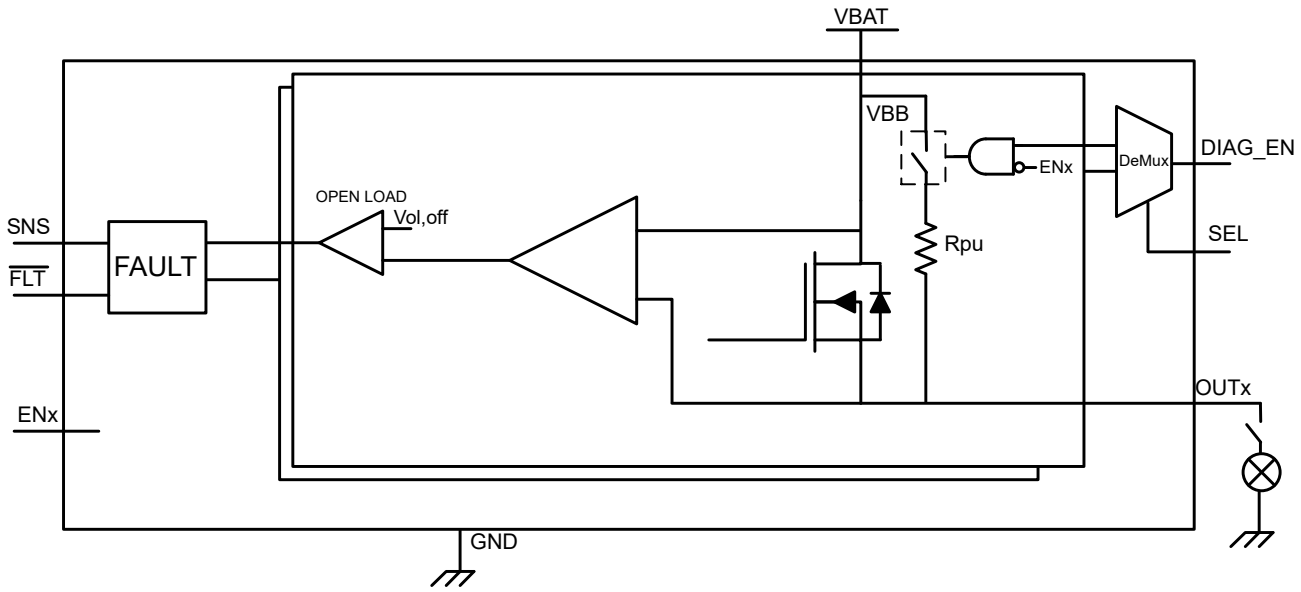


Figure 7-12. Open-Load Detection in Off-State

7.3.6.3 Short-to-Battery Detection

Short-to-battery has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See Fault Table for more details.

7.3.6.4 Reverse-Polarity and Battery Protection

Reverse-polarity, commonly referred to as reverse battery, occurs when the ground of the device goes to the battery potential, V_{GND} = V_{BAT}, and the supply pin goes to ground, V_{BB} = 0V. In this case, if the EN1 pin has a path to the *ground* plane, then the FET turns on to lower the power dissipation through the main channel and prevent current flow through the body diode. The resistor/diode ground network (if there is not a central blocking diode on the supply) is required for the device to protect itself during a reverse battery event.

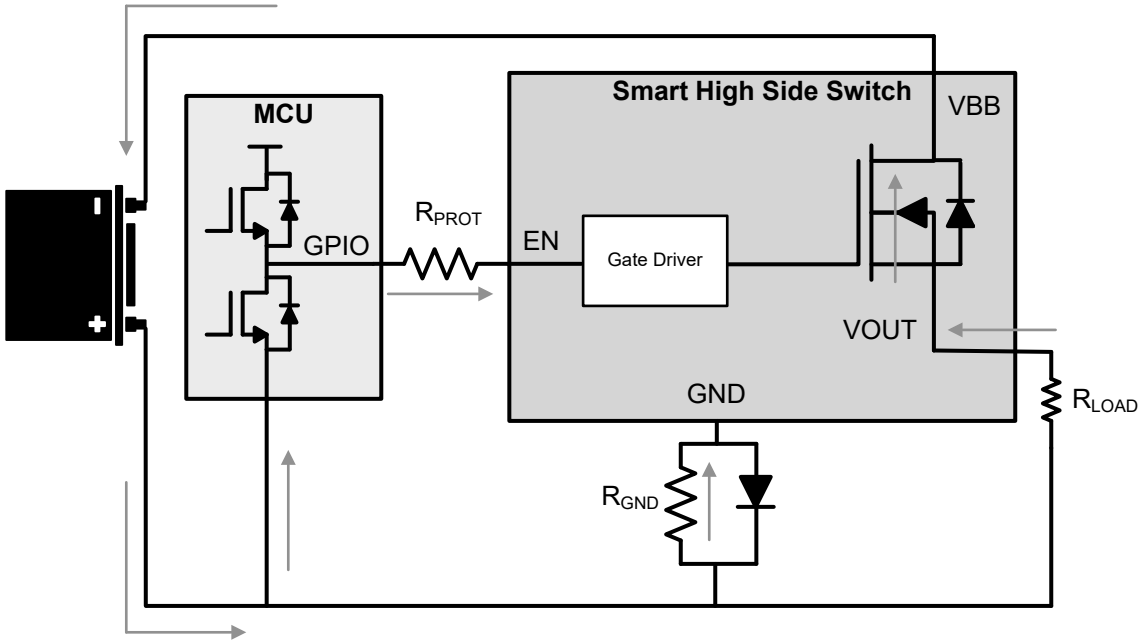


Figure 7-13. Reverse Battery Circuit

For more external protection circuitry information, see Section 7.3.7.5. See the fault truth table in Fault Table for more details.

7.3.6.5 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (absolute thermal shutdown) and dynamic temperature protection (relative thermal shutdown). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

7.3.6.5.1 Thermal Protection Behavior

The thermal protection behavior can be split up into three categories of events that can happen. Figure 7-14 shows each of these categories.

1. **Relative thermal shutdown**: The device is enabled into an overcurrent event. The output current rises up to the I_{ILIM} level and the $\overline{FLT}$ goes low. With this large amount of current going through the junction temperature of the FET increases rapidly with respect to the controller temperature. When the power FET temperature rises T_{REL} amount above the controller junction temperature $\Delta T = T_{FET} – T_{CON} > T_{REL}$, the device shuts down. For auto-retry version, after t_{RETRY}, the part tries to restart. The latch version requires EN to be toggled to re-enable the channel. The $\overline{FLT}$ pin is asserted until the fault condition is cleared. The first plot in Figure 7-14 shows the relative thermal shutdown behavior for the auto-retry version.
2. **Absolute thermal shutdown**: the device is still enabled in an overcurrent event. However, in this case the junction temperature rises up and hits an absolute reference temperature, T_{ABS}, and then shuts down. For auto-retry version, the device does not recover until both $T_J < T_{ABS} – T_{hys}$ and the t_{RETRY} timer has expired. For latch version, toggling EN is required to re-enable the channel. The second plot in Figure 7-14 shows the absolute thermal shutdown behavior for the auto-retry version.
3. **Latch behavior**: the device is enabled into an overcurrent event. The DIAG_EN pin is high so that diagnostics can be monitored on SNS and FLT. For the latched version of the device, if the part shuts down due to a thermal fault, either relative thermal shutdown or absolute thermal shutdown, the device does not enable the channel until the EN pin is toggled. The third plot in Figure 7-14 shows the relative thermal shutdown behavior for the variants with LATCH pin when LATCH pin is HIGH.

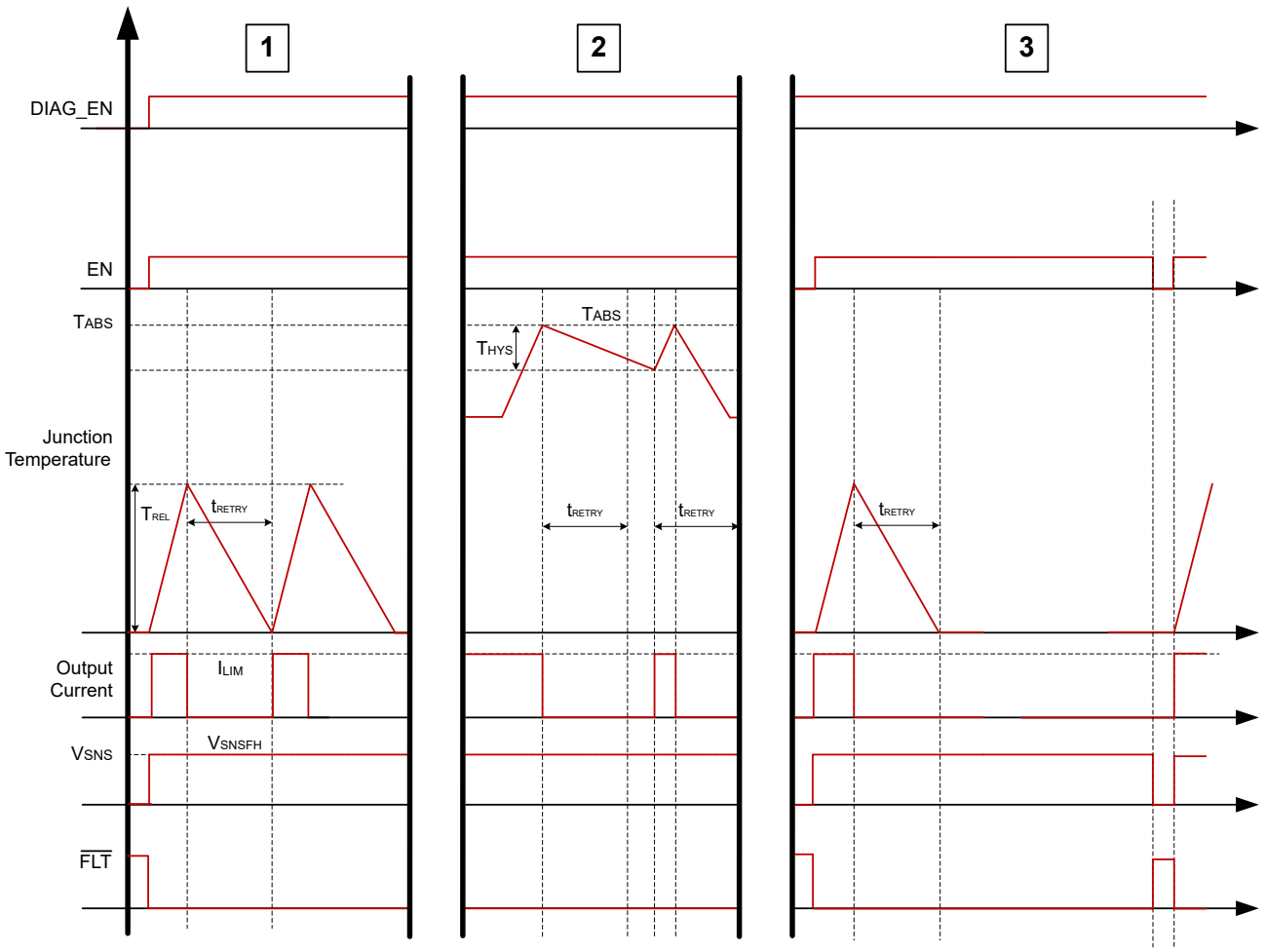


Figure 7-14. Thermal Behavior

7.3.7 Full Protections

7.3.7.1 UVLO Protection

The device monitors the supply voltage V_{VBB}, to prevent unpredicted behaviors when V_{VBB} is too low. When V_{VBB} falls down to V_{UVLOF}, the device shuts down. When V_{VBB} rises up to V_{UVLOR}, the device turns on.

7.3.7.2 Loss of GND Protection

When loss of GND occurs, all the channels are disabled regardless of control pin status, and the part is not powered.

Case 1 (loss of device GND): loss of GND protection is active when the thermal pad (Tab), I_{C_GND}, and current limit ground are one trace connected to the system ground, as shown in Figure 7-15.

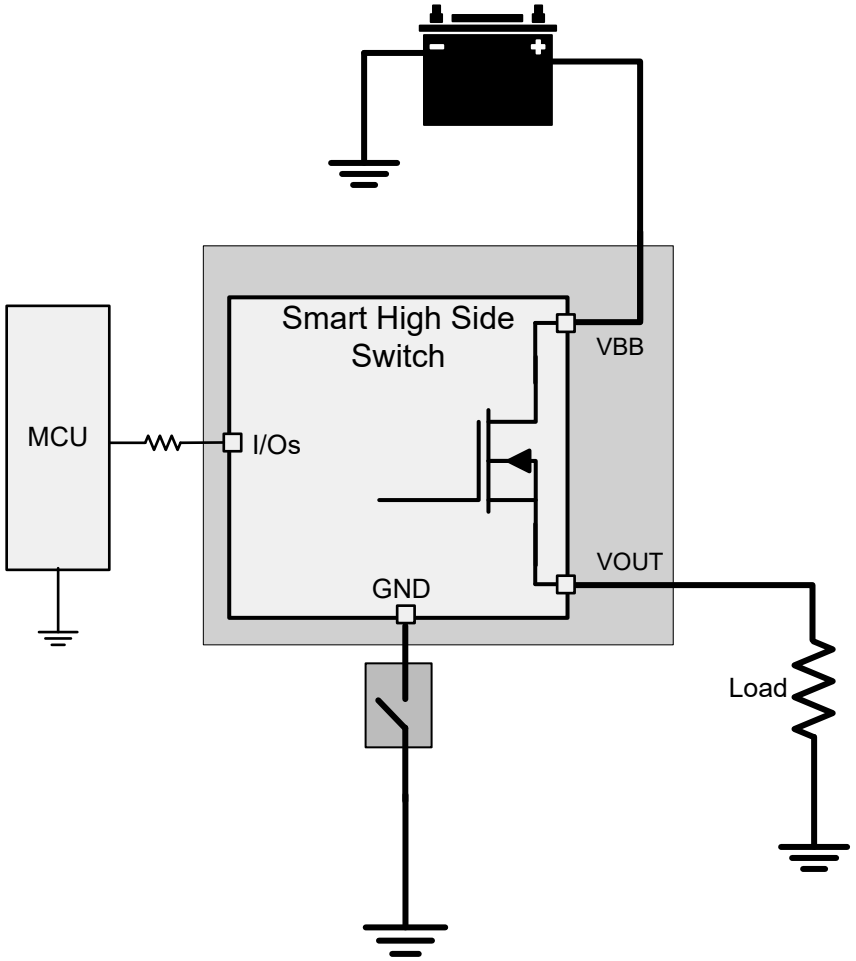


Figure 7-15. Loss of Device GND

Case 2 (loss of module GND): when the whole ECU module GND is lost, protections are also active. At this condition, the load GND remains connected.

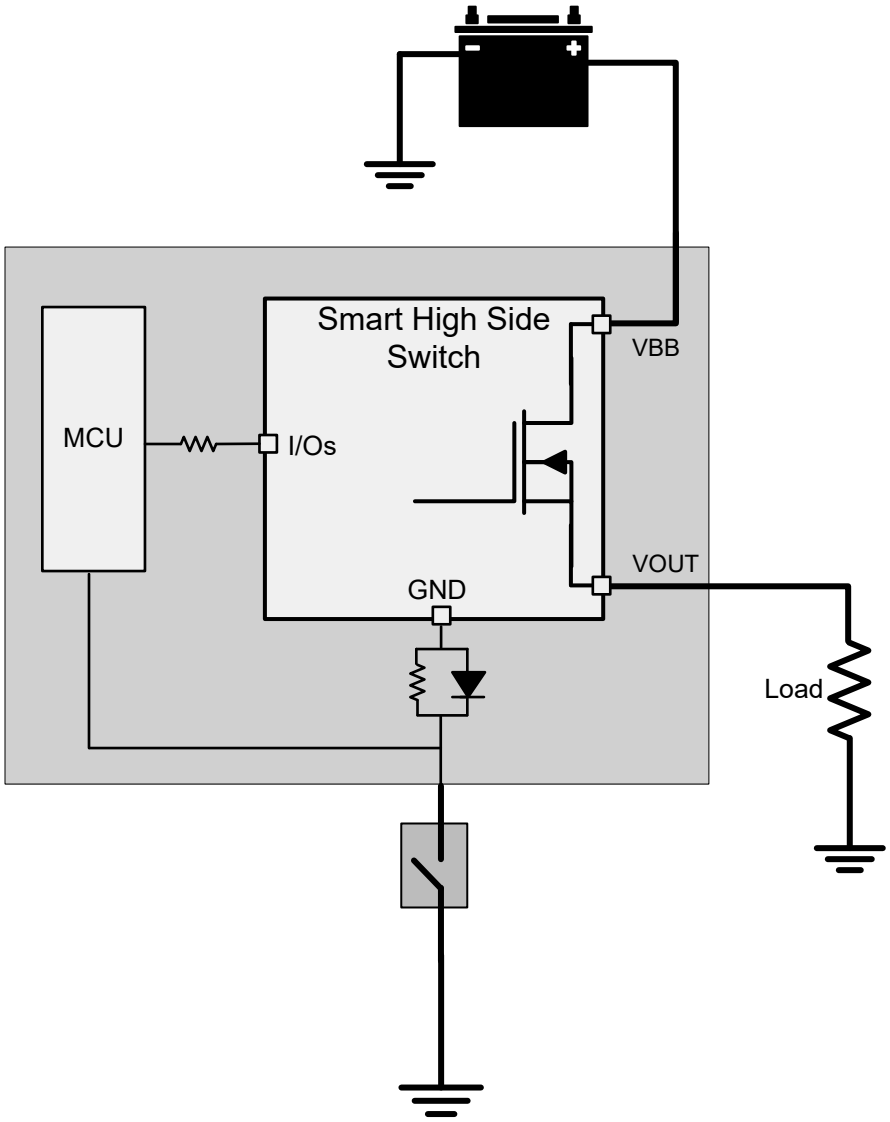


Figure 7-16. Loss of Module GND

7.3.7.3 Loss of Power Supply Protection

When loss of supply occurs, output is turned off regardless of whether the input is high or low. For a resistive or capacitive load, loss of supply protection is easy to achieve due to no more power. The worst case is a charged inductive load. In this case, the current is driven from all of the IOs to maintain the inductance output loop. TI recommends either the MCU serial resistor plus the GND network (diode and resistor in parallel) or external free-wheeling circuitry.

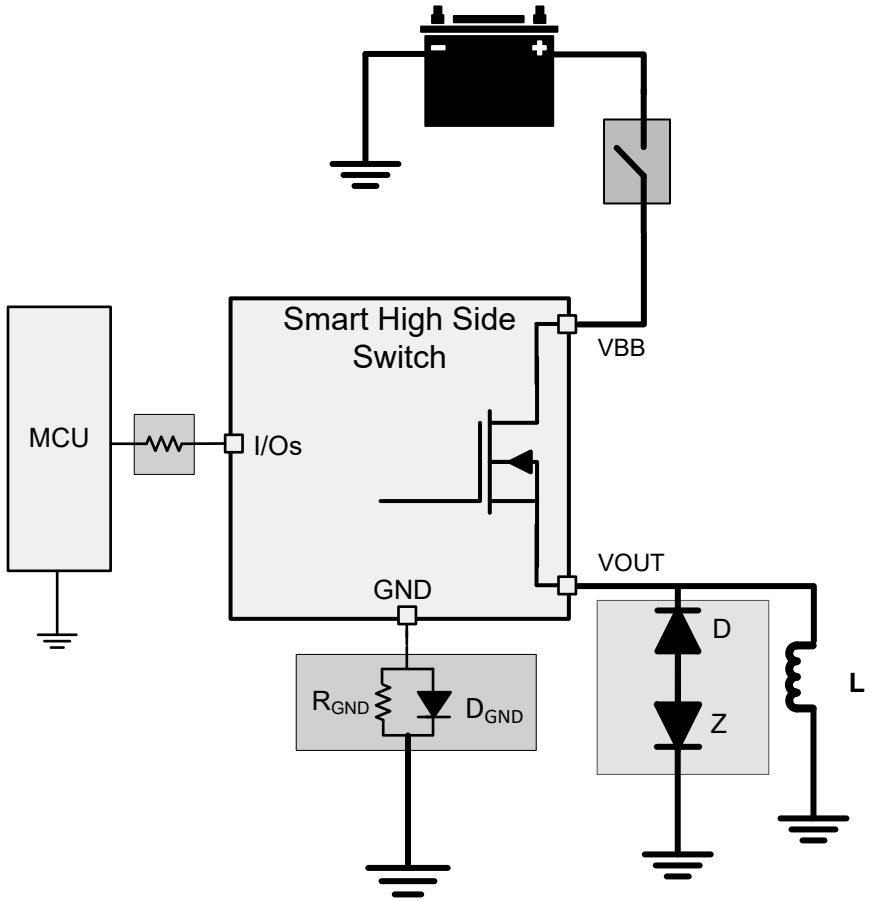


Figure 7-17. Loss of Battery

7.3.7.4 Loss of VDD

In the case of a loss of VDD supply input, the device continues to operate normally without any change in state. The only impact of the loss of VDD supply is an increase in quiescent current consumption through the VBB pin.

7.3.7.5 Reverse Current Protection

Method 1: block diode connected with V_{BB}. Both the device and load are protected when in reverse polarity. The blocking diode does not allow any of the current to flow during reverse battery condition.

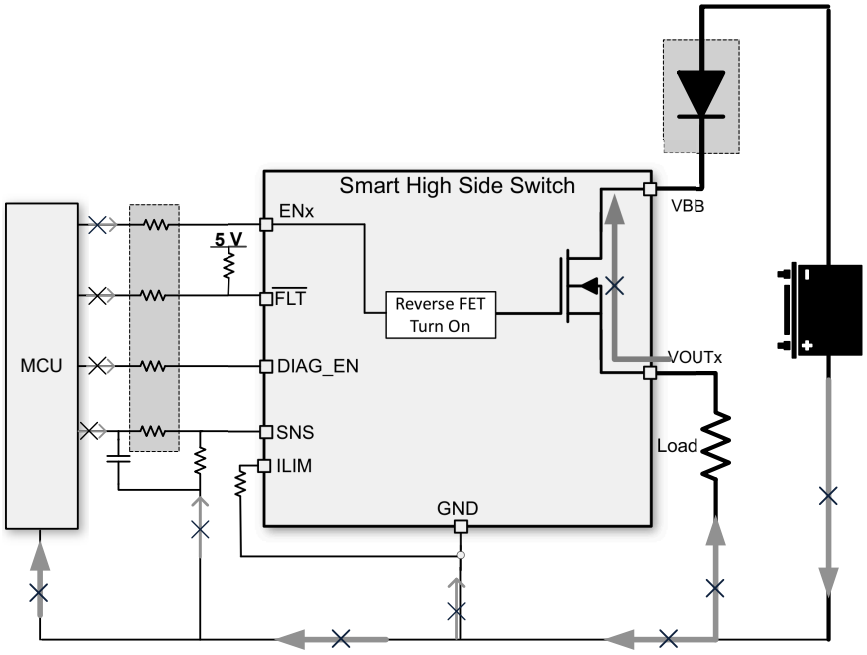


Figure 7-18. Reverse Protection With Block Diode

Method 2 (GND network protection): only the high-side device is protected under this connection. The load reverse current is limited by the impedance of the load itself. Note when reverse polarity happens, the continuous reverse current through the power FET must not make the heat build up be greater than the absolute maximum junction temperature. This can be calculated using the $R_{ON(REV)}$ value and the $R_{\theta JA}$ specification. In the reverse battery condition it is important that the FET comes on to lower the power dissipation. This action is achieved through the path from EN to system ground where the positive voltage is being applied. No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, ensure the following proper connections for the normal operation:

- Connect the current limit programmable resistor to the device GND.

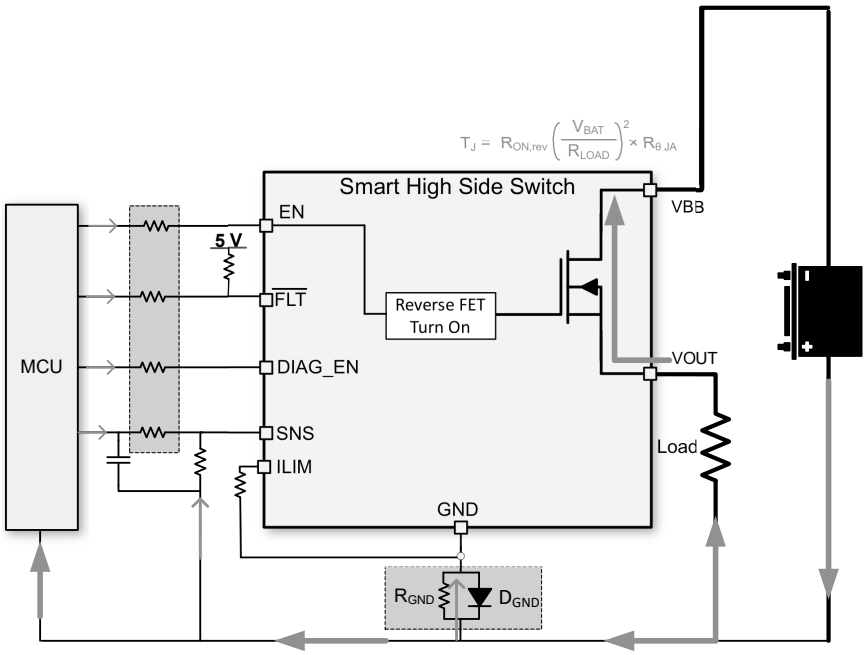


Figure 7-19. Reverse Protection With GND Network

- **Recommendation – resistor and diode in parallel:** a peak negative spike can occur when the inductive load is switching off, which can damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are a 1kΩ resistor in parallel with an I_F > 100mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.

  If multiple high-side power switches are used, the resistor can be shared among devices.
- **Ground Resistor:** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses.

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \quad (6)$$

  where

  – $-V_{CC}$ is the maximum reverse battery voltage (typically –16V).
  – $-I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in the *Absolute Maximum Ratings*.
- **Ground Diode:** A diode is needed to block the reverse voltage, which also brings a ground shift (≈ 600mV). Additionally, the diode must be ≈ 200V reverse voltage for the ISO 7637 pulse 1 testing so that it does not get biased.

7.3.7.6 Protection for MCU I/Os

In many conditions, such as the negative ISO pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin can damage the MCU I/O pins (more likely, the internal circuitry connected to the pins). Therefore, the serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 10kΩ resistance for the R_{PROT} resistors.

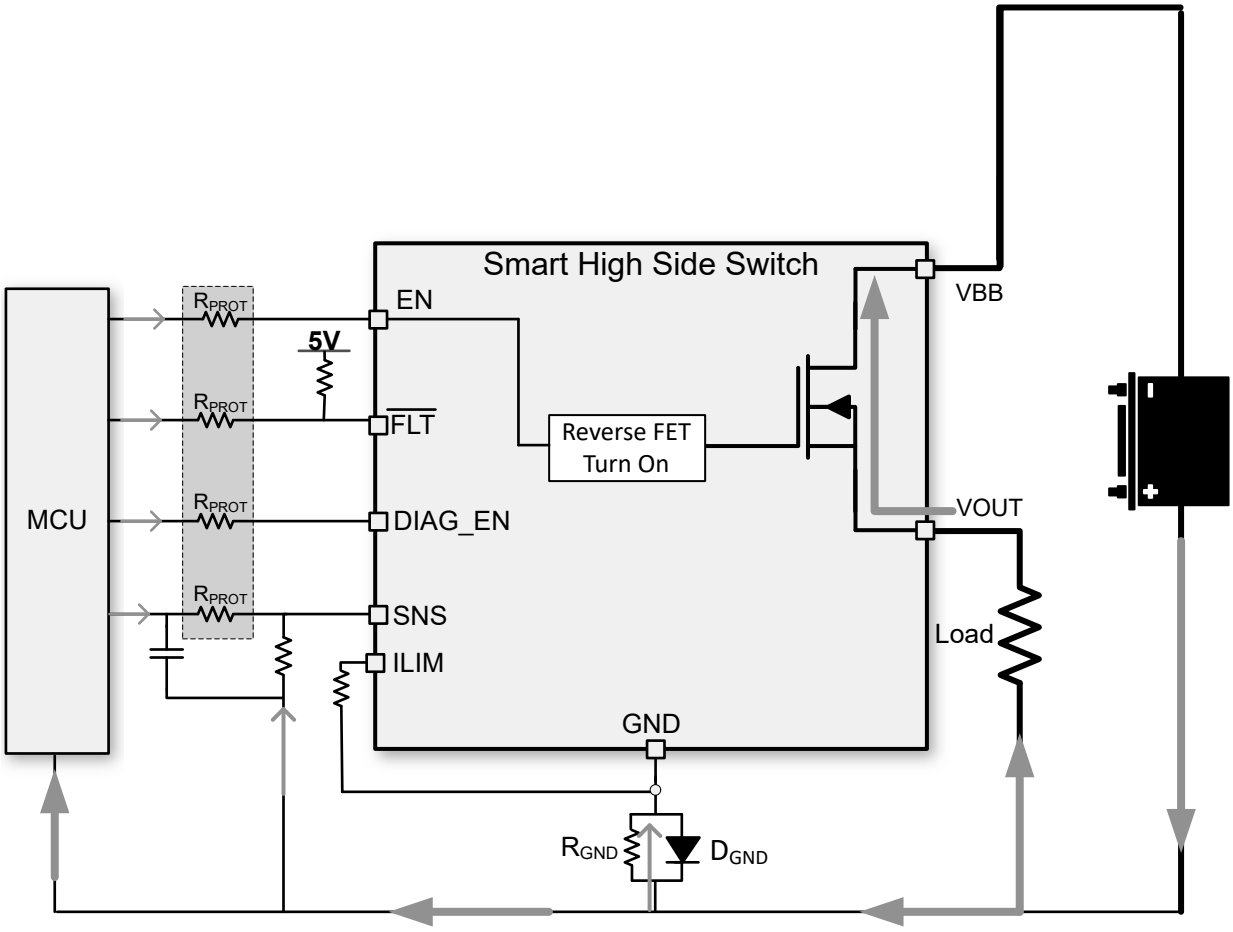


Figure 7-20. MCU I/O Protections

7.4 Device Functional Modes

7.4.1 Operational Modes

The device has several states to transition into based on the ENx pins and the DIAG_EN pin.

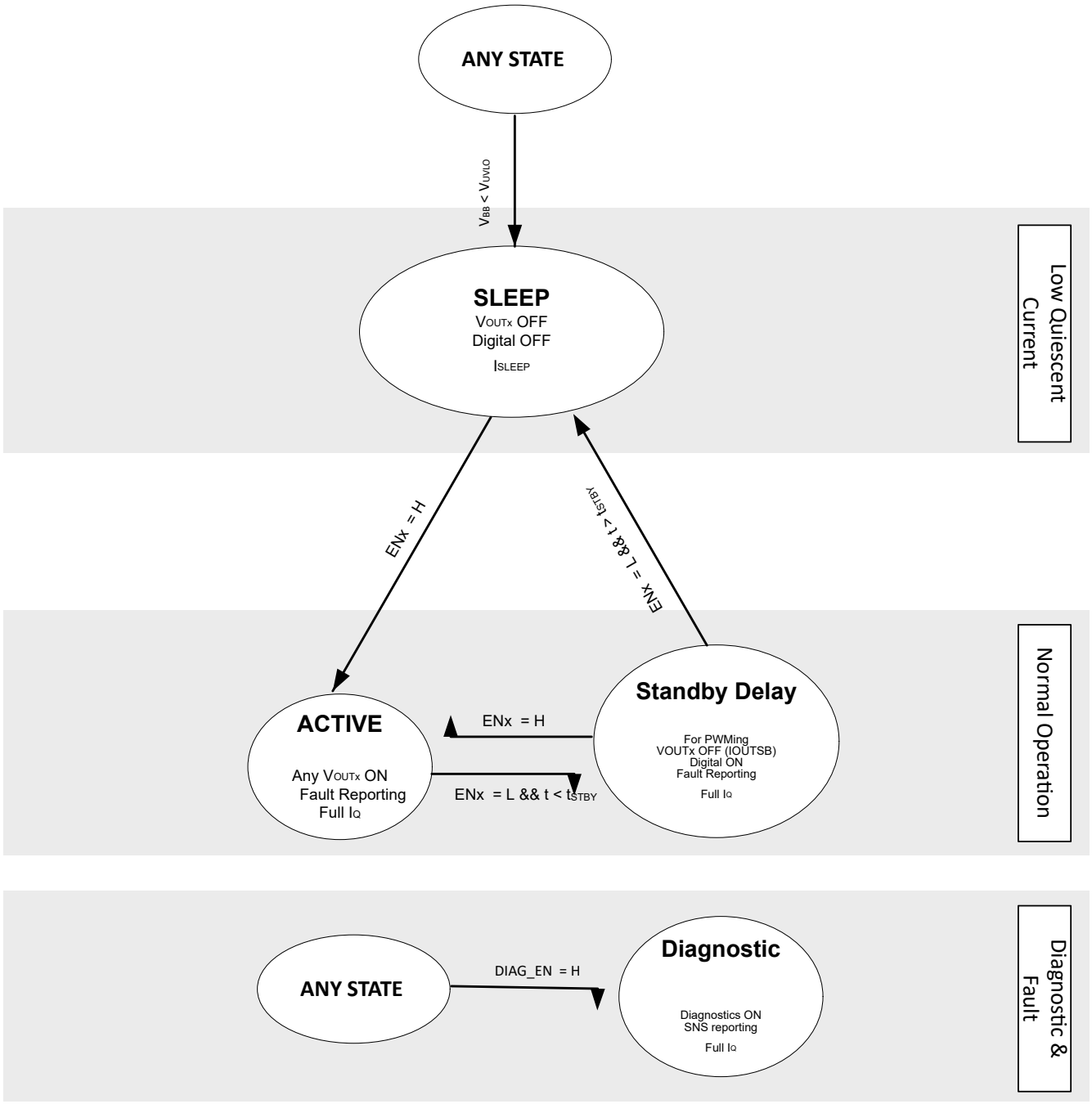


Figure 7-21. State Diagram

SLEEP

In the SLEEP state, everything inside the device is turned off and the quiscent current is the I_{SLEEP}. The device only transitions out of the SLEEP state if the ENx pins or DIAG_EN pin is pulled high. From the SLEEP state, the device is able to transfer into the ACTIVE state if any of the ENx pins are pulled high, or into the DIAGNOSTIC state if the DIAG_EN pin, without any of the ENx pins, goes high. Additionally, if the device is in any of the states and VBB drops below V_{UVLOF}, the device transitions into SLEEP state.

DIAGNOSTIC

The DIAGNOSTIC state is when the device is outputting diagnostics on the SNS and $\overline{FLT}$ pins. This can happen when the device is in any previous state and the DIAG_EN pin goes high. The off-state diagnostics are comprised of open load detection in off state and short to battery detection. The SNS pin only outputs a fault for the channel associated to the SEL pin values. From the DIAGNOSTIC state, the device transfers into the ACTIVE state if the DIAG_EN pin goes back low and any channel is on or the STANDBY DELAY state if all channels are OFF.

ACTIVE

The ACTIVE state is when any of the channel outputs are on by the ENx pin associated. In the ACTIVE state, the current limit value is set by the external resistor on the ILIM pin. If the DIAG_EN pin is pulled high while in the ACTIVE state, the SNS pin outputs a proportional current to the load current of the channel associated to the SEL pins configuration until a fault occurs on that channel. The device can transition out of the ACTIVE state by turning off all of the channels while DIAG_EN is high or low, or a fault occurring. If all of the channels turn off and DIAG_EN is high, the device transitions into the DIAGNOSTIC state. If all of the channels turn off and the DIAG_EN pin is low, then the device transfers into the STANDBY DELAY state. However, if the ENx pins are still high and a fault occurs, the device transitions into the FAULT state.

FAULT

The FAULT state occurs when the ENx pins are high but some event has caused the channel to behave differently from normal operation. These fault events include: absolute thermal shutdown, relative thermal shutdown, and current limit. Each of these fault events either directly or eventually shut off the channel to protect the device and system. After the device shuts off and waits for t_{RETRY} amount of time and has cooled below the T_{HYS} threshold, the output/s that were on try to come back on again and the device transitions back into the ACTIVE state or DIAGNOSTIC state.

STANDBY DELAY

The STANDBY DELAY state is when the ENx pins are all low, outputs are all turned off and the DIAG_EN pin is also low but there has not yet been t_{STBY} amount of time. This state is included so that the channel outputs can be PWM'd without all of the internal rails being cut off and put to SLEEP mode. Once the device has waited t_{STBY}, the device completely shuts down and transitions into SLEEP. However, if during t_{STBY}, ENx were to go high, the device transitions into ACTIVE without shutting completely down. Similarly if the DIAG_EN goes high, the device transitions into DIAGNOSTIC.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS482H85-Q1 device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

8.2 Typical Application

The following figure shows an example of the external circuitry connections.

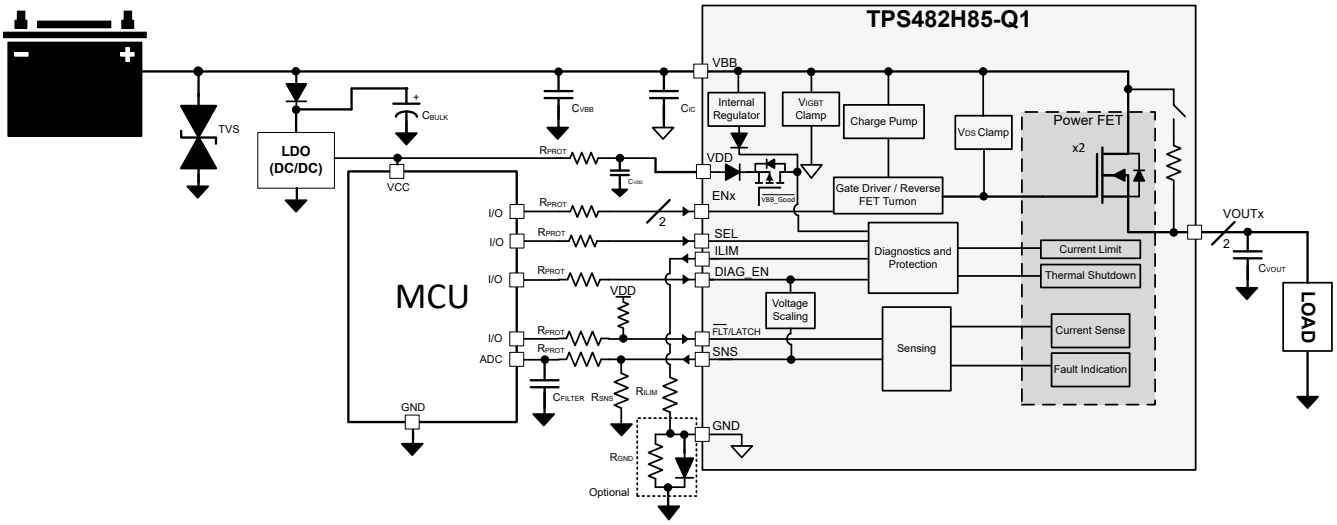


Figure 8-1. Typical Application Diagram for GPIO version

Table 8-1. Recommended Component Values

COMPONENT	DESCRIPTION	PURPOSE
TVS	SMBJ70CA	Filter voltage transients coming from battery
C_{VBB}	4.7µF	Stabilize the input supply. Prevent the device from losing power during short-circuit situation.
C_{IC}	100nF	Minimal amount of capacitance on input for EMI mitigation
C_{BULK}	10µF	Help filter voltage transients on the supply rail
C_{VDD}	100nF	Stabilize the VDD supply and limit supply excursions. Needed with either external or internal VDD supplies.
R_{PROT}	10kΩ	Protection resistor for microcontroller and device I/O pins
R_{LIM}	Discrete values as listed in Table 7-1	Set current limit threshold
R_{SNS}	1kΩ	Translate the sense current into sense voltage
C_{FILTER}	150pF	Coupled with RPROT on the SNS line creates a low pass filter to filter out noise going into the ADC of the MCU
C_{VOUT}	22nF	Improves EMI performance, filtering of voltage transients
R_{PULLUP}	4.7kΩ	Pull up resistor for open-drain pins ($\overline{FLT}$ and LPM)

Table 8-1. Recommended Component Values (continued)

COMPONENT	DESCRIPTION	PURPOSE
R_{GND}	1kΩ	Stabilize GND potential during turn-off of inductive load
D_{GND}	MSX1PJ-M3/89A Diode	Keeps GND close to system ground during normal operation

8.2.1 Design Requirements

Table 8-2. Example Design Requirements

PARAMETER	VALUE
V_{DIAG_EN}	5V
$I_{LOAD,max}$	1A
$I_{LOAD,min}$	20mA
$V_{ADC,min}$	5mV
V_{HR}	1V

8.2.2 Detailed Design Procedure

To keep the 1A nominal current in the 0V to 4V current-sense range, calculate the R_{SNS} resistor using Equation 1. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

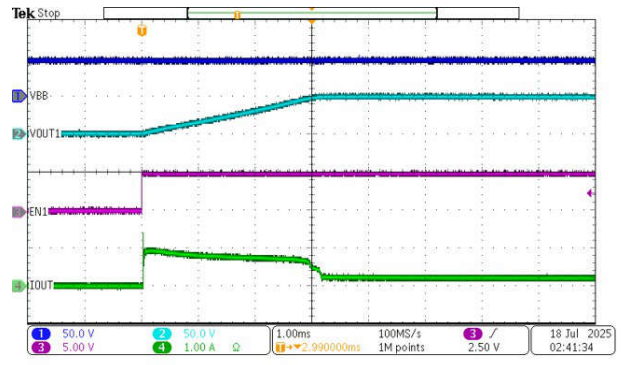
$$V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \leq R_{SNS} \leq (V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \quad (7)$$

The design requirement listed in Table 8-2 yields 500Ω ≤ R_{SNS} ≤ 8000Ω, and 1kΩ R_{SNS} satisfies the requirements.

To set the adjustable current limit value, use the R_{ILIM} recommended in the Table 7-1. In this application, to leave enough margin for the current transient and ripple, a 45.3kΩ R_{ILIM} resistor satisfies the requirements.

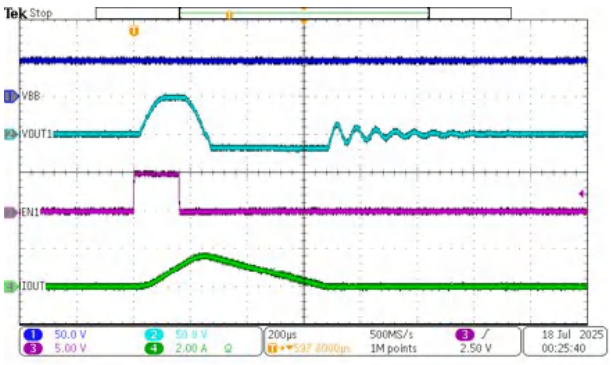
8.2.3 Application Curves

Figure 8-2 shows a test example of soft-start when driving a big capacitive load. Figure 8-3 shows the VDS clamp engaging during inductive load discharge.



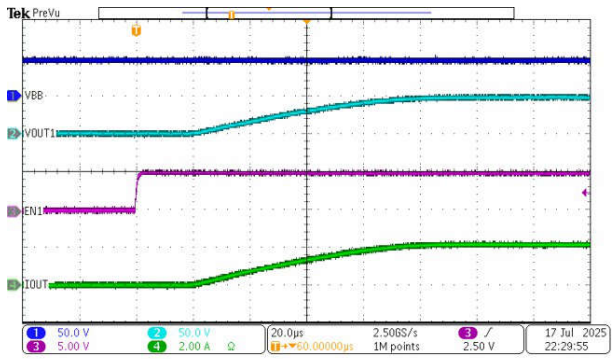
V_{BB} = 48V R_{ILIM} = 59kΩ Z_{OUT} = 100Ω + 47µF
T_A = 25°C

Figure 8-2. Capacitive Load Driving



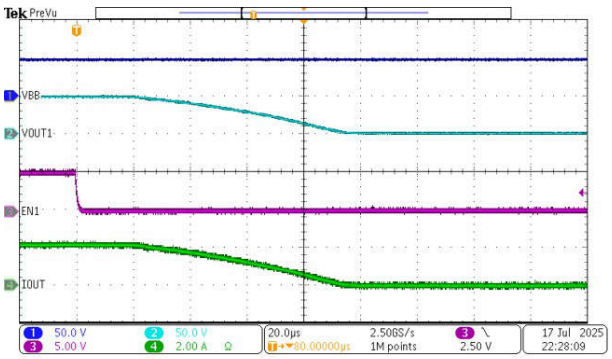
V_{BB} = 48V Z_{OUT} = 5mH T_A = 25°C

Figure 8-3. Inductive Load Discharge



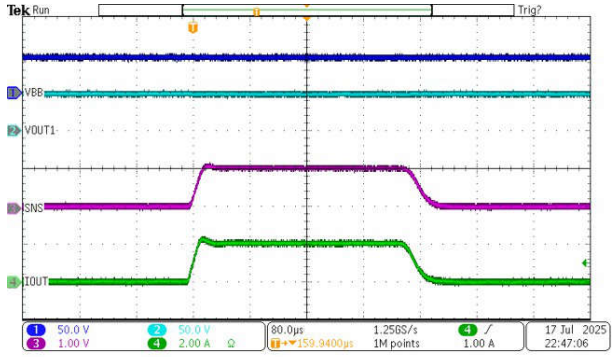
V_{BB} = 48V Z_{OUT} = 24Ω T_A = 25°C

Figure 8-4. Turn-on with Resistive Load



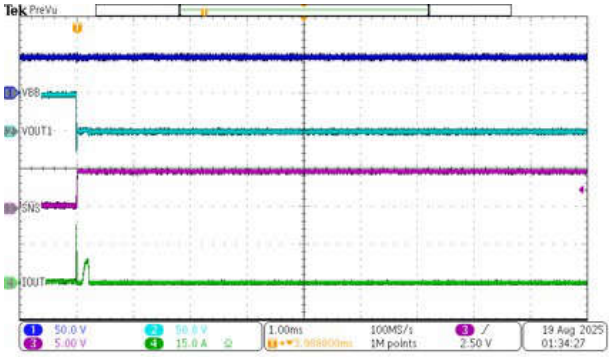
V_{BB} = 48V Z_{OUT} = 24Ω T_A = 25°C

Figure 8-5. Turn-off with Resistive Load



V_{BB} = 48V Load: 0A -> 2A -> 0A T_A = 25°C

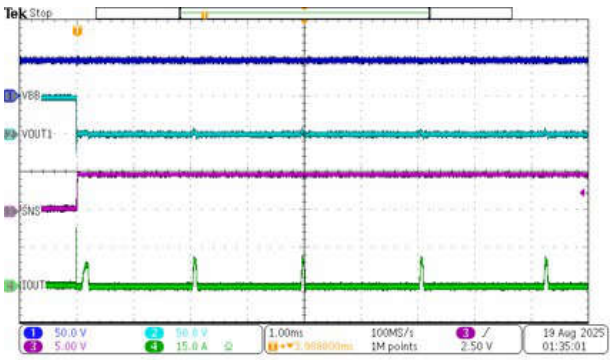
Figure 8-6. Load Transient Behavior



V_{BB} = 48V R_{ILIM} = OPEN Z_{OUT} = 100mΩ + 5µH

T_A = 25°C

Figure 8-7. Hot Short (Latch behavior)



V_{BB} = 48V R_{ILIM} = OPEN Z_{OUT} = 100mΩ + 5µH

T_A = 25°C

Figure 8-8. Hot Short (Retry behavior)

8.3 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 24V/48V automotive system. The supply voltage must be within the range specified in the *Recommended Operating Conditions*.

Table 8-3. Voltage Operating Ranges

VBB VOLTAGE RANGE	NOTE
6V to 58V	Nominal 24V/48V automotive battery voltage range. All parametric specifications apply and the device is fully functional and protected.
58V to 70V for unidirectional clamp version	Extended upper 48V automotive battery operation. Device is fully functional and protected but some parametrics such as R_{ON}, current sense accuracy, current limit accuracy, and timing parameters can deviate from specifications. Check the individual specifications in Section 6.5 to confirm the voltage range it is applicable for.
58V to 65V for bidirectional clamp version	Extended upper 48V automotive battery operation. Device is fully functional and protected but some parametrics such as R_{ON}, current sense accuracy, current limit accuracy, and timing parameters can deviate from specifications. Check the individual specifications in Section 6.5 to confirm the voltage range it is applicable for.
65V to 80V for bidirectional clamp version	Max of 100µs duration is allowed in this voltage range. . Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.

8.4 Layout

8.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. The PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package VBB and VOUT pads to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

8.4.2 Layout Examples

8.4.2.1 Without a GND Network

Without a GND network, tie the GND pin to the board GND copper directly. Put thermal vias under VBB and VOUT pins for better thermal performance.

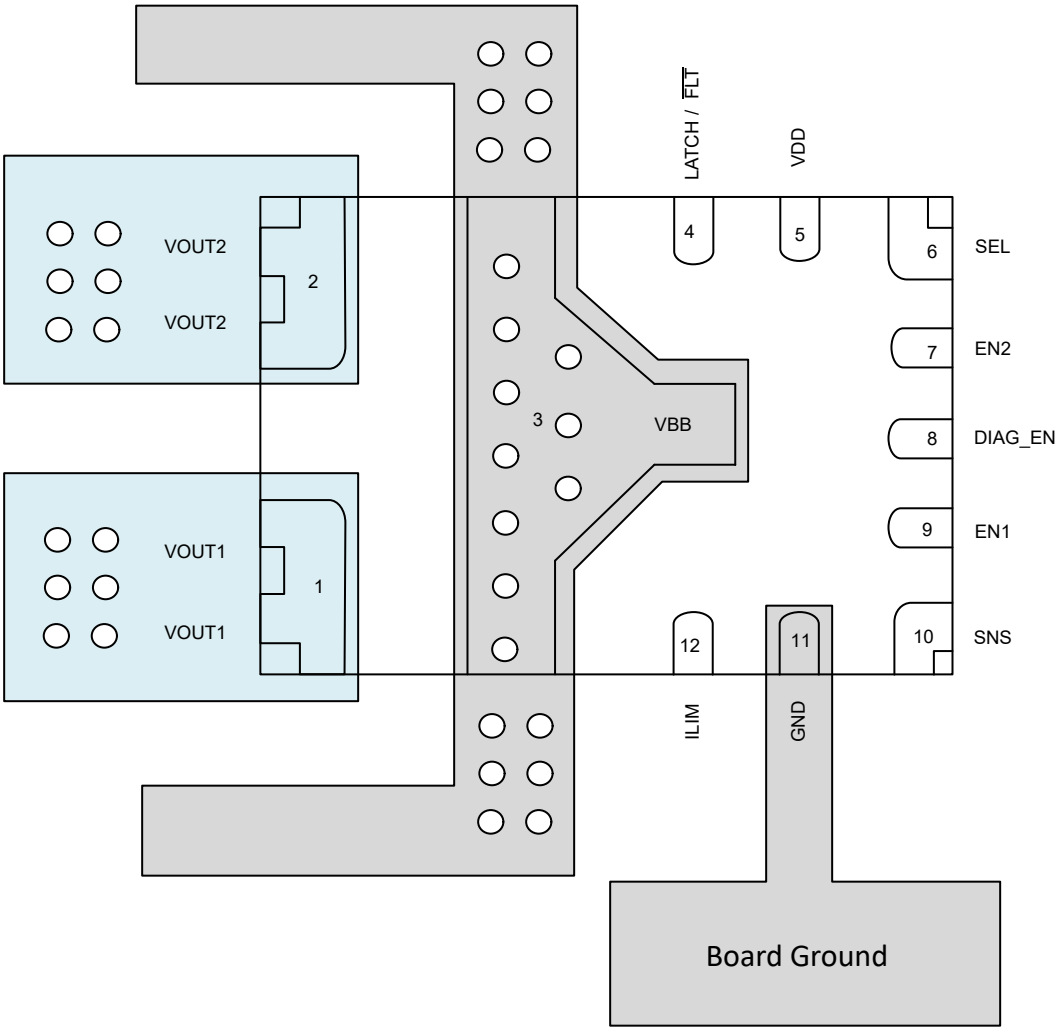


Figure 8-9. Layout Example Without a GND Network

8.4.2.2 With a GND Network

With a GND network, have the IC GND and board GND connected via the ground network. Put thermal vias under VBB and VOUT pins for better thermal performance.

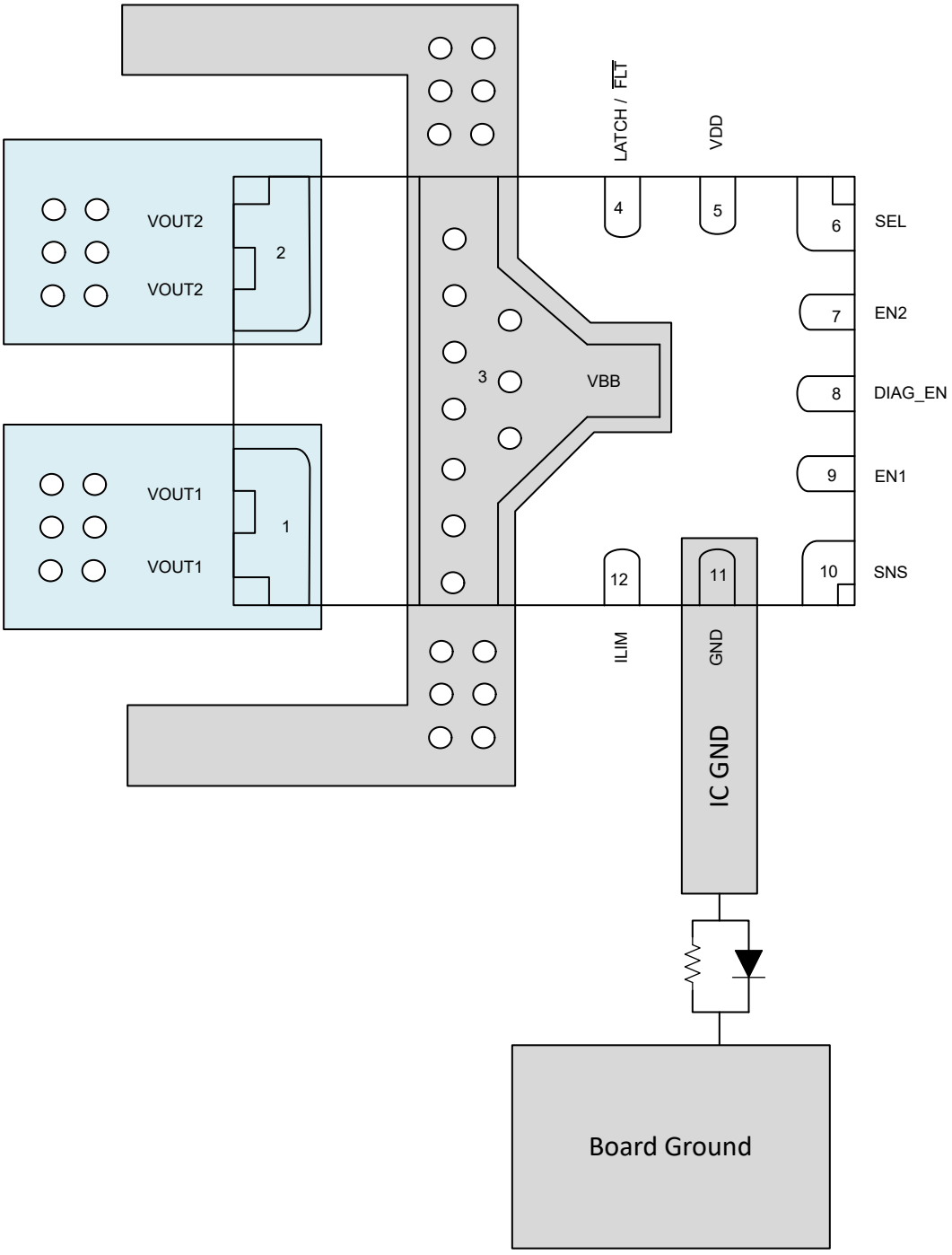


Figure 8-10. Layout Example With a GND Network

9 Device and Documentation Support

9.1 Third-Party Products Disclaimer

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9.3 Support Resources

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2025) to Revision A (October 2025)	Page
• Changed status from Advance Information to Production Data	1
• FLT now reports regardless of DIAG_EN	24
• FLT now reports regardless of DIAG_EN	25
• Updated Table 7-3 to add description for auto-retry and latch versions	25

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS482H85AQCHURQ1	Active	Preproduction	VQFN-HR (CHU) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS482H85BQCHURQ1	Active	Preproduction	VQFN-HR (CHU) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS482H85BQCHURQ1.A	Active	Preproduction	VQFN-HR (CHU) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

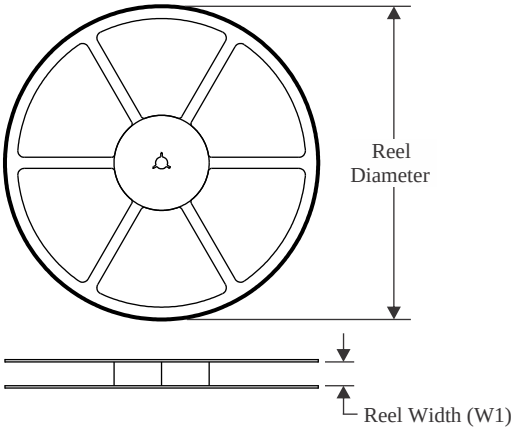
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

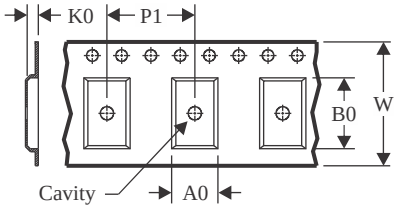
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

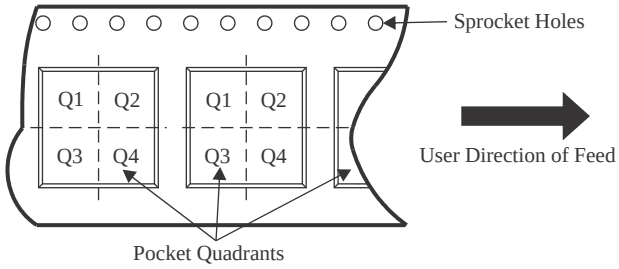


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

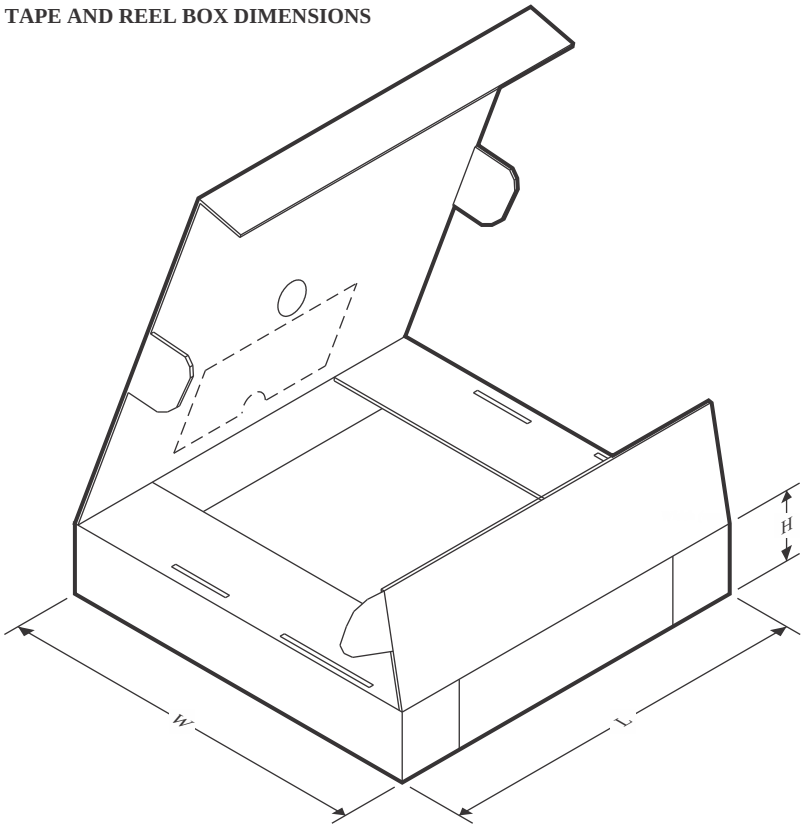
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS482H85AQCHURQ1	VQFN-HR	CHU	12	3000	330.0	12.4	3.3	3.8	1.2	8.0	12.0	Q2
TPS482H85BQCHURQ1	VQFN-HR	CHU	12	3000	330.0	12.4	3.3	3.8	1.2	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS482H85AQCHURQ1	VQFN-HR	CHU	12	3000	367.0	367.0	35.0
TPS482H85BQCHURQ1	VQFN-HR	CHU	12	3000	367.0	367.0	35.0

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