TPS4812-Q1 双方向 IMON、低消費電力モード、負荷ウェークアップ、I²t、診断機能付き、100V 低 I_Q 車載用ハイサイド スイッチ コントローラ

1 特長

- AEC-Q100 車載グレード 1 温度認定済み
- 3.5V～95V の入力範囲 (絶対最大定格 100V)
- 最低 –65V までの逆入出力保護
- 内蔵 12V チャージ ポンプ
- 低消費電力モードでの I_Q = 20µA ($\overline{LPM}$ = Low)
- 低シャットダウン電流 (EN/UVLO = Low): 1µA
- デュアル ゲートドライブ: GATE: ソース 0.5A / シンク 2A G: ソース 100µA / シンク 0.39A
- 調整可能なサーキット ブレーカ タイマ (I2t) 付きの高精度 I²t 過電流保護 (IOC)
- 高精度で高速 (5µs) の短絡保護機能
- 可変の負荷ウェークアップ スレッショルド、または WAKE 通知付きの $\overline{LPM}$ トリガによる、低消費電力モードからアクティブ モードへの高速遷移 (5µs)
- 高精度アナログ双方向電流モニタ出力 (IMON、I_DIR): ±2% (30mV V_{SNS})
- NTC ベースの過熱検出 (TMP) とモニタリング出力 (ITMPO)
- 短絡フォルト時のフォルト表示 ($\overline{FLT}$)、I²t、チャージ ポンプ UVLO、過熱
- TPS48120-Q1 (I²t イネーブル)、TPS48121-Q1 (I²t ディセーブル)
- 高精度 (±2%) で調整可能な低電圧誤動作防止 (UVLO)

2 アプリケーション

- パワー ディストリビューション ボックス
- ボディ コントロール モジュール
- DC/DC コンバータ
- バッテリ マネージメント システム

3 概要

TPS4812-Q1 は、保護および診断機能を備えた 低 IQ のスマート ハイサイド ドライバのファミリです。このデバイスは、3.5V～95V の広い動作電圧範囲、100V の絶対最大電圧を備えており、12V、24V、48V の車載用システム設計に適しています。

この製品には 2 つのゲート ドライブが内蔵されており、0.5A のソースと 2A のシンク (GATE) と、100µA のソースと 0.39A のシンク (G) があります。$\overline{LPM}$ が Low のとき、低消費電力パスがオンに維持され、メイン FET がオフになり、IQ は 20µA (標準値) になります。DRN と CS2- の間に配置された R_{BYPASS} 抵抗を使用して、自動負荷ウェークアップのスレッショルドを調整できます。EN/UVLO が Low のとき、IQ は 1µA (標準値) に減少します。

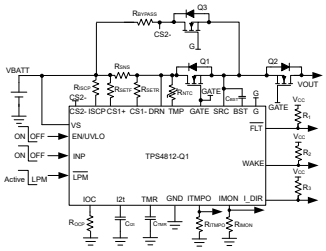
このデバイスは、高精度の双方向電流センシング (±2%) 出力 (IMON、I_DIR) を備えており、外付け R_{SNS} 抵抗と $\overline{FLT}$ 通知を使用して、可変の I²t ベースの過電流および短絡保護を実現しています。自動リトライおよびラッチオフ フォルト動作は設定可能です。このデバイスは、外部 FET の過熱検出用に、NTC ベースの温度センシング (TMP) およびモニタリング監視出力 (ITMPO) も備えています。

TPS4812-Q1 は、23 ピン VQFN パッケージで供給されます。

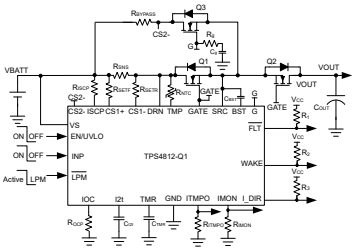
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS48120-Q1、TPS48121-Q1	RGE (VQFN、23)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



負荷ウェークアップ付き PAAT 負荷を駆動する TPS48120-Q1 アプリケーション回路



負荷ウェークアップおよびバルク コンデンサ充電付きで PAAT 負荷を駆動する TPS48120-Q1 アプリケーション回路

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4 Device Comparison

表 4-1. Device Comparison

Device name /Feature	TPS48120-Q1	TPS48121-Q1
I^2T Protection	Yes	No

5 Pin Configuration and Functions

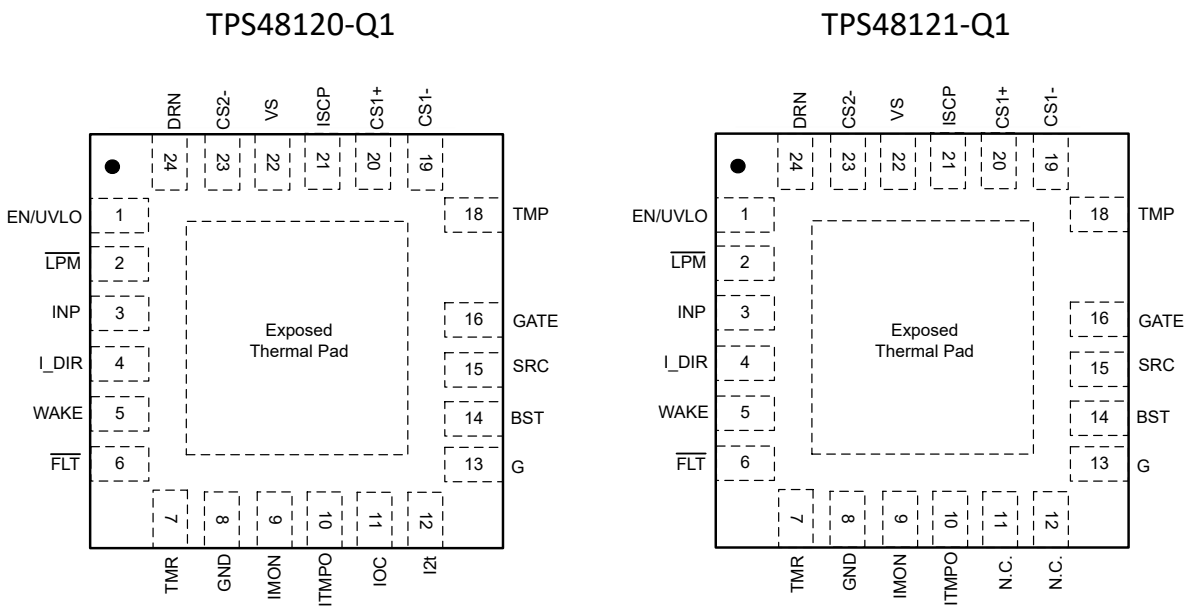


図 5-1. RGE Package, 23-Pin VQFN (Transparent Top View)

表 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	TPS48120-Q1	TPS48121-Q1		
EN/UVLO	1	1	I	EN/UVLO input. A voltage on this pin above $V_{(UVLOR)}$ 1.21V enables normal operation. If EN/UVLO is below $V_{(UVLOF)}$ then Gate drives are turned OFF. Forcing this pin below $V_{(ENF)}$ 0.3V shuts down the device reducing quiescent current to approximately 1µA (typ). Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pull down of 100nA pulls EN/UVLO low and keeps the device in OFF state.
$\overline{\text{LPM}}$	2	2	I	Mode control input. When driven high, the device enters into active mode. When driven low, the devices enter into low power mode. If low power mode is not required, $\overline{\text{LPM}}$ pin can be tied to EN/UVLO pin. When $\overline{\text{LPM}}$ is left floating an internal pull down of 100nA pulls $\overline{\text{LPM}}$ low.
INP	3	3	I	Input signal for external FET control. CMOS compatible input reference to GND that sets the state of GATE pin. INP has an internal weak pull down of 100nA to GND to keep GATE pulled to SRC when INP is left floating.
I_DIR	4	4	I	Open drain I_DIR output. This pin is asserted low by device when current through CS1+ and CS1– flows in reverse direction.

表 5-1. Pin Functions (続き)

PIN			TYPE[1]	DESCRIPTION
NAME	TPS48120-Q1	TPS48121-Q1		
WAKE	5	5	O	Open drain WAKE output. This pin is asserted low by device when device enters into active mode (when $\overline{LPM}$ is driven high or when a load wakeup event has occurred).
$\overline{FLT}$	6	6	O	Open drain fault output. $\overline{FLT}$ goes low during charge pump UVLO, Main FET SCP, I^2t timer trigger, NTC based external FET overtemperature fault. This pin asserts low after the voltage on the I2t pin has reached the fault threshold of 2V. This pin indicates the main FET is about to turn off due to an overload condition. This pin asserts low along with GATE turn off during short-circuit. The $\overline{FLT}$ pin does not go to a high impedance state until the overcurrent condition and the auto-retry time expire.
TMR	7	7	I	Auto-retry or latch timer input after overcurrent fault. A capacitor across TMR pin to GND sets the times for retry periods. Leave open for fastest setting. Connect resistor across C_{TMR} from TMR pin to GND for latch-off functionality.
GND	8	8	G	Connect GND to system ground.
IMON	9	9	O	Analog bi-directional current monitor output. This pin sources a scaled down ratio of current through the external current sense resistor R_{SNS}. A resistor from this pin to GND converts current proportional to voltage. If unused, leave floating or can be connected to ground.
ITMPO	10	10	O	Analog temperature output. Analog voltage feedback provides a voltage proportional to thermistor temperature. If unused, leave floating.
IOC	11	—	I	Overcurrent detection setting. A resistor across IOC to GND sets the over current comparator threshold. IOC pin can also be driven externally using MCU.
N.C.	—	11	—	No connect.
I2t	12	—	O	I2t timer input. A capacitor across I2t pin to GND sets the times for overcurrent (t_{OC}).
N.C.	—	12	—	No connect.
G	13	13	O	Gate of external bypass FET. 100µA peak source and 0.39A sink capacity. Connect to the gate of the external bypass FET.
BST	14	14	O	High side bootstrapped supply. An external capacitor with a minimum value of 0.1µF should be connected between this pin and SRC. Voltage swing on this pin is 12V to (VIN + 12V).
SRC	15	15	O	Source connection of the external FET.
GATE	16	16	O	High current gate driver pull-up and pull-down. 0.5A peak source and 2A sink capacity. This pin pulls GATE up to BST and down to SRC. For the fastest tun-on and turn-off, tie this pin directly to the gate of the external high side MOSFET in main path.

表 5-1. Pin Functions (続き)

PIN			TYPE(1)	DESCRIPTION
NAME	TPS48120-Q1	TPS48121-Q1		
TMP	18	18	I	Temperature input. Analog connection to external NTC thermistor Connect TMP pin directly to VS if this feature is not used
CS1–	19	19	I	Main path current sense negative input. Connect a resistor (R_{SETR}) across CS1– to the external current sense resistor to set IMON gain in reverse direction.
CS1+	20	20	I	Main path current sense positive input. Connect a resistor (R_{SETF}) across CS1+ to the external current sense resistor to set IMON gain in forward direction. Connect CS1+ and CS1– to VBATT if main FET current sensing is not used.
ISCP	21	21	I	Short-circuit detection threshold setting. Connect ISCP to DRN if short-circuit protection is not desired.
VS	22	22	P	Supply pin of the controller.
CS2–	23	23	I	Bypass path current sense negative input.
DRN	24	24	I	Main path SCP sense negative input. Connect DRN+ and CS2– together to VBATT after RSNS if bypass path is not used.
GND	Thermal Pad	—	—	Connect exposed thermal pad to GND plane.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input pins	VS, CS1+, CS1–, DRN, CS2–, ISCP, TMP to GND	–65	100	V
Input pins	VS, CS1+, CS1–, DRN, CS2–, ISCP, TMP to SRC	–65	100	V
Input pins	SRC to GND	–65	100	V
Input pins	GATE, G, BST to SRC	–0.3	19	V
Input pins	TMR to GND	–0.3	5.5	V
Input pins	IOC to GND, TPS48120-Q1 only	–1	5.5	V
Input pins	EN/UVLO, INP, $\overline{LPM}$; $V_{(VS)}$ > 0 V	–1	100	V
Input pins	EN/UVLO, INP, $\overline{LPM}$; $V_{(VS)}$ ≤ 0 V	$V_{(VS)}$	(100 + $V_{(VS)}$)	V
Input pins	CS1+ to CS1–	–0.3	0.4	V
Input pins	DRN to CS2–	–5	100	V
Output pins	$\overline{FLT}$, I_DIR, WAKE to GND	–1	20	V
Output pins	IMON to GND	–1	5.5	V
Output pins	I2t, ITMPO to GND, TPS48120-Q1 only	–1	7.5	V
Output pins	ITMPO to GND, TPS48121-Q1 only	–1	7.5	V
Output pins	GATE, G, BST to GND	–65	112	V
Sink current	$I_{(\overline{FLT})}$, $I_{(I\_DIR)}$, $I_{(WAKE)}$		10	mA
Sink current	$I_{(CS1+)}$ to $I_{(CS1–)}$, 1msec ; $I_{(DRN)}$ to $I_{(CS2–)}$, 1msec		100	mA
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input pins	VS, CS1+, CS1–, DRN, CS2–, ISCP, TMP to GND	–60		95	V
Input pins	EN/UVLO, INP, $\overline{LPM}$	0		95	V
Input pins	IOC, TMR to GND, , TPS48120-Q1 only	0		5	V
Input pins	TMR to GND, TPS48121-Q1 only	0		5	V
Output pins	I2t, IMON, ITMPO to GND, TPS48120-Q1 only	0		5	V
Output pins	IMON, ITMPO to GND, TPS48121-Q1 only	0		5	V
Output pins	$\overline{FLT}$, WAKE, I_DIR to GND	0		15	V
External capacitor	VS, SRC to GND	22			nF

6.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
External capacitor	BST to SRC	0.1			µF
External capacitor	I2t to GND	10			nF
External capacitor	TMR to GND	1			nF
Tj	Operating junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		TPS4812x-Q1 RGE (VQFN) 23 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40 °C to +125°C. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VS)						
VS	Operating input voltage		3.5		95	V
$V_{(S\_PORR)}$	Input supply POR threshold, rising		2.06	2.6	3.12	V
$V_{(S\_PORF)}$	Input supply POR threshold, falling		2	2.5	3.01	V
	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = $V_{(\overline{LPM})}$ = 2 V		430	525	µA
	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = $V_{(\overline{LPM})}$ = 2 V TPS48121-Q1 Only		370	470	µA
	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2V, $V_{(\overline{LPM})}$ = 0 V		20	24	µA
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(SRC)}$ = 48 V, $V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V		0.9	3.4	µA
$I_{(REV\_VS)}$	$I_{(VS)}$ leakage current during Reverse Polarity	0 V ≤ $V_{(VS)}$ ≤ – 65 V			60	µA
$I_{(REV\_SRC)}$	$I_{(SRC)}$ leakage current during Reverse Polarity	0 V ≤ $V_{(VS)}$ ≤ – 65 V			27	µA
ENABLE, UNDERVOLTAGE LOCKOUT (EN/UVLO) AND OVER VOLTAGE PROTECTION INPUT (OV)						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.16	1.2	1.245	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.09	1.11	1.16	V
$V_{(ENR)}$	Enable threshold voltage for low Iq shutdown, rising				1	V
$V_{(ENF)}$	Enable threshold voltage for low Iq shutdown, falling		0.3			V

6.5 Electrical Characteristics (続き)

T_J = –40 °C to +125°C. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(EN/UVLO)}$	Enable input leakage current	$V_{(EN/UVLO)}$ = 48 V			500	nA
CHARGE PUMP (BST–SRC)						
$I_{(BST\_LPM)}$	Charge Pump Supply current in LPM	$V_{(BST-SRC)}$ = 10 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(\overline{LPM})}$ = 0 V	175	360	575	µA
$I_{(BST\_AM)}$	Charge Pump Supply current in active mode	$V_{(BST-SRC)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(\overline{LPM})}$ = 2 V	300	540	775	µA
$V_{(BST\ UVLO)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, rising	$V_{(EN/UVLO)}$ = 2 V	7	7.6	8.4	V
	$V_{(BST-SRC)}$ UVLO voltage threshold, falling	$V_{(EN/UVLO)}$ = 2 V	6	6.6	7.2	V
$VCP_{(AM\_LOW)}$	Charge Pump Turn ON voltage in active mode	$V_{(EN/UVLO)}$ = 2 V, $V_{(\overline{LPM})}$ = 2 V	9.5	10.4	12.3	V
$VCP_{(AM\_HIGH)}$	Charge Pump Turnoff voltage in active mode	$V_{(EN/UVLO)}$ = 2 V, $V_{(\overline{LPM})}$ = 2 V	10.42	11.3	13	V
$VCP_{(LPM\_LOW)}$	Charge Pump Turn ON voltage in low power mode	$V_{(EN/UVLO)}$ = 2 V, $V_{(\overline{LPM})}$ = 0 V	8.3	9.3	10.6	V
$VCP_{(LPM\_HIGH)}$	Charge Pump Turnoff voltage in low power mode	$V_{(EN/UVLO)}$ = 2 V, $V_{(\overline{LPM})}$ = 0 V	9.02	10.3	11.8	V
$VCP_{(VS\_3V)}$	Charge Pump Voltage at $V_{(VS)}$ = 3 V	$V_{(EN/UVLO)}$ = 2 V	8			V
$V_{(G\_GOOD)}$	G Drive Good rising threshold w.r.t BST when bypass comparator reference changes from 2 V to 200 mV			2.3		V
$I_{(SRC)}$	SRC pin leakage current	$V_{(EN/UVLO)}$ = 2 V, $V_{(INP)}$ = 0, $V_{(\overline{LPM})}$ = 2 V		1	1.57	µA
GATE DRIVER OUTPUTS (GATE, G)						
$I_{(GATE)}$	Peak Source Current			0.5		A
$I_{(GATE)}$	Peak Sink Current			2		A
$I_{(G)}$	Gate charge (sourcing) current, on state			100		µA
$I_{(G)}$	G Peak Sink Current			390		mA
CURRENT SENSE AND CURRENT MONITOR (CS1+, CS1–, IMON, I_DIR)						
$V_{(OS\_SET)}$	Input referred offset (V_{SNS} to $V_{(IMON)}$ scaling)		-140		140	µV
$V_{(GE\_SET)}$	Gain error (V_{SNS} to $V_{(IMON)}$ scaling)		–1		1	%
$V_{(IMON\_Acc)}$	IMON accuracy	V_{SNS} = ±6 mV	–5		5	%
$V_{(IMON\_Acc)}$	IMON accuracy	V_{SNS} = ±10 mV	–5		5	%
$V_{(IMON\_Acc)}$	IMON accuracy	V_{SNS} = ±15 mV	–2		2	%
$V_{(IMON\_Acc)}$	IMON accuracy	V_{SNS} = ±30 mV	–2		2	%
OVERCURRENT (I2t) AND SHORT CIRCUIT PROTECTION (IOC, I2t, ISCP, DRN)						
$V_{(OCP)}$	OCP threshold accuracy	15 mV ≥ $V_{(OCP)}$ ≥ 100 mV	–7.5		7.5	%
$I^2_{(I2t\_Acc)}$	I^2 current accuracy on I2t pin	15 mV ≥ $V_{(OCP)}$ ≥ 100 mV V_{SNS} = $V_{(OCP)}$ + 50% of $V_{(OCP)}$	-15		15	%
$I^2_{(I2t\_Acc)}$	I^2 current accuracy on I2t pin	15 mV ≥ $V_{(OCP)}$ ≥ 100 mV V_{SNS} = $V_{(OCP)}$ + 100% of $V_{(OCP)}$	-10		10	%
$I^2_{(I2t\_Acc)}$	I^2 current accuracy on I2t pin	15 mV ≥ $V_{(OCP)}$ ≥ 100 mV V_{SNS} = $V_{(OCP)}$ + 200% of $V_{(OCP)}$	-10		10	%
$V_{(I2t\_OC)}$	I2t pin voltage threshold for overcurrent shutdown		1.93	2	2.09	V

6.5 Electrical Characteristics (続き)

T_J = –40 °C to +125°C. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(I2t\_Charge)}$	Charging current on I2t pin to $V_{(I2t\_OFFSET)}$			5100		µA
$R_{(I2t\_Discharge)}$	Internal switch discharge resistance			1200		Ω
$V_{(I2t\_OFFSET)}$	I2t pin offset voltage		490	500	415	mV
$V_{(REF\_OC)}$	IOC pin reference voltage		190	200	205	mV
$V_{(SCP)}$	SCP threshold accuracy	$V_{(SNS\_SCP)}$ = 20 mV, $R_{(ISCP)}$ = 732 Ω	19	20	21	mV
$V_{(SCP)}$	SCP threshold accuracy	$V_{(SNS\_SCP)}$ = 100 mV, $R_{(ISCP)}$ = 3.92 kΩ	95	100	105	mV
I_{SCP}	SCP Input Bias current		24.4	25	25.2	µA
LOAD WAKEUP COMPARATOR (CS2-, DRN)						
$V_{(LPM\_SCP)}$	Short-circuit threshold in LPM		1.72	2	2.17	V
$V_{(LWU)}$	Load wakeup current threshold		177	200	218	mV
AUTO-RETRY OR LATCH-OFF TIMER (TMR)						
$I_{(TMR\_SRC\_FLT)}$	TMR source current		2	2.5	3	µA
$I_{(TMR\_SNK)}$	TMR sink current		2	2.5	3	µA
$V_{(TMR\_HIGH)}$	Voltage at TMR pin for AR counter rising threshold		1.04	1.23	1.42	V
$V_{(TMR\_LOW)}$	Voltage at TMR pin for AR counter falling threshold		0.15	0.25	0.39	V
$N_{(A\text{-}R\ Count)}$				32		
TEMPERATURE MONITOR (CS1–, TMP, ITMPO)						
$V_{(REF\_TMP)}$	Temperature amplifier internal reference voltage		475	500	525	mV
$V_{(ITMPO)}$	Temperature monitor output voltage at 150°C $R_{(NTC)}$ = 10 kΩ at 25°C	$R_{(TMP)}$ = 330 Ω, $R_{(NTC)}$ = 309 Ω at 150°C, $R_{(ITMPO)}$ = 2.55 kΩ	-6		6.64	%
$V_{(ITMPO)}$	Temperature monitor output voltage at 150°C $R_{(NTC)}$ = 47 kΩ at 25°C	$R_{(TMP)}$ = 1 kΩ, $R_{(NTC)}$ = 520 Ω at 150°C, $R_{(ITMPO)}$ = 6.19 kΩ	-6		6.67	%
$I_{(TMP)}$	TMP leakage current				100	nA
$V_{(TMP\_OT)}$	Over temperature threshold		1.9	2	2.06	V
INPUT CONTROLS (INP, INP_G, $\overline{LPM}$), & FAULT FLAG ($\overline{FLT}$)						
$R_{(\overline{FLT})}$, $R_{(WAKE)}$, $R_{(I\_DIR)}$	$\overline{FLT}$, WAKE, I_DIR Pull-down resistance			70		Ω
$I_{(\overline{FLT})}$, $I_{(WAKE)}$, $I_{(I\_DIR)}$	$\overline{FLT}$, WAKE, I_DIR leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 20 V, 0 V ≤ $V_{(WAKE)}$ ≤ 20 V, 0 V ≤ $V_{(I\_DIR)}$ ≤ 20 V			400	nA
$V_{(INP\_H)}$, $V_{(\overline{LPM}\_H)}$					2	V
$V_{(INP\_L)}$, $V_{(\overline{LPM}\_L)}$			0.72			V
$V_{(INP\_Hys)}$, $V_{(\overline{LPM}\_Hys)}$	INP, $\overline{LPM}$ Hysteresis			400		mV
$I_{(INP)}$, $I_{(\overline{LPM})}$	INP, $\overline{LPM}$ leakage current				200	nA

6.6 Switching Characteristics

T_J = –40 °C to +125°C. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{GATE(INP\_H)}$	INP Turn ON propogation Delay	INP ↑ to GATE ↑, $C_{L(GATE)}$ = 47 nF		1.2	2.5	µs

6.6 Switching Characteristics (続き)

T_J = –40 ℃ to +125℃. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{GATE(INP\_L)}$	INP Turn OFF propogation Delay	INP ↓ to GATE ↓, $C_{L(GATE)}$ = 47 nF		0.35	1.5	µs
$t_{G\_ON(\overline{LPM})}$	Active mode to LPM mode transition delay	$\overline{LPM}$ ↓ to G ↑, $C_{L(G)}$ = 1 nF		1.8	9	µs
$t_{GATE\_OFF(\overline{LPM})}$	Active mode to LPM mode transition delay	$\overline{LPM}$ ↓, G ↑ (above $V_{(G\_GOOD)}$) to GATE ↓, WAKE ↑ (low to High Z), $C_{L(GATE)}$ = 47 nF		37	51	µs
$t_{GATE(WAKE\_\overline{LPM})}$	LPM Mode to Active mode transition delay with $\overline{LPM}$ trigger	$\overline{LPM}$ ↑ to GATE ↑, $C_{L(GATE)}$ = 47 nF		3.8	6	µs
$t_{G(WAKE\_\overline{LPM})}$	LPM Mode to Active mode transition delay with $\overline{LPM}$ trigger	$\overline{LPM}$ ↑, GATE ↑ (above $V_{(G\_GOOD)}$) to G ↓, WAKE ↓, $C_{L(G)}$ = 47 nF, $V_{(\overline{LPM})}$ = 0 V		9	15	µs
$t_{GATE(WAKE\_LWU)}$	GATE turn ON propagation delay during Load wakeup	$V_{(DRN–CS2-)}$ ↑ $V_{(LWU)}$ to GATE ↑, $C_{L(GATE)}$ = 47 nF, $V_{(\overline{LPM})}$ = 0 V		4	5.5	µs
$t_{G(WAKE\_LWU)}$	G turn OFF propagation delay during Load wakeup	$V_{(DRN–CS2-)}$ ↑ $V_{(LWU)}$, GATE ↑ (above $V_{(G\_GOOD)}$) to G ↓, WAKE ↓, $C_{L(G)}$ = 47 nF, $V_{(\overline{LPM})}$ = 0 V		9	15	µs
$t_{GATE(EN\_OFF)}$	EN Turn OFF Propogation Delay	EN ↓ to GATE ↓, $C_{L(GATE)}$ = 47 nF, $\overline{LPM}$ = High		3.1	4.5	µs
$t_{GATE(UVLO\_OFF)}$	UVLO Turn OFF Propogation Delay	UVLO ↓ to GATE ↓, $C_{L(GATE)}$ = 47 nF, $\overline{LPM}$ = High		4	6.5	µs
$t_{GATE(UVLO\_ON)}$	UVLO to GATE Turn ON Propogation Delay with CBT pre-biased > VPORF and INP kept high	EN/UVLO ↑ to GATE ↑, $C_{L(GATE)}$ = 47 nF, INP = 2 V, , $\overline{LPM}$ = High		8.5	25	µs
$t_{GATE(VS\_OFF)}$	GATE Turn OFF Propogation Delay with VS falling < VPORF and INP, EN/UVLO kept high	VS ↓ (cross VPORF) to GATE ↓, $C_{L(GATE)}$ = 47 nF, INP = EN/UVLO = 2V, $\overline{LPM}$ = High		25	40	µs
t_{SC}	Short Circuit Protection propogation Delay in Active Mode	$V_{(CS1+–CS1-)}$ ↑ $V_{(SCP)}$ to GATE ↓, $C_{L(GATE)}$ = 47 nF, $V_{(\overline{LPM})}$ = 2 V		3.9	5	µs
t_{LPM_SC}	Short Circuit Protection propogation Delay in LPM (Powerup into LPM with short)	$V_{(DRN–CS2-)}$ ↑ $V_{(LPM\_SCP)}$ to GATE ↑, $C_{L(GATE)}$ = 47 nF, $V_{(\overline{LPM})}$ = 0 V		3.1	4.5	µs
$t_{GATE(\overline{FLT}\_ASSERT)}$	$\overline{FLT}$ assertion delay during short circuit	$V_{(CS1+–CS1–)}$ ↑ $V_{(SCP)}$ to $\overline{FLT}$ ↓		15	21	µs
$t_{GATE(\overline{FLT}\_DE\_ASSERT)}$	$\overline{FLT}$ de-assertion delay during short circuit	$V_{(CS1+–CS1–)}$ ↓ $V_{(SCP)}$ to $\overline{FLT}$ ↑		3.8		µs
$t_{GATE(\overline{FLT}\_ASSERT\_BSTUVLO)}$	$\overline{FLT}$ assertion delay during GATE Drive UVLO	$V_{(GATE–SRC)}$ ↓ $V_{(BSTUVLOR)}$ to $\overline{FLT}$ ↓		30		µs
$t_{GATE(\overline{FLT}\_DE\_ASSERT\_BSTUVLO)}$	$\overline{FLT}$ de-assertion delay during GATE Drive UVLO	$V_{(GATE–SRC)}$ ↑ $V_{(BSTUVLOR)}$ to $\overline{FLT}$ ↑		15		µs
$t_{(IDIR\_DELAY)}$	Delay for current direction indication on I_DIR pin	$V_{(SNS)}$ ↑ or ↓ to $V_{(I\_DIR)}$ ↑ or ↓		6.5	10	µs

6.7 Typical Characteristics

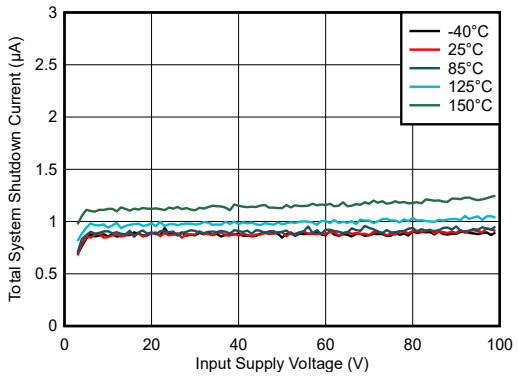


図 6-1. Shutdown Supply Current vs Supply Voltage

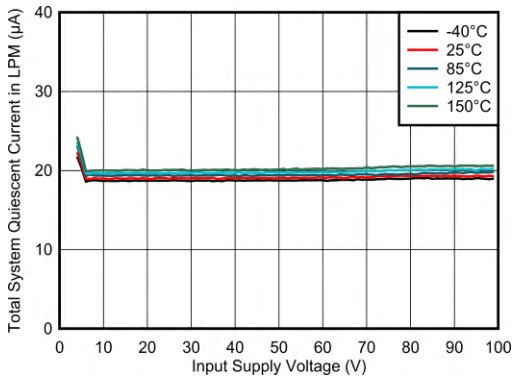


図 6-2. Operating Quiescent Current in LPM vs Supply Voltage

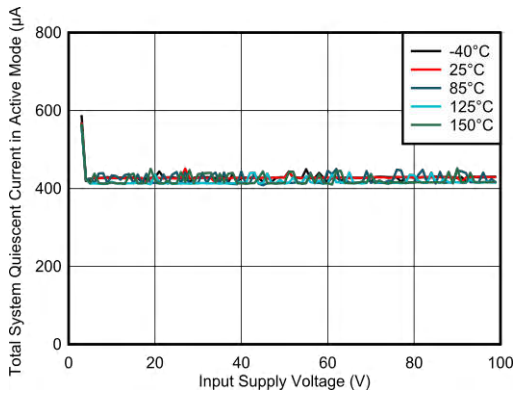


図 6-3. Operating Quiescent Current in Active Mode vs Supply Voltage

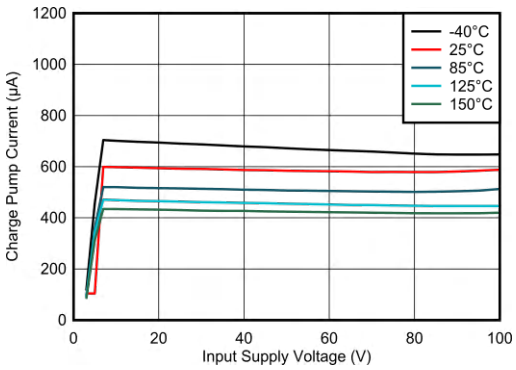


図 6-4. Charge Pump Current vs Supply Voltage

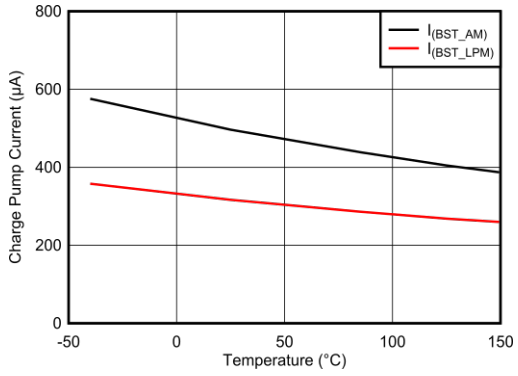


図 6-5. Charge Pump Current vs Temperature

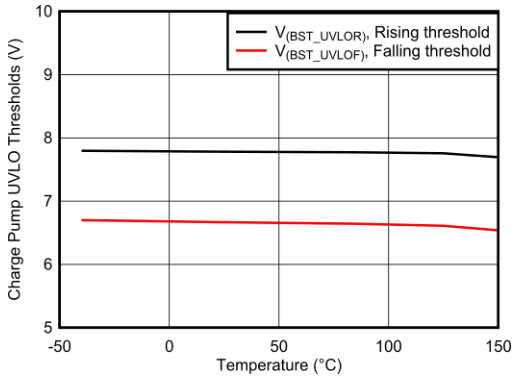
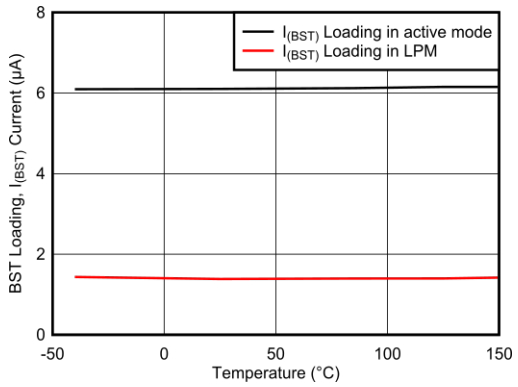


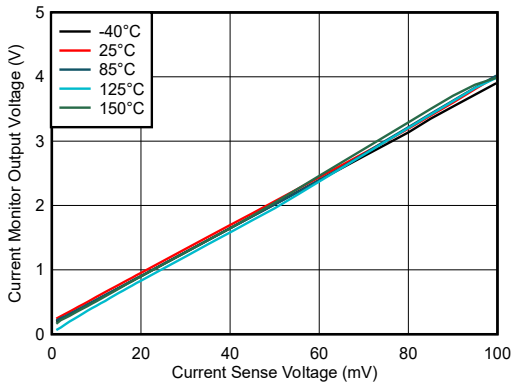
図 6-6. Charge Pump UVLO Thresholds vs Temperature

6.7 Typical Characteristics (continued)



$V_{(BST)}$ = 15V $V_{(SRC)}$ = 0V

図 6-7. BST Loading Current ($I_{(BST)}$) vs Temperature



R_{IMON} = 5.6kΩ R_{SET} = 124Ω

図 6-8. Current Monitor Voltage ($V_{(IMON)}$) vs Sense Voltage (V_{SNS})

7 Parameter Measurement Information

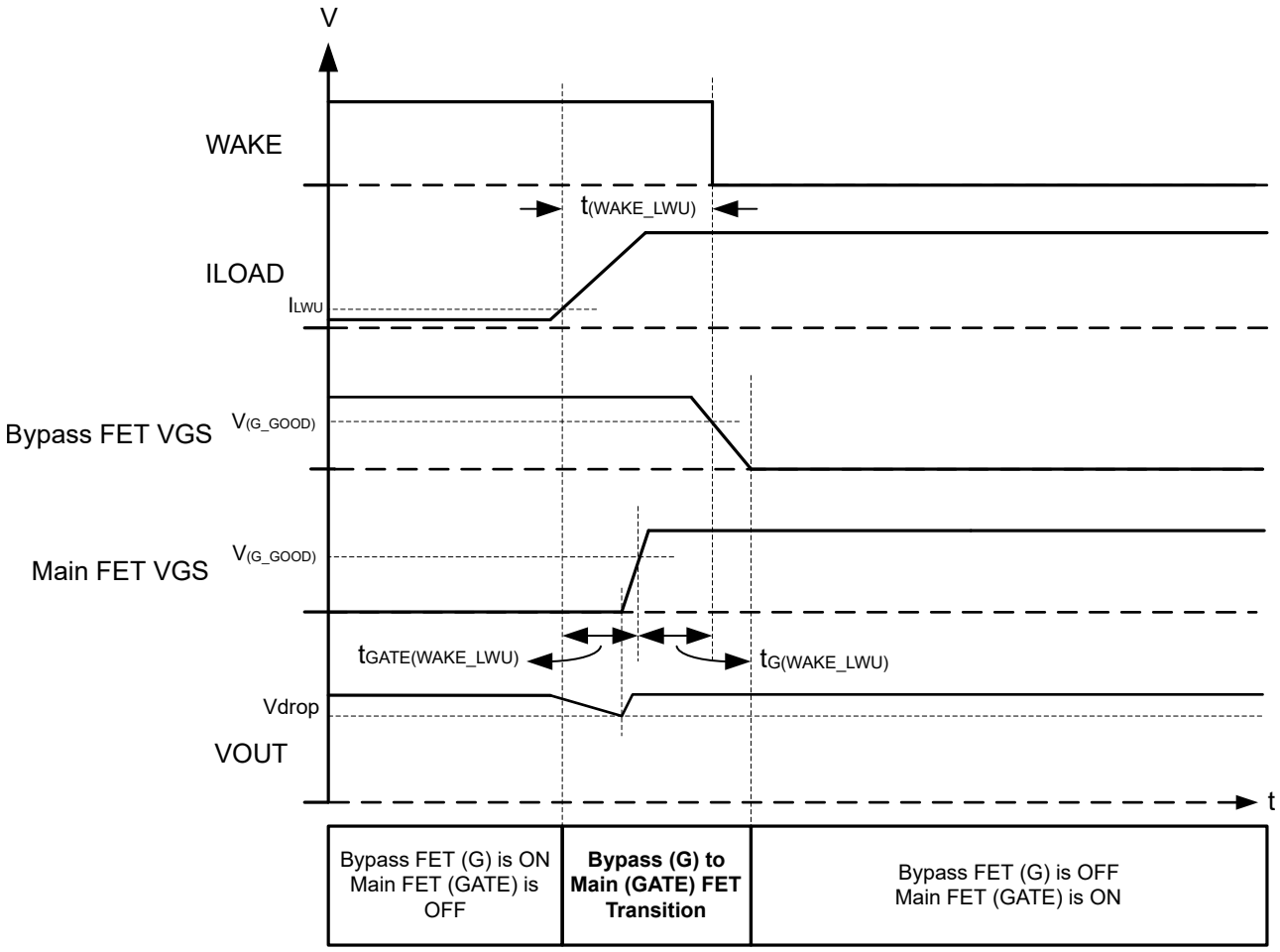


図 7-1. System Wake to Active Mode From Low Power Mode by Load Wakeup

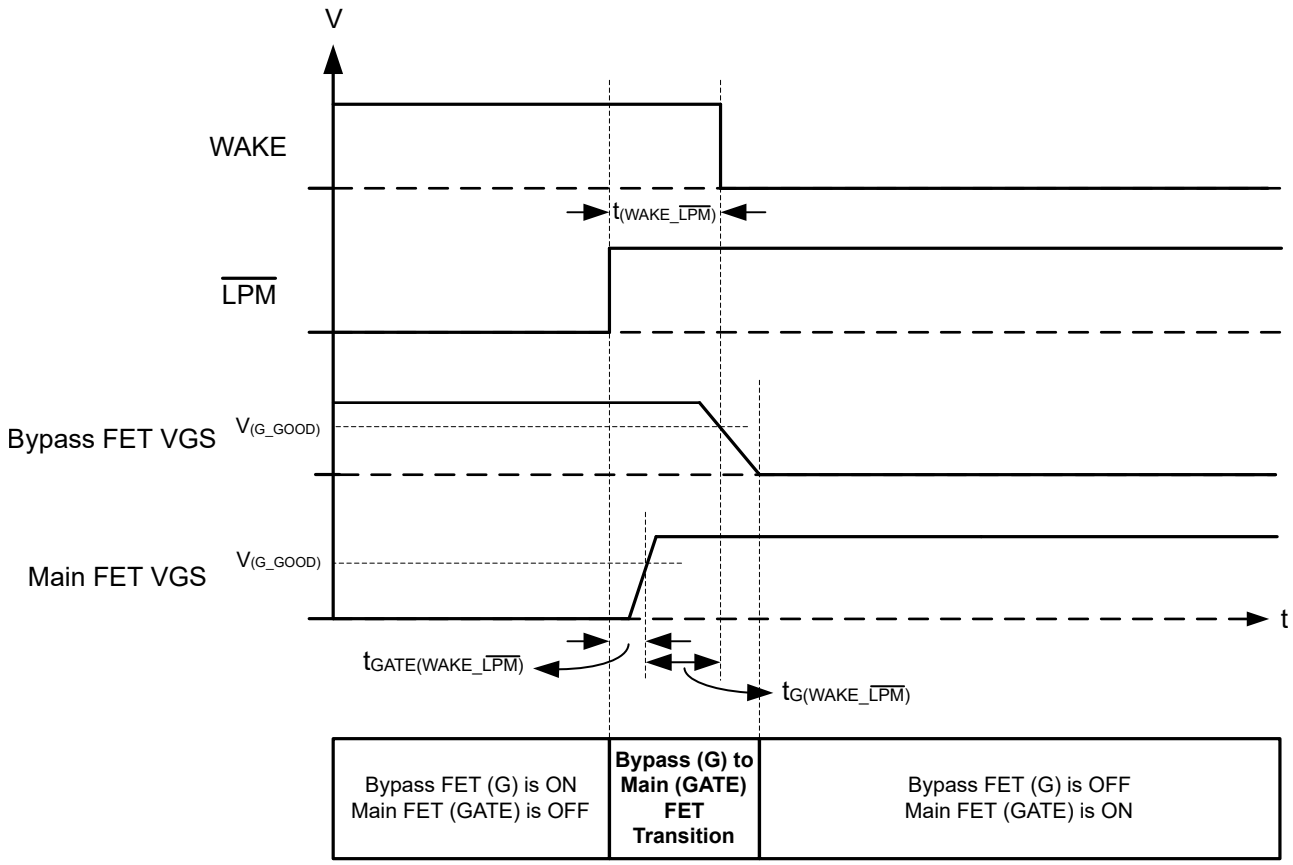


図 7-2. System Wake to Active Mode From Low Power Mode by $\overline{\text{LPM}}$ External Trigger

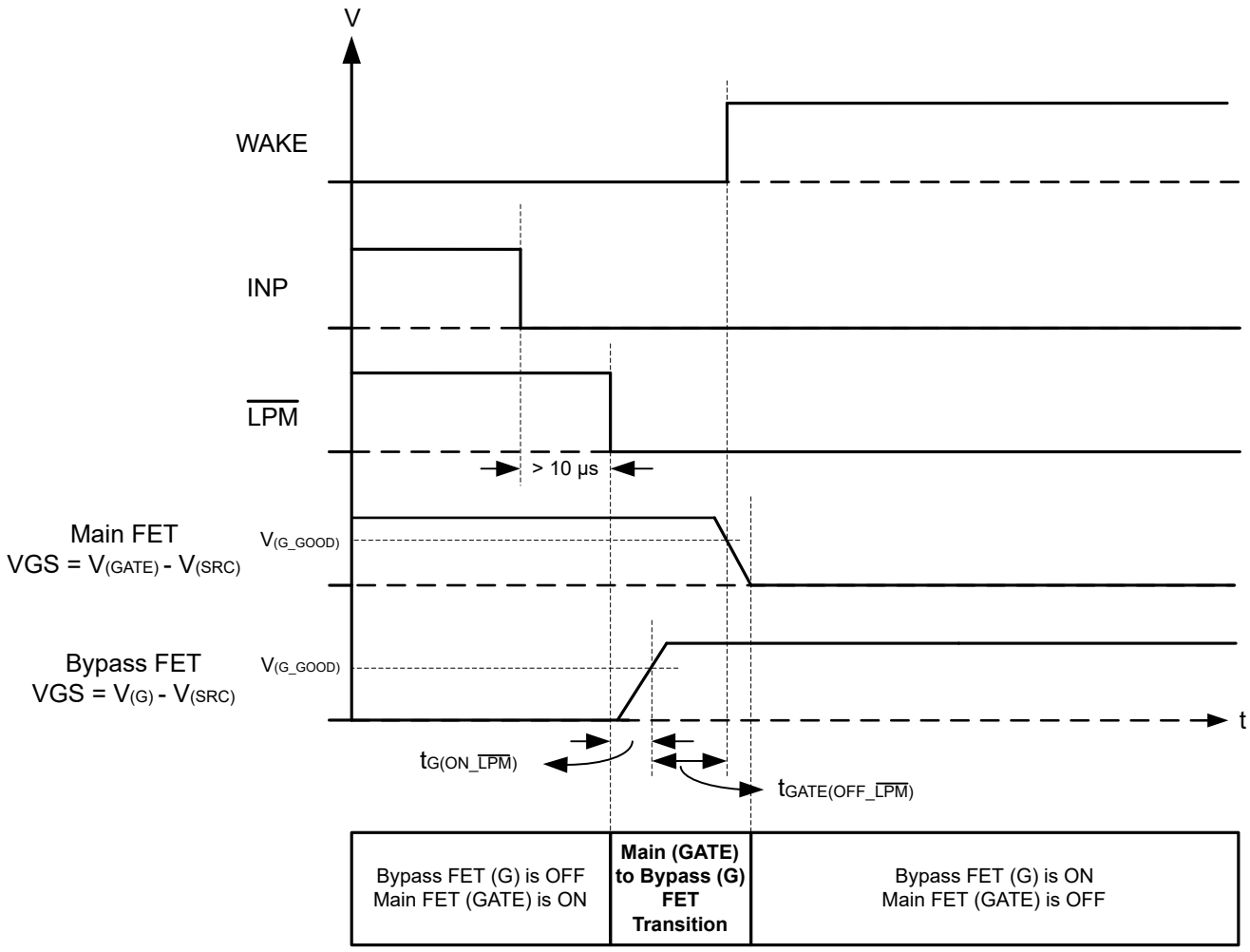


図 7-3. Active Mode to Low Power Mode by $\overline{\text{LPM}}$ Trigger

8 Detailed Description

8.1 Overview

TPS4812-Q1 is a family of low I_Q smart high side drivers with protection and diagnostics. The TPS4812-Q1 has wide operating voltage range of 3.5V to 95V and 100V absolute-maximum rating. The device is suitable for 12V, 24V, and 48V automotive system designs.

TPS4812-Q1 has two integrated gate drives with 0.5A peak source and 2A sink gate driver to drive FETs in main path and 100µA source and 0.39A sink capacity for the low power path. The strong gate drive (GATE) enables power switching using parallel FETs in high current system designs where INP pin can be used as the GATE control input.

In the low power mode with $\overline{\text{LPM}}$ = Low, the low power path FET (G drive) is kept ON and the main FETs (GATE drive) are turned OFF. The device consumes low I_Q of 20µA (typ) in this mode. Auto load wakeup threshold and output bulk capacitor charging current can be programmed using R_{BYPASS} resistor placed across DRN and CS2– pins in low power path. I_Q reduces to 1µA (typical) with EN/UVLO pulled low. The device features WAKE output pin to indicate the mode of operation (Active/Low power mode).

The device has accurate current sensing (±2% at 30mV VSNS) output (IMON) enabling systems for energy management. The device has integrated accurate and adjustable I^2t based overcurrent and short circuit protection by using an external R_{SNS} resistor. Auto-retry and latch-off fault behavior can be configured.

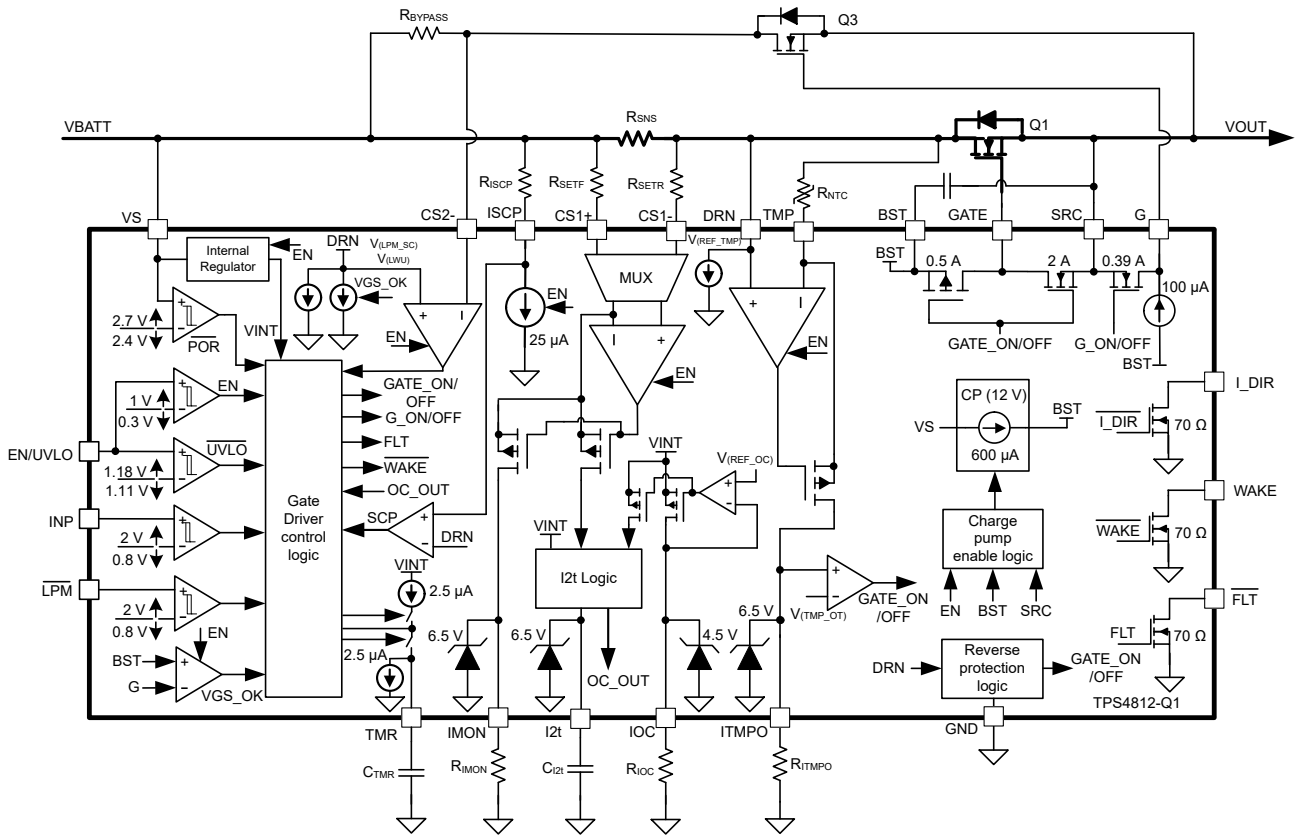
TPS4812-Q1 indicate fault on open drain $\overline{\text{FLT}}$ output during overcurrent, short circuit, charge pump under voltage and external FET overtemperature conditions.

TPS4812-Q1 has integrated reverse polarity protection down to –65V and do not need any external components to protect the ICs during an input reverse polarity fault.

The device features NTC based temperature sensing (TMP) and monitor output (ITMPO) output to sense overtemperature of external FETs enabling robust thermal system designs.

The TPS4812x-Q1 is available in a 23-pin QFN package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Charge Pump and Gate Driver Output (VS, GATE, BST, SRC)

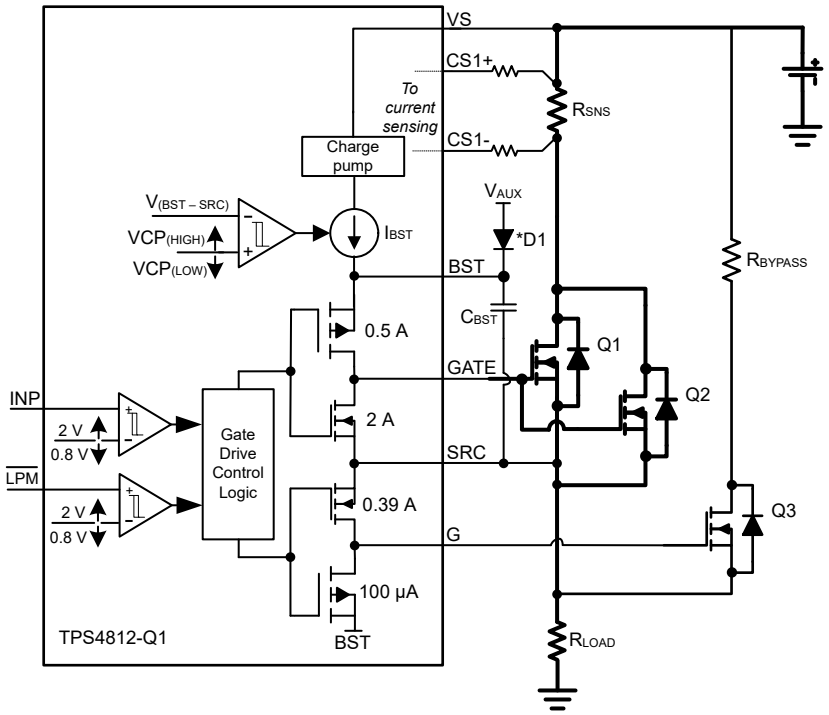


図 8-1. Gate Driver

図 8-1 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 0.5A/2A peak source/sink gate driver (GATE) for main FETs Q1, Q2, and 100µA/0.39A peak source/sink current gate driver (G) for bypass FET Q3. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 12V in active mode, 600µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, C_{BST} that is placed across the gate driver (BST and SRC).

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the C_{BST} capacitor. After the voltage across C_{BST} crosses $V_{(BST\_UVLOR)}$, the GATE driver section is activated. The device has a 1V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Choose C_{BST} based on the external FET Q_G and allowed dip during FET turn ON. In active mode, the charge pump remains enabled until the BST to SRC voltage reaches $VCP_{(HIGH\_AM)}$, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to $VCP_{(LOW\_AM)}$ typically at which point the charge pump is enabled.

The voltage between BST and SRC continue to charge and discharge between $VCP_{(HIGH\_AM)}$ and $VCP_{(LOW\_AM)}$ in active mode as shown in 図 8-2:

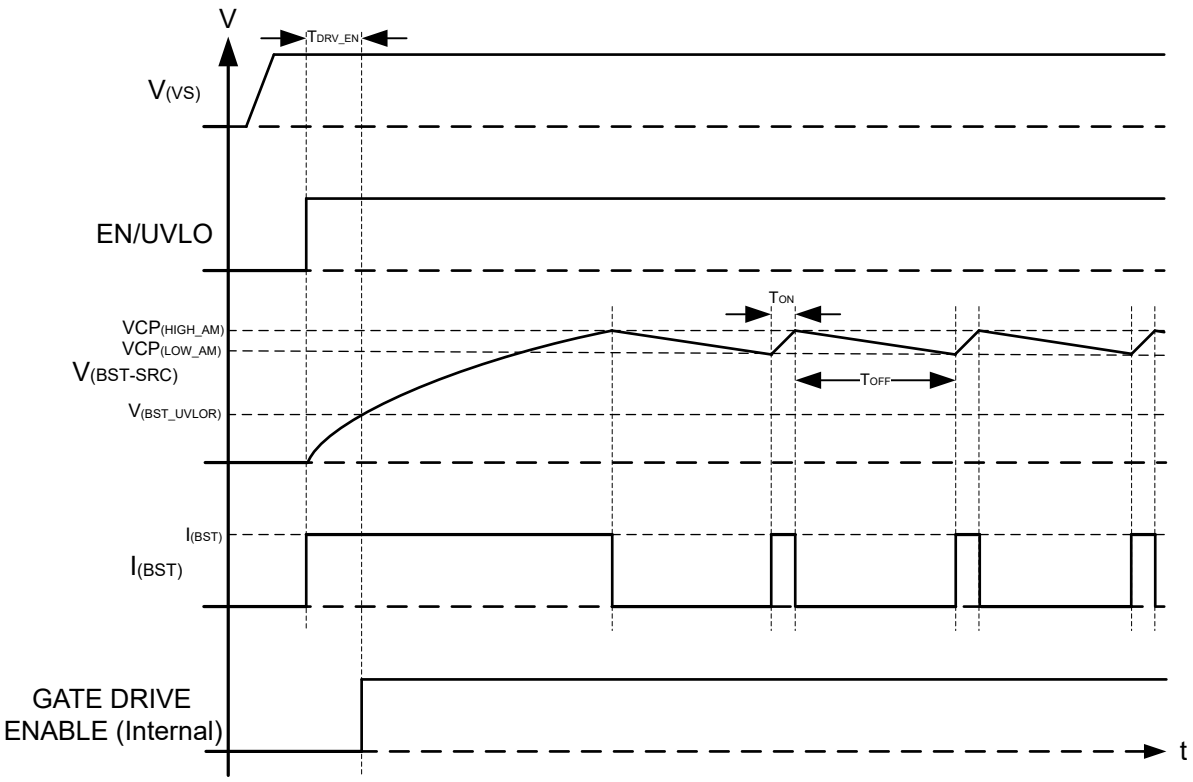


図 8-2. Charge Pump Operation

Use 式 1 to calculate the initial gate driver enable delay:

$$T_{DRV\_EN} = \frac{C_{BST} \times V_{(BST\_UVLOR)}}{600\ \mu A} \quad (1)$$

Where,

C_{BST} is the charge pump capacitance connected across BST and SRC pins.

$V_{(BST\_UVLOR)}$ = 7.6V (typ).

If T_{DRV_EN} needs to be reduced then pre-bias BST terminal externally using an external VAUX or input supply through a low leakage diode D1 as shown in 図 8-3. With this connection, T_{DRV_EN} reduces to 350µs.

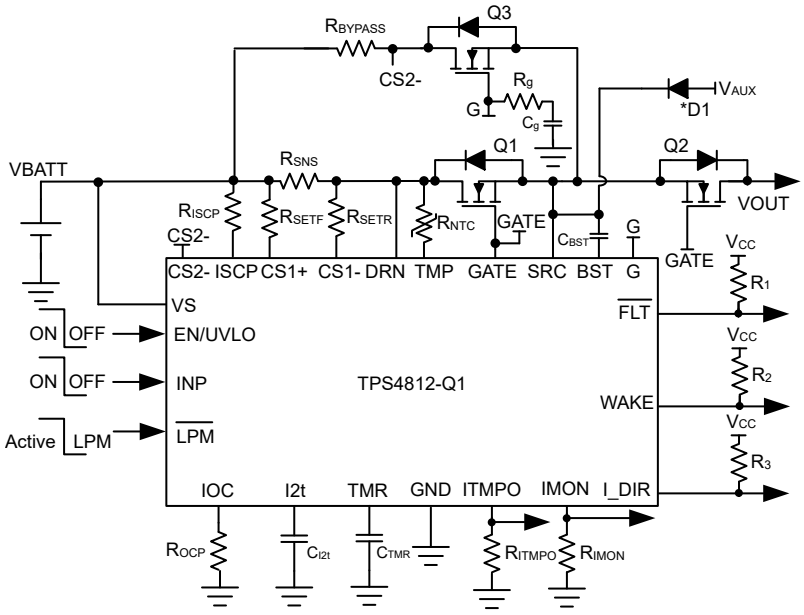


図 8-3. TPS4812-Q1 Application Circuit With External Supply to BST

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V_{AUX} can be supplied by external supply ranging between 8.1V and 15V. Input supply VS can also be connected to BST via D1 diode for reducing T_{DRV_EN}.

8.3.2 Capacitive Load Driving

Certain end equipment like automotive power distribution unit and zonal controller power different loads including other ECUs. These ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur and potentially damaging the power FETs.

To limit the inrush current during capacitive load switching, the following system design techniques can be used with TPS4812-Q1 device.

8.3.2.1 Using Low-Power Bypass FET (G Drive) for Load Capacitor Charging

In high-current applications where several FETs are connected in parallel, the gate slew rate control for the main FETs is not recommended due to unequal distribution of inrush currents among the FETs resulting in over sizing of the FETs.

The TPS4812-Q1 integrates gate driver (G) with a dedicated control input ($\overline{LPM}$) and bypass comparator between DRN and CS2– pins. This feature can be used to drive a separate low power bypass FET and pre-charge the capacitive load with inrush current limiting. 図 8-4 shows the low power bypass FET implementation for capacitive load charging using TPS4812-Q1. An external capacitor C_g reduces the gate turn ON slew rate and controls the inrush current.

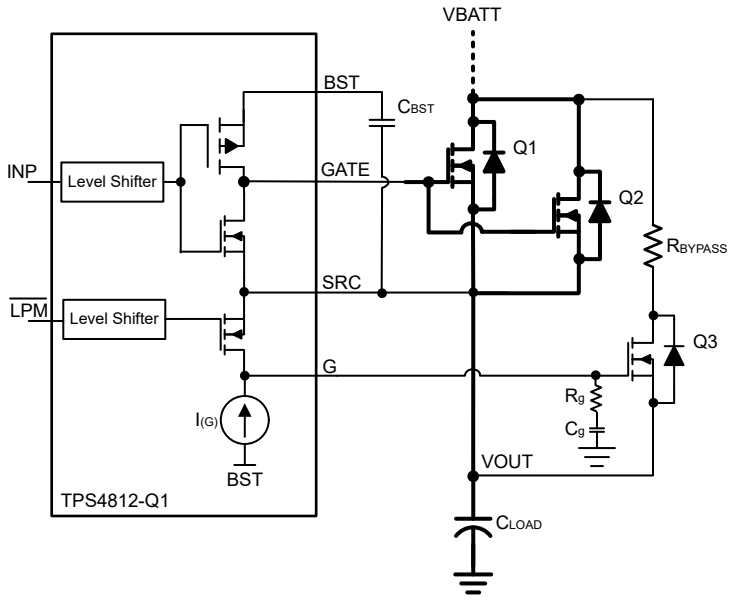


図 8-4. Capacitor Charging Using Gate (G) Slew Rate Control of Low-Power Bypass FET

During power-up with EN/UVLO pulled high and $\overline{\text{LPM}}$ pulled low, the device turns ON bypass FET (G) by pulling G high with 100µA of source current and the main FETs (GATE) is kept OFF. In this low power mode (LPM), TPS4812-Q1 senses voltage between DRN and CS2– pins along with VGS of bypass FET (G to SRC). The voltage across DRN and CS2– is compared initially with $V_{(LPM\_SCP)}$ threshold (2V typical) to detect powerup into short fault event until $V_{(G\_GOOD)}$ threshold is reached.

After $V_{(G\_GOOD)}$ threshold is reached, the voltage between DRN and CS2– is compared against $V_{(LWU)}$ threshold (200mV typ) for load wakeup event. With this scheme capacitor charging current (I_{INRUSH}) can be set at higher than load wakeup threshold (I_{LWU}) and power-up into short event can also be detected reliably as shown in 図 8-5.

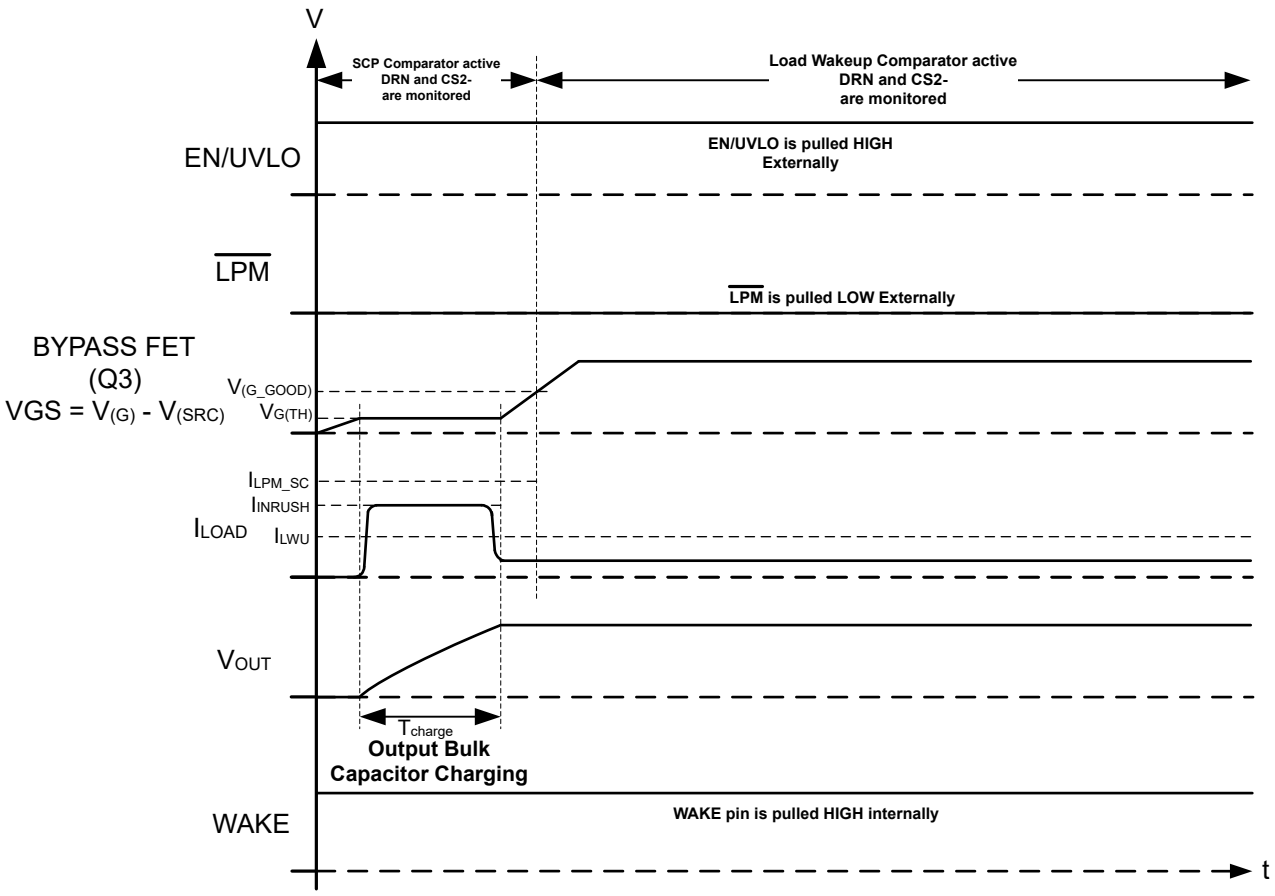


図 8-5. Timing Diagram for Bulk Capacitor Charging Using Bypass Path

Setting the Load Wakeup Trigger Threshold:

During normal operation, the series resistor R_{BYPASS} is used to set load wakeup current threshold. After $V_{(G\_GOOD)}$ threshold is reached, the voltage between DRN and CS2– is compared against $V_{(LWU)}$ threshold (200mV typ) for load wakeup event.

RBYPASS can be selected using 式 2:

$$R_{BYPASS} = \frac{V_{(LWU)}}{I_{LWU}} \quad (2)$$

Setting the INRUSH Current:

Use 式 3 to calculate the I_{INRUSH}:

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \quad (3)$$

Where,

C_{LOAD} is the load capacitance.

V_{BATT} is the input voltage and T_{charge} is the charge time.

I_{INRUSH} should be always less than wakeup in short in low power mode (I_{LPM_SC}) current which can be calculated using 式 4:

$$I_{LPM\_SC} = \frac{V_{(LPM\_SCP)}}{R_{BYPASS}} \quad (4)$$

Use 式 5 to calculate the required C_g value.

$$C_g = \frac{C_{LOAD} \times I_{(G)}}{I_{INRUSH}} \quad (5)$$

Where,

$I_{(G)}$ is 100µA (typical),

A series resistor R_g must be used in conjunction with C_g to limit the discharge current from C_g during turn-off. The recommended value for Rg is between 220Ω to 470Ω.

After the output capacitor is charged, main FETs can be controlled (GATE drive) and bypass FET (G drive) can be turned OFF by driving $\overline{LPM}$ high externally. The main FETs (G drive) can now be turned ON by driving INP high.

図 8-6 shows application circuit to charge large output capacitors using low power bypass path in high current applications.

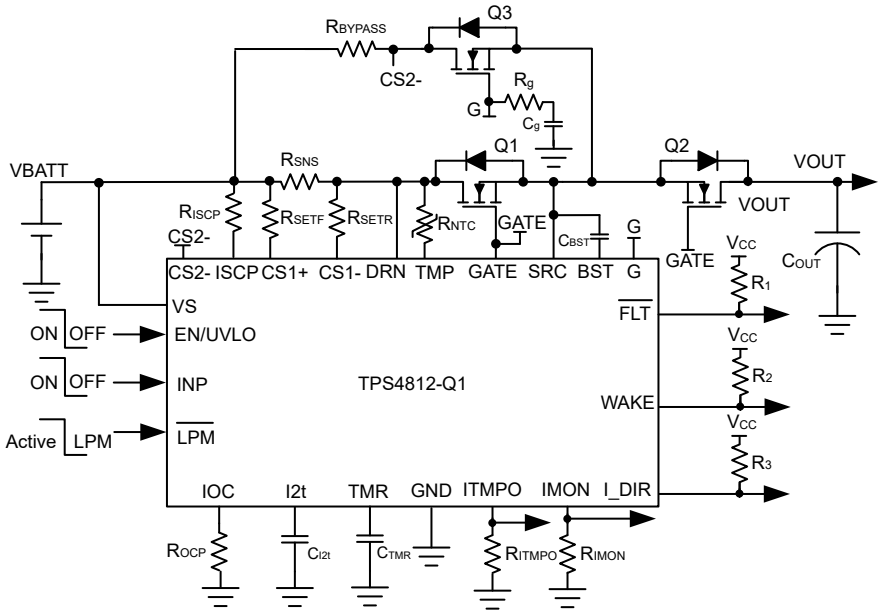


図 8-6. TPS4812-Q1 Application Circuit for Capacitive Load Driving Using Low-Power Bypass FET (Q_3) and Series Resistor (R_{BYPASS})

8.3.2.2 Using Main FET (GATE Drive) Gate Slew Rate Control

In the applications where low power bypass path is not used, the cap charging can be done using main FET GATE drive control.

For limiting inrush current during turn-ON of the main FET with capacitive loads, use R_1, R_2, C_1, and D_2 as shown in 図 8-7. The R_1 and C_1 components slow down the voltage ramp rate at the gate of main FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

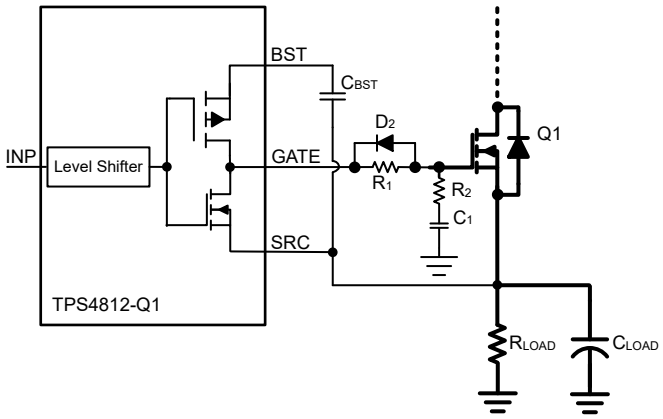


図 8-7. Inrush Current Limiting in Main Path

Use the 式 6 to calculate the inrush current during turn-ON of the FET.

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \quad (6)$$

$$C_1 = \frac{0.63 \times V_{(BST\ -\ SRC)} \times C_{LOAD}}{R_1 \times I_{INRUSH}} \quad (7)$$

Where,

C_{LOAD} is the load capacitance.

VBATT is the input voltage and T_{charge} is the charge time.

$V_{(BST\text{-}SRC)}$ is the charge pump voltage (12V).

Use a damping resistor R_2 (~10Ω) in series with C_1. 式 8 can be used to compute required C_1 value for a target inrush current. A 100kΩ resistor for R_1 can be a good starting point for calculations.

D_2 ensures fast turn OFF of GATE drive by bypassing R_1.

C_1 results in an additional loading on C_{BST} to charge during turn-ON. Use 式 8 to calculate the required C_{BST} value:

$$C_{BST} = \frac{Q_{g(total)}}{\Delta V_{BST}} + 10 \times C_1 \quad (8)$$

Where,

$Q_{g(total)}$ is the total gate charge of the FET.

ΔV_{BST} (1V typical) is the ripple voltage across BST to SRC pins.

8.3.3 Overcurrent and Short-Circuit Protection

TPS4812-Q1 features integrated accurate I^2t functionality for the implementation of a robust and flexible overcurrent protection mechanism. This I^2t functionality features an intelligent circuit breaking aimed at protecting PCB traces, connectors and wire harness from overheating, with no impact on load transients like inrush currents and bulk capacitor charging.

The device also features accurate and configurable short-circuit protection threshold (I_{SC}) with fixed response time (t_{SC} = 5us max).

図 8-8 shows the overall current-time characteristics.

- Configurable I^2t based overcurrent protection (I_{OC}) threshold and adjustable response time (t_{OC} and t_{OC_MIN})
- Adjustable short-circuit threshold (I_{SC}) with internally fixed fast response (t_{SC})

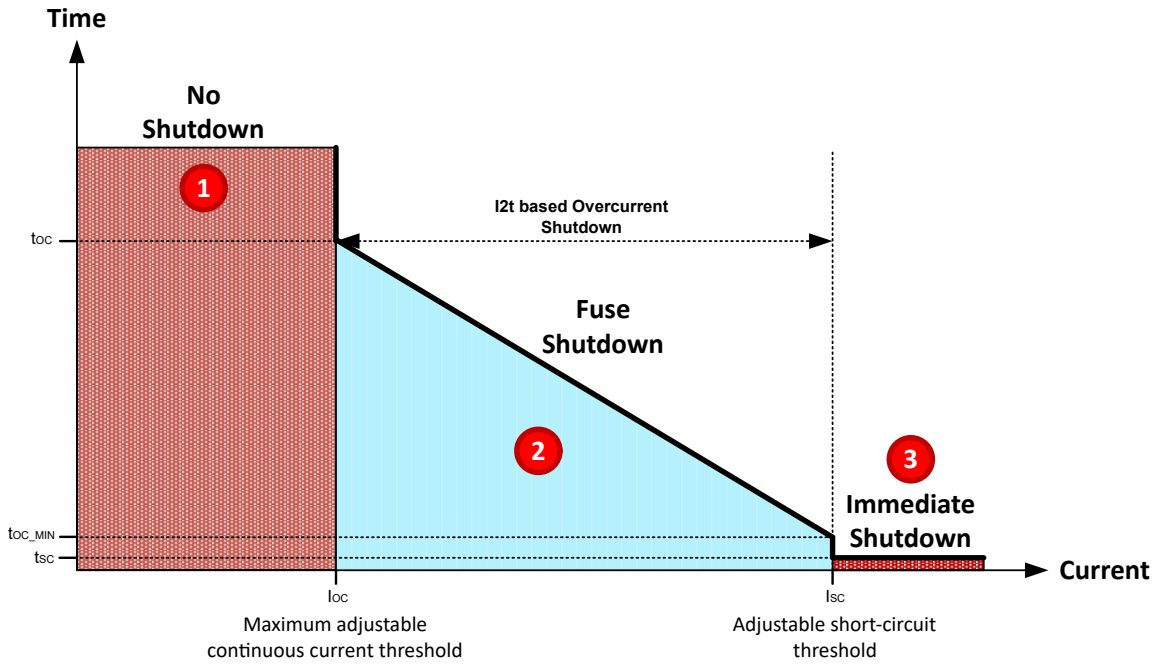


図 8-8. Configurable Current vs Time characteristics curve for TPS4812-Q1

8.3.3.1 I^2t-Based Overcurrent Protection

The I^2t profile for TPS4812-Q1 is set by two parameters which are I^2t start overcurrent threshold, I_{OC} and I^2t ampere squared second factor (melting point or breaking point). The overcurrent protection time t_{OC} is determined based on set I^2t factor when load current is higher than set I_{OC} threshold.

Setting I^2t Protection Starting Threshold, R_{IOC}

The I^2t protection starting threshold I_{OC} is set using an external resistor R_{IOC} across IOC and GND pins.

Use 式 9 to calculate the required R_{IOC} value:

$$R_{IOC}\left(\Omega\right) = \frac{V_{(REF\_OC)}}{K \times \left(I_{OC}\right)^2} \tag{9}$$

Where,

$V_{(REF\_OC)}$ is internal reference voltage of 200mV.

I_{OC} is the overcurrent level.

The scaling factor, K can be calculated by 式 10:

$$\text{Scaling factor}\left(K\right) = \frac{\left(0.1 \times \frac{R_{SNS}}{R_{SET}}\right)^2}{I_{BIAS}} \tag{10}$$

Where,

I_{BIAS} is internal reference current of 5µA.

R_{SET} is the resistor connected across CS1+ and input battery supply.

R_{SNS} is the current sense resistor.

Setting I^2t Profile, C_{I2t}

The device senses the voltage across the external current sense resistor (R_{SNS}) through CS1+ and CS1–. When sensed voltage across R_{SNS} exceeds I_{OC} threshold set by R_{IOC} resistor, C_{I2t} capacitor starts charging with current proportional to $I_{LOAD}{}^2 – I_{OC}{}^2$ current.

The time to turn OFF the gate drive at maximum overcurrent limit (I_{OC_MAX}) can be determined using 式 11:

$$t_{OC\_MIN}\left(s\right) = \frac{\text{I2T factor}}{I_{OC\_MAX} \times I_{OC\_MAX}} \tag{11}$$

注

The maximum overcurrent limit (I_{OC_MAX}) can 5% to 10% below short-circuit protection threshold (I_{SC}).

Use 式 12 to calculate the required C_{I2t} value.

$$C_{I2t}\left(F\right) = \frac{K \times t_{OC\_MIN}}{V_{(I2t\_OC)} - V_{(I2t\_OFFSET)}} \times \left[I_{OC\_MAX}{}^2 - I_{OC}{}^2\right] \tag{12}$$

Where,

$V_{(I2t\_OC)}$ is I^2t trip threshold voltage of 2V (typ).

$V_{(I2t\_OFFSET)}$ is offset voltage of 500mV (typ) on I2t pin during normal operation.

t_{OC_MIN} is the desired overcurrent response time at maximum overcurrent threshold I_{OC_MAX}.

8.3.3.1.1 I^2t-Based Overcurrent Protection With Auto-Retry

The C_{I2t} programs the over current protection delay (t_{OC_MIN}) and C_{TMR} programs auto-retry time (t_{RETRY}). Once the voltage across CS1+ and CS1– exceeds the set point ($V_{(OCP)}$), the C_{I2t} capacitor starts charging with current proportional to $I_{LOAD}^{\ 2} – I_{OC}^{\ 2}$ current.

After C_{I2t} charges to $V_{(I2t\_OC)}$, GATE pulls low to SRC turning OFF the main FET and $\overline{FLT}$ assets low as same time. Post this event, the auto-retry behavior starts. The C_{TMR} starts charging with 2.5µA pullup current till voltage reaches $V_{(TMR\_HIGH)}$ level. After this level, capacitor starts discharging with 2.5µA pulldown current.

After the voltage reaches $V_{(TMR\_LOW)}$ level, the capacitor starts charging again with 2.5µA pullup. After 32 charging-discharging cycles of C_{TMR} the FET turns ON back and $\overline{FLT}$ de-asserts after de-assertion delay.

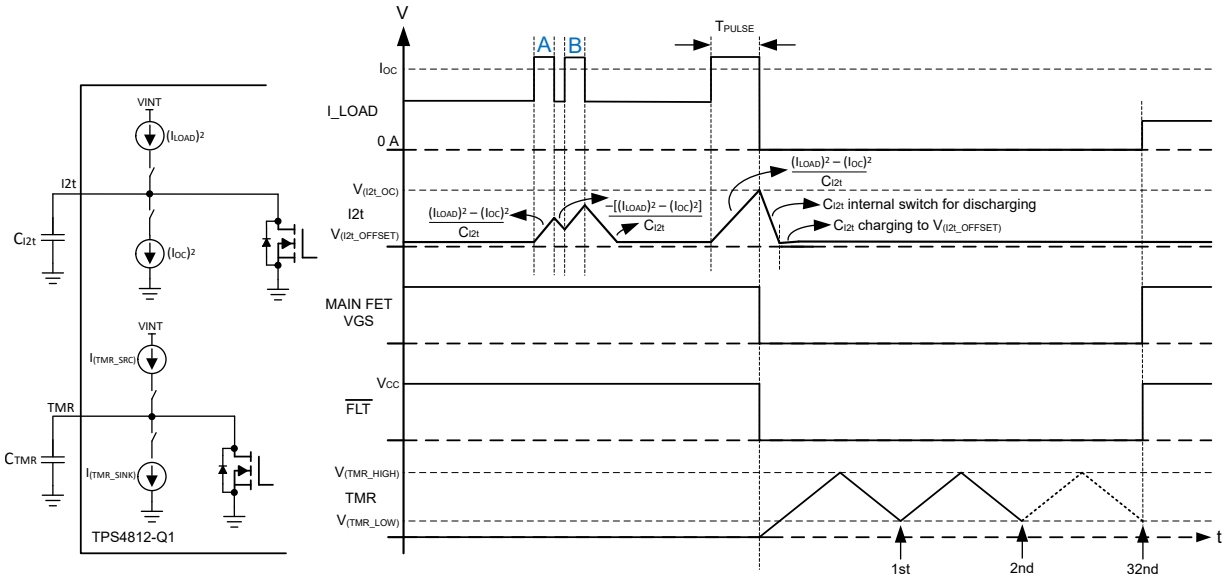


図 8-9. I^2t-Based Overcurrent Protection With Auto-Retry

The auto-retry time can be set by CTMR capacitor to be connected across TMR and GND pins as per 式 13.

$$t_{RETRY}\left(s\right) = 64 \times C_{TMR} \times \left[\frac{V_{(TMR\_HIGH)} - V_{(TMR\_LOW)}}{I_{(TMR\_SRC)}}\right] \quad (13)$$

where

$V_{(TMR\_HIGH)}$ is 1.2V (typ) and $V_{(TMR\_LOW)}$ is 0.2V (typ).

$I_{(TMR\_SRC)}$ is internal source current on TMR pin with 2.5µA (typ) value.

8.3.3.1.2 I^2t-Based Overcurrent Protection With Latch-Off

Connect 100kΩ resistor across TMR pin to GND for latch-off configuration.

Latch is reset on falling edge of INP or $\overline{LPM}$ going low or EN/UVLO (below $V_{(ENF)}$) or power cycle VS below $V_{(VS\_PORF)}$. At low edge, the timer counter is reset and C_{TMR} is discharged. GATE pulls up to BST when INP is pulled high.

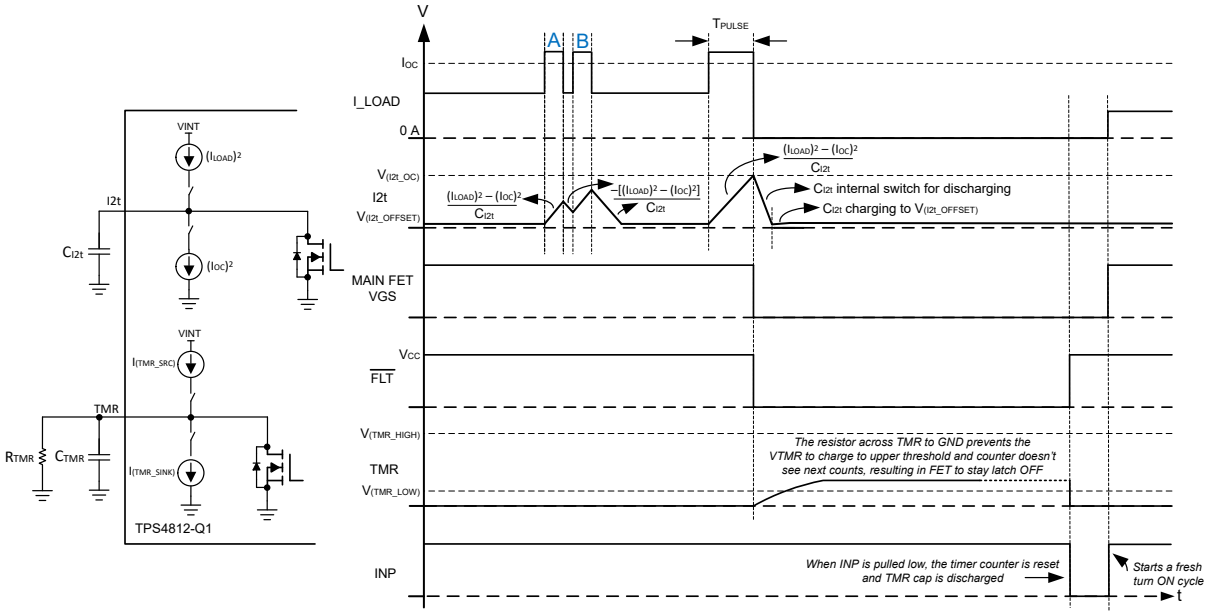


図 8-10. I^2t-Based Overcurrent Protection With Latch-Off

8.3.3.2 Short-Circuit Protection

The short-circuit current threshold (I_{SC}) can be set R_{ISCP} resistor. Use 式 14 to calculate the required R_{ISCP} value.

$$R_{ISCP}\left(k\Omega\right) = \frac{I_{SC} \times R_{SNS} - 1.8}{I_{SCP}} \tag{14}$$

where

I_{SC} is the short-circuit current threshold in Ampere.

R_{SNS} is external current sense resistor in miliohms.

I_{SCP} is the internal reference current of 25µA.

When the load current exceeds the I_{SC} threshold then, GATE pulls low to SRC within 5µs (max) in TPS4812-Q1, protecting the main path FETs and $\overline{FLT}$ asserts low at the same time. Subsequent to this event, the charge and discharge cycles of C_{TMR} starts similar to the behavior post FET OFF event in the overcurrent protection scheme.

Latch-off can also achieved in the similar way as explained in the overcurrent protection scheme.

8.3.4 Analog Current Monitor Output (IMON)

TPS4812-Q1 features an accurate analog load current monitor output (IMON) with adjustable gain (ON in active mode and load wakeup only). The current source at IMON terminal is configured to be proportional to the current

flowing through the R_{SNS} current sense resistor. This current can be converted to a voltage using a resistor R_{IMON} from IMON terminal to GND pins.

This voltage, computed using following equation, can be used as a means of monitoring current flow through the system.

Use 式 15 to calculate the $V_{(IMON)}$ for TPS48120-Q1 variant with I^2t enabled.

$$V_{(IMON)} = \left(V_{SNS} + V_{(VOS\_SET)}\right) \times \frac{0.9 \times R_{IMON}}{R_{SET}} \quad (15)$$

Use 式 16 to calculate the $V_{(IMON)}$ for TPS48121-Q1 variant with I^2t disabled.

$$V_{(IMON)} = \left(V_{SNS} + V_{(VOS\_SET)}\right) \times \frac{R_{IMON}}{R_{SET}} \quad (16)$$

Where,

$V_{SNS} = I_{LOAD} \times R_{SNS}$,

$V_{(OS\_SET)}$ is the input referred offset (±140µV) of the current sense amplifier (V_{SNS} to $V_{(IMON)}$ scaling),

0.9 is the current mirror factor between the current sense amplifier and the IMON pass FET.

The maximum voltage range for monitoring the current ($V_{(IMONmax)}$) is limited to minimum([$V_{(VS)}$ – 0.5V], 5.5V)

to ensure linear output. This puts limitation on maximum value of R_{IMON} resistor. The IMON pin has an internal clamp of 6.5V (typical).

Accuracy of the current mirror factor is <±1%. Use the following equation to calculate the overall accuracy of $V_{(IMON)}$.

$$\%\, V_{(IMON)} = \frac{V_{(OS\_SET)}}{V_{SNS}} \times 100 \quad (17)$$

TPS4812-Q1 features bi-directional current sensing (across CS1+ and CS1–) and monitoring using IMON output to get magnitude of scaled voltage across R_{SNS} (V_{SNS}) and open drain I_DIR output pin indicating direction of current.

I_DIR output is pulled high if current is flowing in forward direction whereas I_DIR is pulled low for reverse current as shown in below figure.

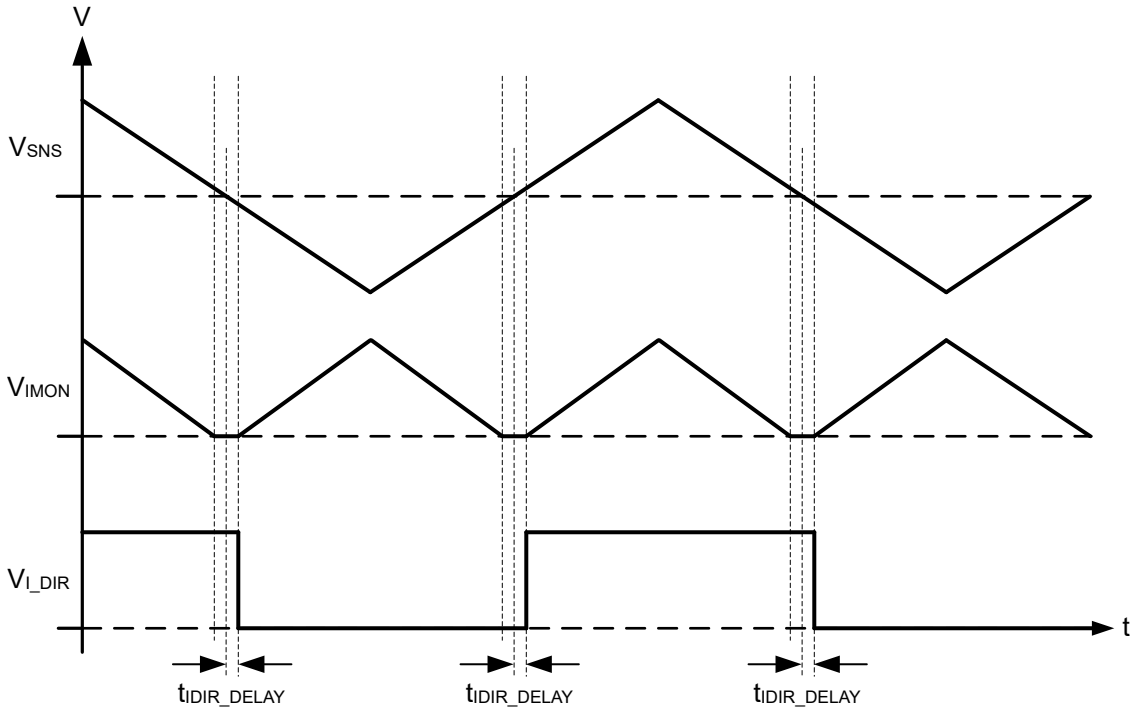


図 8-11. TPS4812-Q1 Bi-directional Current Monitoring Timing Diagram

8.3.5 NTC-Based Temperature Sensing (TMP) and Analog Monitor Output (ITMPO)

TPS4812-Q1 features an integrated temperature monitoring amplifier (ON in active mode and load wakeup only). This temperature monitoring function is implemented with a differential amplifier with input pin as TMP and output pin as ITMPO.

The analog output voltage, V_{ITMPO} represents the temperature sensed by R_{NTC}which can be directly read on pin ITMPO (Temperature monitoring output) by microcontroller.

V_{ITMPO} can be calculated based on following equation:

$$V_{ITMPO} = \left(V_{REF\_TMP} + V_{TMP\_OFFSET}\right) \times \frac{R_{ITMPO}}{\left(R_{NTC} + R_{TMP}\right)} \quad (18)$$

where,

V_{REF_TMP} is 500mV (typical)

V_{TMP_OFFSET} is ±5mV

R_{TMP} is 330Ω for 10k NTC at 25°C

R_{TMP} is 1kΩ for 47k NTC at 25°C

TPS4812-Q1 has integrated comparator on ITMPO pin to detect external main FET overtemperature fault. When voltage on ITMPO exceeds above $V_{(TMP\_OT)}$ (2V typ) threshold then main FET (GATE) turns off, device goes into latch-off and $\overline{FLT}$ asserts low. Latch is reset on falling edge of INP or $\overline{LPM}$ going low or EN/UVLO (below $V_{(ENF)}$) or power cycle VS below $V_{(VS\_PORF)}$.

External FET overtemperature threshold can be programmed based on following equation:

$$V_{(TMP\_OT)} = \left(V_{REF\_TMP} + V_{TMP\_OFFSET}\right) \times \frac{R_{ITMPO} + R_{INT}}{\left(R_{NTC} + R_{TMP}\right)} \quad (19)$$

Where,

R_{ITMPO} is resistor in ohm on ITMPO pin.

$V_{(TMP\_OT)}$ is fixed external FET overtemperature threshold of 2V (typical).

R_{INT} is internal resistor with 200Ω (typical) and 90/340Ω min/max value.

R_{NTC} is the NTC thermistor resistance which varies with the temperature and R_{TMP} is a normal resistor used to linearize the thermistor behavior with respect to temperature, shown in 図 8-12:

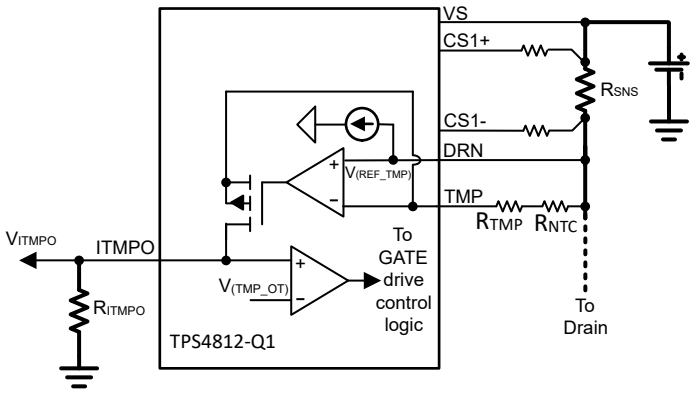


図 8-12. NTC-Based Temperature Sensing and Monitoring Output

8.3.6 Fault Indication and Diagnosis ($\overline{FLT}$)

The TPS4812-Q1 feature integrated charge pump UVLO feature. The voltage across BST-SRC is internally monitored. If the voltage is < $V_{(BST\_UVLO)}$ then $\overline{FLT}$ is asserted low. Both the GATE and G gate drives also get disabled in this condition turning OFF main and bypass FETs. $\overline{FLT}$ gets de-asserted and gate drivers get enabled when BST to SRC voltage rises above $V_{(BST\_UVLO)}$.

$\overline{FLT}$ assets low in TPS4812-Q1 when short-circuit or I2t based overcurrent or charge pump UVLO or NTC based external FET overtemperature is detected.

8.3.7 Reverse Polarity Protection

The TPS4812-Q1 devices features integrated reverse polarity protection to protect the device from failing during input and output reverse polarity faults. Reverse polarity faults occur during installation and maintenance of the end equipment. The device is tolerant to reverse polarity voltages down to –65V both on input and on the output.

On the output side, the device can see transient negative voltages during regular operation due to output cable harness inductance kickbacks when the switches are turned OFF. In such systems the output negative voltage level is limited by the output side TVS or a diode.

8.3.8 Undervoltage Protection (UVLO)

TPS4812-Q1 features an accurate undervoltage protection (< ±2 %) using EN/UVLO pin. When EN/UVLO pin voltage goes below 1.12V(typ), then GATE and G goes low.

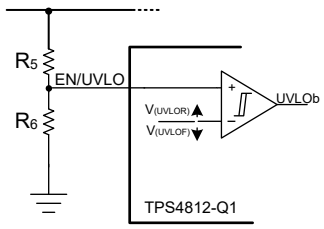


図 8-13. Programming Undervoltage Protection Threshold

8.4 Device Functional Modes

8.4.1 State Diagram

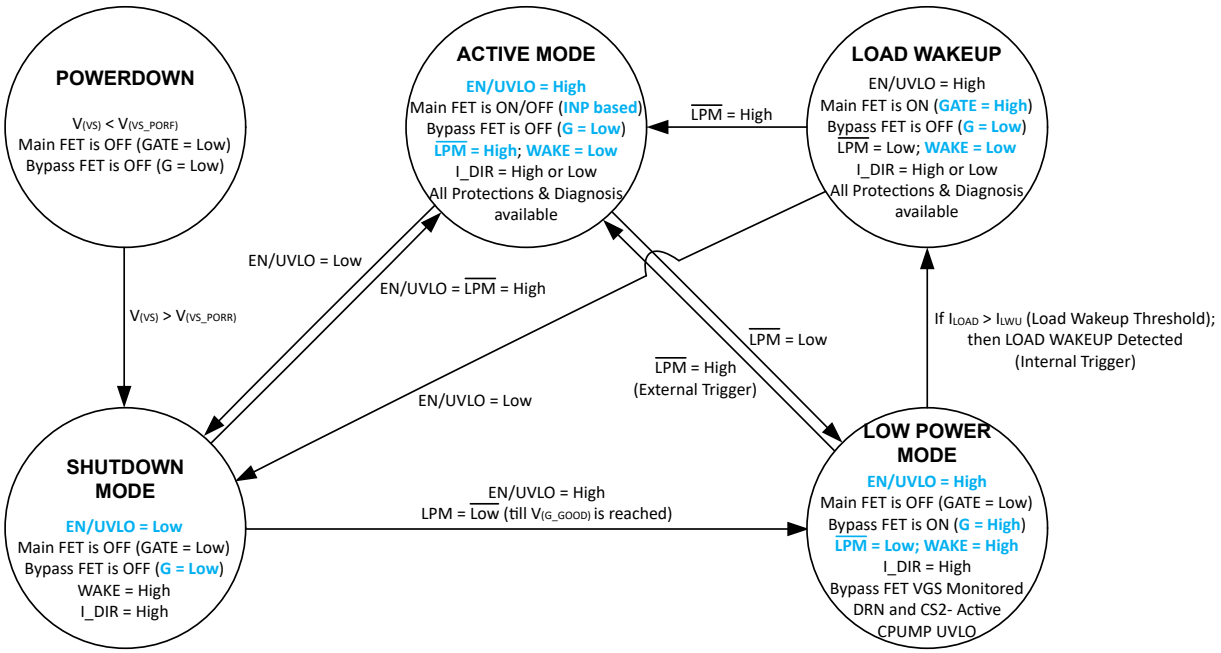


図 8-14. State Diagram

8.4.2 State Transition Timing Diagram

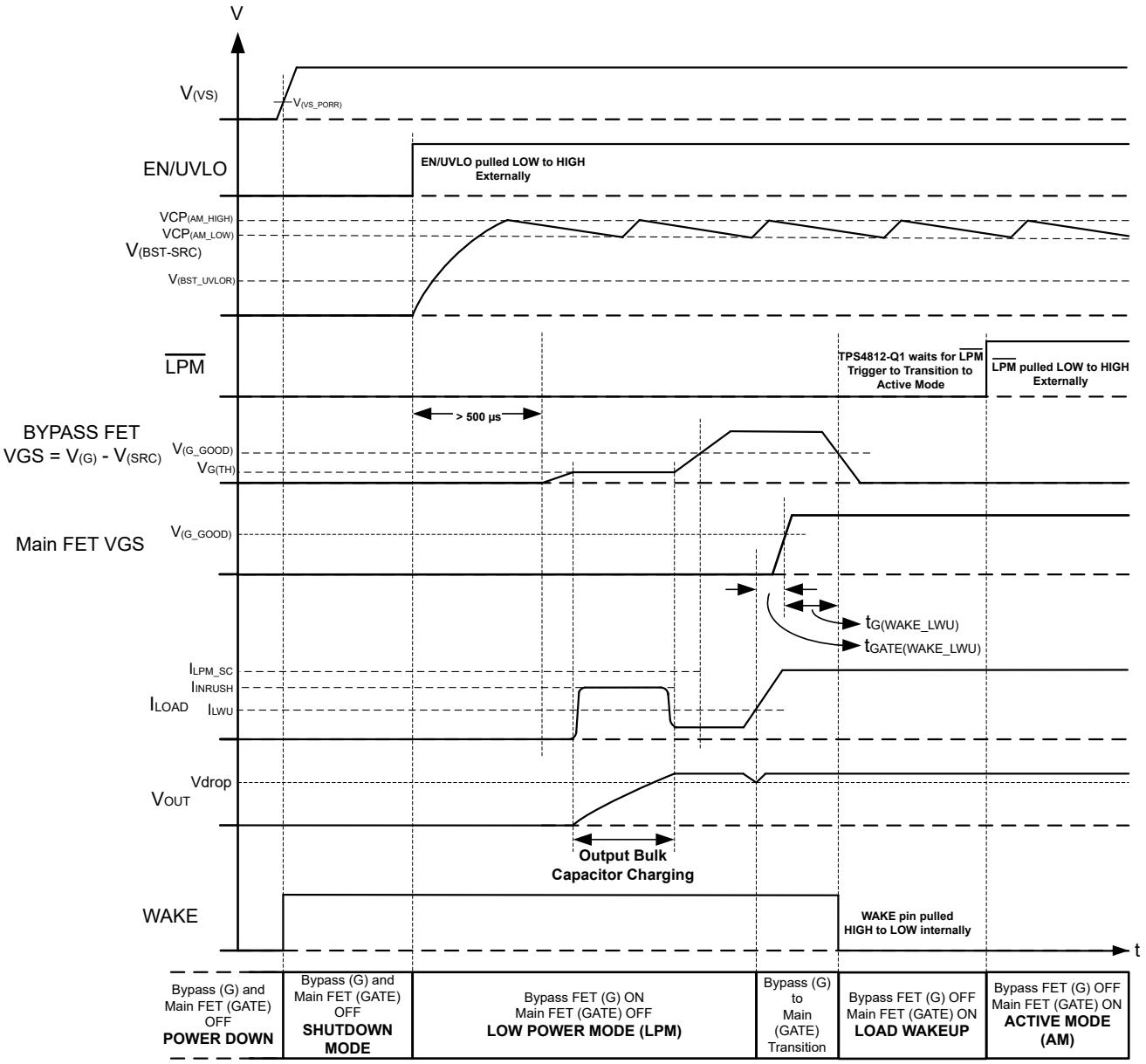


図 8-15. State Transition Timing Diagram With Load Wakeup Event

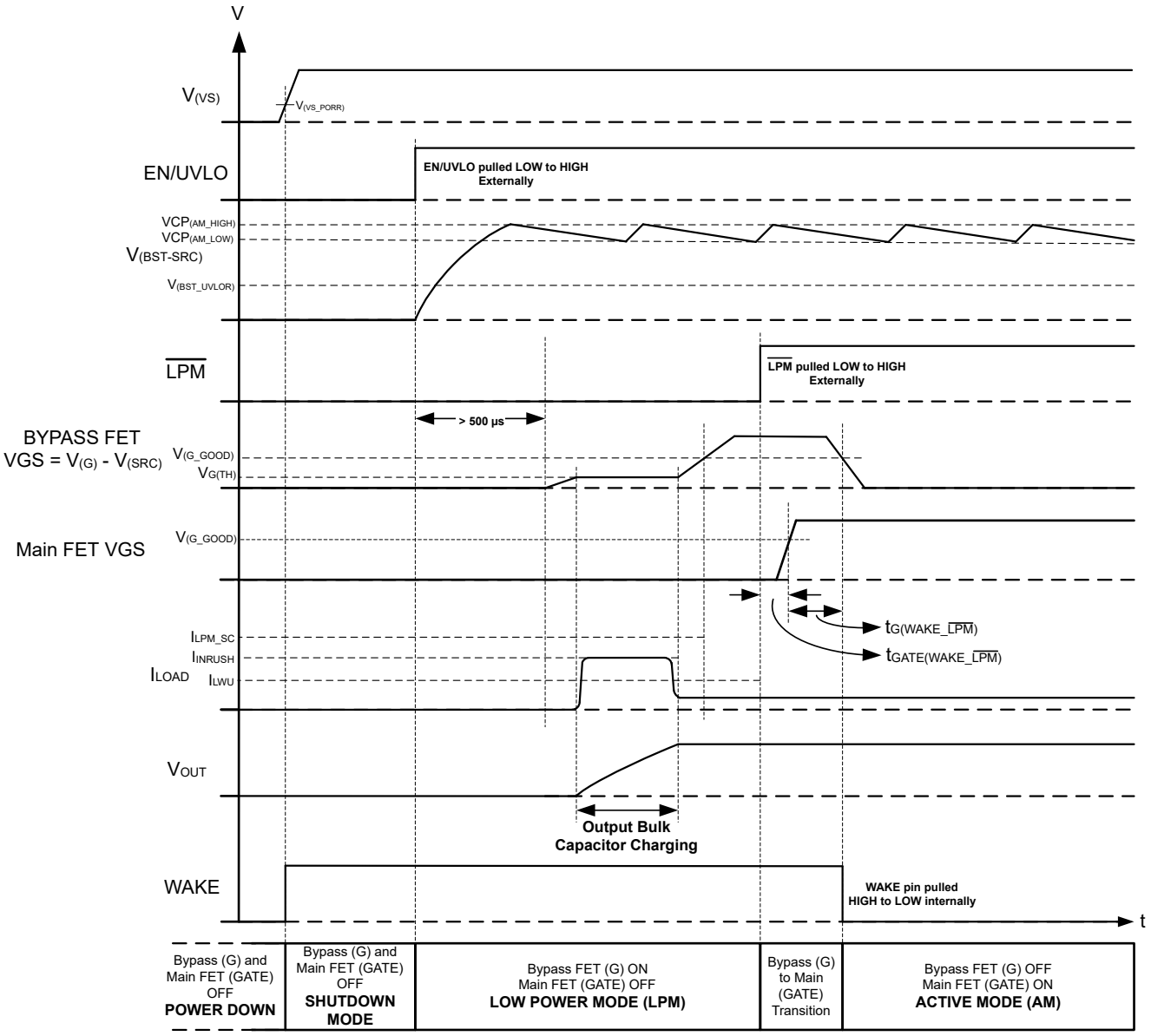


図 8-16. State Transition Timing Diagram With $\overline{\text{LPM}}$ Trigger

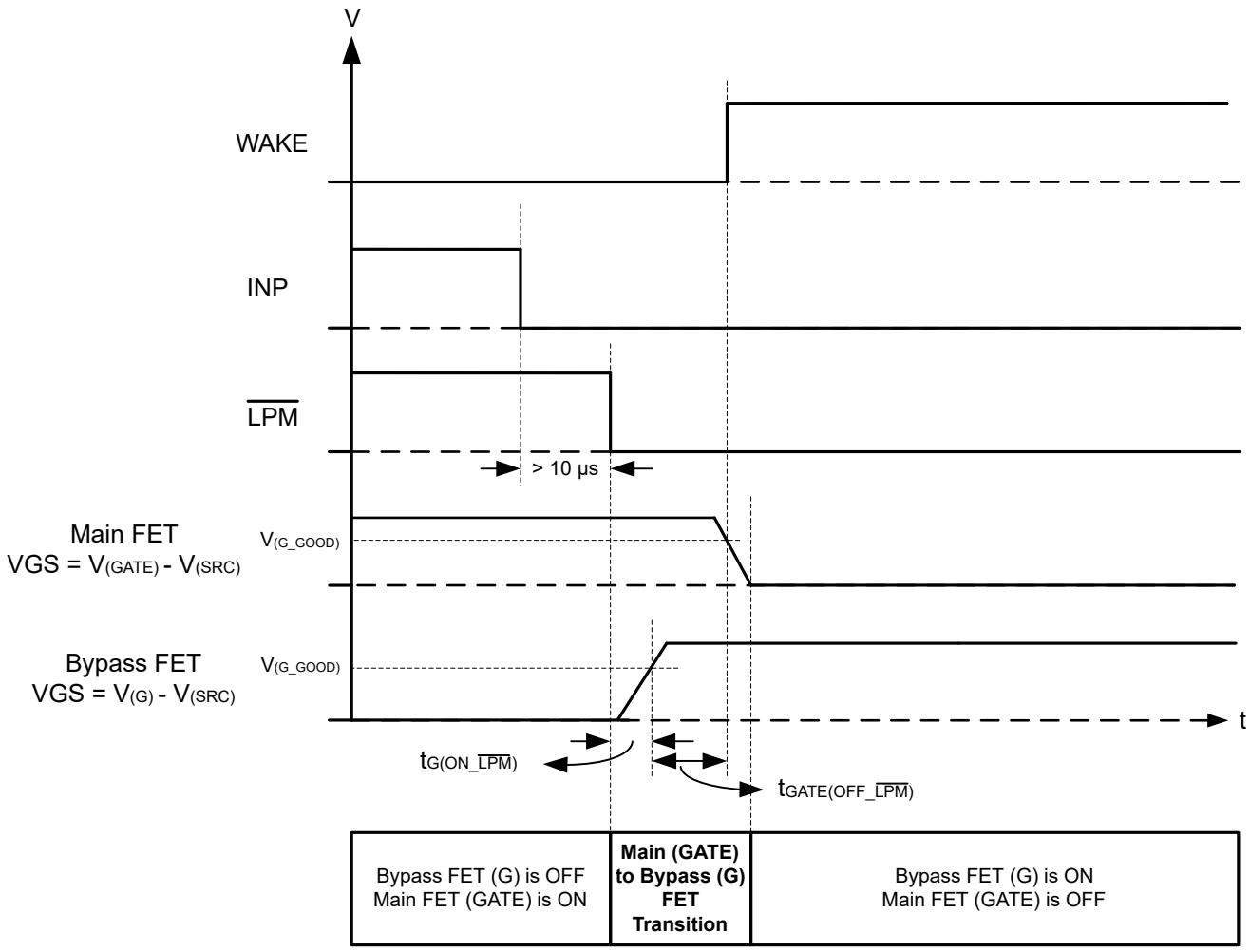


図 8-17. $\overline{\text{LPM}}$ and INP Signal Sequencing Consideration to Enter Into Low Power Mode From Active Mode

8.4.3 Power Down

If applied VS voltage is below $V_{(VS\_PORF)}$ then the device is in disabled state. In this mode, the charge pump and all the protection features are disabled. Both the gate drive outputs (GATE and G) are low.

8.4.4 Shutdown Mode

With VS > $V_{(VS\_PORR)}$ and EN/UVLO pulled < $V_{(ENF)}$, the device transitions to low I_Q shutdown mode. In this mode, the charge pump and all the protection features are disabled. Both the gate drive outputs (GATE and G) are low. The device consumes low I_Q of 1µA (typical) in this mode.

- **Shutdown to Low Power Mode:**

  To transition from shutdown to low power mode, drive EN/UVLO high (> $V_{(ENR)}$) and simultaneously drive $\overline{\text{LPM}}$ low for > 500µs.
- **Shutdown to Active Mode:**

  To transition from shutdown to active mode directly, drive EN/UVLO and $\overline{\text{LPM}}$ together high at same time.

8.4.5 Low Power Mode (LPM)

The device transitions from shutdown to low power mode when EN/UVLO is driven high (>$V_{(ENR)}$) and $\overline{\text{LPM}}$ is driven low for >500µs simultaneously.

The device can also transition from active mode to low power mode when $\overline{\text{LPM}}$ is pulled low. When entering from active mode to low power mode, $\overline{\text{LPM}}$ and INP signal sequencing consideration can be followed as per 図 8-17. Pulling INP low before $\overline{\text{LPM}}$ results in main FET (GATE drive) turning OFF which can cause output voltage droop momentarily before bypass FET (G drive) turns ON. Pulling INP low after at least 10µs of $\overline{\text{LPM}}$ is pulled low makes a seamless transition from active to low power mode without any output voltage dip.

In this mode, charge pump and G gate drive are enabled. The main FET (GATE drive) is OFF and bypass FET (G drive) is turned ON and WAKE pin asserts high in this state. TPS4812-Q1 consumes low I_Q of 20µA (typical) in low power mode.

The device transitions from low power mode to active mode when:

- **External Trigger:** $\overline{\text{LPM}}$ is pulled high externally
- **Internal Trigger:** Load current exceeds load wakeup trigger threshold (I_{LWU})

After load current exceeds load wakeup threshold (I_{LWU}), the device automatically turns ON main FET (GATE drive) first and bypass FET (G drive) is turned OFF after main FET (GATE drive) has fully turned ON and WAKE asserts low indicating the exit from the low power mode.

The device waits for external $\overline{\text{LPM}}$ signal to go high to transition into Active mode.

Protections available in low power mode are:

- **Input UVLO:** Bypass FET (G drive) is turned OFF when voltage on EN/UVLO falls below $V_{(UVLOF)}$.
- **Charge pump UVLO:** Bypass FET (G drive) is turned OFF when voltage between BST to SRC falls below $V_{(BST\_UVLOF)}$ and $\overline{\text{FLT}}$ asserts low.
- **Bypass FET Short-circuit Protection (Wakeup in short):** This protection is available until VGS of bypass FET (G to SRC) reaches V_{G_GOOD} threshold. If voltage across DRN and CS2– exceeds the set short-circuit threshold $V_{(LPM\_SCP)}$ then, the device transitions to LOAD WAKEUP state by turning ON main FET (GATE drive) within t_{LPM_SC} time.

  In LOAD WAKEUP state if load current is still high and exceeds set short-circuit threshold (V_{SCP}) then, the device turns OFF main path (GATE drive) and bypass FET (G drive) within t_{SC} time. The device goes in auto-retry or latch-off based on the selected configuration and $\overline{\text{FLT}}$ asserts low.

8.4.6 Active Mode (AM)

The device transitions from shutdown mode to active mode directly when EN/UVLO and $\overline{\text{LPM}}$ are driven high together at same time.

TPS4812-Q1 transitions from low power mode into active mode by:

- **External Trigger:** Drive $\overline{\text{LPM}}$ high externally.
- **Internal Trigger:** After load current exceeds load wakeup threshold (I_{LWU}), TPS4812-Q1 automatically turns ON main FET (GATE drive) and turns OFF the bypass FET (G drive). Drive $\overline{\text{LPM}}$ high after load wakeup event to switch to active mode.

In this mode, charge pump, gate drivers and all protections are enabled. The main FET (GATE drive) can be tuned ON or OFF by driving INP high or low respectively and bypass FET (G drive) is turned OFF and WAKE pin asserts low in this state.

The device exits active mode and enters low power mode when $\overline{\text{LPM}}$ is pulled low.

Protections available in active state are:

- **Input UVLO:** Main FET (GATE drive) is turned OFF when voltage on EN/UVLO falls below $V_{(UVLOF)}$.
- **Charge pump UVLO**: Main FET (GATE drive) is turned OFF when voltage between BST to SRC falls below $V_{(BST\_UVLOF)}$ and $\overline{\text{FLT}}$ asserts low.
- **Main path I^2t protection:** Main FET (GATE drive) is turned OFF when voltage across CS1+ and CS1– remains above I^2t start threshold ($V_{(OCP)}$) for time set by the I^2t factor based on C_{I2t}. The device goes in auto-retry or latch-off based on the selected configuration and $\overline{\text{FLT}}$ asserts low.

- **Main path Short-circuit protection**: Main FET (GATE drive) is turned OFF when voltage across CS1+ and CS1– exceeds the set short-circuit threshold ($V_{(SCP)}$). The device goes in auto-retry or latch-off based on the selected configuration and $\overline{FLT}$ asserts low.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application 1: Driving Power at all times (PAAT) Loads With Automatic Load Wakeup

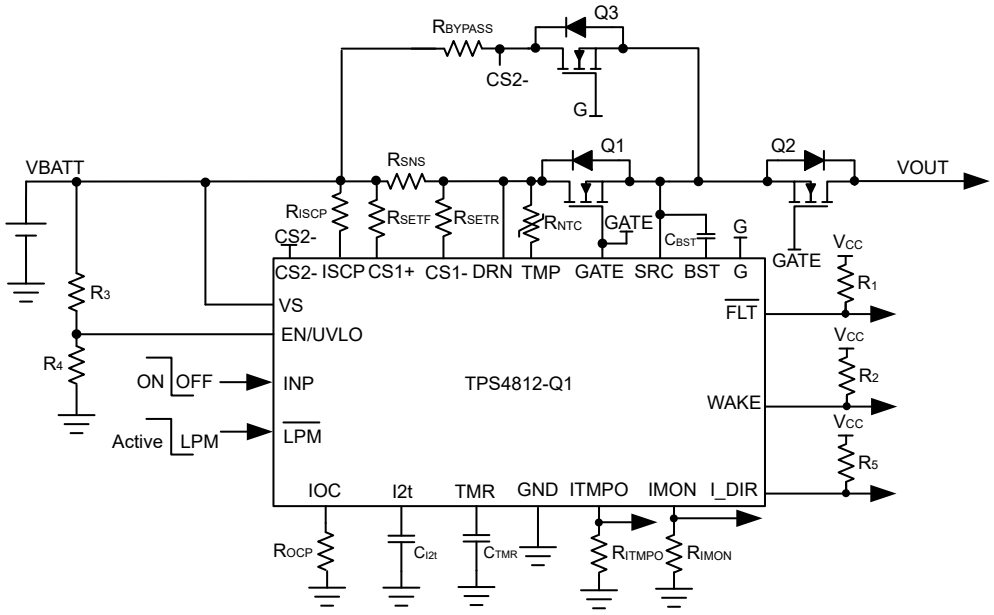


図 9-1. TPS4812-Q1 Application circuit for driving power at all times (PAAT) loads with automatic load wakeup

9.2.1 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{BATT_MIN} to V_{BATT_MAX}	36V to 60V
Undervoltage lockout set point, V_{INUVLO}	24V
Maximum load current, I_{OUT}	35A
I^2t Start threshold, I_{OC}	40A
I^2t Protection threshold	$3000A^2s$
Maximum overcurrent threshold, I_{OC_MAX}	120A
Short-circuit protection threshold, I_{SC}	130A
Fault response	Auto-retry
Auto-retry time	1000ms

表 9-1. Design Parameters (続き)

PARAMETER	VALUE
Load wakeup threshold, I_{LWU}	200mA

9.2.2 Detailed Design Procedure

Selection of Current Sense Resistor, R_{SNS}

The recommended range of the I^2t based overcurrent protection threshold voltage, $V_{(SNS\_OCP)}$, extends from 6mV to 200mV. Values near the low threshold of 6mV can be affected by the system noise. Values near the upper threshold of 200mV can cause high power dissipation in the current sense resistor. To minimize both the concerns, 20mV is selected as the I^2t protection start threshold voltage. The current sense resistor, R_{SNS} can be calculated using following equation:

$$R_{SNS} = \frac{V_{(SNS\_OCP)}}{I_{OC}} \tag{20}$$

For 40A (I_{OC}) of I^2t protection start threshold, R_{SNS} is calculated to be 0.5mΩ,

Two of 1mΩ, 1% sense resistor can be used in parallel.

Selection of IMON Scaling Resistor, R_{SET}

R_{SET} is the resistor connected between VS or input supply and CS1+ pins. This resistor scales the I^2t based overcurrent protection threshold voltage and coordinates with R_{IOC}, charging current on C_{I2t} and R_{IMON} to determine the I^2t profile and current monitoring output.

The maximum current on I^2t pin can be calculated based on short-circuit protection (I_{SC}) threshold based on following equation:

$$I_{I2t\_MAX}\left(\mu A\right) = K \times {I_{SC}}^2 \tag{21}$$

where scaling factor, K can be calculate based on below equation:

$$\text{Scaling factor}\left(K\right) = \frac{\left(0.1 \times \frac{R_{SNS}}{R_{SET}}\right)^2}{I_{BIAS}} \tag{22}$$

R_{SET} needs to adjusted so that I_{I2t_MAX} is always less than 100µA. The recommended range of R_{SET} is 100Ω–500Ω.

R_{SET} is selected as 300Ω, 1% for this design example to get I_{2t_MAX} current <100µA.

Choosing the Current Monitoring Resistor, R_{IMON}

Voltage at IMON pin $V_{(IMON)}$ is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The R_{IMON} must be selected based on the maximum load current and the input voltage range of the ADC used. R_{IMON} is set using following equation:

$$V_{(IMON)} = \left(V_{SNS} + V_{(VOS\_SET)}\right) \times \frac{0.9 \times R_{IMON}}{R_{SET}} \tag{23}$$

Where $V_{SNS} = I_{OC\_MAX} \times R_{SNS}$ and $V_{(OS\_SET)}$ is the input referred offset (±150µV) of the current sense amplifier. For I_{OC_MAX} = 120A and considering the operating range of ADC to be 0V to 3.3V (for example, $V_{(IMON)}$ = 3.3V), R_{IMON} is calculated to be 18.33kΩ.

Selecting R_{IMON} value less than shown in 式 23 ensures that ADC limits are not exceeded for maximum value of load current. Choose the closest available standard value: 18.2kΩ, 1%

Selection of Main path MOSFETs, Q1 and Q2

Q1 and Q2 For selecting the MOSFET Q1 and Q2, important electrical parameters are the maximum continuous drain current ID, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance $R_{DS(ON)}$. The maximum continuous drain current rating (ID) must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application. Considering 60V as the maximum application voltage due to load dump, MOSFETs with VDS voltage rating of 80V is chosen for this application.

The maximum VGS TPS4812-Q1 can drive is 12V, so a MOSFET with 15V minimum VGS rating must be selected.

To reduce the MOSFET conduction losses, an appropriate $R_{DS(ON)}$ is preferred. Based on the design requirements, two of IAUS200N08S5N023 are selected and its ratings are:

- 80V $V_{DS(MAX)}$ and ±20V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 2.3mΩ typical at 10V VGS
- MOSFET Qg(total) is 110nC max

TI recommends to make sure that the short-circuit conditions such V_{BATT_MAX} and I_{SC} are within SOA of selected FETs (Q1 and Q2) for >t_{SC} (5µs max) timing.

Selection of Bootstrap Capacitor, C_{BST}

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 600µA. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving two parallel BUK7J1R4-40H MOSFETs.

$$C_{BST} = \frac{Q_{g(total)}}{1\,V} \tag{24}$$

Choose closest available standard value: 220nF, 10 %.

Programming the I^2t Profile, R_{IOC} and C_{I2t} Selection

The R_{IOC} sets the I^2t protection start threshold, whose value can be calculated using following equation:

$$R_{IOC}\left(\Omega\right) = \frac{V_{(REF\_OC)}}{K \times \left(I_{OC}\right)^2} \tag{25}$$

where scaling factor, K can be calculate based on following equation:

$$\text{Scaling factor}\left(K\right) = \frac{\left(0.1 \times \frac{R_{SNS}}{R_{SET}}\right)^2}{I_{BIAS}} \tag{26}$$

To set 40A as I^2t protection start threshold, R_{IOC} value is calculated to be 23kΩ.

Choose the closest available standard value: 23kΩ, 1%.

The time to turn OFF the gate drive at maximum overcurrent limit (I_{OC_MAX}) can be determined using below equation:

$$t_{OC\_MIN}\left(s\right) = \frac{\text{I2T factor}}{I_{OC\_MAX} \times I_{OC\_MAX}} \tag{27}$$

To set 3000A^{2}s as I^{2}t factor, t_{OC_MIN} value is calculated to be 208ms.

Use 式 28 to calculate the required C_{I2t} value:

$$C_{I2t}\left(F\right) = \frac{K \times t_{OC\_MIN}}{V_{(I2t\_OC)} - V_{(I2t\_OFFSET)}} \times \left[I_{OC\_MAX}{}^2 - I_{OC}{}^2\right] \quad (28)$$

To set 3000A^{2}s as I^{2}t factor with 40A as I^{2}T start threshold and 120A as maximum overcurrent, C_{I2t} is calculated to be ~880nF.

Choose the closest available standard value: 1µF, 10%.

Programming the Short-Circuit Protection Threshold, R_{ISCP} Selection

The R_{ISCP} sets the short-circuit protection threshold, whose value can be calculated using following equation:

$$R_{ISCP}\left(k\Omega\right) = \frac{I_{SC} \times R_{SNS} - 1.8}{I_{SCP}} \quad (29)$$

To set 130A as short-circuit protection threshold, R_{ISCP} value is calculated to be 2.53kΩ for two FETs in parallel. Choose the closest available standard value: 2.55kΩ, 1%.

Programming the Fault Timer Period, C_{TMR} Selection

For the design example under discussion, the auto-retry time, t_{RETRY} can be set by selecting appropriate capacitor C_{TMR} from TMR pin to ground. The value of C_{TMR} to set 1ms for t_{RETRY} can be calculated using following equation:

$$t_{RETRY}\left(s\right) = 64 \times C_{TMR} \times \left[\frac{V_{(TMR\_HIGH)} - V_{(TMR\_LOW)}}{I_{(TMR\_SRC)}}\right] \quad (30)$$

To set 1000ms as auto-retry time, C_{TMR} value is calculated to be 39.06nF.

Choose closest available standard value: 47nF, 10%.

Programming the Load Wakeup Threshold, R_{BYPASS} and Q3 Selection

During normal operation, the resistor R_{BYPASS} along with bypass FET R_{DSON} is used to set load wakeup current threshold. For selecting the MOSFET Q3, important electrical parameters are the maximum continuous drain current ID, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance $R_{DS(ON)}$.

Based on the design requirements, SQS182ELNW-T1 is selected and its ratings are:

- 80V $V_{DS(MAX)}$ and ±20V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 11mΩ typical at 10V VGS
- MOSFET $Q_{g(total)}$ is 26nC typical
- MOSET $V_{GS(th)}$ is 1.4V min
- MOSFET C_{ISS} is 1457pF typical

R_{BYPASS} resistor value can be selected using below equation:

$$R_{BYPASS} = \frac{V_{(LWU)}}{I_{LWU}} \quad (31)$$

To set 200mA load wakeup current, R_{BYPASS} resistor is calculated to be 1Ω.

The average power rating of the bypass resistor can be calculated by following equation:

$$P_{AVG} = I_{LWU}{}^2 \times R_{BYPASS} \quad (32)$$

The average power dissipation of R_{BYPASS} is calculated to be 0.04W.

The peak power dissipation in the bypass resistor is given by following equation:

$$P_{PEAK} = \frac{V_{BATT\_MAX}^2}{R_{BYPASS}} \quad (33)$$

The peak power dissipation of R_{BYPASS} is calculated to be ~3600W. The peak power dissipation time for power-up with short into LPM can be derived from $t_{(LPM\_SC)}$ parameter (5µs) in electrical characteristics table.

Based on P_{PEAK} and $t_{(LPM\_SC)}$, Two of 2Ω, 1%, 1.5W CRCW25122R00JNEGHP resistor are used in parallel to support both average and peak power dissipation for >$t_{(LPM\_SC)}$ time. TI suggests the designer to share the entire power dissipation profile of bypass resistor with the resistor manufacturer and get their recommendation.

The peak short-circuit current in bypass path can be calculated based on following equation:

$$I_{PEAK\_BYPASS} = \frac{V_{BATT\_MAX}}{R_{BYPASS}} \quad (34)$$

I_{PEAK_BYPASS} is calculated to be 60A based on R_{BYPASS} selected in 式 31. TI suggest the designer to ensure that operating point (V_{BATT_MAX}, I_{PEAK_BYPASS}) for bypass path (Q3) is within the SOA curve for > $t_{(LPM\_SC)}$ time.

Setting the Undervoltage Lockout Set Point, R3 and R4

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider network of R3 and R4 connected between VS, EN/UVLO and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving below equation:

$$V_{(UVLOR)} = V_{INUVLO} \times \frac{R4}{R3 + R4} \quad (35)$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for R3 and R4. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I_{(R34)}$ must be chosen to be 20 times greater than the leakage current of UVLO pin.

From the device electrical specifications, $V_{(UVLOR)}$ = 1.2V. From the design requirements, V_{INUVLO} is 24V. To solve the equation, first choose the value of R3 = 470kΩ and use 式 35 to solve for R4 = 24.3kΩ.

Choose the closest standard 1% resistor values: R3 = 470kΩ, and R4 = 24.9kΩ.

9.2.3 Application Curves

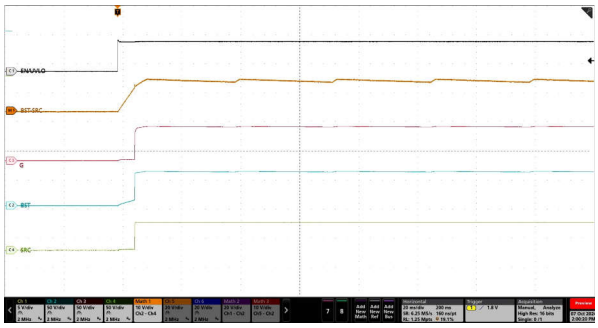


図 9-2. Start-Up Profile of Low Power Path ($\overline{LPM}$ = Low, VIN = 48V, No Load, C_{BST} = 470nF)

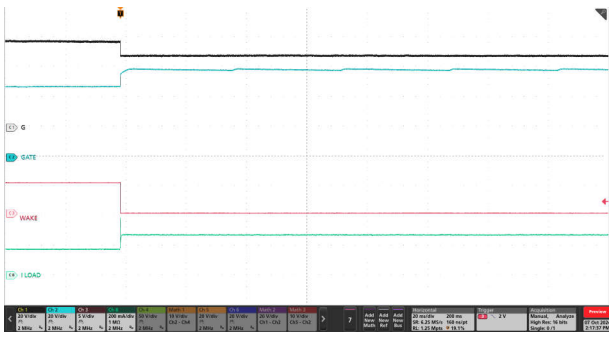


図 9-3. State Transition From LPM to Active Mode ($\overline{LPM}$ = Low, VIN = 48V, EN/UVLO = High)

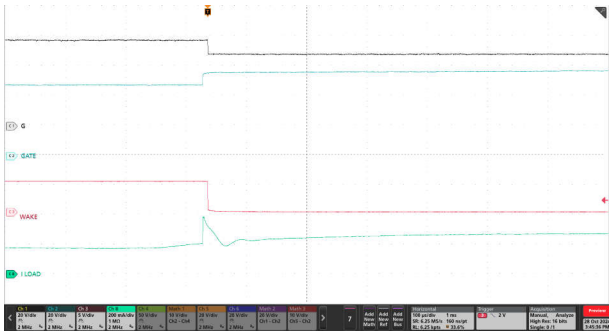


図 9-4. Zoom-In View of State Transition From LPM to Active Mode ($\overline{LPM}$ = Low, VIN = 48V, EN/UVLO = High)

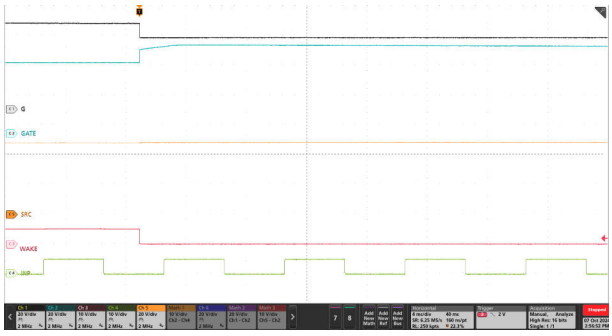


図 9-5. When $\overline{LPM}$ = Low in LOAD WAKEUP state, INP Has No Control on GATE

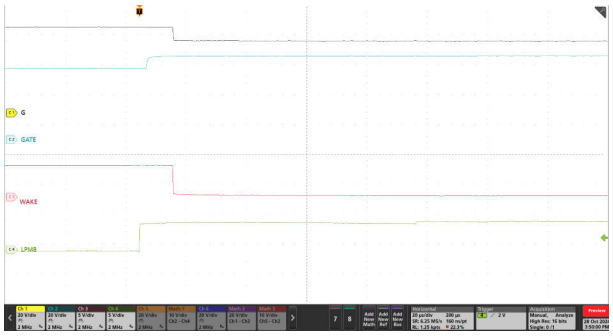


図 9-6. State Transition From LPM to Active Mode ($\overline{LPM}$ = Low to High, VIN = 48V, No Load)

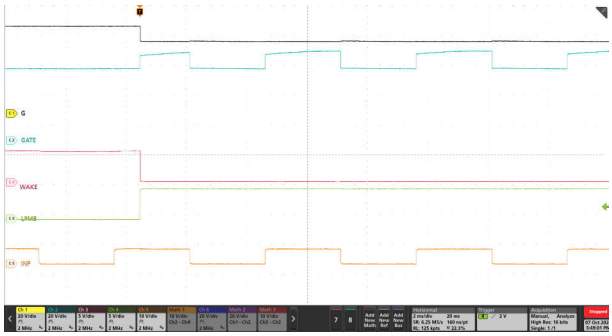


図 9-7. With $\overline{LPM}$ = Low to High, INP Gained Control on GATE (VIN = 48V, No Load)

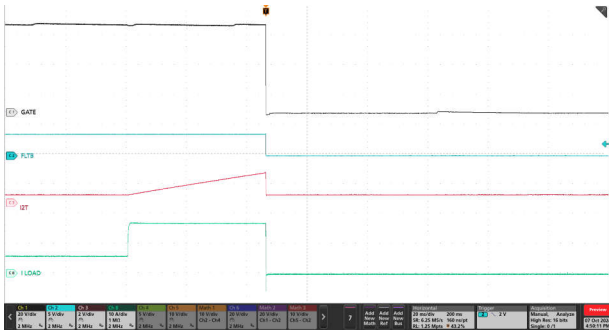


図 9-8. I^2T based Overcurrent Response of TPS4812-Q1 EVM for 6A to 16A Load Step

図 9-9. I^2T based Overcurrent Response of TPS4812-Q1 EVM for 6A to 23A Load Step

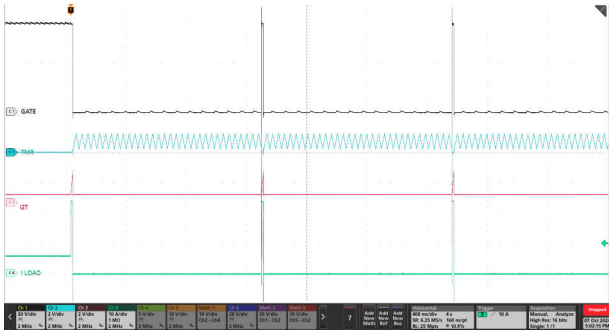


図 9-10. Auto-Retry Response of TPS4812-Q1 for an I^2T-Based Overcurrent Fault

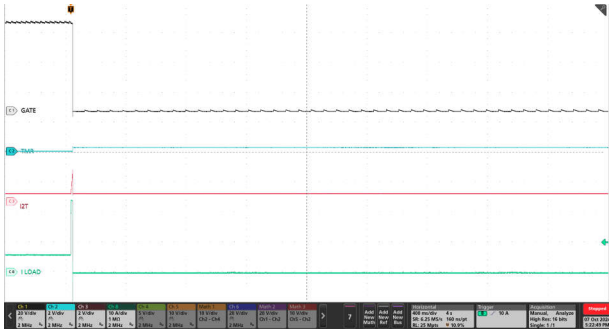


図 9-11. Latch-Off Response of TPS4812-Q1 for an I^2T-Based Overcurrent Fault

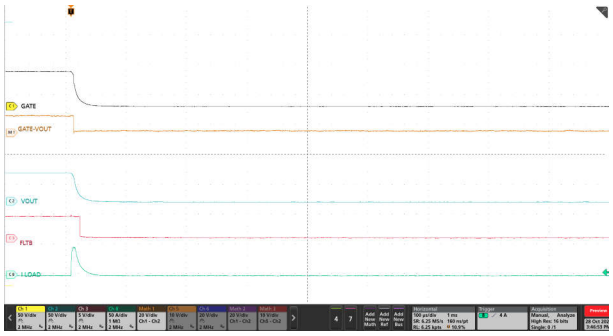


図 9-12. Output Short-Circuit Response of TPS4812-Q1

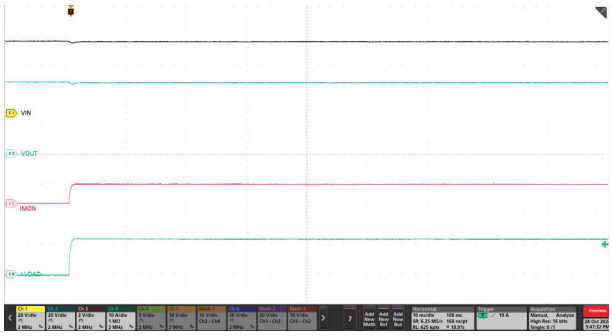


図 9-13. TPS4812-Q1 Current Monitoring Output (IMON) Transient Response

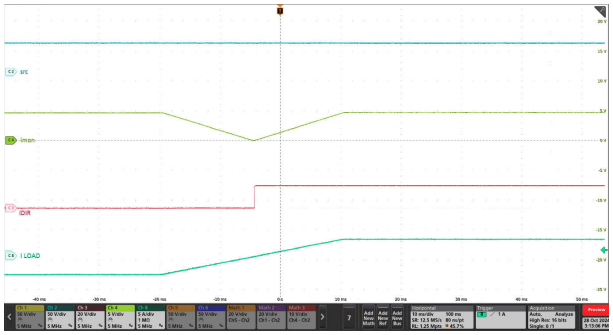


図 9-14. TPS4812-Q1 Bi-directional Current Monitoring Output (IMON, I_DIR) Transient Response

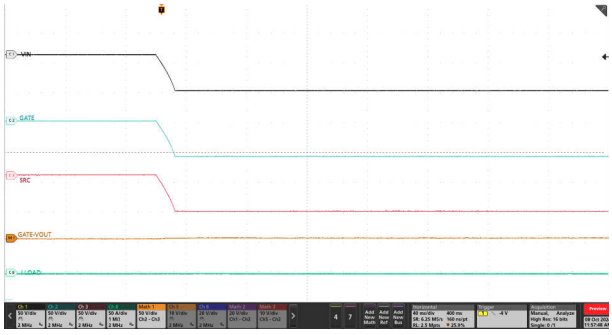


図 9-15. GATE Turn-OFF During Input Reverse Battery Fault

9.3 Typical Application 2: Driving Power at all times (PAAT) Loads With Automatic Load Wakeup and Output Bulk Capacitor Charging

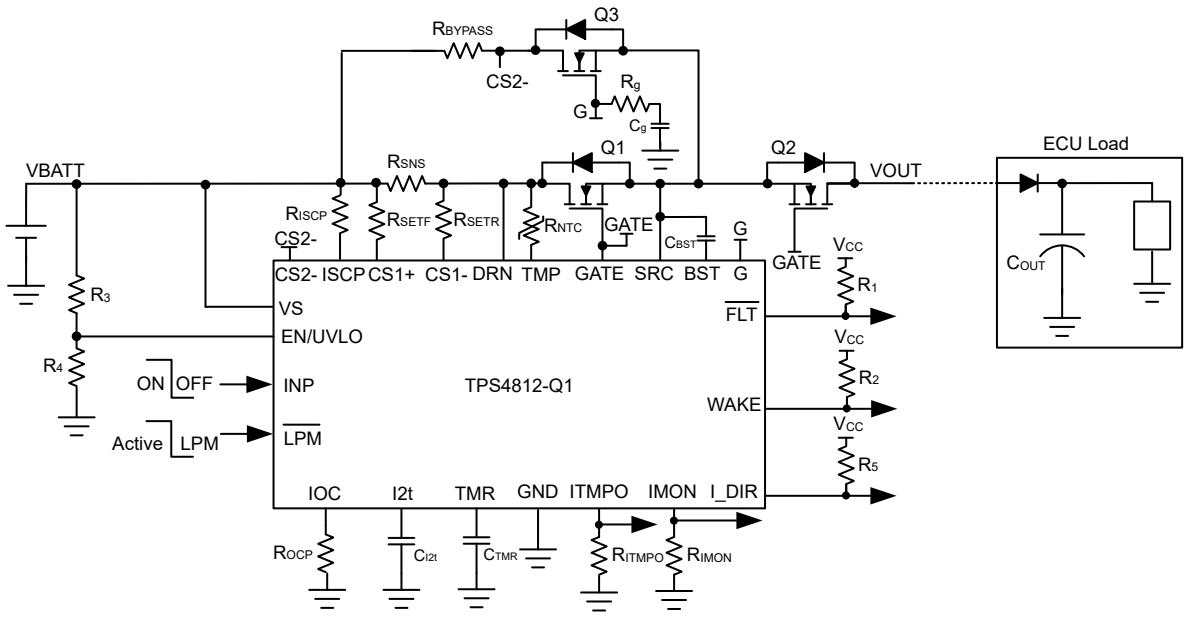


図 9-16. TPS4812-Q1 Application circuit for driving power at all times (PAAT) loads with automatic load wakeup and output bulk capacitor charging

9.3.1 Design Requirements

表 9-2. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{BATT_MIN} to V_{BATT_MAX}	36V to 60V
Undervoltage lockout set point, V_{INUVLO}	24V
Maximum load current, I_{OUT}	35A
I^2T Start threshold, I_{OC}	40A
I^2T Protection threshold	$3000A^2s$
Maximum overcurrent threshold, I_{OC_MAX}	120A
Short-circuit protection threshold, I_{SC}	130A
Fault response	Auto-retry
Auto-retry time	1000ms
Load wakeup threshold, I_{LWU}	200mA
Output bulk capacitor, C_{OUT}	1mF
C_{OUT} charging time, T_{charge}	40ms

9.3.2 External Component Selection

By following similar design procedure as outlined in , the external component values are calculated as below:

- R_{SNS} = 0.5mΩ
- R_{SET} = 300Ω
- R_{IMON} = 18.2kΩ
- R_{IOC} = 23kΩ to set 40A as I^2t protection start threshold
- C_{I2t} = 1µF to set $3000A^2s$ as I^2T factor
- C_{BST} = 220nF
- R_{ISCP} = 2.55kΩ to set 130A as short-circuit protection threshold
- C_{TMR} = 47nF to set 1000ms auto-retry time
- R3 and R4 are selected as 470kΩ and 24.9kΩ respectively to set VIN undervoltage lockout threshold at 24V

Programming the Load Wakeup Threshold, R_{BYPASS} and Q_3 Selection

During normal operation, the series resistor R_{BYPASS} is used to set load wakeup current threshold. After V_{G_GOOD} threshold is reached, the voltage between DRN and CS2– is compared against $V_{(LWU)}$ threshold (200mV typ) for load wakeup event. For selecting the MOSFET Q3, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance R_{DSON}.

Based on the design requirements, IAUS200N08S5N023 is selected and its ratings are:

- 80V $V_{DS(MAX)}$ and ±20V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 2.3mΩ typical at 10V VGS

R_{BYPASS} resistor value can be selected using below equation:

$$R_{BYPASS} = \frac{V_{(LWU)}}{I_{LWU}} \quad (36)$$

To set 200mA load wakeup current, R_{BYPASS} resistor is calculated to be 1Ω.

The average power rating of the bypass resistor can be calculated by following equation:

$$P_{AVG} = I_{LWU}^2 \times R_{BYPASS} \quad (37)$$

The average power dissipation of R_{BYPASS} is calculated to be 0.04W.

The peak power dissipation in the bypass resistor is given by following equation:

$$P_{PEAK} = \frac{V_{BATT\_MAX}^2}{R_{BYPASS}} \quad (38)$$

The peak power dissipation of R_{BYPASS} is calculated to be ~3600W. The peak power dissipation time for power-up with short into LPM can be derived from $t_{(LPM\_SC)}$ parameter (5µs) in electrical characteristics table.

Based on P_{PEAK} and $t_{(LPM\_SC)}$, Two of 2Ω, 1%, 1.5W CRCW25122R00JNEGHP resistor are used in parallel to support both average and peak power dissipation for > $t_{(LPM\_SC)}$ time. TI suggests the designer to share the entire power dissipation profile of bypass resistor with the resistor manufacturer and get their recommendation.

The peak short-circuit current in bypass path can be calculated based on following equation:

$$I_{PEAK\_BYPASS} = \frac{V_{BATT\_MAX}}{R_{BYPASS}} \quad (39)$$

I_{PEAK_BYPASS} is calculated to be 60A based on R_{BYPASS} selected in 式 36. TI suggest the designer to ensure that operating point (V_{BATT_MAX}, I_{PEAK_BYPASS}) for bypass path (Q3) is within the SOA curve for > $t_{(LPM\_SC)}$ time.

Programming the Inrush Current, R_g and C_g Selection

Use following equation to calculate the I_{INRUSH}:

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT\_MAX}}{T_{charge}} \quad (40)$$

I_{INRUSH} calculated in 式 40 should be always less than wakeup in short in low power mode (I_{LPM_SC}) current which can be calculated using following equation:

$$I_{LPM\_SC} = \frac{2\ V}{R_{BYPASS}} \quad (41)$$

For 1Ω R_{BYPASS}, I_{LPM_SC} is calculated to be 2A which is less than I_{INRUSH}.

Use following equation to calculate the required C_g based on I_{INRUSH} calculated in 式 40.

$$C_g = \frac{C_{LOAD} \times I_{(G)}}{I_{INRUSH}} \quad (42)$$

Where, $I_{(G)}$ is 100µA (typical)

To set I_{INRUSH} at 1.5A, C_g value is calculated to be ~50nF.

A series resistor R_g must be used in conjunction with Cg to limit the discharge current from Cg during turn-off .

The chosen value of R_g is 100Ω and C_g is 68nF.

9.3.3 Application Curves

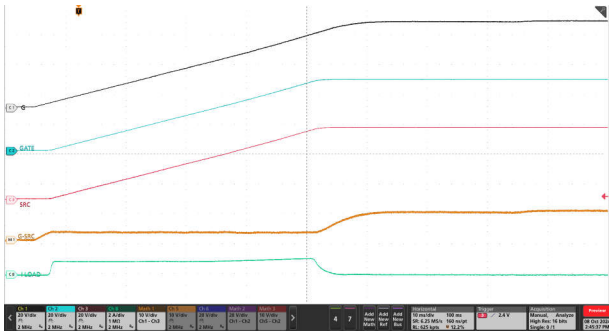


図 9-17. Inrush Current Profile With 1000µF at the Output ($\overline{\text{LPM}}$ = Low)

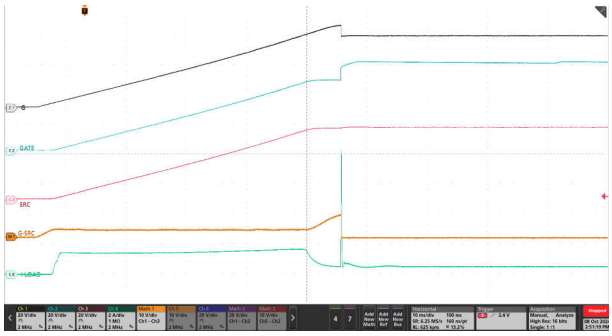


図 9-18. Inrush Current Profile With 1000µF at the Output and 0.5A Load ($\overline{\text{LPM}}$ = Low)

9.4 Power Supply Recommendations

When the external MOSFETs turn-OFF during the conditions such as INP control, overcurrent or short-circuit protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the Absolute Maximum Ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS4812-Q1 gets powered from the VS pin. Voltage at this pin must be maintained above $V_{(VS\_PORR)}$ level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place a R_{VS} – C_{VS} filter between the input supply line and VS pin to filter out the supply noise. TI recommends an R_{VS} value around 100-Ω and C_{VS} value around 0.1 µF.

TPS4812-Q1 uses DRN pin for sensing input reverse polarity fault event. If the input power supply source is noisy with transients, then TI recommends to place a R_{DRN} – C_{DRN} filter between the input supply line and DRN pin to filter out the supply noise. TI recommends an R_{DRN} value around 10-Ω and C_{DRN} value around 0.1 µF.

In a case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS1+ and CS1– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add a placeholder for RC filter components across the sense resistor (R_{SNS}) and tweak the values during test in the real system.

図 9-19 shows the circuit implementation with optional protection components.

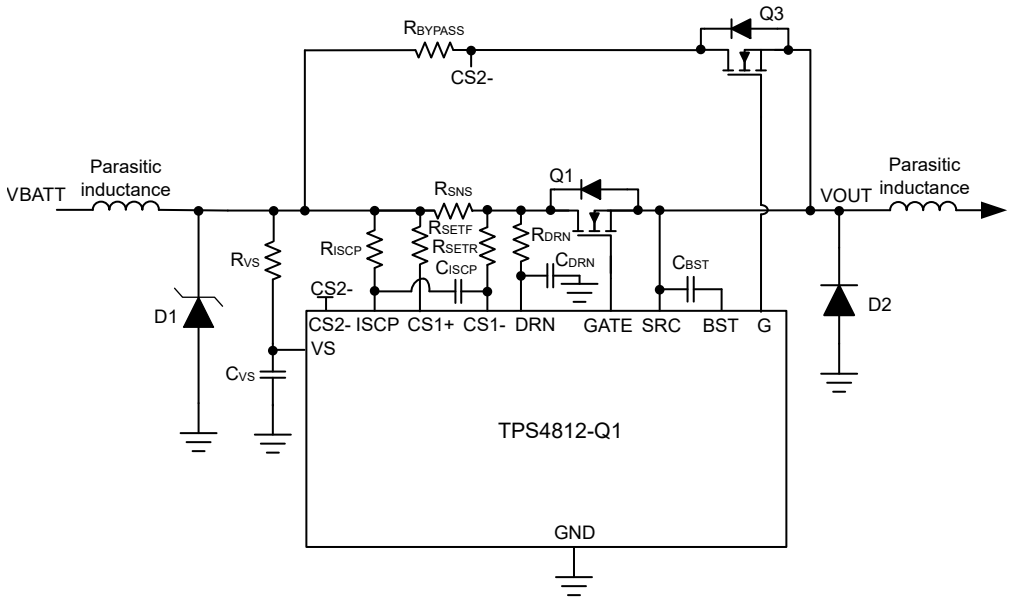


図 9-19. Circuit Implementation With Optional Protection Components For TPS4812-Q1

9.5 Layout

9.5.1 Layout Guidelines

- The sense resistor (R_{SNS}) must be placed close to the TPS4812-Q1 and then connect R_{SNS} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.
- For all the applications, TI recommends a 0.1 µF or higher value ceramic decoupling capacitor between VS terminal and GND. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- The high current path from the board's input to the load, and the return path, must be parallel and close to each other to minimize loop inductance.
- The external MOSFETs must be placed close to the controller such that the GATE of the MOSFETs are close to GATE pin to form short GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- The external boot-strap capacitor must be placed close to BST and SRC pins to form very short loop.
- The ground connections for the various components around the TPS4812-Q1 must be connected directly to each other, and to the TPS4812-Q1's GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.

9.5.2 Layout Example

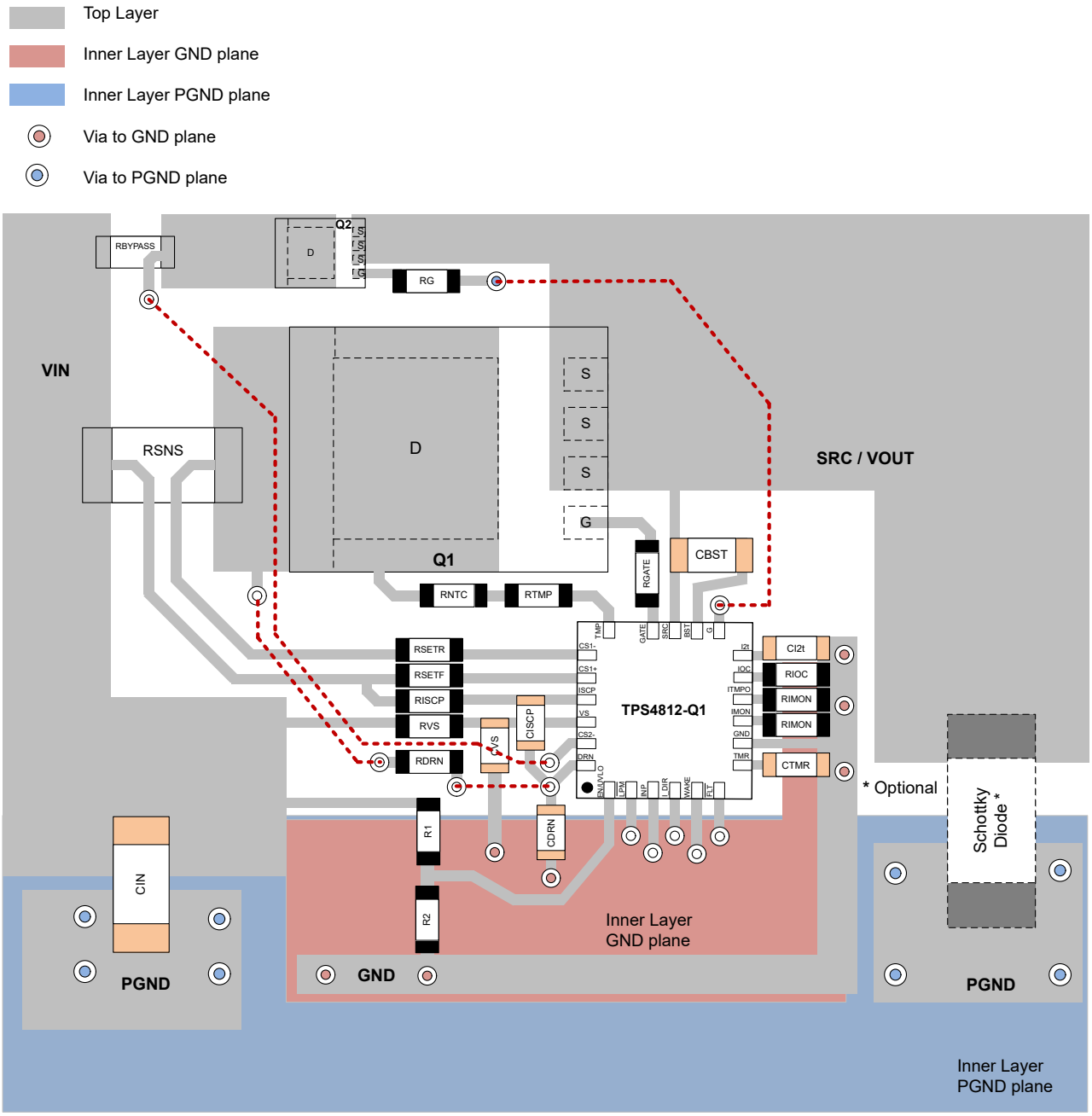


図 9-20. Typical PCB Layout Example of TPS4812-Q1

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS48120QRGERQ1	Active	Production	VQFN (RGE) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 48120Q
TPS48120QRGERQ1.A	Active	Production	VQFN (RGE) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TPS48120QRGERQ1	TPS 48120Q
TPS48121QRGERQ1	Active	Production	VQFN (RGE) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 48121Q
TPS48121QRGERQ1.A	Active	Production	VQFN (RGE) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TPS48121QRGERQ1	TPS 48121Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

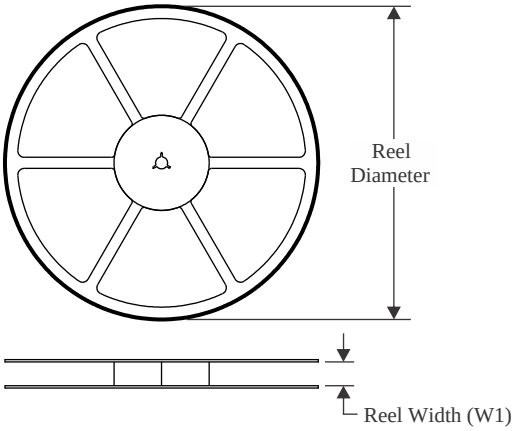
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

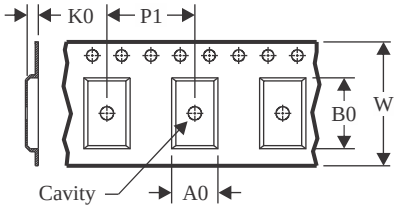
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

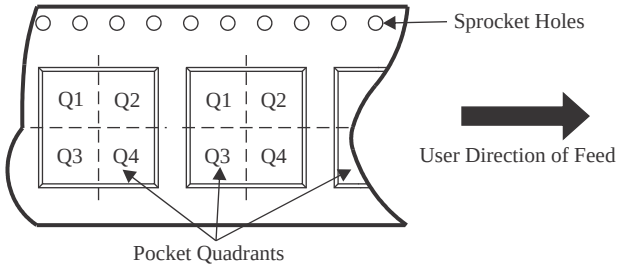


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

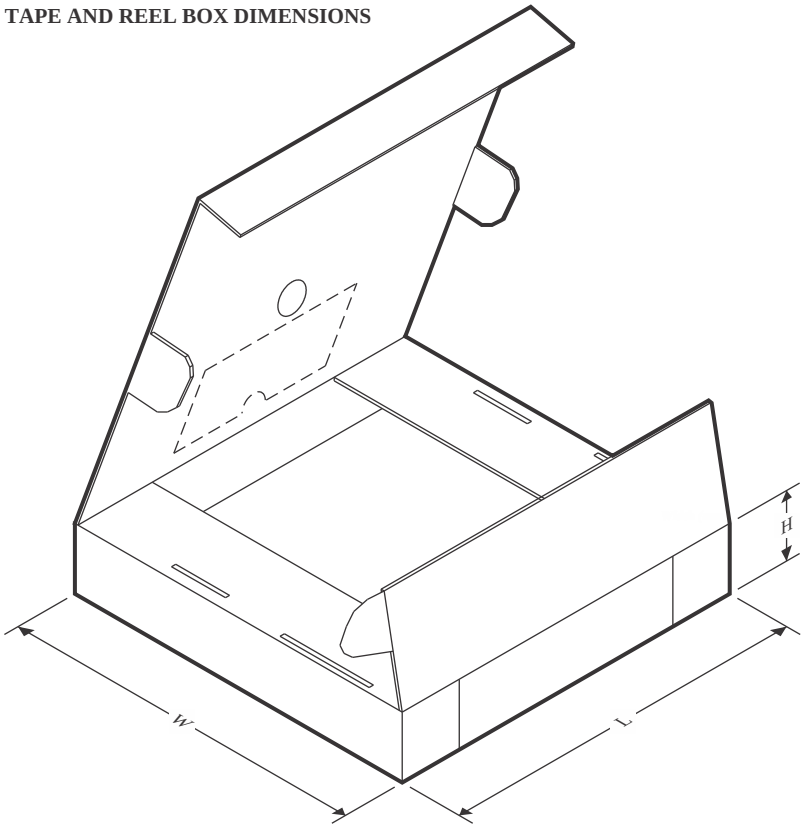
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS48120QRGERQ1	VQFN	RGE	23	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS48121QRGERQ1	VQFN	RGE	23	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS48120QRGERQ1	VQFN	RGE	23	3000	367.0	367.0	35.0
TPS48121QRGERQ1	VQFN	RGE	23	3000	367.0	367.0	35.0

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265