TPS4800-Q1 逆極性保護、短絡保護および診断機能を備えた 100V 車載用低 I_Q ハイサイド ドライバ

1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～+125℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 3.5V～95V の入力範囲 (絶対最大定格 100V)
- 最低 –65V までの逆入力保護
- 内蔵 11V チャージ ポンプ
- 低い静止電流:43µA (動作時)
- 1.5µA の低シャットダウン電流 (EN/UVLO = Low)
- 強力なゲート ドライバ (2A のソースとシンク)
- 外付けの Rsense または可変遅延 (TMR) 付き MOSFET VDS センシングを使用した可変短絡保護 (ISCP)
- ハイサイドまたはローサイドの電流検出構成 (CS_SEL)
- 短絡フォルト時のフォルト表示 ($\overline{FLT}$)、入力低電圧および短絡コンパレータ診断 (SCP_TEST)
- ゲート駆動 UVLO のフォルト表示 (FLT_GD)
- 可変低電圧誤動作防止 (UVLO) および過電圧保護 (OV)

2 アプリケーション

- 車載用 48V BMS
- DC/DC コンバータ
- 電動工具

3 概要

TPS48000-Q1 は、保護および診断機能を備えた、100V、低 I_Q スマート ハイサイド ドライバです。本デバイスは、動作電圧範囲が 3.5V～95V と広いため、12V、24V、48V のシステム設計に適しています。このデバイスは、最低 -65V の負の電源電圧に耐えられ、負荷を保護できます。

大電流システム設計において並列 MOSFET を使用して電力スイッチングを可能にする強力な (2A) ゲート ドライブを備えています。

このデバイスは、可変短絡保護機能を備えています。自動リトライおよびラッチオフ フォルト動作は設定可能です。電流検出は、CS+ および CS– ピンを使用して、外付けの検出抵抗、または MOSFET VDS センシングのいずれかを使用して実行できます。CS_SEL ピン入力を使用して、ハイサイドまたはローサイドの電流検出抵抗構成が可能です。このデバイスは、SCP_TEST 入力の外部制御を使用した、内蔵の短絡コンパレータを診断する機能も備えています。

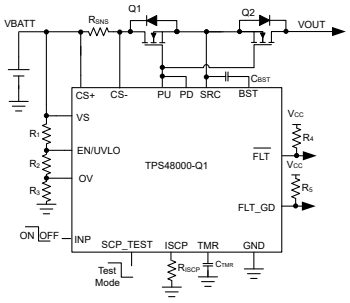
動作時の静止電流が 43µA (代表値) と低いため、常時オンのシステム設計が可能です。EN/UVLO が Low で、静止電流が 1.5µA (代表値) まで低減します。

TPS48000-Q1 は、19 ピンの VSSOP パッケージで供給されます。

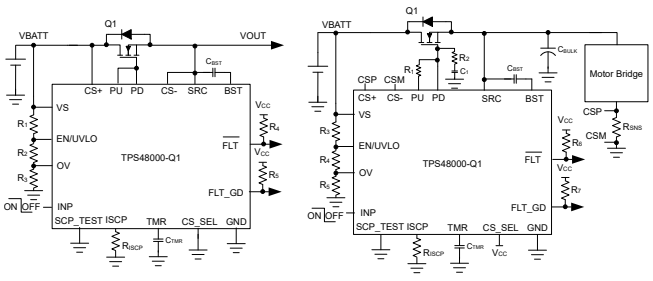
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS48000-Q1	DGX (VSSOP、19)	5.1mm × 3.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



DC-DC 用スマート ハイサイド ドライバ



ハイサイド VDS センシングとローサイド電流センシングを使用する構成

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4 Pin Configuration and Functions

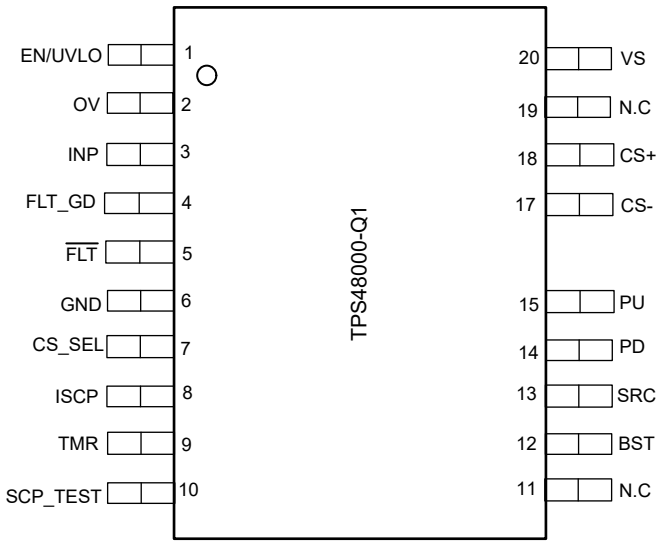


図 4-1. DGX Package, 19-Pin VSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN/UVLO	1	I	EN/UVLO Input. A voltage on this pin above 1.24V enables normal operation. Forcing this pin below 0.3V shuts down the device reducing quiescent current to 1.5µA (typical). Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pull down of 100nA pulls EN/UVLO low and keeps the device in shutdown state.
OV	2	I	Adjustable overvoltage threshold input. Connect a resistor ladder from input supply, OV to GND. When the voltage at OVP exceeds the overvoltage cut-off threshold then the PD is pulled down to SRC turning OFF the external FET. When the voltage at OV goes below OV falling threshold then PU gets pulled up to BST, turning ON the external FET. OV must be connected to GND when not used. When OV is left floating an internal pull down of 100nA pulls OV low and keeps PU pulled up to BST.
INP	3	I	Input Signal for external discharge FET control. CMOS compatible input reference to GND that sets the state of PD and PU pins. INP has an internal weak pull down of 100nA to GND to keep PD pulled to SRC when INP is left floating.
FLT_GD	4	O	Open Drain Fault Output for gate drive UVLO. This pin asserts low when gate drive across PU to SRC is above 7.5V.
$\overline{\text{FLT}}$	5	O	Open Drain Fault Output. This pin asserts low during short circuit fault, input UVLO, overvoltage and during SCP comparator diagnosis. If $\overline{\text{FLT}}$ feature is not desired then connect it to GND.
GND	6	G	Connect GND to system ground.

表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CS_SEL	7	I	Current sense select input. Connect this pin to ground to activate high side current sense. Drive this pin to >2V to activate low side current sensing. CS_SEL has an internal weak pull down of 100nA to GND.
ISCP	8	I	Short circuit detection setting. A resistor across ISCP to GND sets the short circuit current comparator threshold. If short-circuit protection feature is not desired then connect CS+, CS–, VS pins together and connect ISCP, TMR pins to GND.
TMR	9	I	Fault Timer Input. A capacitor across TMR pin to GND sets the times for fault turn-off. Leave it open for fastest setting. If short-circuit protection feature is not desired then connect CS+, CS–, VS pins together and connect ISCP, TMR pins to GND.
SCP_TEST	10	I	Internal short circuit comparator (SCP) diagnosis input. When SCP_TEST is driven low to high with INP pulled high, the internal SCP comparator operation is checked. $\overline{FLT}$ goes low and PD gets pulled to SRC if SCP comparator is functional. Connect SCP_TEST pin to GND if this feature is not desired. SCP_TEST has an internal weak pull down of 100nA to GND.
N.C	11	—	No connect.
BST	12	O	High Side Bootstrapped Supply. An external capacitor with a minimum value of $>Q_{g(tot)}$ of the external FET must be connected between this pin and SRC.
SRC	13	O	Source connection of the external FET.
PD	14	O	High Current Gate Driver Pull-Down. This pin pulls down to SRC. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.
PU	15	O	High Current Gate Driver Pull-Up. This pin pulls up to BST. Connect this pin to PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the in-rush current during turn-on.
CS-	17	I	Current sense negative input.
CS+	18	I	Current sense positive input.
N.C	19	—	No connect.
VS	20	P	Supply pin of the controller.

(1) I = input, O = output, I/O = input and output, P = power, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	VS, CS+, CS– to GND	–65	100	V
	SRC to GND	–65	100	
	PU, PD, BST to SRC	–0.3	19	
	ISCP, TMR, SCP_TEST to GND	–0.3	5.5	
	EN/UVLO, OV, INP, CS_SEL, $V_{(VS)}$ > 0 V	–1	70	
	EN/UVLO, OV, INP, CS_SEL, $V_{(VS)}$ ≤ 0 V	$V_{(VS)}$	(70 + $V_{(VS)}$)	
	CS+ to CS–	–1	100	V
	$\overline{FLT}$, FLT_GD to GND	–1	20	V
Sink current	$I_{(\overline{FLT})}$, $I_{(WAKE)}$		10	mA
	$I_{(CS+)}$, $I_{(CS–)}$, 1msec	–100	100	mA
Output Pins	PU, PD, G2, BST to GND	–65	112	V
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN/UVLO, VS, SCP_TEST)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	VS to GND	3.5		95	V
	Minimum voltage on VS pin for Short Circuit Protection	4			
	EN/UVLO, INP, CS_SEL to GND	0		65	
Output Pins	$\overline{FLT}$, WAKE to GND	0		15	V
External Capacitor	VS, SRC to GND	22			nF
	BST to SRC	0.1			µF
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC(1)		TPS4800-Q1 DGX 19 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

T_J = –40 °C to +125°C. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VS	Operating input voltage		3.5		95	V
$V_{(S\_PORR)}$	Input supply POR threshold, rising		1.78	2.5	3.27	V
$V_{(S\_PORF)}$	Input supply POR threshold, falling		1.71	2.36	3.1	V
	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V		46	55	µA
	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V, –40°C ≤ T_J ≤ +85°C			53	µA
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V		0.75	3.3	µA
$I_{(REV)}$	$I_{(VS)}$ leakage current during Reverse Polarity	0 V ≤ $V_{(VS)}$ ≤ – 65 V	19	22.4	37	µA
ENABLE, UNDERVOLTAGE LOCKOUT (EN/UVLO), SHORT CIRCUIT COMPARATOR TEST (SCP_TEST) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.176	1.23	1.287	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.09	1.136	1.184	V
$V_{(ENR)}$	Enable threshold voltage for low Iq shutdown, rising				1	V
$V_{(ENF)}$	Enable threshold voltage for low Iq shutdown, falling		0.3			V
$I_{(EN/UVLO)}$	Enable input leakage current	$V_{(EN/UVLO)}$ = 70 V	130		478	nA
$V_{(SCP\_TEST\_H)}$	SCP test mode rising threshold				2	V
$V_{(SCP\_TEST\_L)}$	SCP test mode falling threshold		0.8			V
$I_{(SCP\_TEST)}$	SCP_TEST input leakage current			90	700	nA
OVER VOLTAGE PROTECTION (OV) INPUT						
$V_{(OVR)}$	Overvoltage threshold input, risIng		1.171	1.225	1.278	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.088	1.138	1.186	V
$I_{(OV)}$	OV Input leakage current			86	200	nA
CHARGE PUMP (BST–SRC)						
$I_{(BST)}$	Charge Pump Supply current	$V_{(BST-SRC)}$ = 10 V, $V_{(EN/UVLO)}$ = 2 V	190	345	466	µA
$V_{(BST\_UVLOR)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, rising	$V_{(EN/UVLO)}$ = 2 V	8.1	9	9.9	V
$V_{(BST\_UVLOF)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, falling	$V_{(EN/UVLO)}$ = 2 V	7.28	8.2	8.9	V
$V_{(BST–SRC\_ON)}$	Charge Pump Turn ON voltage	$V_{(EN/UVLO)}$ = 2 V	9.3	10.3	11.4	V
$V_{(BST–SRC\_OFF)}$	Charge Pump Turn OFF voltage	$V_{(EN/UVLO)}$ = 2 V	10.4	11.6	12.8	V
$V_{(BST–SRC)}$	Charge Pump Voltage at $V_{(VS)}$ = 3.5 V	$V_{(EN/UVLO)}$ = 2 V	9.1	10.5	11.62	V

5.5 Electrical Characteristics (続き)

T_J = –40 ℃ to +125℃. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVER OUTPUTS (G1PU, G1PD)						
$I_{(PU)}$	Peak Source Current			1.69		A
$I_{(PD)}$	Peak Sink Current			2		A
$V_{(G\_GOOD)}$	VGS good threshold		5.5	7	8.3	V
SHORT CIRCUIT PROTECTION (ISCP)						
I_{SCP}	SCP Input Bias current		8.4	10	12.33	µA
$V_{(SCP)}$	SCP threshold	$R_{(ISCP)}$ = 140.5 kΩ		300		mV
		$R_{(ISCP)}$ = 28 kΩ	60	75	90	mV
		$R_{(ISCP)}$ = 10.5 kΩ	32	40	48	mV
		$R_{(ISCP)}$ = 500 Ω	15	20	25	mV
		$R_{(ISCP)}$ = Open			757	mV
$V_{(SCP)}$	SCP threshold with external bias on ISCP pin	$V_{(ISCP)}$ = 1.405 V	283	300	315	mV
		$V_{(ISCP)}$ = 280 mV	67.8	75	81.7	mV
		$V_{(ISCP)}$ = 105 mV	33.3	40	46.2	mV
DELAY TIMER (TMR)						
$I_{(TMR\_SRC\_CB)}$	TMR source current		67	87	104	µA
$I_{(TMR\_SRC\_FLT)}$	TMR source current		1.4	2.73	3.8	µA
$I_{(TMR\_SNK)}$	TMR sink current		2.17	2.8	3.4	µA
$V_{(TMR\_SC)}$			0.93	1.1	1.2	V
$V_{(TMR\_LOW)}$			0.15	0.21	0.25	V
$N_{(A\text{-}R\ Count)}$				32		
INPUT CONTROL (INP), FAULT FLAGS ($\overline{FLT}$, FLT_GD)						
$R_{(\overline{FLT})}$, $R_{(FLT\_GD)}$	$\overline{FLT}$, FLT_GD Pull-down resistance		53	85	107	Ω
$I_{(\overline{FLT})}$, $I_{(FLT\_GD)}$	$\overline{FLT}$, FLT_GD Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 20 V			410	nA
$V_{(INP\_H)}$					2	V
$V_{(INP\_L)}$			0.8			V
$I_{(INP)}$	INP Input leakage current			89	206	nA
$V_{(CS\_SEL\_H)}$	CS_SEL threshold for low side sensing		1.35		2	V
$V_{(CS\_SEL\_L)}$	CS_SEL threshold for high side sensing		0.8		1.36	V
$I_{(CS\_SEL)}$	CS_SEL Input leakage current		10	88.8	200	nA

5.6 Switching Characteristics

T_J = –40 ℃ to +125℃. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PU(INP\_H)}$	INP Turn ON propogation Delay	INP ↑ to PU ↑, C_L = 47 nF	0.32		1.53	µs
$t_{PD(INP\_L)}$	INP Turn OFF propogation Delay	INP ↓ to PD ↓, C_L = 47 nF		0.36	1	µs
$t_{PD(EN\_OFF)}$	EN Turn OFF Propogation Delay	EN ↓ to PD ↓, C_L = 47 nF	2.2	4.6	6	µs
$t_{PD(UVLO\_OFF)}$	UVLO Turn OFF Propogation Delay	UVLO ↓ to PD ↓ and $\overline{FLT}$ ↓, C_L = 47 nF	2.8	4.8	6	µs
$t_{PD(OV\_OFF)}$	OV Turn Off progopation Delay	OV ↑ to PD ↓ and $\overline{FLT}$ ↓, C_L = 47 nF		4.5	5.4	µs
t_{SC}	Hard Short-circuit protection propogation delay	$V_{(CS+-CS-)}$ ↑ $V_{(SCP)}$ to PD ↓, CL = 47 nF, $C_{(TMR)}$ = Open			4	µs

5.6 Switching Characteristics (続き)

T_J = –40 ℃ to +125℃. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SC_PUS}	Short-circuit protection propogation delay during power up with output short circuit	C_{TMR} = Open			10	µs
$t_{PD(\overline{FLT}\_SC)}$	$\overline{FLT}$ assertion delay during short circuit	$V_{(CS+-CS-)}$ ↑ $V_{(SCP)}$ to $\overline{FLT}$ ↓, $C_{(TMR)}$ = Open		10.5	15	µs
F_{ISCP}	ISCP Pulse current frequency			1.18		kHz
$t_{PD(FLT\_GD)}$	FLT assertion delay during Gate Drive UVLO	$V_{(PU-SRC)}$ ↑ $V_{(BSTUVLOR)}$ to FLT_GD ↓		120		µs
$t_{PD(FLT\_GD)}$	FLT de-assertion delay during Gate Drive UVLO	$V_{(PU-SRC)}$ ↓ $V_{(BSTUVLOR)}$ to FLT_GD ↑		127		µs

5.7 Typical Characteristics

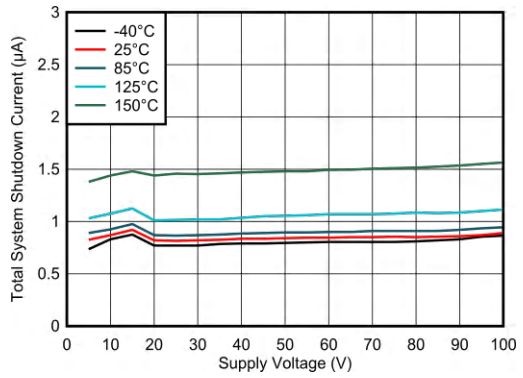


図 5-1. Shutdown Supply Current vs Supply Voltage

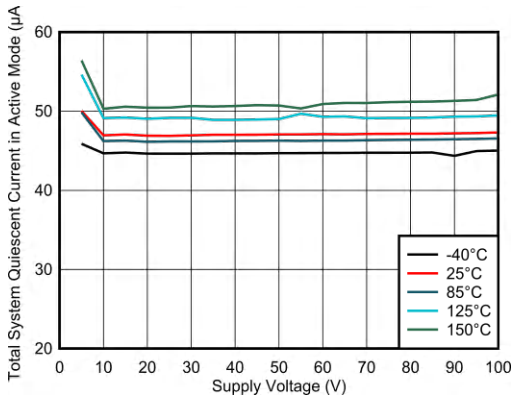


図 5-2. Operating Quiescent Current in Active Mode vs Supply Voltage

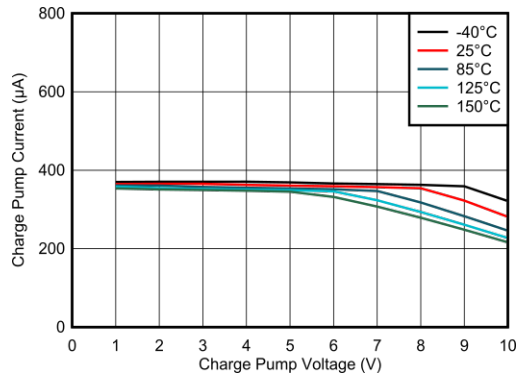
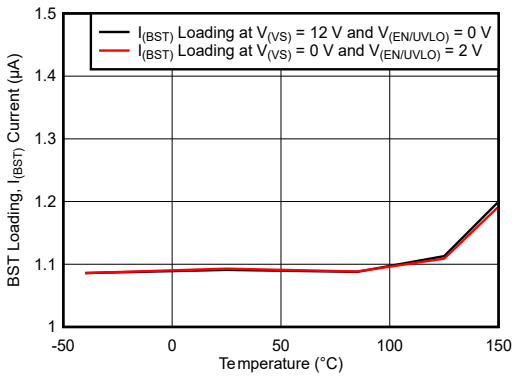


図 5-3. Charge Pump Current vs Charge Pump Voltage



$V_{(BST)}$ = 15 V $V_{(SRC)}$ = 0 V

図 5-4. BST Loading Current ($I_{(BST)}$) vs Temperature

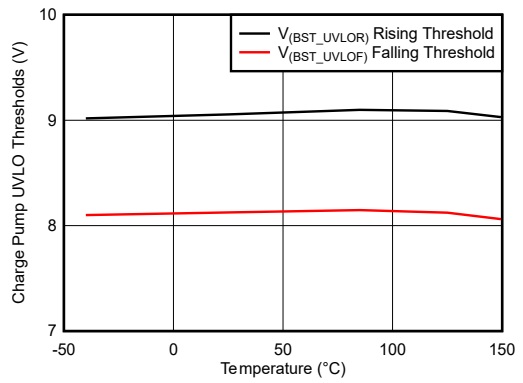


図 5-5. Charge Pump UVLO Thresholds vs Temperature

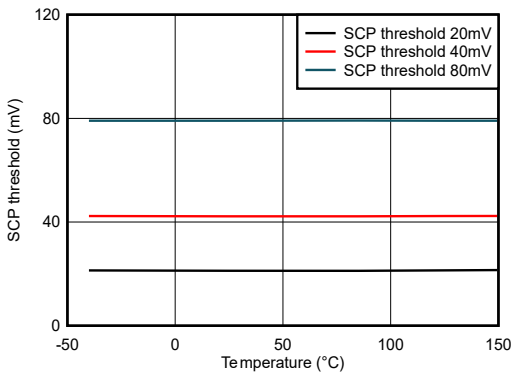


図 5-6. Short-Circuit Threshold ($V_{(SCP)}$) vs Temperature

5.7 Typical Characteristics (continued)

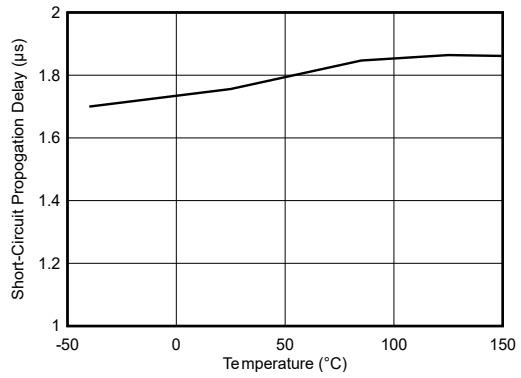


図 5-7. Short Circuit Protection Response Time (t_{SC}) vs Temperature

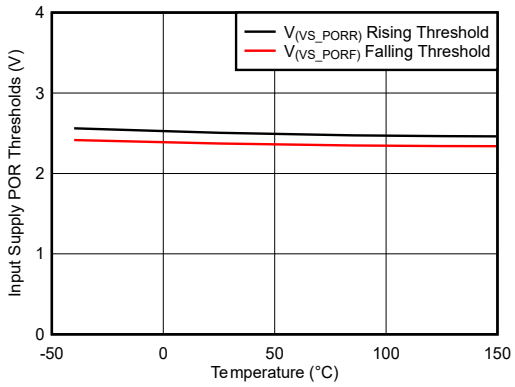


図 5-8. Input Supply POR Thresholds vs Temperature

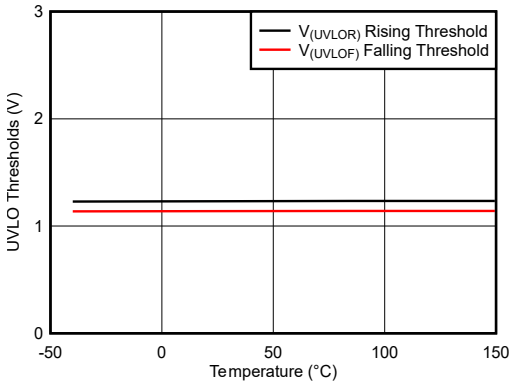


図 5-9. Input Supply UVLO Thresholds vs Temperature

6 Parameter Measurement Information

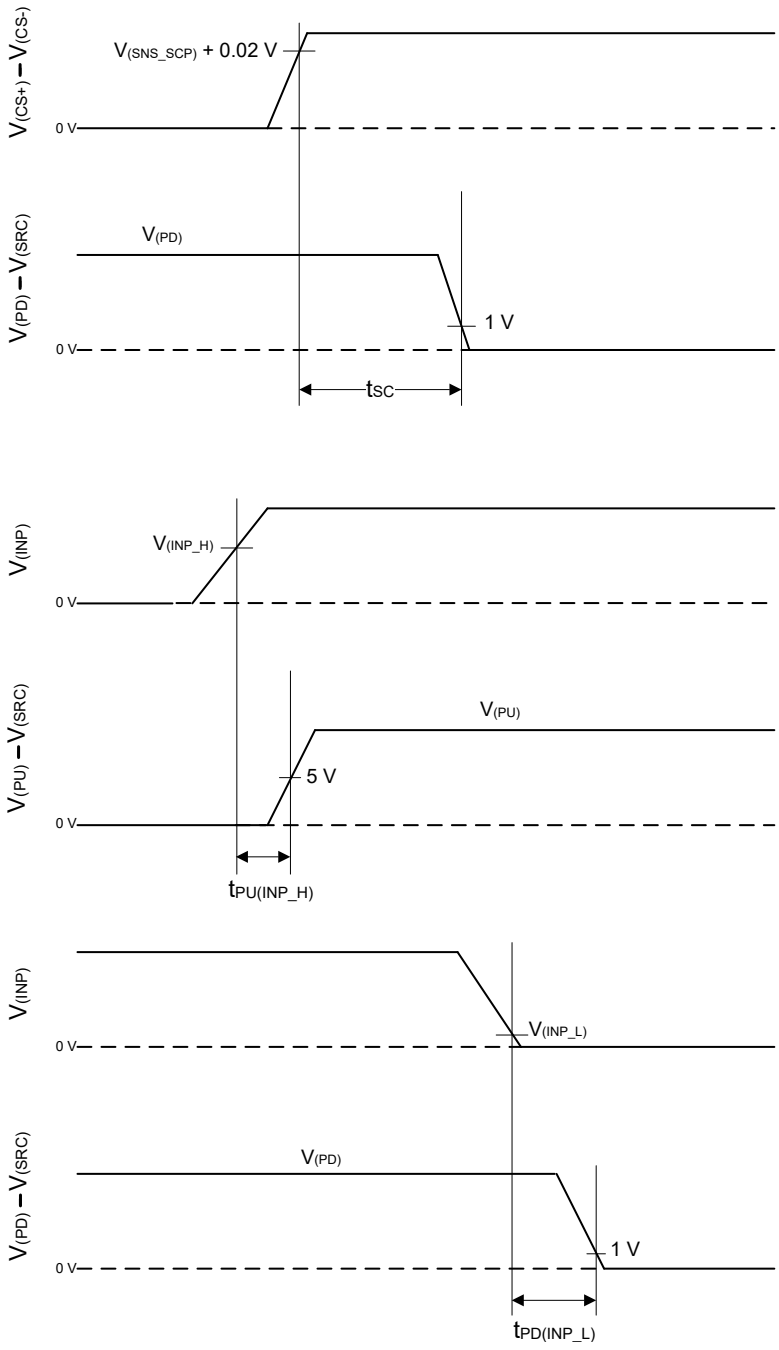


図 6-1. Timing Waveforms

7 Detailed Description

7.1 Overview

The TPS48000-Q1 is a 100-V low IQ smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5 V–95V, the device is suitable for 12V, 24V and 48V system designs. The device can withstand and protect the loads from negative supply voltages down to –65V.

It has a strong 1.69A/2A peak source/sink gate driver that enables power switching using parallel FETs in high current system designs.

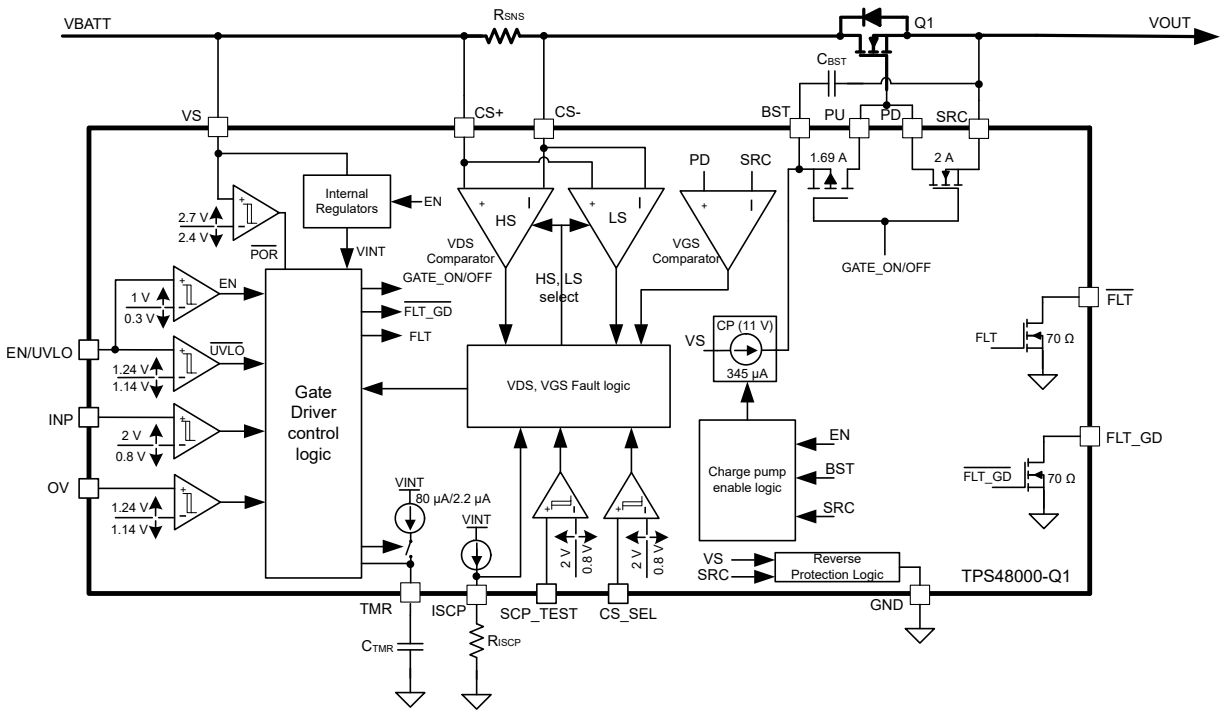
The device provides configurable short circuit protection using ISCP and TMR pins for adjusting the threshold and response time respectively. Auto-retry and latch-off fault behavior can be configured. With TPS48000-Q1, current sensing an be done either by an external sense resistor or by MOSFET VDS sensing. High side or low side current sense resistor configuration is possible by using CS_SEL pin input. Diagnosis of the integrated short circuit comparator is possible using external control on SCP_TEST input.

The device has adjustable under voltage and overvoltage protection.

The device indicates fault ($\overline{\text{FLT}}$) on open drain output during during short circuit and input under voltage, overvoltage conditions. It also have a dedicate fault indication (FLT_GD) to indicate the gate drive UVLO condition.

Low Quiescent Current 43µA (typical) in operation enables always ON system designs. Quiescent current reduces to 1.5µA (typical) with EN/UVLO low.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Charge Pump and Gate Driver Output (VS, PU, PD, BST, SRC)

図 7-1 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 1.69A/2A peak source/sink gate driver (PU, PD) for driving power FET. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 11V, 345µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, C_{BST} that is placed across the gate driver (BST and SRC).

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the C_{BST} capacitor. After the voltage across C_{BST} crosses $V_{(BST\_UVLOR)}$, the GATE driver section is activated. The device has a 1V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Choose C_{BST} based on the external FET Q_G and allowed dip during FET turn-ON. The charge pump remains enabled until the BST to SRC voltage reaches 11.8V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 10V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between 11.8V and 10V as shown in the 図 7-2.

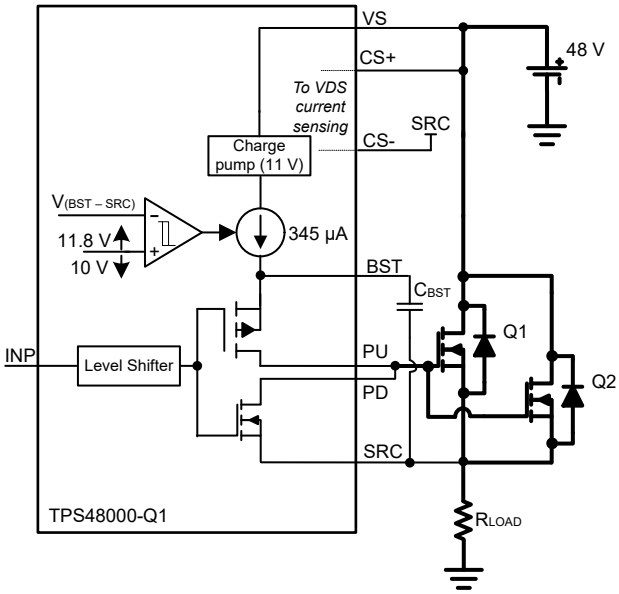


図 7-1. Gate Driver

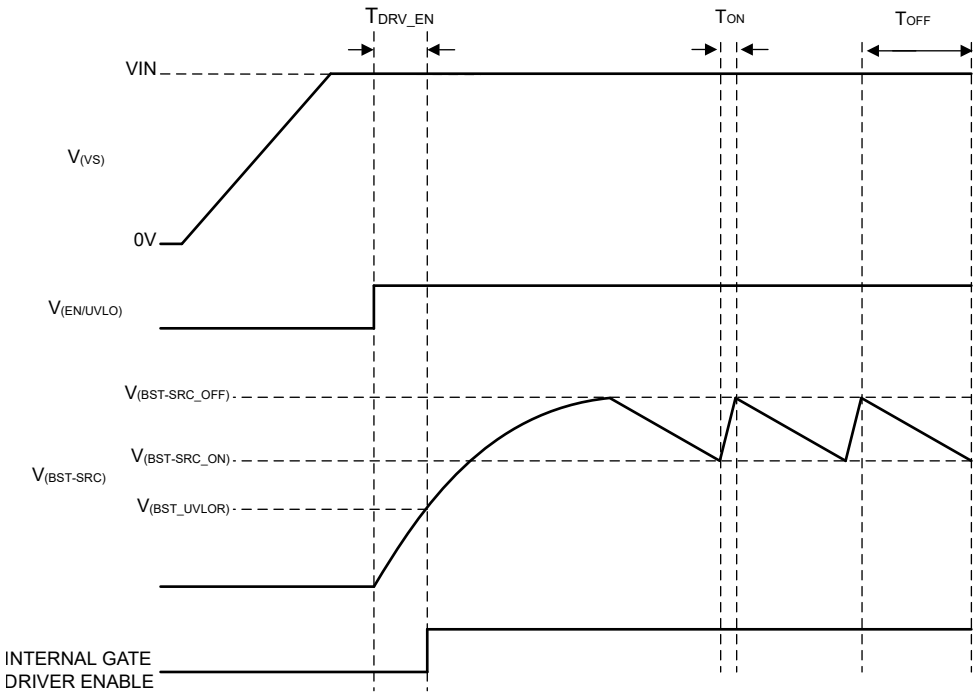


図 7-2. Charge Pump Operation

Use the following equation to calculate the initial gate driver enable delay:

$$T_{DRV\_EN} = \frac{C_{BST} \times V_{(BST\_UVLOR)}}{345\ \mu A} \quad (1)$$

Where,

C_{BST} is the charge pump capacitance connected across BST and SRC pins.

$V_{(BST\_UVLOR)}$ = 9.5V (max).

If T_{DRV_EN} must be reduced then pre-bias BST terminal externally using an external V_{AUX} supply through a low leakage diode D_1 as shown in 図 7-3. With this connection, T_{DRV_EN} reduces to 400µs. TPS48000-Q1 application circuit with external supply to BST is shown in 図 7-3.

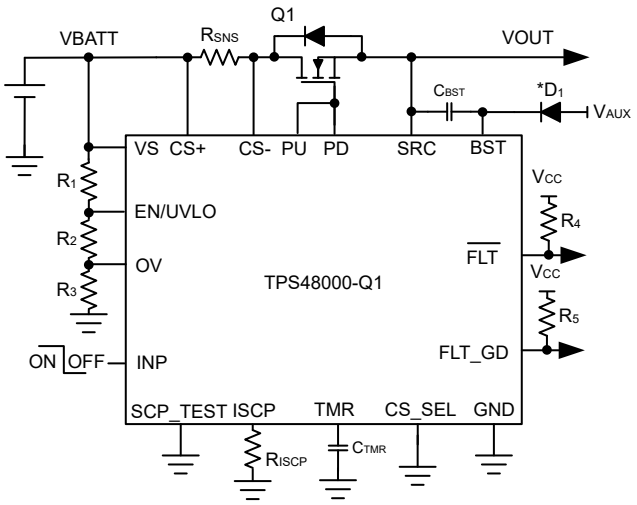


図 7-3. TPS48000-Q1 Application Circuit With External Supply to BST

注

V_{AUX} can be supplied by external regulated supply ranging between 8V and 18V.

7.3.2 Capacitive Load Driving Using FET Gate (PU, PD) Slew Rate Control

Certain end equipments like automotive power distribution unit power different loads including other ECUs. These ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur potentially damaging the power FETs. To limit the inrush current during capacitive load switching, the following system design technique can be used with TPS48000-Q1.

For limiting inrush current during turn ON of the FET with capacitive loads, use R_1, R_2, C_1 as shown in 図 7-4. The R_1 and C_1 components slow down the voltage ramp rate at the gate of the FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

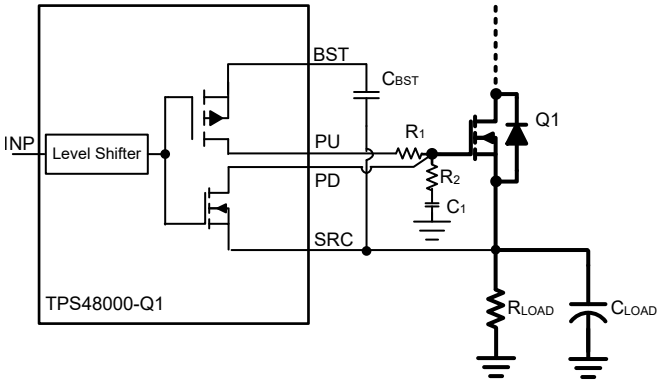


図 7-4. Inrush Current limiting

Use the 式 2 to calculate the inrush current during turn-ON of the FET.

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \quad (2)$$

$$C_1 = \frac{0.63 \times V_{(BST\ -\ SRC)} \times C_{LOAD}}{R_1 \times I_{INRUSH}} \quad (3)$$

Where,

C_{LOAD} is the load capacitance,

VBATT is the input voltage and T_{charge} is the charge time,

$V_{(BST-SRC)}$ is the charge pump voltage (11V),

Use a damping resistor R_2 (~ 10Ω) in series with C_1. 式 3 can be used to compute required C_1 value for a target inrush current. A 100kΩ resistor for R_1 can be a good starting point for calculations.

Connecting PD pin of TPS48000-Q1 directly to the gate of the external FET ensures fast turn OFF without any impact of R_1 and C_1 components.

C_1 results in an additional loading on C_{BST} to charge during turn-ON. Use below equation to calculate the required C_{BST} value:

$$C_{BST} = \frac{Q_{g(total)}}{\Delta V_{BST}} + 10 \times C_1 \quad (4)$$

Where,

$Q_{g(total)}$ is the total gate charge of the FET.

ΔV_{BST} (1V typical) is the ripple voltage across BST to SRC pins.

7.3.3 Short-Circuit Protection

The TPS48000-Q1 feature adjustable short circuit protection. The threshold and response time can be adjusted using R_{ISCP} resistor and C_{TMR} capacitor respectively. The device senses the voltage across CS+ and CS– pins. These pins can be connected across the FET drain and source terminals for FET R_{DSON} sensing or across an external high and low side current sense resistor (R_{SNS}) as shown in 図 7-5, 図 7-6, , 図 7-7 and 図 7-8 respectively.

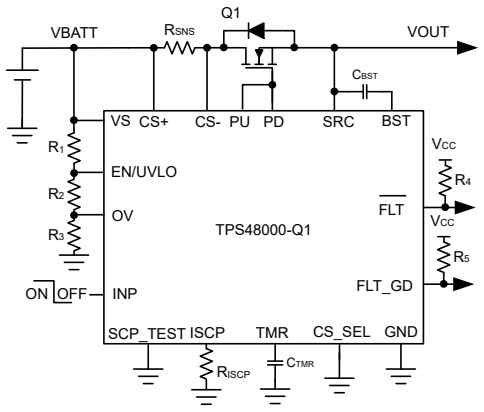


図 7-5. TPS48000-Q1 Application Circuit With External Sense Resistor RSNS Based High Side Current Sensing

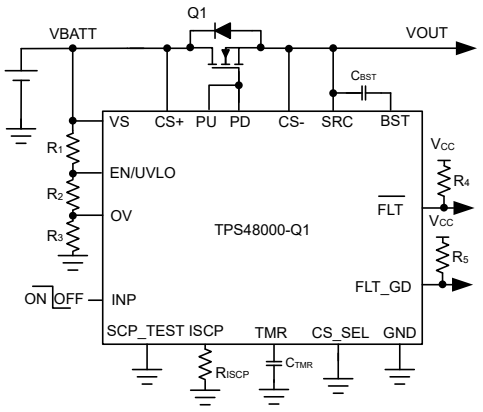


図 7-6. TPS48000-Q1 Application Circuit With MOSFET RDSON Based Current Sensing

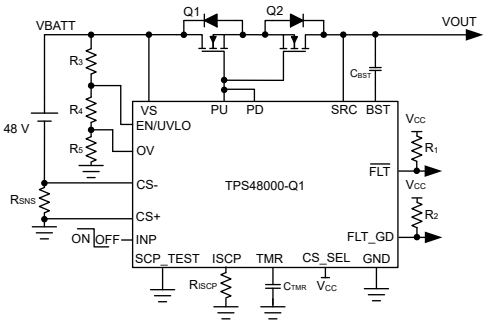


図 7-7. TPS48000-Q1 Application Circuit With External Sense Resistor RSNS Based Low Side Current Sensing on Battery Side

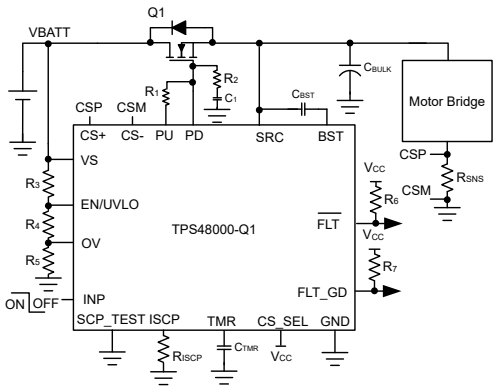


図 7-8. TPS48000-Q1 Application Circuit With External Sense Resistor RSNS Based Low Side Current Sensing

Set the short-circuit detection threshold using an external R_{ISCP} resistor across ISCP and GND pins. Use 式 5 to calculate the required R_{ISCP} value:

$$R_{ISCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{SNS} - 19\ mV\right)}{2\ \mu A} \quad (5)$$

Where,

R_{SNS} is the high or low side current sense resistor value or the FET R_{DSON} value.

I_{SC} is the desired short circuit current level.

The short circuit protection response is fastest with no C_{TMR} cap connected across TMR and GND pins.

With device powered ON and EN/UVLO, INP pulled high, During Q_1 turn ON, first VGS of external FET is sensed by monitoring the voltage across PD to SRC. Once PD to SRC voltage raises above $V_{(G\_GOOD)}$ (7.5V typical) threshold which ensures that the external FET is enhanced, then the SCP comparator output is monitored. If the sensed voltage across CS+ and CS– exceeds the short-circuit set point (V_{SCP}), PD pulls low to SRC and $\overline{FLT}$ asserts low. Subsequent events can be set either to be auto-retry or latch off as described in following sections.

VGS of external FET (Q_1) is only monitored when CS_SEL is pulled low. VGS of external FET (Q_1) is not monitored for low side current sensing as shown in 図 7-7 and 図 7-8.

注

Short-circuit threshold can also be set by connecting external bias voltage on ISCP pin via buffer instead of R_{ISCP} resistor enabling system design with improved SCP threshold accuracy as mentioned in electrical characteristics table. The external bias voltage to be forced on ISCP pin can be calculated by below eqaution:

$V_{(SCP\_BIAS)}$ in mV = I_{SC} x R_{SNS} x 5 - 95mV

7.3.3.1 Short-Circuit Protection With Auto-Retry

The C_{TMR} programs the short-circuit protection delay (t_{SC}) and auto-retry time (t_{RETRY}). Once the voltage across CS+ and CS– exceeds the set point, the C_{TMR} starts charging with 80µA pull-up current.

After C_{TMR} charges to $V_{(TMR\_SC)}$, PD pulls low to SRC and $\overline{FLT}$ asserts low providing warning on impending FET turn OFF. Post this event, the auto-retry behavior starts. The C_{TMR} capacitor starts discharging with 2.5uA pulldown current. After the voltage reaches $V_{(TMR\_LOW)}$ level, the capacitor starts charging with 2.2uA pullup. After 32 charging-discharging cycles of C_{TMR} the FET turns ON back and $\overline{FLT}$ de-asserts.

The device retry time (t_{RETRY}) is based on C_{TMR} for the first time as per 式 7.

Use 式 6 to calculate the C_{TMR} capacitor to be connected across TMR and GND.

$$C_{TMR} = \frac{I_{TMR} \times t_{SC}}{1.1} \quad (6)$$

Where,

I_{TMR} is internal pull-up current of 80µA.

t_{SC} is desired short-circuit response time.

Leave TMR floating for fastest short-circuit response time.

$$t_{RETRY} = 22.7 \times 10^{6} \times C_{TMR} \quad (7)$$

If the short-circuit pulse duration is below t_{SC} then the FET remains ON and C_{TMR} gets discharged using internal pull down switch.

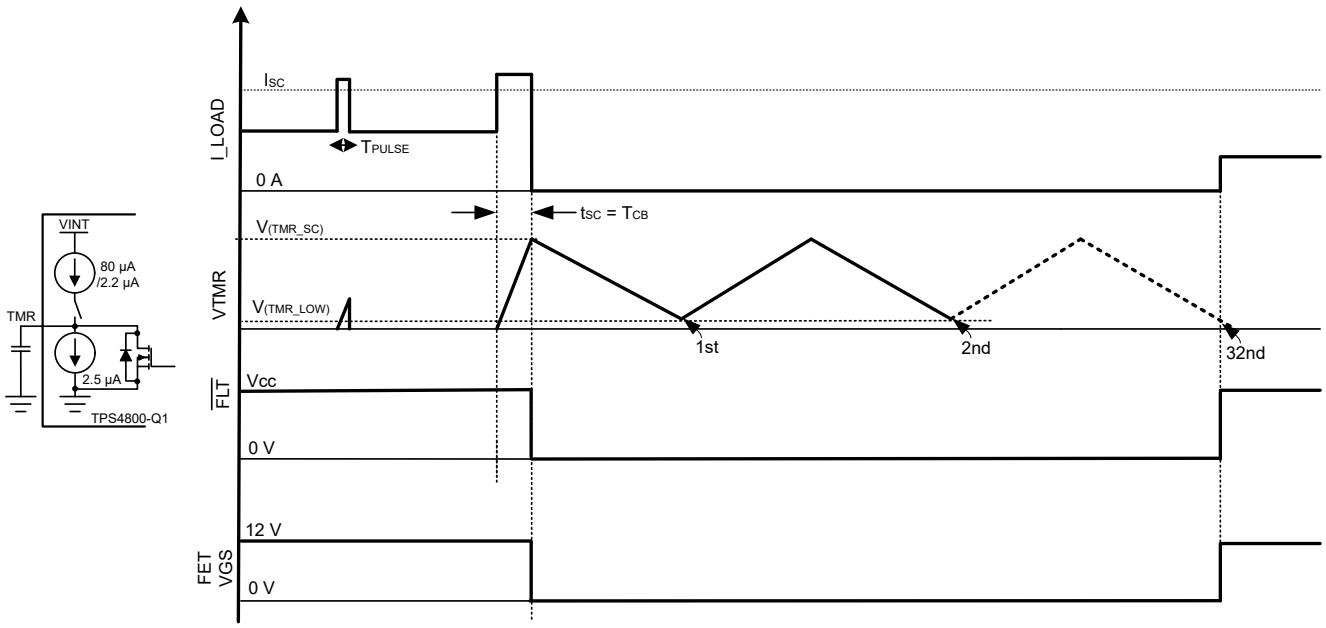


図 7-9. Short-Circuit Protection With Auto-Retry

7.3.3.2 Short-Circuit Protection With Latch-Off

Connect an approximately 100kΩ resistor across C_{TMR} as shown in . With this resistor, during the charging cycle, the voltage across C_{TMR} gets clamped to a level below $V_{(TMR\_SC)}$ resulting in a latch-off behavior and $\overline{FLT}$ asserts low at same time.

Use 式 8 to calculate C_{TMR} capacitor to be connected between TMR and GND for R_{TMR} = 100kΩ.

$$C_{TMR} = \frac{t_{SC}}{R_{TMR} \times \ln\left(\frac{1}{1 - \frac{1.1}{R_{TMR} \times 80\ \mu A}}\right)} \quad (8)$$

Where,

I_{TMR} is internal pull-up current of 80µA.

t_{SC} is desired short-circuit response time.

Toggle INP or EN/UVLO (below $V_{(ENF)}$) or power cycle VS below $V_{(VS\_PORF)}$ to reset the latch. At low edge, the timer counter is reset and C_{TMR} is discharged. PU pulls up to BST when INP is pulled high.

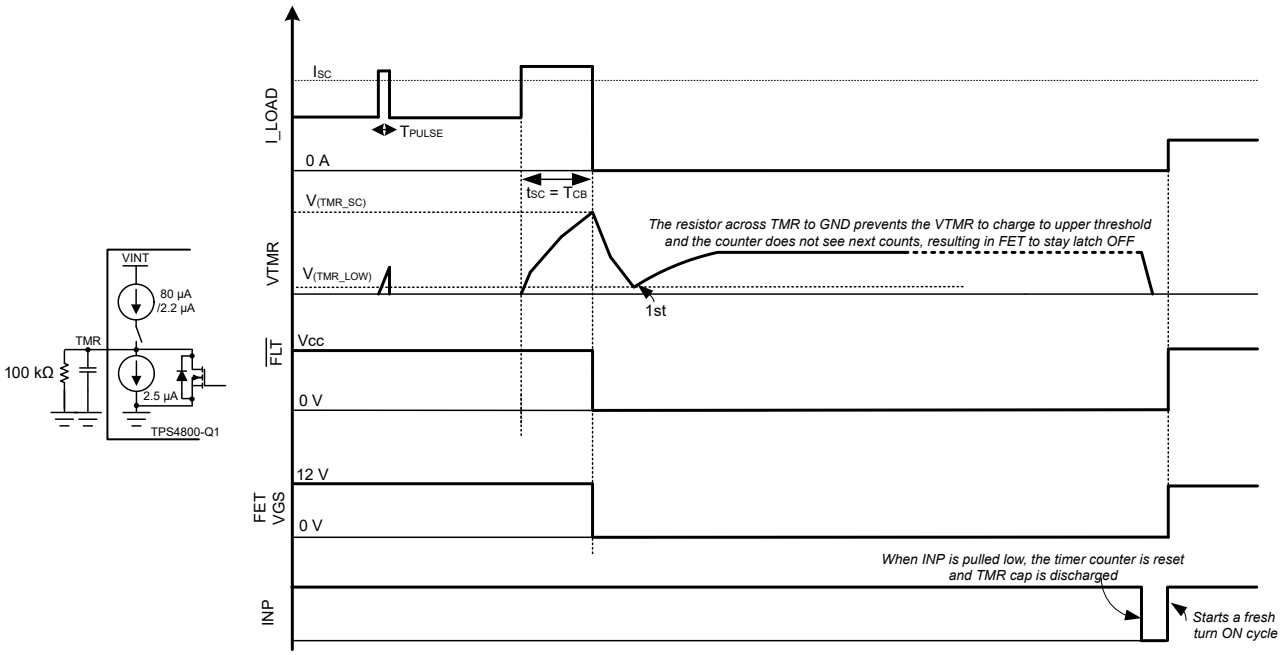


図 7-10. Short-Circuit Protection With Latch-Off

7.3.4 Overvoltage (OV) and Undervoltage Protection (UVLO)

TPS48000-Q1 has an accurate undervoltage protection (< ±2%) using EN/UVLO pin and an accurate overvoltage protection (< ±2%), providing robust load protection. $\overline{FLT}$ is asserted when input undervoltage or overvoltage fault is detected. Connect a resistor ladder as shown in 図 7-11 for undervoltage and overvoltage protection threshold programming.

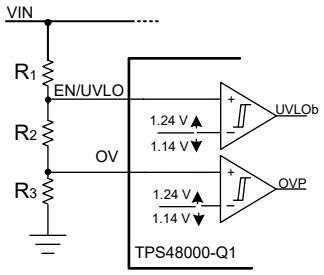


図 7-11. Programming Overvoltage and Undervoltage Protection Threshold

7.3.5 Reverse Polarity Protection

The TPS48000-Q1 devices features integrated reverse polarity protection to protect the device from failing during input and output reverse polarity faults. Reverse polarity faults can occur during jump start, installation and maintenance of the end equipment's.

The device is tolerant to reverse polarity voltages down to -65V both on input and output.

On the output side, the device can see transient negative voltages during regular operation due to output cable harness inductance kickbacks when the switches are turned OFF. In such systems, the output negative voltage level is limited by the output side TVS or a diode.

7.3.6 Short-Circuit Protection Diagnosis (SCP_TEST)

In the safety critical designs, short-circuit protection (SCP) feature and its diagnosis is important.

The TPS48000-Q1 features the diagnosis of the internal short circuit protection. When SCP_TEST is driven low to high then, a voltage is applied internally across the SCP comparator inputs to simulate a short circuit event. The comparator output controls the gate drive (PU/PD) and also the $\overline{\text{FLT}}$. If the gate drive goes low (with initially being high) and $\overline{\text{FLT}}$ alos goes low then it indicates that the SCP is good otherwise it is to be treated as SCP feature is not functional.

If the SCP_TEST feature is not used, then connect SCP_TEST pin to GND.

7.3.7 TPS48000-Q1 as a Simple Gate Driver

図 7-12 shows application schematics of TPS48000-Q1 as a simple gate driver in load disconnect switch as well as back-to-back FETs driving topologies. The short-circuit protection feature is disabled.

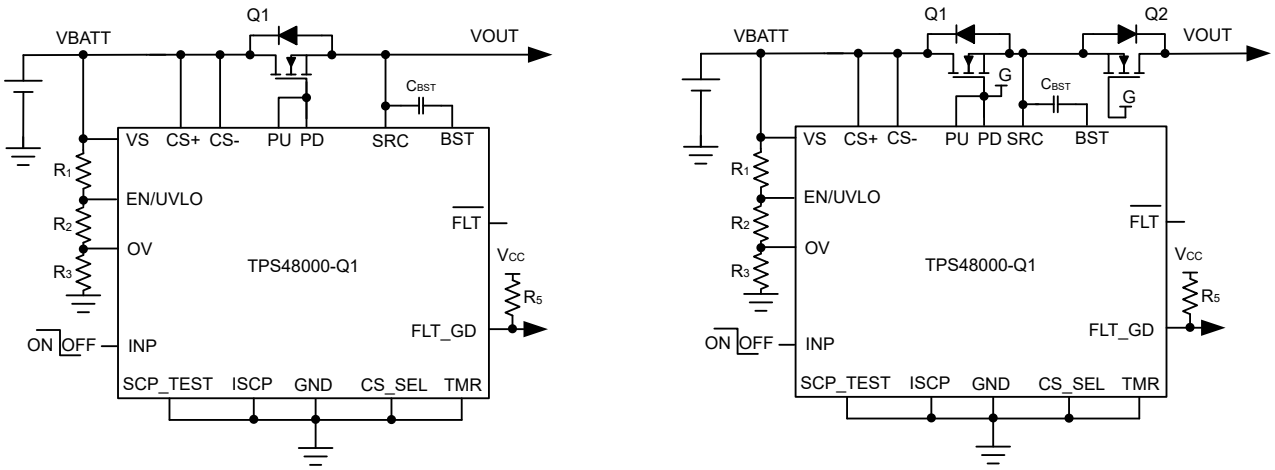


図 7-12. TPS48000-Q1 Application Circuit for Simple Gate Driver Design

7.4 Device Functional Modes

The TPS48000-Q1 has two modes of operation. Active mode and low IQ shutdown mode.

If the EN/UVLO pin voltage is greater than $V_{(ENR)}$ rising threshold, then the device is in active mode. In active state the internal charge pump is enabled, gate drivers, all the protection and diagnostic features are enabled.

If the EN/UVLO voltage is pulled below $V_{(ENF)}$ falling threshold, the device enters into low IQ shutdown mode. In this mode, the charge pump, gate drivers and all the protection features are disabled. The gate drive and external FETs turn OFF. The TPS48000-Q1 consumes low IQ of 1.5 µA (typical) in this mode.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS48000-Q1 is a 100V low IQ smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5 V–95V, the device is suitable for 12V, 24V and 48V system designs. The device can withstand and protect the loads from negative supply voltages down to –65V. It has strong 1.69A/2A peak source/sink gate driver enabling power switching using parallel FETs in high current system designs.

The device provides configurable short circuit protection using ISCP and TMR pins for adjusting the threshold and response time respectively. Auto-retry and latch-off fault behavior can be configured. With TPS48000-Q1, current sensing can be done either by an external sense resistor or by MOSFET VDS sensing. High or low side current sense resistor configuration is possible by using CS_SEL pin input.

Diagnosis of the integrated short circuit comparator can be done using external control on SCP_TEST input.The device indicates fault ($\overline{FLT}$) on open drain output during during short circuit and input under voltage, overvoltage conditions. It also have a dedicate fault indication (FLT_GD) to indicate the gate drive UVLO condition.

Low Quiescent Current 43µA operation enables always ON system designs. Quiescent current reduces to 1.5µA (typical) with EN/UVLO low.

8.2 Typical Application: Driving Power at all Times (PAAT) Loads

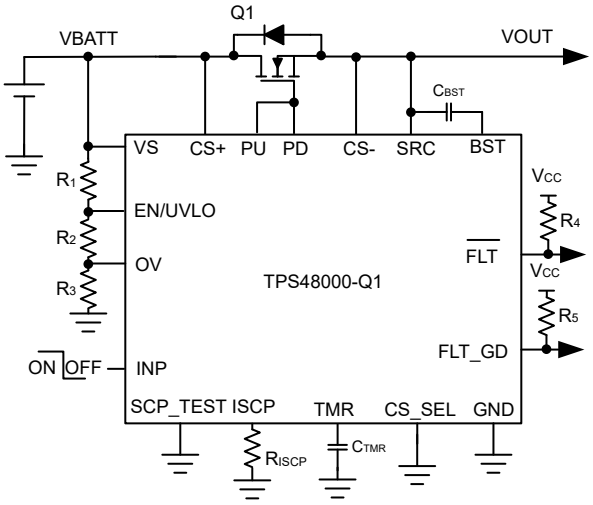


図 8-1. TPS48000-Q1 Application Circuit for driving PAAT loads with VDS based Current Sensing

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
Input Voltage Range, V_{IN}	16 to 60V
Undervoltage lockout set point, VIN_{UVLO}	16V
Overvoltage set point, VIN_{OVP}	60V
Maximum load current, I_{OUT}	20A
Short-circuit protection threshold, I_{SC}	60A
Fault timer period, t_{SC}	50µs
Fault response	Auto-Retry
Current sensing	MOSFET VDS

8.2.2 Detailed Design Procedure

Selection of MOSFET, Q_1

For selecting the MOSFET Q_1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application. Considering 60V as the maximum application voltage due to load dump, MOSFETs with V_{DS} voltage rating of 80V is chosen for this application.

The maximum V_{GS} TPS48000-Q1 can drive is 11V, so a MOSFET with 15V minimum V_{GS} rating must be selected.

To reduce the MOSFET conduction losses, an appropriate $R_{DS(ON)}$ is preferred.

Based on the design requirements, IAUS200N08S5N023 is selected and its ratings are:

- 80V $V_{DS(MAX)}$ and ±20V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 2.3mΩ typical at 10V V_{GS}
- MOSFET $Q_{g(total)}$ is 85nC typical

TI recommends to make sure that the short-circuit conditions such max V_{IN} and I_{SC} are within SOA of selected FET (Q_1) for at-least > t_{SC} timing.

Selection of Bootstrap Capacitor, C_{BST}

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 345µA. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving IAUS200N08S5N023 MOSFET

$$C_{BST} = \frac{Q_{g(total)}}{1\,V} = 85\,nF \tag{9}$$

Choose closest available standard value: 100nF, 10%.

Programming the Short-Circuit Protection Threshold – R_{ISCP} Selection

The R_{ISCP} sets the short-circuit protection threshold, whose value can be calculated using below equation:

$$R_{ISCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{DS\_ON} - 19\,mV\right)}{2\,\mu A} \tag{10}$$

To set 60 A as short-circuit protection threshold, R_{ISCP} value is calculated to be 50.5kΩ.

Choose the closest available standard value: 51kΩ, 1%.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS+ and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add placeholder for RC filter components across sense resistor (R_{SNS}) and tweak the values during test in the real system. The RC filter components should not be used in current sense designs by MOSFET VDS sensing to avoid impact on the short-circuit protection response.

Programming the Fault timer Period – C_{TMR} Selection

For the design example under discussion, overcurrent transients are allowed for 50µs duration. This blanking interval, t_{SC} (or circuit breaker interval, T_{CB}) can be set by selecting appropriate capacitor C_{TMR} from TMR pin to ground. The value of C_{TMR} to set 50µs for t_{SC} can be calculated using following equation:

$$C_{TMR} = \frac{80\ \mu A \times t_{SC}}{1.1} \quad (11)$$

Choose closest available standard value: 3.3nF, 10%.

Setting the Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage set point are adjusted using an external voltage divider network of R_1, R_2 and R_3 connected between VS, EN/UVLO, OV and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving 式 12 and 式 13.

$$V_{(OVR)} = \frac{R_3}{(R_1 + R_2 + R_3)} \times VIN_{OVP} \quad (12)$$

$$V_{(UVLOR)} = \frac{R_2 + R_3}{(R_1 + R_2 + R_3)} \times VIN_{UVLO} \quad (13)$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for R_1, R_2 and R_3. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I(R_{123})$ must be chosen to be 20 times greater than the leakage current of UVLO and OV pins.

From the device electrical specifications, $V_{(OVR)}$ = 1.24V and $V_{(UVLOR)}$ = 1.24V. From the design requirements, VIN_{OVP} is 60V and VIN_{UVLO} is 16V. To solve the equation, first choose the value of R_1 = 470kΩ and use 式 12 to solve for (R_2 + R_3) = 39.5kΩ. Use 式 13 and value of (R_2 + R_3) to solve for R_3 = 10.5kΩ and finally R_2 = 29kΩ. Choose the closest standard 1% resistor values: R_1 = 470kΩ, R_2 = 29.4kΩ, and R_3 = 10kΩ.

8.2.3 Application Curves

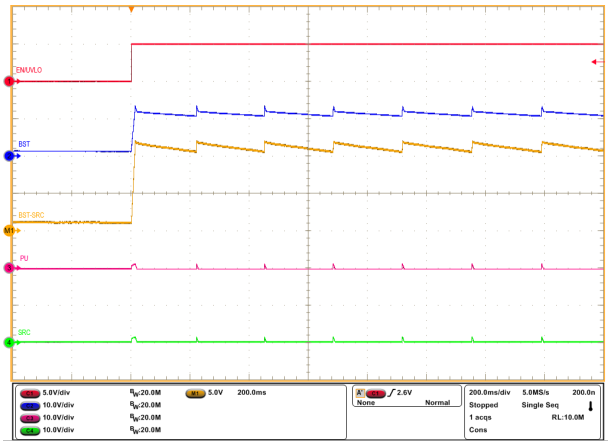


図 8-2. Start-Up Profile of Bootstrap Voltage with INP = GND and C_{BST} = 470nF

図 8-3. Start-Up Profile of Bootstrap Voltage with INP = HIGH and C_{BST} = 470nF

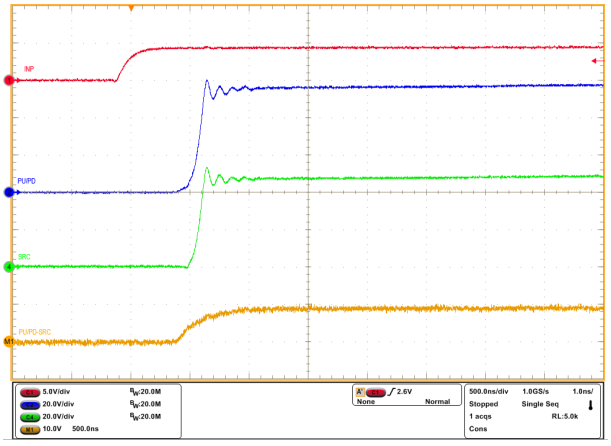


図 8-4. Turn-ON Response of TPS48000-Q1 for INP -> LOW to HIGH and C_{BST} = 470nF

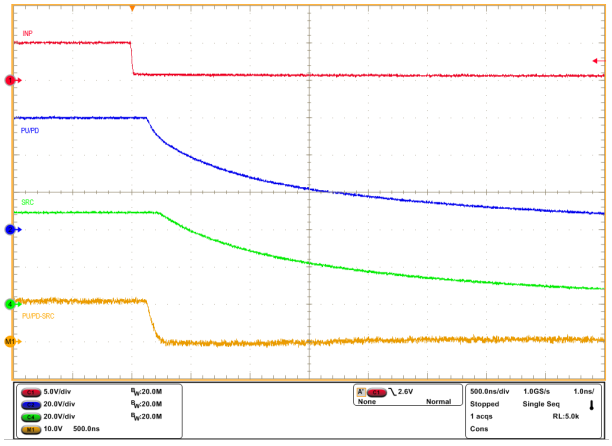


図 8-5. Turn-OFF Response of TPS48000-Q1 for INP -> HIGH to LOW and C_{BST} = 470nF

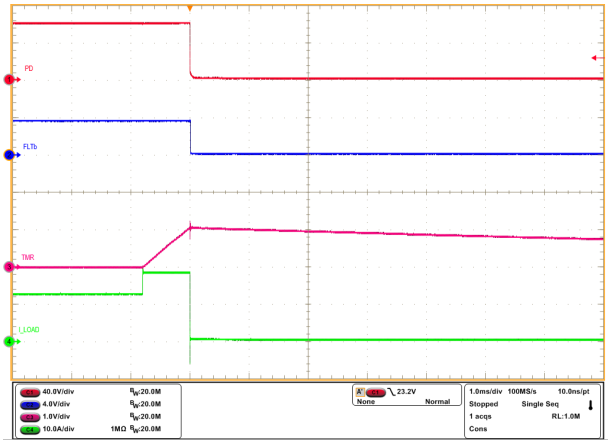


図 8-6. Overcurrent Response of TPS48000-Q1 for a Load Step from 12A to 18A with 15A Shortcircuit Protection Setting and t_{sc} = 1ms

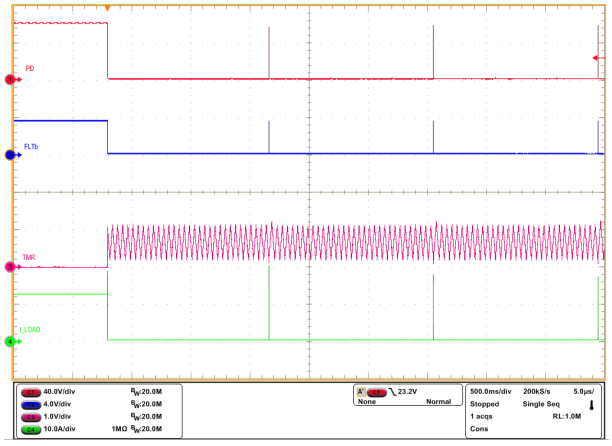


図 8-7. Auto-Retry Response of TPS48000-Q1 for an Overcurrent Fault

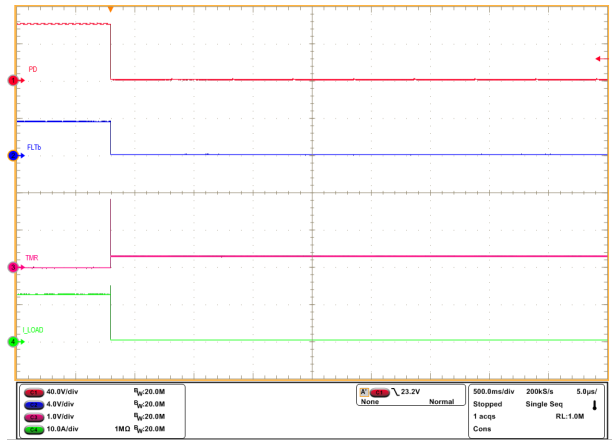


図 8-8. Latch-Off Response of TPS48000-Q1 for an Overcurrent Fault

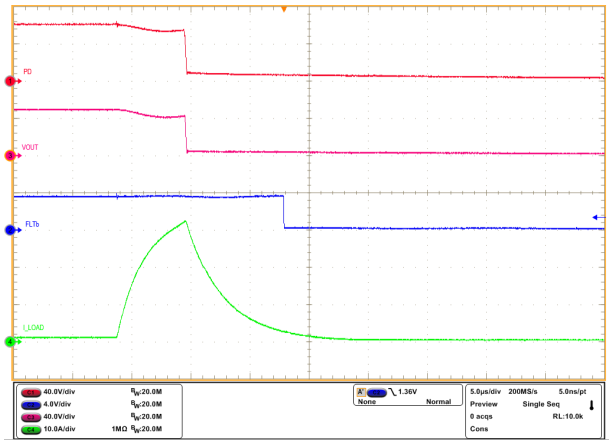


図 8-9. Output Short-Circuit Response of TPS48000-Q1 Device with 15A Shortcircuit Protection Setting and TMR = OPEN

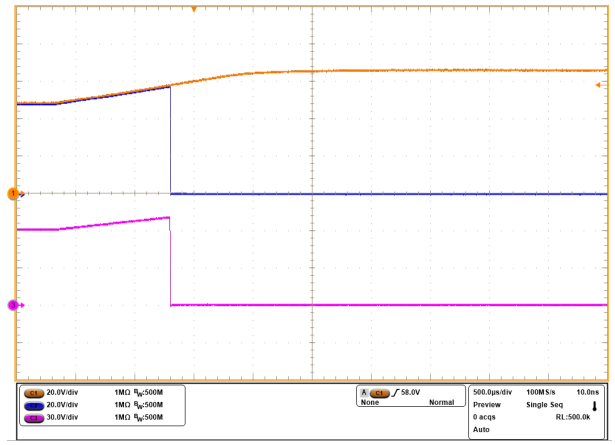


図 8-10. Overvoltage Cutoff Response of TPS48000-Q1 at 58V Level

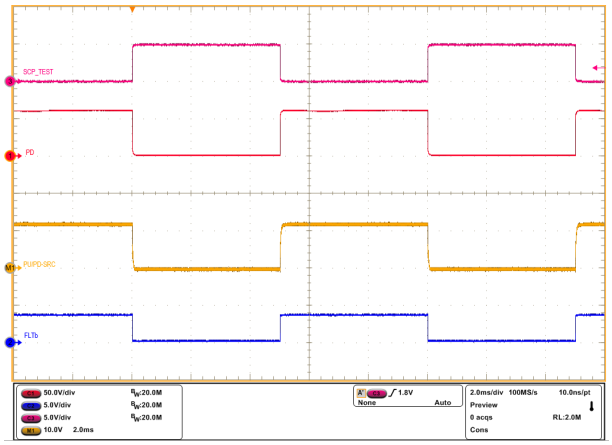


図 8-11. Short-Circuit Protection Diagnosis Test Response of TPS48000-Q1

8.3 Power Supply Recommendations

When the external MOSFETs turn-OFF during the conditions such as INP1 control, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS48000-Q1 gets powered from the VS pin. Voltage at this pin must be maintained above $V_{(VS\_PORR)}$ level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place a R_{VS} – C_{VS} filter between the input supply line and VS pin to filter out the supply noise. TI recommends R_{VS} value around 100Ω.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS+ and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add placeholder for RC filter components across sense resistor (R_{SNS}) and tweak the values during test in the real system. The RC filter components must not be used in current sense designs by MOSFET VDS sensing to avoid impact on the short-circuit protection response.

The following figure shows the circuit implementation with optional protection components.

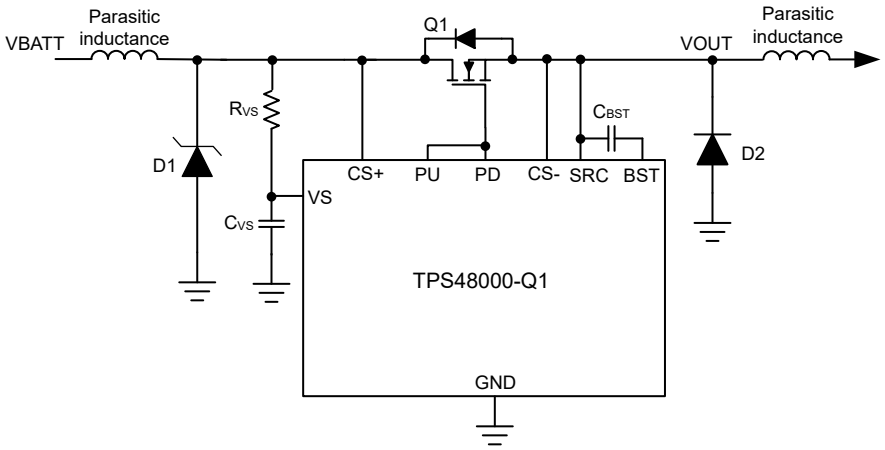


図 8-12. Circuit Implementation With Optional Protection Components For TPS48000-Q1

8.4 Layout

8.4.1 Layout Guidelines

- Place the sense resistor (R_{SNS}) close to the TPS48000-Q1 and then connect R_{SNS} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.

  For VDS based Current Sensing, follow the same kevlin techniques across the MOSFET.
- Choose a 0.1 µF or higher value ceramic decoupling capacitor between VS terminal and GND for all the applications. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- Make the high-current path from the board input to the load, and the return path, parallel and close to each other to minimize loop inductance.
- Place the external MOSFETs close to the controller GATE drive pins (PU/PD) such that the GATE of the MOSFETs are close to the controller GATE drive pins and forms a shorter GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- Place the external boot-strap capacitor close to BST and SRC pins to form very short loop.
- Connect the ground connections for the various components around the TPS48000-Q1 directly to each other, and to the TPS48000-Q1 GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.

8.4.2 Layout Example

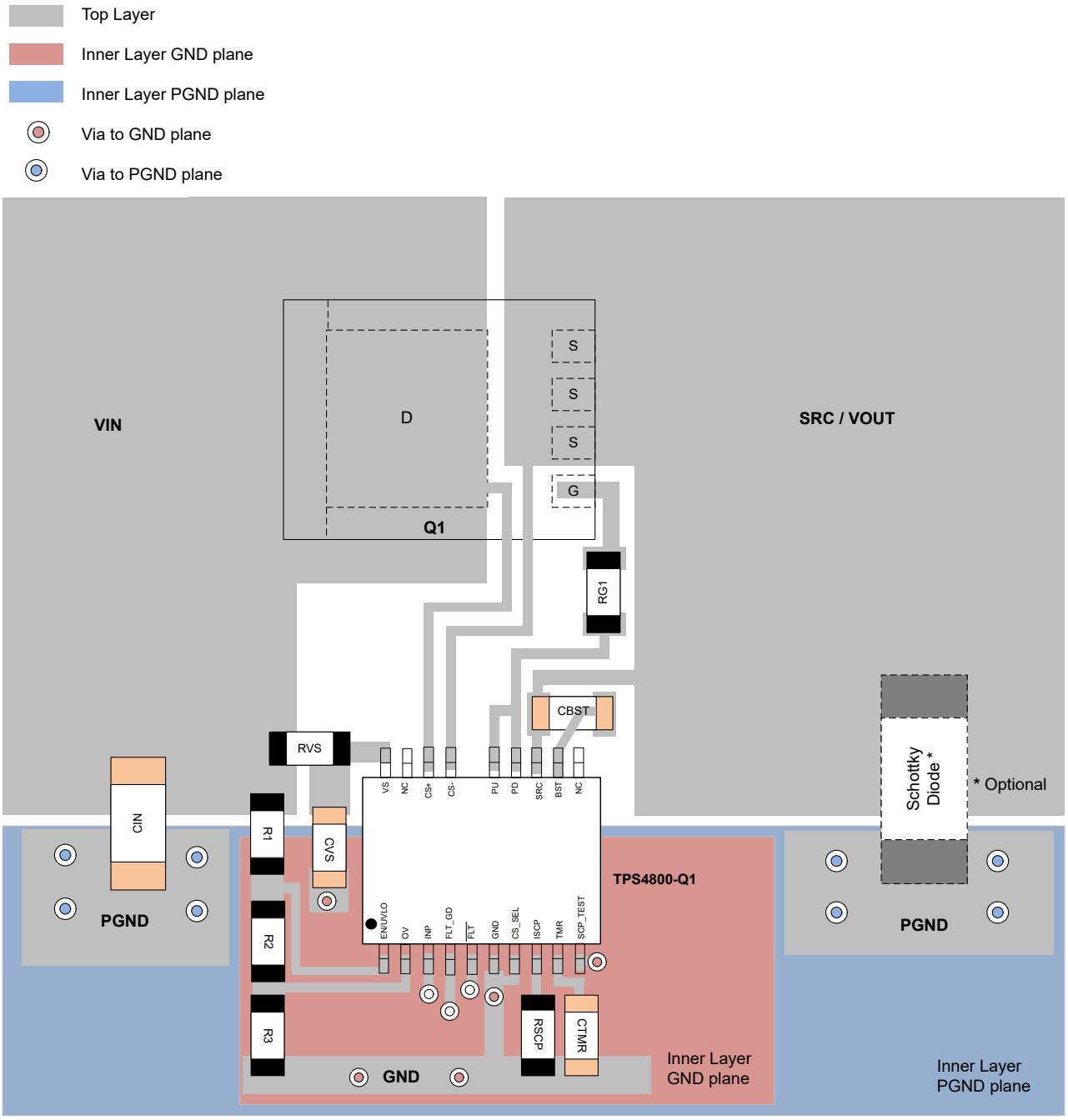


図 8-13. Typical PCB Layout Example for TPS48000-Q1 With VDS based Current Sensing

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2023) to Revision A (December 2024)	Page
• ドキュメントのステータスを「事前情報」から「*量産データ*」	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS48000QDGXRQ1	Active	Preproduction	VSSOP (DGX) | 19	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS48000QDGXRQ1.A	Active	Preproduction	VSSOP (DGX) | 19	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS48000QDGXRQ1	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4800
TPS48000QDGXRQ1.A	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4800

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

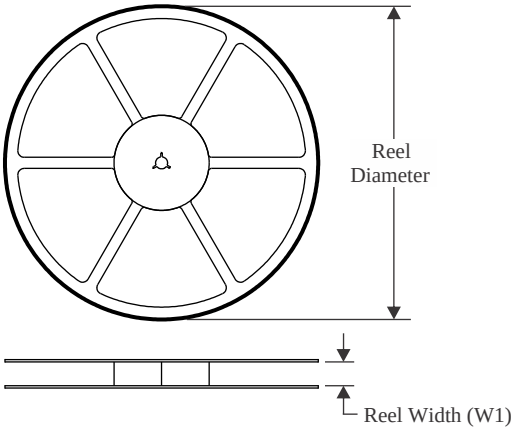
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

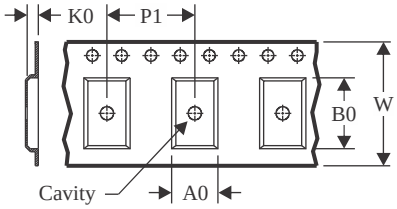
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

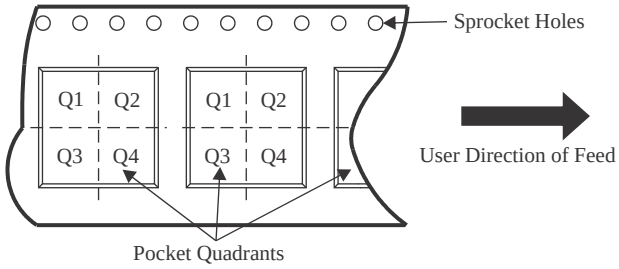


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

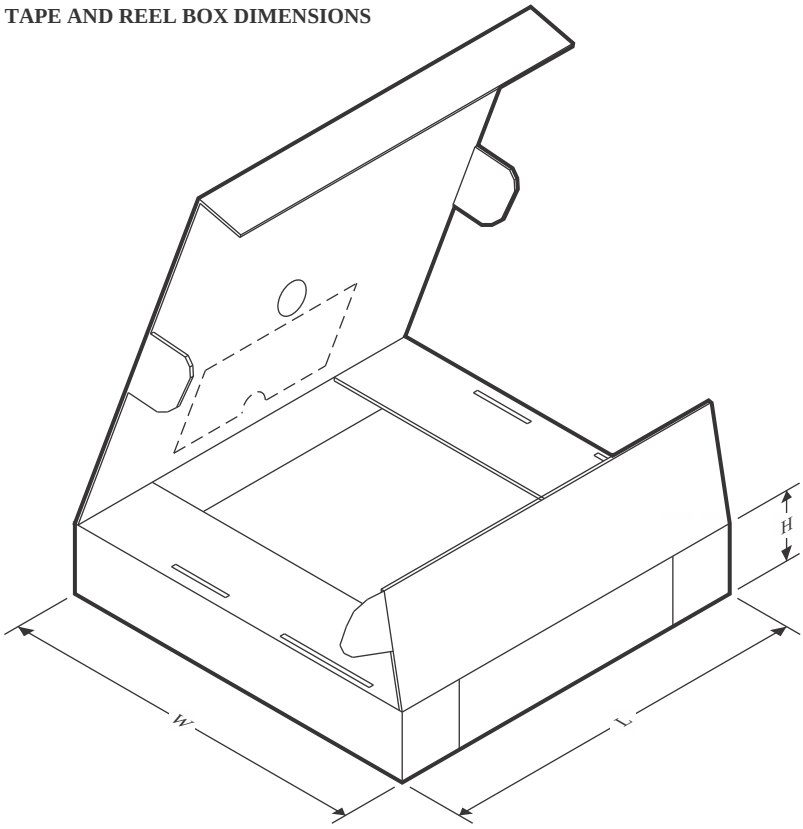
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS48000QDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

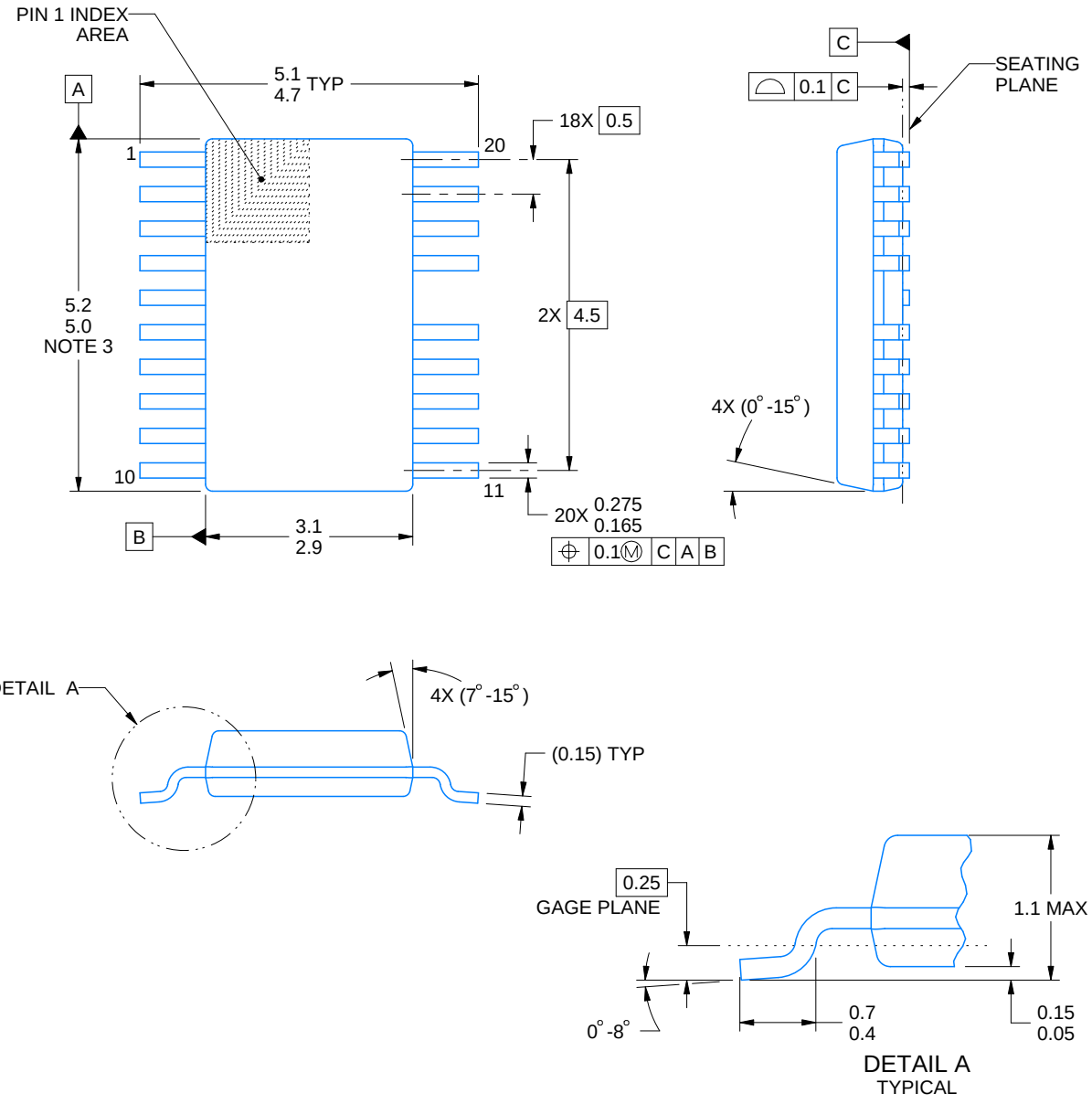
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS48000QDGXRQ1	VSSOP	DGX	19	5000	353.0	353.0	32.0

PACKAGE OUTLINE

DGX0019A

VSSOP - 1.1 mm max height

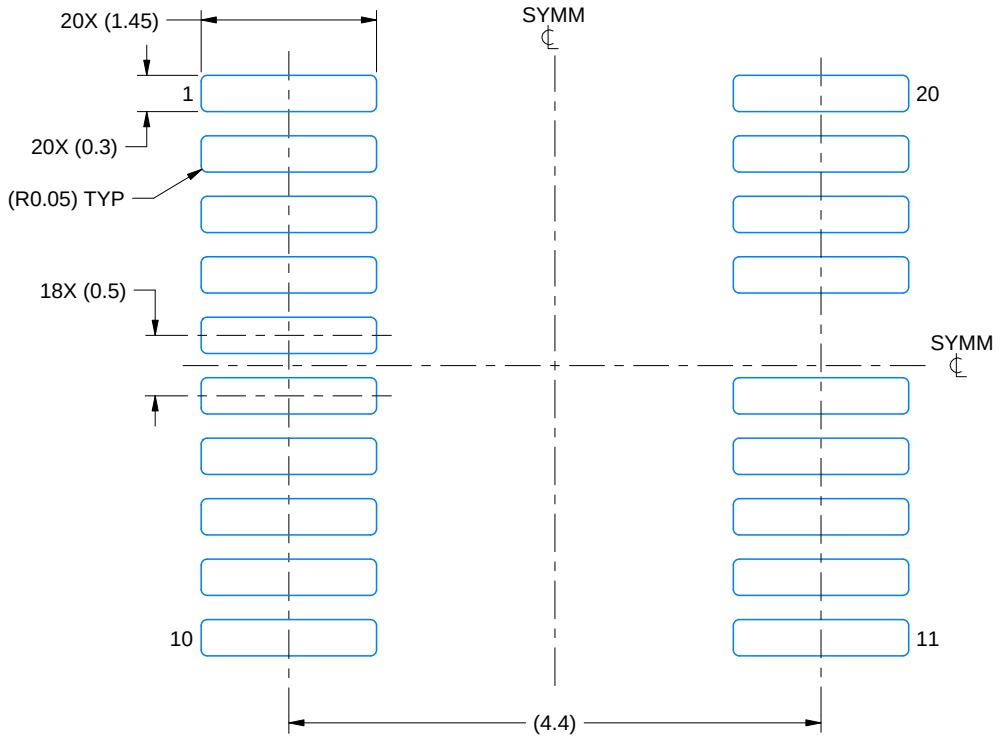
SMALL OUTLINE PACKAGE



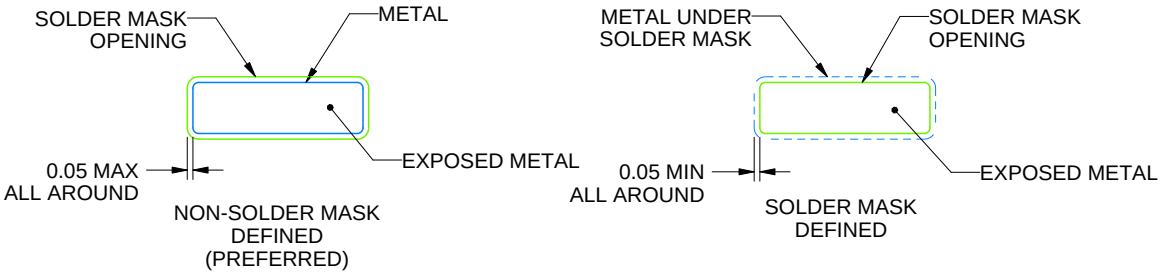
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X



SOLDER MASK DETAILS

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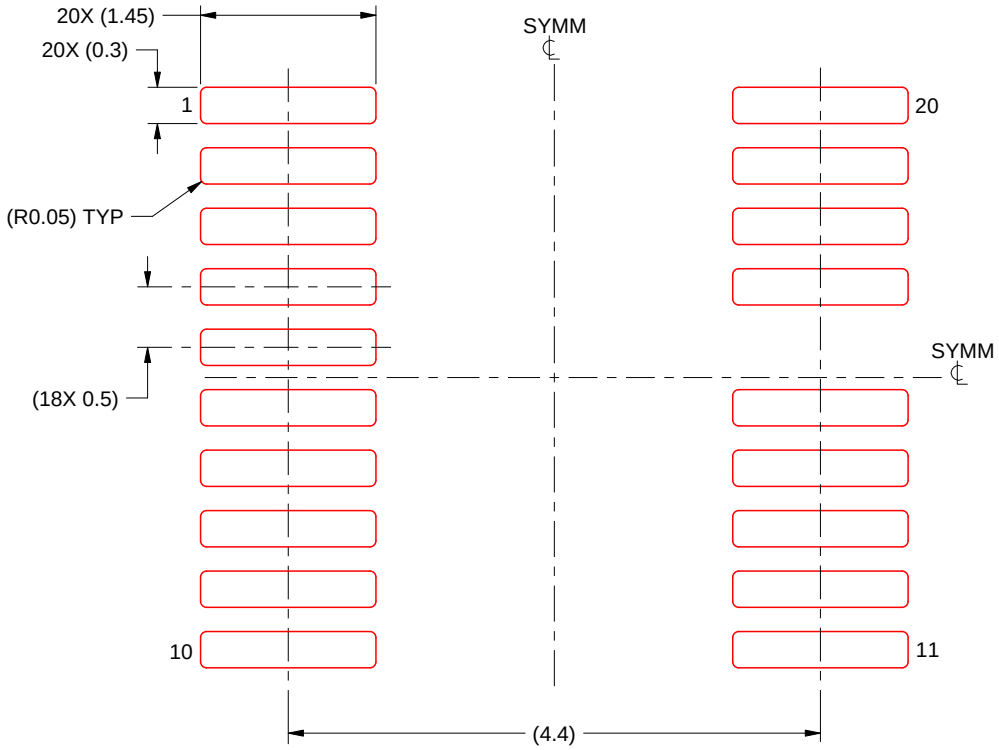
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226944/A 07/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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