TPS40190 4.5V～15V 入力、電圧モード同期整流降圧型コントローラ

1 特長

- 動作入力電圧範囲: 4.5V～15V
- 基準電圧：0.591V、±1%
- 電圧モード制御
- 内部のハウスキーピング、ドライバ電力、外部の軽負荷に対応する 5V レギュレータを内蔵
- 設定可能な短絡保護スレッショルド
- プリバイアス出力対応
- 300kHz の固定スイッチング周波数
- 内部ソフトスタート
- 小型の 3mm × 3mm、10 ピン SON パッケージ
- N チャネル MOSFET 用のブートストラップ付きドライバ
- 適応型のクロス導通防止
- 内部ブートストラップ・ダイオード
- 低スイッチング損失の 1.2A ドライバ

2 アプリケーション

- ケーブル・モデム CPE
- デジタル・セットトップ・ボックス
- グラフィック/オーディオ・カード
- エントリ・レベルおよびミッドレンジのサーバー

3 概要

TPS40190 は公称 4.5V～15V の電圧で動作する低コストの同期整流降圧型コントローラであり、固定周波数の電圧モード電源を実装します。このコントローラは、適応型のクロス導通防止機能によりハイサイド MOSFET と整流器 MOSFET が同時にオンしないようにして、2 つの MOSFET の貫通電流を防止しています。

本コントローラは、3 つの値のいずれかをユーザーが選択できる短絡保護スレッショルドも備えています。この保護レベルは、COMP から GND に接続した 1 つの外付け抵抗で設定されます。起動中に、COMP に接続されているインピーダンスを検出し、その情報をデコードすることで 3 つのスレッショルドのいずれかを選択します。コントローラが出力の短絡を検出した場合、両方の MOSFET がオフになり、タイムアウト期間が終了するまで再起動を試みません。これにより、持続的フォルトが発生した場合の消費電力を制限します。

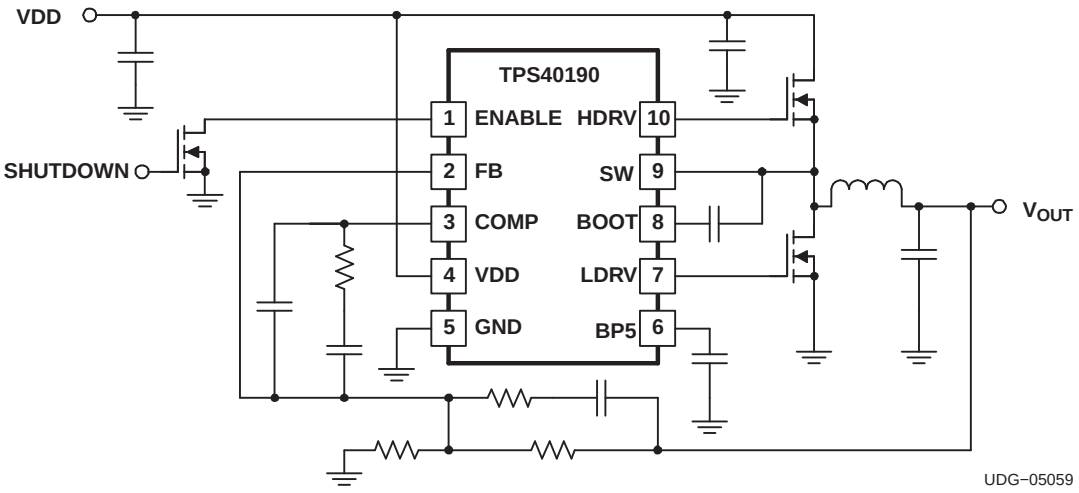
TPS40190 は電力段でのスイッチング損失を最小化する強力なドライバを備えているため、MOSFET の発熱を抑えることができ、またスイッチング時間をそれほど犠牲にしないで大きな MOSFET を使用できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS40190	VSON (10)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

アプリケーション概略図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (July 2012) から Revision D に変更 **Page**

- 編集上の変更のみ、技術的な改訂なし ... 1
- 「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Deleted Ordering Information table ... 3

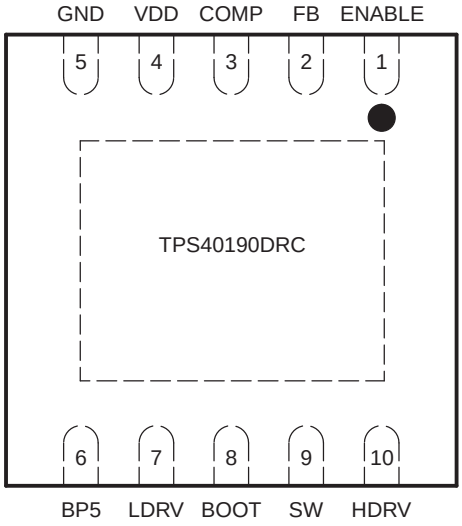
Revision B (August 2007) から Revision C に変更 **Page**

- Added a new paragraph to the end of the Enable Functionality section ... 14

5 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View

DRC PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ENABLE	I	Logic level input that starts or stops the controller from an external user command. A high level turns the controller on. This pin has a high-impedance internal pull-up integrated into the device. Because this pin is high impedance, a 10-nF capacitor to ground or an external pull-up resistor (100 kΩ) to VDD is recommended to avoid noise coupling to this pin.
2	FB	I	Inverting input to the error amplifier
3	COMP	O	Output of the error amplifier. Connecting a resistance from COMP to GND sets the output short circuit detection threshold. See applications information for details.
4	VDD	I	Power input to the controller
5	GND	—	Common connection for the controller
6	BP5	O	Output bypass for the internal regulator. Connect 4.7-μF capacitor from this pin to GND. Low power, low noise loads may be connected here if desired. The sum of the external load and the gate drive requirements must not exceed 40 mA. The regulator is turned off when the ENABLE pin is pulled low.
7	LDRV	O	Output to the rectifier FET gate
8	BOOT	I	Power supply for the flying high-side driver
9	SW	I	Sense line for the adaptive anti cross conduction circuitry. Serves as common connection for the flying high side FET driver
10	HDRV	O	Bootstrapped output for driving the gate of the high side N channel FET.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range	VDD	–0.3	16.5	V
	SW	–5	22	
	BOOT-SW, HDRV-SW (differential from BOOT or HDRV to SW)	–0.3	6	
	COMP	–0.3	3	
	FB, BP5, LDRV, ENABLE	–0.3	6	
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Dissipation Ratings

PACKAGE	$R_{\theta JA}$ High-K Board(1) (°C/W)	$R_{\theta JC}$ (2) (°C/W)
DRC	47.9	14.1

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch (7.5-cm x 7.5-cm), multilayer board with one-ounce internal power and ground planes and two-ounce copper traces on top and bottom of the board.
(2) The junction-to-case impedance is measured from the die to the thermal pad on the device package.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Input voltage	4.5		15	V
T_A	Operating free-air temperature	–40		85	°C

6.4 Electrical Characteristics

T_A = –40°C to 85°C, V_{VDD}= 12 V_{dc}, T_A =T_J, and all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage range	0°C ≤ T_J ≤ 85°C	585	591	597	mV
		-40°C ≤ T_J ≤ 85°C	582	591	597	
INPUT SUPPLY						
V_{VDD}	Input voltage range		4.5		15.0	V
I_{VDD}	Operating current	V_{ENABLE} = 2.5 V, Outputs switching			2.5	mA
		V_{ENABLE} = 0.6 V			20	µA
ON BOARD REGULATOR						
V_{5VBP}	Output voltage	V_{VDD} > 6 V, I_{5VBP} ≤ 10 mA	5.1	5.3	5.5	V
V_{DO}	Regulator dropout voltage	V_{VDD} - V_{BP5} , V_{VDD} = 5 V, I_{BP5} ≤ 25 mA		270	400	mV
I_{SC}	Regulator current limit threshold		40			mA
I_{BP5}	Average current(1)				40	
OSCILLATOR						
f_{SW}	Switching frequency		240	300	360	kHz
V_{RMP}	Ramp amplitude(2)			0.75		V
V_{VALLEY}	Valley voltage(2)			0.5		V
PWM						
D_{MAX}	Maximum duty cycle(2)		85%			
$t_{ON(min)}$	Minimum controlled pulse(2)				130	ns
t_{DEAD}	Output driver dead time	HDRV off to LDRV on		50		ns
		LDRV off to HDRV on		25		
SOFT-START						
t_{SS}	Soft-start time		3.0	4.7	7.0	ms
t_{SSDLY}	Soft-start delay time(3)			6		ms
t_{REG}	Time to regulation			10.5		ms
ERROR AMPLIFIER						
GBWP	Gain bandwidth product(2)		5			MHz
A_{OL}	DC gain(2)		60			dB
I_{IB}	Input bias current (current out of FB pin)		100		0	nA
I_{EAOP}	Output source current	V_{FB} = 0 V	1			mA
I_{EAOM}	Output sink current	V_{FB} = 2 V	1			mA
SHORT CIRCUIT PROTECTION						
$t_{PSS(min)}$	Minimum pulse during short circuit(2)				250	ns
t_{BLNK}	Blanking time(2)		100	140	180	ns
t_{OFF}	Off-time between restart attempts		25	95		ms
V_{ILIM}	Short circuit comparator threshold voltage	$R_{COMP(GND)}$ = OPEN, T_J = 25°C	256	320	384	mV
		$R_{COMP(GND)}$ = 4 kΩ, T_J = 25°C	128	160	192	
		$R_{COMP(GND)}$ = 12 kΩ, T_J = 25°C	368	460	552	

(1) 40 mA is the current available for MOSFET gate drive, the device itself and any external loads. The sum of these must not exceed 40 mA.
(2) Specified by design. Not production tested.
(3) The delay time is the time delay from application of power to the device or from assertion of ENABLE until the output begins to rise.

Electrical Characteristics (continued)

T_A = –40°C to 85°C, V_{VDD}= 12 V_{dc}, T_A =T_J, and all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = -100 mA		3	6	Ω
R_{HDLO}	High-side driver pull-down resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = 100 mA		1.5	3	Ω
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = -100 mA		2.5	5	Ω
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 100 mA		0.8	1.5	Ω
t_{HRISE}	High-side driver rise time(2)	C_{LOAD} = 1 nF		15	35	ns
t_{HFALL}	High-side driver fall time(2)	C_{LOAD} = 1 nF		10	25	ns
t_{LRISE}	Low-side driver rise time(2)	C_{LOAD} = 1 nF		15	35	ns
t_{LFALL}	Low-side driver fall time(2)	C_{LOAD} = 1 nF		10	25	ns
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{UVLO}	Turn-on voltage		4.1	4.25	4.4	V
$UVLO_{HYST}$	Hysteresis		270	320	370	mV
SHUTDOWN						
V_{IH}	High-level input voltage	ENABLE			2.8	V
V_{IL}	Low-level input votlage	ENABLE	0.6			V
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA	0.6	0.8	1.2	V

6.5 Typical Characteristics

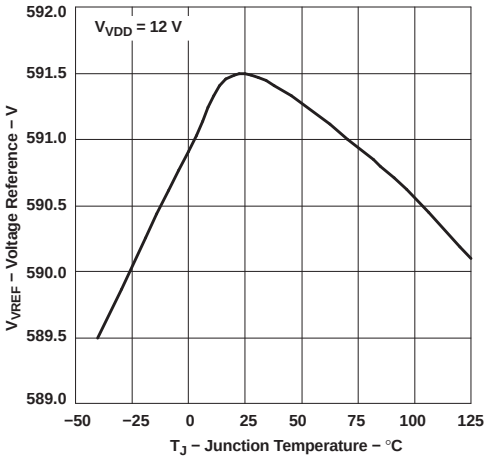


Figure 1. Reference Voltage vs Temperature

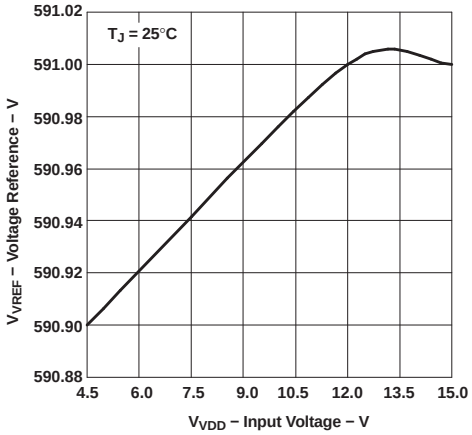


Figure 2. Reference Voltage vs Input Voltage

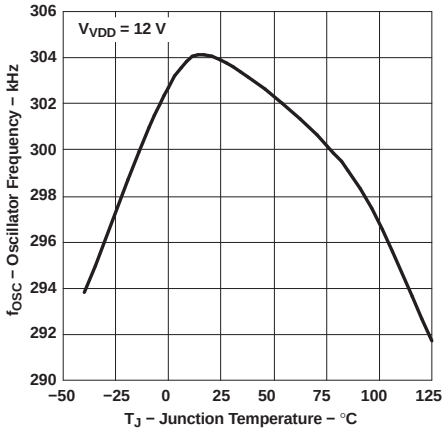


Figure 3. Oscillator Frequency vs Temperature

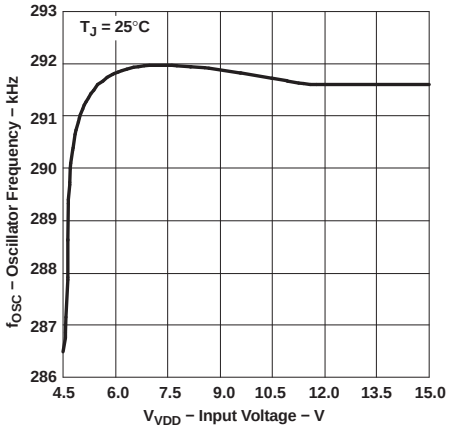


Figure 4. Oscillator Frequency vs Input Voltage

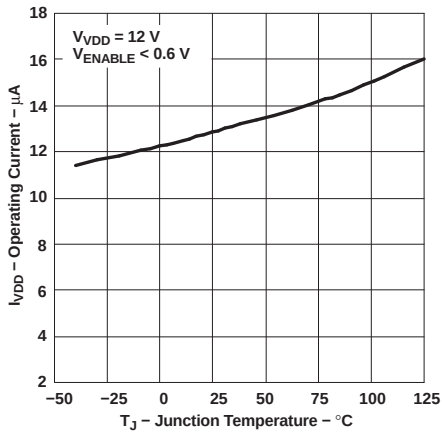


Figure 5. Operating Current vs Temperature

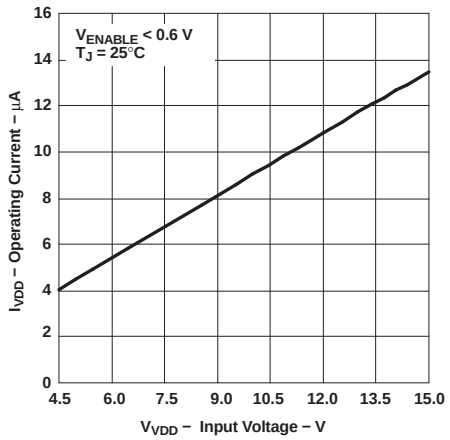


Figure 6. Operating Current vs Input Voltage

Typical Characteristics (continued)

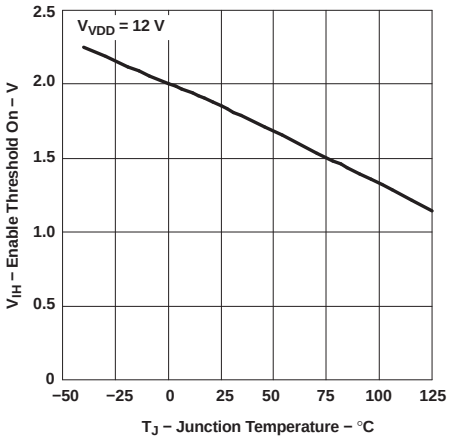


Figure 7. Enable Threshold On vs Temperature

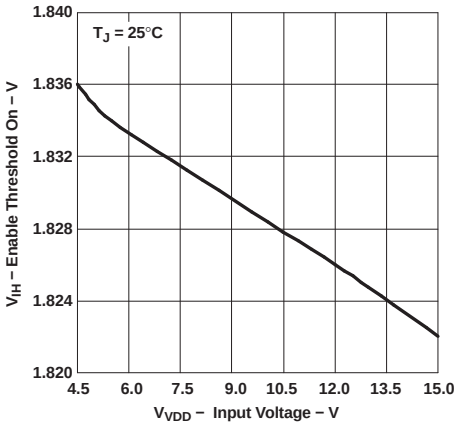


Figure 8. Enable Threshold On vs Input Voltage

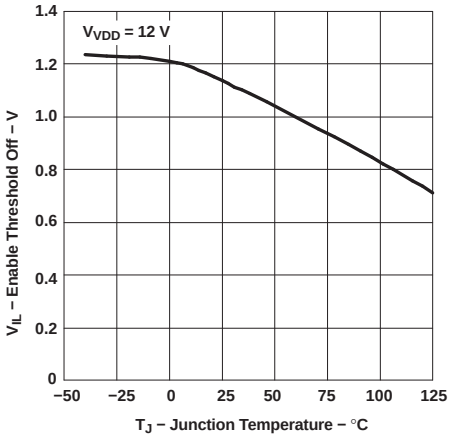


Figure 9. Enable Threshold Off vs Temperature

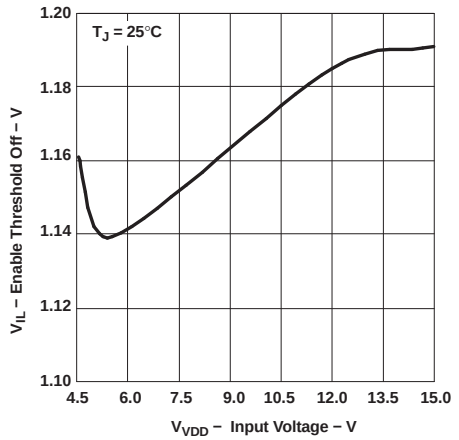


Figure 10. Enable Threshold Off vs Input Voltage

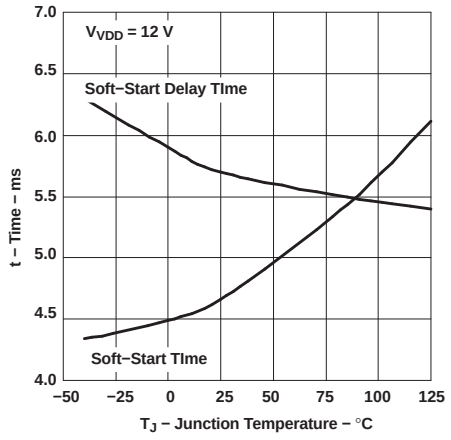


Figure 11. Soft Start Timing vs Temperature

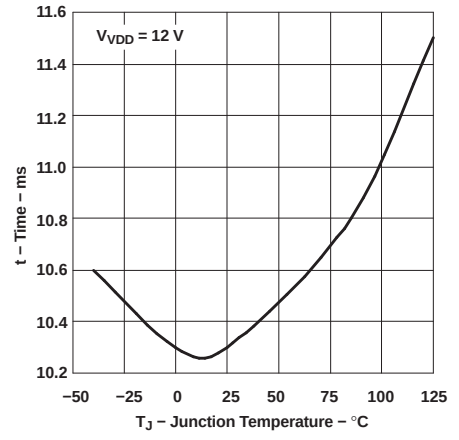


Figure 12. Total Startup Time vs Temperature

Typical Characteristics (continued)

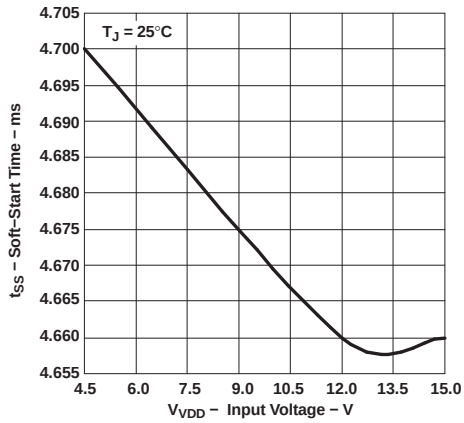


Figure 13. Soft Start Timing vs Input Voltage

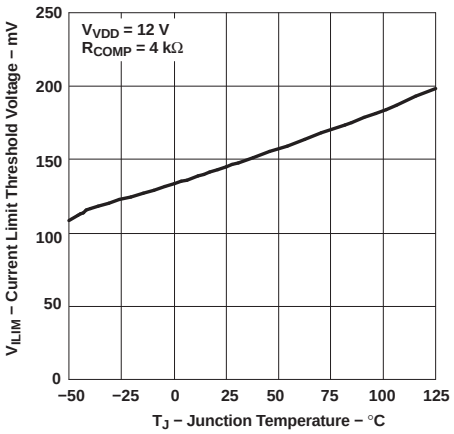


Figure 14. Current Limit Threshold vs Temperature

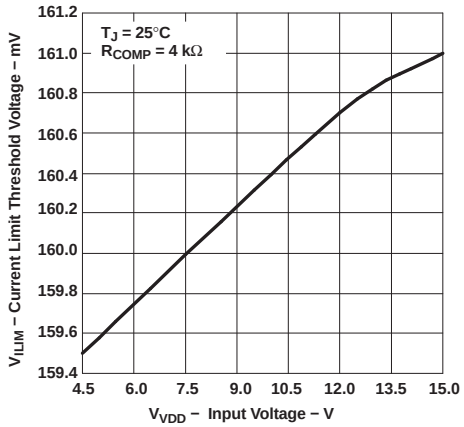


Figure 15. Current Limit Threshold vs Input Voltage

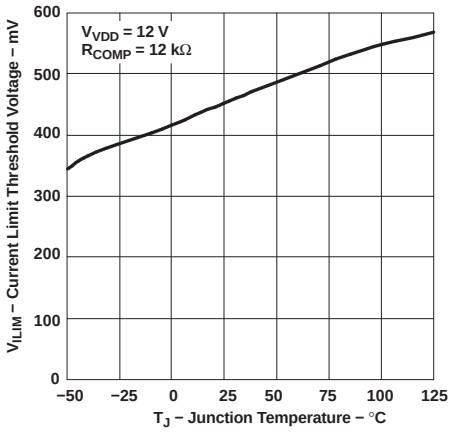


Figure 16. Current Limit Threshold vs Temperature

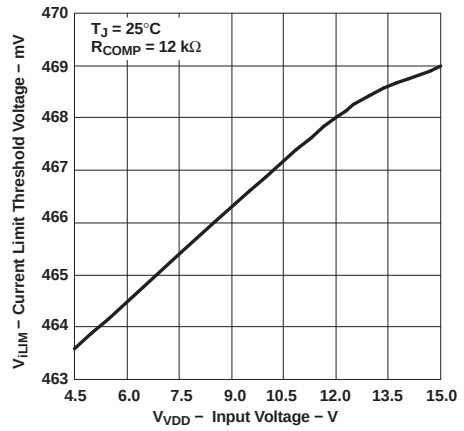


Figure 17. Current Limit Threshold vs Input Voltage

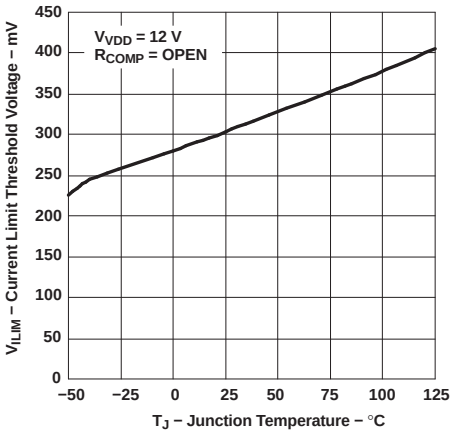


Figure 18. Current Limit Threshold vs Temperature

Typical Characteristics (continued)

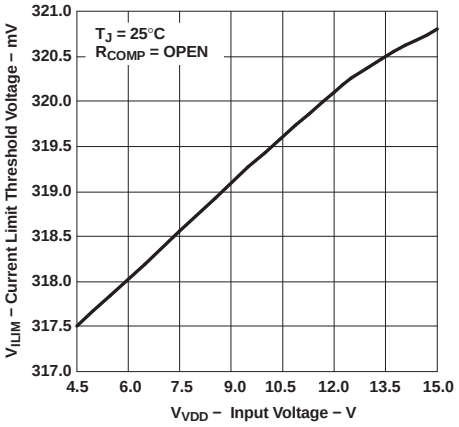


Figure 19. Current Limit Threshold vs Input Voltage

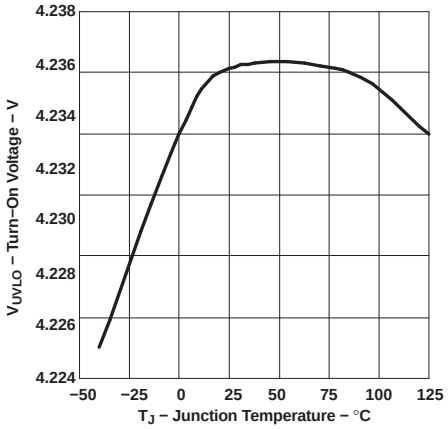


Figure 20. Undervoltage Lockout Turn On Voltage vs Temperature

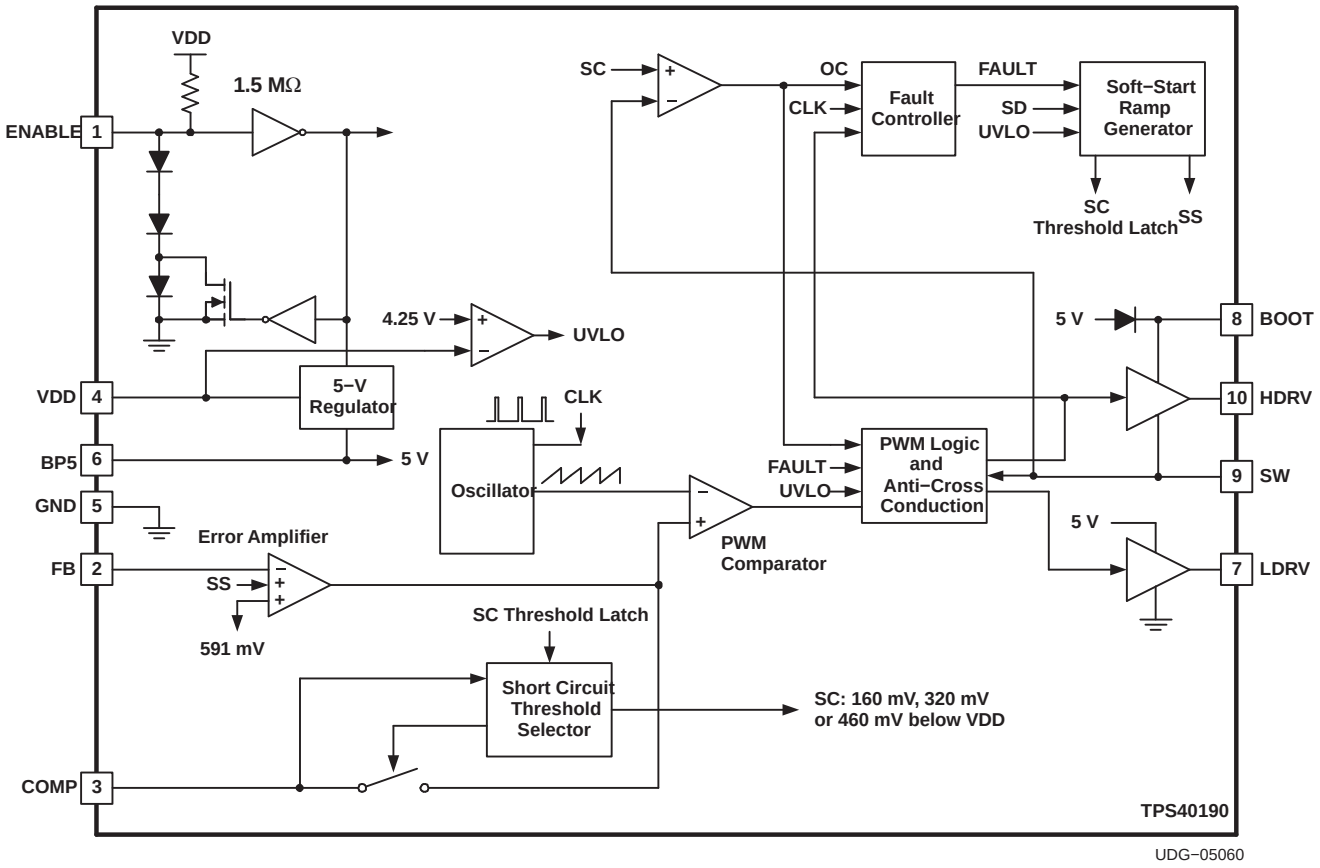
7 Detailed Description

7.1 Overview

The TPS40190 is a cost optimized controller providing all the necessary features to construct a high-performance DC-DC converter while keeping costs to a minimum. Support for pre-biased outputs eliminates concerns about damaging sensitive loads during start-up. Strong gate drivers for the high side and rectifier N-channel MOSFETs decrease switching losses for increased efficiency. Adaptive gate drive timing minimizes body diode conduction in the rectifier MOSFET, also increasing efficiency. Selectable short circuit protection thresholds and hiccup recovery from a short-circuit increase design flexibility and minimize power dissipation in the event of a prolonged output fault. A dedicated enable pin (ENABLE) allows the converter to be placed in a very low quiescent current shutdown mode.

Internally fixed switching frequency and soft-start time reduce external component count, simplifying design and layout, as well as reducing footprint and cost. The 3-mm × 3-mm package size also contributes to a reduced overall converter footprint.

7.2 Functional Block Diagram



UDG−05060

7.3 Feature Description

7.3.1 Internally Fixed Parameters

The TPS40190 has a fixed internal switching frequency of 300 kHz. Soft-start time is fixed at 4.7 ms typical and the UVLO level is set between 4.1 V and 4.4 V.

Feature Description (continued)

7.3.2 Output Short Circuit Protection

The short circuit detection in the TPS40190 is done by sensing the voltage drop across the high side FET when it is on. If the voltage drop across this FET exceeds the selected threshold in any given switching cycle, a counter counts up one count and the FET is turned off early. If the voltage drop across that FET does not exceed this threshold, the counter is decremented for that cycle and the FET is allowed to remain on for the normal pulse width commanded by the internal pulse width modulator. If the counter fills up (a count of 7) a fault condition is declared and the drivers turn both FETs off. After a timeout of approximately 95 ms, the controller attempts to restart. If a short circuit is still present at the output, the current ramps quickly up to the short-circuit threshold and another fault condition is declared. The device then waits 95 ms to attempt to restart again.

Typical waveforms during a short circuit event are shown in Figure 21 and Figure 22.

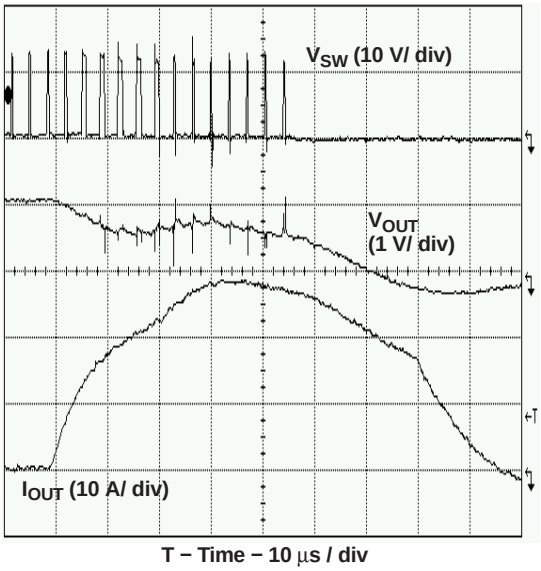


Figure 21. Output Short Circuit Detected (Nominal Threshold 25 A)

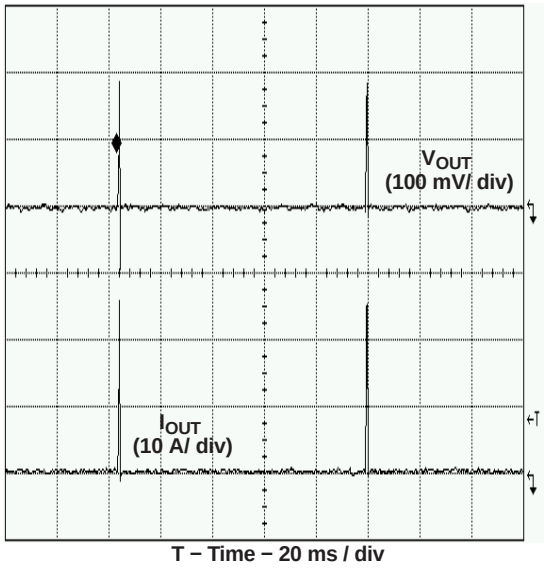


Figure 22. Output Fault Hiccup Restart Timing

The TPS40190 provides three selectable short circuit protection thresholds: 160 mV, 320 mV and 460 mV. The particular threshold is selected by connecting a resistor from COMP to GND. Table 1 gives the short circuit thresholds for corresponding resistors from COMP to GND. Note that since the TPS40190 measures the resistance from COMP to GND during a 2-ms window, the compensation network from COMP to FB should have a time constant significantly less than 1 ms or there can be issues detecting the resistance and setting the correct short circuit threshold. This network should have no DC path from COMP to FB.

The short circuit detection threshold in the TPS40190 has some temperature compensation built in to help offset the high-side FET rise in resistance as its temperature rises. A typical FET has a resistance temperature coefficient of about 4500 ppm/°C. The temperature coefficient of the short circuit threshold is approximately 4200 ppm/°C. Figure 23 shows how the short circuit threshold increases with temperature to help compensate for the FET resistance increase. The relative FET resistance change is based on an estimate of a linear 4500 ppm/°C temperature coefficient. The effectiveness of this compensation depends on how tight the thermal coupling between the TPS40190 and the high-side FET is. Better thermal coupling between the TPS40190 and the high-side FET gives better compensation effectiveness.

Feature Description (continued)

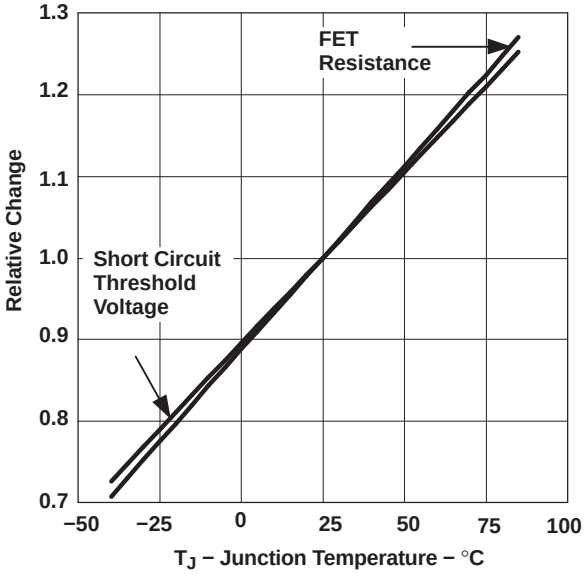


Figure 23. Relative Short Circuit Threshold Change vs Temperature

Table 1. Short Circuit Threshold Voltage Selection

SHORT CIRCUIT PROTECTION RESISTANCE, R_{COMP} (kΩ)	NOMINAL CURRENT LIMIT VOLTAGE, V_{ILIM} (mV)
10.8 to 13.2	460
OPEN	320
3.6 to 4.4	160

The range of short circuit current thresholds that can be expected is given by Equation 1 and Equation 2.

$$I_{SCP(max)} = \frac{V_{ILIM(max)}}{R_{DS(onMIN)}} \quad (1)$$

$$I_{SCP(min)} = \frac{V_{ILIM(min)}}{R_{DS(onMAX)}}$$

where

- I_{SCP} is the short circuit current
- V_{ILIM} is the short circuit threshold
- $R_{DS(on)}$ is the channel resistance of the high-side MOSFET (2)

7.3.3 Enable Functionality

The TPS40190 has a dedicated ENABLE pin. This simplifies user level interface design since no multiplexed functions exist. Another benefit is a true low power shutdown mode of operation. In this state, the BP5 regulator is turned off. When the ENABLE pin is pulled to GND, the TPS40190 consumes a typical 20-μA of current. A functionally equivalent circuit to the enable circuitry on the TPS40190 is shown in Figure 24.

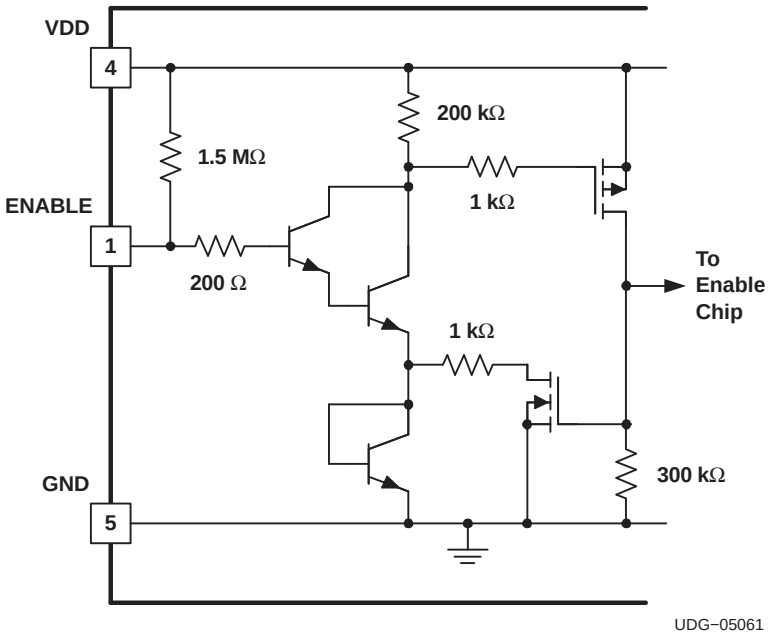


Figure 24. TPS40190 ENABLE Pin Internal Circuitry

If the ENABLE pin is left floating, the chip starts automatically. The pin must be pulled to less than 600 mV to ensure that the TPS40190 is in shutdown mode. Note that the ENABLE pin is relatively high impedance. In some situations, there could be enough noise nearby to cause the ENABLE pin to swing below the 600 mV threshold and give erroneous shutdown commands to the rest of the device. There are two solutions to this problem should it arise.

1. Place a capacitor from ENABLE to GND. A side effect of this is to delay the start of the converter while the capacitor charges past the enable threshold
2. Place a resistor from VDD to ENABLE. This causes more current to flow in the shutdown mode, but does not delay converter startup. If a resistor is used, the total current into the ENABLE pin should be limited to no more than 500 μA.

The ENABLE pin is self-clamping. The clamp voltage can be as low as 1 V with a 1-kΩ ground impedance. Due to this self-clamping feature, the pull-up impedance on the ENABLE pin should be selected to limit the sink current to less than 500 μA. Driving the ENABLE pin with a low-impedance source voltage can result in damage to the device. Because of the self-clamping feature, it requires care when connecting multiple ENABLE pins together. For enabling multiple TPS4019x devices (TPS40190, TPS40192, TPS40193, TPS40195, TPS40197), see the Application Report SLVA509.

Typical waveforms for startup and shutdown using the ENABLE pin are shown in Figure 25 and Figure 26.

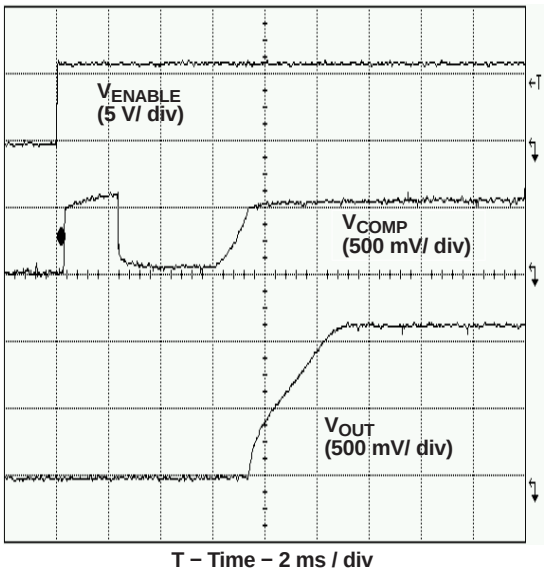


Figure 25. Startup Using ENABLE Pin

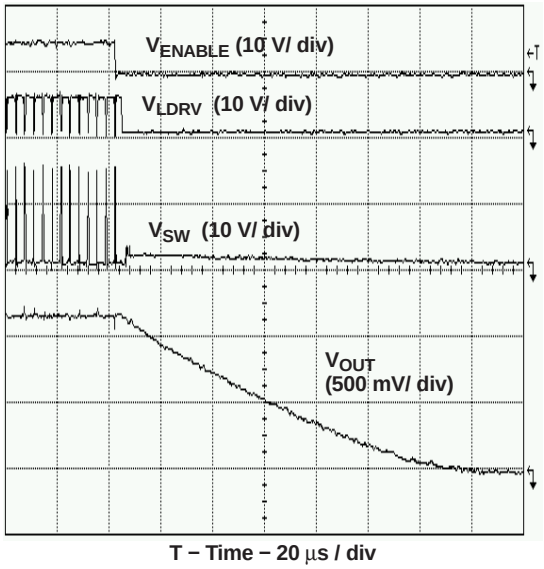


Figure 26. Shutdown Using ENABLE Pin

7.3.4 5-V Regulator

The TPS40190 has an on board 5-V regulator that allows the part to operate from a single voltage feed. No separate 5-V feed to the part is required. This regulator needs to have 4.7-µF of capacitance on the BP5 pin for stability. A ceramic capacitor is suggested for this purpose.

This regulator can also be used to supply power to nearby circuitry, eliminating the need for a separate LDO in some cases. If this pin is used for external loads, keep in mind that this is the power supply for the internals of the TPS40190. While efforts have been made to reduce sensitivity, any noise induced on this line has an adverse effect on the overall performance of the internal circuitry and shows up as increased pulse jitter, or skewed reference voltage. This regulator is turned off when the ENABLE pin is pulled low.

The amount of power available from this pin varies with the size of the power MOSFETs that the drivers must operate. Larger MOSFETs require more gate drive current and reduces the amount of power available on this pin for other tasks.

The total amount of current required by the gate drive and the external circuitry should not exceed 40 mA. The current required to drive the FET gates can be found from Equation 3.

$$I_G = f_{SW} \times \left(Q_{G\,(high)} + Q_{G\,(low)}\right) \quad (3)$$

Where

- I_G is the required gate drive current
- f_{SW} is the switching frequency (300 kHz)
- $Q_{G(high)}$ is the gate charge requirement for the high-side FET at 5 V V_{GS}
- $Q_{G(low)}$ is the gate charge requirement for the low-side FET at 5 V V_{GS}

7.3.5 Startup Sequence and Timing

The TPS40190 startup sequence is as follows. After input power is applied, the 5-V onboard regulator comes up. Once this regulator comes up, the TPS40190 goes through a period where it samples the impedance at the COMP pin and decides the short circuit protection threshold voltage. This is accomplished by placing 400 mV on the COMP pin for approximately 2 ms. During this time, the current is measured and compared against internal thresholds to select the short circuit protection threshold. After this, the COMP pin is brought low for 4 ms. This ensures that the feedback loop is preconditioned at startup and no sudden output rise occurs at the output of the converter when the converter is allowed to start switching. After these initial 6 milliseconds, the internal soft-start circuitry is engaged and the converter is allowed to start. See Figure 27.

7.3.6 Prebias Outputs

Some applications require that the converter not sink current during start-up if a pre-existing voltage is higher than the output. Because synchronous buck converters inherently sink current some method of overcoming this characteristic must be employed. Applications that require this operation are typically power rails for a multi supply processor or ASIC. The method used in this controller, is to not allow the low side or rectifier FET to turn on until there the output voltage commanded by the start up ramp is higher than the pre-existing output voltage. This is detected by monitoring the internal pulse width modulator (PWM) for its first output pulse. Because this controller uses a closed loop startup, the first output pulse from the PWM does not occur until the output voltage is commanded to be higher than the pre-existing voltage. This effectively limits the controller to sourcing current only during the startup sequence.

If the pre-existing voltage is higher than the intended regulation point for the output of the converter, the converter starts and sinks current when the soft-start time has completed. A typical pre-biased start-up is shown in Figure 28.

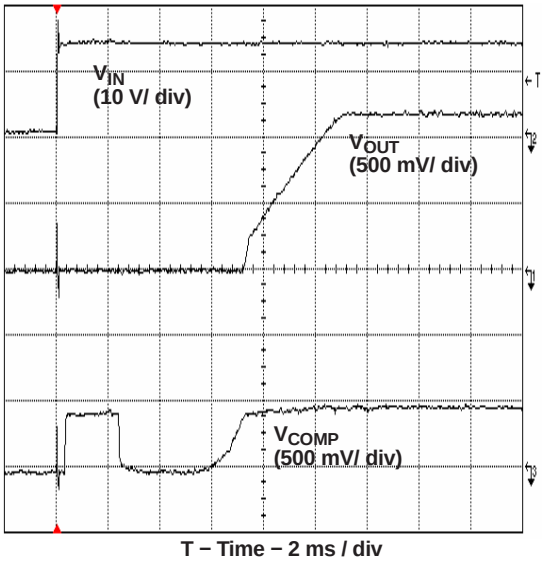


Figure 27. TPS40190 Start-up Timing

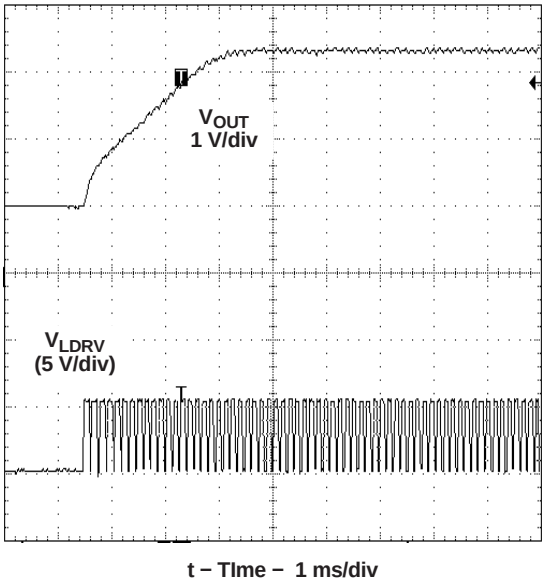


Figure 28. Prebiased Start-up Timing

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Applications

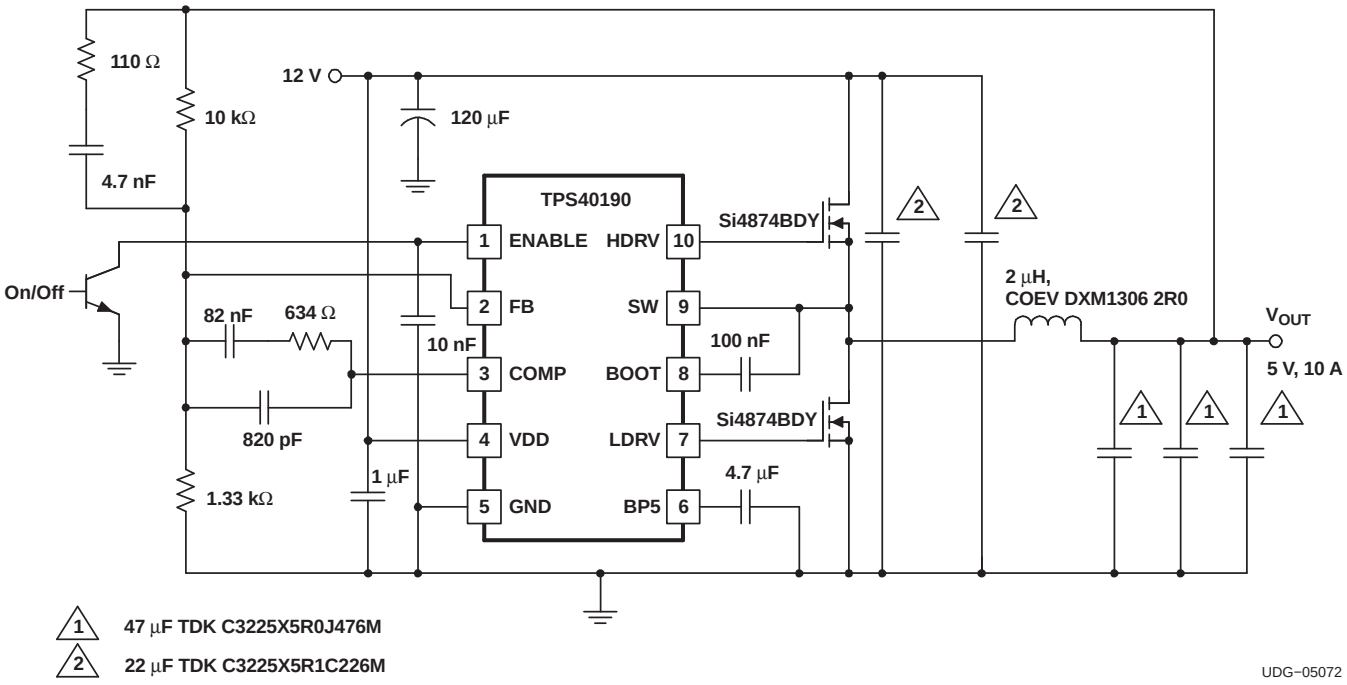


Figure 29. 12-V to 5-V at 10 A

Typical Applications (continued)

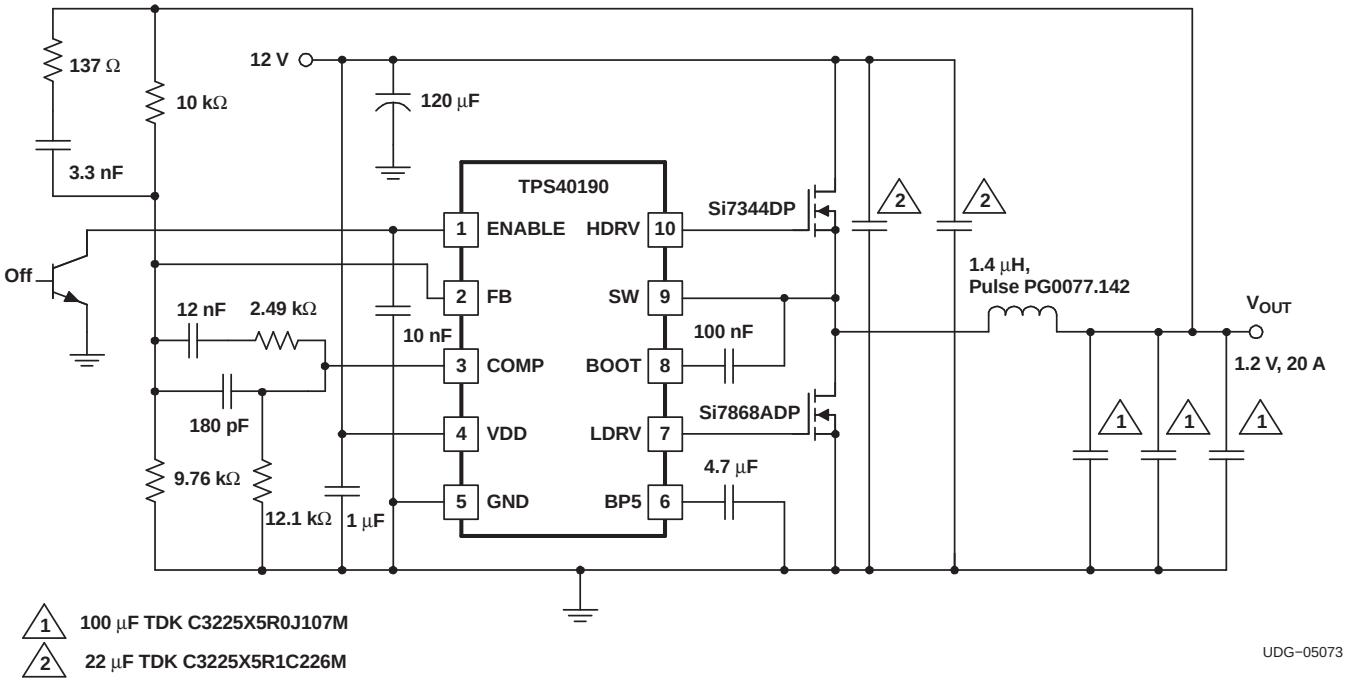


Figure 30. 12-V to 1.2-V at 20 A

Typical Applications (continued)

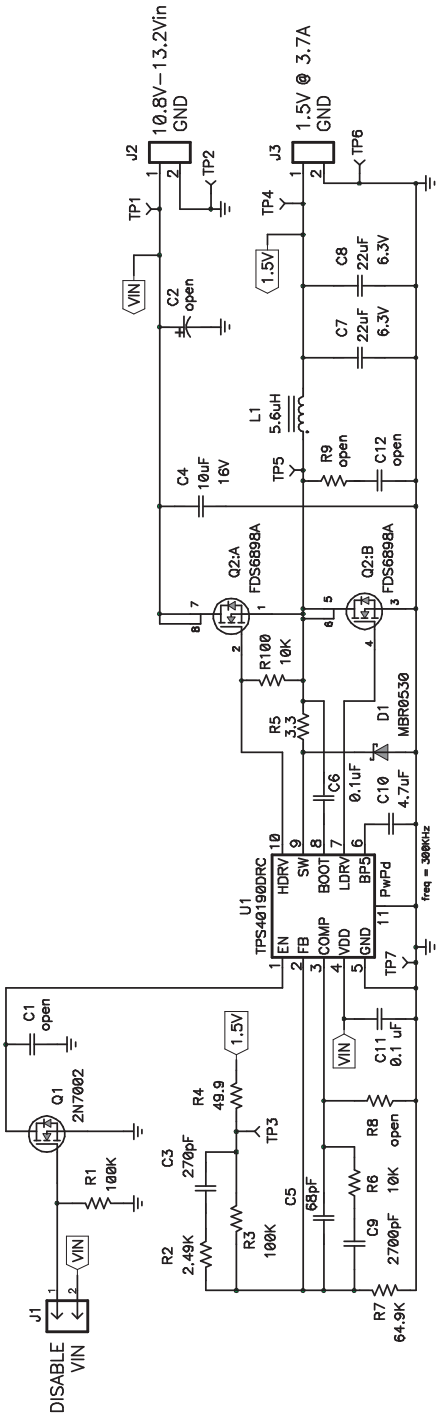


Figure 31. PMP1285, 12-V to 1.5-V, at 3.7 A

9 デバイスおよびドキュメントのサポート

9.1 ドキュメントのサポート

9.1.1 関連資料

関連資料については、以下を参照してください。

- TI アプリケーション・レポート、『*Enabling Multiple TPS4019x Devices*』、SLVA509 (英語)

9.2 ドキュメントの更新通知を受け取る方法

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9.3 コミュニティ・リソース

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9.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS40190DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	0190
TPS40190DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0190
TPS40190DRCR.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0190
TPS40190DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0190
TPS40190DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	0190
TPS40190DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	0190
TPS40190DRCT.B	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	0190
TPS40190DRCTG4	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	0190

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

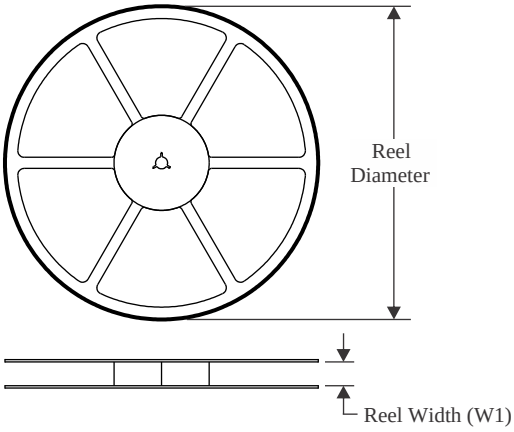
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

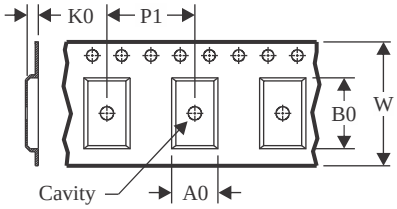
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

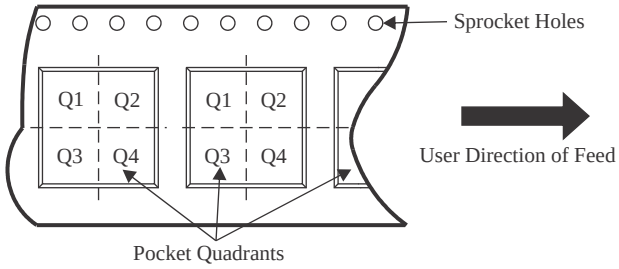


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

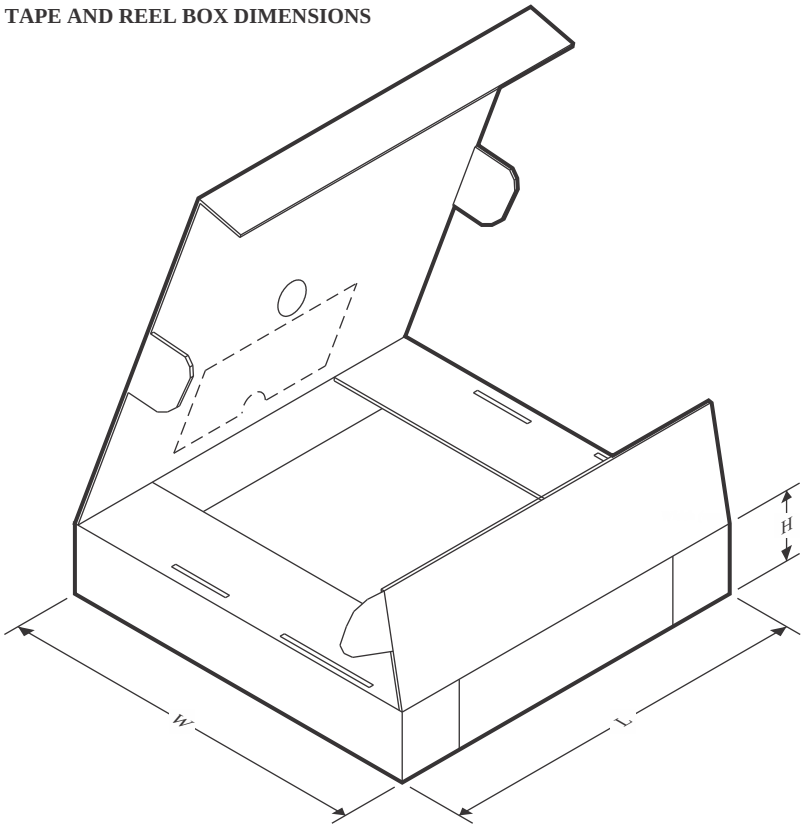
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40190DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS40190DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40190DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40190DRCR	VSON	DRC	10	3000	367.0	367.0	38.0
TPS40190DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS40190DRCT	VSON	DRC	10	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

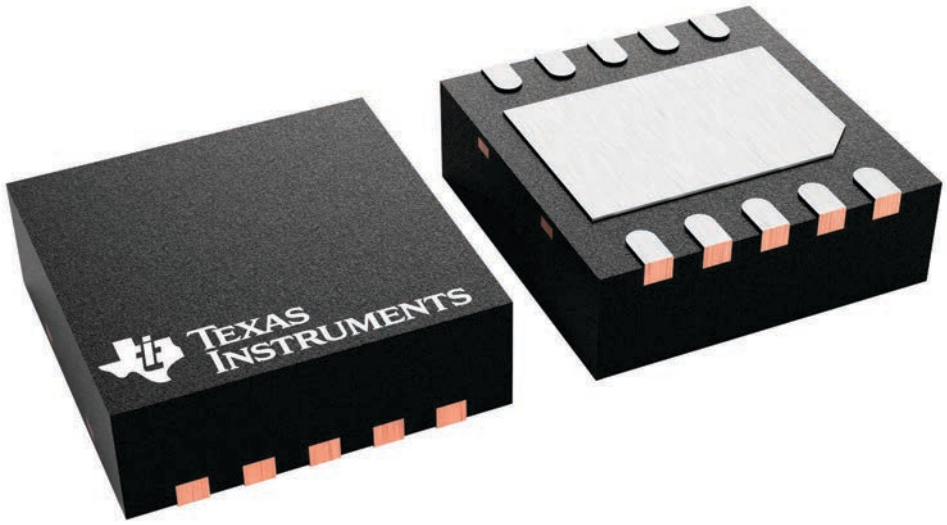
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



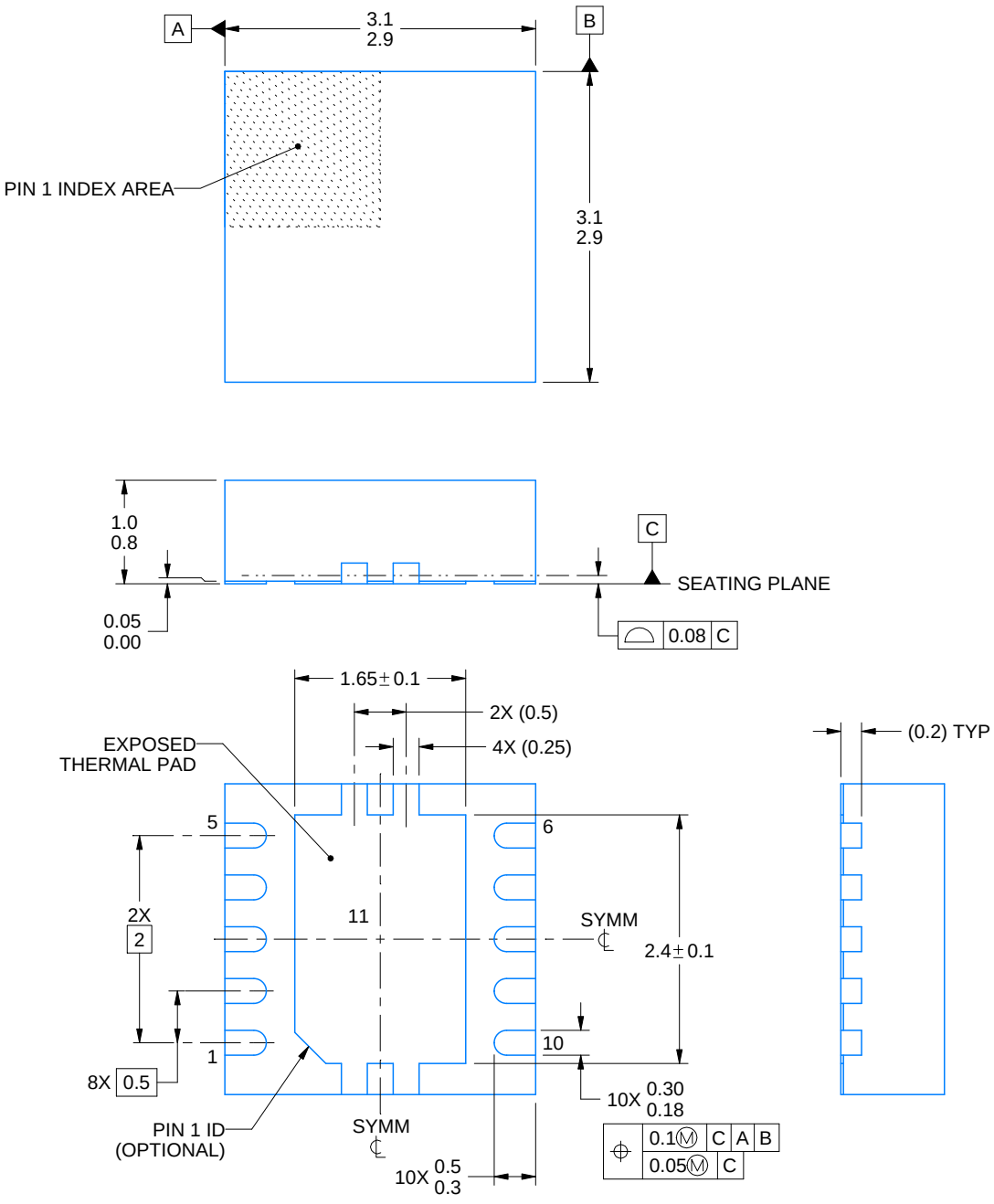
4226193/A

DRC0010J

PACKAGE OUTLINE

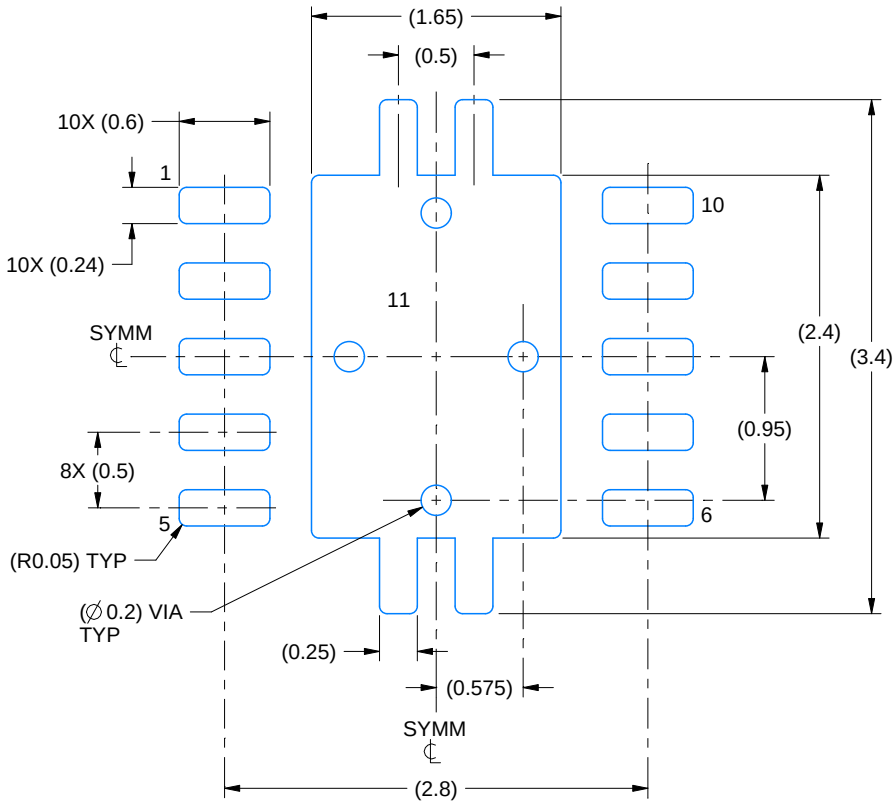
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

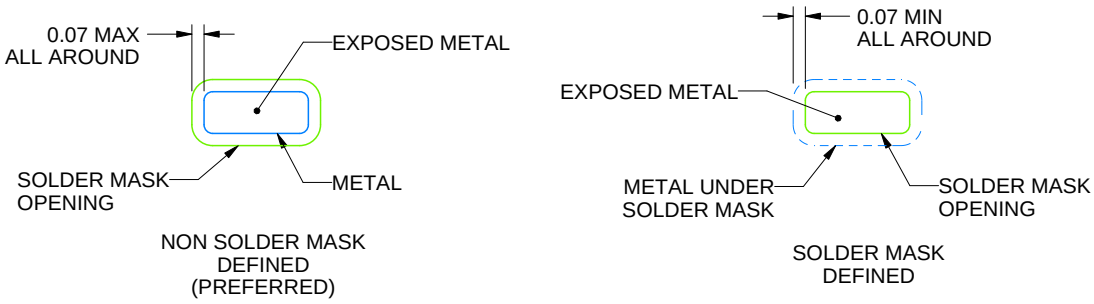


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

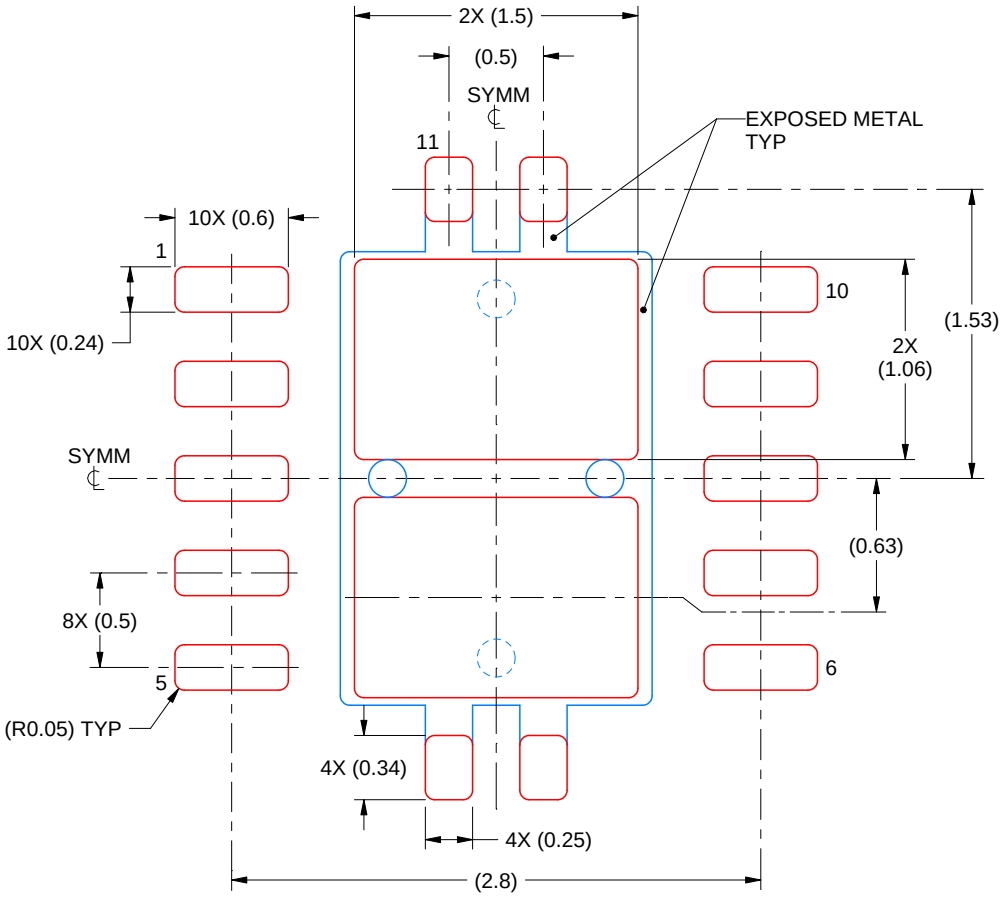
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月