TEXAS INSTRUMENTS
TPS40054, TPS40055, TPS40057
JAJS116J – DECEMBER 2003 – REVISED JUNE 2022

TPS4005x 入力範囲の広い同期整流降圧コントローラ

1 特長

- 新製品が利用可能
  - LM5145 入力電圧範囲とデューティ・サイクル範囲の広い 75V 同期整流降圧コントローラ
  - LM5146 デューティ・サイクル範囲の広い 100V 同期整流降圧 DC/DC コントローラ
- 動作入力電圧：8V～40V
- 入力電圧フィードフォワード補償
- 1% 未満の内蔵 0.7V 基準電圧
- プログラム可能な固定周波数 (最大 1MHz) の電圧モード・コントローラ
- ハイサイド N チャネル MOSFET および同期式 N チャネル MOSFET 用ゲート駆動出力を内蔵
- 16 ピン PowerPAD™ パッケージ ($R_{\theta JC}$ = 2°C/W)
- サーマル・シャットダウン
- 外部同期可能
- プログラム可能なハイサイド検出の短絡保護
- プログラマブルな閉ループのソフト・スタート
- TPS40054 ソースのみ
- TPS40055 ソースおよびシンク
- TPS40057 V_O プリバイアス付きのソースおよびシンク

2 アプリケーション

- パワー・モジュール
- ネットワーキングとテレコム
- 産業用およびサーバー

3 概要

TPS4005x は、高電圧で入力電圧範囲が広い (8V～40V) 同期整流降圧コントローラのファミリです。TPS4005x ファミリは、ソフト・スタート、UVLO、動作周波数、電圧フィードフォワード、ハイサイド電流制限、ループ補償など各種の機能をユーザーがプログラム可能なため、柔軟な設計を行えます。

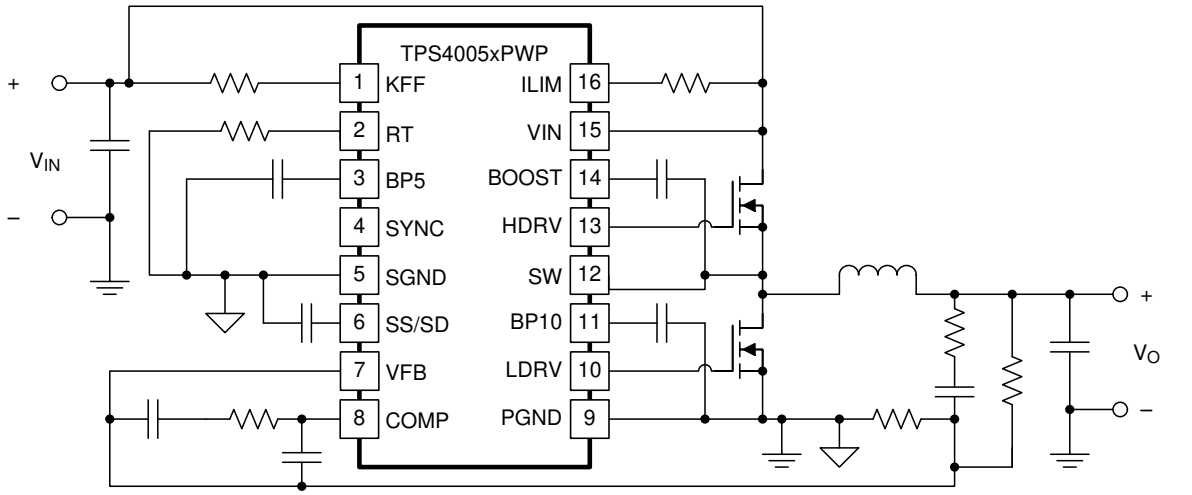
TPS4005x は、電圧フィードフォワード制御を実施することで、広い入力電圧範囲 (4:1) にわたって良好なライン・レギュレーションと、入力ライン過渡に対する高速な応答を実現します。入力が変動しても変調器のゲインがほぼ一定なので、ループ補償が容易です。電流制限を外部でプログラム可能なため、パルス単位の電流制限と、内部のフォルト・カウンタを使用した Hiccup モード動作が可能になり、より長い時間の過負荷に対応できます。

LM5145 と LM5146 は新製品で、BOM コストの削減、効率の向上、ソリューション・サイズの小型化など、多くの特長があります。LM5145 と LM5146 を使用する WEBENCH® 設計を開始。

製品情報

型番	パッケージ(1)	本体サイズ (公称)
TPS40054	HTSSOP (16)	5.00mm × 4.40mm
TPS40055		
TPS40057		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

Table of Contents

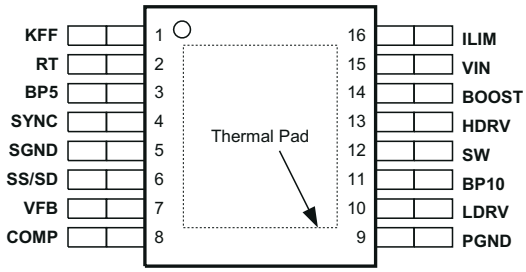
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (December 2014) to Revision J (June 2022)	Page
• LM5145 および LM5146 の特長の箇条書き項目を追加	1
• 従来の用語をすべてコントローラに変更	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Removed all TPS40055-Q1 references and third paragraph from セクション 8.2	21
• Removed TPS40055-Q1, TPS40192, TPS40193, and TPS40200 references from 表 11-1 in *Device Support* .	33

Changes from Revision H (July 2012) to Revision I (December 2014)	Page
• Added *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	3

5 Pin Configuration and Functions



A. For more information on the PWP package, refer to the *PowerPAD™ Thermally Enhanced Package* application report.
B. A PowerPAD heat slug must be connected to SGND (pin 5) or electrically isolated from all other pins.

図 5-1. 16-Pin PWP HTSSOP Package (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOST	14	O	Gate drive voltage for the high side N-channel MOSFET. The BOOST voltage is 9 V greater than the SW voltage. Connect a 0.1-µF ceramic capacitor from this pin to the drain of the lower MOSFET.
BP5	3	O	5-V reference. Bypass this pin to ground with a 0.1-µF ceramic capacitor. This pin can be used with an external DC load of 1 mA or less.
BP10	11	O	10-V reference used for gate drive of the N-channel synchronous rectifier. Bypass this pin with a 1-µF ceramic capacitor. This pin can be used with an external DC load of 1 mA or less.
COMP	8	O	Output of the error amplifier and input to the PWM comparator. A feedback network is connected from this pin to the VFB pin to compensate the overall loop. The COMP pin is internally clamped above the peak of the ramp to improve large signal transient response.
HDRV	13	O	Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).
ILIM	16	I	Current limit pin. Used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VCC. The voltage on this pin is compared to the voltage drop (VIN – SW) across the high-side MOSFET during conduction.
KFF	1	I	A resistor is connected from this pin to VIN to program the amount of voltage feedforward and UVLO level. The current fed into this pin is internally divided and used to control the slope of the PWM ramp.
LDRV	10	O	Gate drive for the N-channel synchronous rectifier. This pin switches from BP10 (MOSFET on) to ground (MOSFET off).
PGND	9		Power ground reference for the device. There should be a low-impedance path from this pin to the source or sources of the lower MOSFET or MOSFETs.
RT	2	I	A resistor is connected from this pin to ground to set the internal oscillator and switching frequency.
SGND	5	—	Signal ground reference for the device
SS/SD	6	I	Soft-start programming and shutdown pin. A capacitor connected from this pin to ground programs the soft-start time. The capacitor is charged with an internal current source of 2.3 µA. The resulting voltage ramp on the SS/SD pin is used as a second non-inverting input to the error amplifier. The output voltage begins to rise when $V_{SS/SD}$ is approximately 0.85 V. The output continues to rise and reaches regulation when $V_{SS/SD}$ is approximately 1.55 V. The controller is considered shut down when $V_{SS/SD}$ is 125 mV or less. The internal circuitry is enabled when $V_{SS/SD}$ is 210 mV or greater. When $V_{SS/SD}$ is less than approximately 0.85 V, the outputs cease switching and the output voltage (V_O) decays while the internal circuitry remains active.
SW	12	I	This pin is connected to the switched node of the converter and used for overcurrent sensing. The TPS40054 also uses this pin for zero current sensing.
SYNC	4	I	Synchronization input for the device. This pin can be used to synchronize the oscillator to an external controller frequency. If synchronization is not used, connect this pin to SGND.
VFB	7	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage, 0.7 V.
VIN	15	I	Supply voltage for the device

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

			MIN	MAX	UNIT
V_{IN}	Input voltage	VFB, SS/SD, SYNC	–0.3	6	V
		VIN, SW	–0.3	45	
		SW, transient < 50 ns		–2.5	
		SW, transient < 50 ns, V_{VIN} < 14 V		–5	
		KFF, with $I_{IN(max)}$ = – 5 mA	–0.3	11	
V_O	Output voltage	COMP, RT, SS/SD	–0.3	6	mA
		KFF		5	
I_O	Output current	RT		200	µA
T_J	Maximum junction temperature(2)			150	°C
T_J	Operating junction temperature		–40	125	
T_{stg}	Storage temperature range		–55	150	°C

(1) Stresses beyond those listed under may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device may shut down at junction temperatures below 150°C.

6.2 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	8	40	V
T_A	Operating free-air temperature	–40	85	°C

6.3 Thermal Information

THERMAL METRIC(1)		TPS4005x HTSSOP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	28	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.9	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.4 Electrical Characteristics

T_A = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 150 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range, VIN		8		40	V
OPERATING CURRENT						
I_{DD}	Quiescent current	Output drivers not switching, V_{FB} ≥ 0.75 V		1.5	3	mA
BP5						
V_{BP5}	Output voltage	I_O ≤ 1 mA	4.7	5	5.2	V
OSCILLATOR/RAMP GENERATOR						
f_{OSC}	Accuracy	8 V ≤ V_{IN} ≤ 40 V	470	520	570	kHz
V_{RAMP}	PWM ramp voltage(1)	V_{PEAK} – V_{VAL}		2		V
V_{IH}	High-level input voltage, SYNC		2			
V_{IL}	Low-level input voltage, SYNC				0.8	V
I_{SYNC}	Input current, SYNC			5	10	µA
	Pulse width, SYNC		50			ns
V_{RT}	RT voltage		2.38	2.5	2.58	V
D_{MAX}	Maximum duty cycle	V_{FB} = 0 V, f_{SW} ≤ 500 kHz	85%		94%	
		V_{FB} = 0 V, 500 kHz ≤ f_{SW} ≤ 1 MHz(1)	80%			
	Minimum duty cycle	V_{FB} ≥ 0.75 V			0%	
V_{KFF}	Feed-forward voltage		3.35	3.48	3.65	V
I_{KFF}	Feedforward current operating range(1) (2)		20		1100	µA
SOFT START						
$I_{SS/SD}$	Soft-start source current		1.65	2.35	2.95	µA
$V_{SS/SD}$	Soft-start clamp voltage			3.7		V
t_{DSCH}	Discharge time	$C_{SS/SD}$ = 220 pF	1.6	2.2	2.8	µs
$t_{SS/SD}$	Soft-start time	$C_{SS/SD}$ = 220 pF, 0 V ≤ $V_{SS/SD}$ ≤ 1.6 V	115	150	215	
BP10						
V_{BP10}	Output voltage	I_O ≤ 1 mA	9	9.6	10.3	V
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage	8 V ≤ V_{IN} ≤ 40 V, T_A = 25°C	0.698	0.7	0.704	V
		8 V ≤ V_{IN} ≤ 40 V, 0°C ≤ T_A ≤ 85°C	0.693	0.7	0.707	
		8 V ≤ V_{IN} ≤ 40 V, -40°C≤ T_A ≤ 85°C	0.693	0.7	0.715	
G_{BW}	Gain bandwidth(1)		3	5		MHz
A_{VOL}	Open loop gain		60	80		dB
I_{OH}	High-level output source current		2	4		mA
I_{OL}	Low-level output sink current		2	4		
V_{OH}	High-level output voltage	I_{SOURCE} = 500 µA	3.2	3.5		V
V_{OL}	Low-level output voltage	I_{SINK} = 500 µA		0.2	0.35	
I_{BIAS}	Input bias current	V_{FB} = 0.7 V		100	200	nA

T_A = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 150 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{SINK}	Current limit sink current		8.5	10	11.5	µA
	Propagation delay to output	V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 0.5 V)		300		ns
		V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 2 V)		200		
t_{ON}	Switch leading-edge blanking pulse time(1)		100			
t_{OFF}	Off time during a fault (soft-start cycle time)			7		cycles
V_{OS}	Offset voltage SW versus ILIM	T_A = 25°C	–90	–70	–50	mV
		V_{ILIM} = 23.6 V, 0°C ≤ T_A ≤ 85°C	–120		–38	
		V_{ILIM} = 23.6 V, -40°C ≤ T_A ≤ 85°C	–120		–20	
OUTPUT DRIVER						
t_{LRISE}	Low-side driver rise time	C_{LOAD} = 2200 pF		48	96	ns
t_{LFALL}	Low-side driver fall time			24	48	
t_{HRISE}	High-side driver rise time	C_{LOAD} = 2200 pF (HDRV – SW)		48	96	
t_{HFALL}	High-side driver fall time			36	72	
V_{OH}	High-level output voltage, HDRV	I_{HDRV} = –0.1 A (HDRV – SW)	V_{BOOST} –1.5 V	V_{BOOST} –1 V		V
V_{OL}	Low-level ouput voltage, HDRV	I_{HDRV} = 0.1 A (HDRV – SW)			0.75	
V_{OH}	High-level ouput voltage, LDRV	I_{LDRV} = –0.1 A	V_{BP10} –1.4 V	V_{BP10} – 1 V		
V_{OL}	Low-level output voltage, LDRV	I_{LDRV} = 0.1 A			0.5	
	Minimum controllable pulse width			100	150	ns
SS/SD SHUTDOWN						
V_{SD}	Shutdown threshold voltage	Outputs off	90	125	160	mV
V_{EN}	Device active threshold voltage		190	210	245	
BOOST REGULATOR						
V_{BOOST}	Output voltage	V_{IN}= 24 V	31.2	32.2	33.5	V
RECTIFIER ZERO CURRENT COMPARATOR (TPS40054 ONLY)						
V_{SW}	Switch voltage	LDRV output OFF	–10	–5	0	mV
SW NODE						
I_{LEAK}	Leakage current(1) (out of pin)				25	µA
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature(1)			165		°C
	Hysteresis(1)			20		
UVLO						
V_{UVLO}	KFF programmable threshold voltage	R_{KFF} = 28.7 kΩ	6.95	7.5	7.95	V
V_{DD}	UVLO, fixed		7.2	7.5	7.9	
V_{DD}	UVLO, hysteresis			0.46		

(1) Specified by design. Not production tested.
(2) I_{KFF} increases with SYNC frequency, maximum duty cycle decreases with I_{KFF}.

6.5 Typical Characteristics

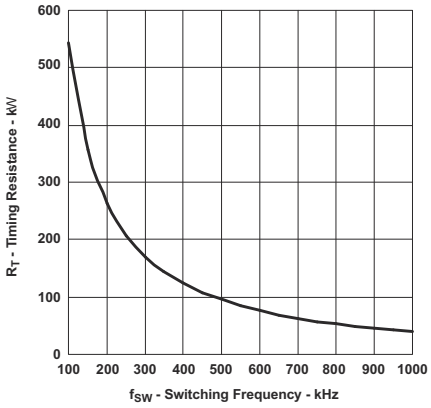


図 6-1. Switching Frequency vs Timing Resistance

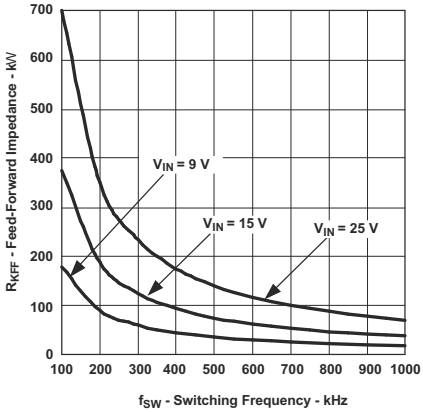


図 6-2. Feed-Forward Impedance vs Switching Frequency

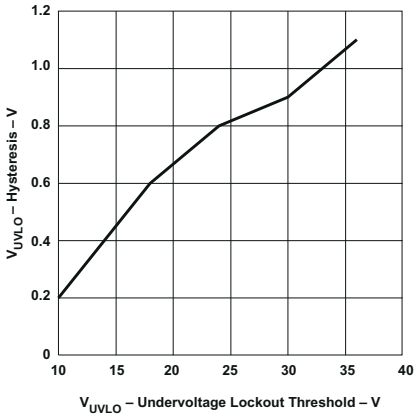


図 6-3. Undervoltage Lockout Threshold vs Hysteresis

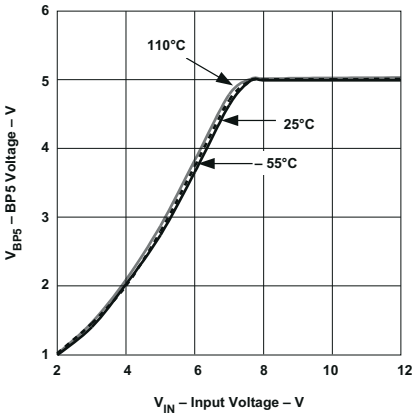


図 6-4. Input Voltage vs BP5 Voltage

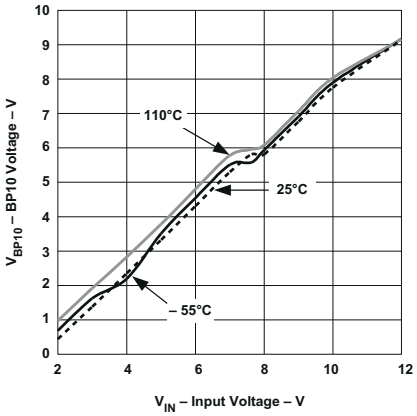


図 6-5. Input Voltage vs BP10 Voltage

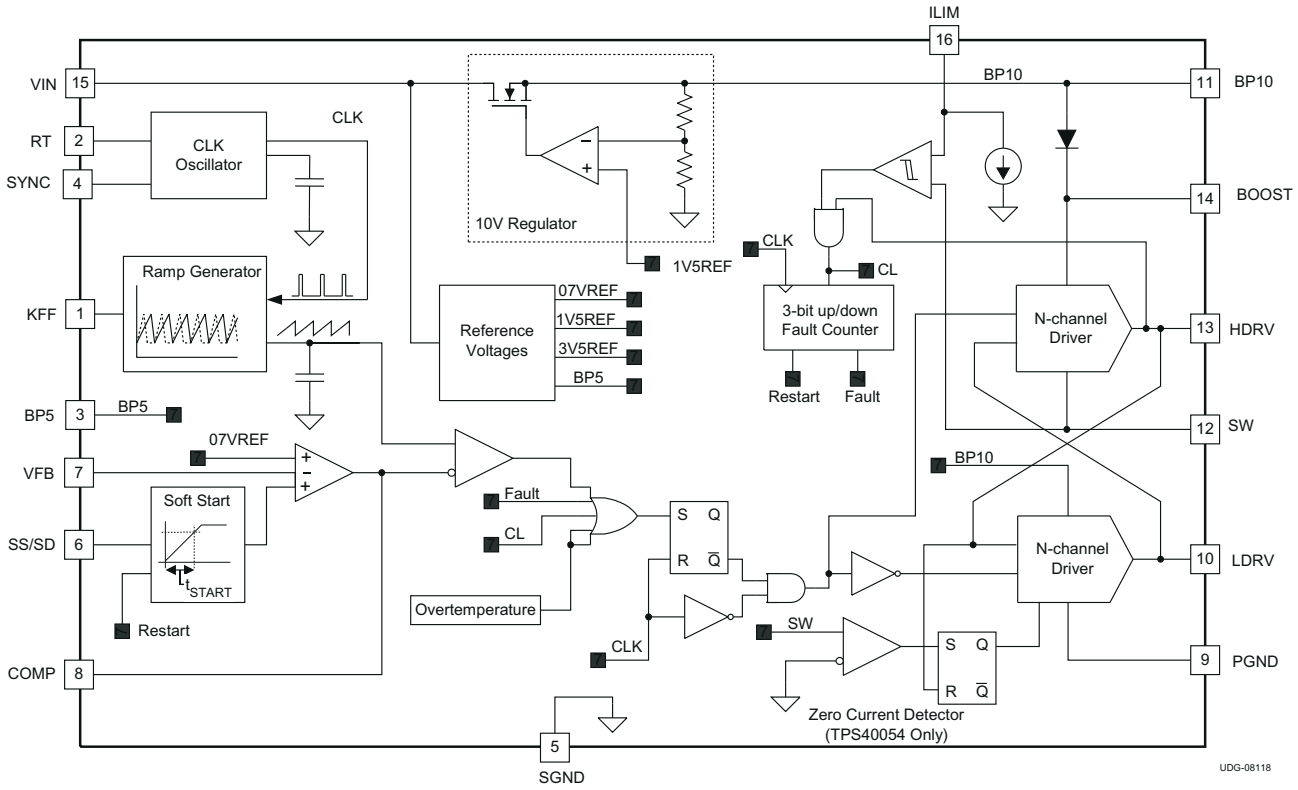
7 Detailed Description

7.1 Overview

The TPS4005x family of synchronous buck controllers are designed to operate over a wide range of input voltages (8 V to 40 V). These devices offer a variety of user programmable functions such as the following:

- Operating frequency
- Soft start
- Voltage feedforward
- High-side current limit
- External loop compensation

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Setting the Switching Frequency (Programming the Clock Oscillator)

The TPS4005x has independent clock oscillator and ramp generator circuits. The clock oscillator serves as the controller clock to the ramp generator circuit. The switching frequency, f_{SW} in kHz, of the clock oscillator is set by a single resistor (R_T) to ground. The clock frequency is related to R_T, in kΩ by 式 1 and the relationship is charted in 図 6-1.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 17 \right) k\Omega \quad (1)$$

7.3.2 Programming The Ramp Generator Circuit

The ramp generator circuit provides the actual ramp used by the PWM comparator. The ramp generator provides voltage feedforward control by varying the PWM ramp slope with line voltage, while maintaining a constant ramp magnitude. Varying the PWM ramp directly with line voltage provides excellent response to line variations because the PWM does not have to wait for loop delays before changing the duty cycle (see 図 7-1).

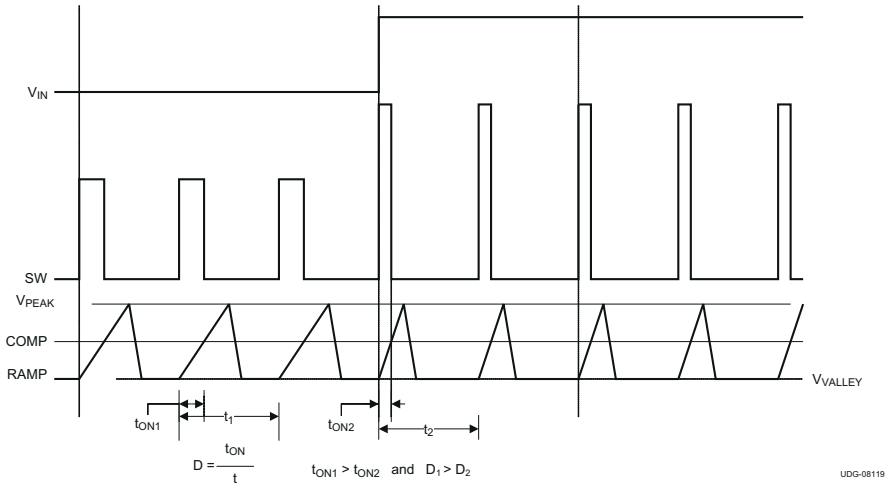


図 7-1. Voltage Feedforward Effect on PWM Duty Cycle

The PWM ramp must be faster than the controller clock frequency or the PWM is prevented from starting. The PWM ramp time is programmed through a single resistor (R_{KFF}) pulled up to VIN. R_{KFF} is related to R_T, and the minimum input voltage, $V_{IN(min)}$, through the following:

$$R_{KFF} = \left(V_{IN(min)} - V_{KFF}\right) \times \left(58.14 \times R_T + 1340\right)\ \Omega \quad (2)$$

where

- $V_{IN(min)}$ is the ensured minimum start-up voltage (the actual start-up voltage is nominally about 10% lower at 25°C). $V_{IN(min)}$ must be programmed equal to or greater than 8 V to ensure start-up and shutdown through the programmed UVLO through the KFF pin.
- R_T is the timing resistance in kΩ.
- V_{KFF} is the voltage at the KFF pin (typical value is 3.48 V).

The curve showing the R_{KFF} required for a given switching frequency, f_{SW}, and V_{UVLO} is shown in 図 6-2.

For low-input voltage and high duty-cycle applications, the voltage feedforward can limit the duty cycle prematurely, but does not occur for most applications. The voltage control loop controls the duty cycle and regulates the output voltage. For more information on large duty cycle operation, refer to the *Effect of Programmable UVLO on Maximum Duty Cycle* application note.

7.3.3 UVLO Operation

The TPS4005x uses variable (user-programmable) UVLO protection. See the *Programming the Ramp Generator* section for more information on setting the UVLO voltage. The UVLO circuit holds the soft start low until the input voltage exceeds the user-programmable undervoltage threshold.

The TPS4005x uses the feedforward pin, KFF, as a user-programmable low-line UVLO detection. This variable low-line UVLO threshold compares the PWM ramp duration to the oscillator clock period. An undervoltage condition exists if the TPS4005x receives a clock pulse before the ramp has reached 90% of its full amplitude. The ramp duration is a function of the ramp slope, which is directly related to the current into the KFF pin. The KFF current is a function of the input voltage and the resistance from KFF to the input voltage. The KFF resistor can be referenced to the oscillator frequency as described in 式 2.

The programmable UVLO function uses a 3-bit counter to prevent spurious shutdowns or turn-ons due to spikes or fast line transients. When the counter reaches a total of seven counts in which the ramp duration is shorter than the clock cycle, a power-good signal is asserted and a soft start initiated, and the upper and lower MOSFETS are turned off.

Once the soft start is initiated, the UVLO circuit must see a total count of seven cycles in which the ramp duration is longer than the clock cycle before an undervoltage condition is declared (see 図 7-2).

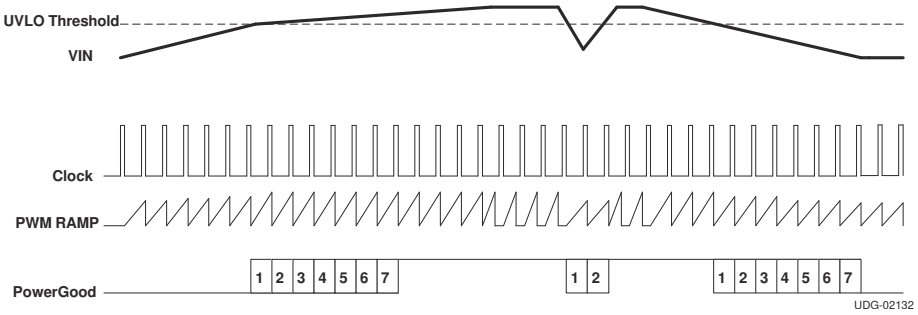


図 7-2. Undervoltage Lockout Operation

The tolerance on the UVLO set point also affects the maximum duty cycle achievable. If the UVLO starts the device at 10% below the nominal start-up voltage, the maximum duty cycle is reduced approximately 10% at the nominal start-up voltage.

The impedance of the input voltage can cause the input voltage, at the controller, to sag when the converter starts to operate and draw current from the input source. Therefore, there is voltage hysteresis that prevents nuisance shutdowns at the UVLO point. With R_T chosen to select the operating frequency and R_{KFF} chosen to select the start-up voltage, the approximate amount of hysteresis voltage is shown in 図 6-3.

Some applications can require an additional circuit to prevent false restarts at the UVLO voltage level. This applies to applications that have high impedance on the input voltage line or that have excessive ringing on the V_{IN} line. The input voltage impedance can cause the input voltage to sag enough at start-up to cause a UVLO shutdown and subsequent restart. Excessive ringing can also affect the voltage seen by the device and cause a UVLO shutdown and restart. A simple external circuit provides a selectable amount of hysteresis to prevent the nuisance UVLO shutdown.

Assuming a hysteresis current of 10% I_{KFF}, and the peak detector charges to 8 V and $V_{IN(min)}$ = 10 V, the value of R_A is calculated by 式 3 using a R_{KFF} = 71.5 kΩ.

$$R_A = \frac{R_{KFF} \times (8 - 3.48)}{0.1 \times \left(V_{IN(min)} - 3.48\right)} = 495\,k\Omega = 499\,k\Omega \tag{3}$$

C_A is chosen to maintain the peak voltage between switching cycles to keep the capacitor charge from drooping 0.1 V (from 8 V to 7.9 V).

$$C_A = \frac{(8 - 3.48)}{(R_A \times 7.9 \times f_{SW})} \tag{4}$$

The value of C_A can calculate to less than 10 pF, but some standard value up to 47 pF works adequately. The diode can be a small-signal switching diode or Schottky rated for more then 20 V. 図 7-3 shows a typical implementation using a small switching diode.

The tolerance on the UVLO set point also affects the maximum duty cycle achievable. If the UVLO starts the device at 10% below the nominal start-up voltage, the maximum duty cycle is reduced approximately 10% at the nominal start-up voltage.

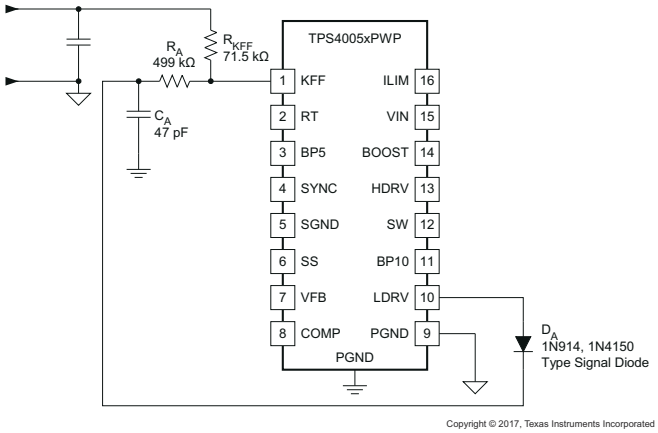


図 7-3. Hysteresis for Programmable UVLO

7.3.4 BP5 and BP10 Internal Voltage Regulators

Start-up characteristics of the BP5 and BP10 regulators over different temperature ranges are shown in 図 6-4 and 図 6-5. Slight variations in the BP5 occurs dependent upon the switching frequency. Variation in the BP10 regulation characteristics is also based on the load presented by switching the external MOSFETs.

7.3.5 Programming Soft Start

The TPS4005x uses a closed-loop soft-start system to ensure a controlled ramp of the output during start-up. The reference voltage used for the start-up is derived in the following manner. A capacitor ($C_{SS/SD}$) is connected to the SS/SD pin. There is a ramped voltage generated at this pin by charging $C_{SS/SD}$ with a current source. A value of 0.85 V is subtracted from the voltage at the SS/SSD pin and is applied to a non-inverting input of the error amplifier. This is the effective soft-start ramp voltage, V_{SSRMP}. The error amplifier also has the 0.7-V reference (V_{FB}) voltage applied to a non-inverting input. The structure of the error amplifier input stage is such that the lower of V_{FB} or V_{SSRMP} becomes the dominant voltage that the error amplifier uses to regulate the FB pin. This provides a clean, closed-loop start-up while V_{SSRMP} is lower than V_{FB} and a precision reference regulated supply as V_{SSRMP} climbs above V_{FB}. To ensure a controlled ramp-up of the output voltage, the soft-start time must be greater than the L-C_O time constant as described in 式 5.

$$t_{START} \geq 2\pi \times \sqrt{L \times C_O} \quad \text{(seconds)} \tag{5}$$

where

- t_{START} is the start-up ramp time in s.

There is a direct correlation between t_{START} and the input current required during start-up. The faster t_{START}, the higher the input current required during start-up. This relationship is described in more detail in the *Programming the Current Limit* section. The soft-start capacitance, $C_{SS/SD}$, is described in 式 6.

For applications in which the V_{IN} supply ramps up slowly (typically between 50 ms and 100 ms), it can be necessary to increase the soft-start time to between approximately 2 ms and 5 ms to prevent nuisance UVLO tripping. The soft-start time must be longer than the time that the V_{IN} supply transitions between 6 V and 7 V.

$$C_{SS/SD} = \left(\frac{I_{SS/SD}}{V_{FB}} \right) \times t_{START} \, (F) \tag{6}$$

where

- $I_{SS/SD}$ is the soft-start charge current (typical value is 2.35 µA).
- V_{FB} is the feedback reference voltage (typical value is 0.7 V).

7.3.6 Programming Current Limit

The TPS4005x uses a two-tier approach for overcurrent protection. The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when the gate is driven high. The MOSFET voltage is compared to the voltage dropped across a resistor connected from VIN pin to the ILIM pin when driven by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor, the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated.

The second tier consists of a fault counter. The fault counter is incremented on an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven, a restart is issued and seven soft-start cycles are initiated. Both the upper and lower MOSFETs are turned off during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero, the PWM is re-enabled. If the fault has been removed, the output starts up normally. If the output is still present, the counter counts seven overcurrent pulses and re-enters the second-tier fault mode. See 図 7-4 for typical overcurrent protection waveforms.

The minimum current limit setpoint (I_{ILIM}) is calculated in 式 7.

$$I_{ILIM} = \left(\frac{C_O \times V_O}{t_{START}} \right) + I_{LOAD} \, (A) \tag{7}$$

where

- I_{LOAD} is the load current at start-up.

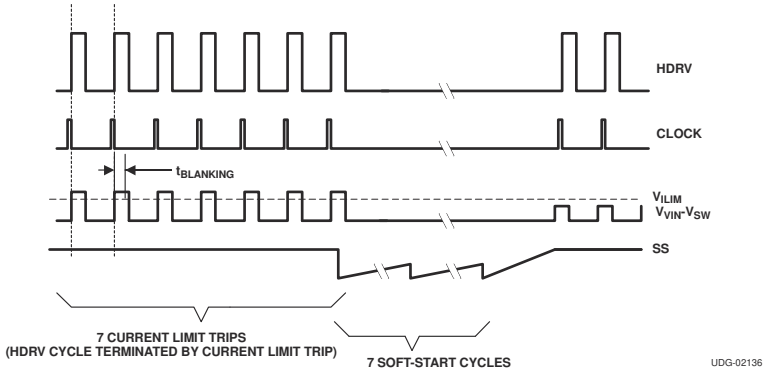


図 7-4. Typical Current Limit Protection Waveforms

The current limit programming resistor (R_{ILIM}) is calculated using 式 8. Care must be taken in choosing the values used for V_{OS} and I_{SINK} in the equation. To ensure the output current at the overcurrent level, the minimum value of I_{SINK} and the maximum value of V_{OS} must be used. The main purpose is hard fault protection of the power switches.

$$R_{ILIM} = \frac{I_{OC} \times R_{DS(on)[max]} + V_{OS}}{1.12 \times I_{SINK}} + \frac{42.86 \times 10^{-3}}{I_{SINK}} \, (\Omega) \tag{8}$$

where

- I_{SINK} is the current into the ILIM pin and is 8.5 µA, minimum.
- I_{OC} is the overcurrent setpoint, which is the DC output current plus one-half of the peak inductor current.
- V_{OS} is the overcurrent comparator offset and is –20 mV maximum.

7.3.7 Synchronizing to an External Supply

The TPS4005x can be synchronized to an external clock through the SYNC pin. Synchronization occurs on the falling edge of the SYNC signal. The synchronization frequency must be in the range of 20% to 30% higher than its programmed free-run frequency. The clock frequency at the SYNC pin replaces the controller clock generated by the oscillator circuit. Pulling the SYNC pin low programs the TPS4005x to freely run at the frequency programmed by R_T.

The higher synchronization must be factored in when programming the PWM ramp generator circuit. If the PWM ramp is interrupted by the SYNC pulse, a UVLO condition is declared and the PWM becomes disabled. Typically, this is of concern under low-line conditions only. In any case, R_{KFF} needs to be adjusted for the higher switching frequency. In order to specify the correct value for R_{KFF} at the synchronizing frequency, calculate a *dummy* value for R_T that would cause the oscillator to run at the synchronizing frequency. Do not use this value of RT in the design.

$$R_{T(dummy)} = \left(\frac{1}{f_{SYNC} \times 17.82 \times 10^{-6}} - 17 \right) (k\Omega) \tag{9}$$

where

- f_{SYNC} is the synchronizing frequency in kHz.

Use the value of $R_{T(dummy)}$ to calculate the value for R_{KFF}.

$$R_{KFF} = \left(V_{IN(min)} - V_{KFF} \right) \times \left(58.14 \times R_{T(dummy)} + 1340 \right) \Omega \tag{10}$$

where

- $R_{T(dummy)}$ is in kΩ.

This value of R_{KFF} ensures that UVLO is not engaged when operating at the synchronization frequency.

7.3.8 Loop Compensation

Voltage-mode buck-type converters are typically compensated using Type III networks. Since the TPS4005x uses voltage feedforward control, the gain of the PWM modulator with voltage feedforward circuit must be included. The generic modulator gain is described in 図 7-5. Duty cycle, D, varies from 0 to 1 as the control voltage, V_C, varies from the minimum ramp voltage to the maximum ramp voltage, V_S. Also, for a synchronous buck converter, $D = V_O / V_{IN}$. To get the control voltage to output voltage modulator gain in terms of the input voltage and ramp voltage:

$$D = \frac{V_O}{V_{IN}} = \frac{V_C}{V_S} \quad \text{or} \quad \frac{V_O}{V_C} = \frac{V_{IN}}{V_S} \tag{11}$$

With the voltage feedforward function, the ramp slope is proportional to the input voltage. Therefore, the moderator DC gain is independent to the change of input voltage.

For the TPS4005x, with $V_{IN(min)}$ being the minimum input voltage required to cause the ramp excursion to reach the maximum ramp amplitude of V_{RAMP}, the modulator DC gain is shown in 式 12.

$$A_{MOD} = \left(\frac{V_{IN(min)}}{V_{RAMP}} \right) \quad \text{or} \quad A_{MOD(dB)} = 20 \times \log \left(\frac{V_{IN(min)}}{V_{RAMP}} \right) \tag{12}$$

For a buck converter using voltage mode control, there is a double pole due to the output L-C_O. The double pole is located at the frequency calculated in 式 13.

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_O}} \quad \text{(Hertz)} \tag{13}$$

There is also a zero created by the output capacitance, C_O, and its associated ESR. The ESR zero is located at the frequency calculated in 式 14.

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(Hertz)} \tag{14}$$

Calculate the value of R_{BIAS} to set the output voltage, V_O.

$$R_{BIAS} = \frac{0.7 \times R1}{V_O - 0.7} \ \Omega \tag{15}$$

The maximum crossover frequency (0 dB loop gain) is set by 式 16.

$$f_C = \frac{f_{SW}}{4} \quad \text{(Hertz)} \tag{16}$$

Typically, f_C is selected to be close to the midpoint between the L-C_O double pole and the ESR zero. At this frequency, the control to output gain has a –2 slope (–40 dB/decade), while the Type III topology has a +1 slope (20 dB/decade), resulting in an overall closed loop –1 slope (–20 dB/decade). 図 7-6 shows the modulator gain, L-C filter, output capacitor ESR zero, and the resulting response to be compensated.

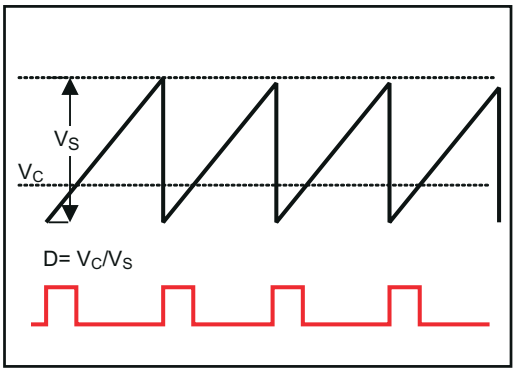


図 7-5. PWM Modulator Relationships

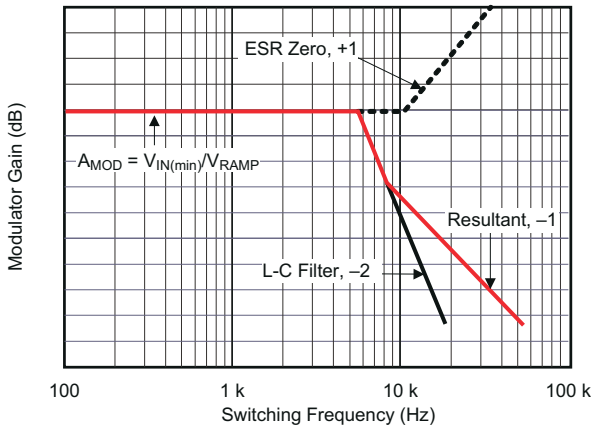


図 7-6. Modulator Gain vs Switching Frequency

A Type III topology, shown in 図 7-7, has two zero-pole pairs in addition to a pole at the origin. The gain and phase boost of a Type III topology is shown in 図 7-8. The two zeros are used to compensate the L-C_O double pole and provide phase boost. The double pole is used to compensate for the ESR zero and provide controlled gain roll-off. In many cases, the second pole can be eliminated and the gain roll-off of the amplifier is used to roll-off the overall gain at higher frequencies.

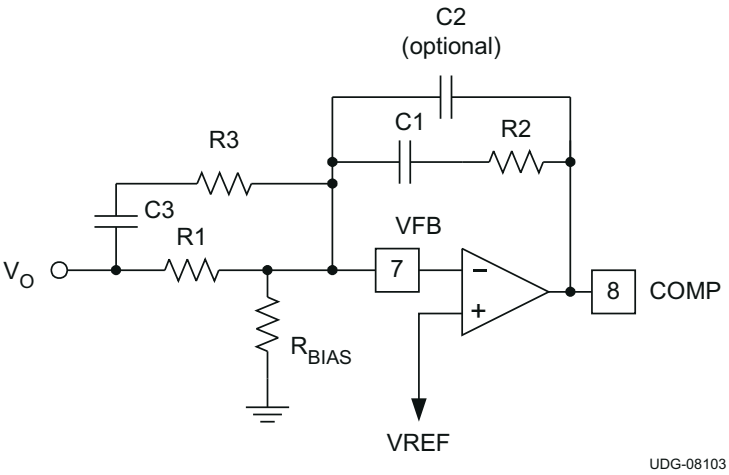


図 7-7. Type III Compensation Configuration

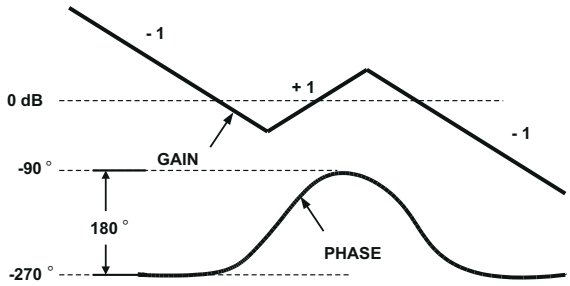


図 7-8. Type III Compensation Gain and Phase

The poles and zeros for a Type III network are described in 式 17 through 式 20.

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \ (Hz) \quad (17)$$

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \ (Hz) \quad (18)$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \ (Hz) \quad (19)$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \ (Hz) \quad (20)$$

The value of R1 is somewhat arbitrary, but influences other component values. A value between 50 kΩ and 100 kΩ usually yields reasonable values.

The unity gain frequency is described in 式 21.

$$f_C = \frac{1}{2\pi \times R1 \times C2 \times G} \ (Hertz) \quad (21)$$

where

- G is the reciprocal of the modulator gain at f_C.

The modulator gain as a function of frequency at f_C is described in 式 22.

$$A_{MOD(f)} = A_{MOD} \times \left(\frac{f_{LC}}{f_C}\right)^2 \text{ and } G = \frac{1}{A_{MOD(f)}} \quad (22)$$

Care must be taken not to load down the output of the error amplifier with the feedback resistor, R2, that is too small. The error amplifier has a finite output source and sink current, which must be considered when sizing R2. A value that is too small does not allow the output to swing over its full range.

$$R2_{(MIN)} = \frac{V_{C\ (max)}}{I_{SOURCE\ (min)}} = \frac{3.5\ V}{2\ mA} = 1750\ \ \Omega \tag{23}$$

7.4 Device Functional Modes

The TPS40057 is safe for prebiased outputs, not turning on the synchronous rectifier until the high-side FET has already started switching. The TPS40054 operates in one quadrant and sources output current only, allowing for paralleling of converters and ensures that one converter does not sink current from another converter. This controller also emulates a non-synchronous buck converter at light loads where the inductor current goes discontinuous. At continuous output inductor currents, the controller operates as a synchronous buck converter to optimize efficiency. The TPS40055 operates in two quadrants, sourcing and sinking output current.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS4005x family of synchronous buck controllers are designed to operate over a wide range of input voltages (8 V to 40 V). These devices are used to convert a higher DC input voltage to a lower DC output voltage for a variety of applications. Use the following design procedure to select key component values for this family of devices.

8.1.1 Selecting the Inductor Value

The inductor value determines the magnitude of ripple current in the output capacitors as well as the load current at which the converter enters discontinuous mode. Too large an inductance results in lower ripple current but is physically larger for the same load current. An inductance that is too small results in larger ripple currents and a greater number of (or more expensive output capacitors for) the same output ripple voltage requirement. A good compromise is to select the inductance value such that the converter does not enter discontinuous mode until the load approximated somewhere between 10% and 30% of the rated output. The inductance value is described in 式 24.

$$L = \frac{(V_{IN} - V_O) \times V_O}{V_{IN} \times \Delta I \times f_{SW}} \quad \text{(Henries)} \tag{24}$$

where

- V_O is the output voltage.
- ΔI is the peak-to-peak inductor current.

8.1.2 Calculating the Output Capacitance

The output capacitance depends on the output ripple voltage requirement, output ripple current, as well as any output voltage deviation requirement during a load transient.

The output ripple voltage is a function of both the output capacitance and capacitor ESR. The worst-case output ripple is described in 式 25.

$$\Delta V = \Delta I \times \left(ESR + \left(\frac{1}{8 \times C_O \times f_{SW}} \right) \right) \tag{25}$$

where

- C_O is the output capacitance.
- ESR is the equivalent series resistance of the output capacitance.

The output ripple voltage is typically between 90% and 95% due to the ESR component.

The output capacitance requirement typically increases in the presence of a load transient requirement. During a step load, the output capacitance must provide energy to the load (light to heavy load step) or absorb excess inductor energy (heavy to light load step) while maintaining the output voltage within acceptable limits. The amount of capacitance depends on the magnitude of the load step, the speed of the loop, and the size of the inductor.

Stepping the load from a heavy load to a light load results in an output overshoot. Excess energy stored in the inductor must be absorbed by the output capacitance. The energy stored in the inductor is described in 式 26.

$$E_L = \frac{1}{2} \times L \times I^2 \quad \text{(Joules)} \tag{26}$$

where

$$I^2 = \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right] \quad \left(\text{(Amperes)}^2 \right) \tag{27}$$

- I_{OH} is the output current under heavy load conditions.
- I_{OL} is the output current under light load conditions.

Energy in the capacitor is described in 式 28.

$$E_C = \frac{1}{2} \times C \times V^2 \quad \text{(Joules)} \tag{28}$$

where

$$V^2 = \left[\left(V_f\right)^2 - \left(V_i\right)^2 \right] \quad \left(\text{Volts}^2 \right) \tag{29}$$

where

- V_f is the final peak capacitor voltage.
- V_i is the initial capacitor voltage.

Substituting 式 27 into 式 26, then substituting 式 29 into 式 28, then setting 式 28 equal to 式 26, and then solving for C_O yields the capacitance described in 式 30.

$$C_O = \frac{L \times \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right]}{\left[\left(V_f\right)^2 - \left(V_i\right)^2 \right]} \quad \text{(Farads)} \tag{30}$$

8.1.3 Calculating the Boost and BP10 Bypass Capacitor

The BOOST capacitance provides a local, low impedance source for the high-side driver. The BOOST capacitor must be a good quality, high-frequency capacitor. The size of the bypass capacitor depends on the total gate charge of the MOSFET and the amount of droop allowed on the bypass capacitor. The BOOST capacitance is described in 式 31.

$$C_{BOOST} = \frac{Q_g}{\Delta V} \quad \text{(Farads)} \tag{31}$$

The 10-V reference pin, BP10V provides energy for both the synchronous MOSFET and the high-side MOSFET through the BOOST capacitor. Neglecting any efficiency penalty, the BP10V capacitance is described in 式 32.

$$C_{BP10} = \frac{\left(Q_{gHS} + Q_{gSR}\right)}{\Delta V} \quad \text{(Farads)} \tag{32}$$

8.1.4 DV-DT Induced Turn-On

MOSFETs are susceptible to dv/dt turn-on particularly in high-voltage (V_{DS}) applications. The turn-on is caused by the capacitor divider that is formed by C_{GD} and C_{GS}. High dv/dt conditions and drain-to-source voltage on the MOSFET causes current flow through C_{GD} and causes the gate-to-source voltage to rise. If the gate-to-source voltage rises above the MOSFET threshold voltage, the MOSFET turns on, resulting in large shoot-through currents. Therefore, the SR MOSFET should be chosen so that the Q_{GD} charge is smaller than the Q_{GS} charge.

8.1.5 High-Side MOSFET Power Dissipation

The power dissipated in the external high-side MOSFET is comprised of conduction and switching losses. The conduction losses are a function of the I_{RMS} current through the MOSFET and the $R_{DS(on)}$ of the MOSFET. The high-side MOSFET conduction losses are defined by 式 33.

$$P_{COND} = \left(I_{RMS}\right)^2 \times R_{DS(on)} \times \left(1 + TC_R \times \left[T_J - 25^{\circ}C\right]\right) \quad (\text{Watts}) \tag{33}$$

where

- TC_R is the temperature coefficient of the MOSFET $R_{DS(on)}$.

The TC_R varies depending on MOSFET technology and manufacturer, but typically ranges between 3500 ppm/°C and 7000 ppm/°C.

The I_{RMS} current for the high-side MOSFET is described in 式 34.

$$I_{RMS} = I_{OUT} \times \sqrt{d} \quad \left(A_{RMS}\right) \tag{34}$$

The switching losses for the high-side MOSFET are described in 式 35.

$$P_{SW(fsw)} = \left(V_{IN} \times I_{OUT} \times t_{SW}\right) \times f_{SW} \quad (\text{Watts}) \tag{35}$$

where

- I_O is the DC output current.
- t_{SW} is the switching rise time, typically < 20 ns.
- f_{SW} is the switching frequency.

Typical switching waveforms are shown in 図 8-1.

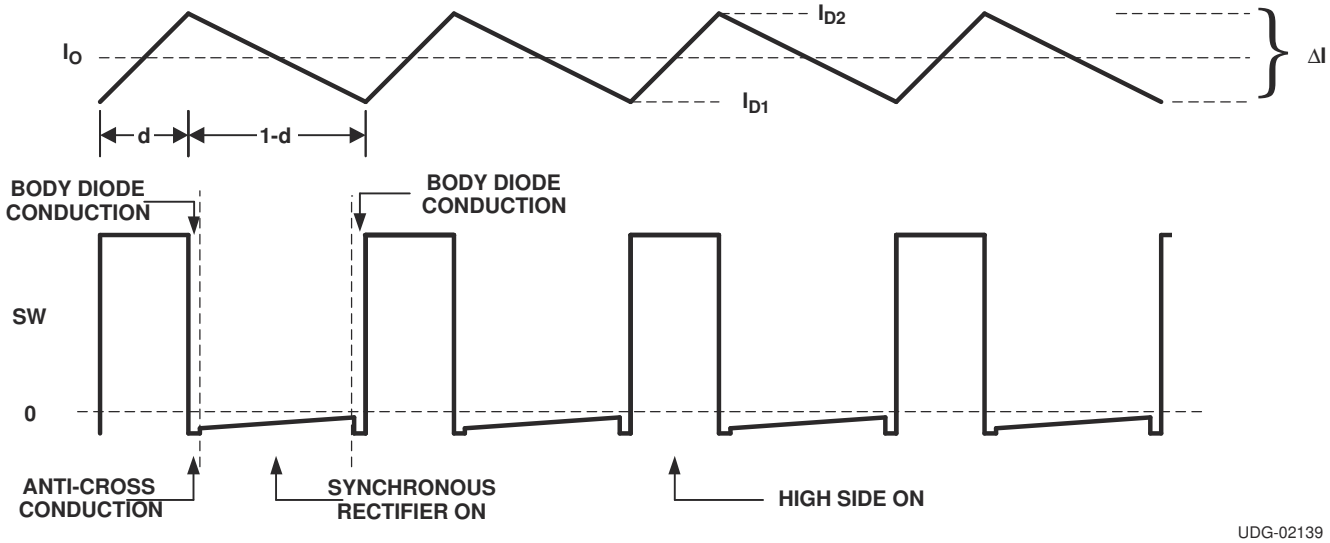


図 8-1. Inductor Current and SW Node Waveforms

The maximum allowable power dissipation in the MOSFET is determined by 式 36.

$$P_T = \frac{\left(T_J - T_A\right)}{\theta_{JA}} \quad \text{(Watts)} \tag{36}$$

where

- $P_T = P_{COND} + P_{SW(fsw)\ (W)}$.
- θ_{JA} is the package thermal impedance.

8.1.6 Synchronous Rectifier MOSFET Power Dissipation

The power dissipated in the synchronous rectifier MOSFET is comprised of three components: $R_{DS(on)}$ conduction losses, body diode conduction losses, and reverse recovery losses. $R_{DS(on)}$ conduction losses can be defined using 式 31 and the RMS current through the synchronous rectifier MOSFET is described in 式 37.

$$I_{RMS} = I_O \times \sqrt{1 - d} \quad \left(\text{Amperes}_{RMS}\right) \tag{37}$$

The body-diode conduction losses are due to forward conduction of the body diode during the anti-cross conduction delay time. The body diode conduction losses are described by 式 38.

$$P_{DC} = 2 \times I_O \times V_F \times t_{DELAY} \times f_{SW} \quad \text{(Watts)} \tag{38}$$

where

- V_F is the body diode forward voltage.
- t_{DELAY} is the delay time just before the SW node rises.

The 2-multiplier is used because the body diode conducts twice during each cycle (once on the rising edge and once on the falling edge). The reverse recovery losses are due to the time it takes for the body diode to recover from a forward bias to a reverse blocking state. The reverse recovery losses are described in 式 39.

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} \quad \text{(Watts)} \tag{39}$$

where

- Q_{RR} is the reverse recovery charge of the body diode.

The Q_{RR} is not always described in a MOSFET data sheet, but can be obtained from the MOSFET vendor. The total synchronous rectifier MOSFET power dissipation is described in 式 40.

$$P_{SR} = P_{DC} + P_{RR} + P_{COND} \quad \text{(Watts)} \tag{40}$$

8.1.7 TPS4005x Power Dissipation

The power dissipation in the TPS4005x is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance (refer to the *PowerPAD Thermally Enhanced Package* application note) can be calculated from 式 41.

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad \text{(Watts/driver)} \tag{41}$$

And the total power dissipation in the TPS4005x, assuming the same MOSFET is selected for both the high-side and synchronous rectifier, is described in 式 42.

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{42}$$

or

$$P_T = \left(2 \times Q_g \times f_{SW} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{43}$$

where

- I_Q is the quiescent operating current (neglecting drivers).

The maximum power capability of the PowerPAD package is dependent on the layout as well as air flow. The thermal impedance from junction to air, assuming 2-oz. copper trace and thermal pad with solder and no air flow:

$$\theta_{JA} = 36.515°C/W \tag{44}$$

The maximum allowable package power dissipation is related to ambient temperature by 式 45.

$$P_T = \frac{T_J - T_A}{\theta_{JA}} \quad \text{(Watts)} \tag{45}$$

Substituting 式 38 into 式 43 and solving for f_{SW} yields the maximum operating frequency for the TPS4005x. The result is described in 式 46.

$$f_{SW} = \left(\frac{\left(\frac{(T_J - T_A)}{\theta_{JA} \times V_{IN}}\right) - I_Q}{2 \times Qg}\right) \text{(Hz)} \tag{46}$$

8.2 Typical Application

図 8-2 shows component selection for the 10-V to 24-V to 3.3-V at 8 A DC-to-DC converter specified in the design example. For an 8-V input application, it can be necessary to add a Schottky diode from BP10 to BOOST to get sufficient gate drive for the upper MOSFET. As seen in 図 6-4, the BP10 output is about 6 V with the input at 8 V, so the upper MOSFET gate drive can be less than 5 V.

A Schottky diode is shown connected across the synchronous rectifier MOSFET as an optional device that can be required if the layout causes excessive negative SW node voltage, greater than or equal to 2 V.

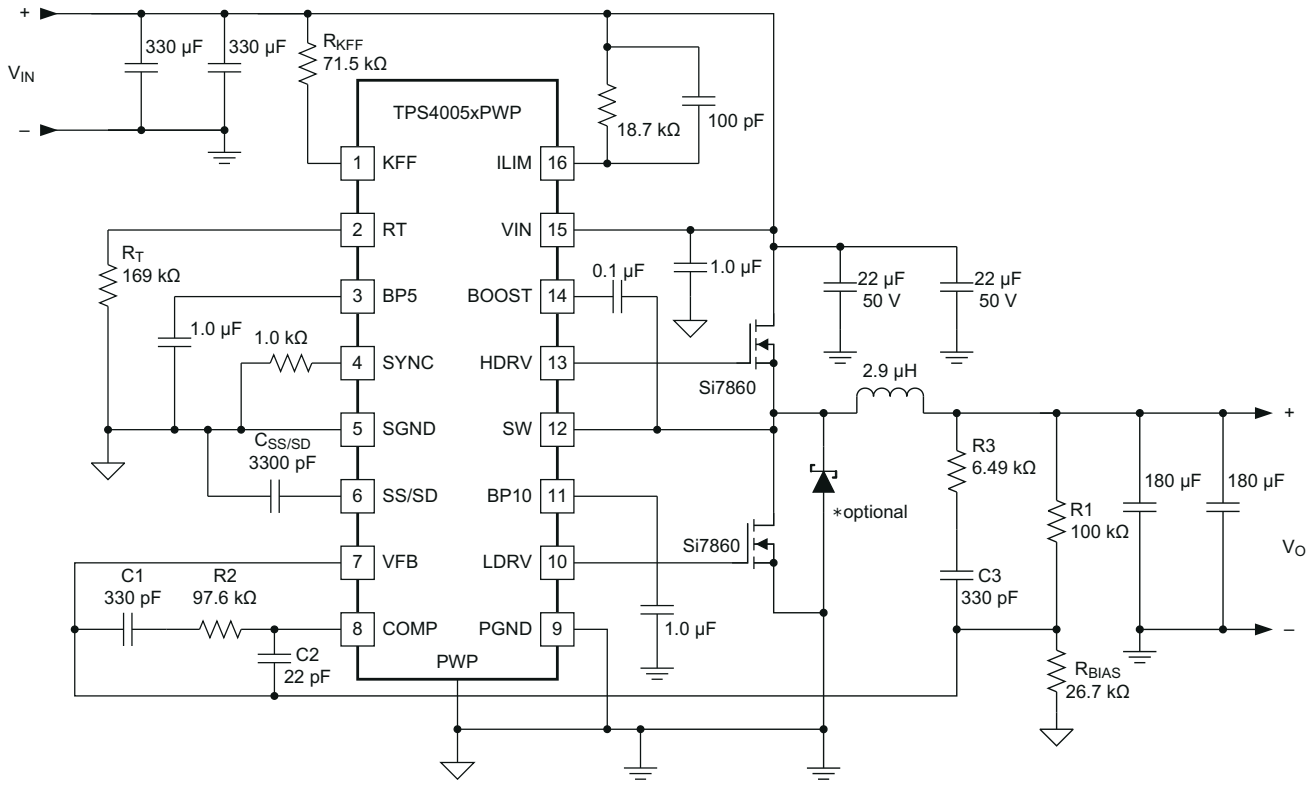


図 8-2. 24-V to 3.3-V at 8-A DC-DC Converter Design Example

8.2.1 Design Requirements

- Input voltage: 10 V_{DC} to 24 V_{DC}
- Output voltage: 3.3 V ±2% (3.234 ≤ V_O ≤ 3.366)
- Output current: 8 A (maximum, steady state), 10 A (surge, 10-ms duration, 10% duty cycle maximum)
- Output ripple: 33 mV_{PP} at 8 A
- Output load response: 0.3 V ≥ 10% to 90% step load change, from 1 A to 7 A
- Operating temperature: –40°C to 85°C
- f_{SW} = 300 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Calculate Maximum and Minimum Duty Cycles

$$D_{MIN} = \frac{V_{O(min)}}{V_{IN(max)}} = \frac{3.234}{24} = 0.135 \qquad D_{MAX} = \frac{V_{O(max)}}{V_{IN(min)}} = \frac{3.366}{10} = 0.337 \tag{47}$$

8.2.2.2 Select Switching Frequency

The switching frequency is based on the minimum duty cycle ratio and the propagation delay of the current limit comparator. In order to maintain current limit capability, the on time of the upper MOSFET, t_{ON}, must be greater than 300 ns (see the *Electrical Characteristics*). Therefore:

$$\left(\frac{V_{O(min)}}{V_{IN(max)}}\right) = \left(\frac{t_{ON}}{t_{SW}}\right) \text{ or } \frac{1}{t_{SW}} = f_{SW} = \left(\frac{\left(\frac{V_{O(min)}}{V_{IN(max)}}\right)}{t_{ON}}\right) \tag{48}$$

Using 400 ns to provide margin,

$$f_{SW} = \frac{0.135}{400\ ns} = 337\ kHz \tag{49}$$

Since the oscillator can vary by 10%, decrease f_{SW}, by 10%

$$f_{SW} = 0.9 \times 337\ kHz = 303\ kHz \tag{50}$$

and, therefore, choose a frequency of 300 kHz.

8.2.2.3 Select ΔI

In this case ΔI is chosen so that the converter enters discontinuous mode at 20% of nominal load.

$$\Delta I = I_O \times 2 \times 0.2 = 8 \times 2 \times 0.2 = 3.2\ A \tag{51}$$

8.2.2.4 Calculate the High-Side MOSFET Power Losses

Power losses in the high-side MOSFET (Si7860DP) at 24-V_{IN} where switching losses dominate can be calculated from 式 52.

$$I_{RMS} = I_O \times \sqrt{d} = 8 \times \sqrt{0.135} = 2.93\ A \tag{52}$$

Substituting 式 34 into 式 33 yields

$$P_{COND} = 2.93^2 \times 0.008 \times (1 + 0.007 \times (150 - 25)) = 0.129\ W \tag{53}$$

and from 式 35, the switching losses can be determined.

$$P_{SW(fsw)} = \left(V_{IN} \times I_O \times t_{SW}\right) \times f_{SW} = 24\ V \times 8\ A \times 20\ ns \times 300\ kHz = 1.152\ W \tag{54}$$

The MOSFET junction temperature can be found by substituting 式 53 and 式 54 into 式 36:

$$T_J = \left(P_{COND} + P_{SW}\right) \times \theta_{JA} + T_A = (0.129 + 1.152) \times 40 + 85 = 136°C \tag{55}$$

8.2.2.5 Calculate Synchronous Rectifier Losses

The synchronous rectifier MOSFET has two loss components, conduction, and diode reverse recovery losses. The conduction losses are due to I_{RMS} losses as well as body diode conduction losses during the dead time associated with the anti-cross conduction delay.

The I_{RMS} current through the synchronous rectifier from 式 37:

$$I_{RMS} = I_O \times \sqrt{1 - d} = 8 \times \sqrt{1 - 0.135} = 7.44\ A_{RMS} \tag{56}$$

The synchronous MOSFET conduction loss from 式 33 is:

$$P_{COND} = 7.44^2 \times 0.008 \times \left(1 + 0.007 \times (150 - 25)\right) = 0.83\,W \quad (57)$$

The body diode conduction loss from 式 38 is:

$$P_{DC} = 2 \times I_O \times V_{FD} \times t_{DELAY} \times f_{SW} = 2 \times 8.0\ A \times 0.8\ V \times 100\ ns \times 300\ kHz = 0.384 \quad (58)$$

The body diode reverse recovery loss from 式 39 is:

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} = 0.5 \times 30\ nC \times 24\ V \times 300\ kHz = 0.108\ W \quad (59)$$

The total power dissipated in the synchronous rectifier MOSFET from 式 40 is:

$$P_{SR} = P_{RR} + P_{COND} + P_{DC} = 0.108 + 0.83 + 0.384 = 1.322\ W \quad (60)$$

The junction temperature of the synchronous rectifier at 85°C is:

$$T_J = P_{SR} \times \theta_{JA} + T_A = (1.322) \times 40 + 85 = 139^oC \quad (61)$$

In typical applications, paralleling the synchronous rectifier MOSFET with a Schottky rectifier increases the overall converter efficiency by approximately 2% due to the lower power dissipation during the body diode conduction and reverse recovery periods.

8.2.2.6 Calculate the Inductor Value

The inductor value is calculated from 式 24.

$$L = \frac{(24 - 3.3\ V) \times 3.3\ V}{24\ V \times 3.2\ A \times 300\ kHz} = 2.96\ \mu H \quad (62)$$

A 2.9-µH Coev DXM1306-2R9 or 2.6-µH Panasonic ETQ-P6F2R9LFA can be used.

8.2.2.7 Set the Switching Frequency

The clock frequency is set with a resistor (R_T) from the RT pin to ground. The value of R_T can be found from 式 1, with f_{SW} in kHz.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 17\right) k\Omega = 170\ k\Omega \quad \therefore \text{ use } 169\ k\Omega \quad (63)$$

8.2.2.8 Program the Ramp Generator Circuit

The PWM ramp is programmed through a resistor (R_{KFF}) from the KFF pin to V_{IN}. The ramp generator also controls the input UVLO voltage. For an undervoltage level of 10 V, R_{KFF} can be calculated from 式 2:

$$R_{KFF} = \left(V_{IN(min)} - 3.48\right) \times \left(58.14 \times R_T + 1340\right) = 72.8 k\Omega \quad \therefore \text{use} 71.5 k\Omega \quad (64)$$

8.2.2.9 Calculate the Output Capacitance (C_O)

In this example the output capacitance is determined by the load response requirement of ΔV = 0.3 V for a 1-A to 8-A step load. C_O can be calculated using 式 30:

$$C_O = \frac{2.9\,\mu \times \left((8\ A)^2 - (1\ A)^2\right)}{\left((3.3)^2 - (3.0)^2\right)} = 97\ \mu F \tag{65}$$

Using 式 25 calculate the ESR required to meet the output ripple requirements.

$$33\,mV = 3.2\,A\left(ESR + \left(\frac{1}{8 \times 97\,\mu F \times 300\,kHz}\right)\right) \tag{66}$$

$$ESR = 10.3\,m\Omega - 4.3\,m\Omega = 6.0\,m\Omega \tag{67}$$

For this design example two Panasonic SP EEFUEOJ1B1R capacitors, (6.3 V, 180 µF, 12 mΩ) are used.

8.2.2.10 Calculate the Soft-Start Capacitor ($C_{SS/SD}$)

This design requires a soft-start time (t_{START}) of 1 ms. $C_{SS/SD}$ can be calculated using 式 6:

$$C_{SS/SD} = \frac{2.35\,\mu A}{0.7\,V} \times 1ms = 3.36\,nF \cong 3300\,pF \tag{68}$$

8.2.2.11 Calculate the Current Limit Resistor (R_{ILIM})

The current limit set point depends on t_{START}, V_O,C_O and I_{LOAD} at start-up as shown in 式 7. For this design,

$$I_{ILIM} > \frac{360\,\mu F \times 3.3\,V}{1\,ms} + 8.0\,A = 9.2\,A \tag{69}$$

For this design, add I_{ILIM} (9.2 A) to one-half the ripple current (1.6 A) and increase this value by 30% to allow for tolerances. This yields a overcurrent setpoint (I_{OC}) of 14 A. $R_{DS(on)}$ is increased 30% (1.3 × 0.008) to allow for MOSFET heating. Using 式 8 to calculate R_{ILIM}.

$$R_{ILIM} = \frac{14 \times 0.0104 - 0.020}{1.12 \times 8.5 \times 10^{-6}} + \frac{42.86 \times 10^{-3}}{8.5 \times 10^{-6}} = 18.24\,k\Omega \cong 18.7\,k\Omega \tag{70}$$

8.2.2.12 Calculate Loop Compensation Values

Calculate the DC modulator gain (A_{MOD}) from 式 12:

$$A_{MOD} = \frac{10}{2} = 5.0 \qquad A_{MOD(dB)} = 20 \times \log(5) = 14\ dB \tag{71}$$

Calculate the output filter L-C_O poles and C_O ESR zeros from 式 13 and 式 14:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C_O}} = \frac{1}{2\pi\sqrt{2.9\ \mu H \times 360\ \mu F}} = 4.93\ kHz \tag{72}$$

and

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} = \frac{1}{2\pi \times 0.006 \times 360\ \mu F} = 73.7\ kHz \tag{73}$$

Select the close-loop 0 dB crossover frequency, f_C. For this example f_C = 20 kHz.

Select the double zero location for the Type III compensation network at the output filter double pole at 4.93 kHz.

Select the double pole location for the Type III compensation network at the output capacitor ESR zero at 73.7 kHz.

The amplifier gain at the crossover frequency of 20 kHz is determined by the reciprocal of the modulator gain AMOD at the crossover frequency from 式 22:

$$A_{MOD(f)} = A_{MOD} \times \left(\frac{f_{LC}}{f_C}\right)^2 = 5 \times \left(\frac{4.93\ kHz}{20\ kHz}\right)^2 = 0.304 \tag{74}$$

And also from 式 22:

$$G = \frac{1}{A_{MOD(f)}} = \frac{1}{0.304} = 3.29 \tag{75}$$

Choose R1 = 100 kΩ

The poles and zeros for a type III network are described in 式 17 through 式 21.

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \therefore C3 = \frac{1}{2\pi \times 100\ k\Omega \times 4.93\ kHz} = 323\ pF,\ \text{choose } 330\ pF \tag{76}$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \therefore R3 = \frac{1}{2\pi \times 330\ pF \times 73.3\ kHz} = 6.55\ k\Omega,\ \text{choose } 6.49\ k\Omega \tag{77}$$

$$f_C = \frac{1}{2\pi \times R1 \times C2 \times G} \therefore C2 = \frac{1}{2\pi \times 100\ k\Omega \times 3.29 \times 20\ kHz} = 24.2\ pF,\ \text{choose } 22\ pF \tag{78}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \therefore R2 = \frac{1}{2\pi \times 22\ pF \times 73.3\ kHz} = 98.2\ k\Omega,\ \text{choose } 97.6\ k\Omega \tag{79}$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \therefore C1 = \frac{1}{2\pi \times 97.6\ k\Omega \times 4.93\ kHz} = 331\ pF,\ \text{choose } 330\ pF \tag{80}$$

Calculate the value of R_{BIAS} from 式 15 with R1 = 100 kΩ.

$$R_{BIAS} = \frac{0.7\ V \times R1}{V_O - 0.7\ V} = \frac{0.7\ V \times 100k\Omega}{3.3\ V - 0.7\ V} = 26.9\ k\Omega,\ \text{choose } 26.7\ k\Omega \tag{81}$$

8.2.2.13 Calculate the Boost and BP10V Bypass Capacitance

The size of the bypass capacitor depends on the total gate charge of the MOSFET being used and the amount of droop allowed on the bypass capacitor. The BOOST capacitance for the Si7860DP, allowing for a 0.5 voltage droop on the BOOST pin from 式 31 is:

$$C_{BOOST} = \frac{Q_g}{\Delta V} = \frac{18\ nC}{0.5\ V} = 36\ nF \tag{82}$$

and the BP10V capacitance from 式 32 is

$$C_{BP(10\ V)} = \frac{Q_{gHS} + Q_{gSR}}{\Delta V} = \frac{2 \times Q_g}{\Delta V} = \frac{36\ nC}{0.5\ V} = 72\ nF \tag{83}$$

For this application, a 0.1-µF capacitor is used for the BOOST bypass capacitor and a 1-µF capacitor is used for the BP10V bypass.

8.2.3 Application Curves

The TPS40055EVM-001 application curves are shown in 図 8-3 to 図 8-7 for reference.

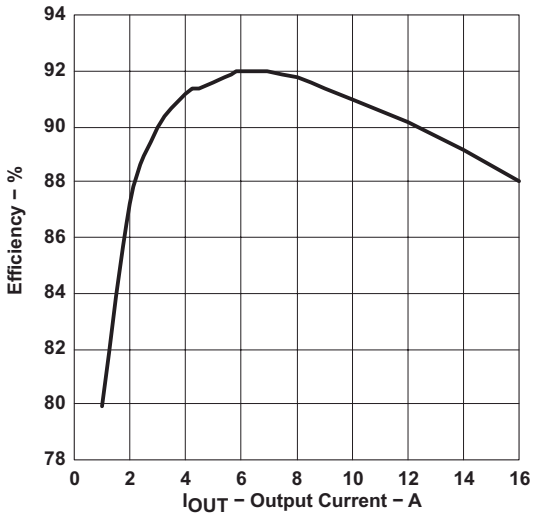


図 8-3. Efficiency vs Load

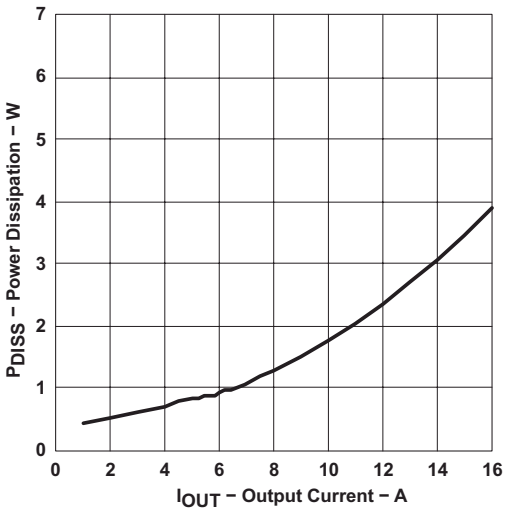


図 8-4. Power Dissipation vs Load

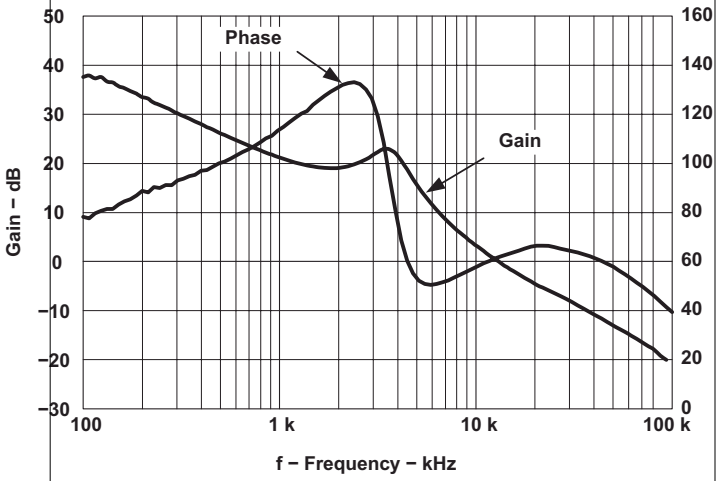


図 8-5. Overall Gain and Phase vs Frequency

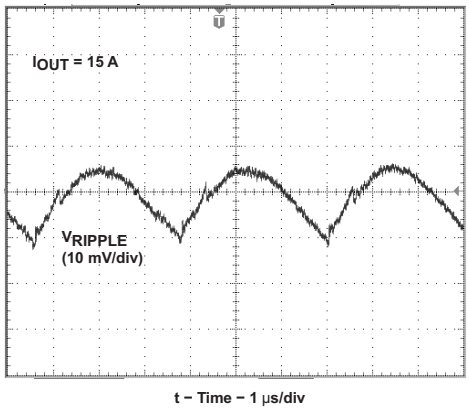


図 8-6. Output Voltage Ripple

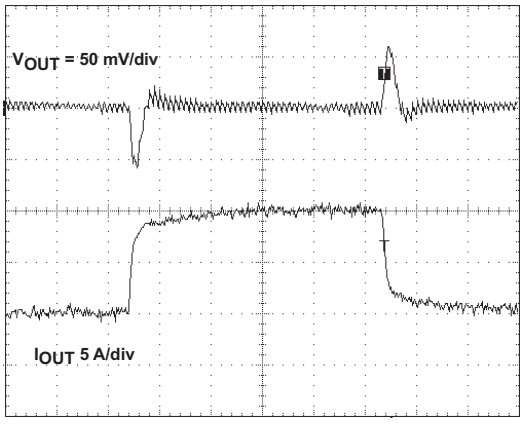


図 8-7. Transient Response

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply between 8 V and 40 V. This supply must be well regulated. Proper bypassing of input supplies and internal regulators is critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in セクション 10.

10 Layout

10.1 Layout Guidelines

The TPS4005x provides separate signal ground (SGND) and power ground (PGND) pins. It is important that circuit grounds are properly separated. Each ground must consist of a plane to minimize its impedance if possible. The high power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (BP10), and the input capacitor must be connected to PGND plane at the input capacitor.

Sensitive nodes such as the FB resistor divider, R_T, and ILIM must be connected to the SGND plane. The SGND plane must only make a single point connection to the PGND plane.

Component placement should ensure that bypass capacitors (BP10 and BP5) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT, and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW).

10.2 Layout Example

The TPS40055EVM-001 layout is shown in 図 10-1 to 図 10-5 for reference.

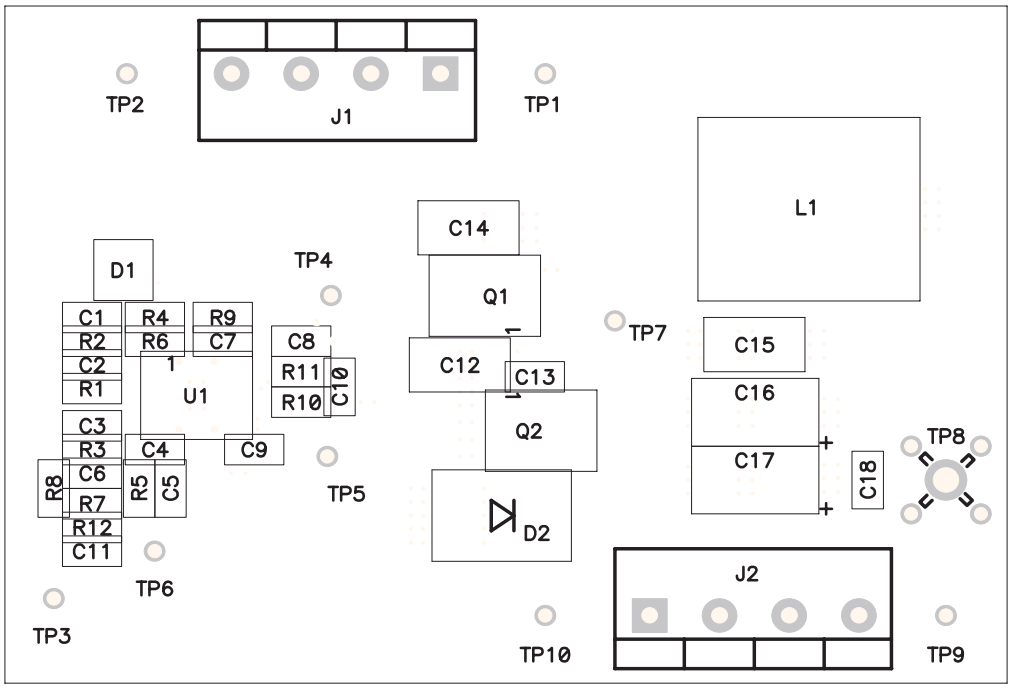


図 10-1. Top-Side Component Assembly

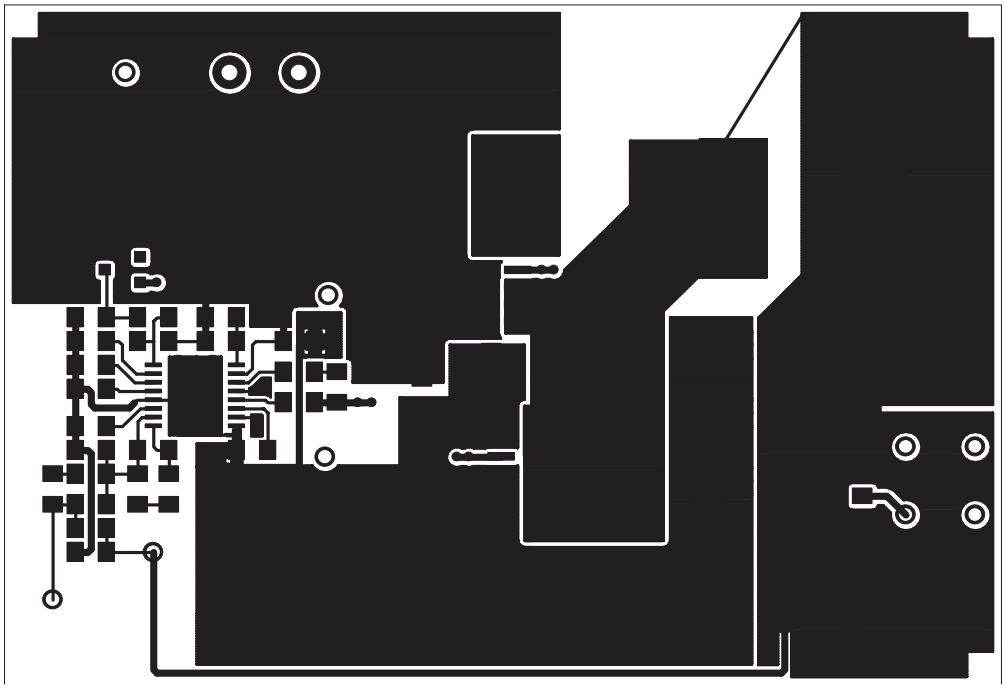


図 10-2. Top-Side Copper

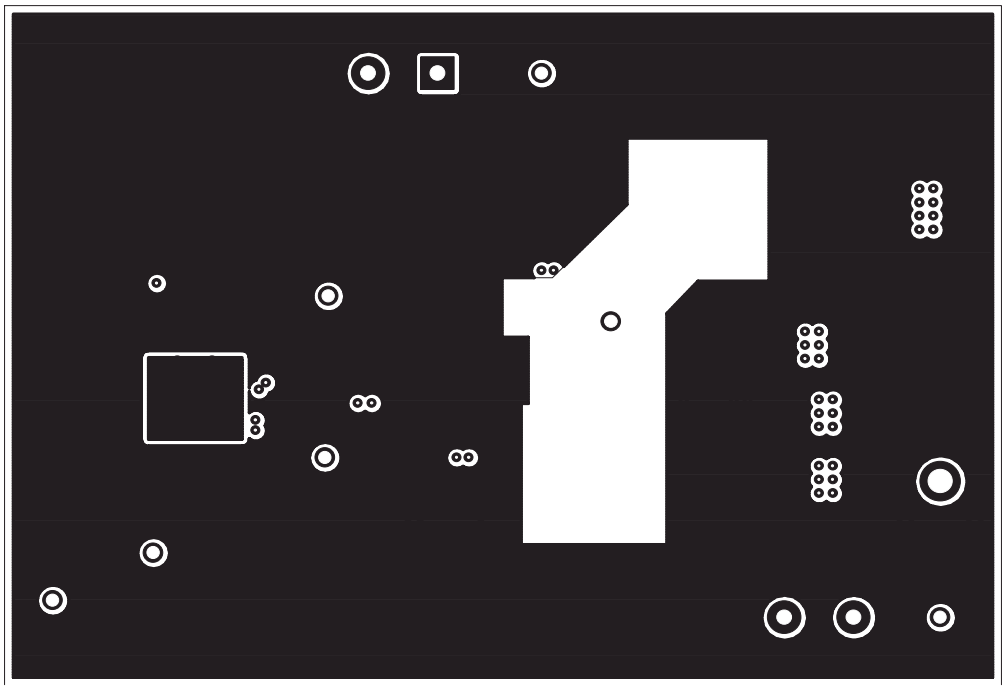


図 10-3. Internal Layer 1 Copper

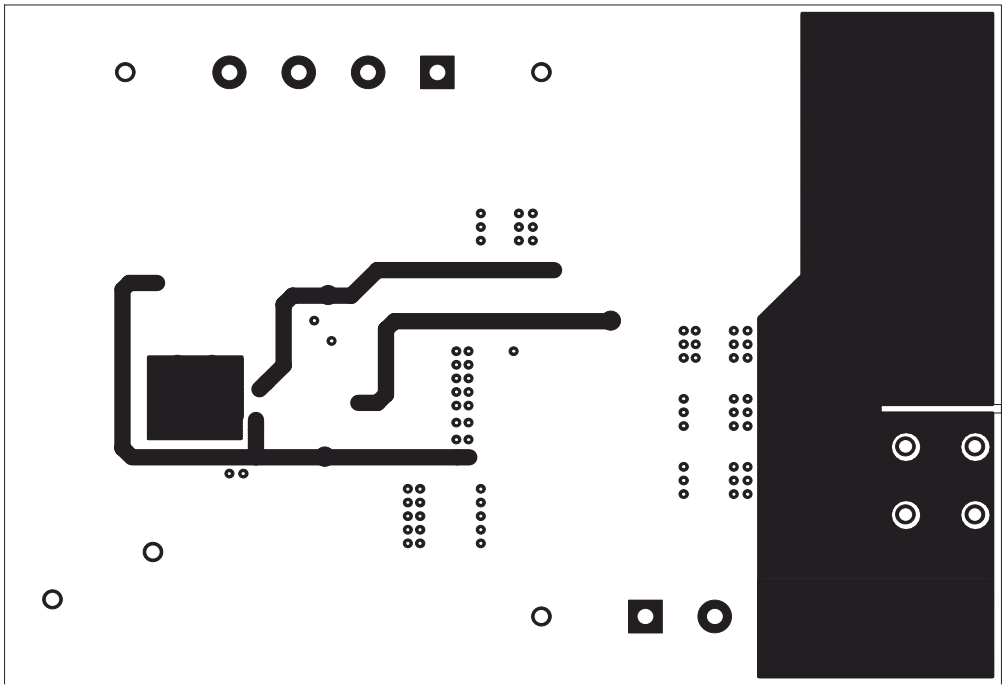


図 10-4. Internal Layer 2 Copper

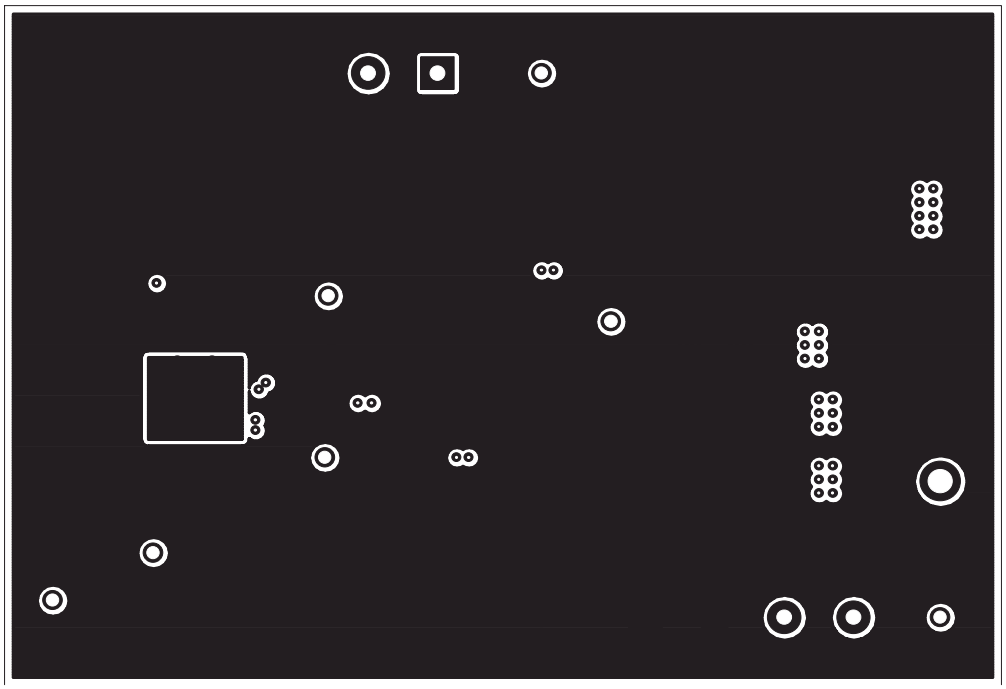


図 10-5. Bottom Layer Copper

10.3 MOSFET Packaging

MOSFET package selection depends on MOSFET power dissipation and the projected operating conditions. In general, for a surface-mount applications, the DPAK style package provides the lowest thermal impedance (θ_{JA}) and, therefore, the highest power dissipation capability. However, the effectiveness of the DPAK depends on proper layout and thermal management. The θ_{JA} specified in the MOSFET data sheet refers to a given copper area and thickness. In most cases, a lowest thermal impedance of 40°C/W requires one square inch of 2-ounce

copper on a G-10/FR-4 board. Lower thermal impedances can be achieved at the expense of board area. Please refer to the selected MOSFET's data sheet for more information regarding proper mounting.

11 Device and Documentation Support

11.1 Device Support

The following devices have characteristics similar to the TPS40054/5/7 and may be of interest.

表 11-1. Related Devices

DEVICE	DESCRIPTION
TPS40055-EP	Enhanced performance TPS40055.
TPS40192	4.5-V to 18-V controller with synchronization power good
TPS40193	
TPS40200	Wide-input non-synchronous DC-DC controller

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

- Balogh, Laszlo, *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, Texas Instruments/Unitrode Corporation, Power Supply Design Seminar, SEM-1400 Topic 2.
- Texas Instruments, *PowerPAD Thermally Enhanced Package* application note

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS40054PWP	NRND	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40054
TPS40054PWP.A	NRND	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40054
TPS40054PWPG4	NRND	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40054
TPS40054PWPR	NRND	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40054
TPS40054PWPR.A	NRND	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40054
TPS40055PWP	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055
TPS40055PWP.A	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055
TPS40055PWPG4	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055
TPS40055PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055
TPS40055PWPR.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055
TPS40055PWPRG4	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055
TPS40057PWP	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057
TPS40057PWP.A	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057
TPS40057PWP.B	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057
TPS40057PWPG4	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057
TPS40057PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057
TPS40057PWPR.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057
TPS40057PWPR.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057
TPS40057PWPRG4	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS40055 :

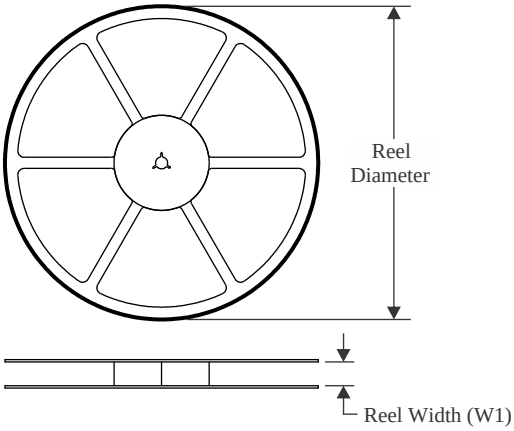
- Enhanced Product : TPS40055-EP

NOTE: Qualified Version Definitions:

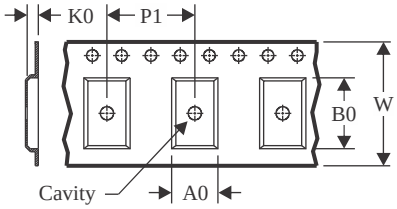
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

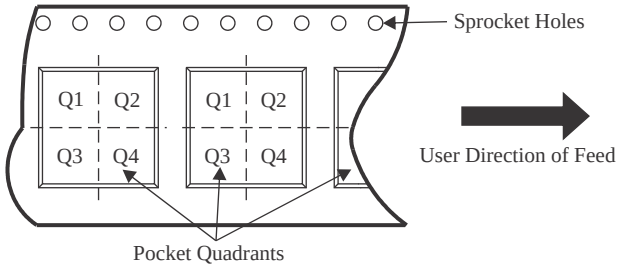


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

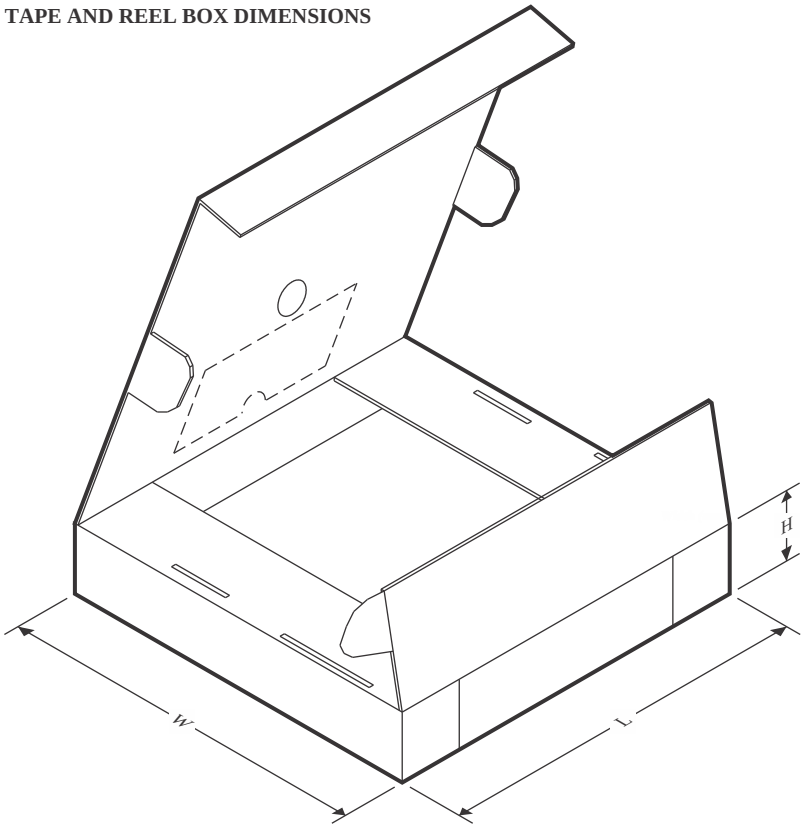
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40054PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS40055PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS40057PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

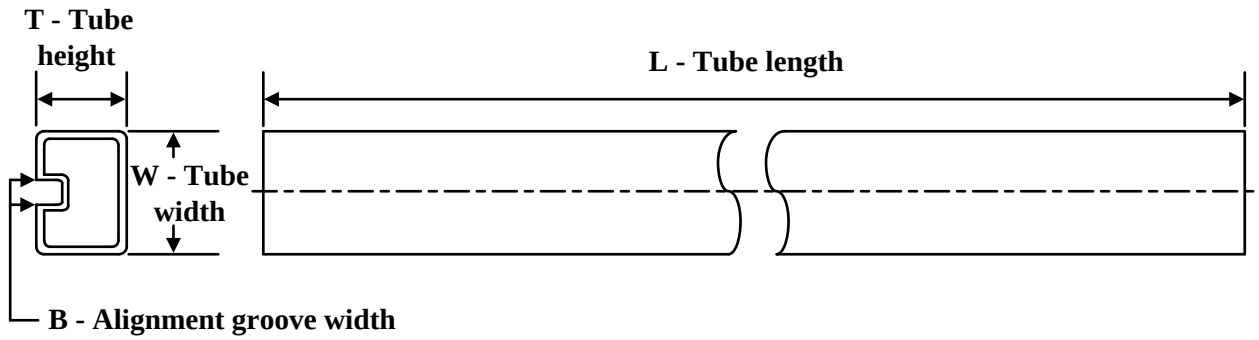
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40054PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS40055PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS40057PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0

TUBE

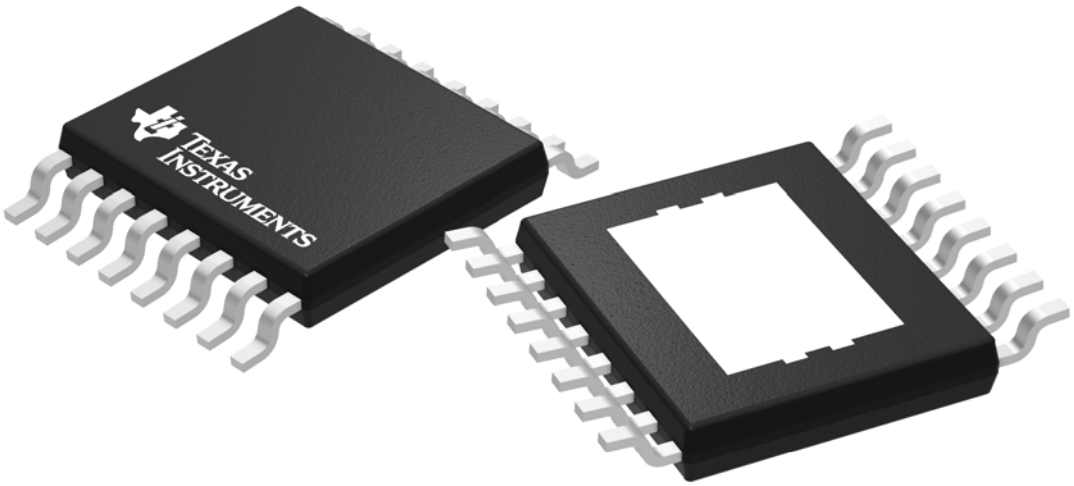


*All dimensions are nominal

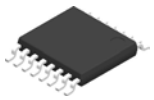
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS40054PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40054PWP.A	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40054PWPG4	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40055PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40055PWP.A	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40055PWPG4	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40057PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40057PWP.A	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40057PWP.B	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40057PWPG4	PWP	HTSSOP	16	90	530	10.2	3600	3.5

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

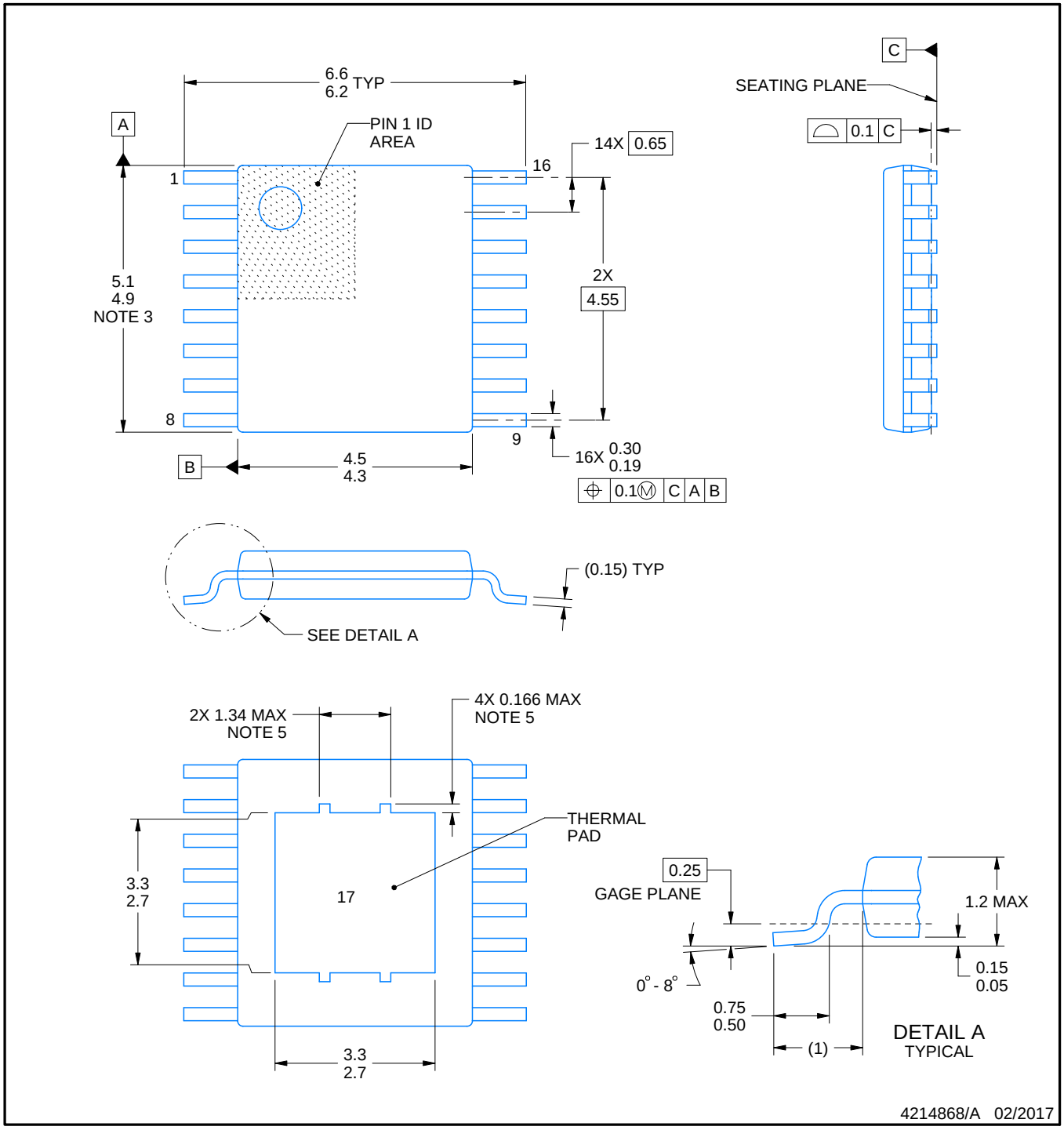


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

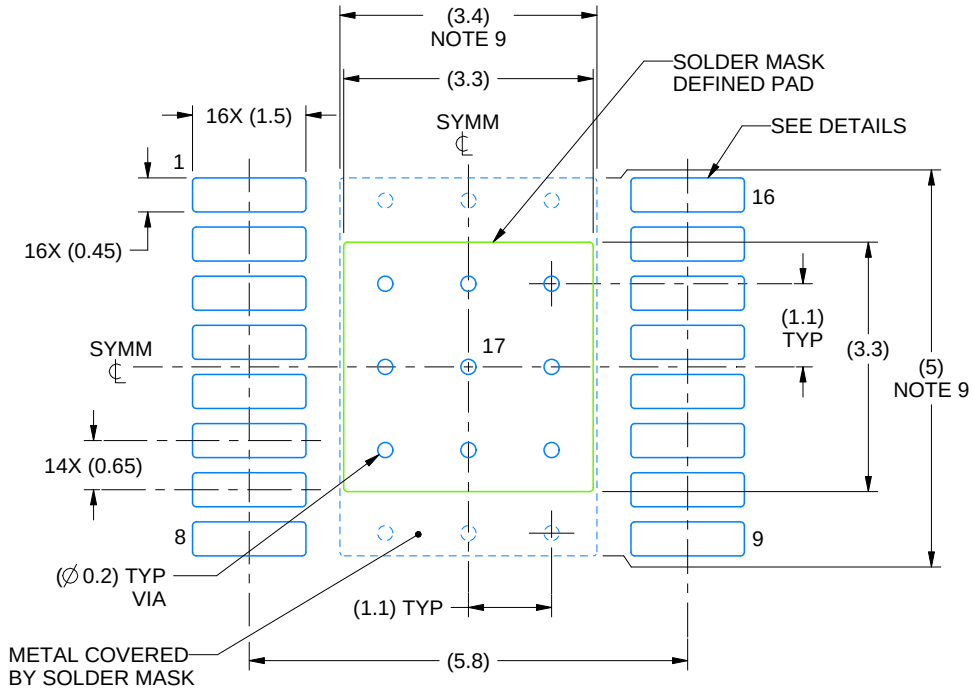
PLASTIC SMALL OUTLINE



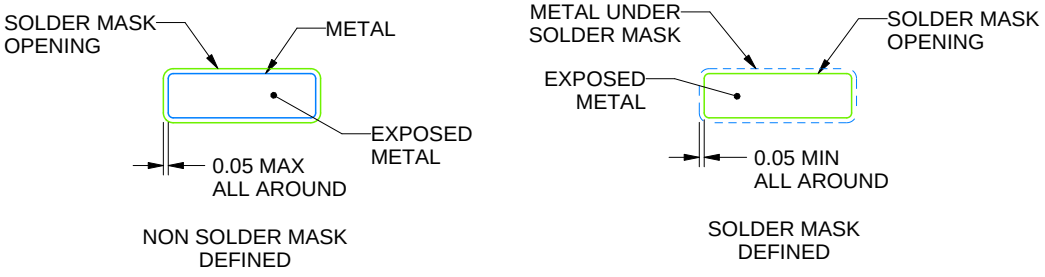
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

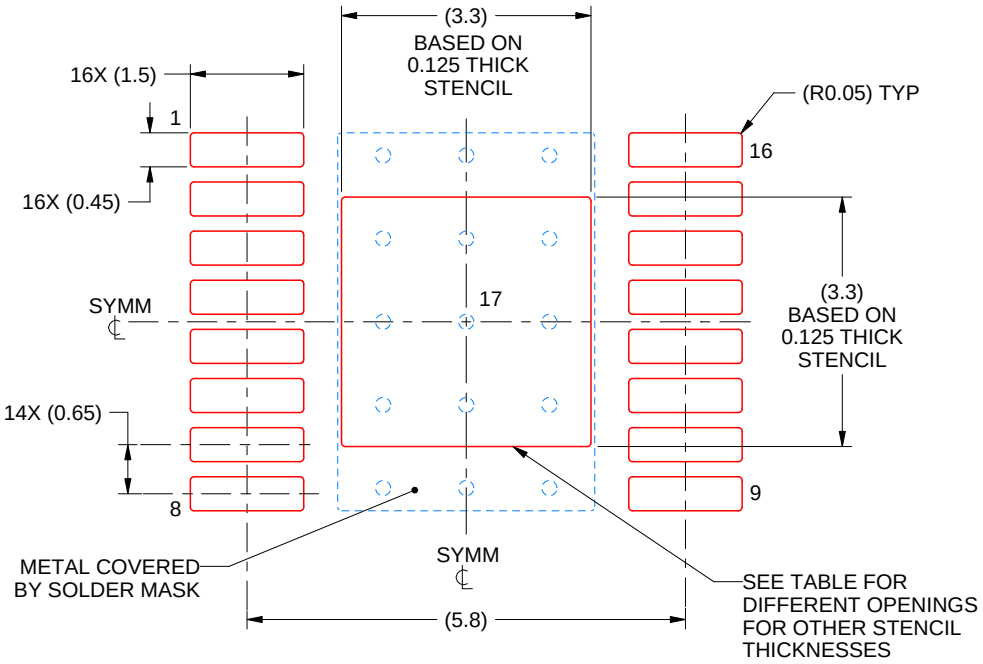


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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