

TPS389006 マルチチャネル過電圧および低電圧 I²C プログラマブル電圧スーパーバイザおよびモニタ

1 特長

- 機能安全準拠
 - 機能安全アプリケーション用の開発向け
 - IEC 61508 システムの設計に役立つ資料
 - SIL 3 までを対象とする決定論的対応能力
 - SIL 3 までを対象とするハードウェア機能
- 最新の SoC を監視
 - ±6mV のスレッショルド精度 (-40°C ~ +125°C)
 - 入力電圧範囲: 2.5V ~ 5.5V
 - 低電圧誤動作防止 (UVLO): 2.48V
 - "Low" スタンバイ静止電流: 200μA
 - 6 チャネル、2 個のリモート・センス付き
 - 固定ウィンドウのスレッショルド・レベル
 - 0.2V ~ 1.475V、5mV ステップ
 - 0.8V ~ 5.5V、20mV ステップ
- 小さなソリューション・サイズとわずかな部品コスト
 - 3mm × 3mm の QFN パッケージ
 - 可変グリッチ耐性 (I²C 利用)
 - 調整可能な電圧スレッショルド・レベル (I²C 利用)
- 安全アプリケーション向けに設計
 - アクティブ Low、オープン・ドレイン NIRQ 出力
 - リアルタイム電圧読み出し用の 8 ビット ADC を内蔵
 - 巡回冗長性検査 (CRC)
 - パケット・エラー・チェック (PEC)
 - シーケンス・ロギングとフォルト・ロギング機能
- レールのタグ付けの同期機能
 - シーケンシング機能を実現するために、[マルチチャネル・シーケンサ](#)と接続

2 アプリケーション

- 医療用ロボット
- 産業用ロボット
- サーバー・スイッチ
- モーター・ドライバ

3 説明

TPS389006 デバイスは、SIL-3 準拠の 6 チャネルのウィンドウ・スーパーバイザ IC で、2 つのリモート・センス・ピンを搭載し、16 ピンの 3mm × 3mm QFN パッケージで供給されます。この高精度のマルチチャネル電圧スーパーバイザは、低電圧電源レールで動作する、電源誤差の余地が小さいシステム向けに設計されています。

リモート・センス・ピンを使用すると、PCB トレース全体での電圧降下を考慮して、大電流コア・レールで高精度の電圧測定を実現できます。I²C 機能により、スレッショルド、リセット遅延、グリッチ・フィルタ、ピン機能を柔軟に選択できます。内部グリッチ耐性およびノイズ・フィルタにより、外部 RC 部品が不要になり、電源過渡による誤リセットを低減できます。また、このデバイスは、外付け抵抗なしで過電圧および低電圧リセットのスレッショルドを設定できるため、総合的な精度、コスト、ソリューション・サイズをさらに最適化でき、安全性システムの信頼性も向上します。

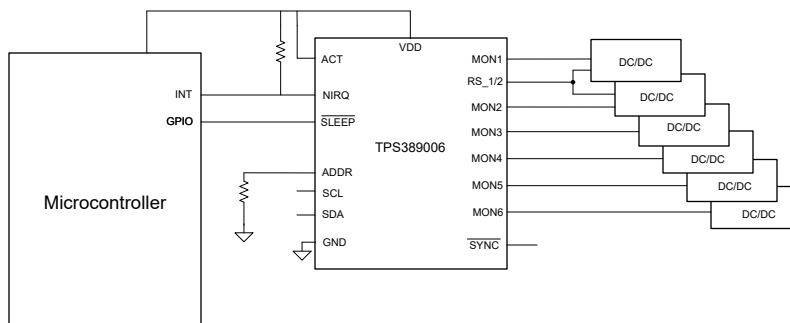
このデバイスには CRC エラー・チェック、電源オン / オフ時のシーケンス・ロギング、電圧読み出しを行うための内蔵 ADC が搭載されており、冗長なエラー・チェックが可能です。さらに、TPS389006 はレールに達したときにタグを付けられる SYNC 機能を提供します。また、TPS389006 デバイスは、テキサス・インスツルメンツの電源シーケンサ [TPS38700](#) と組み合わせて、SIL-3 レベル準拠のための電圧監視に加えて、適切なパワーオン・シーケンスを確保します。

製品情報

| 部品番号 | パッケージ (1) | 本体サイズ (公称) |
|-----------|-----------|------------|
| TPS389006 | WQFN (16) | 3mm × 3mm |

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。





TPS389006 回路例

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE | REVISION | NOTES |
|-----------|----------|-----------------|
| June 2023 | * | Initial Release |

5 Device Comparison

図 5-1 shows the device nomenclature of the TPS389006. Contact TI sales representatives or go online to TI's [E2E forum](#) for details and availability of other options; minimum order quantities apply.

See [セクション 12.1](#) for more information regarding the device ordering codes. [表 12-1](#) and [表 12-2](#) show how to decode the function of the device based on its part number.

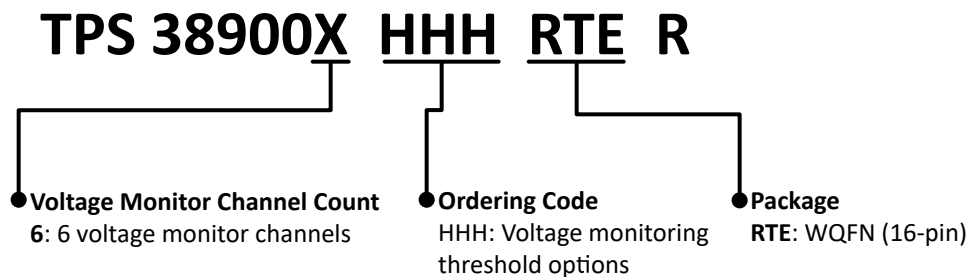
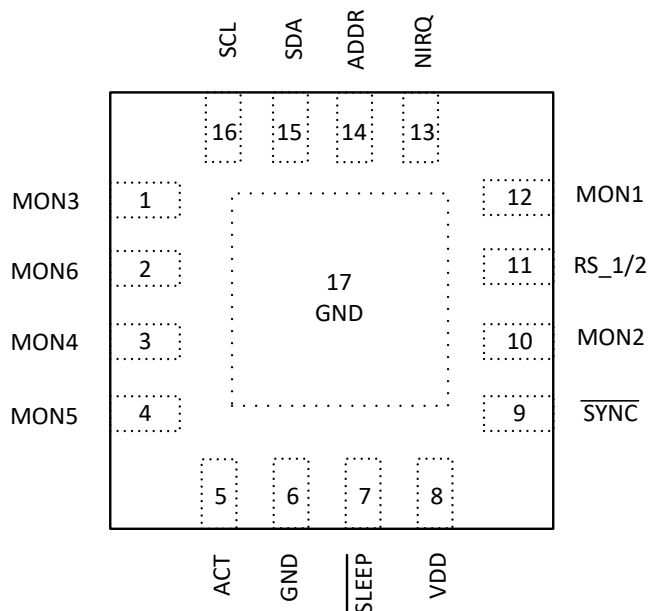


図 5-1. TPS389006 Device Nomenclature

6 Pin Configuration and Functions



**图 6-1. RTE Package
16-Pin WQFN
TPS389006 Top View**

表 6-1. Pin Functions

| NO. | PIN | | I/O | DESCRIPTION |
|-----|-----------|------|-----|--|
| | TPS389006 | NAME | | |
| 1 | MON3 | | I | Voltage monitor channel 3 |
| 2 | MON6 | | I | Voltage monitor channel 6 |
| 3 | MON4 | | I | Voltage monitor channel 4 |
| 4 | MON5 | | I | Voltage monitor channel 5 |
| 5 | ACT | | I | Active high device enable |
| 6 | GND | | - | Power ground |
| 7 | SLEEP | | I | Active low sleep enable |
| 8 | VDD | | - | Power supply rail |
| 9 | SYNC | | I/O | Sequence logging synchronization across multiple devices |
| 10 | MON2 | | I | Voltage monitor channel 2 |
| 11 | RS_1/2 | | I | Voltage monitor channel 1/2 remote sense |
| 12 | MON1 | | I | Voltage monitor channel 1 |
| 13 | NIRQ | | O | Active-low open-drain interrupt output |
| 14 | ADDR | | I | I ² C address select pin |
| 15 | SDA | | I/O | I ² C data pin |
| 16 | SCL | | I | I ² C clock pin |
| 17 | GND | | - | Exposed power ground pad |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|----------------------------|--|-----------------------------|---------|------|
| Voltage | VDD | −0.3 | 6 | V |
| Voltage | NIRQ | −0.3 | 6 | V |
| Voltage | ACT, SLEEP, SYNC, SCL, SDA | −0.3 | VDD+0.3 | V |
| Voltage | ADDR | −0.3 | 2 | V |
| Voltage | MONx | −0.3 | 6 | V |
| Current | NIRQ | | ±10 | mA |
| Temperature ⁽²⁾ | Continuous total power dissipation | See the Thermal Information | | |
| | Operating junction temperature, T _J | −40 | 150 | °C |
| | Operating free-air temperature, T _A | −40 | 125 | °C |
| | Storage temperature, T _{stg} | −65 | 150 | °C |

- (1) Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that T_J = T_A.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±500 | |
| | | | ±750 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|--------------------------------|--------------------------------------|-----|-----|-----|------|
| VDD | Supply pin voltage | 2.5 | | 5.5 | V |
| NIRQ | Pin voltage | 0 | | 5.5 | V |
| I _{NIRQ} | Pin Currents | 0 | | ±1 | mA |
| ADDR | Address pin voltage | 0 | | 1.8 | V |
| MONx | Monitor Pins | 0 | | 5.5 | V |
| ACT, SLEEP, SYNC, SCL, SDA | Pin Voltage | 0 | | VDD | V |
| R _{UP} ⁽¹⁾ | Pull-up resistor (Open Drain config) | 10 | | 100 | kΩ |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS389006 | UNIT |
|-------------------------------|--|------------|------|
| | | RTE (WQFN) | |
| | | PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 53.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 51.4 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 17.2 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.3 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 20.7 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 3.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

At 2.6 V ≤ VDD ≤ 5.5 V, NIRQ Voltage = 10 kΩ to VDD, NIRQ load = 10 pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD = 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|--|--------------------------|------|------|-------|------|
| COMMON PARAMETERS | | | | | | |
| VDD | Input supply voltage | | 2.6 | | 5.5 | V |
| VDD _{UVLO} | Rising Threshold | | 2.67 | | 2.81 | V |
| | Falling Threshold | | 2.48 | | 2.60 | V |
| V _{POR} | Power on Reset Voltage ⁽²⁾ | | | | 1.65 | V |
| I _{DD_Active} | Supply current into VDD pin (MON = LF/HF active) ACT = High, Sleep = High | VDD ≤ 5.5V | | 1.55 | 2 | mA |
| I _{DD_Sleep} | Supply current into VDD pin (MON = LF/HF active) ACT = High, Sleep = Low, I2C = Sleep power bit set to 1 | VDD ≤ 5.5V | | 1.55 | 2 | mA |
| I _{DD_Idle} | Supply current into VDD pin (MON = OVLF active) ACT = Low, Idle state-I2C active and OVLF mon | VDD ≤ 5.5V >10ms BIST | | 200 | 280 | μA |
| I _{DD_Deep Sleep} | Supply current into VDD pin (MON = HF active), ACT = High, Sleep = Low, I2C = Sleep power bit set to 0 | VDD ≤ 5.5V | | 275 | 380 | μA |
| V _{MONX} | MON voltage range | | 0.2 | | 5.5 | V |
| I _{MONX} | Input current MONx pins | V _{MON} = 5V | | | 20 | μA |
| I _{MONX_ADJ} | Input current for ADJ version (1x) | V _{MON} = 5V | | | 0.1 | μA |
| VMON_LF | 1x mode (No scaling) | | 0.2 | | 1.475 | V |
| | with 4x scaling | | 0.8 | | 5.5 | V |
| VMON_HF | 1x mode (No scaling) | | 0.2 | | 1.475 | V |
| | with 4x scaling | | 0.8 | | 5.5 | V |
| Threshold granularity_HF | 1x mode (No scaling) LSB | | | 5 | | mV |
| | 4x mode (With scaling) LSB | | | 20 | | mV |
| LPF cutoff LF | Range of Programmable values (I ² C selectable) | Low Freq channel | 250 | | 4000 | Hz |
| LPF cutoff HF | | High Freq channel | | 4 | | Mhz |

7.5 Electrical Characteristics (continued)

At 2.6 V ≤ VDD ≤ 5.5 V, NIRQ Voltage = 10 kΩ to VDD, NIRQ load = 10 pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at TJ = 25°C, typical conditions at VDD = 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---|---|------|------|------|------|
| Accuracy_HF | VMON | 0.2V ≤ VMONX ≤ 1.0V | –6 | | 6 | mV |
| | | 1.0V < VMONX ≤ 1.475V | –7.5 | | 7.5 | mV |
| | | 1.475V < VMONX ≤ 2.95V | –0.6 | | 0.6 | % |
| | | VMONX > 2.95V | –0.7 | | 0.7 | % |
| VHYS_HF | Hysteresis on UV,OV pin(Hysteresis is with respect of the tripoint ((UV),(OV)) (1)) | 0.2V ≤ VMONX ≤ 1.475V | | 5 | 11 | mV |
| | | 1.475V < VMONX ≤ 2.95V | | 9 | 16 | mV |
| | | VMONX > 2.95V | | 17 | 28 | mV |
| MON_OFF | OFF Voltage threshold | Monitored falling edge of VMON | 140 | | 215 | mV |
| ILKG | Output leakage current -NIRQ | VDD = VNIRQ = 5.5V | | | 300 | nA |
| ACT_L | Logic Low input | DEV_CONFIG.SOC_IF1=1 | | | 0.36 | V |
| ACT_H | Logic high input | DEV_CONFIG.SOC_IF1=1 | 0.84 | | | V |
| SLEEP_L | Logic Low input | DEV_CONFIG.SOC_IF1=1 | | | 0.36 | V |
| SLEEP_H | Logic high input | DEV_CONFIG.SOC_IF1=1 | 0.84 | | | V |
| SYNC_L | Input High | DEV_CONFIG.SOC_IF1=1 | | | 0.36 | V |
| SYNC_H | Input Low | DEV_CONFIG.SOC_IF1=1 | 0.84 | | | V |
| SYNC_PU | Internal Pull-up | | 25 | | 100 | kΩ |
| SYNC_OL | with 10kΩ external pull up | | | | 0.1 | V |
| ACT | Internal Pull down | | | 100 | | kΩ |
| SLEEP | Internal Pull down | | | 100 | | kΩ |
| UV,OV | Steps/Resolution | 0.2V < VMONX ≤ 1.475V | | 5 | | mV |
| | | 0.8V < VMONX < 5.5V | | 20 | | |
| VOL | Low level output voltage-NIRQ | NIRQ ,5.5V/5mA | | | 100 | mV |
| ILkg(OD) | Open-Drain output leakage current-NIRQ | NIRQ pin in High Impedance, VNIRQ = 5.5, Not asserted state | | | 90 | nA |
| IADDR | ADDR pin current | | | 20 | | μA |
| I ² C ADDR | (Hex format) | R=5.36k | | 0x30 | | |
| | | R=16.2k | | 0x31 | | |
| | | R=26.7k | | 0x32 | | |
| | | R=37.4k | | 0x33 | | |
| | | R=47.5k | | 0x34 | | |
| | | R=59.0k | | 0x35 | | |
| | | R=69.8k | | 0x36 | | |
| | | R=80.6k | | 0x37 | | |
| TSD | Thermal Shutdown | | | 155 | | °C |
| TSD Hys | Thermal Shutdown Hysteresis | | | 20 | | °C |
| RS | Remote sense range | | –100 | | 100 | mV |
| ADC SPECIFICATION | | | | | | |
| Vin | Input Range | | 0.2 | | 5.5 | V |
| Res_LF | Resolution | 1x mode (No scaling) | | 5 | | mV |
| | | 4x mode | | 20 | | mV |
| fs | Sample Rate | | | 125 | | ksps |
| VHYS_LF | Hysteresis LF faults | 1x mode (No scaling) | | 10 | 15 | mV |
| VHYS_LF | Hysteresis LF faults | 4x mode | | 40 | 55 | mV |

7.5 Electrical Characteristics (continued)

At 2.6 V ≤ VDD ≤ 5.5 V, NIRQ Voltage = 10 kΩ to VDD, NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at TJ = 25°C, typical conditions at VDD = 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---------------------------------|----------------------|-----|-----|-----|------|
| Accuracy_LF | VMON | 1x mode (No scaling) | -12 | | +12 | mV |
| | | 4x mode | -40 | | +40 | mV |
| I2C ELECTRICAL SPECIFICATIONS | | | | | | |
| C _B | Capacitive load for SDA and SCL | | | | 400 | pF |
| SDA,SCL | Low Threshold | DEV_CONFIG.SOC_IF1=0 | | | 0.8 | V |
| SDA,SCL | High Threshold | DEV_CONFIG.SOC_IF1=0 | 2.0 | | | V |

- (1) Hysteresis is with respect of the tripoint (VIT-(UV), VIT+(OV)).
- (2) VPOR is the minimum VDDX voltage level for a controlled output state.

7.6 Timing Requirements

At 2.6 V ≤ VDD ≤ 5.5 V, NIRQ Voltage = 10 kΩ to VDD, NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at TJ = 25°C, typical conditions at VDD = 3.3 V.

| | | | MIN | NOM | MAX | UNIT |
|--------------------------|--|---------------------|-----|-----|-------|------|
| COMMON PARAMETERS | | | | | | |
| tBIST | POR to ready with BIST, TEST_CFG.AT_POR=1 | includes OTP load | | | 12 | ms |
| tNBIST | POR to ready without BIST, TEST_CFG.AT_POR=0 | includes OTP load | | | 2 | ms |
| BIST | BIST time, TEST_CFG.AT_POR=1 or TEST_CFG.AT_SHDN=1 | | | | 10 | ms |
| ti2C_ACT | I2C active from BIST complete | | | | 0 | μs |
| tSEQ_Range | Sequence timestamp range, ACT or SLEEP edge to max counter | | | | 4 | s |
| tSEQ_LSB | Sequence timestamp resolution | | | 50 | | μs |
| tMON_ACT | Monitoring active from ACT rising edge | | | | 10 | μs |
| tSEQ_ACT | Sequence tagging active from ACT or SLEEP edge | | | | 12 | μs |
| tNIRQ | Fault detection to NIRQ assertion latency (except OV/UV faults) | | | | 25 | μs |
| tPD_NIRQ_1X | HF fault Propagation detect delay (default deglitch filter) includes digital delay | VIT_OV/UV +/- 100mV | | | 650 | ns |
| tPD_NIRQ_4X | HF fault Propagation detect delay (default deglitch filter) includes digital delay | VIT_OV/UV +/- 400mV | | | 750 | ns |
| tSEQ_ACC | Accuracy of sequence timestamp | | -5 | | 5 | % |
| tGI_R | UV & OV debounce range via I2C | FLT_HF(N) | 0.1 | | 102.4 | μs |

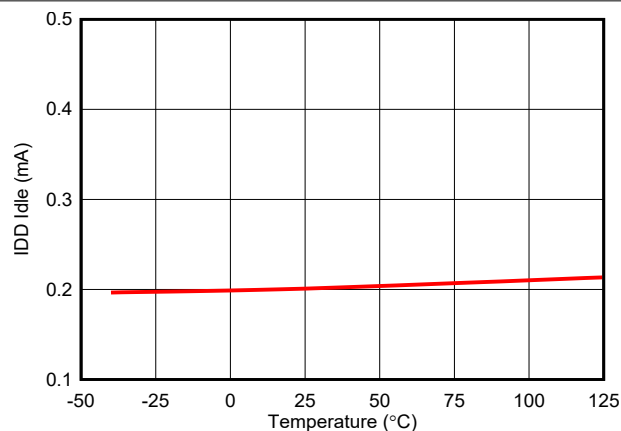
7.6 Timing Requirements (continued)

At 2.6 V ≤ VDD ≤ 5.5 V, NIRQ Voltage = 10 kΩ to VDD, NIRQ load = 10 pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD = 3.3 V.

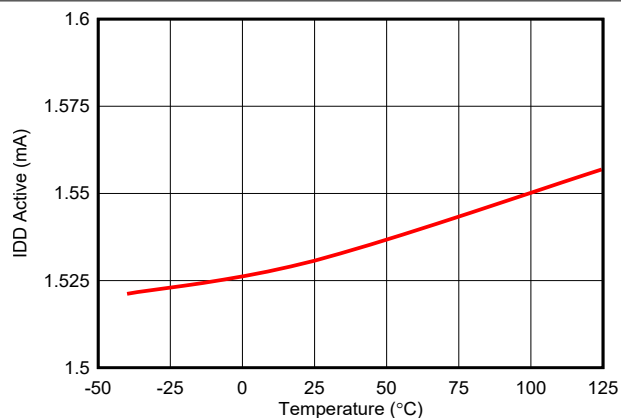
| | | | MIN | NOM | MAX | UNIT |
|-----------------------------------|---|--|------|-----|------|------|
| I2C TIMING CHARACTERISTICS | | | | | | |
| f _{SCL} | Serial clock frequency | Standard mode | | | 100 | kHz |
| f _{SCL} | Serial clock frequency | Fast mode | | | 400 | kHz |
| f _{SCL} | Serial clock frequency | Fast mode + | | | 1 | MHz |
| t _{LOW} | SCL low time | Standard mode | 4.7 | | | μs |
| t _{LOW} | SCL low time | Fast mode | 1.3 | | | μs |
| t _{LOW} | SCL low time | Fast mode + | 0.5 | | | μs |
| t _{HIGH} | SCL high time | Standard mode | 4 | | | μs |
| t _{HIGH} | SCL high time | Fast mode + | 0.26 | | | μs |
| t _{SU,DAT} | Data setup time | Standard mode | 250 | | | ns |
| t _{SU,DAT} | Data setup time | Fast mode | 100 | | | ns |
| t _{SU,DAT} | Data setup time | Fast mode + | 50 | | | ns |
| t _{HD,DAT} | Data hold time | Standard mode | 10 | | 3450 | ns |
| t _{HD,DAT} | Data hold time | Fast mode | 10 | | 900 | ns |
| t _{HD,DAT} | Data hold time | Fast mode + | 10 | | | ns |
| t _{SU,STA} | Setup time for a Start or Repeated Start condition | Standard mode | 4.7 | | | μs |
| t _{SU,STA} | Setup time for a Start or Repeated Start condition | Fast mode | 0.6 | | | μs |
| t _{SU,STA} | Setup time for a Start or Repeated Start condition | Fast mode + | 0.26 | | | μs |
| t _{HD,STA} | Hold time for a Start or Repeated Start condition | Standard mode | 4 | | | μs |
| t _{HD,STA} | Hold time for a Start or Repeated Start condition | Fast mode | 0.6 | | | μs |
| t _{HD,STA} | Hold time for a Start or Repeated Start condition | Fast mode + | 0.26 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | Standard mode | 4.7 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | Fast mode | 1.3 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | Fast mode + | 0.5 | | | μs |
| t _{SU,STO} | Setup time for a Stop condition | Standard mode | 4 | | | μs |
| t _{SU,STO} | Setup time for a Stop condition | Fast mode | 0.6 | | | μs |
| t _{SU,STO} | Setup time for a Stop condition | Fast mode + | 0.26 | | | μs |
| trDA | Rise time of SDA signal | Standard mode | | | 1000 | |
| trDA | Rise time of SDA signal | Fast mode | 20 | | 300 | ns |
| trDA | Rise time of SDA signal | Fast mode + | | | 120 | ns |
| tfDA | Fall time of SDA signal | Standard mode | | | 300 | ns |
| tfDA | Fall time of SDA signal | Fast mode | 1.4 | | 300 | ns |
| tfDA | Fall time of SDA signal | Fast mode + | 6.5 | | 120 | ns |
| trCL | Rise time of SCL signal | Standard mode | | | 1000 | ns |
| trCL | Rise time of SCL signal | Fast mode | 20 | | 300 | ns |
| trCL | Rise time of SCL signal | Fast mode + | | | 120 | ns |
| tfCL | Fall time of SCL signal | Standard mode | | | 300 | ns |
| tfCL | Fall time of SCL signal | Fast mode | 6.5 | | 300 | ns |
| tfCL | Fall time of SCL signal | Fast mode + | 6.5 | | 120 | ns |
| tSP | Pulse width of SCL and SDA spikes that are suppressed | Standard mode, Fast mode and Fast mode + | | | 50 | ns |

7.7 Typical Characteristics

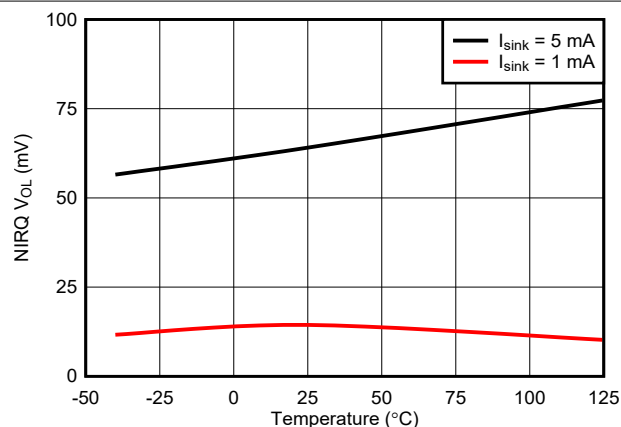
At $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, and $R_{PU} = 10\text{ k}\Omega$, unless otherwise noted.



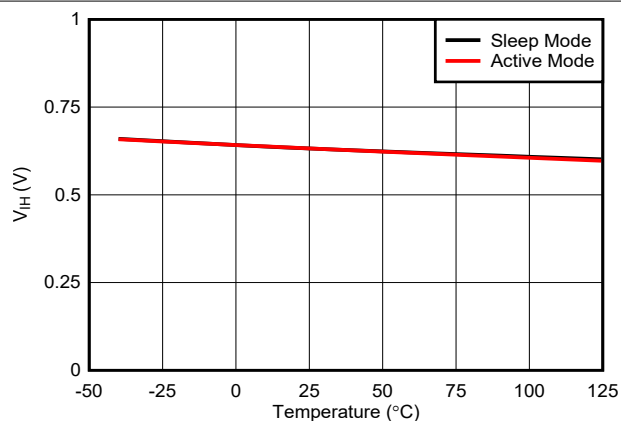
7-1. Idle Input Current Vs Temperature



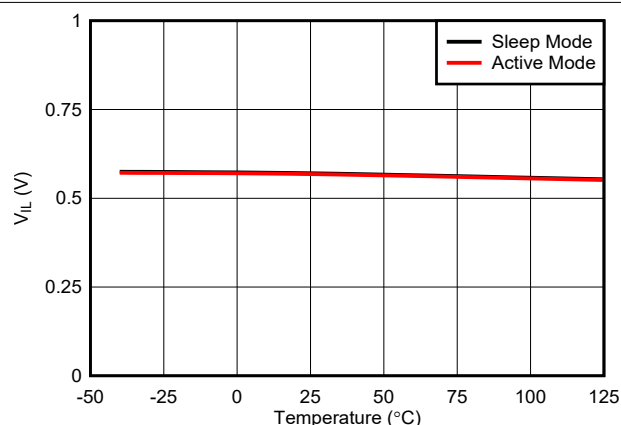
7-2. Active Input Current Vs Temperature



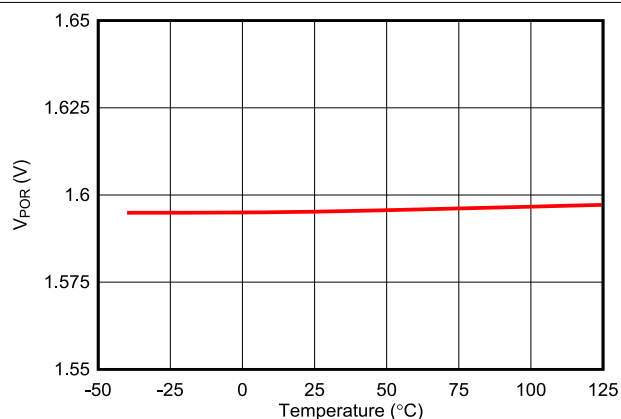
7-3. NIRQ Low Level Output Voltage Vs Temperature



7-4. High Level Input Voltage Vs Temperature



7-5. Low Level Input Voltage Vs Temperature



7-6. Power-on-Reset Voltage Vs Temperature

8 Detailed Description

8.1 Overview

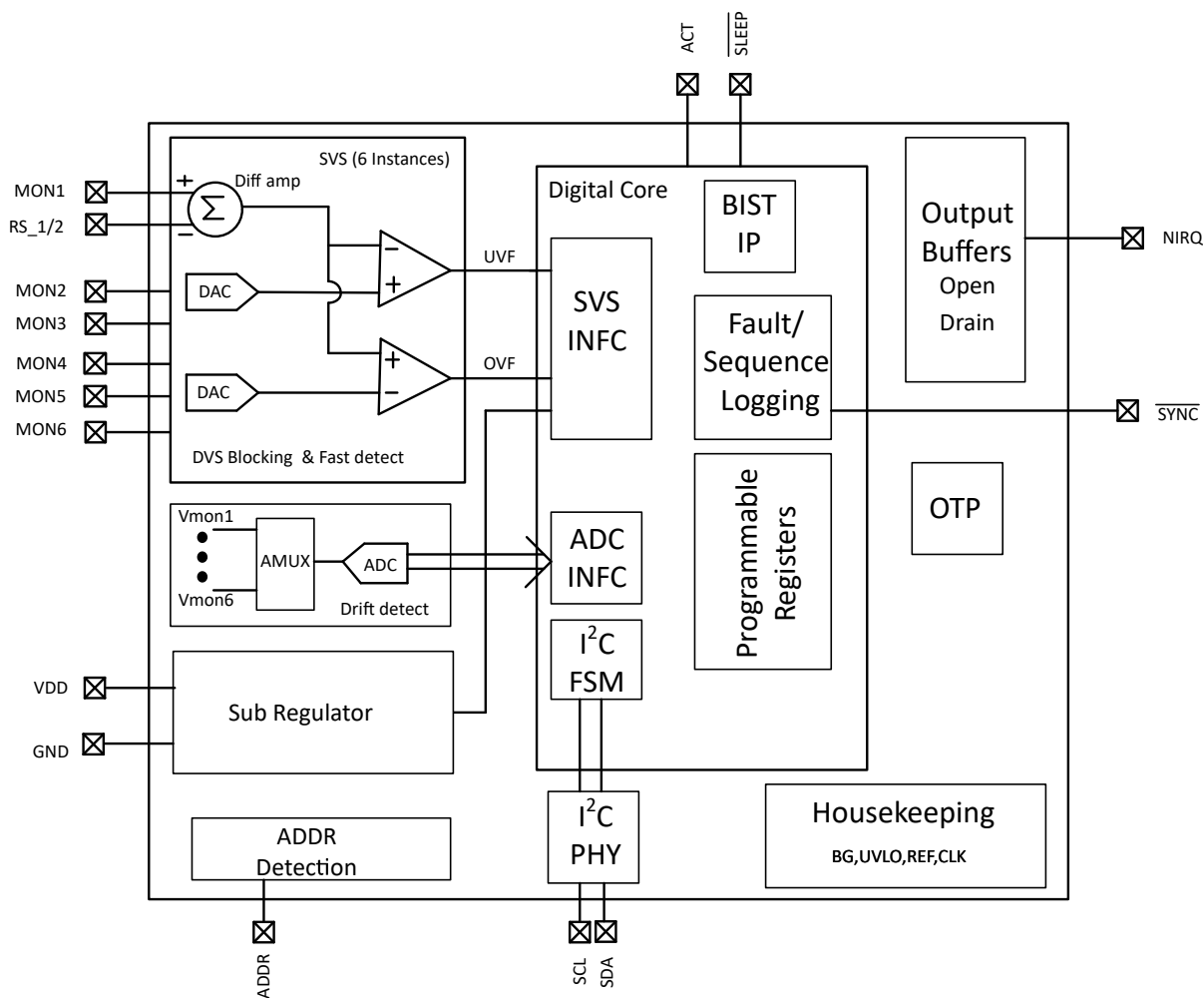
The TPS389006 family of devices has six channels that can be configured for over voltage, under voltage or both in a window configuration. The TPS389006 features highly accurate window threshold voltages (up to ± 6 mV) and a variety of voltage thresholds which can be factory configured or set on boot up by I²C commands.

The TPS389006 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

The TPS389006 also has a sequence logging feature to monitor and assign timestamps/log for the power rails turning on and off. It can perform sequence logging on a single device or across multiple devices on a board. It uses the $\overline{\text{SYNC}}$ pin to communicate across multiple devices. When either the ACT or $\overline{\text{SLEEP}}$ pin transitions from low to high or high to low, the sequence logging function becomes active until the expiry of the sequence timeout (SEQ_TOUT). During the sequence timeout, the UV faults can be masked (Automask - AMSK).

The TPS389006 is designed to assert active low output signals (NIRQ) when the monitored voltage is outside the safe window. The factory configuration can have the interrupts disabled for over voltage and under voltage faults, sequence timeout, BIST enabled at POR, sequence fault interrupts disabled, and over voltage and under voltage deglitch settings depending on the OTP.

8.2 Functional Block Diagram



8-1. TPS389006 Block Diagram

8.3 Feature Description

8.3.1 I²C

The TPS389006 device follows the I²C protocol (up to 1MHz) to manage communication with host devices such as a MCU or System on Chip (SoC). I²C is a two wire communication protocol implemented using two signals, clock (SCL) and data (SDA). The host device is the primary controller of communication. TPS389006 device responds over the data line during read or write operations as defined by I²C protocol. Both SCL and SDA signals are open drain topology and can be used in a wired-OR configuration with other devices to share the communication bus. Both SCL and SDA pins need an external pull up resistor to supply voltage (10 kΩ recommended).

Figure 8-2 shows the timing relationship between SCL and SDA lines to transfer 1 byte of data. SCL line is always controlled by host. To transfer 1 byte data, host needs to send 9 clocks on SCL. 8 clocks for data and 1 clock for ACK or NACK. SDA line is controlled by either the host or TPS389006 device based on the read or write operation. Figure 8-2 and Figure 8-3 highlight the communication protocol flow and which device controls SDA line at various instances during active communication.

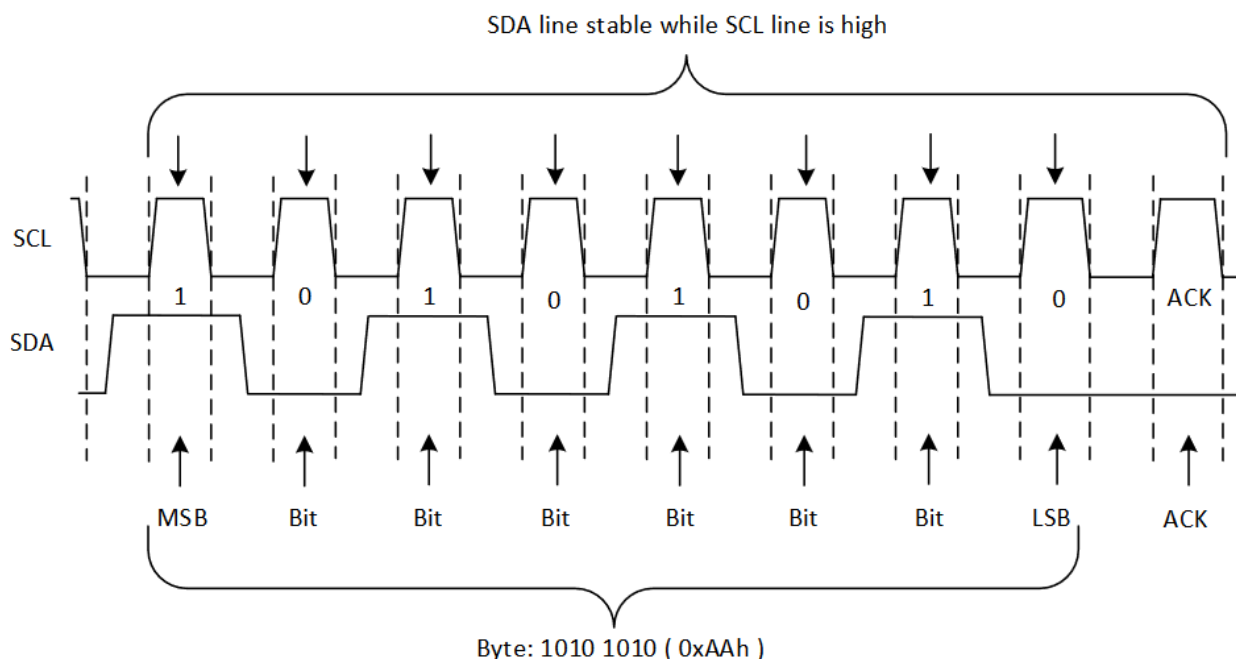
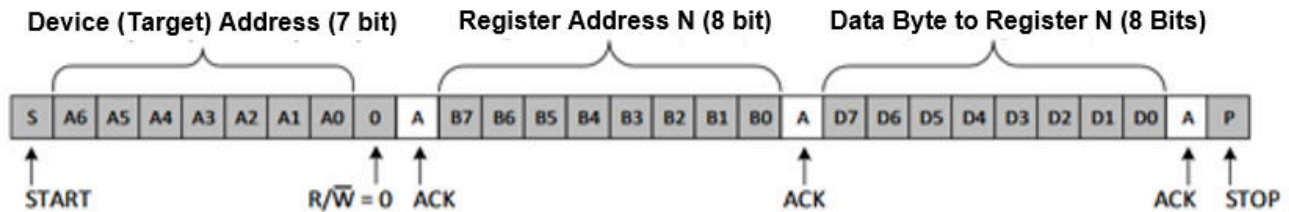


Figure 8-2. SCL to SDA Timing for 1 Byte Data Transfer

- ☒ Controller Controls SDA Line
- ☐ Target Controls SDA Line

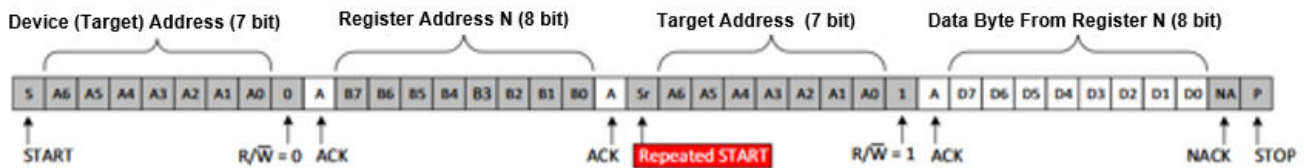
Write to One Register in a Device



8-3. I²C Write Protocol

- ☒ Controller Controls SDA Line
- ☐ Target Controls SDA Line

Read From One Register in a Device



8-4. I²C Read Protocol

Before initiating communication over I²C protocol, host needs to confirm the I²C bus is available for communication. Monitor the SCL and SDA lines, if any line is pulled low, the I²C bus is occupied. Host needs to wait until the bus is available for communication. Once the bus is available for communication, the host can initiate read or write operation by issuing a START condition. Once the I²C communication is complete, release the bus by issuing STOP command. 8-5 shows how to implement START and STOP condition.

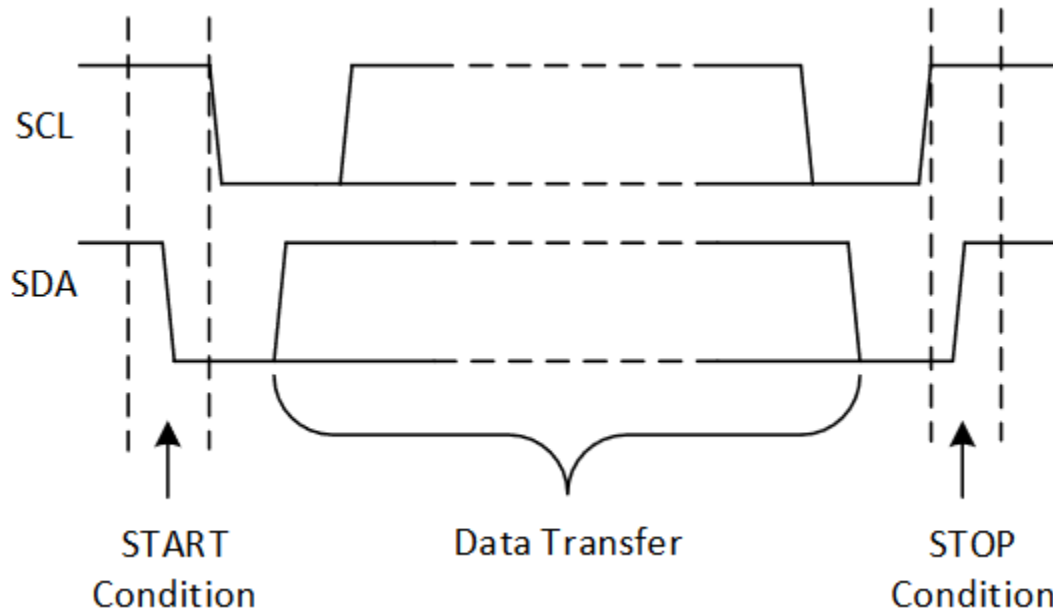


図 8-5. I²C START and STOP Condition

表 8-1 shows the different functionality available when programming with I²C.

表 8-1. User Programmable I²C Functions

| FUNCTIONS | DESCRIPTION |
|--|--|
| Thresholds for OV/UV- fast loop | Adjustable in 5 mV steps from 0.2 V to 1.475 V and 20 mV steps from 0.8 V to 5.5 V |
| Thresholds for drift -positive and negative | Adjustable in 5 mV steps from 0.2 V to 1.475 V and 20 mV steps from 0.8 V to 5.5 V |
| Voltage Monitoring scaling | 1 or 4 |
| Glitch (debounce) immunity for OV/UV-fast loop | 0.1 us to 102.4 us |
| Enable sequence timeout | 1 ms to 4 s |
| Sleep sequence timeout | 1 ms to 4 s |
| SYNC pulse width | 50 us to 2600 us |
| Expected ON/OFF Sequence on ACT | Used for sequence logging |
| Expected ON/OFF Sequence on Sleep | Used for sequence logging |
| Auto Mask OFF-ON-OFF via ACT | Selectable for each MON channel |
| Auto Mask OFF-ON-OFF via SLEEP | Selectable for each MON channel |
| Packet error checking for I ² C | Enabling or Disabling |
| Force NIRQ assertion | Controlled by I ² C register |
| Individual channel MON | Enable or Disable |
| Interrupt disable functions | BIST, PEC, TSD, CRC |

8.3.2 Auto Mask (AMSK)

In the case of power up AMSK_ON and AMSK_EXS registers apply. It masks interrupts till the MON voltage crosses the UVLF threshold or sequence timeout expires whichever is sooner. In the case of power down AMSK_OFF and AMSK_ENS registers apply. It masks interrupts till the MON voltage is below the OFF threshold and then the OVLF interrupts are active.

表 8-2 summarizes the auto-mask operation for the ACT and SLEEP transitions.

表 8-2. Transition Table

| TRANSITION | AUTO-MASK APPLIED | AUTO-MASK APPLIES TO | AUTO-MASK INACTIVE | INTERRUPTS ACTIVE FOR MON CHANNELS NOT IN AUTO-MASK |
|--------------------------------|-------------------|------------------------------|--|---|
| ACT (Low -> High) | AMSK_ON | IEN_UVLF, IEN_UVHF, IEN_OVHF | SEQ_TOUT expires or rail crosses UVLF | At ACT=High |
| ACT (High -> Low) | AMSK_OFF | IEN_UVLF, IEN_UVHF, IEN_OVHF | Auto-mask active in transition till SEQ_TOUT expires | Until SEQ_TOUT expires |
| SLEEP (Low -> High) ACT = High | AMSK_EXS | IEN_UVLF, IEN_UVHF, IEN_OVHF | SEQ_TOUT expires or rail crosses UVLF | Always active |
| SLEEP (High -> Low) ACT = High | AMSK_ENS | IEN_UVLF, IEN_UVHF, IEN_OVHF | Auto-mask active | Always active |

8.3.3 PEC

TPS389006 supports Packet Error Checking (PEC). It uses a CRC-8 represented by the polynomial $C(x)=x^8 + x^2 + x + 1$, with CRC initial value set to 0x00. The PEC calculation includes all bytes in the transmission, including address, command and data. The PEC calculation does not include ACK or NACK bits or START,STOP or REPEATED START conditions. The device which acts as a peripheral and supports PEC must be prepared to perform the transfer with or without a PEC, verify the correctness of the PEC if present and only process the message if PEC is correct.

- If PEC is enabled by EN_PEC, and the PEC byte is present in the write transaction, the device will NACK and assert NIRQ if PEC byte is incorrect.
- If PEC is enabled by EN_PEC, and the PEC byte is not present in the write transaction

-If REQ_PEC = 0, missing PEC is treated as good PEC and register write succeeds. NIRQ is not asserted.

-If REQ_PEC = 1, missing PEC is treated as incorrect PEC and register write fails. NIRQ is asserted.

8.3.4 VDD

The TPS389006 is designed to operate from an input voltage supply range between 2.5 V to 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 1-μF capacitor between the VDD pin and the GND pin.

V_{DD} needs to be at or above $V_{DD(MIN)}$ for at least the start-up delay ($t_{SD} + t_D$) for the device to be fully functional.

8.3.5 MON

The TPS389006 combines two comparators with a precision reference voltage and a trimmed resistor divider per monitor (MON) channel. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides noise immunity and ensures stable operation.

Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the MON input in order to reduce sensitivity to transient voltages on the monitored signal. Specific deglitch times can also be set independently for each MON via I²C registers

When monitoring VDD supply voltage, the MON pin can be connected directly to VDD. The output (NIRQ) is high impedance when voltage at the MON pin is between upper and lower boundary of threshold.

8.3.6 NIRQ

In a typical TPS389006 application, the NIRQ output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the enable input of a voltage regulator such as a DC-DC converter or low-dropout regulator (LDO).

The TPS389006 has an open drain active low output that requires a pull-up resistor to hold these lines high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. The pull-up resistor value is determined by

V_{OL} , output capacitive loading, and output leakage current. These values are specified in [セクション 7](#). The open drain output can be connected as a wired-OR logic with other open drain signals such as another TPS389006 NIRQ pin.

8.3.7 ADC

The ADC used in the TPS389006 runs on a 1Mhz clock with an effective sampling rate of 1/8 MHz (= 125 kHz). Initially, the ADC records with a resolution of 12 bits (1LSB = 0.41667mV) which is later round off to 8-bit data for I²C transaction. (1LSB = 5mV) The ADC uses ping-pong architecture in which it requires 2us for both sampling and conversion per channel with a total of 2 sampling channels. While CH0 performs coarse conversion, CH1 does fine conversion and vice versa.

Digitized 8-bit data is updated once the fine conversion is completed, which occurs once every 8 μ s. Each I²C transaction initiated for reading 8-bit MON_LVL data (the ADC data of a particular channel), 8-bit data is paused from updating until the I²C transaction completes.

Voltage scaling is done using a resistor ladder, but for differential mode channels, a chopping circuit is used to get the average of both of the voltages (VMON + VMON_RS)/2 since VMON_RS can be negative and can't be converted into an ADC code. VMON – VMON_RS is calculated digitally by subtracting ((VMON + VMON_RS) /2) from VMON and then multiplying by 2.

The MONX channels can be configured in 1x (0.2V to 1.475V) or 4x mode (0.8V to 5.5V). For differential mode channels configured in 1x mode, (MON1 and MON2) the ADC range is limited up to 1.7V. To configure an ADC channel above 1.7 V, please use 4x mode.

Real time voltage measurements use [式 1](#).

$$V_{VI} = ((ADC[7:0] * 5mV) + 0.2) * (VRANGE_MULT) \quad (1)$$

1. ADC[7:0] is translated to a corresponding decimal value. The value of ADC[7:0] corresponding to MON1-MON6 can be read from registers [0x40-0x45](#) of [セクション 8.5.1](#).
2. VRANGE_MULT corresponds to the selected monitor voltage multiplier set in register [0x1F](#) of [セクション 8.5.2](#).
3. VRANGE_MULT is set to a decimal 1 or 4 value depending on monitored value.

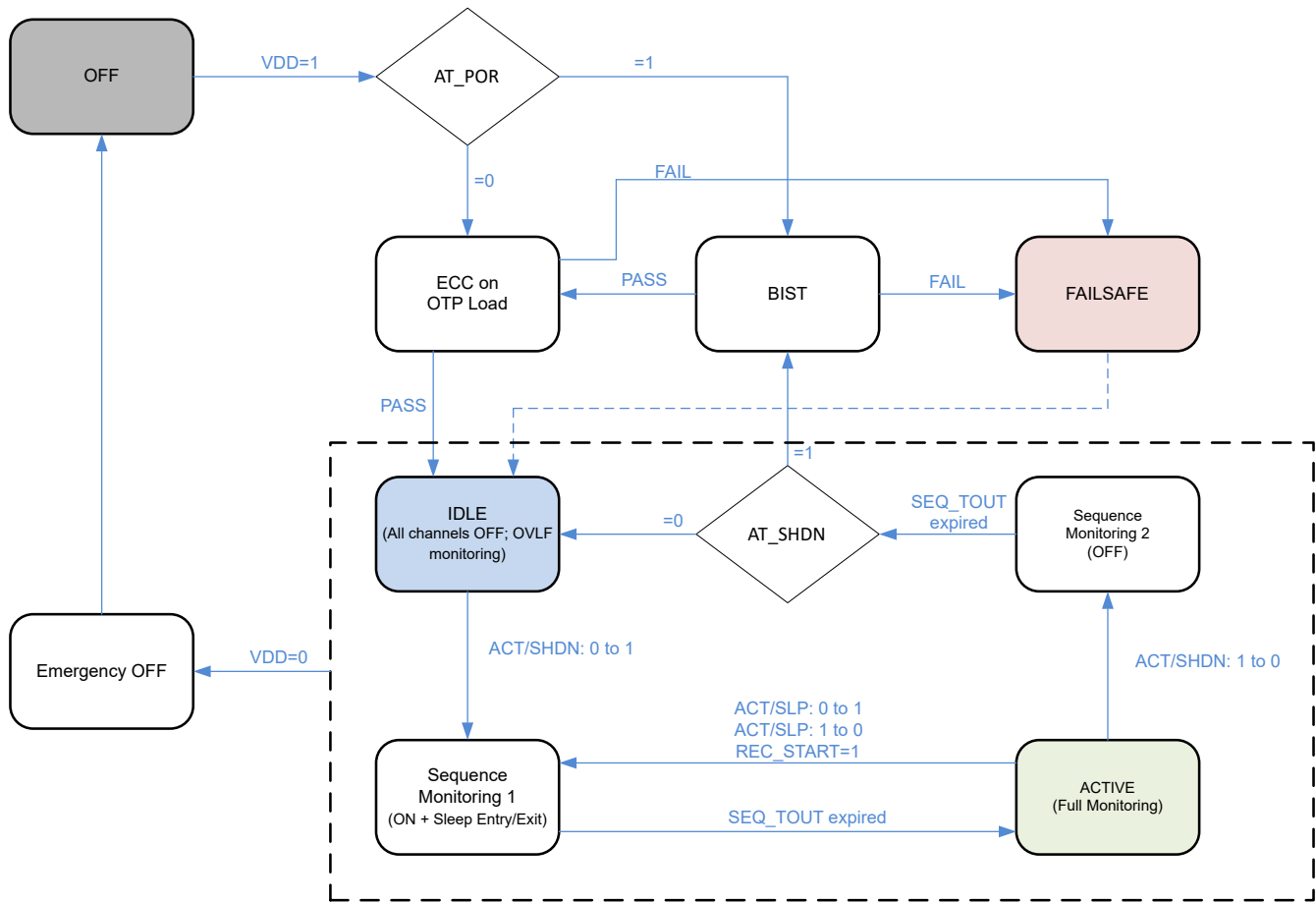
8.3.8 Time Stamp

Time stamp measurement use [式 2](#). The time stamps are used for sequence logging purposes to determine the order in which the rails are turned on or off.

$$t_{stamp} = 50\mu s * CLOCK[15:0] \quad (2)$$

1. CLOCK[15:0] translated to corresponding decimal value. The value of CLOCK[15:0] corresponding to MON1-MON6 can be read from registers [0x90-0x9B](#) of [BANK0](#).

8.4 Device Functional Modes



8-6. TPS389006 State Diagram

8.4.1 Built-In Self Test and Configuration Load

Built-In Self Test (BIST) is performed:

1. At Power On Reset (POR), if TEST_CFG.AT_POR=1
2. When exiting ACTIVE state due to ACT transitioning from 1→0, if TEST_CFG.AT_SHDN=1

Configuration load from OTP is assisted by ECC (supporting SEC-DED). This is to protect against data integrity issues and to maximize system availability.

During BIST, NIRQ is de-asserted (asserted in case of failure), input pins are ignored, $\overline{\text{SYNC}}$ is tri-stated, and the I²C block is inactive with SDA and SCL de-asserted. The BIST includes device testing to meet the Functional Safety goals outlined in functional safety documentation. Once BIST is completed without failure, I²C is immediately active and the device enters the IDLE state after loading the configuration data from OTP. If BIST fails and/or ECC reports Double-Error Detection (DED; meant for detecting multiple bit flips when loading data from memory), NIRQ is asserted, the device enters FAILSAFE state, and a best effort attempt is made to keep the I²C function active. TEST_INFO register may provide additional information on the test results.

The detailed behavior upon success/failure of the BIST is controlled by INT_TEST and IEN_TEST registers. Reporting of the BIST results is carried out through:

- NIRQ pin: pulled low depending on the test result and BIST_C and BIST bits in IEN_TEST
- I_BIST_C and BIST bits in INT_TEST register depending on IEN_TEST settings
- VMON_STAT.ST_BIST_C register bit
- TEST_INFO[3:0] register bits

8.4.1.1 Notes on BIST Execution

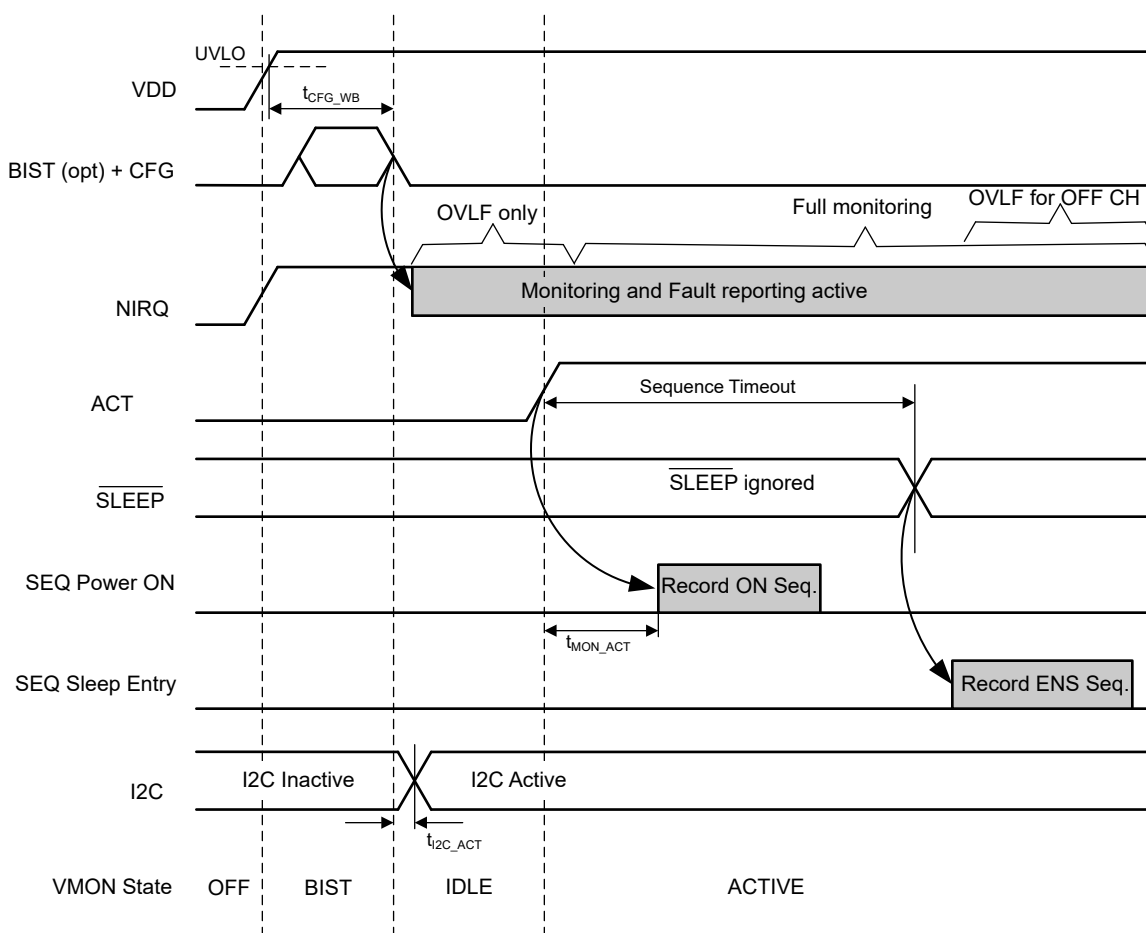
Upon Power-On-Reset, the TPS389006 needs to make a decision whether to run BIST or not, based on the value of the [TEST_CFG.AT_POR](#) register bit. Assuming that ECC on this register is performed after BIST has checked the ECC logic itself, it is not possible to guarantee its data integrity before running BIST.

8.4.2 TPS389006 Power ON

When the TPS389006 is powered ON, BIST is optionally executed (depending on TEST_CFG.AT_POR register bit); I²C and fault reporting (through NIRQ) become active as soon as BIST is completed and configuration is loaded from OTP (assisted by ECC, supporting SEC-DED).

The details of the configuration load ECC and BIST results are reported in TEST_INFO register.

Upon detection of the ACT rising edge, the TPS389006 starts the sequence timeout timer and the monitoring of the power ON sequence. SLEEP is ignored until ACT is High and the sequence timeout has expired. The TPS389006 will then act on SLEEP transitions to monitor/record Sleep Entry/Exit sequences.



8-7. TPS389006 Power ON Signaling and Internal States

BIST completion can be detected through interrupt or register polling:

- Interrupt: INT_TEST.I_BIST_C flag is set and NIRQ is asserted if IEN_TEST.BIST_C=1
- Polling: VMON_STAT register can be polled to read the ST_BIST_C bit

8.4.3 General Monitoring

TPS389006 has multiple monitoring modes including IDLE, ACTIVE, SLEEP, and DEEP SLEEP. These modes refer to the monitoring states of the device shown in [表 8-3](#).

8.4.3.1 IDLE Monitoring

The TPS389006 is in IDLE state when ACT is Low and BIST is completed.

In this state, all monitored channels are expected to be in the OFF state (below the OFF threshold).

For the enabled channels in OFF state, only the Over-voltage Low Frequency (OVLF) thresholds are monitored to ensure the reliability limits are not violated.

8.4.3.2 ACTIVE Monitoring

The TPS389006 is in ACTIVE state when ACT is High.

VMON monitors high frequency channel levels (copparator sense path) and low frequency channel levels (ADC sense path) against Under-Voltage High Frequency (UVHF), Over-Voltage High Frequency (OVHF), Under-Voltage Low Frequency (UVLF), and Over-Voltage Low Frequency (OVLF) thresholds.

Some channels can be connected to rails which are controlled by user software. Such channels can be in the OFF state (below the OFF threshold) when the TPS389006 is in an ACTIVE state, and have the UVLF/UVHF interrupts normally disabled. Once these rails are turned ON, the TPS389006 host enables the channels UVLF/UVHF interrupts to allow full monitoring. Similarly, before these rails are turned OFF, the TPS389006 host disables the channels UVLF/UVHF interrupts to avoid false UV violations during the ramp down. As these channels are not part of the sequencing initiated by ACT or $\overline{\text{SLEEP}}$, their UVLF/UVHF/OVHF interrupts cannot be automatically enabled/disabled using the auto-mask registers. While in the OFF state, only the OVLF thresholds are monitored to ensure the reliability limits are not violated.

Other enabled channels can be in OFF state as a result of the $\overline{\text{SLEEP}}$ 1→0 transition sequence. Those channels are identified by the AMSK_ENS auto-mask register, used to avoid UVLF interrupts (as well as UVHF and OVHF interrupts) during the transition. For those channels in the OFF state and identified by the AMSK_ENS register, only the OVLF thresholds are monitored to ensure the reliability limits are not violated.

表 8-3. Modes of Operation Summary

| Mode | Pin/Bit Condition | Iq | Monitored- Triggers NIRQ if CHx enabled | Status only | ADC/Telemetry |
|---|--------------------------------|-------|---|-------------|---------------|
| ACTIVE | ACT=High, Sleep=High | 1.5mA | OVLF, UVLF, OVHF, UVHF | OFF | Enabled |
| IDLE | ACT=Low, Sleep=X | 230uA | OVLF | OFF | Disabled |
| SLEEP ACT=High, SLEEP=Low Sleep Power bit=1 | CHx not assigned to Sleep | 1.5mA | OVLF, UVLF, OVHF, UVHF | OFF | Enabled |
| | CHx assigned to Sleep (AMSK=1) | | OVLF | OFF | |
| | CHx assigned to Sleep (AMSK=0) | | OVLF, UVLF, OVHF, UVHF | OFF | |
| DEEP SLEEP ACT=High, SLEEP=Low Sleep Power bit=0 | CHx not assigned to Sleep | 330uA | OVHF, UVHF | - | Disabled |
| | CHx assigned to Sleep (AMSK=1) | | No monitoring | - | |
| | CHx assigned to Sleep (AMSK=0) | | OVHF, UVHF | - | |

8.4.3.3 Sequence Monitoring 1

In addition to voltage monitoring, voltage rails sequences are also monitored on ACT and $\overline{\text{SLEEP}}$ changes, or on setting SEQ_REC_CTL.REC_START=1.

Sequence Monitoring 1 is a transitional state entered when:

1. ACT transitions 0→1
2. $\overline{\text{SLEEP}}$ transitions 0→1, if ACT=1
3. $\overline{\text{SLEEP}}$ transitions 1→0, if ACT=1

4. Host sets SEQ_REC_CTL.REC_START=1

The first three transitions trigger the same set of actions, with the TPS389006 always ending in the ACTIVE state. However, the registers used to log and check the sequencing information are different.

The fourth method to start sequence monitoring (register bit set by the host) gives the flexibility to the host to decide when and where to track a sequence while the external signals are static. This is useful, for example, when software shutdown is initiated using FORCE_SHUTDOWN[1:0].

The following sections describe the actions for the first three cases explicitly for clarity.

8.4.3.3.1 ACT Transitions 0→1

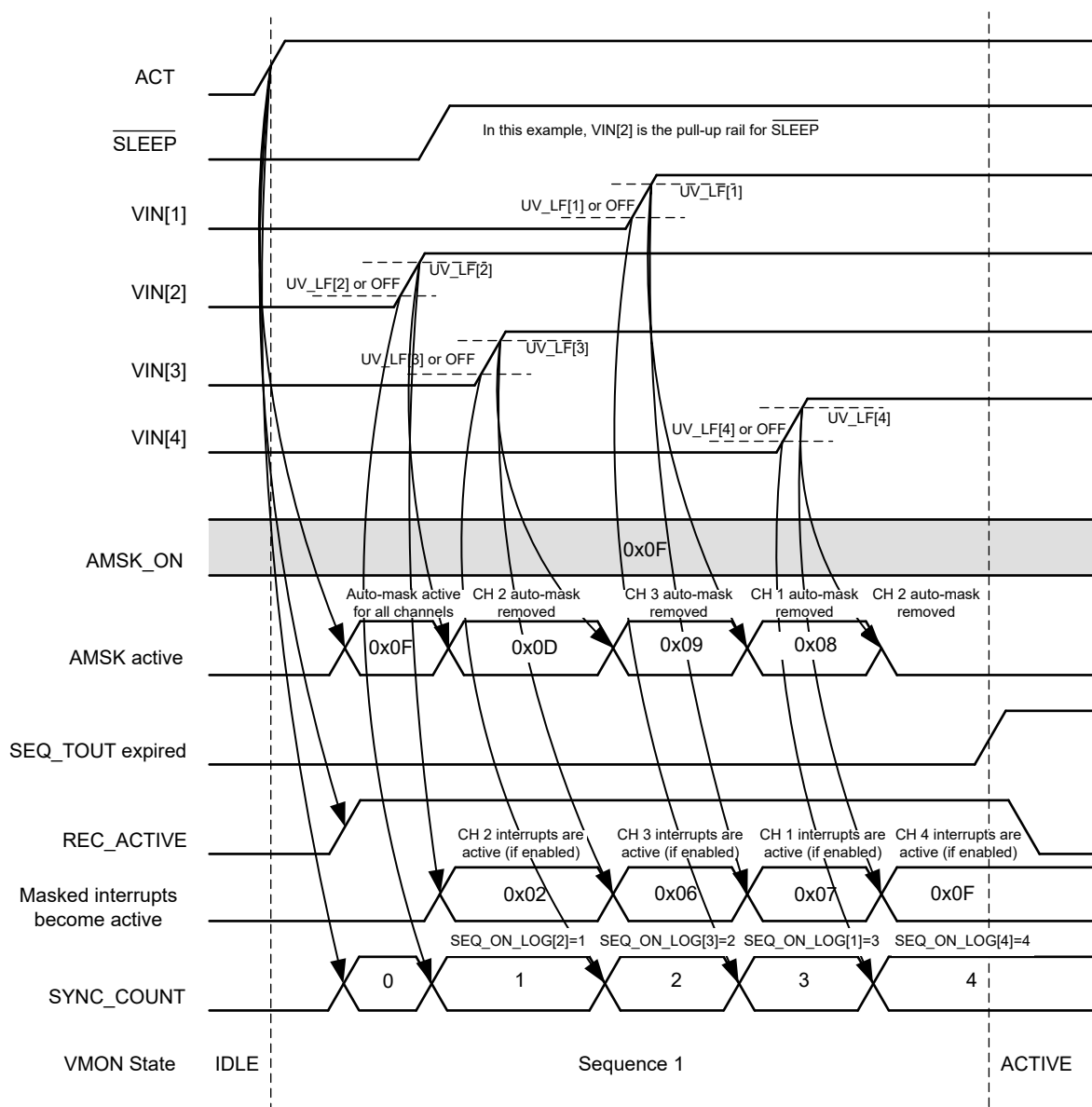
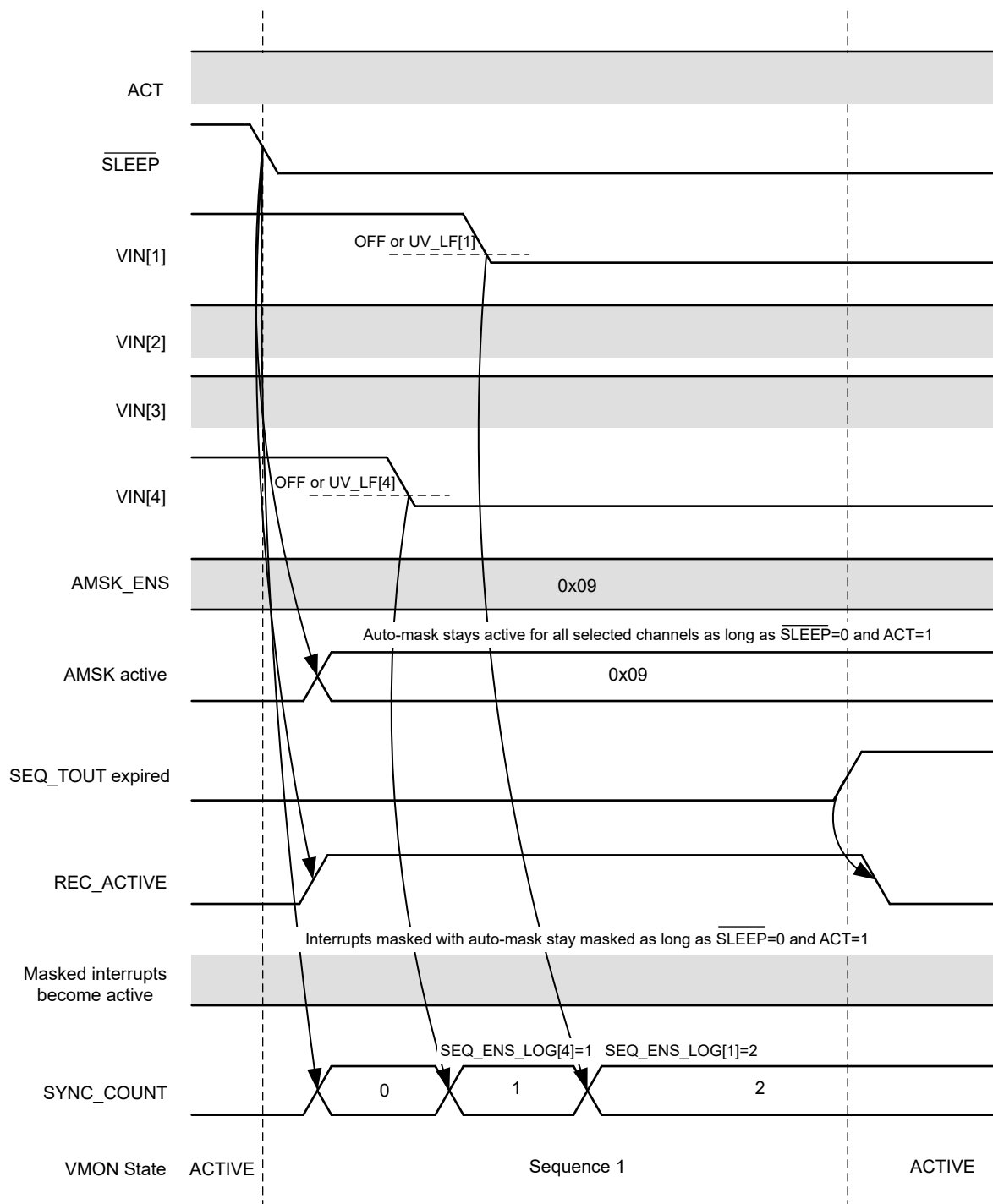


FIG 8-8. ACT 0→1 Transition

1. The TPS389006 takes several actions on the ACT 0→1 transition:
 - a. The synchronization counter is reset to 0.
 - b. The REC_ACTIVE bit is set, and SEQ[1:0] bits are updated to 00b.

- c. If the sequence overwrite bit is enabled (EN_SEQ_OW=1), the sequence logging registers (SEQ_ON_LOG[N]) are overwritten with new data. If there was data in the registers that was not read by the host (SEQ_ON_RDY still set), the sequence overwrite flag (SEQ_ON_OW) gets set.
 - d. If the timestamps overwrite bit is enabled (EN_TS_OW=1), the timestamp logging registers (SEQ_TIME_xSB[N]) are overwritten with new data. If there was data in the registers that was not read by the host (TS_RDY still set), the timestamp overwrite flag (TS_OW) is set.
 - e. If the sequence overwrite bit is disabled (EN_SEQ_OW=0) and there was data in the registers SEQ_ON_LOG[N] that was not read and acknowledged by the host (SEQ_ON_RDY still set), the sequence overwrite flag (SEQ_ON_OW) is set and does not overwrite the registers with new data.
 - f. If the timestamp overwrite bit is disabled (EN_TS_OW=0) and there was data in the registers SEQ_TIME_xSB[N] that was not read and acknowledged by the host (TS_RDY still set), the timestamp overwrite flag (TS_OW) is set and does not overwrite the registers with new data.
 - g. The internal sequence timer is (re)started.
2. All TPS389006 inputs selected with auto-mask register AMASK_ON start with masked (disabled) interrupts for Under-Voltage Low Frequency (UVLF), Under-Voltage High Frequency (UVHF), and Over-Voltage High Frequency (OVHF) conditions.
3. As each rail passes the UVLF threshold (UV_LF[N]), automatically (and expected to happen within about 5-10 μ s) the relevant UV and OV interrupts are unmasked and enabled/disabled according to the IEN_UVLF, IEN_UVHF, and IEN_OVHF registers.
4. As each rail passes the UVLF or OFF threshold (depending on SEQ_UP_THLD.OFF_UV[N] register setting), the rail is tagged with a counter corresponding to the order of rising edge transition. A timestamp is also logged.
 - a. the tag value stored in the relevant status register SEQ_ON_LOG[N] if allowed as per overwrite settings and status. also, the timestamp of the event is stored in registers SEQ_TIME_MSB[N] and SEQ_TIME_LSB[N] as allowed by the overwrite settings and status.
 - b. the SEQ_ON_LOG[N] register is compared to the expected sequence order value defined in register SEQ_EXP[N], and an interrupt is generated if different and if the relevant interrupt enable bit is set (IEN_SEQ_ON). Note that if overwrite settings and recording status do not allow writing new data to the logging registers, then the comparison cannot be performed and no interrupt will be generated.
5. After a timeout, tagging stops.
 - a. Clear the REC_ACTIVE bit.
 - b. If rails are up with the correct sequence, TPS389006 is in ACTIVE state and starts normal monitoring.
 - c. If any rail has a tag not matching the configured value in SEQ_ON_EXP[N] register, NIRQ is asserted. The TPS389006 continues normal monitoring.
 - d. If $\overline{\text{SLEEP}}$ is low, the TPS389006 will not start recording the Sleep Entry sequence, as sequence recording is started on ACT and $\overline{\text{SLEEP}}$ transitions, or when initiated through I²C command.

8.4.3.3.2 SLEEP Transition 1→0

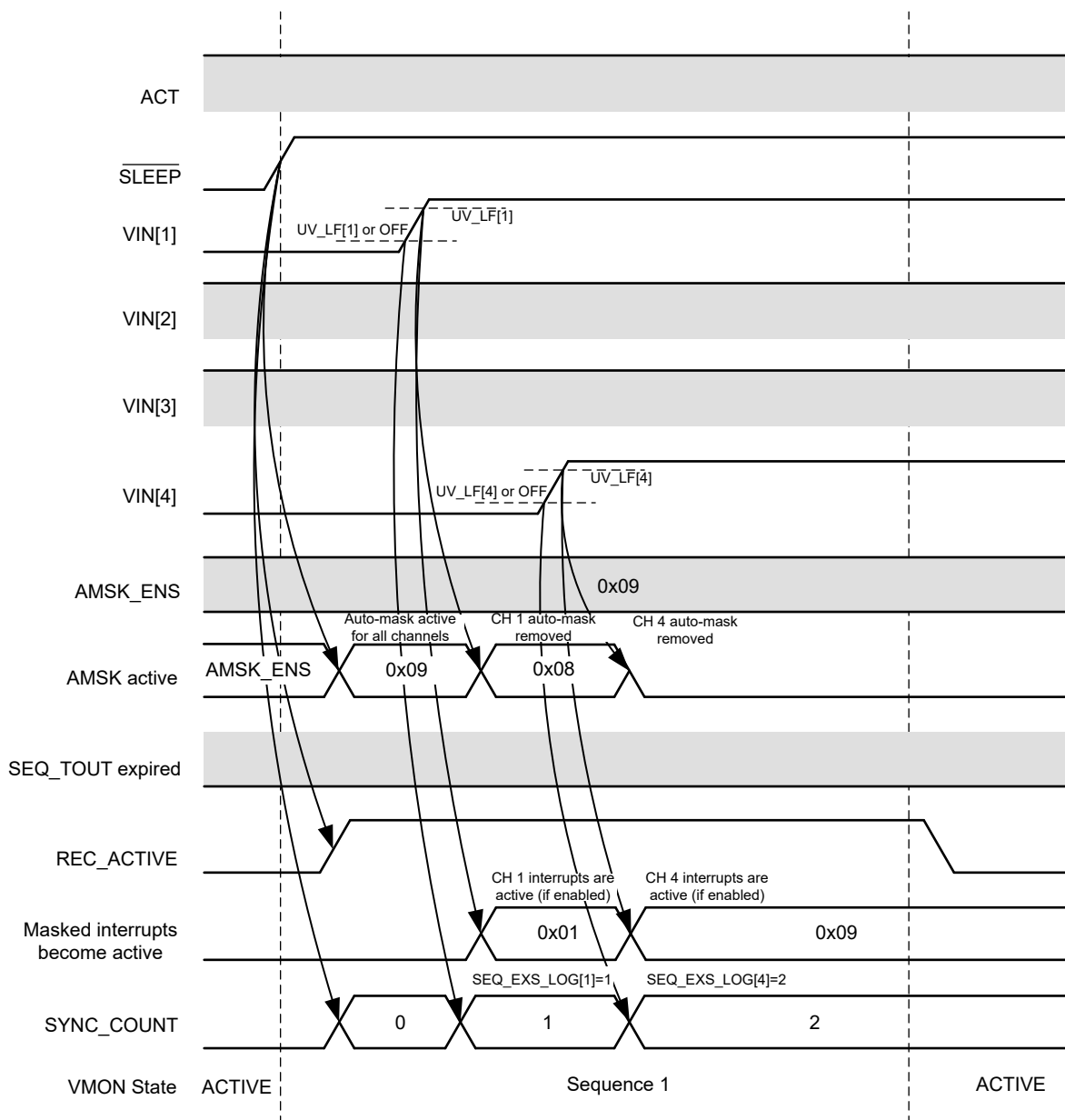


8-9. SLEEP 1→0 Transition

1. The TPS389006 takes several actions on the $\overline{\text{SLEEP}}$ 1→0 transition:
 - a. The synchronization counter is reset to 0.
 - b. The REC_ACTIVE bit is set, and SEQ[1:0] bits are updated to 11b.
 - c. If the sequence overwrite bit is enabled (EN_SEQ_OW=1), the sequence logging registers (SEQ_ENS_LOG[N]) are overwritten with new data. If there was data in the registers that was not read by the host (SEQ_ENS_RDY still set), the timestamp overwrite flag (TS_OW) is set.

- d. If the timestamp overwrite bit is enabled (EN_TS_OW=1), the timestamp logging registers (SEQ_TIME_xSB[N]) are overwritten with new data. If there was data in the registers that was not read by the host (TS_RDY still set), the timestamp overwrite flag (TS_OW) is set.
- e. If the sequence overwrite bit is disabled (EN_SEQ_OW=0) and there was data in the registers SEQ_ENS_LOG[N] that was not read and acknowledged by the host (SEQ_ENS_RDY still set), the sequence overwrite flag (SEQ_ENS_OW) is set, and the registers are not overwritten with new data.
- f. If the timestamp overwrite bit is disabled (EN_TS_OW=0) and there was data in the registers SEQ_TIME_xSB[N] that was not read and acknowledged by the host (TS_RDY still set), the timestamp overwrite flag (TS_OW) is set, and the registers are not overwritten with new data.
- g. The internal sequence timer is (re)started.
2. Relevant TPS389006 inputs selected with auto-mask register AMSK_ENS are set with masked interrupts for UVLF, UVHF and OVHF conditions.
3. As each rail passes the OFF or UVLF threshold (depending on SEQ_DN_THLD.OFF_UV[N] register setting), the rail is tagged with a counter corresponding to the order of falling edge transition. A timestamp is also logged.
 - a. The tag value is stored in the relevant status register SEQ_ENS_LOG[N] if allowed as per overwrite settings and status. Also, the timestamp of the event is stored in registers SEQ_TIME_MSB[N] and SEQ_TIME_LSB[N] as allowed by the overwrite settings and status.
 - b. The SEQ_ENS_LOG[N] register is compared to the expected sequence order value defined in register SEQ_ENS_EXP[N], and an interrupt is generated if different and if the relevant interrupt enable bit is set (IEN_SEQ_ENS). Note that if overwrite settings and recording status do not allow writing new data to the logging registers, then the comparison cannot be performed and no interrupt will be generated.
4. After timeout, tagging stops.
 - a. The REC_ACTIVE bit is cleared.
 - b. If rails are down with the correct sequence, TPS389006 is in ACTIVE state and continues normal monitoring (only OVLF thresholds are monitored for enabled channels in OFF state).

8.4.3.3.3 SLEEP Transition 0→1



8-10. SLEEP 0→1 Transition

1. The TPS389006 takes several actions on the SLEEP 0→1 transition:
 - a. The synchronization counter is reset to 0.
 - b. The REC_ACTIVE bit is set, and SEQ[1:0] bits are updated to 10b.
 - c. If the sequence overwrite bit is enabled (EN_SEQ_OW=1), the sequence logging registers (SEQ_EXS_LOG[N]) are overwritten with new data. If there was data in the registers that was not read by the host (SEQ_EXS_RDY still set), the sequence overwrite flag (SEQ_EXS_OW) is set.
 - d. If the timestamp overwrite bit is enabled (EN_TS_OW=1), the timestamp logging registers (SEQ_TIME_xSB[N]) are overwritten with new data. If there was data in the registers that was not read by the host (TS_RDY still set), the timestamp overwrite flag (TS_OW) is set.
 - e. If the sequence overwrite bit is disabled (EN_SEQ_OW=0) and there was data in the registers SEQ_EXS_LOG[N] that was not read and acknowledged by the host (SEQ_EXS_RDY still set), the sequence overwrite flag (SEQ_EXS_OW) is set, and the registers are not overwritten with new data.

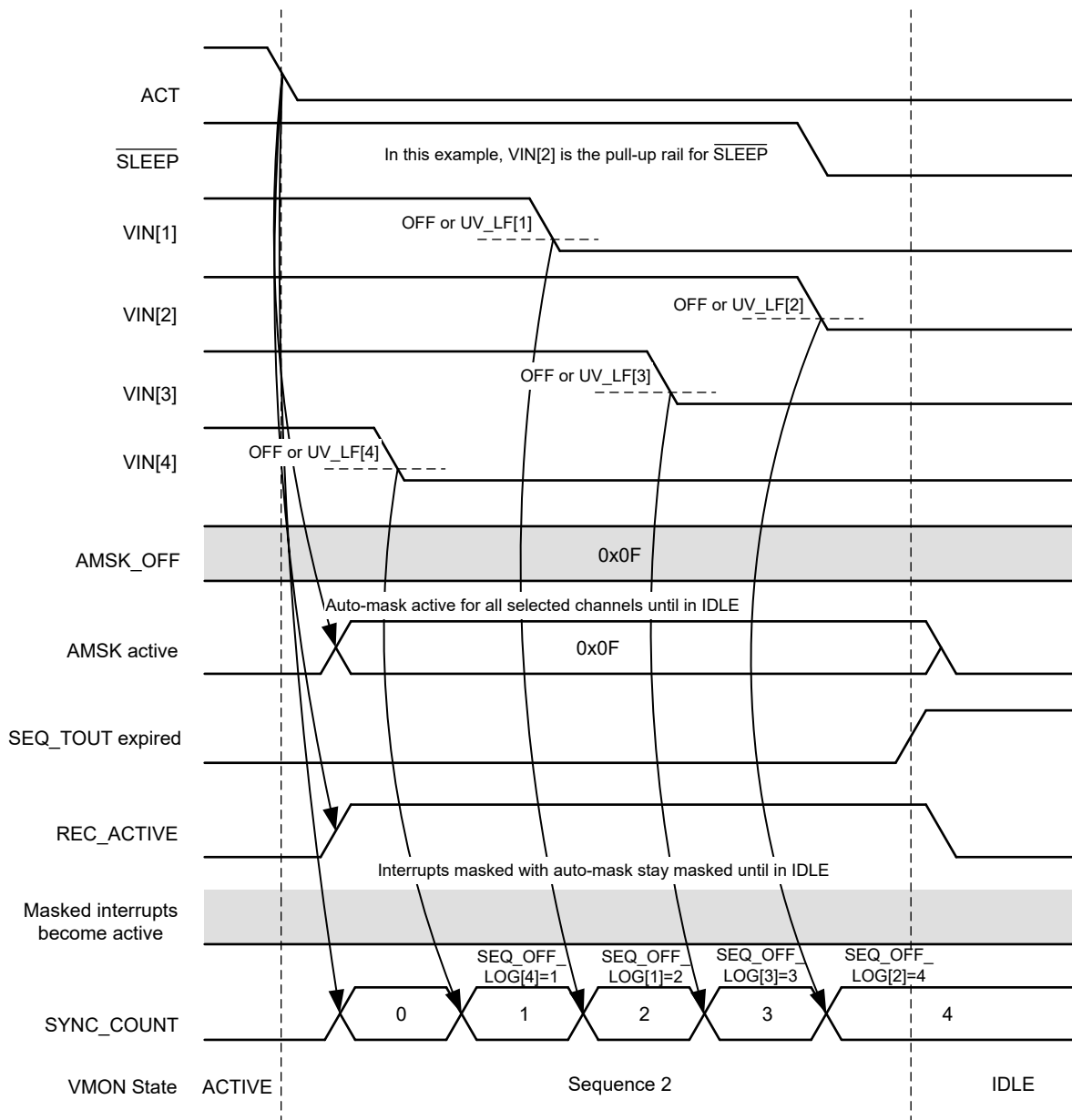
- f. If the timestamp overwrite bit is disabled (EN_TS_OW=0) and there was data in the registers SEQ_TIME_xSB[N] that was not read and acknowledged by the host (TS_RDY still set), the timestamp overwrite flag (TS_OW) is set, and the registers are not overwritten with new data.
 - g. The internal sequence timer is (re)started.
2. Relevant TPS389006 inputs selected with auto-mask register AMSK_EXS are set with masked (disabled) interrupts for UVLF, UVHF, and OVHF conditions.
3. As each rail passes the UVLF threshold (UV_LF[N]), automatically (and expected to happen within about 5-10 μ s) the relevant UV and OV interrupts are unmasked and enabled/disabled according to the IEN_UVLF, IEN_UVHF, and IEN_OVHF registers.
4. As each rail passes the UVLF or OFF threshold (depending on SEQ_UP_THLD.OFF_UV[N] register setting), the rail is tagged with a counter corresponding to the order of rising edge transition. A timestamp is also logged.
 - a. The tag value is stored in the relevant status register SEQ_EXS_LOG[N] if allowed as per overwrite settings and status. Also, the timestamp of the event is stored in registers SEQ_TIME_MSB[N] and SEQ_TIME_LSB[N] as allowed by the overwrite settings and status.
 - b. The SEQ_EXS_LOG[N] register is compared to the expected sequence order value defined in register SEQ_EXS_EXP[N], and an interrupt is generated if different and if relevant interrupt enable bit is set (IEN_SEQ_EXS). Note that if overwrite settings and recording status do not allow writing new data to the logging registers, then the comparison cannot be performed and no interrupt will be generated.
5. After a timeout, tagging stops.
 - a. The REC_ACTIVE bit is cleared.
 - b. If rails are up with the correct sequence, TPS389006 is in ACTIVE state and starts normal monitoring.
 - c. If any rail has a tag not matching the configured value in SEQ_EXS_EXP[N] register, NIRQ is asserted. TPS389006 continues normal monitoring.

8.4.3.4 Sequence Monitoring 2

Sequence Monitoring 2 is very similar to Sequence Monitoring 1, however, an extra step is taken when exiting this transitioning state depending on the TEST_CFG.AT_SHDN register bit.

Sequence Monitoring 2 is entered when ACT transitions 1→0. The actions taken are described in [セクション 8.4.3.4.1](#).

8.4.3.4.1 ACT Transition 1→0



8-11. ACT 1→0 Transition

1. The TPS389006 takes several actions on the ACT 1→0 transition:
 - a. The synchronization counter is reset to 0.
 - b. The REC_ACTIVE bit is set, and SEQ[1:0] bits are updated to 01b.
 - c. If the sequence overwrite bit is enabled (EN_SEQ_OW=1), the sequence logging registers (SEQ_OFF_LOG[N]) are overwritten with new data. If there was data in the registers that was not read by the host (SEQ_OFF_RDY still set), the sequence overwrite flag (SEQ_OFF_OW) is set.
 - d. If the timestamp overwrite bit is enabled (EN_TS_OW=1), the timestamp logging registers (SEQ_TIME_xSB[N]) are overwritten with new data. If there was data in the registers that was not read by the host (TS_RDY still set), the timestamp overwrite flag (TS_OW) is set.
 - e. If the sequence overwrite bit is disabled (EN_SEQ_OW=0) and there was data in the registers SEQ_OFF_LOG[N] that was not read and acknowledged by the host (SEQ_OFF_RDY still set), the sequence overwrite flag (SEQ_OFF_OW) is set, and the registers are not overwritten with new data.

- f. If the timestamp overwrite bit is disabled (EN_TS_OW=0) and there was data in the registers SEQ_TIME_xSB[N] that was not read and acknowledged by the host (TS_RDY still set), the timestamp overwrite flag (TS_OW) is set, and the registers are not overwritten with new data.
 - g. The internal sequence timer is (re)started.
 2. All TPS389006 inputs selected with auto-mask register AMSK_OFF are set with masked (disabled) interrupts for UVLF, UVHF, and OVHF conditions.
 3. As each rail passes the OFF or UVLF threshold (depending on SEQ_DN_THLD.OFF_UV[N] register setting), the rail is tagged with a counter corresponding to the order of falling edge transition. A timestamp is also logged.
 - a. The tag value is stored in the relevant status register SEQ_OFF_LOG[N] if allowed as per overwrite settings and status. Also, the timestamp of the event is stored in registers SEQ_TIME_MSB[N] and SEQ_TIME_LSB[N] as allowed by the overwrite settings and status.
 - b. The SEQ_OFF_LOG[N] register is compared to the expected sequence order value defined in register SEQ_OFF_EXP[N], and an interrupt is generated if different and if relevant interrupt enable bit is set (IEN_SEQ_OFF). Note that if overwrite settings and recording status do not allow writing new data to the logging registers, then the comparison cannot be performed and no interrupt will be generated.
 4. After timeout, tagging stops.
 - a. The REC_ACTIVE bit is cleared.
 - b. If rails are down with the correct sequence, proceed to check TEST_CFG.AT_SHDN register bit.
 - c. If any rail has a tag not matching the configured value in SEQ_OFF_EXP[N] register, NIRQ is asserted. TPS389006 proceeds to check TEST_CFG.AT_SHDN register bit.
 5. If TEST_CFG.AT_SHDN register bit is set, BIST is executed (next state depends on BIST results).
 6. If TEST_CFG.AT_SHDN register bit is no set, the TPS389006 enters IDLE state.

8.5 Register Maps

The register map is designed to support up to 16 channels through register banks, with the following organization:

- [Bank 0 - Status Register Set Summary:](#)
 - Vendor info and usage registers (bank independent)
 - Interrupt registers
 - Status registers
 - Bank selection register (bank independent)
 - Protection registers (bank independent)
 - Device configuration registers (bank independent)
- [Bank 1 - Channel 1-8 Configuration Register Set Summary:](#)
 - Vendor info and usage registers (bank independent)
 - Control registers (device global registers)
 - Monitor configuration registers (channel specific registers)
 - Sequence configuration registers (both device global and channel specific registers)
 - Bank selection register (bank independent)
 - Protection registers (bank independent)
 - Device configuration registers (bank independent)

Bank independent registers are accessible at the same address irrespective of the current bank selection. Access to other registers requires the proper bank being selected.

All registers are 8-bit wide, and are loaded at boot with the default value described here or with the OTP value programmed at the factory.

Unused registers addresses are reserved for future use and support up to 16 channels.

Write accesses to protected registers (see PROT1/2 details), invalid registers, or valid registers with invalid data, should be NACK'd.

8.5.1 BANK0 Registers

表 8-4 lists the memory-mapped registers for the BANK0 registers. All register offset addresses not listed in 表 8-4 should be considered as reserved locations and the register contents should not be modified.

表 8-4. BANK0 Registers

| Address | Acronym | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|-----------------|-----------|----------------|----------|------------|-------------|-------------|-------------|
| 0x10 | INT_SRC | F_OTHER | RSVD | | | | TEST | CONTROL | MONITOR |
| 0x11 | INT_MONITOR | SEQ_ON | SEQ_OFF | SEQ_EXS | SEQ_ENS | OV_LF | OV_HF | UV_LF | UV_HF |
| 0x12 | INT_UVHF | RSVD | | UVHF[N] | | | | | |
| 0x14 | INT_UVLF | RSVD | | UVLF[N] | | | | | |
| 0x16 | INT_OVHF | RSVD | | OVHF[N] | | | | | |
| 0x18 | INT_OVLF | RSVD | | OVLF[N] | | | | | |
| 0x1A | INT_SEQ_ON | RSVD | | F_SEQ_ON[N] | | | | | |
| 0x1C | INT_SEQ_OFF | RSVD | | F_SEQ_OFF[N] | | | | | |
| 0x1E | INT_SEQ_EXS | RSVD | | F_SEQ_EXS[N] | | | | | |
| 0x20 | INT_SEQ_ENS | RSVD | | F_SEQ_ENS[N] | | | | | |
| 0x22 | INT_CONTROL | RSVD | | | F_CRC | F_NIRQ | F_TSD | F_SYNC | F_PEC |
| 0x23 | INT_TEST | RSVD | | | | ECC_SE_C | ECC_DE_D | I_BIST_C | BIST |
| 0x24 | INT_VENDOR | LDO_OV_Error | | Freq_DEV_Error | | SHORT_DET | OPEN_DET | RSVD | |
| 0x30 | VMON_STAT | FAILSAFE | ST_BIDT_C | ST_VDD | ST_NIRQ | ST_ACTS_LP | ST_ACTS_HDN | ST_SYNC | RSVD |
| 0x31 | TEST_INFO | RSVD | | ECC_SE_C | ECC_DE_D | BIST_VM | BIST_NV_M | BIST_L | BIST_A |
| 0x32 | OFF_STAT | RSVD | | VIN[N] | | | | | |
| 0x34 | SEQ_REC_STAT | REC_ACTIVE | SEQ | | TS_RDY | SEQ_ON_RDY | SEQ_OFF_RDY | SEQ_EXS_RDY | SEQ_ENS_RDY |
| 0x35 | SEQ_OW_STAT | RSVD | | | TS_OW | SEQ_ON_OW | SEQ_OFF_OW | SEQ_EXS_OW | SEQ_ENS_OW |
| 0x36 | SEQ_ORD_STAT | SYNC_COUNT[7:0] | | | | | | | |
| 0x40 | MON_LVL[1] | ADC[7:0] | | | | | | | |
| 0x41 | MON_LVL[2] | ADC[7:0] | | | | | | | |
| 0x42 | MON_LVL[3] | ADC[7:0] | | | | | | | |
| 0x43 | MON_LVL[4] | ADC[7:0] | | | | | | | |
| 0x44 | MON_LVL[5] | ADC[7:0] | | | | | | | |
| 0x45 | MON_LVL[6] | ADC[7:0] | | | | | | | |
| 0x50 | SEQ_ON_LOG[1] | ORDER[7:0] | | | | | | | |
| 0x51 | SEQ_ON_LOG[2] | ORDER[7:0] | | | | | | | |
| 0x52 | SEQ_ON_LOG[3] | ORDER[7:0] | | | | | | | |
| 0x53 | SEQ_ON_LOG[4] | ORDER[7:0] | | | | | | | |
| 0x54 | SEQ_ON_LOG[5] | ORDER[7:0] | | | | | | | |
| 0x55 | SEQ_ON_LOG[6] | ORDER[7:0] | | | | | | | |
| 0x60 | SEQ_OFF_LOG[1] | ORDER[7:0] | | | | | | | |
| 0x61 | SEQ_OFF_LOG[2] | ORDER[7:0] | | | | | | | |
| 0x62 | SEQ_OFF_LOG[3] | ORDER[7:0] | | | | | | | |
| 0x63 | SEQ_OFF_LOG[4] | ORDER[7:0] | | | | | | | |
| 0x64 | SEQ_OFF_LOG[5] | ORDER[7:0] | | | | | | | |

表 8-4. BANK0 Registers (continued)

| Address | Acronym | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------------|------------|---------------|--------|-------|-------|-----------------|-------------|--------|
| 0x65 | SEQ_OFF_LOG[6] | ORDER[7:0] | | | | | | | |
| 0x70 | SEQ_EXS_LOG[1] | ORDER[7:0] | | | | | | | |
| 0x71 | SEQ_EXS_LOG[2] | ORDER[7:0] | | | | | | | |
| 0x72 | SEQ_EXS_LOG[3] | ORDER[7:0] | | | | | | | |
| 0x73 | SEQ_EXS_LOG[4] | ORDER[7:0] | | | | | | | |
| 0x74 | SEQ_EXS_LOG[5] | ORDER[7:0] | | | | | | | |
| 0x75 | SEQ_EXS_LOG[6] | ORDER[7:0] | | | | | | | |
| 0x80 | SEQ_ENS_LOG[1] | ORDER[7:0] | | | | | | | |
| 0x81 | SEQ_ENS_LOG[2] | ORDER[7:0] | | | | | | | |
| 0x82 | SEQ_ENS_LOG[3] | ORDER[7:0] | | | | | | | |
| 0x83 | SEQ_ENS_LOG[4] | ORDER[7:0] | | | | | | | |
| 0x84 | SEQ_ENS_LOG[5] | ORDER[7:0] | | | | | | | |
| 0x85 | SEQ_ENS_LOG[6] | ORDER[7:0] | | | | | | | |
| 0x90 | SEQ_TIME_MSB[1] | CLOCK[7:0] | | | | | | | |
| 0x91 | SEQ_TIME_LSB[1] | CLOCK[7:0] | | | | | | | |
| 0x92 | SEQ_TIME_MSB[2] | CLOCK[7:0] | | | | | | | |
| 0x93 | SEQ_TIME_LSB[2] | CLOCK[7:0] | | | | | | | |
| 0x94 | SEQ_TIME_MSB[3] | CLOCK[7:0] | | | | | | | |
| 0x95 | SEQ_TIME_LSB[3] | CLOCK[7:0] | | | | | | | |
| 0x96 | SEQ_TIME_MSB[4] | CLOCK[7:0] | | | | | | | |
| 0x97 | SEQ_TIME_LSB[4] | CLOCK[7:0] | | | | | | | |
| 0x98 | SEQ_TIME_MSB[5] | CLOCK[7:0] | | | | | | | |
| 0x99 | SEQ_TIME_LSB[5] | CLOCK[7:0] | | | | | | | |
| 0x9A | SEQ_TIME_MSB[6] | CLOCK[7:0] | | | | | | | |
| 0x9B | SEQ_TIME_LSB[6] | CLOCK[7:0] | | | | | | | |
| 0xF0 | BANK_SEL | RSVD | | | | | | BANK_SELECT | BANK |
| 0xF1 | PROT1 | RSVD | | WRKC | WRKS | CFG | IEN | MON | SEQ |
| 0xF2 | PROT2 | RSVD | | WRKC | WRKS | CFG | IEN | MON | SEQ |
| 0xF3 | PROT_MON2 | RSVD | | MON[N] | | | | | |
| 0xF9 | I2CADDR | RSVD | ADDR_NVM[3:0] | | | | ADDR_STRAP[2:0] | | |
| 0xFA | DEV_CFG | RSVD | | | | | | | SOC_IF |

Complex bit access types are encoded to fit into small table cells. 表 8-5 shows the codes that are used for access types in this section.

表 8-5. BANK0 Access Type Codes

| Access Type | Code | Description |
|-------------------------------|---------|---------------------|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| W1C | W 1C | Write 1 to clear |
| Reset or Default Value | | |

表 8-5. BANK0 Access Type Codes (continued)

| Access Type | Code | Description |
|-------------|------|--|
| -n | | Value after reset or the default value |

8.5.1.1 INT_SRC Register (Address = 0x10) [Default = X]

INT_SRC is shown in 表 8-6.

Return to the [Summary Table](#).

Global Interrupt Source Status register. This register contains fault interrupts on UV/OV HF/LF interrupts and internal fault interrupt and other interrupt. INT_SRC represents the reason why NIRQ was asserted. When the host processor receives NIRQ, the processor can read this register to quickly determine the source of the interrupt. If this register is clear, then the device did not assert NIRQ.

表 8-6. INT_SRC Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|---------|------|---------|--|
| 7 | F_OTHER | R | X | Vendor specific internal fault. Details reported in INT_F_OTHER. This bit represents the ORed value of all bits in INT_F_OTHER. 0b = No fault reported in INT_F_OTHER 1b = Fault reported in INT_F_OTHER |
| 6:3 | RSVD | R | X | RSVD |
| 2 | TEST | R | X | Internal test or configuration load fault. Details reported in INT_TEST. Represents ORed value of all bits in INT_TEST. 0b = No test/configuration fault detected 1b = Test/configuration fault detected |
| 1 | CONTROL | R | X | Control status or communication fault. Details reported in INT_CONTROL. Represents ORed value of all bits in INT_CONTROL. 0b = No status or communication fault detected 1b = Status or communication fault detected |
| 0 | MONITOR | R | X | Voltage or sequence monitor fault. Details reported in INT_MONITOR. Represents ORed value of all bits in INT_MONITOR. 0b = No voltage or sequence fault detected 1b = Voltage or sequence fault detected |

8.5.1.2 INT_MONITOR Register (Address = 0x11) [Default = X]

INT_MONITOR is shown in 表 8-7.

Return to the [Summary Table](#).

Voltage and Sequence Monitor Interrupt Status register. This register contains fault interrupts for sequence entry/exit from act/sleep modes and HF and LF faults.

表 8-7. INT_MONITOR Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|---|
| 7 | SEQ_ON | R | X | Power ON Sequence Fault. Details reported in INT_SEQ_ON. Represents ORed value of all bits in INT_SEQ_ON. A Power ON Sequence fault occurs when the content of SEQ_ON_LOG[N] register does not match the value defined in SEQ_ON_EXP[N] register. 0b = No Power ON Sequence fault detected 1b = Power ON Sequence fault detected |

表 8-7. INT_MONITOR Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|---------|------|---------|--|
| 6 | SEQ_OFF | R | X | Power OFF Sequence Fault. Details reported in INT_SEQ_OFF. Represents ORed value of all bits in INT_SEQ_OFF. A Power OFF Sequence fault occurs when the content of SEQ_OFF_LOG[N] register does not match the value defined in SEQ_OFF_EXP[N] register. 0b = No Power OFF Sequence fault detected 1b = Power OFF Sequence fault detected |
| 5 | SEQ_EXS | R | X | Exit Sleep Sequence Fault. Details reported in INT_SEQ_EXS. Represents ORed value of all bits in INT_SEQ_EXS. An Exit Sleep Sequence fault occurs when the content of SEQ_EXS_LOG[N] register does not match the value defined in SEQ_EXS_EXP[N] register. 0b = No Exit Sleep Sequence fault detected 1b = Exit Sleep Sequence fault detected |
| 4 | SEQ_ENS | R | X | Entry Sleep Sequence Fault. Details reported in INT_SEQ_ENS. Represents ORed value of all bits in INT_SEQ_ENS. An Entry Sleep Sequence fault occurs when the content of SEQ_ENS_LOG[N] register does not match the value defined in SEQ_ENS_EXP[N] register. 0b = No Entry Sleep Sequence fault detected 1b = Entry Sleep Sequence fault detected |
| 3 | OV_LF | R | X | Over-Voltage Low Frequency Fault. Details reported in INT_OVLF. Represents ORed value of all bits in INT_OVLF. 0b = No OVLF fault detected 1b = OVLF fault detected |
| 2 | OV_HF | R | X | Over-Voltage High Frequency Fault. Details reported in INT_OVHF. Represents ORed value of all bits in INT_OVHF. 0b = No OVHF fault detected 1b = OVHF fault detected |
| 1 | UV_LF | R | X | Under-Voltage Low Frequency Fault. Details reported in INT_UVLF. Represents ORed value of all bits in INT_UVLF. 0b = No UVLF fault detected 1b = UVLF fault detected |
| 0 | UV_HF | R | X | Under-Voltage High Frequency Fault. Details reported in INT_UVHF. Represents ORed value of all bits in INT_UVHF. 0b = No UVHF fault detected 1b = UVHF fault detected |

8.5.1.3 INT_UVHF Register (Address = 0x12) [Default = X]

INT_UVHF is shown in 表 8-8.

Return to the [Summary Table](#).

High Frequency channel Under-Voltage Interrupt Status register. This register contains information on which channel had a UV HF fault.

表 8-8. INT_UVHF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|-------|---------|-------------|
| 7:6 | RSVD | R/W1C | X | RSVD |

表 8-8. INT_UVHF Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|---------|-------|---------|--|
| 5:0 | UVHF[N] | R/W1C | X | Under-Voltage High Frequency Fault for channel N (1 through 6). Trips if channel N High Frequency signal goes below UV_HF[N]. The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the UVHF fault condition is also removed (channel N High Frequency signal is above UV_HF[N]). 0b = Channel N has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1b = Channel N has UVHF fault detected |

8.5.1.4 INT_UVLF Register (Address = 0x14) [Default = X]

INT_UVLF is shown in 表 8-9.

Return to the [Summary Table](#).

Low Frequency channel Under-Voltage Interrupt Status register. This register contains information on which channel had a UV LF fault.

表 8-9. INT_UVLF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|---------|-------|---------|---|
| 7:6 | RSVD | R/W1C | X | RSVD |
| 5:0 | UVLF[N] | R/W1C | X | Under-Voltage Low Frequency Fault for channel N (1 through 6). Trips if channel N Low Frequency signal goes below UV_LF[N]. The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the UVLF fault condition is also removed (channel N Low Frequency signal is above UV_LF[N]). 0b = Channel N has no UVLF fault detected (or interrupt disabled in IEN_UVLF register) 1b = Channel N has UVLF fault detected |

8.5.1.5 INT_OVHF Register (Address = 0x16) [Default = X]

INT_OVHF is shown in 表 8-10.

Return to the [Summary Table](#).

High Frequency channel Over-Voltage Interrupt Status register. This register contains information on which channel had an OV HF fault.

表 8-10. INT_OVHF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|-------|---------|-------------|
| 7:6 | RSVD | R/W1C | X | RSVD |

表 8-10. INT_OVHF Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|---------|-------|---------|--|
| 5:0 | OVHF[N] | R/W1C | X | Over-Voltage High Frequency Fault for channel N (1 through 6). Trips if channel N High Frequency signal goes above OV_HF[N]. The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the OVHF fault condition is also removed (channel N High Frequency signal is below OV_HF[N]). 0b = Channel N has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1b = Channel N has OVHF fault detected |

8.5.1.6 INT_OVLF Register (Address = 0x18) [Default = X]

INT_OVLF is shown in 表 8-11.

Return to the [Summary Table](#).

Low Frequency channel Over-Voltage Interrupt Status register. This register contains information on which channel had an OV LF fault.

表 8-11. INT_OVLF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|---------|-------|---------|--|
| 7:6 | RSVD | R/W1C | X | RSVD |
| 5:0 | OVLF[N] | R/W1C | X | Over-Voltage Low Frequency Fault for channel N (1 through 6). Trips if channel N Low Frequency signal goes above OV_LF[N]. The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the OVLF fault condition is also removed (channel N Low Frequency signal is below OV_LF[N]). 0b = Channel N has no OVLF fault detected (or interrupt disabled in IEN_OVLF register) 1b = Channel N has OVLF fault detected |

8.5.1.7 INT_SEQ_ON Register (Address = 0x1A) [Default = X]

INT_SEQ_ON is shown in 表 8-12.

Return to the [Summary Table](#).

Power ON Sequence (ACT/ SLEEP 0 to 1) Interrupt Status register. This register contains information on which channel did not follow on sequence.

表 8-12. INT_SEQ_ON Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|-------|---------|-------------|
| 7:6 | RSVD | R/W1C | X | RSVD |

表 8-12. INT_SEQ_ON Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|-------------|-------|---------|--|
| 5:0 | F_SEQ_ON[N] | R/W1C | X | Power ON Sequence Fault for channel N (1 through 6). Trips if channel N recorded Power ON Sequence counter in SEQ_ON_LOG[N] register does not match the value defined in SEQ_ON_EXP[N] register. The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit. The bit will be set again during next sequence if the same fault is detected. 0b = Channel N has no Power ON Sequence fault detected (or interrupt disabled in IEN_SEQ_ON register) 1b = Channel N has Power ON Sequence fault detected |

8.5.1.8 INT_SEQ_OFF Register (Address = 0x1C) [Default = X]

INT_SEQ_OFF is shown in 表 8-13.

Return to the [Summary Table](#).

Power OFF Sequence (ACT/ SLEEP 1 to 0) Interrupt Status register. This register contains information on which channel did not follow off sequence.

表 8-13. INT_SEQ_OFF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------------|-------|---------|---|
| 7:6 | RSVD | R/W1C | X | RSVD |
| 5:0 | F_SEQ_OFF[N] | R/W1C | X | Power OFF Sequence Fault for channel N (1 through 6). Trips if channel N recorded Power OFF Sequence counter in SEQ_OFF_LOG[N] register does not match the value defined in SEQ_OFF_EXP[N] register. The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit. The bit will be set again during next sequence if the same fault is detected. 0b = Channel N has no Power OFF Sequence fault detected (or interrupt disabled in IEN_SEQ_OFF register) 1b = Channel N has Power OFF Sequence fault detected |

8.5.1.9 INT_SEQ_EXS Register (Address = 0x1E) [Default = X]

INT_SEQ_EXS is shown in 表 8-14.

Return to the [Summary Table](#).

Exit Sleep Sequence (ACT/ SLEEP 0 to 1) Interrupt Status register. This register contains information on which channel did not follow sleep exit sequence.

表 8-14. INT_SEQ_EXS Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|-------|---------|-------------|
| 7:6 | RSVD | R/W1C | X | RSVD |

表 8-14. INT_SEQ_EXS Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|--------------|-------|---------|---|
| 5:0 | F_SEQ_EXS[N] | R/W1C | X | Exit Sleep Sequence Fault for channel N (1 through 6). Trips if channel N recorded Exit Sleep Sequence counter in SEQ_EXS_LOG[N] register does not match the value defined in SEQ_EXS_EXP[N] register. The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit. The bit will be set again during next sequence if the same fault is detected. 0b = Channel N has no Exit Sleep Sequence fault detected (or interrupt disabled in IEN_SEQ_EXS register) 1b = Channel N has Exit Sleep Sequence fault detected |

8.5.1.10 INT_SEQ_ENS Register (Address = 0x20) [Default = X]

INT_SEQ_ENS is shown in [表 8-15](#).

Return to the [Summary Table](#).

Entry Sleep Sequence (SLEEP 1 to 0) Interrupt Status register. This register contains information on which channel did not follow sleep entry sequence.

表 8-15. INT_SEQ_ENS Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------------|-------|---------|--|
| 7:6 | RSVD | R/W1C | X | RSVD |
| 5:0 | F_SEQ_ENS[N] | R/W1C | X | Entry Sleep Sequence Fault for channel N (1 through 6). Trips if channel N recorded Entry Sleep Sequence counter in SEQ_ENS_LOG[N] register does not match the value defined in SEQ_ENS_EXP[N] register. 0b = Channel N has no Entry Sleep Sequence fault detected (or interrupt disabled in IEN_SEQ_ENS register) 1b = Channel N has Entry Sleep Sequence fault detected |

8.5.1.11 INT_CONTROL Register (Address = 0x22) [Default = X]

INT_CONTROL is shown in [表 8-16](#).

Return to the [Summary Table](#).

Control and Communication Interrupt Status Register.

表 8-16. INT_CONTROL Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|-------|---------|---|
| 7:5 | RSVD | R/W1C | X | RSVD |
| 4 | F_CRC | R/W1C | X | Runtime register CRC Fault: The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit. The bit will be set again during next register CRC check if the same fault is detected. 0b = No fault detected (or IEN_CONTROL.RT_CRC is disabled) 1b = Register CRC fault detected |

表 8-16. INT_CONTROL Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|--------|-------|---------|--|
| 3 | F_NIRQ | R/W1C | X | Interrupt pin fault (fault bit always enabled no enable bit available): The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the NIRQ fault condition is also removed. 0b = No fault detected on NIRQ pin 1b = Low resistance path to supply detected on NIRQ pin |
| 2 | F_TSD | R/W1C | X | Thermal Shutdown fault: The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the TSD fault condition is also removed. 0b = No TSD fault detected (or IEN_CONTROL.TSD is disabled) 1b = TSD fault detected |
| 1 | F_SYNC | R/W1C | X | $\overline{\text{SYNC}}$ pin fault: The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the $\overline{\text{SYNC}}$ fault condition is also removed. 0b = No fault detected on $\overline{\text{SYNC}}$ pin (or IEN_CONTROL.SYNC is disabled) 1b = Low resistance path to supply detected on $\overline{\text{SYNC}}$ pin |
| 0 | F_PEC | R/W1C | X | Packet Error Checking fault: The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit. The bit will be set again during next I2C transaction if the same fault is detected. |

8.5.1.12 INT_TEST Register (Address = 0x23) [Default = X]

INT_TEST is shown in 表 8-17.

Return to the [Summary Table](#).

Internal Test and Configuration Load Interrupt Status Register.

表 8-17. INT_TEST Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|---------|-------|---------|--|
| 7:4 | RSVD | R/W1C | X | RSVD |
| 3 | ECC_SEC | R/W1C | X | ECC single-error corrected on OTP configuration load: Write-1-to-clear will clear the bit. The bit will be set again during next OTP configuration load if the same fault is detected. 0b = No single-error corrected (or IEN_TEST.ECC_SEC is disabled) 1b = Single-error corrected |

表 8-17. INT_TEST Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|----------|-------|---------|---|
| 2 | ECC_DED | R/W1C | X | ECC double-error detected on OTP configuration load: The fault bit is always enabled (there is no associated interrupt enable bit). Write-1-to-clear will clear the bit. The bit will be set again during next OTP configuration load if the same fault is detected. 0b = No double-error detected on OTP load 1b = Double-error detected on OTP load |
| 1 | I_BIST_C | R/W1C | X | Indication of Built-In Self-Test complete: Write-1-to-clear will clear the bit. The bit will be set again on completion of next BIST execution. Write-1-to-clear will clear the bit. The bit will be set again on completion of next BIST execution. 0b = BIST not complete (or IEN_TEST.BIST_C is disabled) 1b = BIST complete |
| 0 | BIST | R/W1C | X | Built-In Self-Test fault: Write-1-to-clear will clear the bit. The bit will be set again during next BIST execution if the same fault is detected. 0b = No BIST fault detected (or IEN_TEST.BIST is disabled) 1b = BIST fault detected |

8.5.1.13 INT_VENDOR Register (Address = 0x24) [Default = X]

INT_VENDOR is shown in [表 8-18](#).

Return to the [Summary Table](#).

This register contains various internal faults and ADDR detect pin fault.

表 8-18. INT_VENDOR Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|-------|---------|--|
| 7 | RSVD | R/W1C | X | RSVD |
| 6 | LDO_OV_Error | R/W1C | X | Internal LDO fault: 0 = No internal LDO fault detected 1 = Internal LDO fault detected Write-1-to-clear will clear the bit. |
| 5 | RSVD | R/W1C | X | RSVD |
| 4 | Freq_DEV_Error | R/W1C | X | Internal Oscillator fault: 0 = No internal oscillator fault detected 1 = Internal oscillator fault detected Write-1-to-clear will clear the bit. |
| 3 | SHORT_DET | R/W1C | X | Address Pin fault: 0 = No address pin fault detected 1 = Address pin fault detected Write-1-to-clear will clear the bit. |
| 2 | OPEN_DET | R/W1C | X | Address Pin fault: 0 = No address pin fault detected 1 = Address pin fault detected Write-1-to-clear will clear the bit. |
| 1:0 | RSVD | R/W1C | X | RSVD |

8.5.1.14 VMON_STAT Register (Address = 0x30) [Default = X]

VMON_STAT is shown in [表 8-19](#).

Return to the [Summary Table](#).

Status flags for internal operations and other non critical conditions. Status register showing completion of BIST, whether active or sleep or active/shutdown.

表 8-19. VMON_STAT Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7 | FAILSAFE | R | X | Fail Safe state: 0 = Not in Fail Safe state 1 = In Fail Safe state |
| 6 | ST_BIDT_C | R | X | Built-In Self-Test state: 0 = BIST not complete 1 = BIST complete |
| 5 | ST_VDD | R | X | Current state of VDD pin: 0 = VDD pin is low. 1 = VDD pin is high. |
| 4 | ST_NIRQ | R | X | Current state of NIRQ input: 0 = NIRQ pin driven low by system. 1 = NIRQ pin driven high by system. |
| 3 | ST_ACTSLP | R | X | Current state of SLEEP input: 0 = SLEEP pin driven low by system. 1 = SLEEP pin driven high by system. |
| 2 | ST_ACTSHDN | R | X | Current state of ACT input: 0 = ACT pin driven low by system. 1 = ACT pin driven high by system. |
| 1 | ST_SYNC | R | X | Current state of SYNC pin: 0 = SYNC pin is low. 1 = SYNC pin is high. |
| 0 | RSVD | R | X | RSVD |

8.5.1.15 TEST_INFO Register (Address = 0x31) [Default = X]

TEST_INFO is shown in 表 8-20.

Return to the [Summary Table](#).

Internal Self-Test and ECC information.

表 8-20. TEST_INFO Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------|------|---------|--|
| 7:6 | RSVD | R | X | RSVD |
| 5 | ECC_SEC | R | X | Status of ECC single-error correction on OTP configuration load. 0 = no error correction applied 1 = single-error correction applied |
| 4 | ECC_DED | R | X | Status of ECC double-error detection on OTP configuration load. 0 = no double-error detected 1 = double-error detected |
| 3 | BIST_VM | R | X | Status of Volatile Memory test output from BIST. 0 = Volatile Memory test pass 1 = Volatile Memory test fail |
| 2 | BIST_NVM | R | X | Status of Non-Volatile Memory test output from BIST. 0 = Non-Volatile Memory test pass 1 = Non-Volatile Memory test fail |
| 1 | BIST_L | R | X | Status of Logic test output from BIST. 0 = Logic test pass 1 = Logic test fail |
| 0 | BIST_A | R | X | Status of Analog test output from BIST. 0 = Analog test pass 1 = Analog test fail |

8.5.1.16 OFF_STAT Register (Address = 0x32) [Default = X]

OFF_STAT is shown in 表 8-21.

Return to the [Summary Table](#).

Channel OFF status.

表 8-21. OFF_STAT Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R | X | RSVD |
| 5:0 | VIN[N] | R | X | This register represents the OFF status of each channel: 0 = channel N is NOT OFF 1 = channel N is OFF (below OFF threshold) |

8.5.1.17 SEQ_REC_STAT Register (Address = 0x34) [Default = X]

SEQ_REC_STAT is shown in 表 8-22.

Return to the [Summary Table](#).

Sequence recording status register.

表 8-22. SEQ_REC_STAT Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|--|
| 7 | REC_ACTIVE | R | X | Indicates the status of sequence logging (recording): 0 = No sequence recording active. 1 = ACT or SLEEP or SEQ_REC_CTL.REC_START initiated a power sequence and recording is active. |
| 6:5 | SEQ | R | X | Current sequence being recorded: 00b = Power ON (ACT 01) 01b = Power OFF (ACT 10) 10b = Sleep Exit (SLEEP 01) 11b = Sleep Entry (SLEEP 10) |
| 4 | TS_RDY | R | X | Timestamp data availability in SEQ_TIME_xSB registers: If EN_TS_OW=0 this bit is cleared when TS_ACK is written to 1 by the host. If EN_TS_OW=1 this bit is cleared when all the SEQ_TIME_xSB[N] registers for the enabled channels (in VIN_CH_EN register) are read. If the bit is set and REC_ACTIVE is also set, then the data in SEQ_TIME_xSB registers is being overwritten. 0 = No new data available or data already read. 1 = New data available (data still needs to be read). |
| 3 | SEQ_ON_RDY | R | X | Power ON sequence data availability in SEQ_ON_LOG registers: If EN_SEQ_OW=0 this bit is cleared when SEQ_ON_ACK is written to 1 by the host. If EN_SEQ_OW=1 this bit is cleared when all the SEQ_ON_LOG registers for the enabled channels (in VIN_CH_EN register) are read. If the bit is set and REC_ACTIVE is set and SEQ [1:0]=00b, then the data in SEQ_ON_LOG registers is being overwritten. 0 = No new data available or data already read. 1 = New data available (data still needs to be read). |
| 2 | SEQ_OFF_RDY | R | X | Power OFF sequence data availability in SEQ_OFF_LOG registers: If EN_SEQ_OW=0 this bit is cleared when SEQ_OFF_ACK is written to 1 by the host. If EN_SEQ_OW=1 this bit is cleared when all the SEQ_OFF_LOG registers for the enabled channels (in VIN_CH_EN register) are read. If the bit is set and REC_ACTIVE is set and SEQ [1:0]=01b, then the data in SEQ_OFF_LOG registers is being overwritten. 0 = No new data available or data already read. 1 = New data available (data still needs to be read). |

表 8-22. SEQ_REC_STAT Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|---|
| 1 | SEQ_EXS_RDY | R | X | Sleep Exit sequence data availability in SEQ_EXS_LOG registers: If EN_SEQ_OW=0 this bit is cleared when SEQ_EXS_ACK is written to 1 by the host. If EN_SEQ_OW=1 this bit is cleared when all the SEQ_EXS_LOG registers for the enabled channels (in VIN_CH_EN register) are read. If the bit is set and REC_ACTIVE is set and SEQ [1:0]=10b, then the data in SEQ_EXS_LOG registers is being overwritten. 0 = No new data available or data already read. 1 = New data available (data still needs to be read). |
| 0 | SEQ_ENS_RDY | R | X | Sleep Entry sequence data availability in SEQ_ENS_LOG registers: If EN_SEQ_OW=0 this bit is cleared when SEQ_ENS_ACK is written to 1 by the host. If EN_SEQ_OW=1 this bit is cleared when all the SEQ_ENS_LOG registers for the enabled channels (in VIN_CH_EN register) are read. If the bit is set and REC_ACTIVE is set and SEQ [1:0]=11b, then the data in SEQ_ENS_LOG registers is being overwritten. 0 = No new data available or data already read. 1 = New data available (data still needs to be read). |

8.5.1.18 SEQ_OW_STAT Register (Address = 0x35) [Default = X]

SEQ_OW_STAT is shown in 表 8-23.

Return to the [Summary Table](#).

Sequence recording overwrite status register.

表 8-23. SEQ_OW_STAT Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:5 | RSVD | R | X | RSVD |
| 4 | TS_OW | R | X | Timestamp data overwritten status: 0 = No data was overwritten 1 = Data was overwritten (if VMON_MISC.EN_TS_OW=1), or data could not be written (if VMON_MISC.EN_TS_OW=0) |
| 3 | SEQ_ON_OW | R | X | Power ON sequence data overwritten status: 0 = No data was overwritten 1 = Data was overwritten (if VMON_MISC.EN_SEQ_OW=1), or data could not be written (if VMON_MISC.EN_SEQ_OW=0) |
| 2 | SEQ_OFF_OW | R | X | Power OFF sequence data overwritten status: 0 = No data was overwritten 1 = Data was overwritten (if VMON_MISC.EN_SEQ_OW=1), or data could not be written (if VMON_MISC.EN_SEQ_OW=0) |
| 1 | SEQ_EXS_OW | R | X | Sleep Exit sequence data overwritten status: 0 = No data was overwritten 1 = Data was overwritten (if VMON_MISC.EN_SEQ_OW=1), or data could not be written (if VMON_MISC.EN_SEQ_OW=0) |
| 0 | SEQ_ENS_OW | R | X | Sleep Entry sequence data overwritten status: 0 = No data was overwritten 1 = Data was overwritten (if VMON_MISC.EN_SEQ_OW=1), or data could not be written (if VMON_MISC.EN_SEQ_OW=0) |

8.5.1.19 SEQ_ORD_STAT Register (Address = 0x36) [Default = X]

SEQ_ORD_STAT is shown in 表 8-24.

Return to the [Summary Table](#).

Sequencing/ $\overline{\text{SYNC}}$ counter (rail order) register value.

表 8-24. SEQ_ORD_STAT Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-----------------|------|---------|---|
| 7:0 | SYNC_COUNT[7:0] | R | X | This register represents the counter value during a power/sleep sequence. It corresponds to the number of $\overline{\text{SYNC}}$ falling edges detected, and used as tag value for monitored channels. |

8.5.1.20 MON_LVL[1] Register (Address = 0x40) [Default = X]

MON_LVL[1] is shown in 表 8-25.

Return to the [Summary Table](#).

For ADC readout -of each channel - 8bits

表 8-25. MON_LVL[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------|------|---------|---|
| 7:0 | ADC[7:0] | R | X | This register represents the 8-bit voltage level of channel 1. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1LSB=5 mV. With scaling set to 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1LSB=20 mV. |

8.5.1.21 MON_LVL[2] Register (Address = 0x41) [Default = X]

MON_LVL[2] is shown in 表 8-26.

Return to the [Summary Table](#).

For ADC readout -of each channel - 8bits

表 8-26. MON_LVL[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------|------|---------|---|
| 7:0 | ADC[7:0] | R | X | This register represents the 8-bit voltage level of channel 2. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1LSB=5 mV. With scaling set to 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1LSB=20 mV. |

8.5.1.22 MON_LVL[3] Register (Address = 0x42) [Default = X]

MON_LVL[3] is shown in 表 8-27.

Return to the [Summary Table](#).

For ADC readout -of each channel - 8bits

表 8-27. MON_LVL[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------|------|---------|--|
| 7:0 | ADC[7:0] | R | X | This register represents the 8-bit voltage level of channel 3. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1LSB=5 mV. With scaling set to 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1LSB=20 mV. |

8.5.1.23 MON_LVL[4] Register (Address = 0x43) [Default = X]

MON_LVL[4] is shown in 表 8-28.

Return to the [Summary Table](#).

For ADC readout -of each channel - 8bits

表 8-28. MON_LVL[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------|------|---------|--|
| 7:0 | ADC[7:0] | R | X | This register represents the 8-bit voltage level of channel 4. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1LSB=5 mV. With scaling set to 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1LSB=20 mV. |

8.5.1.24 MON_LVL[5] Register (Address = 0x44) [Default = X]

MON_LVL[5] is shown in 表 8-29.

Return to the [Summary Table](#).

For ADC readout -of each channel - 8bits

表 8-29. MON_LVL[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------|------|---------|--|
| 7:0 | ADC[7:0] | R | X | This register represents the 8-bit voltage level of channel 5. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1LSB=5 mV. With scaling set to 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1LSB=20 mV. |

8.5.1.25 MON_LVL[6] Register (Address = 0x45) [Default = X]

MON_LVL[6] is shown in 表 8-30.

Return to the [Summary Table](#).

For ADC readout -of each channel - 8bits

表 8-30. MON_LVL[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------|------|---------|---|
| 7:0 | ADC[7:0] | R | X | This register represents the 8-bit voltage level of channel 6. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1LSB=5 mV. With scaling set to 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1LSB=20 mV. |

8.5.1.26 SEQ_ON_LOG[1] Register (Address = 0x50) [Default = X]

SEQ_ON_LOG[1] is shown in [表 8-31](#).

Return to the [Summary Table](#).

Channel N Power ON sequence order value (ACT/ $\overline{\text{SLEEP}}$ 0 to 1).

表 8-31. SEQ_ON_LOG[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power ON sequence order value for channel 1. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage rising level passes the UV_LF[N] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.27 SEQ_ON_LOG[2] Register (Address = 0x51) [Default = X]

SEQ_ON_LOG[2] is shown in [表 8-32](#).

Return to the [Summary Table](#).

Channel N Power ON sequence order value (ACT/ $\overline{\text{SLEEP}}$ 0 to 1).

表 8-32. SEQ_ON_LOG[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power ON sequence order value for channel 2. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage rising level passes the UV_LF[N] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.28 SEQ_ON_LOG[3] Register (Address = 0x52) [Default = X]

SEQ_ON_LOG[3] is shown in [表 8-33](#).

Return to the [Summary Table](#).

Channel N Power ON sequence order value (ACT/ $\overline{\text{SLEEP}}$ 0 to 1).

表 8-33. SEQ_ON_LOG[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power ON sequence order value for channel 3. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage rising level passes the UV_LF[N] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.29 SEQ_ON_LOG[4] Register (Address = 0x53) [Default = X]

SEQ_ON_LOG[4] is shown in 表 8-34.

Return to the [Summary Table](#).

Channel N Power ON sequence order value (ACT/ $\overline{\text{SLEEP}}$ 0 to 1).

表 8-34. SEQ_ON_LOG[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power ON sequence order value for channel 4. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage rising level passes the UV_LF[N] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.30 SEQ_ON_LOG[5] Register (Address = 0x54) [Default = X]

SEQ_ON_LOG[5] is shown in 表 8-35.

Return to the [Summary Table](#).

Channel N Power ON sequence order value (ACT/ $\overline{\text{SLEEP}}$ 0 to 1).

表 8-35. SEQ_ON_LOG[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power ON sequence order value for channel 5. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage rising level passes the UV_LF[N] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.31 SEQ_ON_LOG[6] Register (Address = 0x55) [Default = X]

SEQ_ON_LOG[6] is shown in 表 8-36.

Return to the [Summary Table](#).

Channel N Power ON sequence order value (ACT/ $\overline{\text{SLEEP}}$ 0 to 1).

表 8-36. SEQ_ON_LOG[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power ON sequence order value for channel 6. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage rising level passes the UV_LF[N] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.32 SEQ_OFF_LOG[1] Register (Address = 0x60) [Default = X]

SEQ_OFF_LOG[1] is shown in 表 8-37.

Return to the [Summary Table](#).

Channel N Power OFF sequence order value (ACT 1 to 0).

表 8-37. SEQ_OFF_LOG[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power OFF sequence order value for channel 1. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.33 SEQ_OFF_LOG[2] Register (Address = 0x61) [Default = X]

SEQ_OFF_LOG[2] is shown in 表 8-38.

Return to the [Summary Table](#).

Channel N Power OFF sequence order value (ACT 1 to 0).

表 8-38. SEQ_OFF_LOG[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power OFF sequence order value for channel 2. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.34 SEQ_OFF_LOG[3] Register (Address = 0x62) [Default = X]

SEQ_OFF_LOG[3] is shown in 表 8-39.

Return to the [Summary Table](#).

Channel N Power OFF sequence order value (ACT 1 to 0).

表 8-39. SEQ_OFF_LOG[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power OFF sequence order value for channel 3. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.35 SEQ_OFF_LOG[4] Register (Address = 0x63) [Default = X]

SEQ_OFF_LOG[4] is shown in 表 8-40.

Return to the [Summary Table](#).

Channel N Power OFF sequence order value (ACT 1 to 0).

表 8-40. SEQ_OFF_LOG[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power OFF sequence order value for channel 4. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.36 SEQ_OFF_LOG[5] Register (Address = 0x64) [Default = X]

SEQ_OFF_LOG[5] is shown in 表 8-41.

Return to the [Summary Table](#).

Channel N Power OFF sequence order value (ACT 1 to 0).

表 8-41. SEQ_OFF_LOG[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power OFF sequence order value for channel 5. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.37 SEQ_OFF_LOG[6] Register (Address = 0x65) [Default = X]

SEQ_OFF_LOG[6] is shown in 表 8-42.

Return to the [Summary Table](#).

Channel N Power OFF sequence order value (ACT 1 to 0).

表 8-42. SEQ_OFF_LOG[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Power OFF sequence order value for channel 6. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.38 SEQ_EXS_LOG[1] Register (Address = 0x70) [Default = X]

SEQ_EXS_LOG[1] is shown in 表 8-43.

Return to the [Summary Table](#).

Channel N Sleep Exit sequence order value ($\overline{\text{SLEEP}}$ 0 to 1).

表 8-43. SEQ_EXS_LOG[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Exit sequence order value for channel 1. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage rising level passes the UV_LF[1] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.39 SEQ_EXS_LOG[2] Register (Address = 0x71) [Default = X]

SEQ_EXS_LOG[2] is shown in 表 8-44.

Return to the [Summary Table](#).

Channel N Sleep Exit sequence order value ($\overline{\text{SLEEP}}$ 0 to 1).

表 8-44. SEQ_EXS_LOG[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Exit sequence order value for channel 2. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage rising level passes the UV_LF[2] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.40 SEQ_EXS_LOG[3] Register (Address = 0x72) [Default = X]

SEQ_EXS_LOG[3] is shown in 表 8-45.

Return to the [Summary Table](#).

Channel N Sleep Exit sequence order value ($\overline{\text{SLEEP}}$ 0 to 1).

表 8-45. SEQ_EXS_LOG[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Exit sequence order value for channel 3. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage rising level passes the UV_LF[3] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.41 SEQ_EXS_LOG[4] Register (Address = 0x73) [Default = X]

SEQ_EXS_LOG[4] is shown in 表 8-46.

Return to the [Summary Table](#).

Channel N Sleep Exit sequence order value ($\overline{\text{SLEEP}}$ 0 to 1).

表 8-46. SEQ_EXS_LOG[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Exit sequence order value for channel 4. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage rising level passes the UV_LF[4] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.42 SEQ_EXS_LOG[5] Register (Address = 0x74) [Default = X]

SEQ_EXS_LOG[5] is shown in 表 8-47.

Return to the [Summary Table](#).

Channel N Sleep Exit sequence order value ($\overline{\text{SLEEP}}$ 0 to 1).

表 8-47. SEQ_EXS_LOG[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Exit sequence order value for channel 5. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage rising level passes the UV_LF[5] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.43 SEQ_EXS_LOG[6] Register (Address = 0x75) [Default = X]

SEQ_EXS_LOG[6] is shown in 表 8-48.

Return to the [Summary Table](#).

Channel N Sleep Exit sequence order value ($\overline{\text{SLEEP}}$ 0 to 1).

表 8-48. SEQ_EXS_LOG[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Exit sequence order value for channel 6. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage rising level passes the UV_LF[6] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.44 SEQ_ENS_LOG[1] Register (Address = 0x80) [Default = X]

SEQ_ENS_LOG[1] is shown in [表 8-49](#).

Return to the [Summary Table](#).

Channel N Sleep Entry sequence order value ($\overline{\text{SLEEP}}$ 1 to 0).

表 8-49. SEQ_ENS_LOG[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Entry sequence order value for channel 1. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.45 SEQ_ENS_LOG[2] Register (Address = 0x81) [Default = X]

SEQ_ENS_LOG[2] is shown in [表 8-50](#).

Return to the [Summary Table](#).

Channel N Sleep Entry sequence order value ($\overline{\text{SLEEP}}$ 1 to 0).

表 8-50. SEQ_ENS_LOG[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Entry sequence order value for channel 2. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.46 SEQ_ENS_LOG[3] Register (Address = 0x82) [Default = X]

SEQ_ENS_LOG[3] is shown in [表 8-51](#).

Return to the [Summary Table](#).

Channel N Sleep Entry sequence order value ($\overline{\text{SLEEP}}$ 1 to 0).

表 8-51. SEQ_ENS_LOG[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Entry sequence order value for channel 3. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.47 SEQ_ENS_LOG[4] Register (Address = 0x83) [Default = X]

SEQ_ENS_LOG[4] is shown in 表 8-52.

Return to the [Summary Table](#).

Channel N Sleep Entry sequence order value ($\overline{\text{SLEEP}}$ 1 to 0).

表 8-52. SEQ_ENS_LOG[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Entry sequence order value for channel 4. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.48 SEQ_ENS_LOG[5] Register (Address = 0x84) [Default = X]

SEQ_ENS_LOG[5] is shown in 表 8-53.

Return to the [Summary Table](#).

Channel N Sleep Entry sequence order value ($\overline{\text{SLEEP}}$ 1 to 0).

表 8-53. SEQ_ENS_LOG[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Entry sequence order value for channel 5. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.49 SEQ_ENS_LOG[6] Register (Address = 0x85) [Default = X]

SEQ_ENS_LOG[6] is shown in 表 8-54.

Return to the [Summary Table](#).

Channel N Sleep Entry sequence order value ($\overline{\text{SLEEP}}$ 1 to 0).

表 8-54. SEQ_ENS_LOG[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R | X | This register stores the Sleep Entry sequence order value for channel 6. The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP. The tag is assigned when the voltage falling level passes the OFF threshold (200 mV). The tag value is the SYNC_ORD_COUNT at the time the threshold is passed. |

8.5.1.50 SEQ_TIME_MSB[1] Register (Address = 0x90) [Default = X]

SEQ_TIME_MSB[1] is shown in [表 8-55](#).

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-55. SEQ_TIME_MSB[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | CLOCK[7:0] | R | X | This register stores the MSB of the sequence timestamp for channel 1. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[1] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50 μ s (equal to tSEQ_LSB). |

8.5.1.51 SEQ_TIME_LSB[1] Register (Address = 0x91) [Default = X]

SEQ_TIME_LSB[1] is shown in [表 8-56](#).

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-56. SEQ_TIME_LSB[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | CLOCK[7:0] | R | X | This register stores the LSB of the sequence timestamp for channel 1. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[1] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50 μ s (equal to tSEQ_LSB). |

8.5.1.52 SEQ_TIME_MSB[2] Register (Address = 0x92) [Default = X]

SEQ_TIME_MSB[2] is shown in [表 8-57](#).

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-57. SEQ_TIME_MSB[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | CLOCK[7:0] | R | X | This register stores the MSB of the sequence timestamp for channel 2. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[2] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50 μ s (equal to tSEQ_LSB). |

8.5.1.53 SEQ_TIME_LSB[2] Register (Address = 0x93) [Default = X]

SEQ_TIME_LSB[2] is shown in 表 8-58.

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-58. SEQ_TIME_LSB[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | CLOCK[7:0] | R | X | This register stores the LSB of the sequence timestamp for channel 2. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[2] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50 μ s (equal to tSEQ_LSB). |

8.5.1.54 SEQ_TIME_MSB[3] Register (Address = 0x94) [Default = X]

SEQ_TIME_MSB[3] is shown in 表 8-59.

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-59. SEQ_TIME_MSB[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | CLOCK[7:0] | R | X | This register stores the MSB of the sequence timestamp for channel 3. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[3] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50 μ s (equal to tSEQ_LSB). |

8.5.1.55 SEQ_TIME_LSB[3] Register (Address = 0x95) [Default = X]

SEQ_TIME_LSB[3] is shown in 表 8-60.

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-60. SEQ_TIME_LSB[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | CLOCK[7:0] | R | X | <p>This register stores the LSB of the sequence timestamp for channel 3.</p> <p>The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.</p> <p>The timestamp is stored when the voltage rising level passes the UV_LF[3] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).</p> <p>The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).</p> <p>The least significant bit corresponds to 50 μs (equal to tSEQ_LSB).</p> |

8.5.1.56 SEQ_TIME_MSB[4] Register (Address = 0x96) [Default = X]

SEQ_TIME_MSB[4] is shown in 表 8-61.

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-61. SEQ_TIME_MSB[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | CLOCK[7:0] | R | X | <p>This register stores the MSB of the sequence timestamp for channel 4.</p> <p>The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.</p> <p>The timestamp is stored when the voltage rising level passes the UV_LF[4] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).</p> <p>The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).</p> <p>The least significant bit corresponds to 50 μs (equal to tSEQ_LSB).</p> |

8.5.1.57 SEQ_TIME_LSB[4] Register (Address = 0x97) [Default = X]

SEQ_TIME_LSB[4] is shown in 表 8-62.

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-62. SEQ_TIME_LSB[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | CLOCK[7:0] | R | X | This register stores the LSB of the sequence timestamp for channel 4. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[4] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50 μ s (equal to tSEQ_LSB). |

8.5.1.58 SEQ_TIME_MSB[5] Register (Address = 0x98) [Default = X]

SEQ_TIME_MSB[5] is shown in 表 8-63.

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-63. SEQ_TIME_MSB[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | CLOCK[7:0] | R | X | This register stores the MSB of the sequence timestamp for channel 5. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[5] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50 μ s (equal to tSEQ_LSB). |

8.5.1.59 SEQ_TIME_LSB[5] Register (Address = 0x99) [Default = X]

SEQ_TIME_LSB[5] is shown in 表 8-64.

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-64. SEQ_TIME_LSB[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | CLOCK[7:0] | R | X | This register stores the LSB of the sequence timestamp for channel 5. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[5] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50 μ s (equal to tSEQ_LSB). |

8.5.1.60 SEQ_TIME_MSB[6] Register (Address = 0x9A) [Default = X]

SEQ_TIME_MSB[6] is shown in 表 8-65.

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-65. SEQ_TIME_MSB[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | CLOCK[7:0] | R | X | <p>This register stores the MSB of the sequence timestamp for channel 6.</p> <p>The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.</p> <p>The timestamp is stored when the voltage rising level passes the UV_LF[6] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).</p> <p>The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).</p> <p>The least significant bit corresponds to 50 μs (equal to tSEQ_LSB).</p> |

8.5.1.61 SEQ_TIME_LSB[6] Register (Address = 0x9B) [Default = X]

SEQ_TIME_LSB[6] is shown in 表 8-66.

Return to the [Summary Table](#).

Channel N Sequence timestamp value MSB and LSB (all sequences).

表 8-66. SEQ_TIME_LSB[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | CLOCK[7:0] | R | X | <p>This register stores the LSB of the sequence timestamp for channel 6.</p> <p>The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.</p> <p>The timestamp is stored when the voltage rising level passes the UV_LF[6] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).</p> <p>The timestamp is stored when the voltage falling level passes the OFF threshold (200 mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).</p> <p>The least significant bit corresponds to 50 μs (equal to tSEQ_LSB).</p> |

8.5.1.62 BANK_SEL Register (Address = 0xF0) [Default = 0x00]

BANK_SEL is shown in 表 8-67.

Return to the [Summary Table](#).

Bank select=0 for Bank 0 and 1 for Bank 1

表 8-67. BANK_SEL Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|---------------------------------|
| 7:2 | RSVD | R/W | 0b | RSVD |
| 1 | BANK_SELECT | R/W | 0b | NA |
| 0 | BANK | R/W | 0b | Register Bank selection number. |

8.5.1.63 PROT1 Register (Address = 0xF1) [Default = 0x00]

PROT1 is shown in 表 8-68.

Return to the [Summary Table](#).

Protection selection registers. In order to write-protect a register group, the host must set the relevant bit in both registers. For security, registers PROT1 and PROT2 need to have POR value = 0x00 and become read-only once set until power cycle. Once set to 1, they cannot be cleared to 0 by the host. They can be cleared (and allow writing different VMON registers configurations) through: A power cycle A reset through VMON_CTL.RESET BIST executed on exiting Sequence 2 (if TEST_CFG.AT_SHDN=1).

表 8-68. PROT1 Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|--|
| 7:6 | RSVD | R/W | 0b | RSVD |
| 5 | WRKC | R/W | 0b | 0b 0 = Control Working (WRKC) registers are writeable. 0b 1 = Writes to control working registers are ignored. |
| 4 | WRKS | R/W | 0b | 0b 0 = Sequence Working (WRKS) registers are writeable. 0b 1 = Writes to sequence working registers are ignored. |
| 3 | CFG | R/W | 0b | 0b 0 = Configuration (CFG) registers are writeable. 0b 1 = Writes to configuration registers are ignored. |
| 2 | IEN | R/W | 0b | 0b 0 = Interrupt Enable (IEN) registers are writeable. 0b 1 = Writes to interrupt enable registers are ignored. |
| 1 | MON | R/W | 0b | 0b 0 = Monitor (MON[N]) registers are writeable. 0b 1 = Writes to monitor registers selected in PROT_MON1 register are ignored. |
| 0 | SEQ | R/W | 0b | 0b 0 = Sequence (SEQ) Registers are writeable. 0b 1 = Writes to sequence registers are ignored. |

8.5.1.64 PROT2 Register (Address = 0xF2) [Default = 0x00]

PROT2 is shown in 表 8-69.

Return to the [Summary Table](#).

Protection selection registers. In order to write-protect a register group, the host must set the relevant bit in both registers. For security, registers PROT1 and PROT2 need to have POR value = 0x00 and become read-only once set until power cycle. Once set to 1, they cannot be cleared to 0 by the host. They can be cleared (and allow writing different VMON registers configurations) through: A power cycle A reset through VMON_CTL.RESET BIST executed on exiting Sequence 2 (if TEST_CFG.AT_SHDN=1).

表 8-69. PROT2 Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|---|
| 7:6 | RSVD | R/W | 0b | RSVD |
| 5 | WRKC | R/W | 0b | 0b 0 = Control Working (WRKC) registers are writeable. 0b 1 = Writes to control working registers are ignored. |

表 8-69. PROT2 Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|--|
| 4 | WRKS | R/W | 0b | 0b 0 = Sequence Working (WRKS) registers are writeable. 0b 1 = Writes to sequence working registers are ignored. |
| 3 | CFG | R/W | 0b | 0b 0 = Configuration (CFG) registers are writeable. 0b 1 = Writes to configuration registers are ignored. |
| 2 | IEN | R/W | 0b | 0b 0 = Interrupt Enable (IEN) registers are writeable. 0b 1 = Writes to interrupt enable registers are ignored. |
| 1 | MON | R/W | 0b | 0b 0 = Monitor (MON[N]) registers are writeable. 0b 1 = Writes to monitor registers selected in PROT_MON1 register are ignored. |
| 0 | SEQ | R/W | 0b | 0b 0 = Sequence (SEQ) Registers are writeable. 0b 1 = Writes to sequence registers are ignored. |

8.5.1.65 PROT_MON2 Register (Address = 0xF3) [Default = 0xC1]

PROT_MON2 is shown in [表 8-70](#).

Return to the [Summary Table](#).

Monitor channels configuration protection.

表 8-70. PROT_MON2 Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R/W | 11b | RSVD |
| 5:0 | MON[N] | R/W | 1b | This register selects the monitor channels configurations that will be protected once PROT1, PROT2 registers are written to protect the MON group. 0 = Monitor configuration registers for channel N are writeable. 1 = Writes to monitor configuration registers for channel N are ignored. |

8.5.1.66 I2CADDR Register (Address = 0xF9) [Default = X]

I2CADDR is shown in [表 8-71](#).

Return to the [Summary Table](#).

3 LSB bits are decided based on resistor value and 5 MSB bits are based on OTP NVM. ADDR_NVM has default value of 30 (Factory default setting)

表 8-71. I2CADDR Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-----------------|------|---------|--|
| 7 | RSVD | R | X | RSVD |
| 6:3 | ADDR_NVM[3:0] | R | X | I2C address four most significant bits. Set in NVM. |
| 2:0 | ADDR_STRAP[2:0] | R | X | I2C address three least significant bits. Set by the strap level detected on ADDR pin, from 000b to 111b. |

8.5.1.67 DEV_CFG Register (Address = 0xFA) [Default = X]

DEV_CFG is shown in 表 8-72.

Return to the [Summary Table](#).

Status of I2C interface voltage levels, 0 for 3.3V I/F and 1 for 1.2/1.8V interface (Factory default setting)

表 8-72. DEV_CFG Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:1 | RSVD | R | X | RSVD |
| 0 | SOC_IF | R | X | Host SoC Interface (includes I2C, ACT, SLEEP, and SYNC). 0 = 3.3 V 1 = 1.2 V/1.8 V |

8.5.2 BANK1 Registers

表 8-73 lists the memory-mapped registers for the BANK1 registers. All register offset addresses not listed in 表 8-73 should be considered as reserved locations and the register contents should not be modified.

表 8-73. BANK1 Registers

| Address | Acronym | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---------|-------------|----------------|-------|-------|---------|-------|-------------|----------------|-------------------|---------------|
| 0x10 | VMON_CTL | DIAG_EN_SCALE | | | SLP_PWR | RSVD | RESET_PROT | SYNC_RST | FORCE_SYNC | FORCE_NIRQ |
| 0x11 | VMON_MISC | RSVD | | | | | EN_TSW | EN_SEQOW | REQ_PEC | EN_PEC |
| 0x12 | TEST_CFG | RSVD | | | | | AT_SHDN | RESERVED | AT_POR | |
| 0x13 | IEN_UVHF | RSVD | | | MON[N] | | | | | |
| 0x14 | IEN_UVLF | RSVD | | | MON[N] | | | | | |
| 0x15 | IEN_OVHF | RSVD | | | MON[N] | | | | | |
| 0x16 | IEN_OVLF | RSVD | | | MON[N] | | | | | |
| 0x17 | IEN_SEQ_ON | RSVD | | | MON[N] | | | | | |
| 0x18 | IEN_SEQ_OFF | RSVD | | | MON[N] | | | | | |
| 0x19 | IEN_SEQ_EXS | RSVD | | | MON[N] | | | | | |
| 0x1A | IEN_SEQ_ENS | RSVD | | | MON[N] | | | | | |
| 0x1B | IEN_CONTROL | RT_CRC Int | | | | | RSVD | TSD Int | SYNC Int | PEC Int |
| 0x1C | IEN_TEST | ECC_SEC | | | | | | RSVD | BIST_Complete_INT | BIST_Fail_INT |
| 0x1E | MON_CH_EN | RSVD | | | MON[N] | | | | | |
| 0x1F | VRANGE_MULT | RSVD | | | MON[N] | | | | | |
| 0x20 | UV_HF[1] | THRESHOLD[7:0] | | | | | | | | |
| 0x21 | OV_HF[1] | THRESHOLD[7:0] | | | | | | | | |
| 0x22 | UV_LF[1] | THRESHOLD[7:0] | | | | | | | | |
| 0x23 | OV_LF[1] | THRESHOLD[7:0] | | | | | | | | |
| 0x24 | FLT_HF[1] | OV_DEB[3:0] | | | | | UV_DEB[3:0] | | | |
| 0x25 | FC_LF[1] | RSVD | | | | | | THRESHOLD[2:0] | | |
| 0x30 | UV_HF[2] | THRESHOLD[7:0] | | | | | | | | |
| 0x31 | OV_HF[2] | THRESHOLD[7:0] | | | | | | | | |
| 0x32 | UV_LF[2] | THRESHOLD[7:0] | | | | | | | | |
| 0x33 | OV_LF[2] | THRESHOLD[7:0] | | | | | | | | |
| 0x34 | FLT_HF[2] | OV_DEB[3:0] | | | | | UV_DEB[3:0] | | | |
| 0x35 | FC_LF[2] | RSVD | | | | | | THRESHOLD[2:0] | | |
| 0x40 | UV_HF[3] | THRESHOLD[7:0] | | | | | | | | |
| 0x41 | OV_HF[3] | THRESHOLD[7:0] | | | | | | | | |
| 0x42 | UV_LF[3] | THRESHOLD[7:0] | | | | | | | | |
| 0x43 | OV_LF[3] | THRESHOLD[7:0] | | | | | | | | |
| 0x44 | FLT_HF[3] | OV_DEB[3:0] | | | | | UV_DEB[3:0] | | | |
| 0x45 | FC_LF[3] | RSVD | | | | | | THRESHOLD[2:0] | | |
| 0x50 | UV_HF[4] | THRESHOLD[7:0] | | | | | | | | |
| 0x51 | OV_HF[4] | THRESHOLD[7:0] | | | | | | | | |
| 0x52 | UV_LF[4] | THRESHOLD[7:0] | | | | | | | | |
| 0x53 | OV_LF[4] | THRESHOLD[7:0] | | | | | | | | |
| 0x54 | FLT_HF[4] | OV_DEB[3:0] | | | | | UV_DEB[3:0] | | | |

表 8-73. BANK1 Registers (continued)

| Address | Acronym | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|------------------|----------|--------|--------|----------------|-----------------|-----------------|-----------------|
| 0x55 | FC_LF[4] | RSVD | | | | | THRESHOLD[2:0] | | |
| 0x60 | UV_HF[5] | THRESHOLD[7:0] | | | | | | | |
| 0x61 | OV_HF[5] | THRESHOLD[7:0] | | | | | | | |
| 0x62 | UV_LF[5] | THRESHOLD[7:0] | | | | | | | |
| 0x63 | OV_LF[5] | THRESHOLD[7:0] | | | | | | | |
| 0x64 | FLT_HF[5] | OV_DEB[3:0] | | | | UV_DEB[3:0] | | | |
| 0x65 | FC_LF[5] | RSVD | | | | | THRESHOLD[2:0] | | |
| 0x70 | UV_HF[6] | THRESHOLD[7:0] | | | | | | | |
| 0x71 | OV_HF[6] | THRESHOLD[7:0] | | | | | | | |
| 0x72 | UV_LF[6] | THRESHOLD[7:0] | | | | | | | |
| 0x73 | OV_LF[6] | THRESHOLD[7:0] | | | | | | | |
| 0x74 | FLT_HF[6] | OV_DEB[3:0] | | | | UV_DEB[3:0] | | | |
| 0x75 | FC_LF[6] | RSVD | | | | | THRESHOLD[2:0] | | |
| 0x9F | TI_CONTROL | ENTER_B IST | RSVD | | | | | | |
| 0xA0 | SEQ_REC_CTL | REC_STA RT | SEQ[1:0] | | TS_ACK | SEQ_ON _ACK | SEQ_OF F_ACK | SEQ_EX S_ACK | SEQ_EN S_ACK |
| 0xA1 | AMSK_ON | RSVD | | MON[N] | | | | | |
| 0xA2 | AMSK_OFF | RSVD | | MON[N] | | | | | |
| 0xA3 | AMSK_EXS | RSVD | | MON[N] | | | | | |
| 0xA4 | AMSK_ENS | RSVD | | MON[N] | | | | | |
| 0xA5 | SEQ_TOUT_MSB | MILLISEC[7:0] | | | | | | | |
| 0xA6 | SEQ_TOUT_LSB | MILLISEC[7:0] | | | | | | | |
| 0xA7 | SEQ_SYNC | PULSE_WIDTH[7:0] | | | | | | | |
| 0xA8 | SEQ_UP_THLD | RSVD | | MON[N] | | | | | |
| 0xA9 | SEQ_DN_THLD | RSVD | | MON[N] | | | | | |
| 0xB0 | SEQ_ON_EXP[1] | ORDER[7:0] | | | | | | | |
| 0xB1 | SEQ_ON_EXP[2] | ORDER[7:0] | | | | | | | |
| 0xB2 | SEQ_ON_EXP[3] | ORDER[7:0] | | | | | | | |
| 0xB3 | SEQ_ON_EXP[4] | ORDER[7:0] | | | | | | | |
| 0xB4 | SEQ_ON_EXP[5] | ORDER[7:0] | | | | | | | |
| 0xB5 | SEQ_ON_EXP[6] | ORDER[7:0] | | | | | | | |
| 0xC0 | SEQ_OFF_EXP[1] | ORDER[7:0] | | | | | | | |
| 0xC1 | SEQ_OFF_EXP[2] | ORDER[7:0] | | | | | | | |
| 0xC2 | SEQ_OFF_EXP[3] | ORDER[7:0] | | | | | | | |
| 0xC3 | SEQ_OFF_EXP[4] | ORDER[7:0] | | | | | | | |
| 0xC4 | SEQ_OFF_EXP[5] | ORDER[7:0] | | | | | | | |
| 0xC5 | SEQ_OFF_EXP[6] | ORDER[7:0] | | | | | | | |
| 0xD0 | SEQ_EXS_EXP[1] | ORDER[7:0] | | | | | | | |
| 0xD1 | SEQ_EXS_EXP[2] | ORDER[7:0] | | | | | | | |
| 0xD2 | SEQ_EXS_EXP[3] | ORDER[7:0] | | | | | | | |
| 0xD3 | SEQ_EXS_EXP[4] | ORDER[7:0] | | | | | | | |
| 0xD4 | SEQ_EXS_EXP[5] | ORDER[7:0] | | | | | | | |
| 0xD5 | SEQ_EXS_EXP[6] | ORDER[7:0] | | | | | | | |
| 0xE0 | SEQ_ENS_EXP[1] | ORDER[7:0] | | | | | | | |
| 0xE1 | SEQ_ENS_EXP[2] | ORDER[7:0] | | | | | | | |

表 8-73. BANK1 Registers (continued)

| Address | Acronym | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------------------------|-------|-------|-------|-------|-------|-------|-------|------------|
| 0xE2 | SEQ_ENS_EXP[3] | | | | | | | | ORDER[7:0] |
| 0xE3 | SEQ_ENS_EXP[4] | | | | | | | | ORDER[7:0] |
| 0xE4 | SEQ_ENS_EXP[5] | | | | | | | | ORDER[7:0] |
| 0xE5 | SEQ_ENS_EXP[6] | | | | | | | | ORDER[7:0] |

Complex bit access types are encoded to fit into small table cells. 表 8-74 shows the codes that are used for access types in this section.

表 8-74. BANK1 Access Type Codes

| Access Type | Code | Description |
|-------------------------------|------|--|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| Reset or Default Value | | |
| -n | | Value after reset or the default value |

8.5.2.1 VMON_CTL Register (Address = 0x10) [Default = X]

VMON_CTL is shown in 表 8-75.

Return to the [Summary Table](#).

Voltage Monitor device control register.

表 8-75. VMON_CTL Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|---------------|------|---------|---|
| 7:6 | DIAG_EN_SCALE | R/W | 0b | Diag EN Scale 00 = No force on GAINSEL of SVS COMPs 01 = Forced to 1x 10 = Forced to 2x 11 = Forced to 4x |
| 5 | SLP_PWR | R/W | 0b | Sleep Power Bit 0 = Sleep low power mode 1 = Sleep high power mode |
| 4 | RSVD | R/W | X | RSVD |
| 3 | RESET_PROT | R/W | 0b | Reset 0 = Always reads 0 1 = Full device Reset |
| 2 | SYNC_RST | R/W | 0b | SYNC counter reset (SEQ_ORD_STAT.SYNC_COUNT). 0 = Always reads 0 1 = Reset SYNC counter |
| 1 | FORCE_SYNC | R/W | 0b | Force SYNC assertion 0 = SYNC pin is de-asserted and controlled by the sequence monitoring logic. 1 = SYNC pin is asserted (forced low) |
| 0 | FORCE_NIRQ | R/W | 0b | Force NIRQ assertion 0 = NIRQ pin is de-asserted and controlled by interrupt registers faults 1 = NIRQ pin is asserted (forced low) |

8.5.2.2 VMON_MISC Register (Address = 0x11) [Default = X]

VMON_MISC is shown in 表 8-76.

Return to the [Summary Table](#).

Miscellaneous voltage monitoring configurations.

表 8-76. VMON_MISC Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-----------|------|---------|---|
| 7:4 | RSVD | R/W | X | RSVD |
| 3 | EN_TS_OW | R/W | 1b | Allow Timestamp recording overwrite 0 = Disabled. If sequence timestamp data is available in the SEQ_TIME_xSB[N] registers and the SEQ_REC_STAT.TS_RDY bit is set (data not read yet), a new sequence will not overwrite the existing data. 1 = Enabled (default). Sequence timestamp data is overwritten with a new sequence, irrelevant of the SEQ_REC_STAT.TS_RDY bit. |
| 2 | EN_SEQ_OW | R/W | 1b | Allow Sequence Order recording overwrite 0 = Disabled. If sequence order data is available in the SEQ_ON_LOG[N], SEQ_OFF_LOG[N], SEQ_EXS_LOG[N], or SEQ_ENS_LOG[N] registers, and the respective SEQ_REC_STAT.SEQ_ON_RDY, SEQ_REC_STAT.SEQ_OFF_RDY, SEQ_REC_STAT.SEQ_EXS_RDY, or SEQ_REC_STAT.SEQ_ENS_RDY bit is set (data not read yet), a new sequence will not overwrite the existing data. 1 = Enabled (default). Sequence order data is overwritten with a new sequence, regardless of the SEQ_REC_STAT.SEQ_ON_RDY, SEQ_REC_STAT.SEQ_OFF_RDY, SEQ_REC_STAT.SEQ_EXS_RDY, or SEQ_REC_STAT.SEQ_ENS_RDY bit. |
| 1 | REQ_PEC | R/W | 0b | Require PEC byte (valid only if EN_PEC is 1): 0 = missing PEC byte is treated as good PEC 1 = missing PEC byte is treated as bad PEC, triggering a fault |
| 0 | EN_PEC | R/W | 0b | PEC: 0 = PEC disabled (default) 1 = PEC enabled |

8.5.2.3 TEST_CFG Register (Address = 0x12) [Default = X]

TEST_CFG is shown in 表 8-77.

Return to the [Summary Table](#).

Built-In Self Test BIST execution configuration.

表 8-77. TEST_CFG Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------|------|---------|---|
| 7:4 | RSVD | R/W | X | RSVD |
| 3 | AT_SHDN | R/W | X | Run BIST when exiting ACTIVE state due to ACT transitioning 1 to 0. Device ready after tCFG_WB. This bit cannot be set in OTP/NVM. Always defaults to 0 when loading configuration from OTP/NVM. |
| 2 | RESERVED | R | X | |

表 8-77. TEST_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 1:0 | AT_POR | R/W | X | Run BIST at POR. Device ready after tCFG_WB. 00b = Valid OTP configuration, skip BIST at POR 01b = Corrupt OTP configuration, run BIST at POR 10b = Corrupt OTP configuration, run BIST at POR 11b = Valid OTP configuration, run BIST at POR |

8.5.2.4 IEN_UVHF Register (Address = 0x13) [Default = X]

IEN_UVHF is shown in 表 8-78.

Return to the [Summary Table](#).

High Frequency channel Undervoltage Interrupt Enable register.

表 8-78. IEN_UVHF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 0b | Undervoltage High Frequency fault Interrupt Enable for VIN channel N (1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled |

8.5.2.5 IEN_UVLF Register (Address = 0x14) [Default = X]

IEN_UVLF is shown in 表 8-79.

Return to the [Summary Table](#).

Low Frequency channel Undervoltage Interrupt Enable register.

表 8-79. IEN_UVLF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|---|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 0b | Undervoltage Low Frequency fault Interrupt Enable for VIN channel N (1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled |

8.5.2.6 IEN_OVHF Register (Address = 0x15) [Default = X]

IEN_OVHF is shown in 表 8-80.

Return to the [Summary Table](#).

High Frequency channel Overvoltage Interrupt Enable register.

表 8-80. IEN_OVHF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|---|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 0b | Overvoltage High Frequency fault Interrupt Enable for VIN channel N (1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled |

8.5.2.7 IEN_OVLF Register (Address = 0x16) [Default = X]

IEN_OVLF is shown in 表 8-81.

Return to the [Summary Table](#).

Low Frequency channel Overvoltage Interrupt Enable register.

表 8-81. IEN_OVLF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 0b | Overvoltage Low Frequency fault Interrupt Enable for VIN channel N (1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled |

8.5.2.8 IEN_SEQ_ON Register (Address = 0x17) [Default = X]

IEN_SEQ_ON is shown in 表 8-82.

Return to the [Summary Table](#).

Power ON Sequence ACT transition 0 to 1 Interrupt Enable register.

表 8-82. IEN_SEQ_ON Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 0b | Power ON Sequence Fault Interrupt Enable for VIN channel N (1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled |

8.5.2.9 IEN_SEQ_OFF Register (Address = 0x18) [Default = X]

IEN_SEQ_OFF is shown in 表 8-83.

Return to the [Summary Table](#).

Power OFF Sequence ACT transition 1 to 0 Interrupt Enable register.

表 8-83. IEN_SEQ_OFF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|---|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 0b | Power OFF Sequence Fault Interrupt Enable for VIN channel N (1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled |

8.5.2.10 IEN_SEQ_EXS Register (Address = 0x19) [Default = X]

IEN_SEQ_EXS is shown in 表 8-84.

Return to the [Summary Table](#).

Exit Sleep Sequence $\overline{\text{SLEEP}}$ transition 0 to 1 Interrupt Enable register.

表 8-84. IEN_SEQ_EXS Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7:6 | RSVD | R/W | X | RSVD |

表 8-84. IEN_SEQ_EXS Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 5:0 | MON[N] | R/W | 0b | Exit Sleep Sequence Fault Interrupt Enable for VIN channel N (1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled |

8.5.2.11 IEN_SEQ_ENS Register (Address = 0x1A) [Default = X]

IEN_SEQ_ENS is shown in 表 8-85.

Return to the [Summary Table](#).

Entry Sleep Sequence **SLEEP** transition 1 to 0 Interrupt Enable register.

表 8-85. IEN_SEQ_ENS Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|---|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 0b | Entry Sleep Sequence Fault Interrupt Enable for VIN channel N (1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled |

8.5.2.12 IEN_CONTROL Register (Address = 0x1B) [Default = X]

IEN_CONTROL is shown in 表 8-86.

Return to the [Summary Table](#).

Control and Communication Fault Interrupt Enable register.

表 8-86. IEN_CONTROL Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:5 | RSVD | R/W | X | RSVD |
| 4 | RT_CRC Int | R/W | 0b | Runtime register Cyclic Redundancy Check (CRC) fault interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled |
| 3 | RSVD | R/W | X | RSVD |
| 2 | TSD Int | R/W | 0b | Thermal Shutdown fault interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled |
| 1 | SYNC Int | R/W | 0b | SYNC pin fault (short to supply or ground detected on SYNC pin) interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled |
| 0 | PEC Int | R/W | 0b | PEC fault (mismatch) interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled |

8.5.2.13 IEN_TEST Register (Address = 0x1C) [Default = X]

IEN_TEST is shown in 表 8-87.

Return to the [Summary Table](#).

Internal Test and Configuration Load Fault Interrupt Enable register.

表 8-87. IEN_TEST Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------------------|------|---------|---|
| 7:4 | RSVD | R/W | X | RSVD |
| 3 | ECC_SEC | R/W | 0b | ECC single-error correction fault (on OTP load) interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled |
| 2 | RSVD | R/W | X | RSVD |
| 1 | BIST_Complete_INT | R/W | 0b | Built-In Self-Test complete interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled |
| 0 | BIST_Fail_INT | R/W | 0b | Built-In Self-Test fault interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled Although expected to be always enabled, it is desirable to have the option to disable it. |

8.5.2.14 MON_CH_EN Register (Address = 0x1E) [Default = X]

MON_CH_EN is shown in [表 8-88](#).

Return to the [Summary Table](#).

Channel 1-6 Voltage Monitoring Enable register.

表 8-88. MON_CH_EN Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|---|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 0b | Voltage Monitoring Enable for VIN channel N (1 through 6). 0 = Channel Monitor disabled 1 = Channel Monitor enabled |

8.5.2.15 VRANGE_MULT Register (Address = 0x1F) [Default = X]

VRANGE_MULT is shown in [表 8-89](#).

Return to the [Summary Table](#).

Channel 1-6 Voltage Monitoring Range/Scaling register.

表 8-89. VRANGE_MULT Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 0b | Voltage Monitoring Range/Scaling for VIN channel N (1 through 6). 0 = 1x scaling (0.2 V to 1.475 V with 5 mV steps) 1 = 4x scaling (0.8 V to 5.9 V with 20 mV steps) |

8.5.2.16 UV_HF[1] Register (Address = 0x20) [Default = 0x00]

UV_HF[1] is shown in [表 8-90](#).

Return to the [Summary Table](#).

Channel 1 High Frequency channel Undervoltage threshold.

表 8-90. UV_HF[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.17 OV_HF[1] Register (Address = 0x21) [Default = 0xFF]

OV_HF[1] is shown in 表 8-91.

Return to the [Summary Table](#).

Channel 1 High Frequency channel Overvoltage threshold.

表 8-91. OV_HF[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.18 UV_LF[1] Register (Address = 0x22) [Default = 0x00]

UV_LF[1] is shown in 表 8-92.

Return to the [Summary Table](#).

Channel 1 Low Frequency channel Undervoltage threshold.

表 8-92. UV_LF[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.19 OV_LF[1] Register (Address = 0x23) [Default = 0xFF]

OV_LF[1] is shown in 表 8-93.

Return to the [Summary Table](#).

Channel 1 Low Frequency channel Overvoltage threshold.

表 8-93. OV_LF[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|-----------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 11111111b | Overvoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.20 FLT_HF[1] Register (Address = 0x24) [Default = 0x00]

FLT_HF[1] is shown in 表 8-94.

Return to the [Summary Table](#).

Channel 1 debounce filter for High Frequency Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

表 8-94. FLT_HF[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|--|
| 7:4 | OV_DEB[3:0] | R/W | 0b | Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |
| 3:0 | UV_DEB[3:0] | R/W | 0b | Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |

8.5.2.21 FC_LF[1] Register (Address = 0x25) [Default = X]

FC_LF[1] is shown in 表 8-95.

Return to the [Summary Table](#).

Channel 1 Low Frequency Path Cutoff Frequency 3 dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies.

表 8-95. FC_LF[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7:3 | RSVD | R/W | X | RSVD |

表 8-95. FC_LF[1] Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|---|
| 2:0 | THRESHOLD[2:0] | R/W | 100b | Low frequency cutoff. 000b = Invalid 001b = Invalid 010b = 250 Hz 011b = 500 Hz 100b = 1 kHz (default) 101b = 2 kHz 110b = 4 kHz 111b = Invalid |

8.5.2.22 UV_HF[2] Register (Address = 0x30) [Default = 0x00]

UV_HF[2] is shown in [表 8-96](#).

Return to the [Summary Table](#).

Channel 2 High Frequency channel Undervoltage threshold.

表 8-96. UV_HF[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.23 OV_HF[2] Register (Address = 0x31) [Default = 0xFF]

OV_HF[2] is shown in [表 8-97](#).

Return to the [Summary Table](#).

Channel 2 High Frequency channel Overvoltage threshold.

表 8-97. OV_HF[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.24 UV_LF[2] Register (Address = 0x32) [Default = 0x00]

UV_LF[2] is shown in [表 8-98](#).

Return to the [Summary Table](#).

Channel 2 Low Frequency channel Undervoltage threshold.

表 8-98. UV_LF[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.25 OV_LF[2] Register (Address = 0x33) [Default = 0xFF]

OV_LF[2] is shown in 表 8-99.

Return to the [Summary Table](#).

Channel 2 Low Frequency channel Overvoltage threshold.

表 8-99. OV_LF[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.26 FLT_HF[2] Register (Address = 0x34) [Default = 0x00]

FLT_HF[2] is shown in 表 8-100.

Return to the [Summary Table](#).

Channel 2 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

表 8-100. FLT_HF[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|---|
| 7:4 | OV_DEB[3:0] | R/W | 0b | Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |

表 8-100. FLT_HF[2] Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|--|
| 3:0 | UV_DEB[3:0] | R/W | 0b | Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |

8.5.2.27 FC_LF[2] Register (Address = 0x35) [Default = X]

FC_LF[2] is shown in 表 8-101.

Return to the [Summary Table](#).

Channel 2 Low Frequency Path Cutoff Frequency 3 dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies.

表 8-101. FC_LF[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:3 | RSVD | R/W | X | RSVD |
| 2:0 | THRESHOLD[2:0] | R/W | 100b | 000b = Invalid 001b = Invalid 010b = 250 Hz 011b = 500 Hz 100b = 1 kHz (default) 101b = 2 kHz 110b = 4 kHz 111b = Invalid |

8.5.2.28 UV_HF[3] Register (Address = 0x40) [Default = 0x00]

UV_HF[3] is shown in 表 8-102.

Return to the [Summary Table](#).

Channel 3 High Frequency channel Undervoltage threshold.

表 8-102. UV_HF[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.29 OV_HF[3] Register (Address = 0x41) [Default = 0xFF]

OV_HF[3] is shown in 表 8-103.

Return to the [Summary Table](#).

Channel 3 High Frequency channel Overvoltage threshold.

表 8-103. OV_HF[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.30 UV_LF[3] Register (Address = 0x42) [Default = 0x00]

UV_LF[3] is shown in 表 8-104.

Return to the [Summary Table](#).

Channel 3 Low Frequency channel Undervoltage threshold.

表 8-104. UV_LF[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.31 OV_LF[3] Register (Address = 0x43) [Default = 0xFF]

OV_LF[3] is shown in 表 8-105.

Return to the [Summary Table](#).

Channel 3 Low Frequency channel Overvoltage threshold.

表 8-105. OV_LF[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.32 FLT_HF[3] Register (Address = 0x44) [Default = 0x00]

FLT_HF[3] is shown in 表 8-106.

Return to the [Summary Table](#).

Channel 3 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

表 8-106. FLT_HF[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|---|
| 7:4 | OV_DEB[3:0] | R/W | 0b | Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |
| 3:0 | UV_DEB[3:0] | R/W | 0b | Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |

8.5.2.33 FC_LF[3] Register (Address = 0x45) [Default = X]

FC_LF[3] is shown in 表 8-107.

Return to the [Summary Table](#).

Channel 3 Low Frequency Path Cutoff Frequency 3 dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies.

表 8-107. FC_LF[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:3 | RSVD | R/W | X | RSVD |
| 2:0 | THRESHOLD[2:0] | R/W | 100b | 000b = Invalid 001b = Invalid 010b = 250 Hz 011b = 500 Hz 100b = 1 kHz (default) 101b = 2 kHz 110b = 4 kHz 111b = Invalid |

8.5.2.34 UV_HF[4] Register (Address = 0x50) [Default = 0x00]

UV_HF[4] is shown in 表 8-108.

Return to the [Summary Table](#).

Channel 4 High Frequency channel Undervoltage threshold.

表 8-108. UV_HF[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.35 OV_HF[4] Register (Address = 0x51) [Default = 0xFF]

OV_HF[4] is shown in 表 8-109.

Return to the [Summary Table](#).

Channel 4 High Frequency channel Overvoltage threshold.

表 8-109. OV_HF[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.36 UV_LF[4] Register (Address = 0x52) [Default = 0x00]

UV_LF[4] is shown in 表 8-110.

Return to the [Summary Table](#).

Channel 4 Low Frequency channel Undervoltage threshold.

表 8-110. UV_LF[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.37 OV_LF[4] Register (Address = 0x53) [Default = 0xFF]

OV_LF[4] is shown in 表 8-111.

Return to the [Summary Table](#).

Channel 4 Low Frequency channel Overvoltage threshold.

表 8-111. OV_LF[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.38 FLT_HF[4] Register (Address = 0x54) [Default = 0x00]

FLT_HF[4] is shown in 表 8-112.

Return to the [Summary Table](#).

Channel 4 debounce filter for HF Fault. The smallest value supported is 0.4 μ s, The largest is 102.4 μ s.

表 8-112. FLT_HF[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|--|
| 7:4 | OV_DEB[3:0] | R/W | 0b | Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |
| 3:0 | UV_DEB[3:0] | R/W | 0b | Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |

8.5.2.39 FC_LF[4] Register (Address = 0x55) [Default = X]

FC_LF[4] is shown in [表 8-113](#).

Return to the [Summary Table](#).

Channel 4 Low Frequency Path Cutoff Frequency 3 dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies.

表 8-113. FC_LF[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:3 | RSVD | R/W | X | RSVD |
| 2:0 | THRESHOLD[2:0] | R/W | 100b | 000b = Invalid 001b = Invalid 010b = 250 Hz 011b = 500 Hz 100b = 1 kHz (default) 101b = 2 kHz 110b = 4 kHz 111b = Invalid |

8.5.2.40 UV_HF[5] Register (Address = 0x60) [Default = 0x00]

UV_HF[5] is shown in [表 8-114](#).

Return to the [Summary Table](#).

Channel 5 High Frequency channel Undervoltage threshold.

表 8-114. UV_HF[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.41 OV_HF[5] Register (Address = 0x61) [Default = 0xFF]

OV_HF[5] is shown in 表 8-115.

Return to the [Summary Table](#).

Channel 5 High Frequency channel Overvoltage threshold.

表 8-115. OV_HF[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.42 UV_LF[5] Register (Address = 0x62) [Default = 0x00]

UV_LF[5] is shown in 表 8-116.

Return to the [Summary Table](#).

Channel 5 Low Frequency channel Undervoltage threshold.

表 8-116. UV_LF[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.43 OV_LF[5] Register (Address = 0x63) [Default = 0xFF]

OV_LF[5] is shown in 表 8-117.

Return to the [Summary Table](#).

Channel 5 Low Frequency channel Overvoltage threshold.

表 8-117. OV_LF[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.44 FLT_HF[5] Register (Address = 0x64) [Default = 0x00]

FLT_HF[5] is shown in 表 8-118.

Return to the [Summary Table](#).

Channel 5 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

表 8-118. FLT_HF[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|---|
| 7:4 | OV_DEB[3:0] | R/W | 0b | Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |
| 3:0 | UV_DEB[3:0] | R/W | 0b | Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |

8.5.2.45 FC_LF[5] Register (Address = 0x65) [Default = X]

FC_LF[5] is shown in 表 8-119.

Return to the [Summary Table](#).

Channel 5 Low Frequency Path Cutoff Frequency 3 dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies.

表 8-119. FC_LF[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:3 | RSVD | R/W | X | RSVD |
| 2:0 | THRESHOLD[2:0] | R/W | 100b | 000b = Invalid 001b = Invalid 010b = 250 Hz 011b = 500 Hz 100b = 1 kHz (default) 101b = 2 kHz 110b = 4 kHz 111b = Invalid |

8.5.2.46 UV_HF[6] Register (Address = 0x70) [Default = 0x00]

UV_HF[6] is shown in 表 8-120.

Return to the [Summary Table](#).

Channel 6 High Frequency channel Undervoltage threshold.

表 8-120. UV_HF[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.47 OV_HF[6] Register (Address = 0x71) [Default = 0xFF]

OV_HF[6] is shown in 表 8-121.

Return to the [Summary Table](#).

Channel 6 High Frequency channel Overvoltage threshold.

表 8-121. OV_HF[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|-----------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 11111111b | Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.48 UV_LF[6] Register (Address = 0x72) [Default = 0x00]

UV_LF[6] is shown in 表 8-122.

Return to the [Summary Table](#).

Channel 6 Low Frequency channel Undervoltage threshold.

表 8-122. UV_LF[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|---|
| 7:0 | THRESHOLD[7:0] | R/W | 0b | Undervoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.49 OV_LF[6] Register (Address = 0x73) [Default = 0xFF]

OV_LF[6] is shown in 表 8-123.

Return to the [Summary Table](#).

Channel 6 Low Frequency channel Overvoltage threshold.

表 8-123. OV_LF[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|----------------|------|----------|--|
| 7:0 | THRESHOLD[7:0] | R/W | 1111111b | Overvoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 V to 5.9 V with 1 LSB = 20 mV. |

8.5.2.50 FLT_HF[6] Register (Address = 0x74) [Default = 0x00]

FLT_HF[6] is shown in [表 8-124](#).

Return to the [Summary Table](#).

Channel 6 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

表 8-124. FLT_HF[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|---|
| 7:4 | OV_DEB[3:0] | R/W | 0b | Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |
| 3:0 | UV_DEB[3:0] | R/W | 0b | Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1 μ s 1000b = 25.6 μ s 0001b = 0.2 μ s 1001b = 51.2 μ s 0010b = 0.4 μ s 1010b = 102.4 μ s 0011b = 0.8 μ s 1011b = 102.4 μ s 0100b = 1.6 μ s 1100b = 102.4 μ s 0101b = 3.2 μ s 1101b = 102.4 μ s 0110b = 6.4 μ s 1110b = 102.4 μ s 0111b = 12.8 μ s 1111b = 102.4 μ s |

8.5.2.51 FC_LF[6] Register (Address = 0x75) [Default = X]

FC_LF[6] is shown in [表 8-125](#).

Return to the [Summary Table](#).

Channel 6 Low Frequency Path Cutoff Frequency 3 dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies.

表 8-125. FC_LF[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7:3 | RSVD | R/W | X | RSVD |

表 8-125. FC_LF[6] Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|----------------|------|---------|--|
| 2:0 | THRESHOLD[2:0] | R/W | 100b | 000b = Invalid 001b = Invalid 010b = 250 Hz 011b = 500 Hz 100b = 1 kHz (default) 101b = 2 kHz 110b = 4 kHz 111b = Invalid |

8.5.2.52 TI_CONTROL Register (Address = 0x9F) [Default = X]

TI_CONTROL is shown in [表 8-126](#).

Return to the [Summary Table](#).

Manual BIST entry register.

表 8-126. TI_CONTROL Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7 | ENTER_BIST | R/W | X | Enter BIST: 0 = Default 1 = Enter BIST |
| 6:0 | RSVD | R/W | X | RSVD |

8.5.2.53 SEQ_REC_CTL Register (Address = 0xA0) [Default = 0x00]

SEQ_REC_CTL is shown in [表 8-127](#).

Return to the [Summary Table](#).

Sequence control register.

表 8-127. SEQ_REC_CTL Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7 | REC_START | R/W | 0b | Software start sequence logging (recording): 0 = Always read 0 1 = Initiate power sequence (selected by SEQ[1:0]) recording. |
| 6:5 | SEQ[1:0] | R/W | 0b | Sequence to record (and compare for faults to corresponding expected sequence order registers): 00b = Power ON (same as ACT 0 to 1) 01b = Power OFF (ACT 1 to 0) 10b = Sleep Exit (SLEEP 0 to 1) 11b = Sleep Entry (SLEEP 1 to 0) |
| 4 | TS_ACK | R/W | 0b | Timestamp data OK to overwrite. Valid and used only if VMON_MISC.EN_TS_OW=0. 00b = Always read 0 01b = Acknowledge Timestamp data and OK to overwrite. SEQ_REC_STAT.TS_RDY and SEQ_OW_STAT.TS_OW are cleared. |
| 3 | SEQ_ON_ACK | R/W | 0b | Power ON sequence data OK to overwrite. Valid and used only if VMON_MISC.EN_SEQ_OW=0. 00b = Always read 0 01b = Acknowledge Power ON sequence data and OK to overwrite. SEQ_REC_STAT.SEQ_ON_RDY and SEQ_OW_STAT.SEQ_ON_OW are cleared. |

表 8-127. SEQ_REC_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Default | Description |
|-----|-------------|------|---------|---|
| 2 | SEQ_OFF_ACK | R/W | 0b | Power OFF sequence data OK to overwrite. Valid and used only if VMON_MISC.EN_SEQ_OW=0. 00b = Always read 0 01b = Acknowledge Power OFF sequence data and OK to overwrite. SEQ_REC_STAT.SEQ_OFF_RDY and SEQ_OW_STAT.SEQ_OFF_OW are cleared. |
| 1 | SEQ_EXS_ACK | R/W | 0b | Sleep Exit sequence data OK to overwrite. Valid and used only if VMON_MISC.EN_SEQ_OW=0. 00b = Always read 0 01b = Acknowledge Sleep Exit sequence data and OK to overwrite. SEQ_REC_STAT.SEQ_EXS_RDY and SEQ_OW_STAT.SEQ_EXS_OW are cleared. |
| 0 | SEQ_ENS_ACK | R/W | 0b | Sleep Entry sequence data OK to overwrite. Valid and used only if VMON_MISC.EN_SEQ_OW=0. 00b = Always read 0 01b = Acknowledge Sleep Entry sequence data and OK to overwrite. SEQ_REC_STAT.SEQ_ENS_RDY and SEQ_OW_STAT.SEQ_ENS_OW are cleared. |

8.5.2.54 AMSK_ON Register (Address = 0xA1) [Default = X]

AMSK_ON is shown in [表 8-128](#).

Return to the [Summary Table](#).

Auto-mask ON register. This register is used to mask UVLF, UVHF, and OVHF interrupts on ACT transition 0 to 1 transitions.

表 8-128. AMSK_ON Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 11111b | Auto-mask on ACT 0 to 1 transition for IEN_UVLF, IEN_UVHF, and IEN_OVHF for VIN channel N (1 through 6). 00b = Channel interrupts not auto-masked 01b = Channel interrupts auto-masked |

8.5.2.55 AMSK_OFF Register (Address = 0xA2) [Default = X]

AMSK_OFF is shown in [表 8-129](#).

Return to the [Summary Table](#).

Auto-mask OFF register. This register is used to mask UVLF, UVHF, and OVHF interrupts on ACT transition 1 to 0 transitions.

表 8-129. AMSK_OFF Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 11111b | Auto-mask on ACT 1 to 0 transition for IEN_UVLF, IEN_UVHF, and IEN_OVHF for VIN channel N (1 through 6). 00b = Channel interrupts not auto-masked 01b = Channel interrupts auto-masked |

8.5.2.56 AMSK_EXS Register (Address = 0xA3) [Default = X]

AMSK_EXS is shown in [表 8-130](#).

Return to the [Summary Table](#).

Auto-mask EXIT register. This register is used to mask UVLF, UVHF, and OVHF interrupts on $\overline{\text{SLEEP}}$ transition 0 to 1 transitions.

表 8-130. AMSK_EXS Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 111111b | Auto-mask on $\overline{\text{SLEEP}}$ 0 to 1 transition for IEN_UVLF, IEN_UVHF, and IEN_OVHF for VIN channel N (1 through 6). 00b = Channel interrupts not auto-masked 01b = Channel interrupts auto-masked |

8.5.2.57 AMSK_ENS Register (Address = 0xA4) [Default = X]

AMSK_ENS is shown in [表 8-131](#).

Return to the [Summary Table](#).

Auto-mask ENTRY register. This register is used to mask UVLF, UVHF, and OVHF interrupts on $\overline{\text{SLEEP}}$ transition 1 to 0 transitions.

表 8-131. AMSK_ENS Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|--|
| 7:6 | RSVD | R/W | X | RSVD |
| 5:0 | MON[N] | R/W | 111111b | Auto-mask on $\overline{\text{SLEEP}}$ 1 to 0 transition for IEN_UVLF, IEN_UVHF, and IEN_OVHF for VIN channel N (1 through 6). 00b = Channel interrupts not auto-masked 01b = Channel interrupts auto-masked |

8.5.2.58 SEQ_TOUT_MSB Register (Address = 0xA5) [Default = 0x00]

SEQ_TOUT_MSB is shown in [表 8-132](#).

Return to the [Summary Table](#).

Sequence timeout most significant bits register.

表 8-132. SEQ_TOUT_MSB Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|---------------|------|---------|--|
| 7:0 | MILLISEC[7:0] | R/W | 0b | ACT and $\overline{\text{SLEEP}}$ transition sequence timeout. After the timeout, the auto-masks (AMSK_*) are released and the IEN_xVxF interrupts become active. 0x 0000 = 1 ms 0x 0001 = 2 ms While the max value is not specified, it is desirable to be able to set this timeout up to 4 s, and at least 256 ms (using only the lower byte at address 0xA6). |

8.5.2.59 SEQ_TOUT_LSB Register (Address = 0xA6) [Default = 0x00]

SEQ_TOUT_LSB is shown in [表 8-133](#).

Return to the [Summary Table](#).

Sequence timeout least significant bits register.

表 8-133. SEQ_TOUT_LSB Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|---------------|------|---------|--|
| 7:0 | MILLISEC[7:0] | R/W | 0b | ACT and SLEEP transition sequence timeout. After the timeout, the auto-masks (AMSK_xxx) are released and the IEN_xVxF interrupts become active. 0x 0000 = 1 ms 0x 0001 = 2 ms While the max value is not specified, it is desirable to be able to set this timeout up to 4 s, and at least 256 ms (using only the lower byte at address 0xA6). |

8.5.2.60 SEQ_SYNC Register (Address = 0xA7) [Default = 0x00]

SEQ_SYNC is shown in 表 8-134.

Return to the [Summary Table](#).

Sequence SYNC pulse duration from 50 us to 2600 us.

表 8-134. SEQ_SYNC Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------------|------|---------|---|
| 7:0 | PULSE_WIDTH[7:0] | R/W | 0b | Pulse width for SYNC synchronization pulse. 00000000b = 50μs 00000001b = 60μs 00000010b = 70μs ... 11111101b = 2580μs 11111110b = 2590μs 11111111b = 2600μs |

8.5.2.61 SEQ_UP_THLD Register (Address = 0xA8) [Default = 0xDF]

SEQ_UP_THLD is shown in 表 8-135.

Return to the [Summary Table](#).

Threshold selection register for up sequence tagging ACT and SLEEP transition 0 to 1 transitions.

表 8-135. SEQ_UP_THLD Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|---|
| 7:6 | RSVD | R/W | 11b | RSVD |
| 5:0 | MON[N] | R/W | 11111b | OFF (200 mV) or UV (UV_LF[N] register) threshold selection for Power ON and Exit Sleep sequence tagging: 00b = Use OFF threshold (200 mV) 01b = Use UV threshold (UV_LF[N] register) 0b = OFF 1b = UVLF |

8.5.2.62 SEQ_DN_THLD Register (Address = 0xA9) [Default = 0x00]

SEQ_DN_THLD is shown in 表 8-136.

Return to the [Summary Table](#).

Threshold selection register for down sequence tagging ACT and SLEEP transition 1 to 0 transitions.

表 8-136. SEQ_DN_THLD Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|--------|------|---------|---|
| 7:6 | RSVD | R/W | 0b | RSVD |
| 5:0 | MON[N] | R/W | 0b | OFF (200 mV) or UV (UV_LF[N] register) threshold selection for Power OFF and Enter Sleep sequence tagging: 00b = Use OFF threshold (200 mV) 01b = Use UV threshold (UV_LF[N] register) 0b = OFF 1b = UVLF |

8.5.2.63 SEQ_ON_EXP[1] Register (Address = 0xB0) [Default = 0x00]

SEQ_ON_EXP[1] is shown in 表 8-137.

Return to the [Summary Table](#).

Channel 1 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 1.

表 8-137. SEQ_ON_EXP[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power ON sequence order value for channel 1. This sequence order value is compared with the SEQ_ON_LOG[1] register assigned to the channel during the sequence triggered by ACT. |

8.5.2.64 SEQ_ON_EXP[2] Register (Address = 0xB1) [Default = 0x00]

SEQ_ON_EXP[2] is shown in 表 8-138.

Return to the [Summary Table](#).

Channel 2 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 2.

表 8-138. SEQ_ON_EXP[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power ON sequence order value for channel 2. This sequence order value is compared with the SEQ_ON_LOG[2] register assigned to the channel during the sequence triggered by ACT. |

8.5.2.65 SEQ_ON_EXP[3] Register (Address = 0xB2) [Default = 0x00]

SEQ_ON_EXP[3] is shown in 表 8-139.

Return to the [Summary Table](#).

Channel 3 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 3

表 8-139. SEQ_ON_EXP[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power ON sequence order value for channel 3. This sequence order value is compared with the SEQ_ON_LOG[3] register assigned to the channel during the sequence triggered by ACT. |

8.5.2.66 SEQ_ON_EXP[4] Register (Address = 0xB3) [Default = 0x00]

SEQ_ON_EXP[4] is shown in 表 8-140.

Return to the [Summary Table](#).

Channel 4 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 4.

表 8-140. SEQ_ON_EXP[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power ON sequence order value for channel 4. This sequence order value is compared with the SEQ_ON_LOG[4] register assigned to the channel during the sequence triggered by ACT. |

8.5.2.67 SEQ_ON_EXP[5] Register (Address = 0xB4) [Default = 0x00]

SEQ_ON_EXP[5] is shown in 表 8-141.

Return to the [Summary Table](#).

Channel 5 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 5.

表 8-141. SEQ_ON_EXP[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power ON sequence order value for channel 5. This sequence order value is compared with the SEQ_ON_LOG[5] register assigned to the channel during the sequence triggered by ACT. |

8.5.2.68 SEQ_ON_EXP[6] Register (Address = 0xB5) [Default = 0x00]

SEQ_ON_EXP[6] is shown in 表 8-142.

Return to the [Summary Table](#).

Channel 6 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 6.

表 8-142. SEQ_ON_EXP[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power ON sequence order value for channel 6. This sequence order value is compared with the SEQ_ON_LOG[6] register assigned to the channel during the sequence triggered by ACT. |

8.5.2.69 SEQ_OFF_EXP[1] Register (Address = 0xC0) [Default = 0x00]

SEQ_OFF_EXP[1] is shown in 表 8-143.

Return to the [Summary Table](#).

Channel 1 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 1.

表 8-143. SEQ_OFF_EXP[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power OFF sequence order value for channel 1. This sequence order value is compared with the SEQ_OFF_LOG[1] register assigned to the channel during the sequence triggered by ACT |

8.5.2.70 SEQ_OFF_EXP[2] Register (Address = 0xC1) [Default = 0x00]

SEQ_OFF_EXP[2] is shown in 表 8-144.

Return to the [Summary Table](#).

Channel 2 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 2.

表 8-144. SEQ_OFF_EXP[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power OFF sequence order value for channel 2. This sequence order value is compared with the SEQ_OFF_LOG[2] register assigned to the channel during the sequence triggered by ACT |

8.5.2.71 SEQ_OFF_EXP[3] Register (Address = 0xC2) [Default = 0x00]

SEQ_OFF_EXP[3] is shown in 表 8-145.

Return to the [Summary Table](#).

Channel 3 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 3.

表 8-145. SEQ_OFF_EXP[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power OFF sequence order value for channel 3. This sequence order value is compared with the SEQ_OFF_LOG[3] register assigned to the channel during the sequence triggered by ACT |

8.5.2.72 SEQ_OFF_EXP[4] Register (Address = 0xC3) [Default = 0x00]

SEQ_OFF_EXP[4] is shown in 表 8-146.

Return to the [Summary Table](#).

Channel 4 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 4.

表 8-146. SEQ_OFF_EXP[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power OFF sequence order value for channel 4. This sequence order value is compared with the SEQ_OFF_LOG[4] register assigned to the channel during the sequence triggered by ACT |

8.5.2.73 SEQ_OFF_EXP[5] Register (Address = 0xC4) [Default = 0x00]

SEQ_OFF_EXP[5] is shown in 表 8-147.

Return to the [Summary Table](#).

Channel 5 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 5.

表 8-147. SEQ_OFF_EXP[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power OFF sequence order value for channel 5. This sequence order value is compared with the SEQ_OFF_LOG[5] register assigned to the channel during the sequence triggered by ACT |

8.5.2.74 SEQ_OFF_EXP[6] Register (Address = 0xC5) [Default = 0x00]

SEQ_OFF_EXP[6] is shown in 表 8-148.

Return to the [Summary Table](#).

Channel 6 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 6.

表 8-148. SEQ_OFF_EXP[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|--|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Power OFF sequence order value for channel 6. This sequence order value is compared with the SEQ_OFF_LOG[6] register assigned to the channel during the sequence triggered by ACT |

8.5.2.75 SEQ_EXS_EXP[1] Register (Address = 0xD0) [Default = 0x00]

SEQ_EXS_EXP[1] is shown in 表 8-149.

Return to the [Summary Table](#).

Channel 1 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 1

表 8-149. SEQ_EXS_EXP[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Exit sequence order value for channel 1. This sequence order value is compared with the SEQ_EXS_LOG[1] register assigned to the channel during the sequence triggered by ACT/ SLEEP. |

8.5.2.76 SEQ_EXS_EXP[2] Register (Address = 0xD1) [Default = 0x00]

SEQ_EXS_EXP[2] is shown in 表 8-150.

Return to the [Summary Table](#).

Channel 2 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 2

表 8-150. SEQ_EXS_EXP[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Exit sequence order value for channel 2. This sequence order value is compared with the SEQ_EXS_LOG[2] register assigned to the channel during the sequence triggered by ACT/ SLEEP. |

8.5.2.77 SEQ_EXS_EXP[3] Register (Address = 0xD2) [Default = 0x00]

SEQ_EXS_EXP[3] is shown in 表 8-151.

Return to the [Summary Table](#).

Channel 3 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 3

表 8-151. SEQ_EXS_EXP[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Exit sequence order value for channel 3. This sequence order value is compared with the SEQ_EXS_LOG[3] register assigned to the channel during the sequence triggered by ACT/ SLEEP. |

8.5.2.78 SEQ_EXS_EXP[4] Register (Address = 0xD3) [Default = 0x00]

SEQ_EXS_EXP[4] is shown in 表 8-152.

Return to the [Summary Table](#).

Channel 4 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 4

表 8-152. SEQ_EXS_EXP[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Exit sequence order value for channel 4. This sequence order value is compared with the SEQ_EXS_LOG[4] register assigned to the channel during the sequence triggered by ACT/ SLEEP. |

8.5.2.79 SEQ_EXS_EXP[5] Register (Address = 0xD4) [Default = 0x00]

SEQ_EXS_EXP[5] is shown in 表 8-153.

Return to the [Summary Table](#).

Channel 5 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 5

表 8-153. SEQ_EXS_EXP[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Exit sequence order value for channel 5. This sequence order value is compared with the SEQ_EXS_LOG[5] register assigned to the channel during the sequence triggered by ACT/ SLEEP. |

8.5.2.80 SEQ_EXS_EXP[6] Register (Address = 0xD5) [Default = 0x00]

SEQ_EXS_EXP[6] is shown in 表 8-154.

Return to the [Summary Table](#).

Channel 6 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 6

表 8-154. SEQ_EXS_EXP[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Exit sequence order value for channel 6. This sequence order value is compared with the SEQ_EXS_LOG[6] register assigned to the channel during the sequence triggered by ACT/ SLEEP. |

8.5.2.81 SEQ_ENS_EXP[1] Register (Address = 0xE0) [Default = 0x00]

SEQ_ENS_EXP[1] is shown in 表 8-155.

Return to the [Summary Table](#).

Channel 1 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 1

表 8-155. SEQ_ENS_EXP[1] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Entry sequence order value for channel 1. This sequence order value is compared with the SEQ_ENS_LOG[1] register assigned to the channel during the sequence triggered by SLEEP. |

8.5.2.82 SEQ_ENS_EXP[2] Register (Address = 0xE1) [Default = 0x00]

SEQ_ENS_EXP[2] is shown in 表 8-156.

Return to the [Summary Table](#).

Channel 2 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 2

表 8-156. SEQ_ENS_EXP[2] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Entry sequence order value for channel 2. This sequence order value is compared with the SEQ_ENS_LOG[2] register assigned to the channel during the sequence triggered by SLEEP. |

8.5.2.83 SEQ_ENS_EXP[3] Register (Address = 0xE2) [Default = 0x00]

SEQ_ENS_EXP[3] is shown in 表 8-157.

Return to the [Summary Table](#).

Channel 3 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 3

表 8-157. SEQ_ENS_EXP[3] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Entry sequence order value for channel 3. This sequence order value is compared with the SEQ_ENS_LOG[3] register assigned to the channel during the sequence triggered by SLEEP. |

8.5.2.84 SEQ_ENS_EXP[4] Register (Address = 0xE3) [Default = 0x00]

SEQ_ENS_EXP[4] is shown in [表 8-158](#).

Return to the [Summary Table](#).

Channel 4 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 4

表 8-158. SEQ_ENS_EXP[4] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Entry sequence order value for channel 4. This sequence order value is compared with the SEQ_ENS_LOG[4] register assigned to the channel during the sequence triggered by SLEEP. |

8.5.2.85 SEQ_ENS_EXP[5] Register (Address = 0xE4) [Default = 0x00]

SEQ_ENS_EXP[5] is shown in [表 8-159](#).

Return to the [Summary Table](#).

Channel 5 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 5

表 8-159. SEQ_ENS_EXP[5] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Entry sequence order value for channel 5. This sequence order value is compared with the SEQ_ENS_LOG[5] register assigned to the channel during the sequence triggered by SLEEP. |

8.5.2.86 SEQ_ENS_EXP[6] Register (Address = 0xE5) [Default = 0x00]

SEQ_ENS_EXP[6] is shown in [表 8-160](#).

Return to the [Summary Table](#).

Channel 6 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 6

表 8-160. SEQ_ENS_EXP[6] Register Field Descriptions

| Bit | Field | Type | Default | Description |
|-----|------------|------|---------|---|
| 7:0 | ORDER[7:0] | R/W | 0b | Expected Sleep Entry sequence order value for channel 6. This sequence order value is compared with the SEQ_ENS_LOG[6] register assigned to the channel during the sequence triggered by SLEEP. |

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Modern SOC and FPGA devices typically have multiple power rails to provide power to the different blocks within the IC. Accurate voltage level and timing requirements are common and must be met in order to ensure proper operation of these devices. By utilizing TPS389006 along with a multichannel voltage sequencer, the power up and power down sequencing requirements as well as the core voltage requirements of the target SOC or FPGA device can be met. This design focuses on meeting the timing requirements for an SOC by using the TPS389006.

9.2 Typical Application

9.2.1 Multichannel Sequencer and Monitor

A typical application for the TPS389006 is shown in [Figure 9-1](#). TPS389006 is used to provide the proper voltage monitoring for the target SOC device. A multichannel voltage monitor TPS389006 is used to monitor the voltage rails as these rails power up and power down to ensure that the correct sequence occurs in both occasions. A safety microcontroller is also used to provide ACT, $\overline{\text{SLEEP}}$, and I²C commands to the TPS389006 monitor the NIRQ pin for active faults. The ACT signal from the safety microcontroller determines when the TPS389006 enters into ACTIVE or IDLE states while the NIRQ pin of the TPS389006 acts as a latched interrupt pin that is set when a fault has occurred. The host microcontroller can clear the fault by writing 1 to the affected register(s). The power rails for the safety microcontroller are not shown in [Figure 9-1](#) for simplicity.

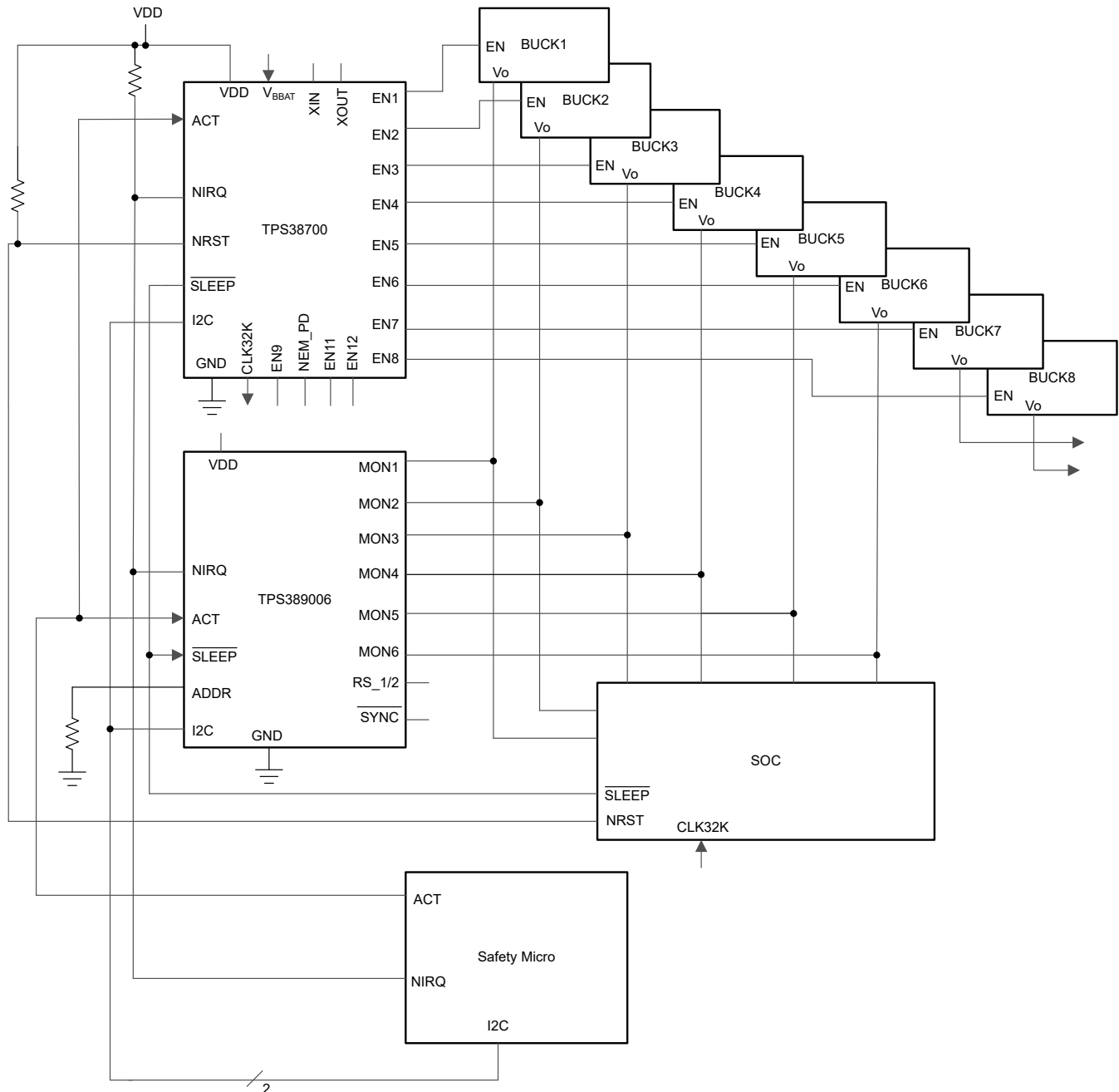


Figure 9-1. TPS389006 Voltage Monitor Design Block Diagram

9.2.2 Design Requirements

Six different voltage rails supplied by DC/DC converters need to be properly monitored in this design. All detected failures in sequencing should be reported via an external hardware interrupt signal. All detected failures should be logged in internal registers and be accessible to an external processor via I²C.

9.2.3 Detailed Design Procedure

TPS389006 device option comes preprogrammed with default values for over voltage, under voltage, expected sequences on power up and down. Please follow the design requirements outlined below.

- NIRQ pin requires a pull up resistor in the range of 10 kΩ to 100 kΩ.
- SDA and SCL lines require pull up resistors in the range of 10 kΩ.
- The ACT pin is driven by an external safety microcontroller. When the ACT pin is driven high, the device enters into ACTIVE mode. When the ACT pin is driven low, the device enters into SLEEP mode.
- The safety microcontroller is used to clear fault interrupts reported through the NIRQ interrupt pin and the INT_SCR1 and INT_SCR2 registers. The interrupt flags can only be cleared by the host microcontroller with a write-1-to-clear operation; interrupt flags are not automatically cleared if the fault condition is no longer present.

9.2.4 Application Curves

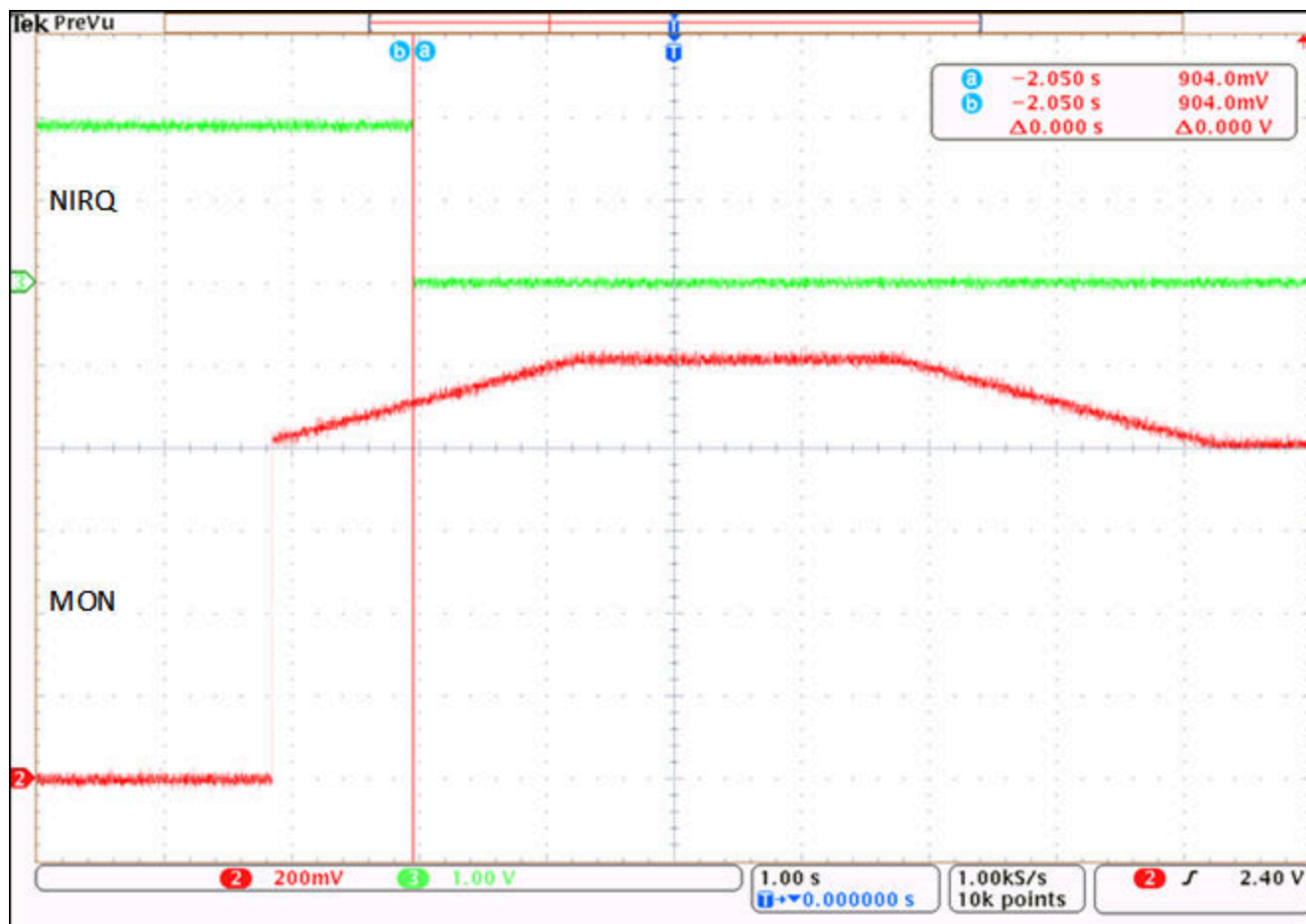
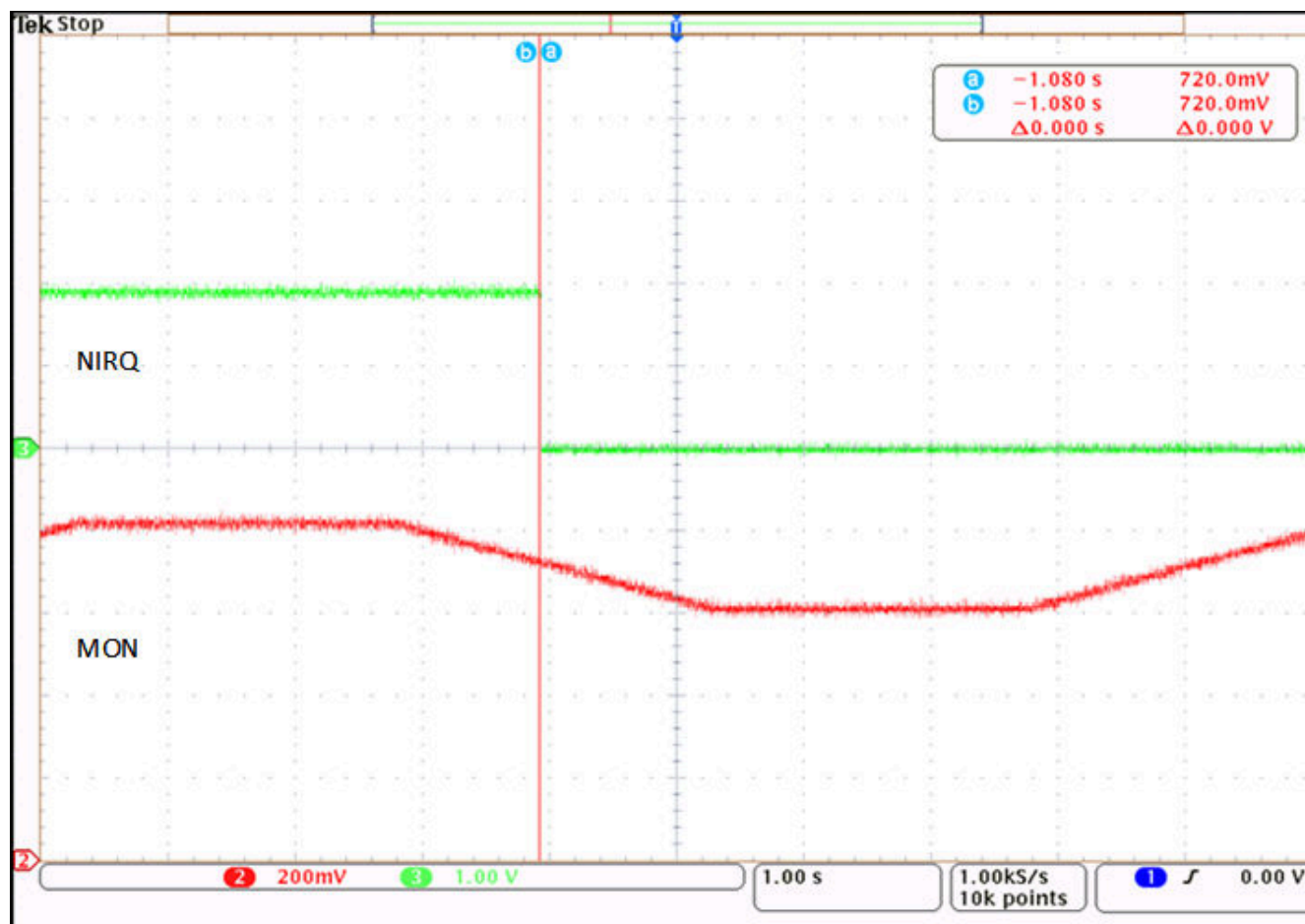


図 9-2. NIRQ Triggered After an Overvoltage Fault



9-3. NIRQ Triggered After an Undervoltage Fault

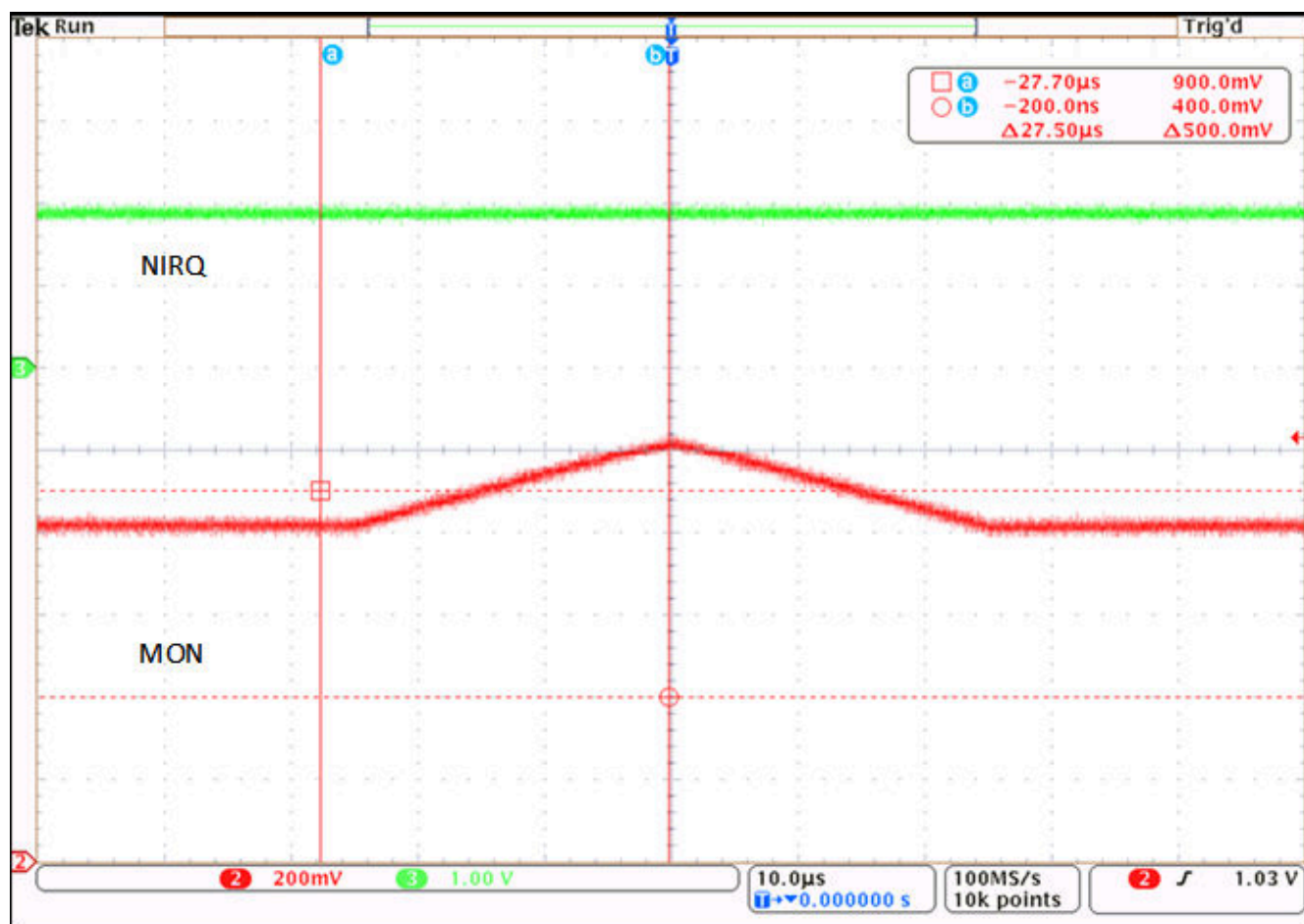


図 9-4. NIRQ Not Triggered on Overvoltage Fault with 51.2 us OV Debounce Filter

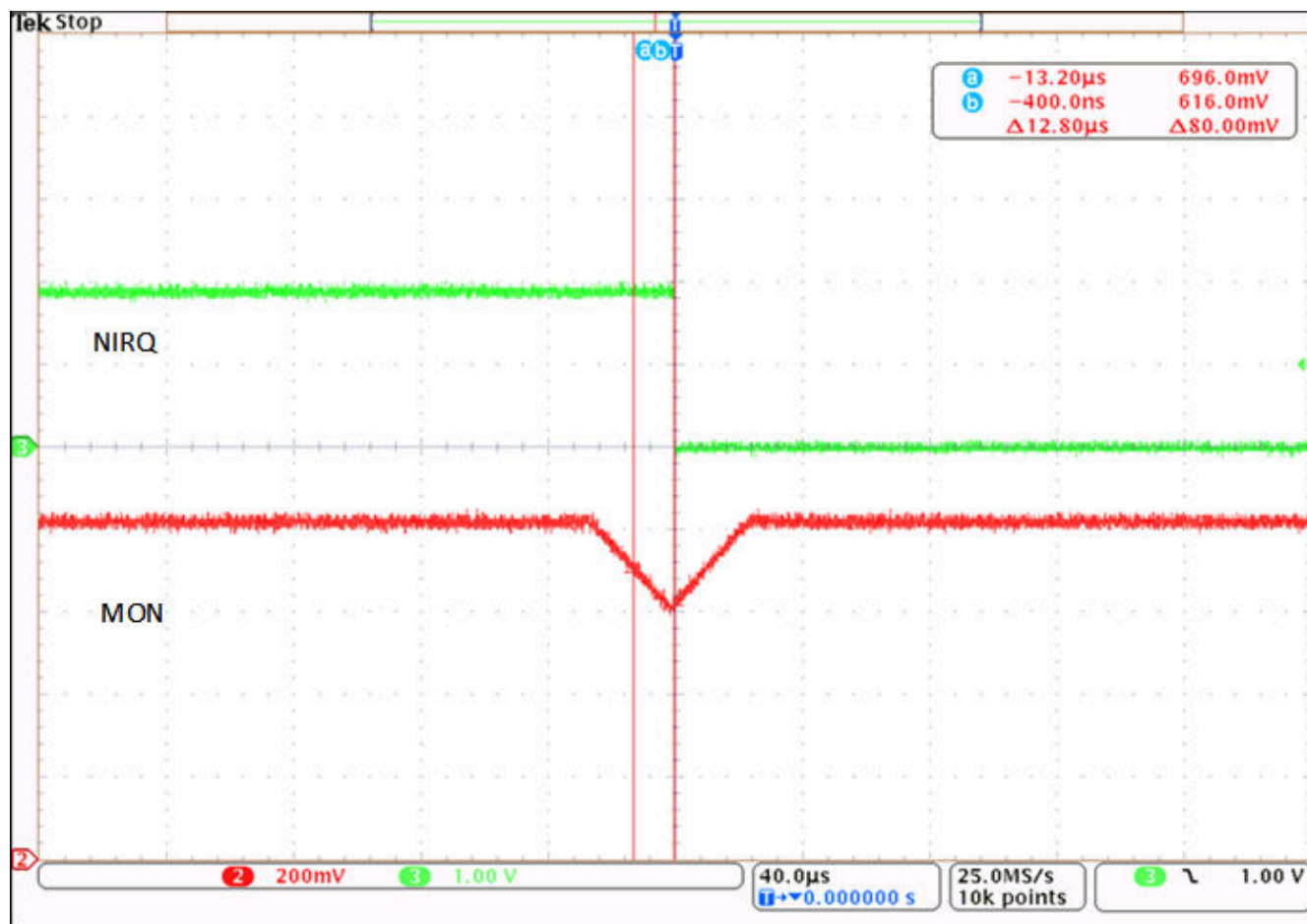
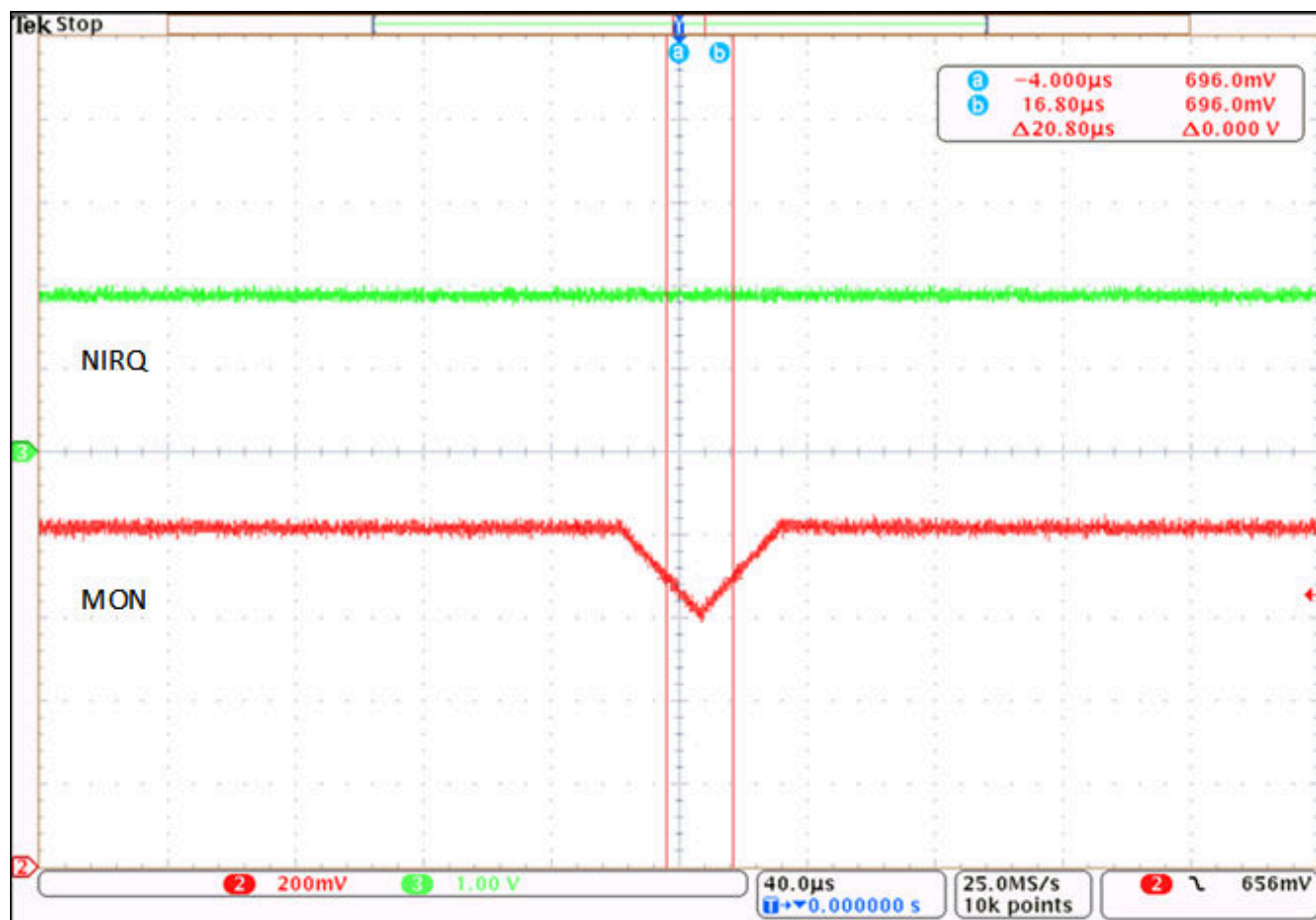
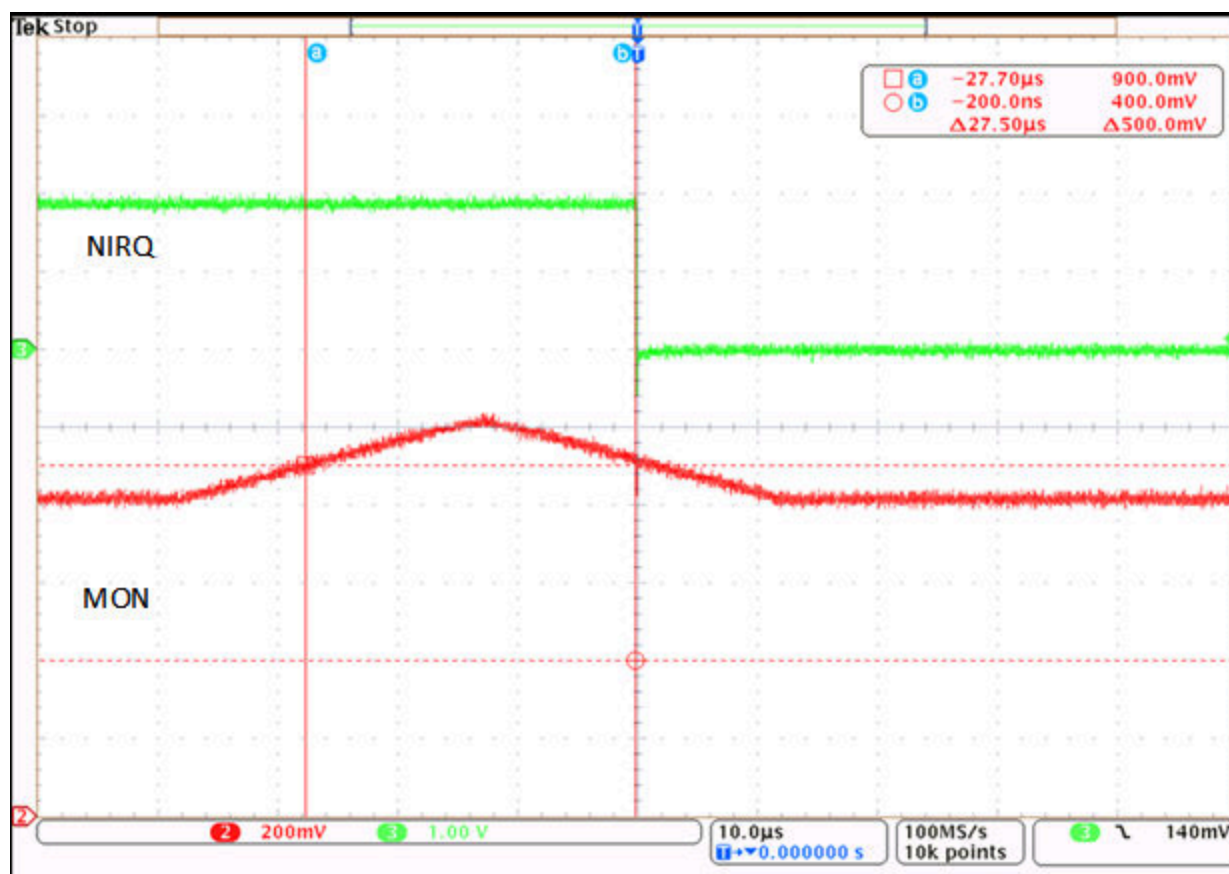


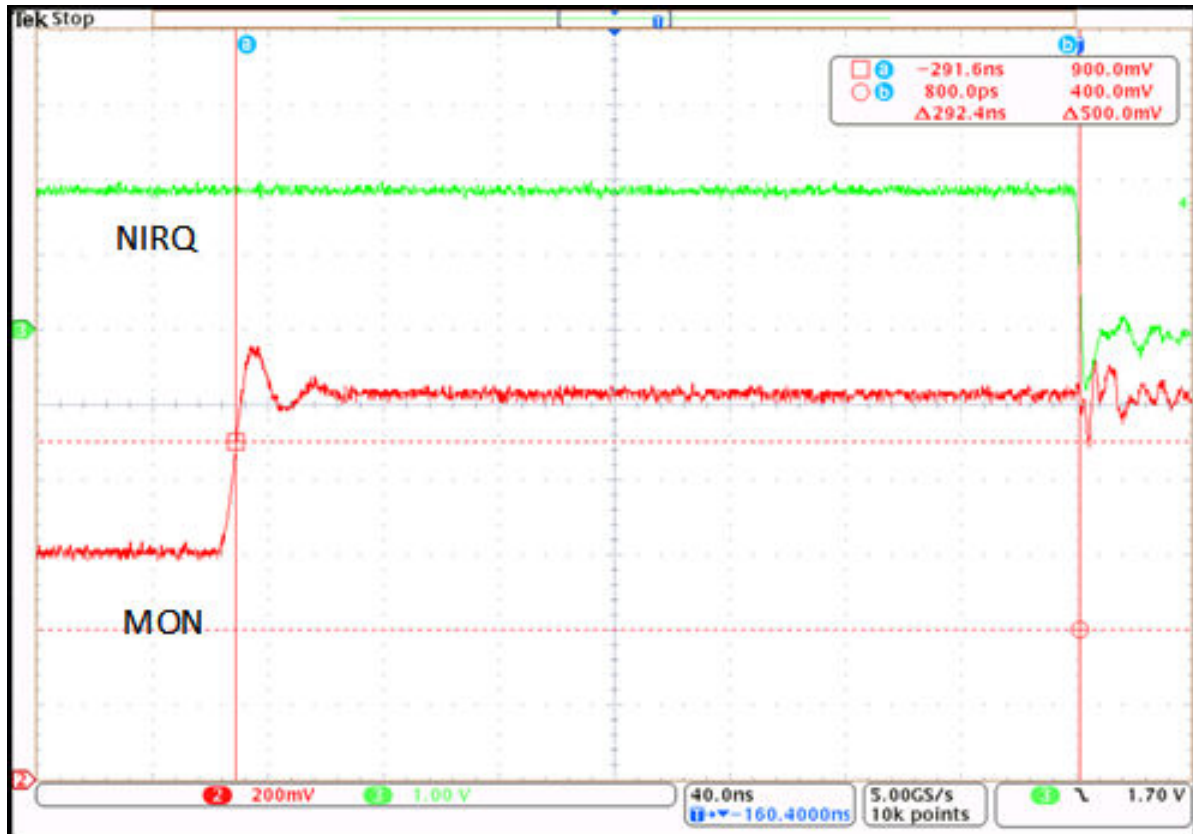
图 9-5. NIRQ Triggered on Undervoltage Fault with 12.8 us UV Debounce Filter



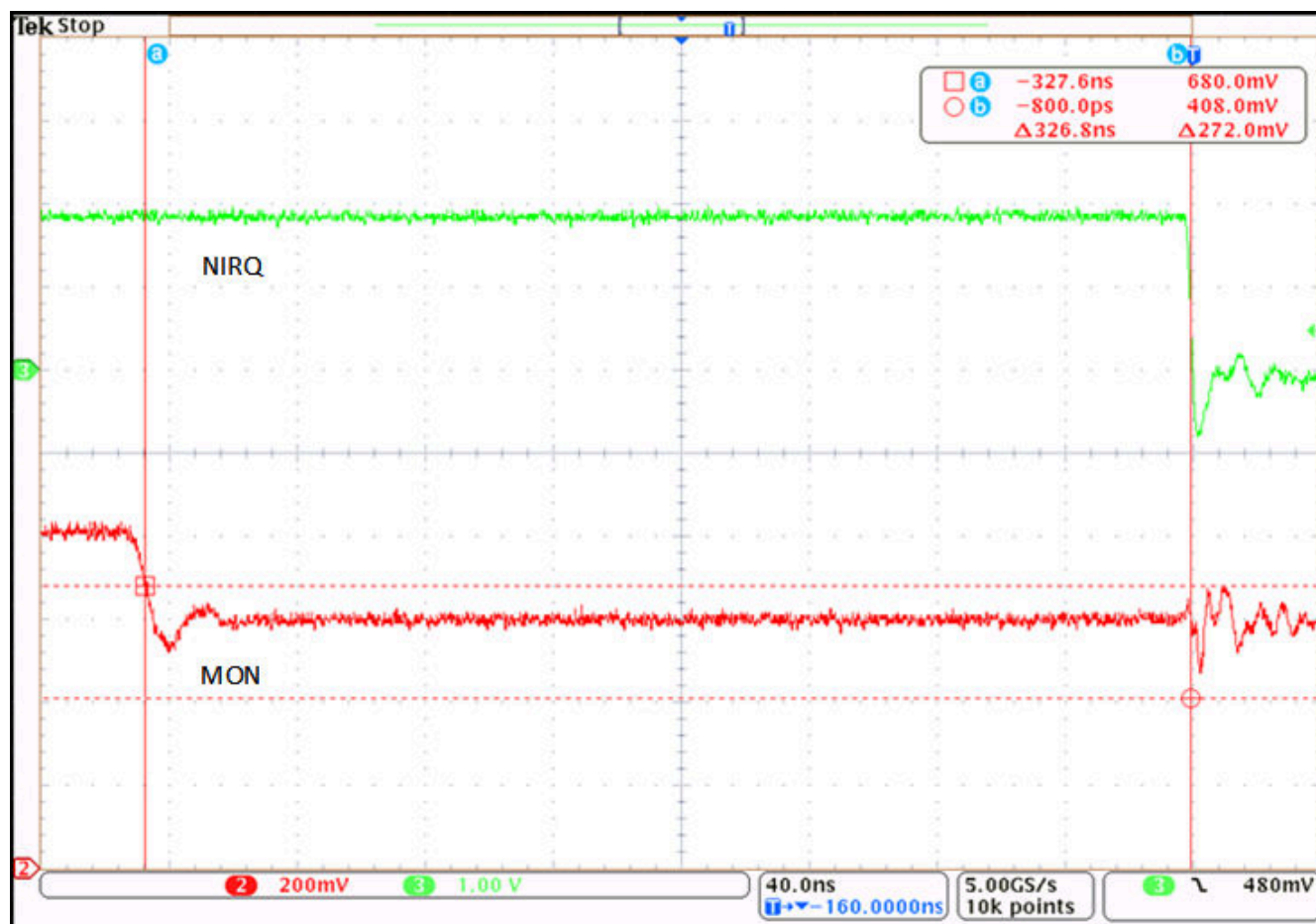
9-6. NIRQ Not Triggered on Undervoltage Fault with 25 us UV Debounce Filter



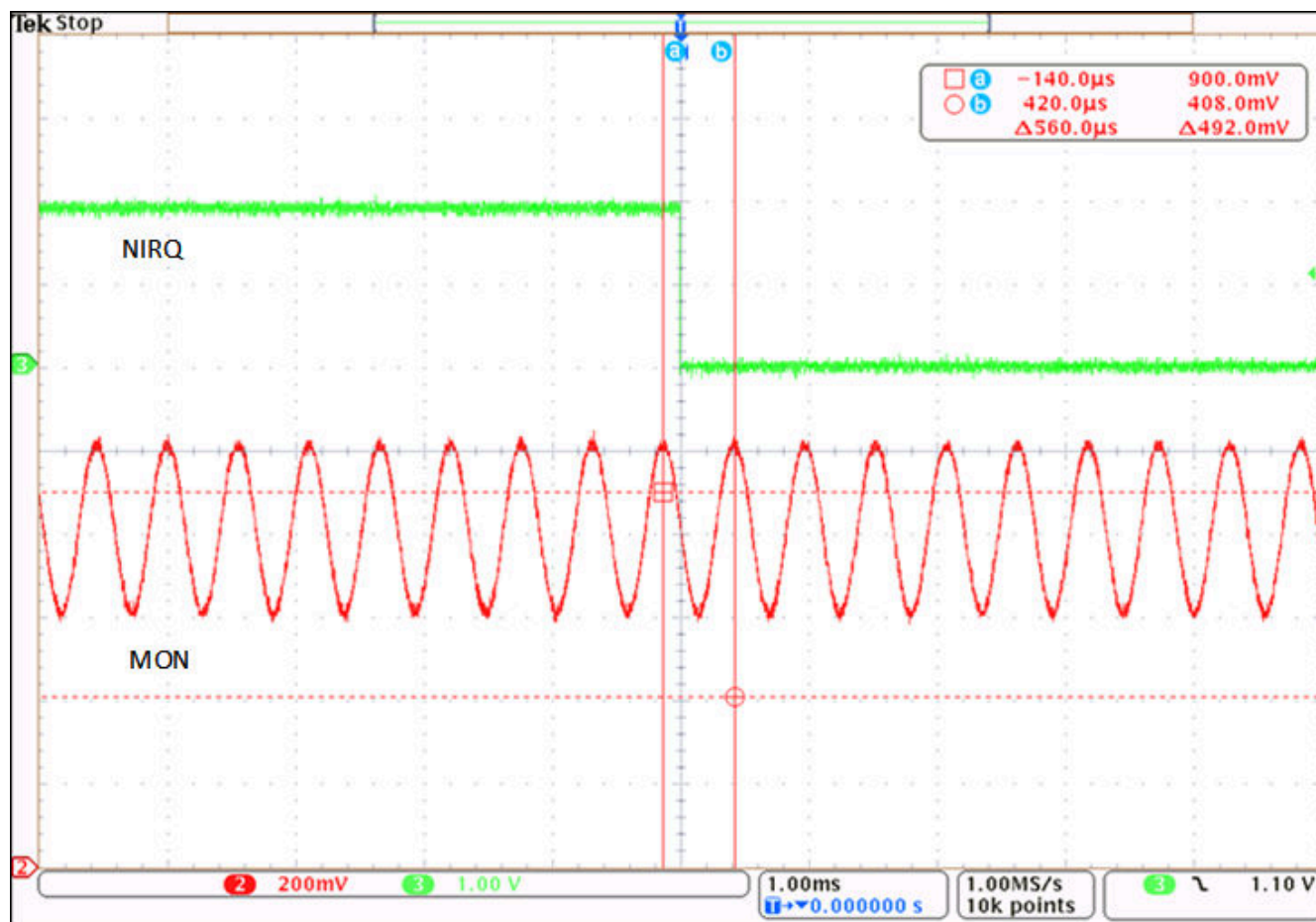
9-7. NIRQ Triggered on Overvoltage Fault with 25 us OV Debounce Filter



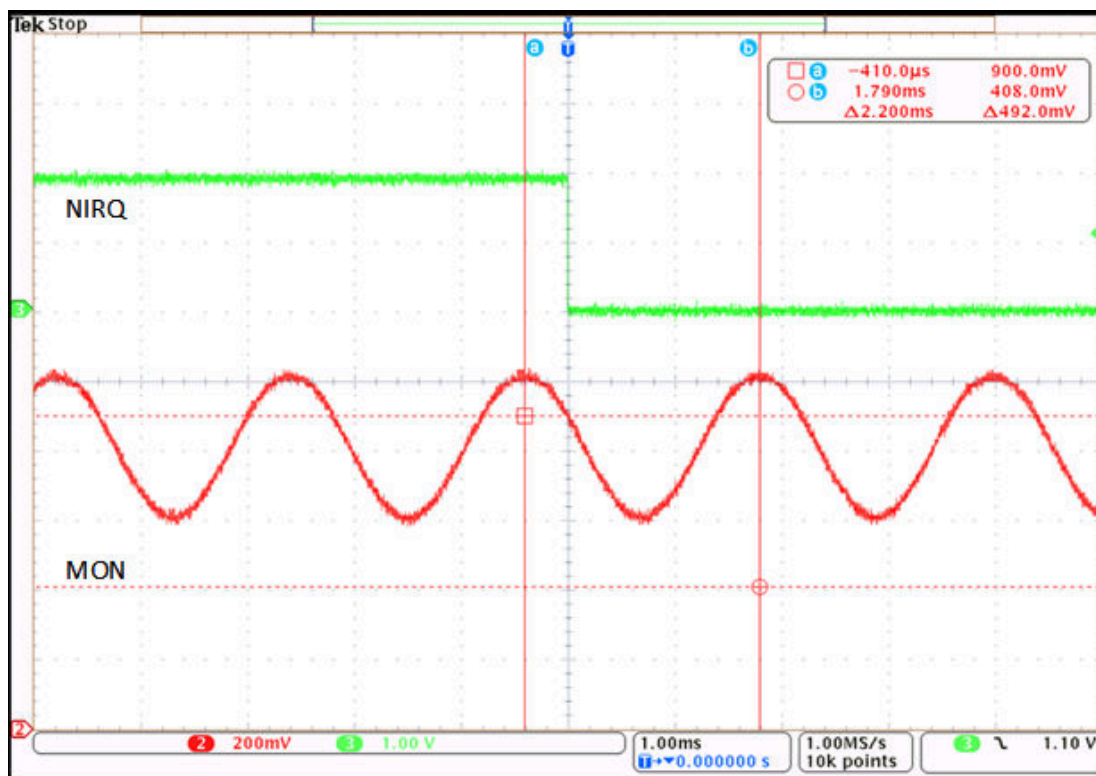
9-8. NIRQ Propogation Delay Resulting from Overvoltage Fault



9-9. NIRQ Propagation Delay Resulting from Undervoltage Fault



9-10. 1 kHz Low Pass Filter Setting. NIRQ Triggered at 1.8 kHz Signal with a 0.8 V DC Component and 200 mVp-p AC Signal. OV and UV Thresholds Set to 0.9V and 0.7V. Reduced the Frequency From 2 kHz Until the NIRQ Pin Went Low.



✉ 9-11. 250 Hz Low Pass Filter setting. NIRQ Triggered at 455 Hz Signal With a 0.8 V DC Component and 200 mVp-p AC Signal. OV and UV Thresholds Set to 0.9V and 0.7V. Reduced the Frequency From 500 Hz Until the NIRQ Pin Went Low.

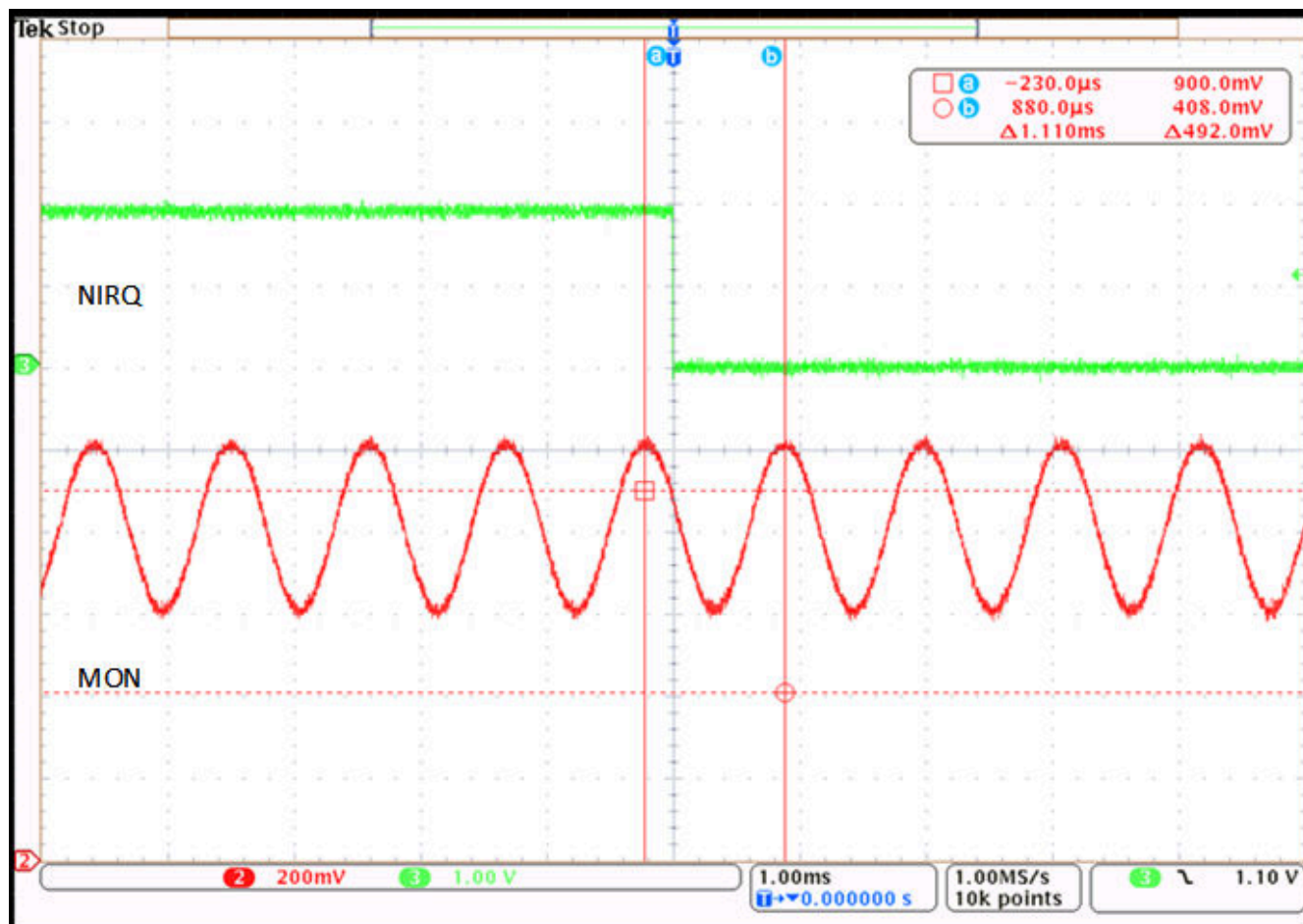


Figure 9-12. 500 Hz Low Pass Filter Setting. NIRQ Triggered at 0.9 kHz Signal With a 0.8 V DC Component and 200 mVp-p AC Signal. OV and UV Thresholds Set to 0.9V and 0.7V. Reduced the Frequency From 1 kHz Until the NIRQ Pin Went Low.

10 Power Supply Recommendations

10.1 Power Supply Guidelines

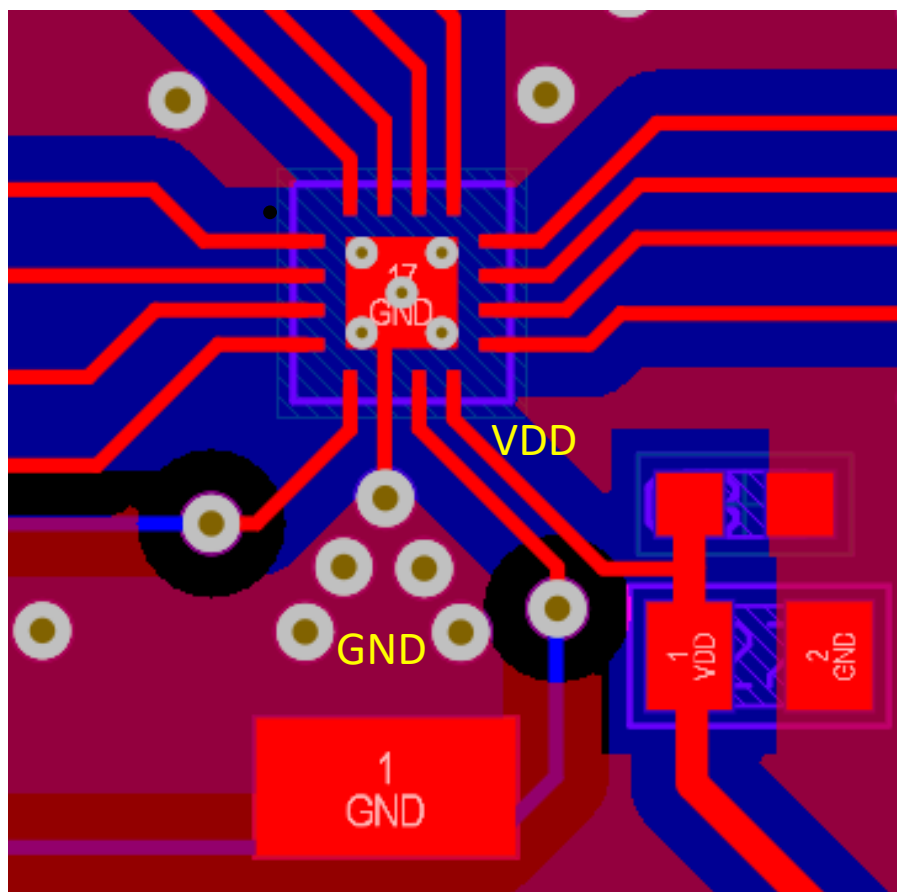
This device is designed to operate from an input supply with a voltage range between 2.5 V to 5.5 V. The device has a 6-V absolute maximum rating on the VDD pin. Good analog practice is to place a 0.1- μ F to 1- μ F capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transient that exceed maximum specifications, additional precautions must be taken. See [SNVA849](#) for more information.

11 Layout

11.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Avoid using long traces of voltage to the MON pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- If differential voltage sensing is required for MON1 and/or MON2, route RS_1/2 pin to the point of measurement
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example



11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Nomenclature

表 12-1 和 表 12-2 show how to decode the function of the device based on its part number.

表 12-1. Device Thresholds

| ORDERING CODE | Thresholds | VMON1 (V) | VMON2 (V) | VMON3 (V) | VMON4 (V) | VMON5 (V) | VMON6 (V) |
|------------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|
| TPS389006ADJRTER | UV_HF/OV_HF | 0.47/0.53 | 0.47/0.53 | 0.66/0.74 | 0.66/0.74 | 0.66/0.74 | 0.66/0.74 |
| | UV_LF/OV_LF | 0.5/0.7 | 0.5/0.7 | 0.5/0.7 | 0.5/0.7 | 0.5/0.7 | 0.5/0.7 |
| TPS389006007RTER | UV_HF/OV_HF | 1.4/2.1 | 1.4/2.1 | 1.4/2.1 | 1.4/2.1 | 1.4/2.1 | 1.4/2.1 |
| | UV_LF/OV_LF | 1.4/2.1 | 1.4/2.1 | 1.4/2.1 | 1.4/2.1 | 1.4/2.1 | 1.4/2.1 |

表 12-2. Device Configuration Table

| ORDERING CODE | FUNCTIONS | SCALING | OV/UV DEBOUNCE | LF CUTOFF | I ² C ADDRESS | BIST | SEQ TIMEOUT | PEC ⁽¹⁾ | I ² C PULL-UP VOLTAGE (V) | ACT/SLEEP |
|------------------|---------------|-------------|-------------------|--------------|--------------------------|--------|-------------|--------------------|---|-----------|
| TPS389006ADJRTER | Monitor LF/HF | 1/1/1/1/1/1 | 102.4μsec | 1kHz | Resistor strap | at POR | 25ms | Disable | 3.3 | Level |
| TPS389006007RTER | Monitor LF/HF | 4/4/4/4/4/4 | 25.6μsec | 1kH | Resistor Strap | At POR | 100ms | Disable | 3.3 | Level |

- (1) For parts with PEC enabled:
- PEC calculation is based on initializing to 0x00.
 - In case of a PEC violation there needs to be a subsequent I²C transaction before NIRQ is asserted.
 - If incorrect PEC is given it will assert NIRQ.
 - If there is an extra byte after successfully writing the correct PEC byte, NIRQ will be asserted and the write will fail.

12.2 Documentation Support

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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12.5 Trademarks

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12.6 静電気放電に関する注意事項



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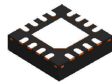
ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.7 用語集

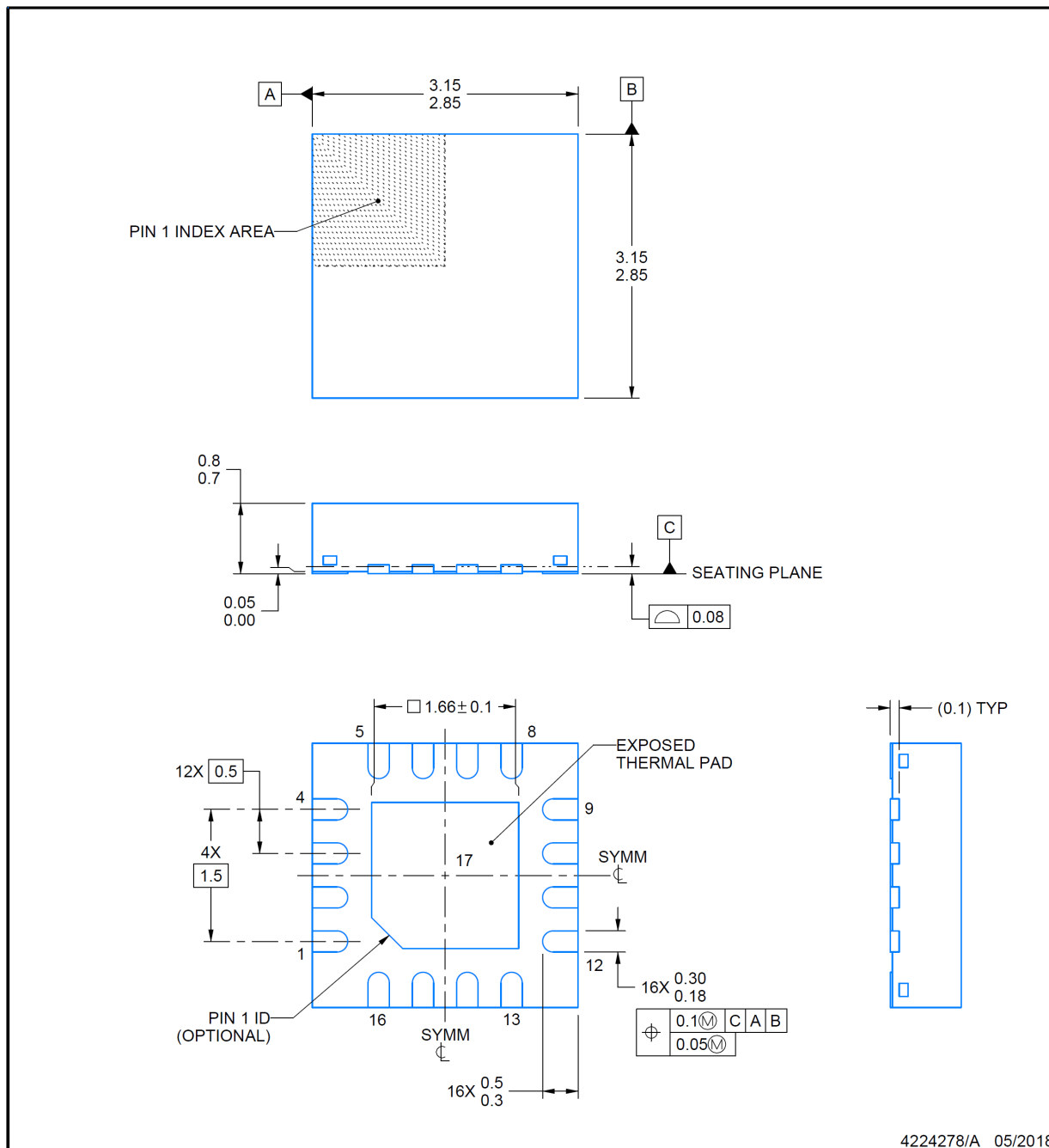
[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**RTE0016J****PACKAGE OUTLINE****WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

**NOTES:**

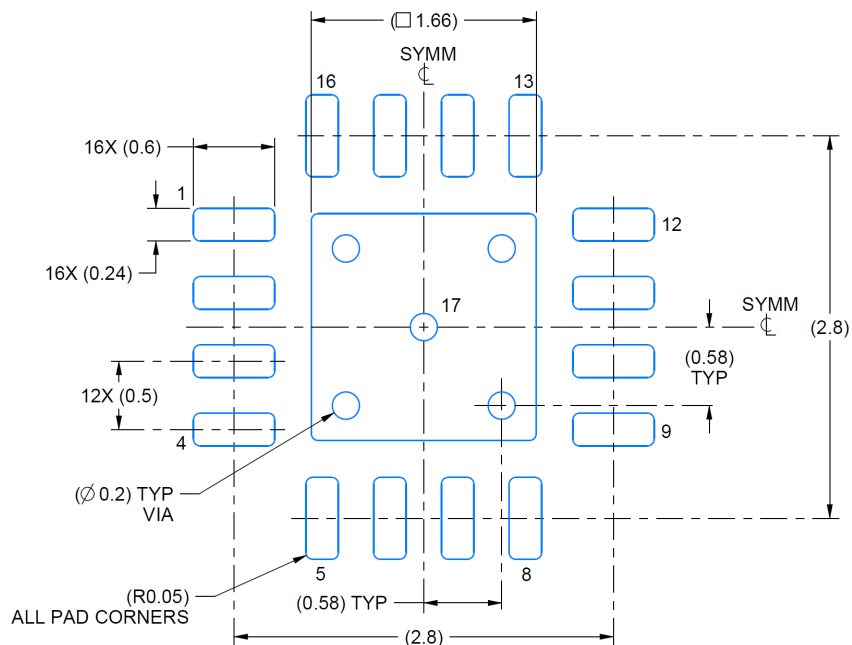
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

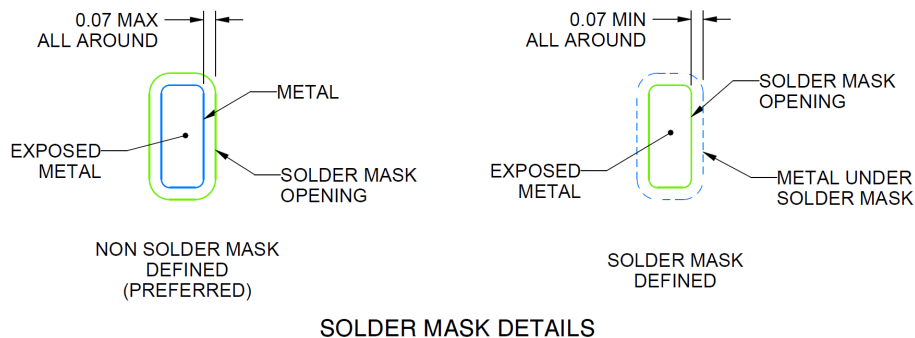
RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



4224278/A 05/2018

NOTES: (continued)

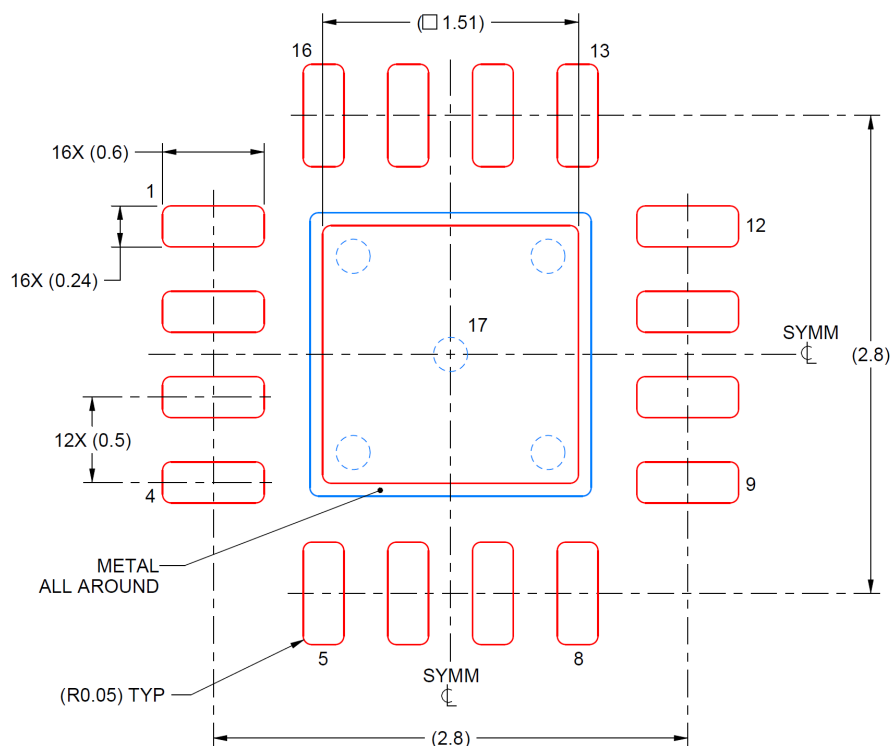
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224278/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS389006007RTER | Active | Production | WQFN (RTE) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 6007R |
| TPS389006007RTER.A | Active | Production | WQFN (RTE) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 6007R |
| TPS389006ADJRTER | Active | Production | WQFN (RTE) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 06ADJ |
| TPS389006ADJRTER.A | Active | Production | WQFN (RTE) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 06ADJ |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS389006 :

- Automotive : [TPS389006-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

GENERIC PACKAGE VIEW

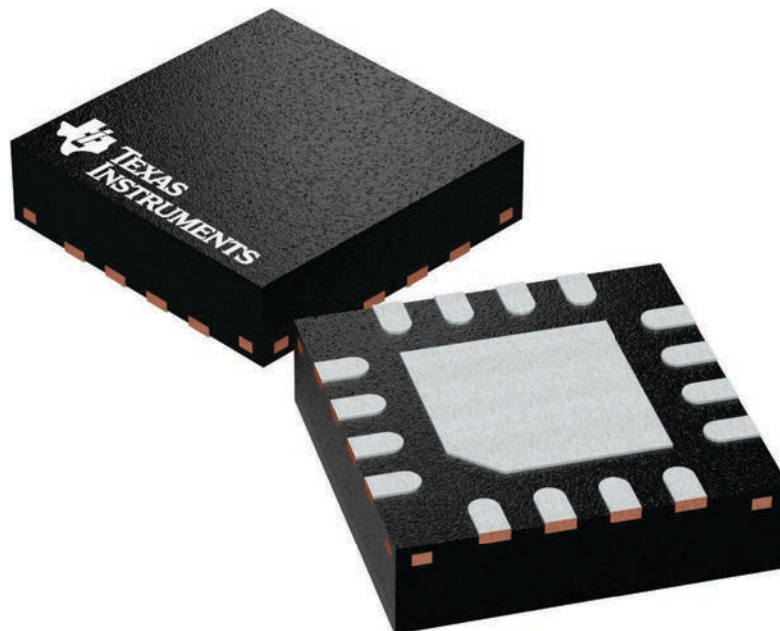
RTE 16

WQFN - 0.8 mm max height

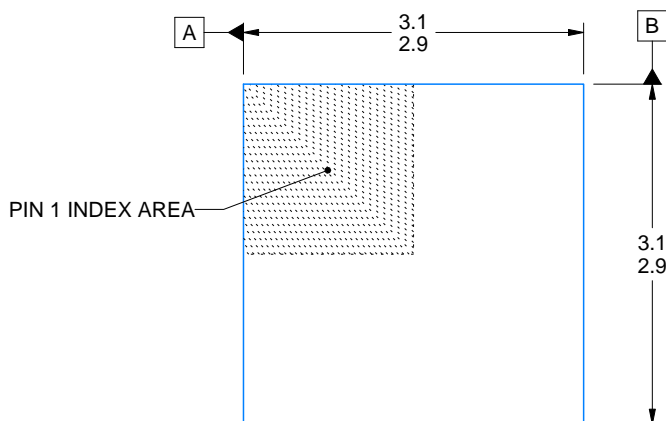
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

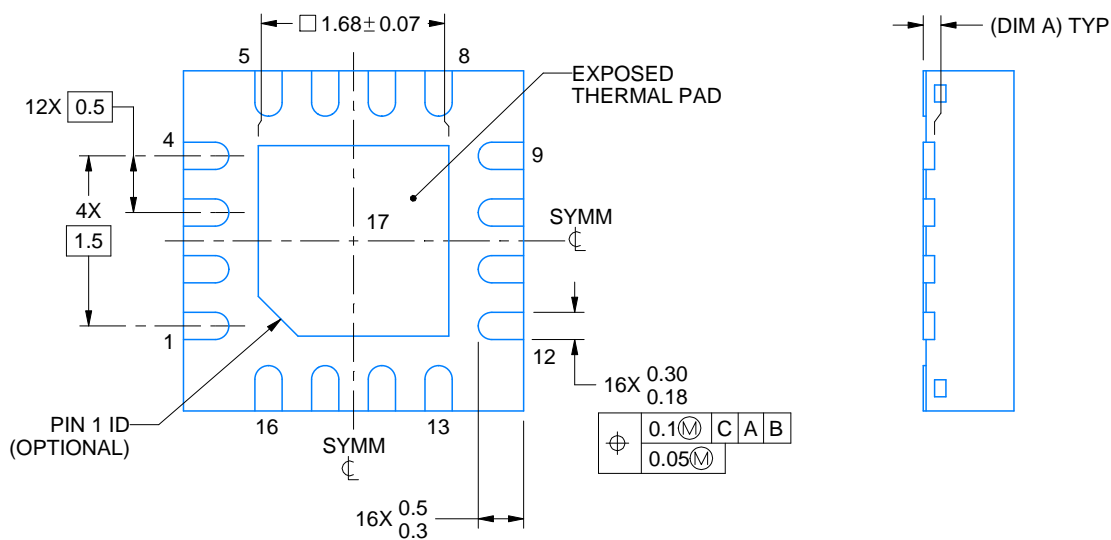
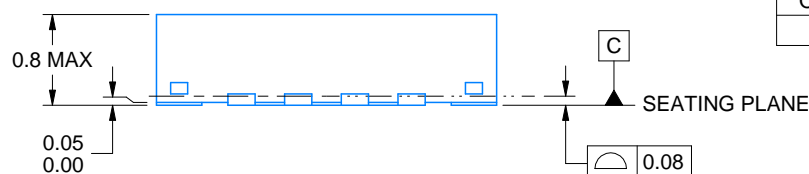
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



| SIDE WALL METAL THICKNESS DIM A | |
|---------------------------------------|----------|
| OPTION 1 | OPTION 2 |
| 0.1 | 0.2 |



4219117/B 04/2022

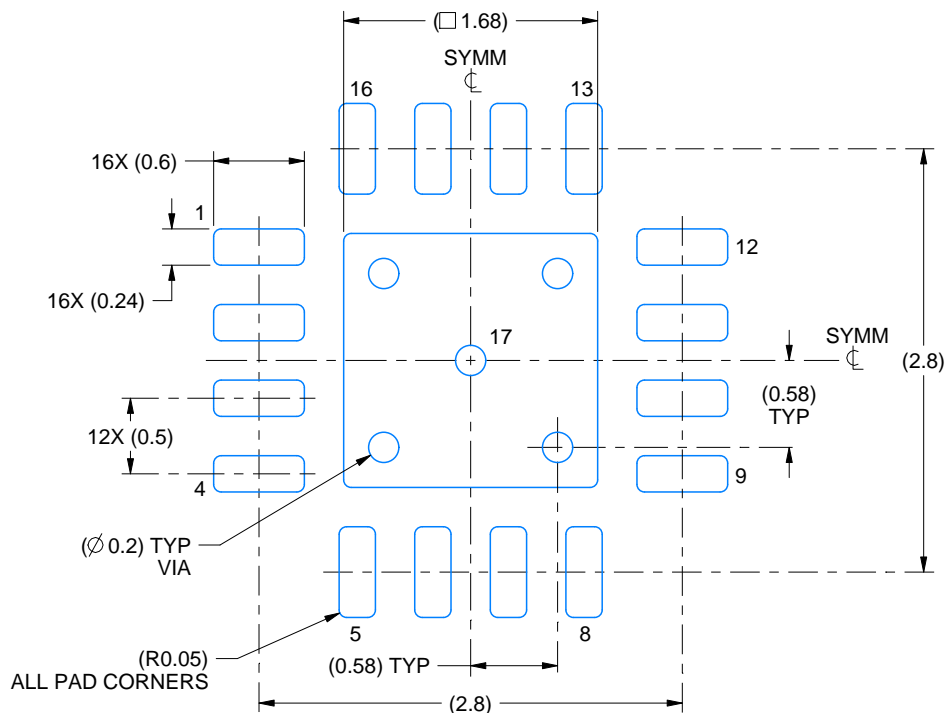
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

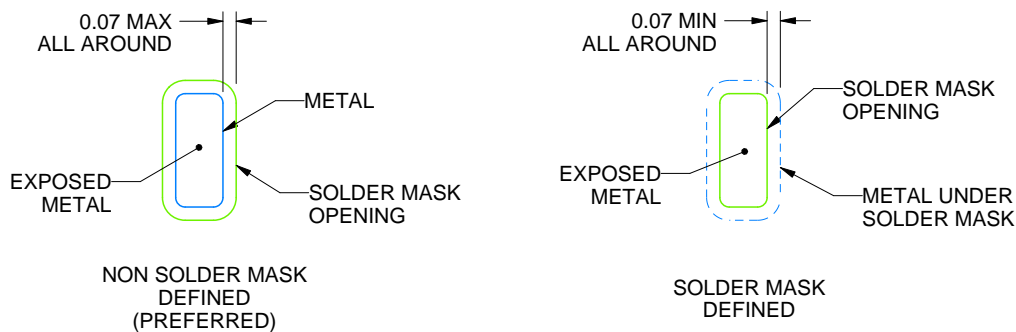
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

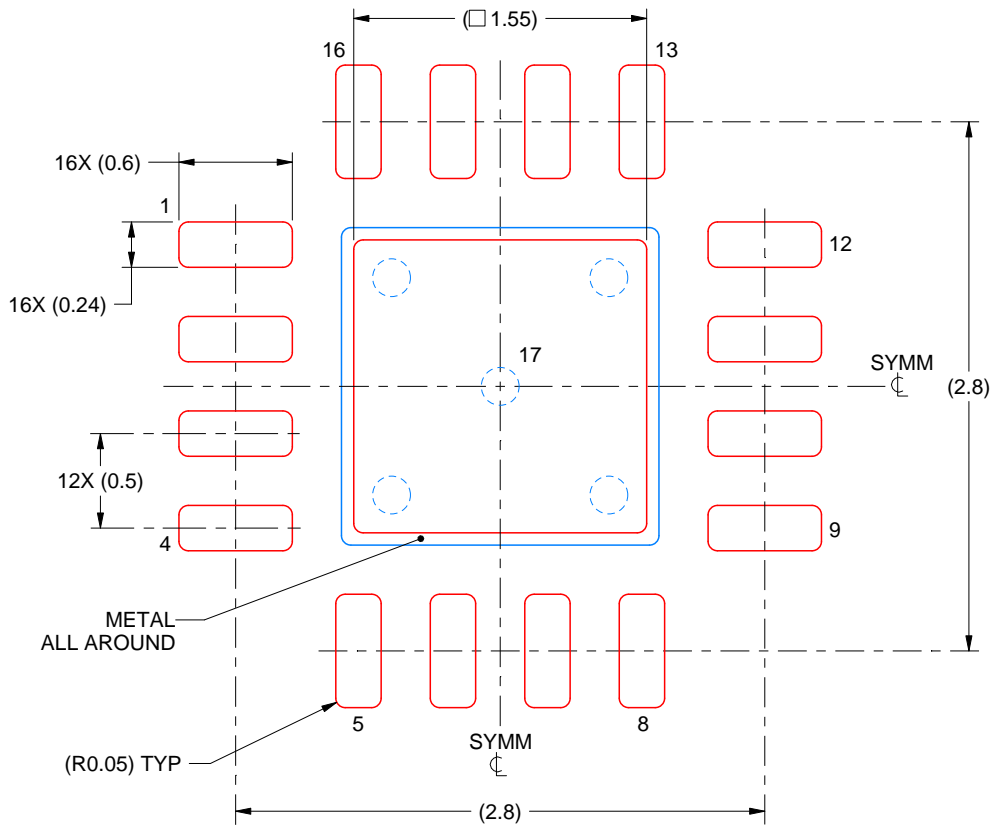
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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