TPS3890-Q1
低静止電流で遅延をプログラム可能な1%精度のスーパバイザ

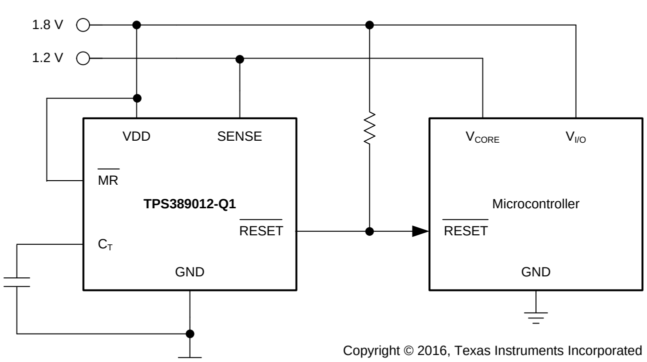
1 特長

- **車載アプリケーションに対応**
- **下記内容でAEC-Q100認定済み：**
  - デバイス温度グレード1: 動作時周囲温度範囲 –40°C～125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC4B
- **パワーオン・リセット(POR)ジェネレータ、遅延時間を25µs～30sに設定可能**
- **非常に低い静止電流: 2.1µA (標準値)**
- **高いスレッショルド精度: 1% (最大値)**
- **高精度のヒステリシス**
- **固定および可変のスレッショルド電圧**
  - 標準レールの固定スレッショルド: 1.2V～5V
  - 最低1.15Vまで調整可能
- **マニュアル・リセット($\overline{\text{MR}}$)入力**
- **オープン・ドレイン$\overline{\text{RESET}}$出力**
- **温度範囲: -40℃～+125℃**
- **パッケージ: 1.5mm×1.5mm WSON**

2 アプリケーション

- **インフォテイメント用ヘッド・ユニット**
- **ハイブリッド/デジタル・クラスタ**
- **外部アンプ**
- **ADASカメラ**
- **車載用ゲートウェイ**

代表的なアプリケーション回路



3 概要

TPS3890-Q1は高精度の電圧スーパーバイザで、静止電流が低く、最低1.15Vのシステム電圧を監視でき、SENSE電圧が設定済みのスレッショルドより低下したとき、またはマニュアル・リセット($\overline{\text{MR}}$)ピンが論理LOWに低下したとき、オープン・ドレインの$\overline{\text{RESET}}$信号をアサートします。$\overline{\text{RESET}}$出力は、SENSE電圧とマニュアル・リセット($\overline{\text{MR}}$)がそれぞれのスレッショルド以上に復帰した後も、ユーザーが設定した遅延時間だけLOWに維持されます。

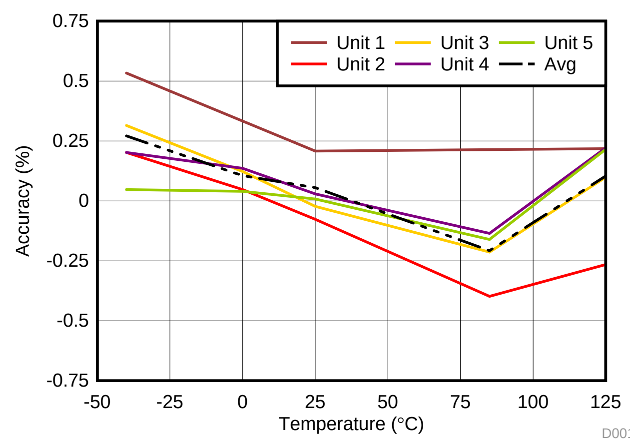
TPS3890-Q1ファミリは、高精度の基準電圧を使用して、1%のスレッショルド精度を実現しています。リセットの遅延時間は、CTピンを外付けのコンデンサへ接続することで、25µs～30sの範囲に設定できます。TPS3890-Q1は静止電流が2.1µAと非常に低く、小形の1.5mm×1.5mmパッケージで供給されるため、バッテリ駆動および実装面積の制限されるアプリケーションに適しています。このデバイスは、-40℃～+125℃の温度範囲(T_J)にわたって完全に動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS3890-Q1	WSON (6)	1.50mm×1.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

V_{ITN}の精度と温度との関係



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4 改訂履歴

Revision A (October 2017) から **Revision B** に変更 — **Page**

- 車載用の特長 追加 ... 1
- Added new voltage options to Device Comparison Table ... 3

2017年**3**月発行のものから更新 — **Page**

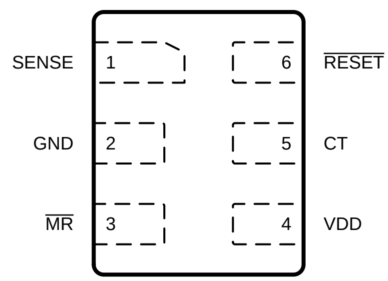
- Added TPS389050L-Q1 to Device Comparison Table ... 3

5 Device Comparison Table

PART NUMBER	NOMINAL SUPPLY VOLTAGE	NEGATIVE THRESHOLD (V_{ITN})	POSITIVE THRESHOLD (V_{ITP})
TPS389001-Q1	Adjustable	1.15 V	1.157 V
TPS389012-Q1	1.2 V	1.15 V	1.157 V
TPS389015-Q1	1.5 V	1.44 V	1.449 V
TPS389018-Q1	1.8 V	1.73 V	1.740 V
TPS389025-Q1	2.5 V	2.40 V	2.414 V
TPS389030-Q1	3.0 V	2.89 V	2.907 V
TPS389033-Q1	3.3 V	3.17 V	3.189 V
TPS389033G-Q1	3.3 V	3.06 V	3.084 V
TPS389033K-Q1	3.3 V	2.93 V	2.947 V
TPS389050-Q1	5.0 V	4.80 V	4.828 V
TPS389050G-Q1	5.0 V	4.65 V	4.677 V
TPS389050L-Q1	5.0 V	4.40 V	4.425 V

6 Pin Configuration and Functions

DSE Package
6-Pin WSON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SENSE	I	This pin is connected to the voltage to be monitored. When the voltage on SENSE falls below the negative threshold voltage V_{ITN}, $\overline{\text{RESET}}$ goes low (asserts). When the voltage on SENSE rises above the positive threshold voltage V_{ITP}, $\overline{\text{RESET}}$ goes high (deasserts).
2	GND	—	Ground
3	$\overline{\text{MR}}$	I	Driving the manual reset pin ($\overline{\text{MR}}$) low causes $\overline{\text{RESET}}$ to go low (assert).
4	VDD	I	Supply voltage pin. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.
5	CT	—	The CT pin offers a user-adjustable delay time. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$ delay time to deassert. $t_{PD(r)}$ (sec) = C_{CT} (µF) × 1.07 + 25 µs (nom).
6	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ is an open-drain output that is driven to a low-impedance state when either the $\overline{\text{MR}}$ pin is driven to a logic low or the monitored voltage on the SENSE pin is lower than the negative threshold voltage (V_{ITN}). $\overline{\text{RESET}}$ remains low (asserted) for the delay time period after both $\overline{\text{MR}}$ is set to a logic high and the SENSE input is above V_{ITP}. A pullup resistor from 10 kΩ to 1 MΩ should be used on this pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	7	V
	SENSE	–0.3	7	
	$\overline{\text{RESET}}$	–0.3	7	
	$\overline{\text{MR}}$	–0.3	7	
	V_{CT}	–0.3	7	
Current	$\overline{\text{RESET}}$	–20	20	mA
Temperature	Operating junction, T_J	–40	125	°C
	Operating ambient, T_A	–40	125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Power-supply voltage	1.5		5.5	V
V_{SENSE}	SENSE voltage	0		5.5	V
V_{RESET}	$\overline{\text{RESET}}$ pin voltage	0		5.5	V
I_{RESET}	$\overline{\text{RESET}}$ pin current	–5		5	mA
C_{IN}	Input capacitor, VDD pin	0	0.1		µF
C_{CT}	Reset timeout capacitor, CT pin	0		26	µF
R_{PU}	Pullup resistor, $\overline{\text{RESET}}$ pin	1		1000	kΩ
T_J	Junction temperature (free-air temperature)	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS3890-Q1	UNIT
		DSE (WSON)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	321.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	207.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	281.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	42.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	284.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	142.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over the operating junction temperature range of –40°C to +125°C ($T_A = T_J$), 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR} = V_{DD}$ (unless otherwise noted); typical values are at V_{DD} = 5.5 V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply voltage		1.5		5.5	V
V_{POR}	Power-on-reset voltage	$V_{OL(max)}$ = 0.2 V, I_{RESET} = 15 µA			0.8	V
I_{DD}	Supply current (into VDD pin)	V_{DD} = 3.3 V, I_{RESET} = 0 mA, –40°C < T_J < 85°C		2.09	3.72	µA
		V_{DD} = 3.3 V, I_{RESET} = 0 mA, –40°C < T_J < 105°C			4.5	
		V_{DD}= 3.3 V, I_{RESET} = 0 mA			5.8	
		V_{DD} = 5.5 V, I_{RESET} = 0 mA, –40°C < T_J < 85°C		2.29	4	
		V_{DD} = 5.5 V, I_{RESET} = 0 mA, –40°C < T_J < 105°C			5.2	
		V_{DD} = 5.5 V, I_{RESET} = 0 mA			6.5	
V_{ITN}, V_{ITP}	SENSE input threshold voltage accuracy		–1%	±0.5%	1%	
V_{HYST}	Hysteresis(1)		0.325%	0.575%	0.825%	
I_{SENSE}	Input current	V_{SENSE} = 5 V			8	µA
		V_{SENSE} = 5 V, TPS389001-Q1, TPS389012-Q1		10	100	nA
I_{CT}	CT pin charge current		0.90	1.15	1.35	µA
V_{CT}	CT pin comparator threshold voltage		1.17	1.23	1.29	V
R_{CT}	CT pin pulldown resistance	When $\overline{RESET}$ is deasserted		200		Ω
V_{IL}	Low-level input voltage ($\overline{MR}$ pin)				0.25 × V_{DD}	V
V_{IH}	High-level output voltage		0.7 x V_{DD}			V
V_{OL}	Low-level output voltage	V_{DD} ≥ 1.5 V, I_{RESET} = 0.4 mA			0.25	V
		V_{DD} ≥ 2.7 V, I_{RESET} = 2 mA			0.25	
		V_{DD} ≥ 4.5 V, I_{RESET} = 3 mA			0.3	
$I_{LKG(OD)}$	Open-drain output leakage	High impedance, $V_{SENSE} = V_{RESET}$ = 5.5 V			250	nA

(1) $V_{HYST} = [(V_{ITP} – V_{ITN}) / V_{ITN}] \times 100\%$.

7.6 Timing Requirements

over the operating junction temperature range of –40°C to +125°C ($T_A = T_J$), 1.5 V ≤ V_{DD} ≤ 5.5 V, $\overline{MR} = V_{DD}$, and 5% input overdrive(1) (unless otherwise noted); typical values are at V_{DD} = 5.5 V and T_J = 25°C

			MIN	NOM	MAX	UNIT
$t_{PD(f)}$	SENSE (falling) to $\overline{RESET}$ propagation delay	C_T = open, V_{DD} = 3.3 V		18		µs
		C_T = open, V_{DD} = 5.5 V		8		
$t_{PD(r)}$	SENSE (rising) to $\overline{RESET}$ propagation delay	C_T = open, V_{DD} = 3.3 V		25		µs
$t_{GI(SENSE)}$	SENSE pin glitch immunity	V_{DD} = 5.5 V		9		µs
$t_{GI(MR)}$	$\overline{MR}$ pin glitch immunity	V_{DD} = 5.5 V		100		ns
t_{MRW}	$\overline{MR}$ pin pulse duration to assert $\overline{RESET}$		1			µs
$t_{d(MR)}$	$\overline{MR}$ pin low to out delay			250		ns
t_{STRT}	Startup delay			325		µs

(1) Overdrive = | (V_{IN} / V_{THRESH} – 1) × 100% |.

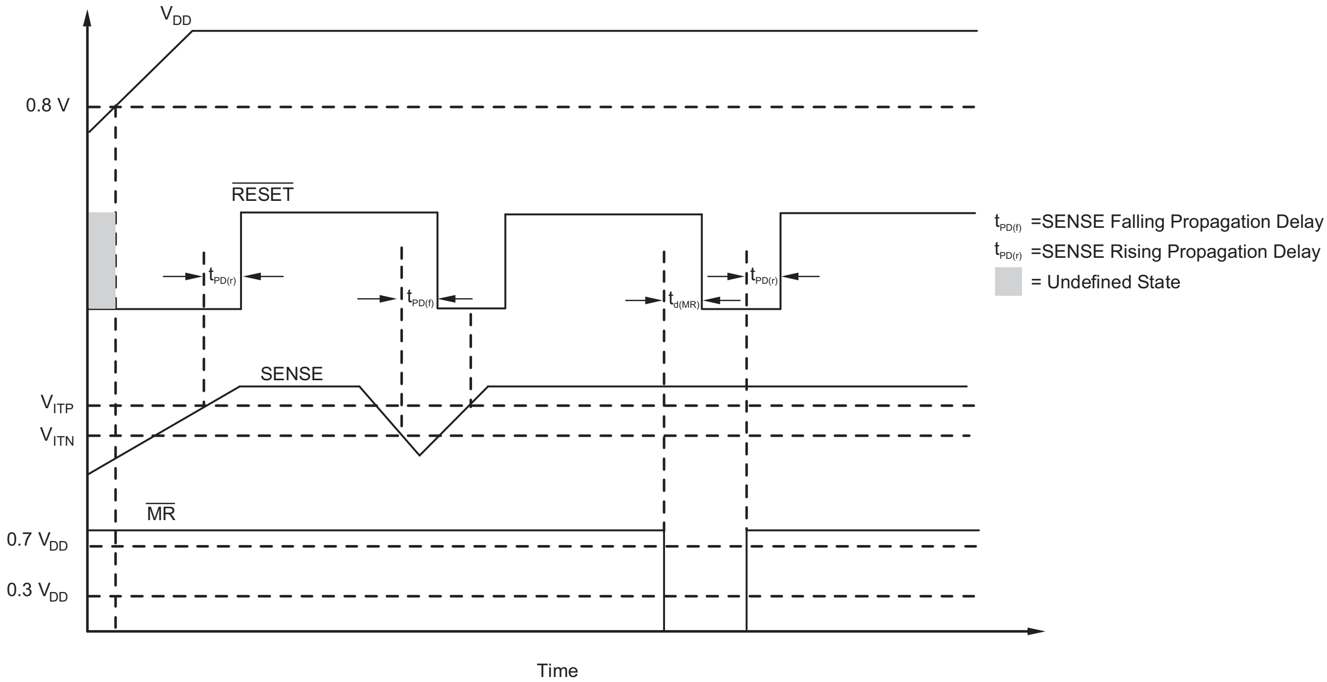


図 1. Timing Diagram

7.7 Typical Characteristics

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR}$ = V_{DD} (unless otherwise noted)

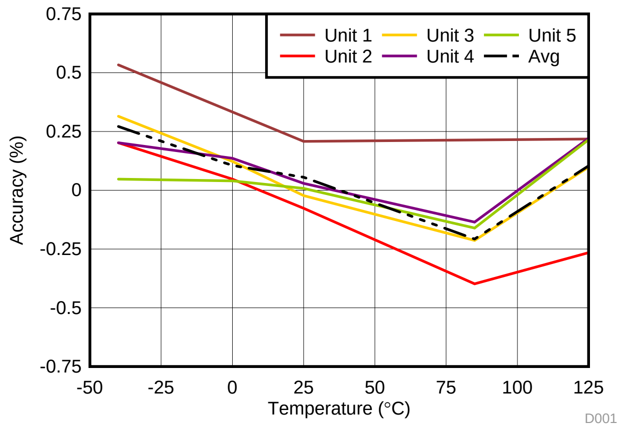


図 2. V_{ITN} Accuracy vs Temperature

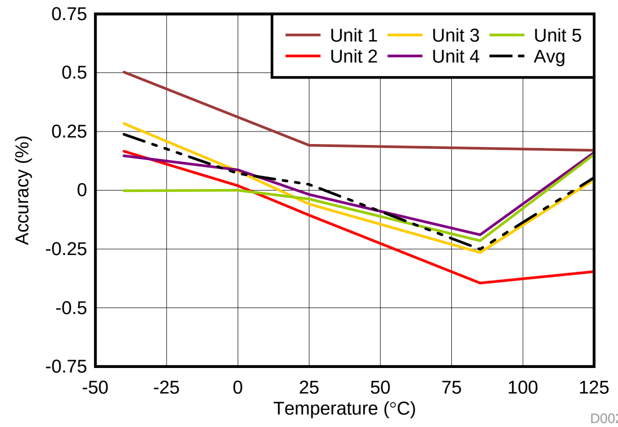
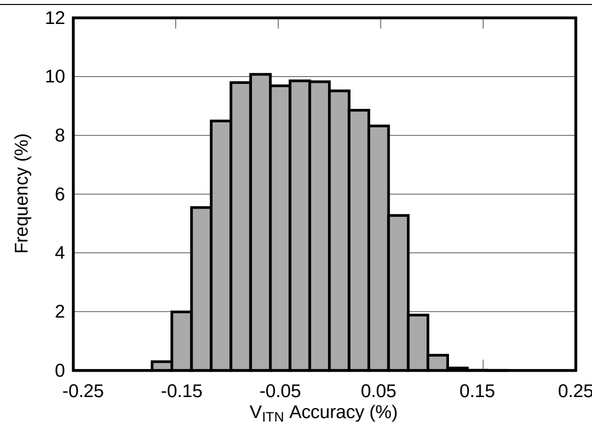
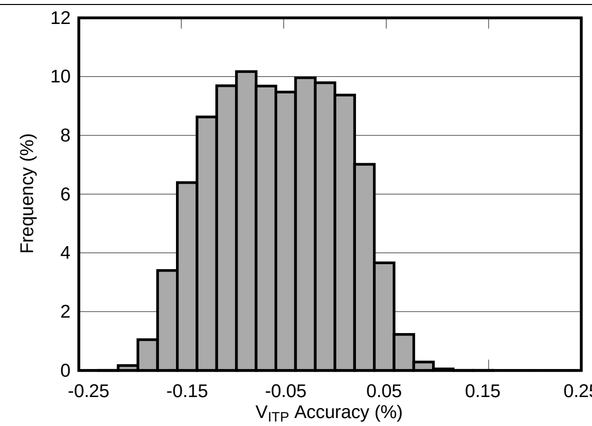


図 3. V_{ITP} Accuracy vs Temperature



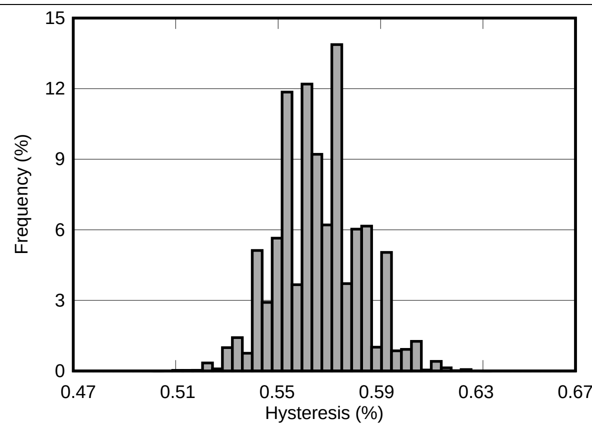
Tested at V_{DD} = 1.5 V and V_{DD} = 5.5 V, total tests = 136,348

図 4. V_{ITN} Accuracy Histogram



Tested at V_{DD} = 1.5 V and V_{DD} = 5.5 V, total tests = 136,348

図 5. V_{ITP} Accuracy Histogram



Tested at V_{DD} = 1.5 V and V_{DD} = 5.5 V, total tests = 136,348

図 6. Hysteresis Histogram

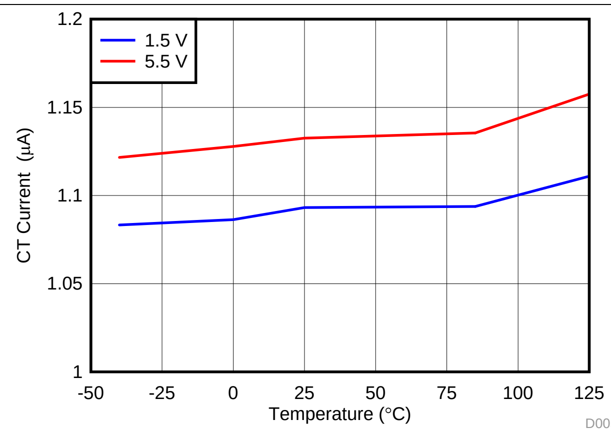
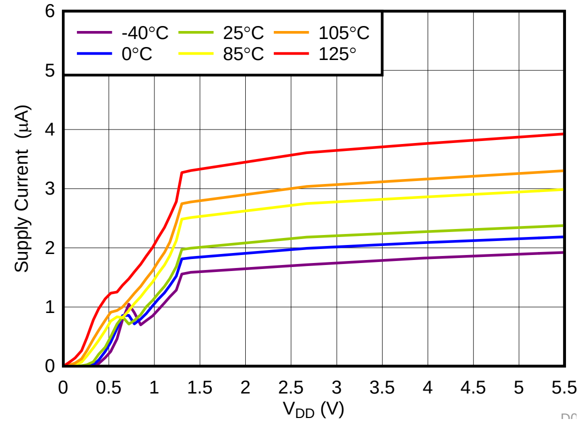


図 7. CT Current vs Temperature

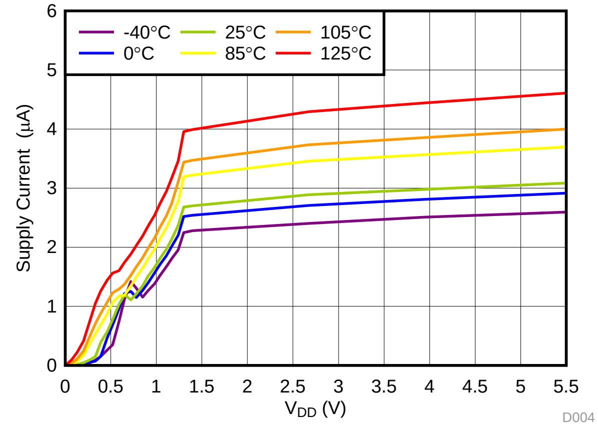
Typical Characteristics (continued)

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR}$ = V_{DD} (unless otherwise noted)



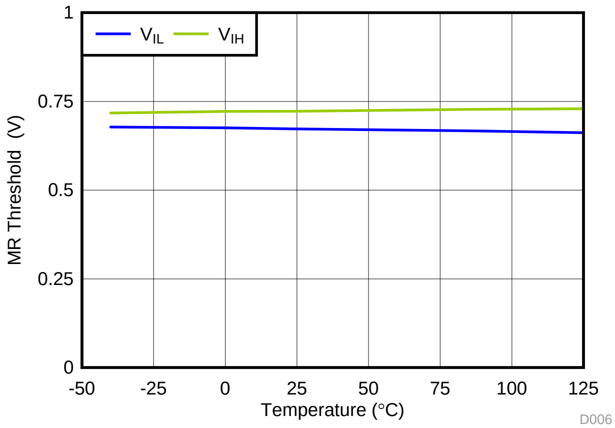
$\overline{MR}$ = V_{DD}

図 8. Supply Current vs Power-Supply Voltage



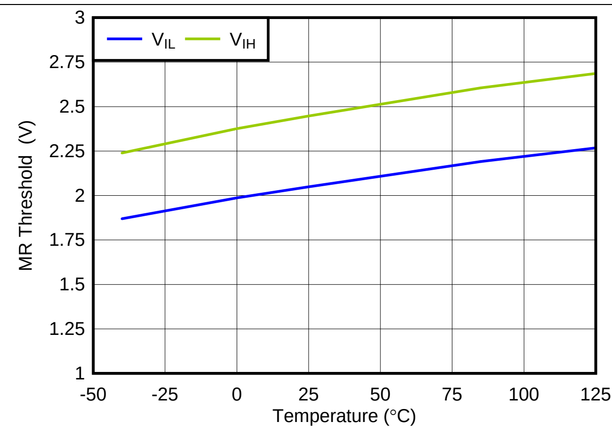
$\overline{MR}$ = 0 V

図 9. Supply Current vs Power-Supply Voltage



V_{DD} = 1.5 V

図 10. $\overline{MR}$ Threshold vs Temperature



V_{DD} = 5.5 V

図 11. $\overline{MR}$ Threshold vs Temperature

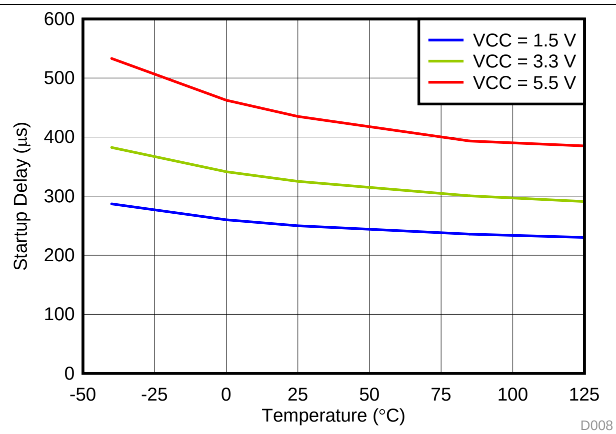
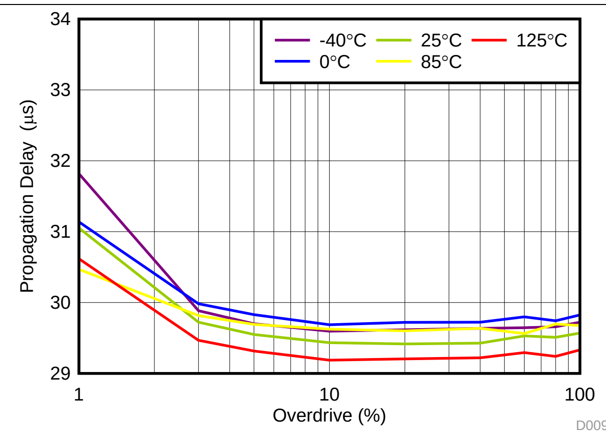


図 12. Startup Delay vs Temperature



V_{DD} = 5.5 V

図 13. Propagation Delay ($t_{PD(r)}$) vs Overdrive

Typical Characteristics (continued)

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR}$ = V_{DD} (unless otherwise noted)

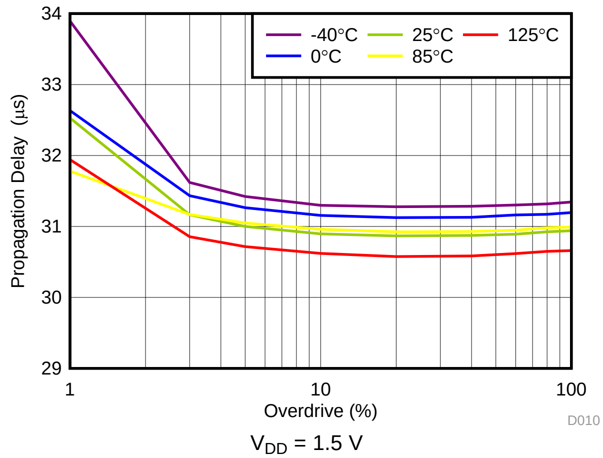


図 14. Propagation Delay ($t_{PD(r)}$) vs Overdrive

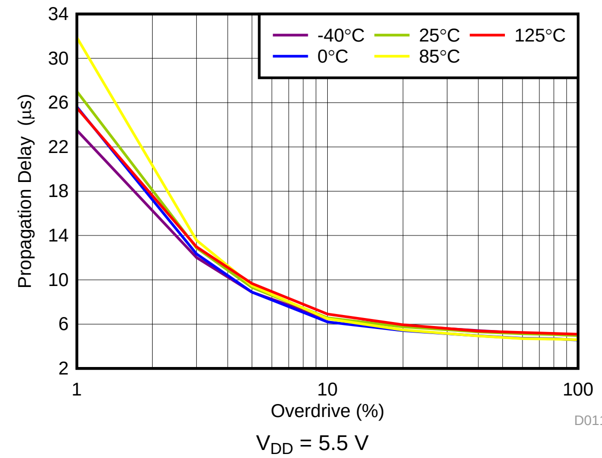


図 15. Propagation Delay ($t_{PD(f)}$) vs Overdrive

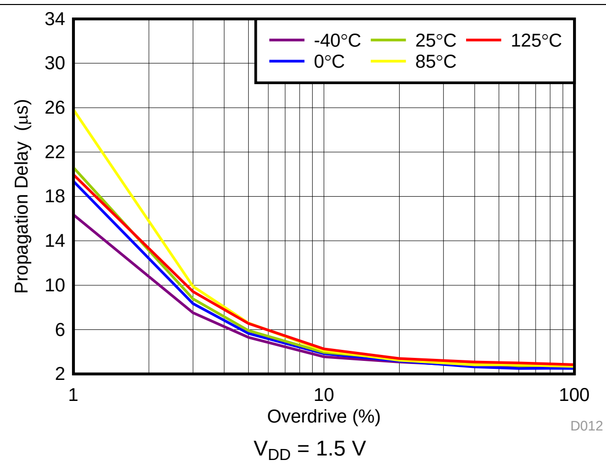


図 16. Propagation Delay ($t_{PD(f)}$) vs Overdrive

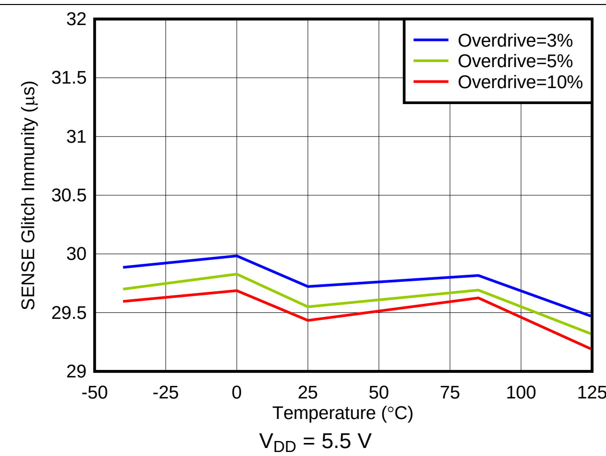


図 17. Low-to-High Glitch Immunity vs Temperature

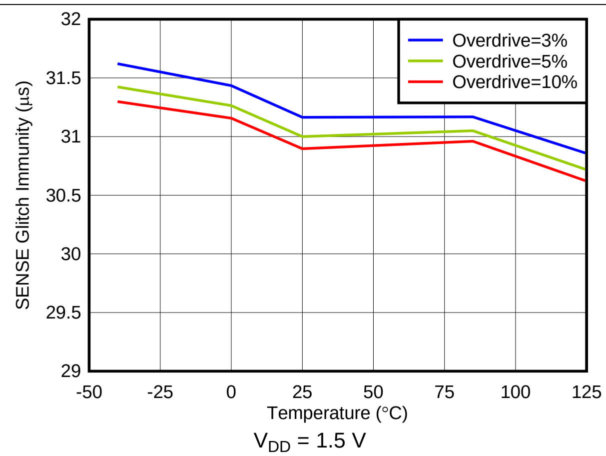


図 18. Low-to-High Glitch Immunity vs Temperature

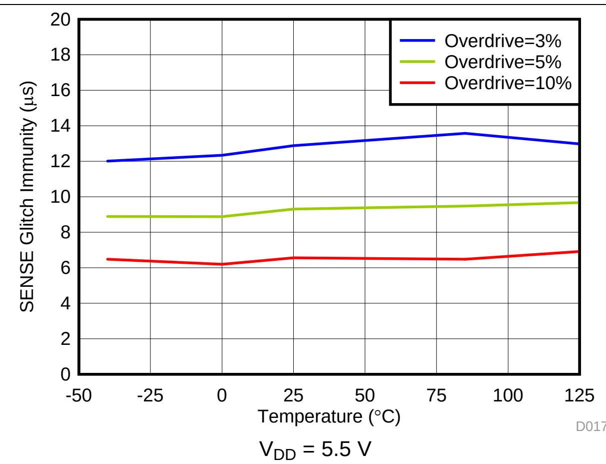
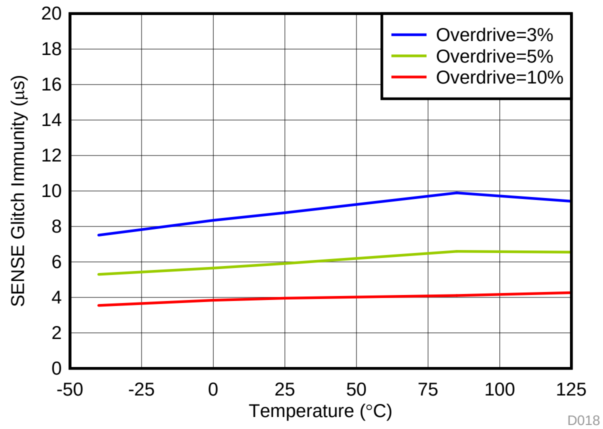


図 19. High-to-Low Glitch Immunity vs Temperature

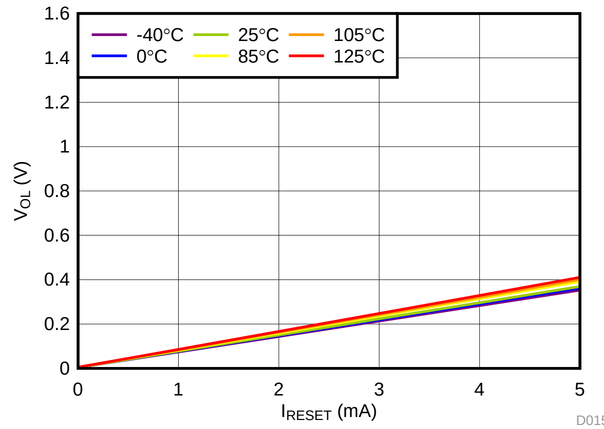
Typical Characteristics (continued)

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR}$ = V_{DD} (unless otherwise noted)



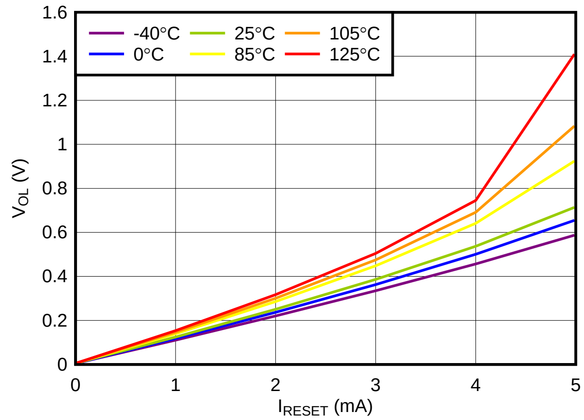
V_{DD} = 1.5 V

図 20. High-to-Low Glitch Immunity vs Temperature



V_{DD} = 5.5 V

図 21. Low-Level Output Voltage vs RESET Current



V_{DD} = 1.5 V

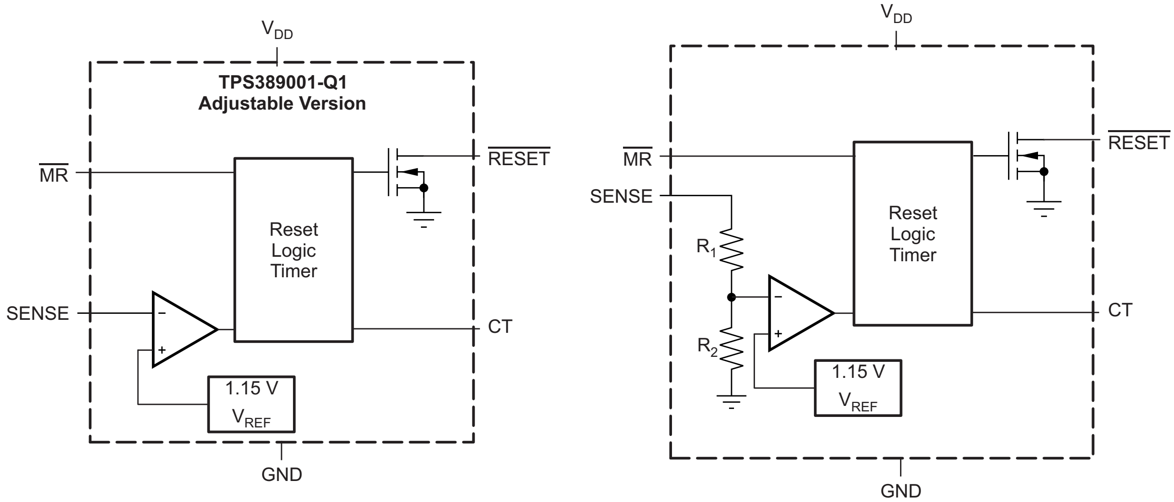
図 22. Low-Level Output Voltage vs RESET Current

8 Detailed Description

8.1 Overview

The TPS3890-Q1 supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{ITN} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above their respective thresholds.

8.2 Functional Block Diagram



Adjustable Voltage Version

Fixed Voltage Version

8.3 Feature Description

The combination of user-adjustable reset delay time with a broad range of threshold voltages allow these devices to be used in a wide array of applications. Fixed negative threshold voltages (V_{ITN}) can be factory set from 1.15 V to 3.17 V (see the *Device Comparison Table* for available options), and the adjustable device can be used to customize the threshold voltage for other application needs by using an external resistor divider. The CT pin allows the reset delay to be set between 25 µs and 30 s with the use of an external capacitor.

8.3.1 User-Configurable $\overline{\text{RESET}}$ Delay Time

The rising $\overline{\text{RESET}}$ delay time ($t_{PD(r)}$) can be configured by installing a capacitor connected to the CT pin. The TPS3890-Q1 uses a CT pin charging current (I_{CT}) of 1.15 µA to help counter the effect of capacitor and board-level leakage currents that can be substantial in certain applications. The rising $\overline{\text{RESET}}$ delay time can be set to any value between 25 µs (no C_{CT} installed) and 30 s (C_{CT} = 26 µF).

The capacitor value needed for a given delay time can be calculated using 式 1:

$$t_{PD(r)}\ (\text{sec}) = C_{CT} \times V_{CT} \div I_{CT} + t_{PD(r)(nom)} \tag{1}$$

The slope of 式 1 is determined by the time that the CT charging current (I_{CT}) takes to charge the external capacitor up to the CT comparator threshold voltage (V_{CT}). When $\overline{\text{RESET}}$ is asserted, the capacitor is discharged through the internal CT pulldown resistor (R_{CT}). When the $\overline{\text{RESET}}$ conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor and when the voltage on this capacitor reaches 1.22 V, $\overline{\text{RESET}}$ is deasserted. Note that in order to minimize the difference between the calculated $\overline{\text{RESET}}$ delay time and the actual $\overline{\text{RESET}}$ delay time, use a low-leakage type capacitor (such as a ceramic capacitor) and minimize parasitic board capacitance around this pin.

Feature Description (continued)

8.3.2 Manual Reset ($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above V_{ITP}, $\overline{\text{RESET}}$ is deasserted after the user-defined reset delay. If $\overline{\text{MR}}$ is not controlled externally, then $\overline{\text{MR}}$ must be connected to VDD. Note that if the logic signal driving $\overline{\text{MR}}$ is not greater than or equal to V_{DD}, then some additional current flows into VDD and out of $\overline{\text{MR}}$ and the difference is apparent when comparing 図 8 and 図 9.

図 23 shows how $\overline{\text{MR}}$ can be used to monitor multiple system voltages when only a single CT capacitor is needed to set the $\overline{\text{RESET}}$ delay time.

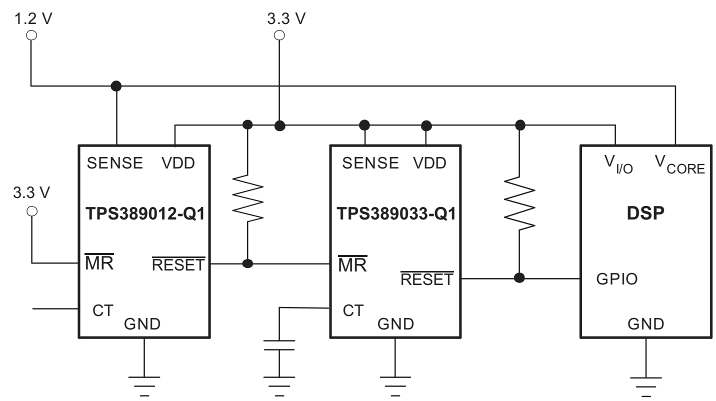


図 23. Using $\overline{\text{MR}}$ to Monitor Multiple System Voltages

8.3.3 $\overline{\text{RESET}}$ Output

$\overline{\text{RESET}}$ remains high (deasserted) as long as SENSE is above the positive threshold (V_{ITP}) and the manual reset signal ($\overline{\text{MR}}$) is logic high. If SENSE falls below the negative threshold (V_{ITN}) or if $\overline{\text{MR}}$ is driven low, then $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to a low impedance.

When $\overline{\text{MR}}$ is again logic high and SENSE is above V_{ITP}, a delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period ($t_{PD(r)}$). When the reset delay has elapsed, the $\overline{\text{RESET}}$ pin goes to a high-impedance state and uses a pullup resistor to hold $\overline{\text{RESET}}$ high. Connect the pullup resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level. $\overline{\text{RESET}}$ can be pulled up to any voltage up to 5.5 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by V_{OL}, the output capacitive loading, and the output leakage current ($I_{LKG(OD)}$).

8.3.4 SENSE Input

The SENSE input can vary from ground to 5.5 V (7.0 V, absolute maximum), regardless of the device supply voltage used. The SENSE pin is used to monitor the critical voltage rail. If the voltage on this pin drops below V_{ITN}, then $\overline{\text{RESET}}$ is asserted. When the voltage on the SENSE pin exceeds the positive threshold voltage, $\overline{\text{RESET}}$ deasserts after the user-defined $\overline{\text{RESET}}$ delay time.

The internal comparator has built-in hysteresis to ensure well-defined $\overline{\text{RESET}}$ assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3890-Q1 device is relatively immune to short transients on the SENSE pin. Glitch immunity is dependent on threshold overdrive, as illustrated in 図 19 for V_{ITN} and 図 18 for V_{ITP}. Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

Feature Description (continued)

The adjustable version (TPS389001-Q1) can be used to monitor any voltage rail down to 1.15 V using the circuit shown in 図 24.

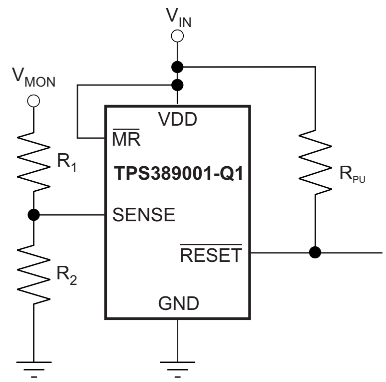


図 24. Using the TPS389001-Q1 to Monitor a User-Defined Threshold Voltage

The target threshold voltage for the monitored supply ($V_{ITx(MON)}$) and the resistor divider values can be calculated by using 式 2 and 式 3, respectively:

$$V_{ITx(MON)} = V_{ITx} \times (1 + R_1 \div R_2) \quad (2)$$

式 3 can be used to calculate either the negative threshold or the positive threshold by replacing V_{ITx} with either V_{ITN} or V_{ITP}, respectively.

$$R_{TOTAL} = R_1 + R_2 \quad (3)$$

Resistors with high values minimize current consumption; however, the input bias current of the device degrades accuracy if the current through the resistors is too low. Therefore, choosing an R_{TOTAL} value so that the current through the resistor divider is at least 100 times larger than the SENSE input current is simplest. See the *Optimizing Resistor Dividers at a Comparator Input* application report for more details on sizing input resistors.

8.3.4.1 Immunity to SENSE Pin Voltage Transients

The TPS3890-Q1 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient. Overdrive is defined by how much VSENSE exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs (that is, undervoltage and overvoltage). Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 4.

$$\text{Overdrive} = | (V_{SENSE} / V_{ITx} – 1) \times 100\% | \quad (4)$$

図 17 to 図 20 illustrate the glitch immunity that the TPS3890-Q1 has versus temperature with three different overdrive voltages. The propagation delay versus overdrive curves (図 13 to 図 16) can be used to determine how sensitive the TPS3890-Q1 family of devices are across an even wider range of overdrive voltages.

8.4 Device Functional Modes

表 1 summarizes the various functional modes of the device.

表 1. Truth Table

V_{DD}	$\overline{\text{MR}}$	SENSE	$\overline{\text{RESET}}$
$V_{DD} < V_{POR}$	—	—	Undefined
$V_{POR} < V_{DD} < V_{DD(MIN)}$ (1)	—	—	L
$V_{DD} \geq V_{DD(MIN)}$	L	—	L
$V_{DD} \geq V_{DD(MIN)}$	H	$V_{SENSE} < V_{ITN}$	L
$V_{DD} \geq V_{DD(MIN)}$	H	$V_{SENSE} > V_{ITP}$	H

(1) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and $\overline{\text{RESET}}$ is held low until V_{DD} falls below V_{POR}.

8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{\text{RESET}}$ signal is determined by the voltage on the SENSE pin and the logic state of $\overline{\text{MR}}$.

- $\overline{\text{MR}}$ high: when the voltage on VDD is greater than 1.5 V, the $\overline{\text{RESET}}$ signal corresponds to the voltage on the SENSE pin relative to the threshold voltage.
- $\overline{\text{MR}}$ low: in this mode, $\overline{\text{RESET}}$ is held low regardless of the voltage on the SENSE pin.

8.4.2 Above Power-On-Reset But Less Than $V_{DD(min)}$ ($V_{POR} < V_{DD} < V_{DD(min)}$)

When the voltage on VDD is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage (V_{POR}), the $\overline{\text{RESET}}$ signal is asserted regardless of the voltage on the SENSE pin.

8.4.3 Below Power-On-Reset ($V_{DD} < V_{POR}$)

When the voltage on VDD is lower thanV_{POR}, the device does not have enough voltage to internally pull the asserted output low and $\overline{\text{RESET}}$ is undefined and must not be relied upon for proper device function.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

A typical application for the TPS389018-Q1 is shown in 図 25. The TPS389018-Q1 can be used to monitor the 1.8-V VDD rail required by the TI Delfino™ microprocessor family. The open-drain $\overline{\text{RESET}}$ output of the TPS389018-Q1 is connected to the $\overline{\text{XRS}}$ input of the microprocessor. A reset event is initiated when the VDD voltage is less than V_{ITN} or when $\overline{\text{MR}}$ is driven low by an external source.

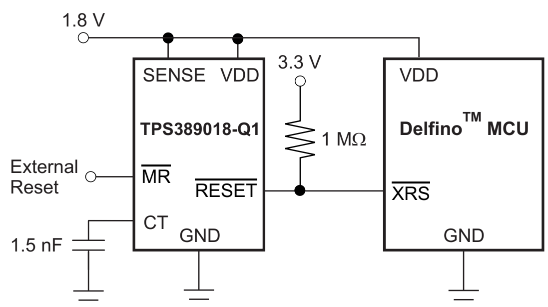


図 25. TPS3890-Q1 Monitoring the Supply Voltage for a Delfino Microprocessor

9.2.1 Design Requirements

The TPS3890-Q1 $\overline{\text{RESET}}$ output can be used to drive the reset ($\overline{\text{XRS}}$) input of a microprocessor. The $\overline{\text{RESET}}$ pin of the TPS3890-Q1 is pulled high with a 1-MΩ resistor; the reset delay time is controlled by the CT capacitor and is set depending on the reset requirement times of the microprocessor. During power-up, $\overline{\text{XRS}}$ must remain low for at least 1 ms after VDD reaches 1.5 V for the C2000™ Delfino family of microprocessors. For 100-MHz operation, the Delfino TMS320F2833x microcontroller uses a supply voltage of 1.8 V that must be monitored by the TPS3890-Q1.

9.2.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS389018-Q1 has a negative threshold of 1.73 V and a positive threshold of 1.74 V, making the device suitable for monitoring a 1.8-V rail. The secondary constraint for this application is the reset delay time that must be at least 1 ms to allow the Delfino microprocessor enough time to startup up correctly. Because a minimum time is required, the worst-case scenario is a supervisor with a high CT charging current (I_{CT}) and a low CT comparator threshold (V_{CT}). For applications with ambient temperatures ranging from –40°C to +125°C, C_{CT} can be calculated using $I_{CT(Max)}$, $V_{CT(MIN)}$, and solving for C_{CT} in 式 1 such that the minimum capacitance required at the CT pin is 1.149 nF. If standard capacitors with ±20% tolerances are used, then the CT capacitor must be 1.5 nF or larger to ensure that the 1-ms delay time is met.

A 0.1-µF decoupling capacitor is connected to the VDD pin as a good analog design practice and a 1-MΩ resistor is used as the $\overline{\text{RESET}}$ pullup resistor to minimize the current consumption when $\overline{\text{RESET}}$ is asserted. The $\overline{\text{MR}}$ pin can be connected to an external signal if desired or connected to VDD if not used.

Typical Application (continued)

9.2.3 Application Curve

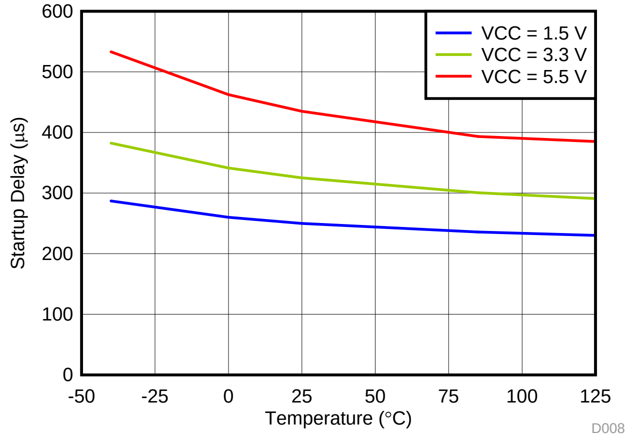


図 26. Startup Delay vs Temperature

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.5 V and 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor near the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the RESET delay time is not adversely affected.

11.2 Layout Example

The layout example in shows how the TPS3890-Q1 is laid out on a printed circuit board (PCB) with a user-defined delay.

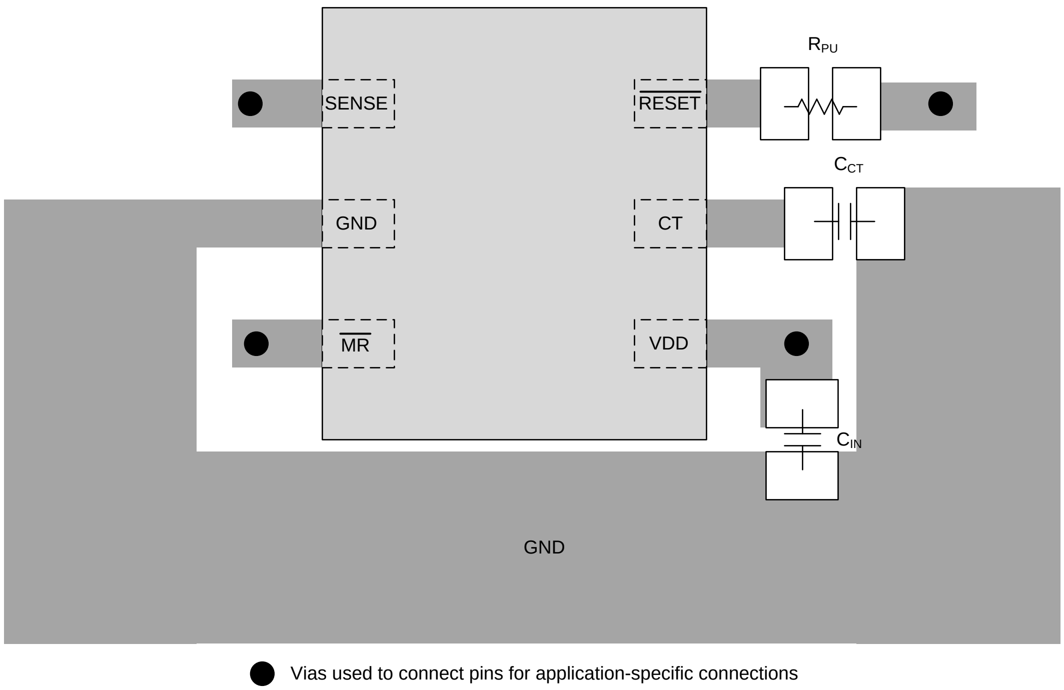


図 27. Recommended Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

表 2 は、TPS389033G-Q1を例として、部品番号からデバイスの機能を解読する方法を示しています。

表 2. デバイスの命名規則

説明	項目表記	値
TPS3890 (高精度のスーパバイザ・ファミリ)	—	—
33 (監視対象の公称レール電圧)	10	1.0V
	12	1.2V
	18	1.8V
	33	3.3V
	50	5.0V
G (V_{ITN}が公称レール電圧の何%下か)	—	4%
	G	7%
	K	11%
	L	12%
Q1 (車載用バージョン)	—	—

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- *『コンパレータ入力の分圧抵抗の最適化』*
- *『電源設計用の感度分析』*
- *『TMS320C28xデジタル信号コントローラの基礎』*
- *『TPS3890EVM-775評価モジュール・ユーザー・ガイド』*
- 『C2000 Delfinoファミリのマイクロプロセッサ』
- *『TMS320F2833xデジタル信号コントローラ(DCS)』*

12.3 ドキュメントの更新通知を受け取る方法

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12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.5 商標

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12.6 静電気放電に関する注意事項

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS389001QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2N
TPS389001QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2N
TPS389012QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2O
TPS389012QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2O
TPS389015QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2P
TPS389015QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2P
TPS389018QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Q
TPS389018QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Q
TPS389025QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2R
TPS389025QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2R
TPS389030QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2S
TPS389030QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2S
TPS389033GQDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7V
TPS389033GQDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7V
TPS389033KQDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7W
TPS389033KQDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7W
TPS389033QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2T
TPS389033QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2T
TPS389050GQDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7T
TPS389050GQDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7T
TPS389050LQDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7U
TPS389050LQDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7U
TPS389050QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7S
TPS389050QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS3890-Q1 :

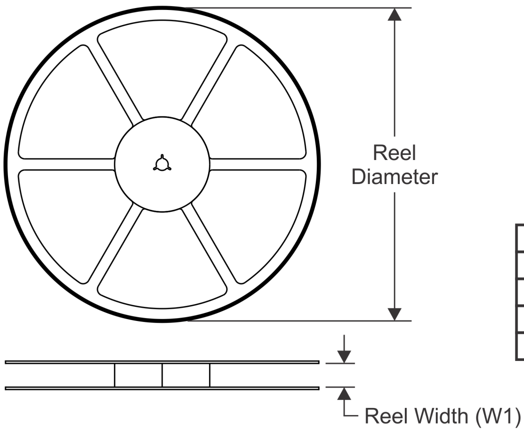
- Catalog : TPS3890

NOTE: Qualified Version Definitions:

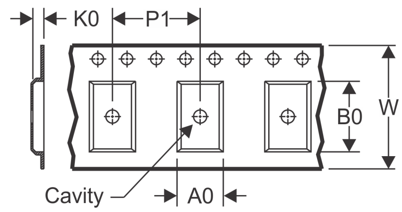
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

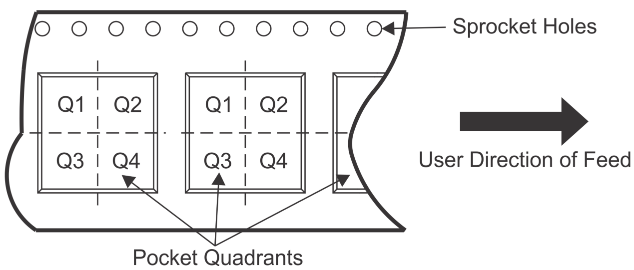


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

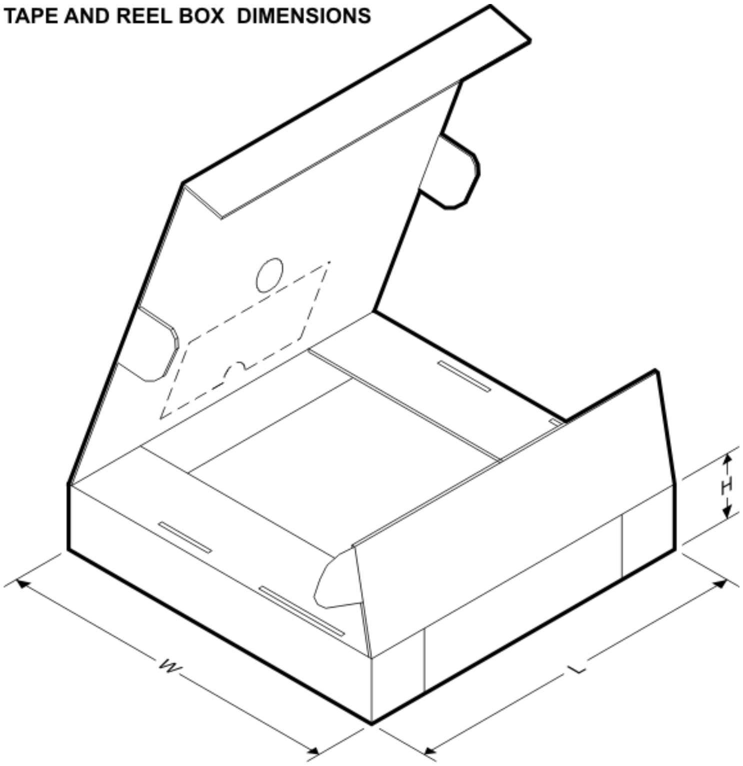
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

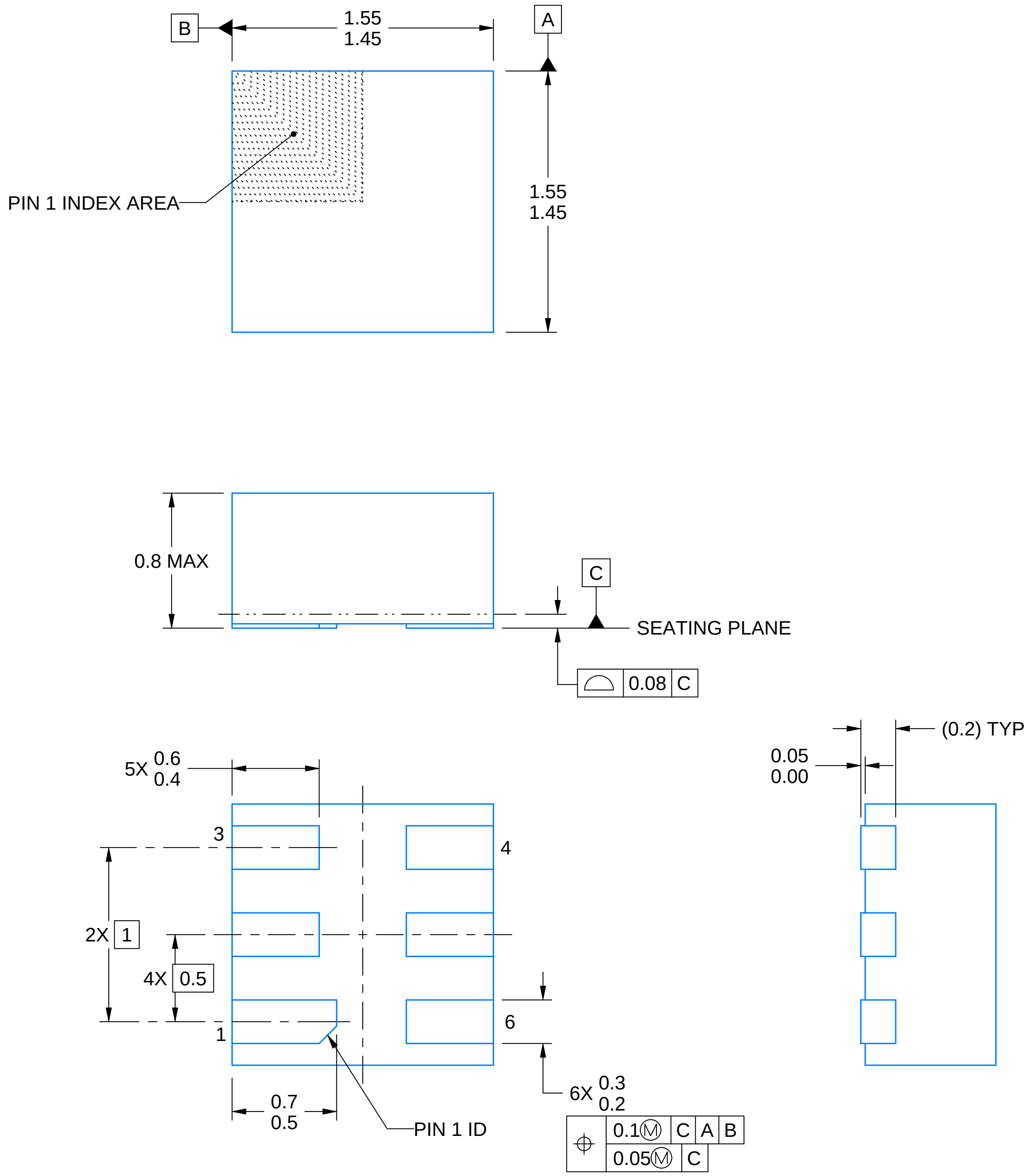
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS389001QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389012QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389015QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389018QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389025QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389030QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033GQDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033KQDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389050GQDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389050LQDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389050QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS389001QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389012QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389015QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389018QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389025QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389030QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389033GQDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389033KQDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389033QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389050GQDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389050LQDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389050QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0



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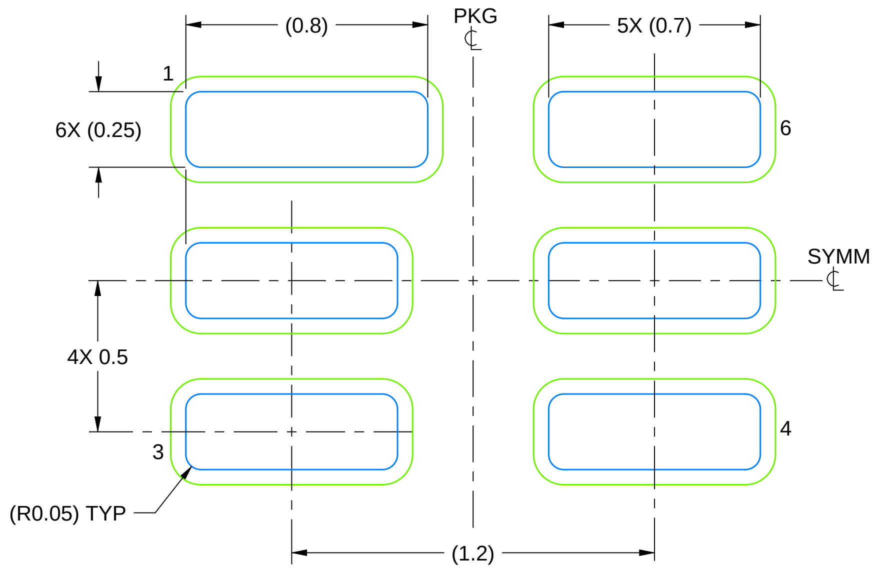
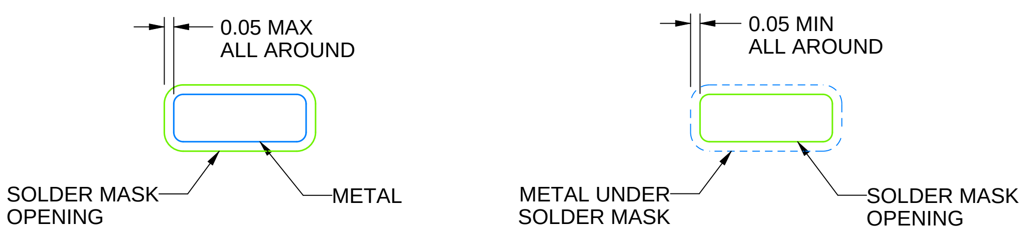
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



PADS 4-6
NON SOLDER MASK
DEFINED

PADS 1-3
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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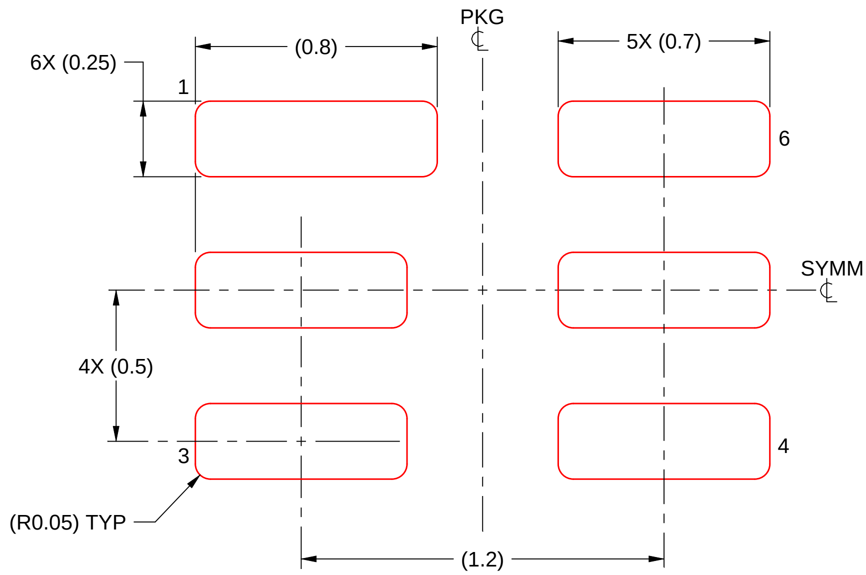
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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