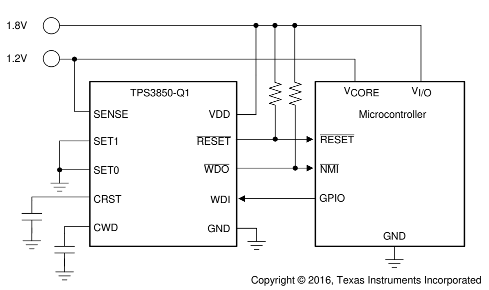
TPS3850-Q1 プログラマブル・ウィンドウ・ウォッチドッグ・タイマ内蔵の高精度電圧監視 IC

1 特長

- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1：–40℃～125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 入力電圧範囲：V_{DD} = 1.6V～6.5V
- 0.8% の電圧スレッショルド精度 (最大)
- 低消費電流：I_{DD} = 10μA (標準値)
- ウォッチドッグのタイムアウトをユーザーがプログラム可能
- リセット遅延をユーザーがプログラム可能
- 高精度のウォッチドッグおよびリセット・タイマを製造時にプログラム可能
- オープン・ドレイン出力
- 高精度の過電圧および低電圧監視
  - 0.9V～5.0V の共通レールをサポート
  - 4% および 7% のフォルト・ウィンドウを利用可能
  - 0.5% のヒステリシス
- ウォッチドッグのディスエーブル機能
- 3mm × 3mm の小型 10 ピン VSON パッケージで供給

2 アプリケーション

- オンボード・チャージャ (OBC) / ワイヤレス・チャージャ
- ドライバー監視
- デジタル・コックピット処理装置
- ADAS ドメイン・コントローラ
- 車載テレマティクス制御ユニット



代表的なアプリケーション回路

3 概要

TPS3850-Q1 は、高精度の電圧スーパーバイザとプログラム可能なウィンドウ・ウォッチドッグ・タイマを組み合わせた製品です。TPS3850-Q1 のウィンドウ・コンパレータは、SENSE ピンの過電圧 ($V_{IT+(OV)}$) および低電圧 ($V_{IT–(UV)}$) スレッショルドの両方について 0.8% の精度 (–40℃～+125℃) を達成しています。また、TPS3850-Q1 には両方のスレッショルドについて高精度のヒステリシスが含まれており、許容誤差の厳しいシステムに理想的です。スーパーバイザの $\overline{\text{RESET}}$ 遅延は、工場でプログラムされたデフォルト遅延設定を使用することも、外付けコンデンサによりプログラムすることもできます。工場でプログラムされる $\overline{\text{RESET}}$ 遅延は 9.5% の精度で、高精度の遅延タイミングです。

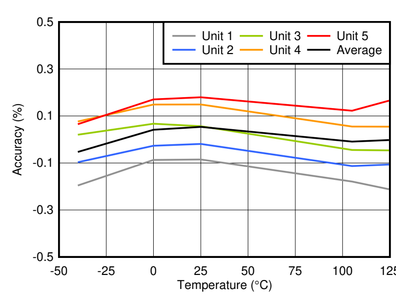
TPS3850-Q1 にはプログラム可能なウィンドウ・ウォッチドッグ・タイマが内蔵されており、広範なアプリケーションに使用できます。専用ウォッチドッグ出力 ($\overline{\text{WDO}}$) により分解能が向上し、フォルト状況の性質を判定するために役立ちます。ウィンドウ・ウォッチドッグのタイムアウトは、工場でプログラムされたデフォルト遅延設定を使用することも、外付けコンデンサによりプログラムすることもできます。ウォッチドッグはロジック・ピンによりディスエーブルできるため、開発プロセスにおいて望ましくないウォッチドッグのタイムアウトを回避できます。

TPS3850-Q1 は、小型の 3.00mm × 3.00mm、10 ピンの VSON パッケージで供給されます。
TPS3850-Q1 では、光学検査を容易にするウェッタブル・フランクを採用しています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS3850-Q1	VSON (10)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



過電圧スレッショルド ($V_{IT+(OV)}$) の精度と温度との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (April 2017) to Revision B (July 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 「±15% 精度の WDT および RST 遅延」を削除	1
• 「機能安全対応」の箇条書き項目を追加	1
• Web サイトにリンクするようにアプリケーションを更新	1
• 分かりやすくするために「SENSE ピンの」を追加	1
• Updated ESD Ratings	4
• Changed I_{CWD} min and max spec	5
• Changed V_{CWD} min and max spec	5
• Added a footnote to for t_{INIT}	6
• Created a separate section for Timing Diagram	7
• Added explanation about capacitors for tWDU.	24
• Changed minimum and maximum limits on t_{WDU} from 0.85 and 1.15 to 0.905 and 1.095 respectively	24
• Changed 0.85 to 0.905 in Equation 14 and 1.15 to 1.05 in Equation 15	31

Changes from Revision * (January 2017) to Revision A (April 2017)	Page
• Changed 0.000381 to 0.000324 in Equation 11	28
• Changed Equation 17 and Equation 18 so that I_{SENSE} is no longer in the denominator	32
• Deleted J row from *Device Nomenclature* table	35

5 Pin Configuration and Functions

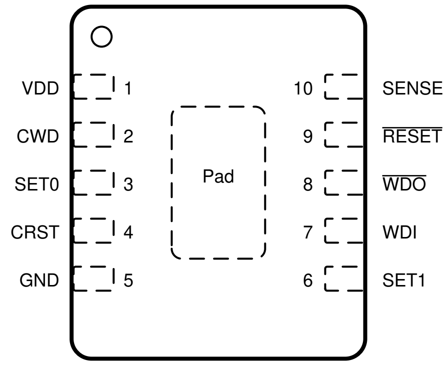


図 5-1. DRC Package 3-mm × 3-mm VSON-10 Top View

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	I/O	
CRST	4	I	Programmable reset timeout pin. Connect a capacitor between this pin and GND to program the reset timeout period. This pin can also be connected by a 10-kΩ pullup resistor to VDD, or left unconnected (NC) for various factory-programmed reset timeout options; see the *CRST Delay* section. When using an external capacitor, use 式 3 to determine the reset timeout.
CWD	2	I	Programmable watchdog timeout input. Watchdog timeout is set by connecting a capacitor between this pin and ground. Furthermore, this pin can also be connected by a 10-kΩ resistor to VDD, or leaving unconnected (NC) further enables the selection of the preset watchdog timeouts; see the *セクション 6.6* table. When using a capacitor, the TPS3850-Q1 determines the window watchdog upper boundary with 式 6. The lower watchdog boundary is set by the SET pins, see 表 8-5 and the *CWD Functionality* section for additional information.
GND	5	—	Ground pin
$\overline{\text{RESET}}$	9	O	Reset output. Connect $\overline{\text{RESET}}$ using a 1-kΩ to 100-kΩ resistor to VDD. $\overline{\text{RESET}}$ goes low when the voltage at the SENSE pin goes below the undervoltage threshold ($V_{IT-(UV)}$) or above the overvoltage threshold ($V_{IT+(OV)}$). When the voltage level at the SENSE pin is within the normal operating range, the $\overline{\text{RESET}}$ timeout counter starts. At timer completion, $\overline{\text{RESET}}$ goes high. During startup, the state of $\overline{\text{RESET}}$ is undefined below the specified power-on-reset voltage (V_{POR}). Above V_{POR}, $\overline{\text{RESET}}$ goes low and remains low until the monitored voltage is within the correct operating range (between $V_{IT-(UV)}$ and $V_{IT(+OV)}$) and the $\overline{\text{RESET}}$ timeout is complete.
SENSE	10	I	SENSE input to monitor the voltage rail. Connect this pin to the supply rail that must be monitored.
SET0	3	I	Logic input. SET0, SET1, and CWD select the watchdog window ratios, timeouts, and disable the watchdog; see the *セクション 6.6* table.
SET1	6	I	Logic input. SET0, SET1, and CWD select the watchdog window ratios, timeouts, and disable the watchdog; see the *セクション 6.6* table.
VDD	1	I	Supply voltage pin. For noisy systems, connecting a 0.1-µF bypass capacitor is recommended.
WDI	7	I	Watchdog input. A falling transition (edge) must occur at this pin between the lower ($t_{WDL(max)}$) and upper ($t_{WDU(min)}$) window boundaries in order for $\overline{\text{WDO}}$ to not assert. When the watchdog is not in use, the SETx pins can be used to disable the watchdog. The input at WDI is ignored when $\overline{\text{RESET}}$ or $\overline{\text{WDO}}$ are low (asserted) and also when the watchdog is disabled. If the watchdog is disabled, then WDI cannot be left unconnected and must be driven to either VDD or GND.
$\overline{\text{WDO}}$	8	O	Watchdog output. Connect $\overline{\text{WDO}}$ with a 1-kΩ to 100-kΩ resistor to VDD. $\overline{\text{WDO}}$ goes low (asserts) when a watchdog timeout occurs. $\overline{\text{WDO}}$ only asserts when $\overline{\text{RESET}}$ is high. When a watchdog timeout occurs, $\overline{\text{WDO}}$ goes low (asserts) for the set $\overline{\text{RESET}}$ timeout delay (t_{RST}). When $\overline{\text{RESET}}$ goes low, $\overline{\text{WDO}}$ is in a high-impedance state.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	7	V
Output voltage	$\overline{\text{RESET}}$, $\overline{\text{WDO}}$	–0.3	7	V
Voltage ranges	SET0, SET1, WDI, SENSE	–0.3	7	V
	CWD, CRST	–0.3	VDD + 0.3(3)	
Output pin current	$\overline{\text{RESET}}$, $\overline{\text{WDO}}$		±20	mA
Input current (all pins)			±20	mA
Continuous total power dissipation		See *セクション 6.4*		
Temperature	Operating junction, T_J (2)	–40	150	°C
	Operating free-air, T_A (2)	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $T_J = T_A$ as a result of the low dissipated power in this device.
(3) The absolute maximum rating is V_{DD} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply pin voltage	1.6		6.5	V
V_{SENSE}	Input pin voltage	0		6.5	V
V_{SET0}	SET0 pin voltage	0		6.5	V
V_{SET1}	SET1 pin voltage	0		6.5	V
C_{CRST}	$\overline{\text{RESET}}$ delay capacitor	0.1(1)		1000(1)	nF
CRST	Pullup resistor to VDD	9	10	11	kΩ
C_{CWD}	Watchdog timing capacitor	0.1(2)		1000(2)	nF
CWD	Pullup resistor to VDD	9	10	11	kΩ
R_{PU}	Pullup resistor, $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$	1	10	100	kΩ
I_{RST}	$\overline{\text{RESET}}$ pin current			10	mA
I_{WDO}	Watchdog output current			10	mA
T_J	Junction temperature	–40		125	°C

(1) Using a C_{CRST} capacitor of 0.1 nF or 1000 nF gives a reset delay of 703 µs or 3.22 seconds, respectively.
(2) Using a C_{CWD} capacitor of 0.1 nF or 1000 nF gives a $t_{WDU(typ)}$ of 62.74 ms or 77.45 seconds, respectively.

6.4 Thermal Information

THERMAL METRIC[1]		TPS3850-Q1	UNIT
		DRC (VSON)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at 1.6 V ≤ V_{DD} ≤ 6.5 V over the operating temperature range of –40°C ≤ T_A, T_J ≤ +125°C (unless otherwise noted); the open-drain pullup resistors are 10 kΩ for each output; typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
V_{DD} [1] [2] [3]	Supply voltage		1.6		6.5	V
I_{DD}	Supply current			10	19	µA
RESET FUNCTION						
V_{POR} [2]	Power-on-reset voltage	I_{RESET} = 15 µA, $V_{OL(MAX)}$ = 0.25 V			0.8	V
V_{UVLO} [1]	Undervoltage lockout voltage			1.35		V
$V_{IT+(OV)}$	Overvoltage SENSE threshold accuracy, entering $\overline{RESET}$		$V_{IT+(nom)}$–0.8%		$V_{IT+(nom)}$+0.8%	
$V_{IT-(UV)}$	Undervoltage SENSE threshold accuracy, entering $\overline{RESET}$		$V_{IT-(nom)}$–0.8%		$V_{IT-(nom)}$+0.8%	
$V_{IT(ADJ)}$	Falling SENSE threshold voltage, adjustable version only		0.3968	0.4	0.4032	V
V_{HYST}	Hysteresis voltage		0.2%	0.5%	0.8%	
I_{CRST}	CRST pin charge current	CRST = 0.5 V	337	375	413	nA
V_{CRST}	CRST pin threshold voltage		1.192	1.21	1.228	V
WINDOW WATCHDOG FUNCTION						
I_{CWD}	CWD pin charge current	CWD = 0.5 V	347	375	403	nA
V_{CWD}	CWD pin threshold voltage		1.196	1.21	1.224	V
V_{OL}	$\overline{RESET}$, $\overline{WDO}$ output low	VDD = 5 V, I_{SINK} = 3 mA			0.4	V
I_D	$\overline{RESET}$, $\overline{WDO}$ output leakage current	VDD = 1.6 V, $V_{\overline{RESET}}$, = $V_{\overline{WDO}}$ = 6.5 V			1	µA
V_{IL}	Low-level input voltage (SET0, SET1)				0.25	V
V_{IH}	High-level input voltage (SET0, SET1)		0.8			V
$V_{IL(WDI)}$	Low-level input voltage (WDI)				0.3 × V_{DD}	V
$V_{IH(WDI)}$	High-level input voltage (WDI)		0.8 × V_{DD}			V
I_{SENSE}	SENSE pin idle current	TPS3850Xyy(y), V_{SENSE} = 5.0 V, VDD = 3.3 V		2.1	2.5	µA
		TPS3850H01 only, V_{SENSE} = 5.0 V, VDD = 3.3 V	–50		50	nA

(1) When V_{DD} falls below V_{UVLO}, $\overline{RESET}$ is driven low.
(2) When V_{DD} falls below V_{POR}, $\overline{RESET}$ and $\overline{WDO}$ are undefined.
(3) During power-on, V_{DD} must be a minimum 1.6 V for at least 300 µs before the output corresponds to the SENSE voltage.

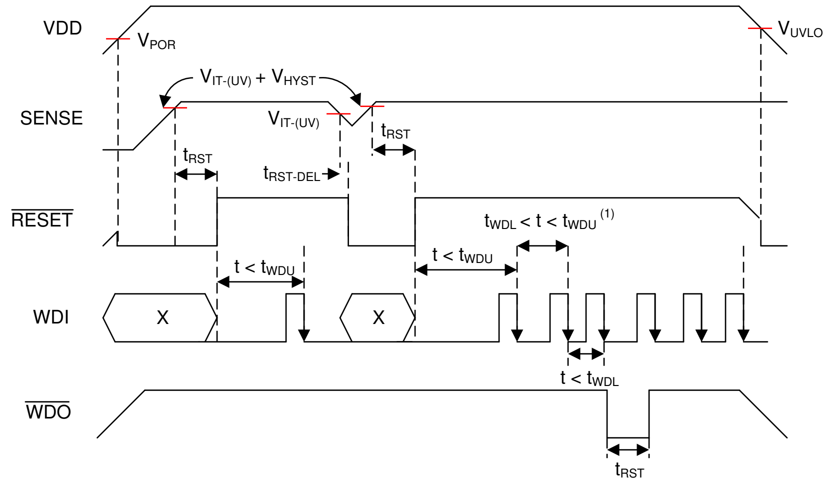
6.6 Timing Requirements

at 1.6 V ≤ V_{DD} ≤ 6.5 V over the operating temperature range of –40°C ≤ T_A, T_J ≤ +125°C (unless otherwise noted); the open-drain pullup resistors are 10 kΩ for each output; typical values are at T_J = 25°C

			MIN	TYP	MAX	UNIT
GENERAL						
t_{INIT}	CWD, CRST pin evaluation period[(1)]			381		µs
t_{SET}	Time required between changing the SET0 and SET1 pins			500		µs
	SET0, SET1 pin setup time			1		µs
	Startup delay[(2)]			300		µs
RESET FUNCTION						
t_{RST}	Reset timeout period	CRST = NC	170	200	230	ms
		CRST = 10 kΩ to VDD	8.5	10	11.5	ms
$t_{RST\text{-}DEL}$	V_{SENSE} to $\overline{\text{RESET}}$ delay	VDD = 5 V, V_{SENSE} = $V_{IT+(OV)}$ + 2.5%		35		µs
		VDD = 5 V, V_{SENSE} = $V_{IT-(UV)}$ – 2.5%		17		µs
WINDOW WATCHDOG FUNCTION						
WD ratio	Window watchdog ratio of lower boundary to upper boundary	CWD = programmable, SET0 = 0, SET1 = 0[(3)]		1/8		
		CWD = programmable, SET0 = 1, SET1 = 1[(3)]		1/2		
		CWD = programmable, SET0 = 0, SET1 = 1[(3)] [(4)]		3/4		
t_{WDL}	Window watchdog lower boundary	CWD = NC, SET0 = 0, SET1 = 0	19.1	22.5	25.9	ms
		CWD = NC, SET0 = 0, SET1 = 1	1.48	1.85	2.22	ms
		CWD = NC, SET0 = 1, SET1 = 0	Watchdog disabled			
		CWD = NC, SET0 = 1, SET1 = 1	680	800	920	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 0	7.65	9.0	10.35	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 1	7.65	9.0	10.35	ms
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 0	Watchdog disabled			
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 1	1.48	1.85	2.22	ms
t_{WDU}	Window watchdog upper boundary	CWD = NC, SET0 = 0, SET1 = 0	46.8	55.0	63.3	ms
		CWD = NC, SET0 = 0, SET1 = 1	23.375	27.5	31.625	ms
		CWD = NC, SET0 = 1, SET1 = 0	Watchdog disabled			
		CWD = NC, SET0 = 1, SET1 = 1	1360	1600	1840	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 0	92.7	109.0	125.4	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 1	165.8	195.0	224.3	ms
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 0	Watchdog disabled			
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 1	9.35	11.0	12.65	ms
$t_{WD\text{-}setup}$	Setup time required for the device to respond to changes on WDI after being enabled			150		µs
	Minimum WDI pulse duration			50		ns
$t_{WD\text{-}del}$	WDI to $\overline{\text{WDO}}$ delay			50		ns

(1) Refer to セクション 8.1.1.2
(2) During power-on, V_{DD} must be a minimum 1.6 V for at least 300 µs before the output corresponds to the SENSE voltage.
(3) 0 refers to V_{SET} ≤ V_{IL}, 1 refers to V_{SET} ≥ V_{IH}.
(4) If this watchdog ratio is used, then $t_{WDL(max)}$ can overlap $t_{WDU(min)}$.

6.7 Timing Diagrams



A. See 図 6-2 for WDI timing requirements.

図 6-1. Timing Diagram

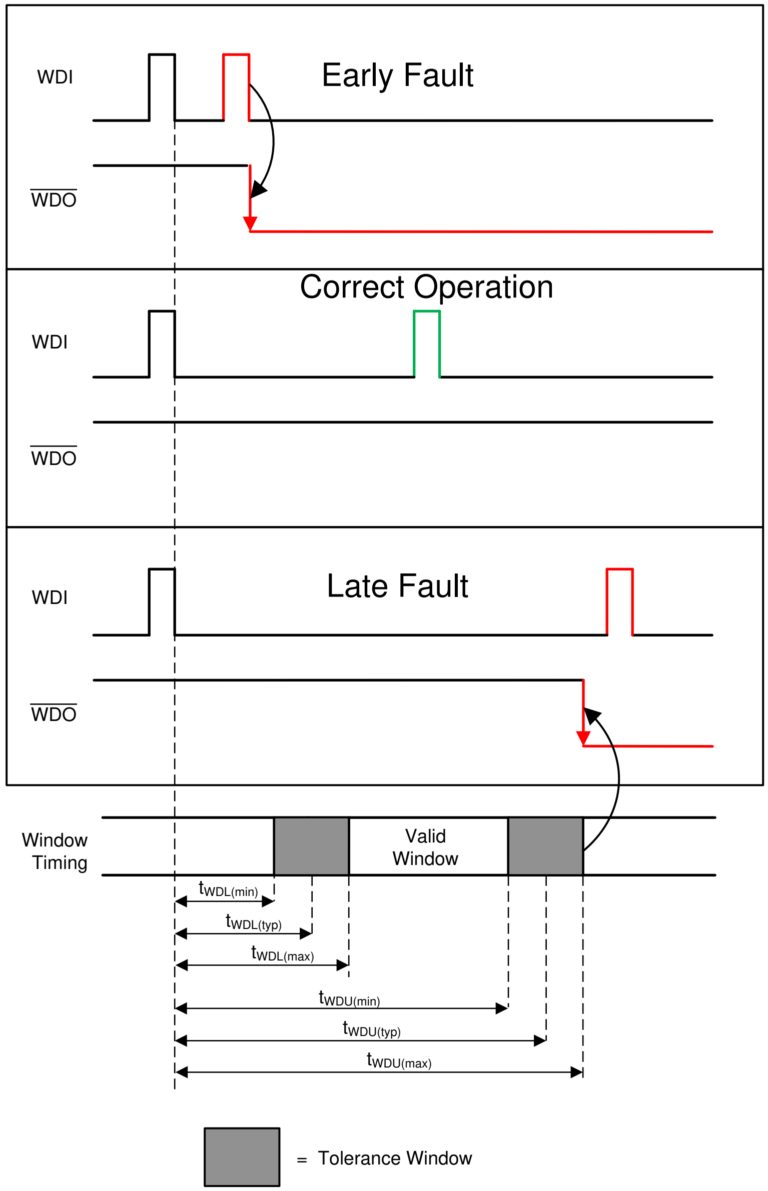


図 6-2. TPS3850-Q1 Window Watchdog Timing

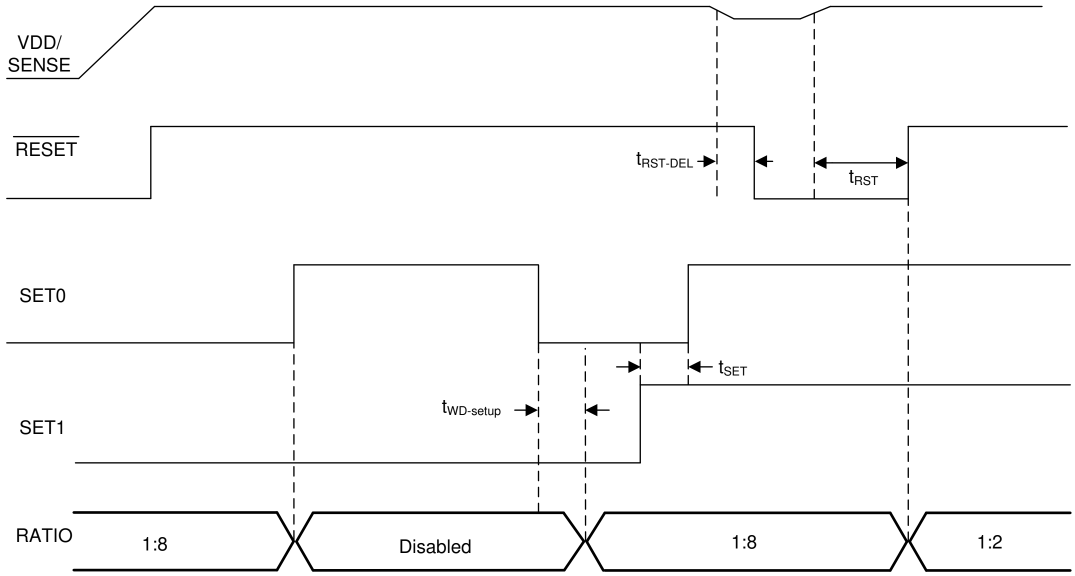


図 6-3. Changing SET0 and SET1 Pins

6.8 Typical Characteristics

all curves are taken at T_A = 25°C with 1.6 V ≤ V_{DD} ≤ 6.5 V (unless otherwise noted)

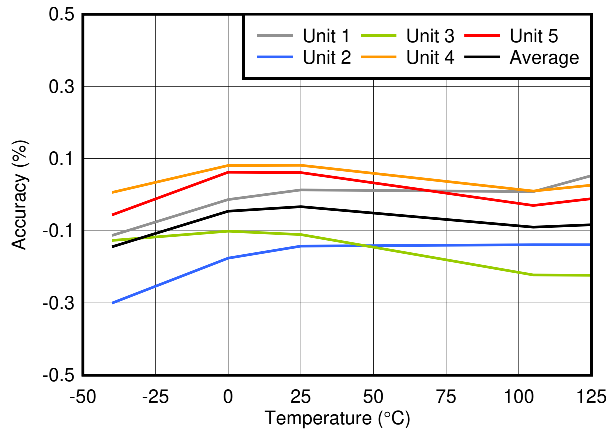


図 6-4. $V_{IT+(OV)}$ Accuracy vs Temperature

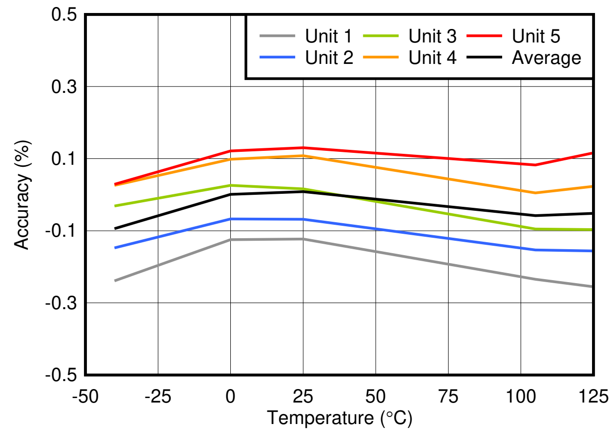


図 6-5. $V_{IT-(UV)}$ Accuracy vs Temperature

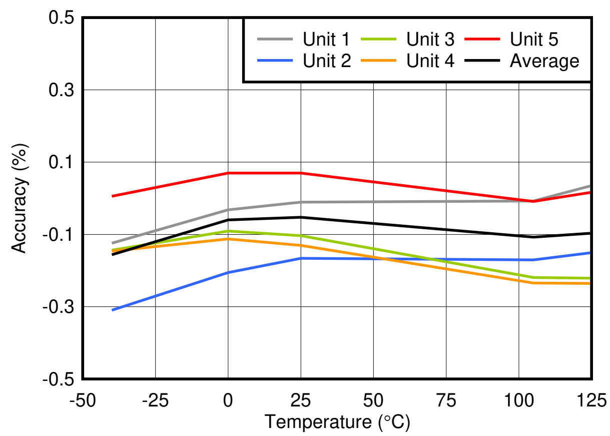


図 6-6. $V_{IT-(OV)}$ Accuracy vs Temperature

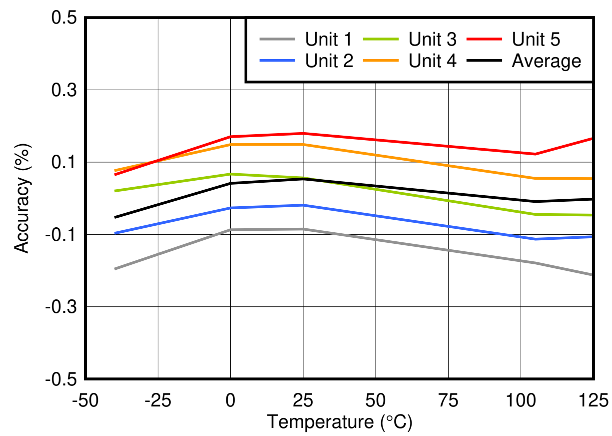
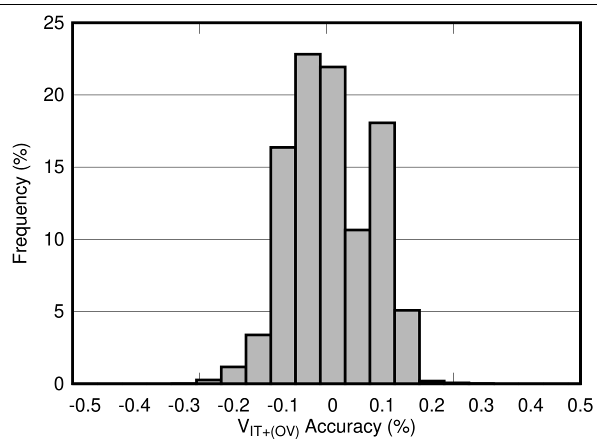
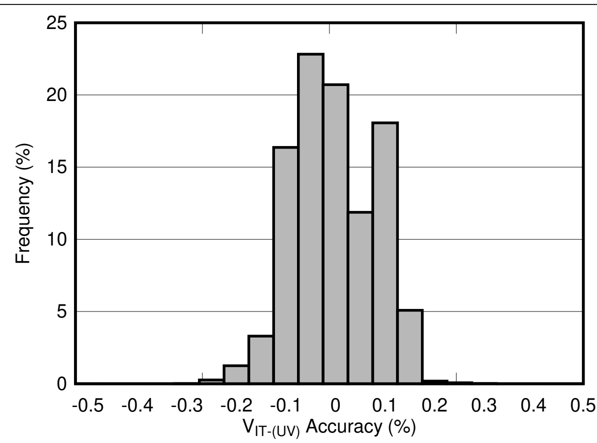


図 6-7. $V_{IT+(UV)}$ Accuracy vs Temperature



Includes G and H versions; with 1.2-V, 1.8-V, 3.0-V, 3.3-V, and 5-V thresholds; total units = 41,111

図 6-8. $V_{IT+(OV)}$ Accuracy Histogram



Includes G and H versions; with 1.2-V, 1.8-V, 3.0-V, 3.3-V, and 5-V thresholds; total units = 41,111

図 6-9. $V_{IT-(UV)}$ Accuracy Histogram

6.8 Typical Characteristics (continued)

all curves are taken at T_A = 25°C with 1.6 V ≤ V_{DD} ≤ 6.5 V (unless otherwise noted)

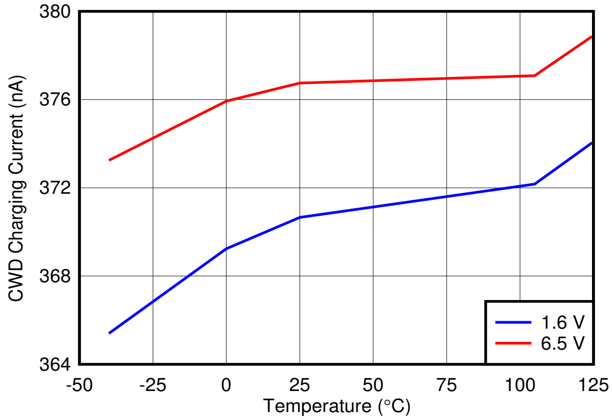


図 6-10. CWD Charging Current vs Temperature

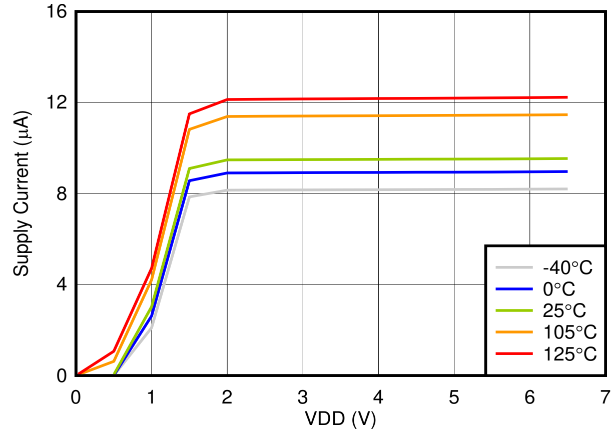
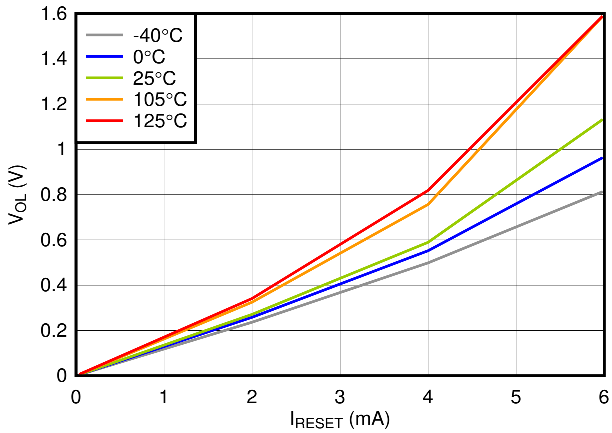
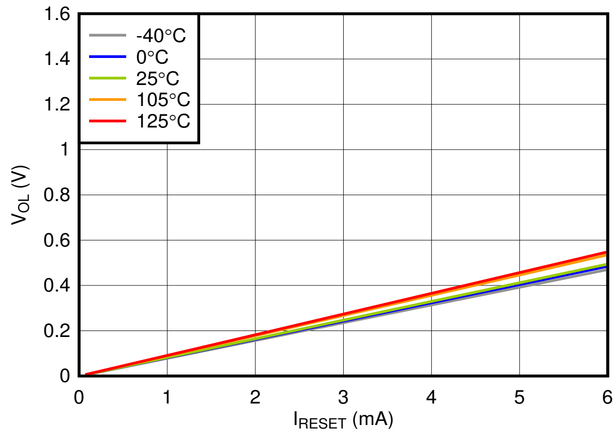


図 6-11. Supply Current vs Power-Supply Voltage



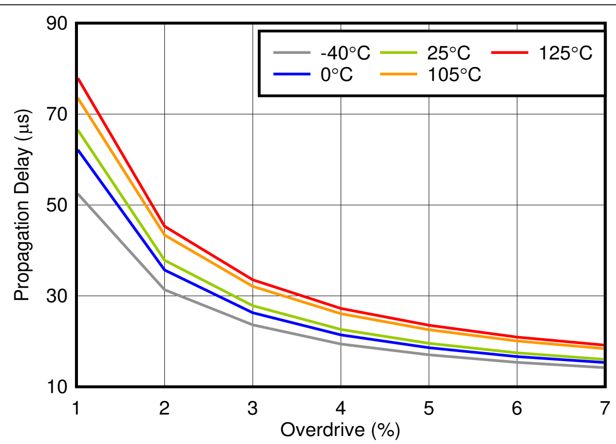
VDD = 1.6 V

図 6-12. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current



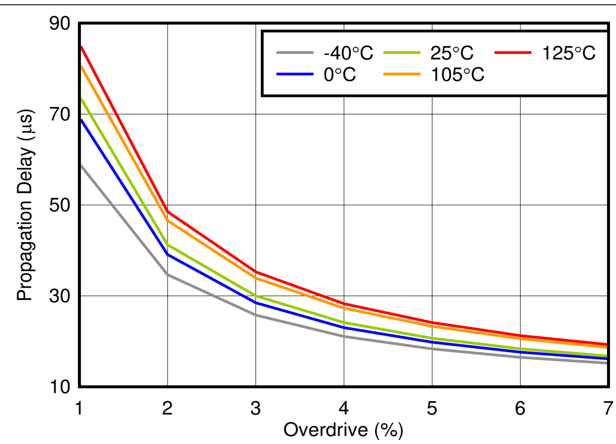
VDD = 6.5 V

図 6-13. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current



VDD = 1.6 V, $V_{IT+(OV)}$ = 0.936 V

図 6-14. Propagation Delay vs Overdrive



VDD = 6.5 V, $V_{IT+(OV)}$ = 0.936 V

図 6-15. Propagation Delay vs Overdrive

6.8 Typical Characteristics (continued)

all curves are taken at T_A = 25°C with 1.6 V ≤ V_{DD} ≤ 6.5 V (unless otherwise noted)

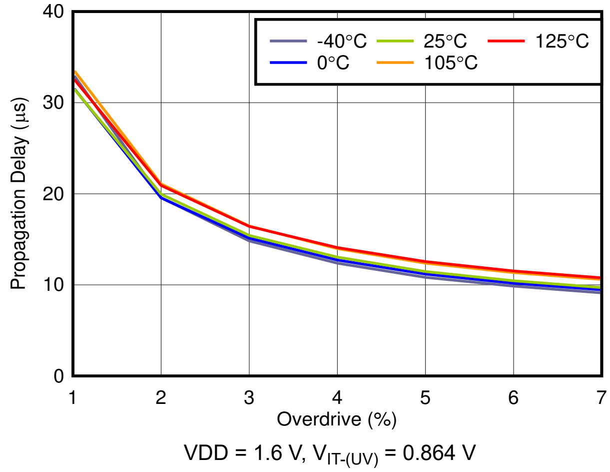


図 6-16. Propagation Delay vs Overdrive

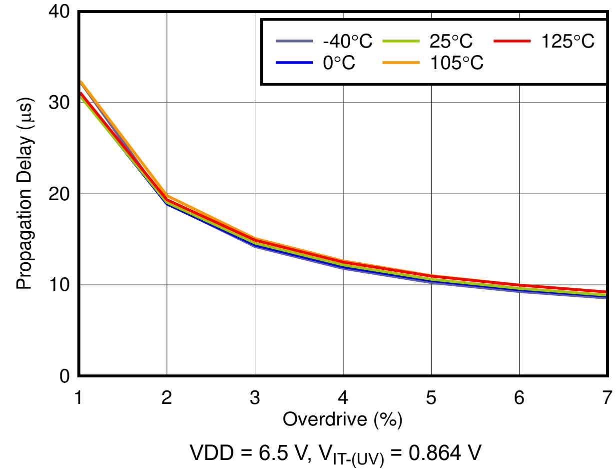


図 6-17. Propagation Delay vs Overdrive

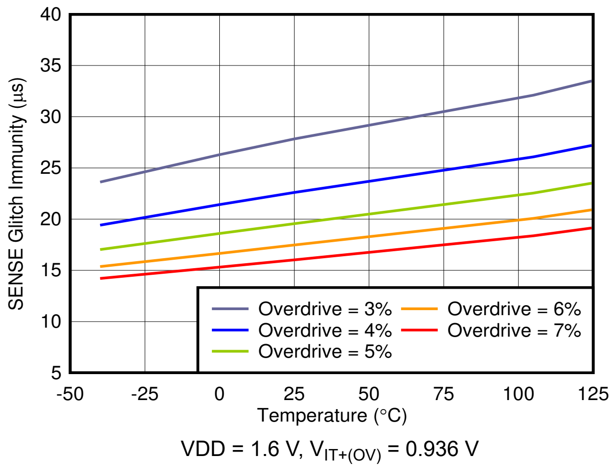


図 6-18. SENSE Glitch Immunity vs Temperature

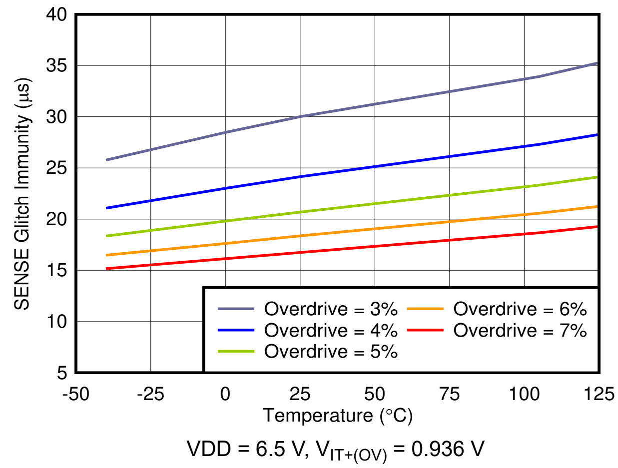


図 6-19. SENSE Glitch Immunity vs Temperature

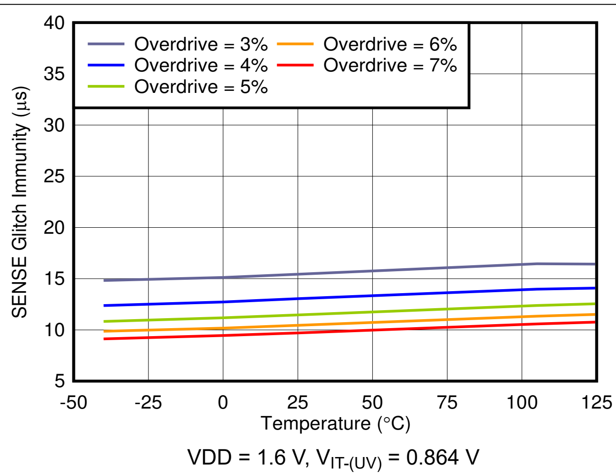


図 6-20. SENSE Glitch Immunity vs Temperature

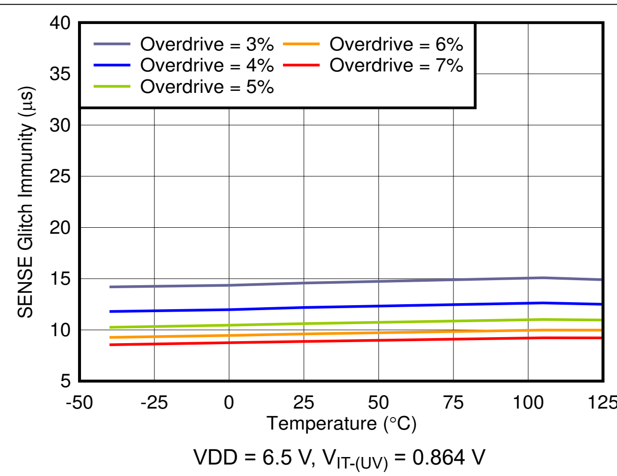


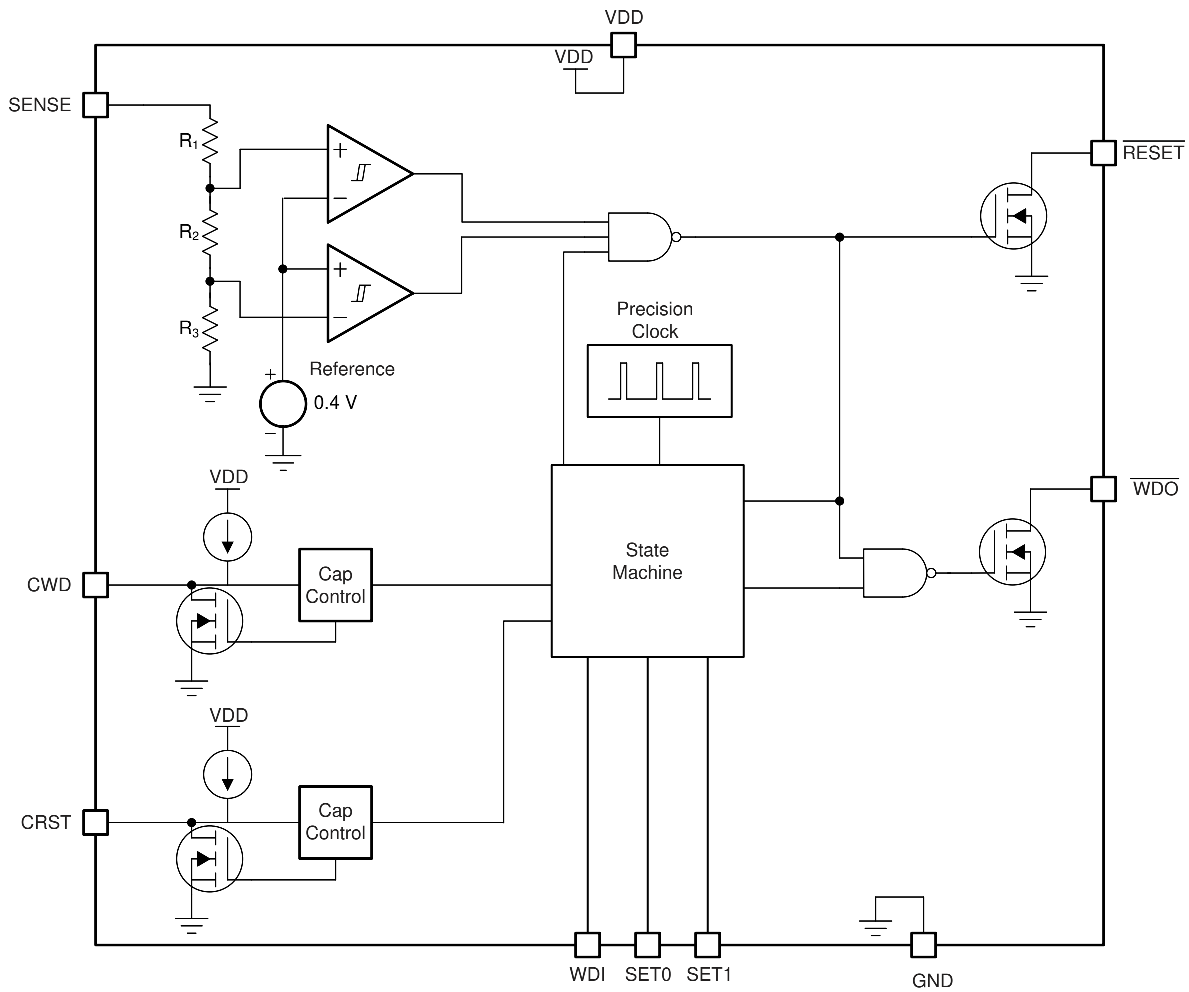
図 6-21. SENSE Glitch Immunity vs Temperature

7 Detailed Description

7.1 Overview

The TPS3850-Q1 is a high-accuracy voltage supervisor with an integrated watchdog timer. This device includes a precision voltage supervisor with both overvoltage ($V_{IT+(OV)}$) and undervoltage ($V_{IT-(UV)}$) thresholds that achieve 0.8% accuracy over the specified temperature range of –40°C to +125°C. In addition, the TPS3850-Q1 includes accurate hysteresis on both thresholds, making the device ideal for use with tight tolerance systems where voltage supervisors must ensure a $\overline{\text{RESET}}$ before the minimum and maximum supply tolerance of the microprocessor or system-on-a-chip (SoC) is reached.

7.2 Functional Block Diagrams



$R_{TOTAL} = R_1 + R_2 + R_3 = 4.5\ M\Omega$.

図 7-1. Fixed Version Block Diagram

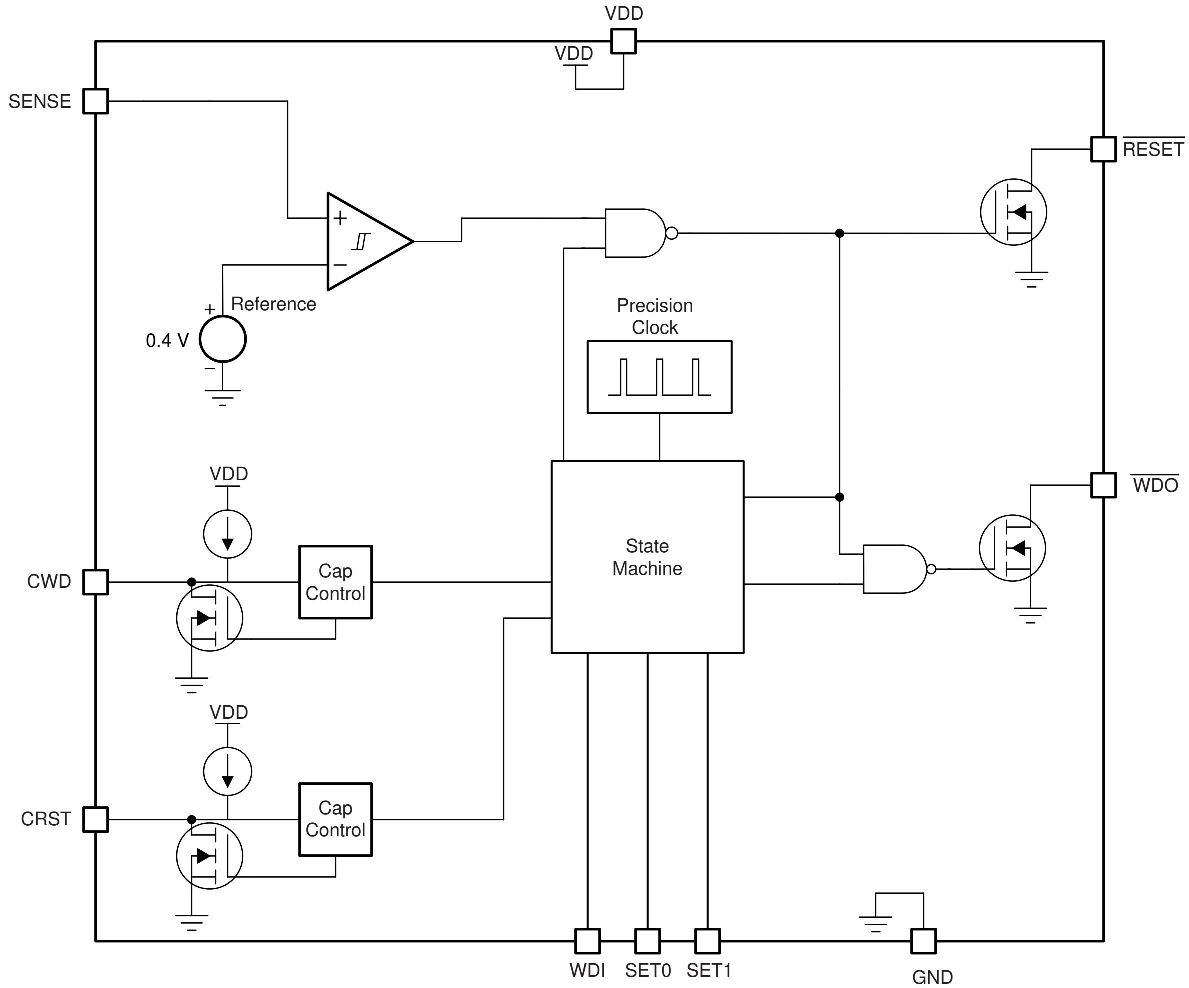


図 7-2. Adjustable Version Block Diagram

7.3 Feature Description

7.3.1 CRST

The CRST pin provides the user the functionality of both high-precision, factory-programmed, reset delay timing options and user-programmable, reset delay timing. The CRST pin can be pulled up to VDD through a resistor, have an external capacitor to ground, or can be left unconnected. The configuration of the CRST pin is re-evaluated by the device every time the voltage on the SENSE line enters the valid window ($V_{IT+(UV)} < V_{SENSE} < V_{IT-(OV)}$). The pin evaluation is controlled by an internal state machine that determines which option is connected to the CRST pin. The sequence of events takes 381 µs (t_{INIT}) to determine if the CRST pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CRST pin is being pulled up to VDD, then a 10-kΩ pullup resistor is required.

7.3.2 $\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ pin features a programmable reset delay time that can be adjusted from 703 µs to 3.22 seconds when using adjustable capacitor timing. $\overline{\text{RESET}}$ is an open-drain output that should be pulled up through a 1-kΩ to 100-kΩ pullup resistor. When V_{DD} is above $V_{DD\ (min)}$, $\overline{\text{RESET}}$ remains high (not asserted) when the SENSE voltage is between the positive threshold ($V_{IT+(OV)}$) and the negative threshold ($V_{IT-(UV)}$). If SENSE falls below $V_{IT-(UV)}$ or rises above $V_{IT+(OV)}$, then $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to a low-impedance state. When SENSE comes back into the valid window, a $\overline{\text{RESET}}$ delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period (t_{RST}). This t_{RST} period is determined by what is connected to the CRST pin; see 図 8-1. When the reset delay has elapsed, the $\overline{\text{RESET}}$ pin goes to a high-impedance state and uses a pullup resistor to hold $\overline{\text{RESET}}$ high. The pullup resistor must be connected to the proper voltage rail to allow other devices to be connected at the correct interface voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by output logic low voltage (V_{OL}), capacitive loading, and leakage current (I_D); see the *セクション 8.1.1* section for more information.

7.3.3 Over- and Undervoltage Fault Detection

The TPS3850-Q1 features both overvoltage detection and undervoltage detection. This detection is achieved through the combination of two comparators with a precision voltage reference and a trimmed resistor divider (fixed versions only). The SENSE pin is used to monitor the critical voltage rail; this configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides some noise immunity and ensures stable operation. If the voltage on the SENSE pin drops below $V_{IT-(UV)}$, then $\overline{\text{RESET}}$ is asserted (driven low). When the voltage on the SENSE pin is between the positive and negative threshold voltages, $\overline{\text{RESET}}$ deasserts after the user-defined $\overline{\text{RESET}}$ delay time, as shown in 図 7-3.

The SENSE input can vary from GND to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, for noisy applications, good analog-design practice is to place a 1-nF to 100-nF bypass capacitor at the SENSE pin to reduce sensitivity to transient voltages on the monitored signal.

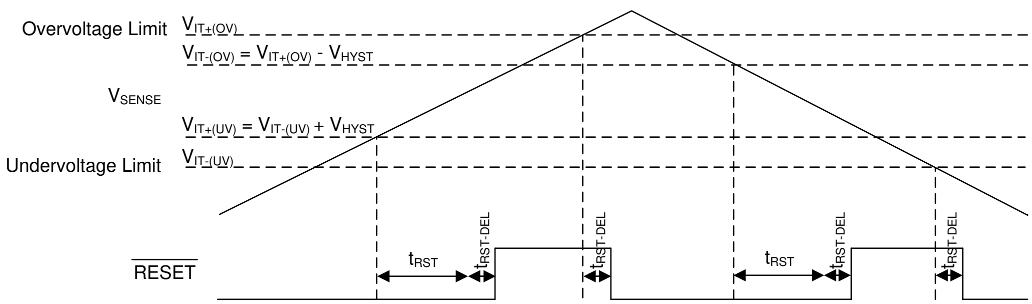


図 7-3. Window Comparator Timing Diagram

7.3.4 Adjustable Operation Using the TPS3850H01Q1

The adjustable version (TPS3850H01Q1) can be used to monitor any voltage rail down to 0.4 V using the circuit illustrated in 図 7-4. When using the TPS3850H01Q1, the device does not function as a window comparator; instead, the device only monitors the undervoltage threshold. To monitor a user-defined voltage, the target threshold voltage for the monitored supply (V_{MON}) and the resistor divider values can be calculated by using 式 1 and 式 2, respectively:

$$V_{MON} = V_{IT(ADJ)} \times \left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

式 1 can be used to calculate either the negative threshold or the positive threshold by replacing V_{ITx} with either V_{ITN} or V_{ITN} + V_{HYST}, respectively.

$$R_{TOTAL} = R_1 + R_2 \tag{2}$$

Large resistor values minimize current consumption; however, the input bias current of the device degrades accuracy if the current through the resistors is too low. Therefore, choosing an R_{TOTAL} value so that the current through the resistor divider is at least 100 times larger than the maximum SENSE pin current (I_{SENSE}) ensures a good degree of accuracy; see the *I_Q vs Accuracy Tradeoff In Designing Resistor Divider Input To A Voltage Supervisor* (SLVA450) for more details on sizing input resistors.

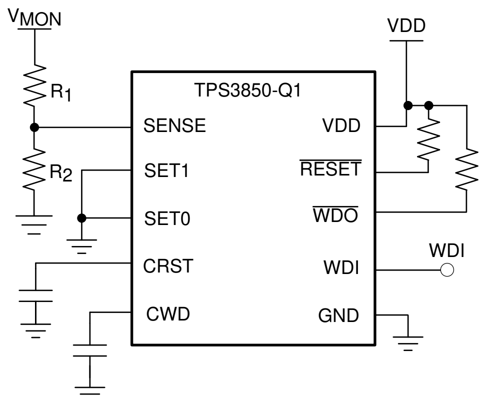


図 7-4. Adjustable Voltage Monitor

7.3.5 Window Watchdog

7.3.5.1 SET0 and SET1

When changing the SET0 or SET1 pins, there are two cases to consider: enabling and disabling the watchdog, and changing the SET0 or SET1 pins when the watchdog is enabled. In case 1 where the watchdog is being enabled or disabled, the changes take effect immediately. However, in case 2, a RESET event must occur in order for the changes to take place.

7.3.5.1.1 Enabling the Window Watchdog

The TPS3850-Q1 features the ability to enable and disable the watchdog timer. This feature allows the user to start with the watchdog timer disabled and then enable the watchdog timer using the SET0 and SET1 pins. The ability to enable and disable the watchdog is useful to avoid undesired watchdog trips during initialization and shutdown. When the SETx pins are changed to disable the watchdog timer, changes on the pins are responded to immediately (as shown in 図 7-5). When the watchdog goes from disabled to enabled, there is a 150 µs ($t_{WD\text{-}setup}$) transition period where the device does not respond to changes on WDI. After this 150-µs period, the device begins to respond to changes on WDI again.

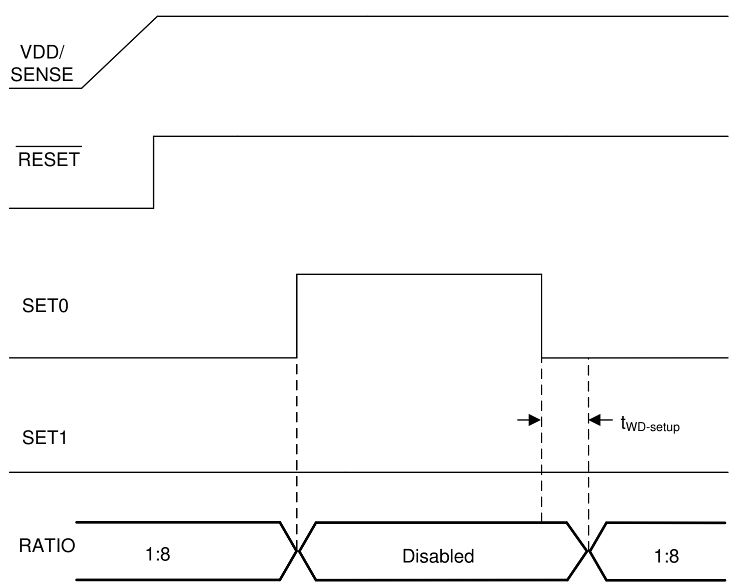
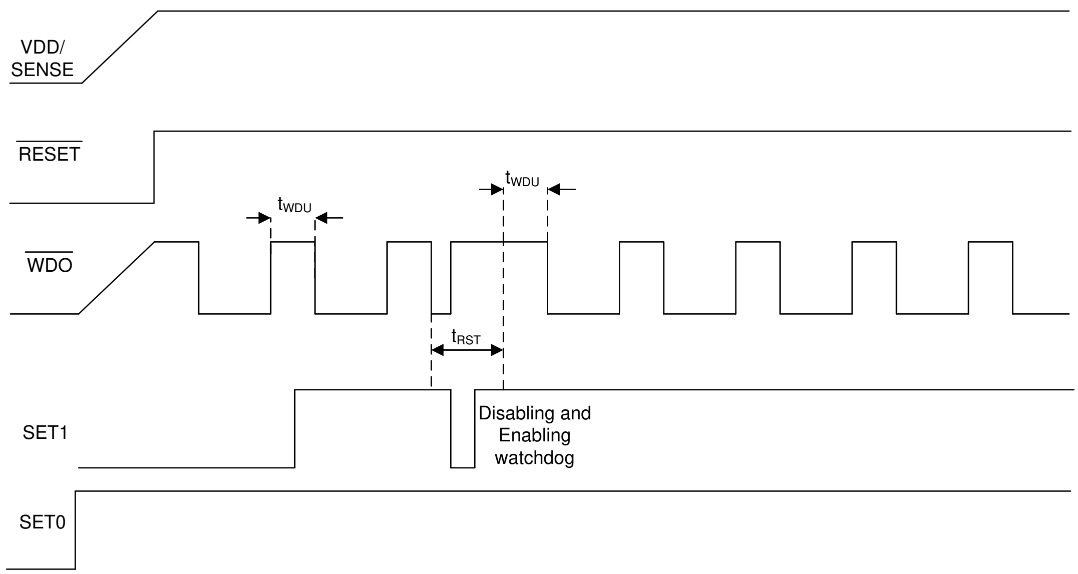


図 7-5. Enabling the Watchdog Timer

7.3.5.1.2 Disabling the Watchdog Timer When Using the CRST Capacitor

When using the TPS3850-Q1 with fixed timing options, if the watchdog is disabled and reenabled while $\overline{WDO}$ is asserted (logic low) the watchdog performs as described in the *セクション 7.3.5.1.1* section. However, if there is a capacitor on the CRST pin, and the watchdog is disabled and reenabled when $\overline{WDO}$ is asserted (logic low), then the watchdog behaves as shown in 図 7-6. When the watchdog is disabled, $\overline{WDO}$ goes high impedance (logic high). However, when the watchdog is enabled again, the t_{RST} period must expire before the watchdog resumes normal operation.



There is no WDI signal in this figure, WDI is always at GND.

図 7-6. Enabling and Disabling the Watchdog Timer During a WDO Reset Event

7.3.5.1.3 SET0 and SET1 During Normal Watchdog Operation

The SET0 and SET1 pins can be used to control the window watchdog ratio of the lower boundary to the upper boundary. There are four possible modes for the watchdog (see 表 8-5): disabled, 1:8 ratio, 3:4 ratio, and 1:2 ratio. If SET0 = 1 and SET1 = 0, then the watchdog is disabled. When the watchdog is disabled, $\overline{\text{WDO}}$ does not assert and the TPS3850-Q1 functions as a normal supervisor. The SET0 and SET1 pins can be changed when the device is operational, but cannot be changed at the same time. If these pins are changed when the device is operational, then there must be a 500-µs (t_{SET}) delay between switching the two pins. If SET0 and SET1 are used to change the reset timing, then a reset event must occur before the new timing condition is latched. This reset can be triggered by SENSE rising above $V_{IT+(OV)}$ or below $V_{IT-(UV)}$, or by bringing V_{DD} below V_{UVLO}. 図 7-7 shows how the SET0 and SET1 pins do not change the watchdog timing option until a reset event has occurred.

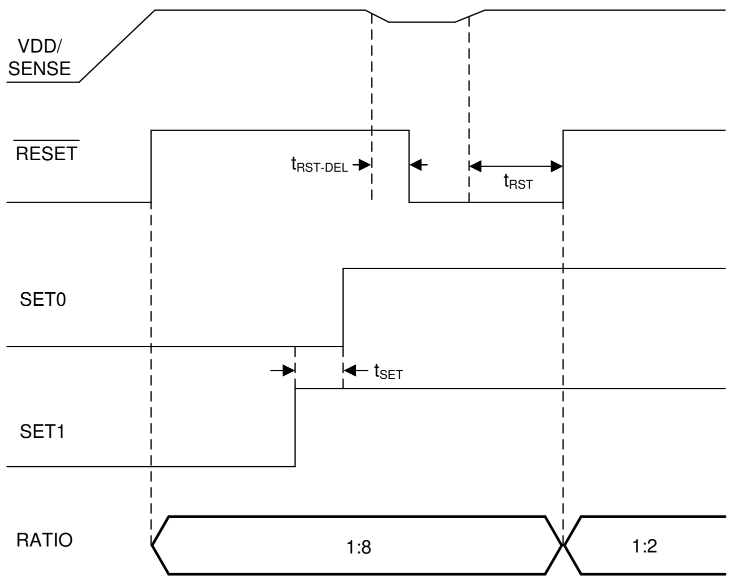


図 7-7. Changing SET0 and SET1 Pins

7.3.6 Window Watchdog Timer

This section provides information for the window watchdog modes of operation. A window watchdog is typically employed in safety-critical applications where a traditional watchdog timer is inadequate. In a traditional watchdog, there is a maximum time in which a pulse must be issued to prevent the reset from occurring. However, in a window watchdog the pulse must be issued between a maximum lower window time ($t_{WDL(max)}$) and the minimum upper window time ($t_{WDU(min)}$) set by the CWD pin and the SET0 and SET1 pins. 表 8-5 describes how t_{WDU} can be used to calculate the timing of t_{WDL}. The t_{WDL} timing can also be changed by adjusting the SET0 and SET1 pins. 図 7-8 shows the valid region for a WDI pulse to be issued to prevent the $\overline{WDO}$ from being triggered and being pulled low.

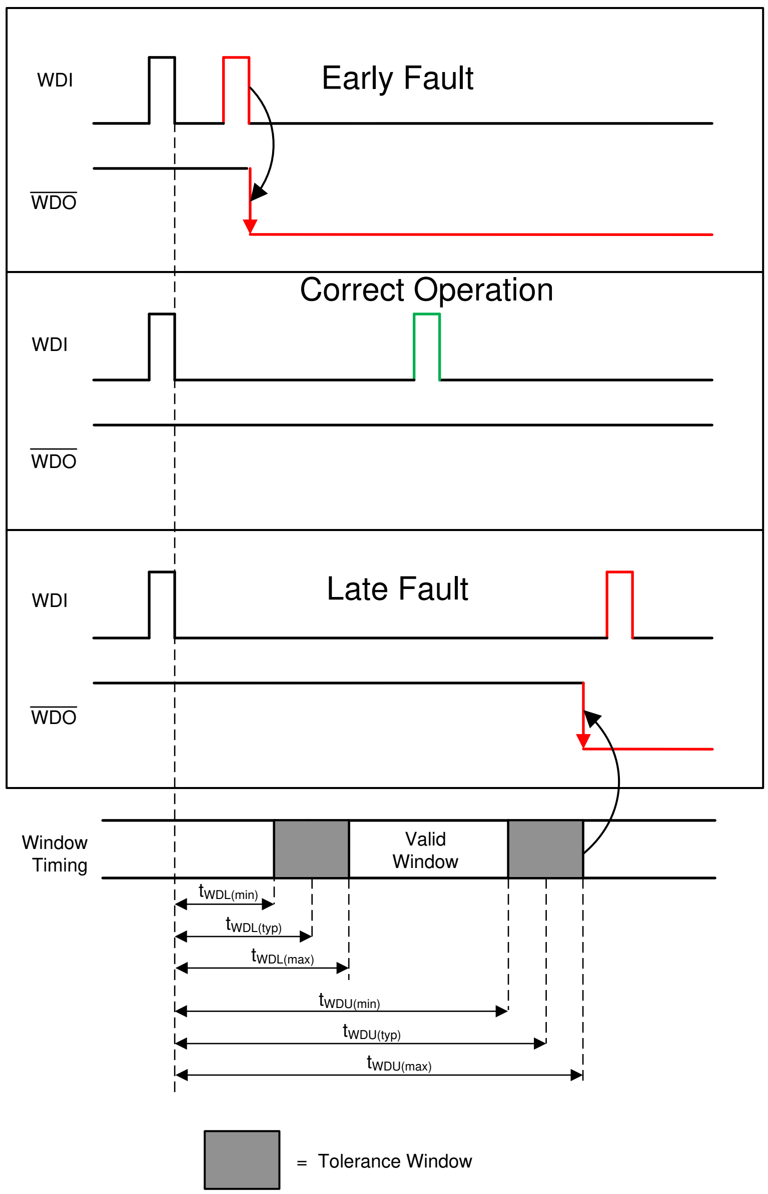


図 7-8. TPS3850-Q1 Window Watchdog Timing

7.3.6.1 CWD

The CWD pin provides the user the functionality of both high-precision, factory-programmed watchdog timing options and user-programmable watchdog timing. The TPS3850-Q1 features three options for setting the watchdog window: connecting a capacitor to the CWD pin, connecting a pullup resistor to VDD, and leaving the CWD pin unconnected. The configuration of the CWD pin is evaluated by the device every time V_{SENSE} enters the valid window ($V_{IT+(UV)} < V_{SENSE} < V_{IT-(OV)}$). The pin evaluation is controlled by an internal state machine that determines which option is connected to the CWD pin. The sequence of events takes 381 µs (t_{INIT}) to determine if the CWD pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CWD pin is being pulled up to VDD using a pullup resistor, then a 10-kΩ resistor is required.

7.3.6.2 WDI Functionality

WDI is the watchdog timer input that controls the $\overline{\text{WDO}}$ output. The WDI input is triggered by the falling edge of the input signal. For the first pulse, the watchdog functions as a traditional watchdog timer; thus, the first pulse must be issued before $t_{WDU(min)}$. After the first pulse, to ensure proper functionality of the watchdog timer, always issue the WDI pulse within the window of $t_{WDL(max)}$ and $t_{WDU(min)}$. If the pulse is issued in this region, then $\overline{\text{WDO}}$ remains unasserted. Otherwise, the device asserts $\overline{\text{WDO}}$, putting the $\overline{\text{WDO}}$ pin into a low-impedance state.

The watchdog input (WDI) is a digital pin. To ensure there is no increase in I_{DD}, drive the WDI pin to either VDD or GND at all times. Putting the pin to an intermediate voltage can cause an increase in supply current (I_{DD}) because of the architecture of the digital logic gates. When $\overline{\text{RESET}}$ is asserted, the watchdog is disabled and all signals input to WDI are ignored. When $\overline{\text{RESET}}$ is no longer asserted, the device resumes normal operation and no longer ignores the signal on WDI. If the watchdog is disabled, drive the WDI pin to either VDD or GND.

7.3.6.3 $\overline{\text{WDO}}$ Functionality

The TPS3850-Q1 features a window watchdog timer with an independent watchdog output ($\overline{\text{WDO}}$). The independent watchdog output provides the flexibility to flag a fault in the watchdog timing without performing an entire system reset. When $\overline{\text{RESET}}$ is not asserted (high), the $\overline{\text{WDO}}$ signal maintains normal operation. When asserted, $\overline{\text{WDO}}$ remains down for t_{RST}. When the $\overline{\text{RESET}}$ signal is asserted (low), the $\overline{\text{WDO}}$ pin goes to a high-impedance state. When $\overline{\text{RESET}}$ is unasserted, the window watchdog timer resumes normal operation and $\overline{\text{WDO}}$ can be used again.

7.4 Device Functional Modes

表 7-1 summarizes the functional modes of the TPS3850-Q1.

表 7-1. Device Functional Modes

VDD	WDI	$\overline{\text{WDO}}$	SENSE	$\overline{\text{RESET}}$
$V_{DD} < V_{POR}$	—	—	—	Undefined
$V_{POR} \le V_{DD} < V_{UVLO}$	Ignored	High	—	Low
$V_{DD} \ge V_{DD\ (min)}$	Ignored	High	$V_{SENSE} < V_{IT+(UV)}$ (1)	Low
	Ignored	High	$V_{SENSE} > V_{IT-(OV)}$ (1)	Low
	$t_{WDL(max)} \le t_{pulse}$ (3) $\le t_{WDU(min)}$	High	$V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)}$ (2)	High
	$t_{WDL(max)} > t_{pulse}$ (3)	Low	$V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)}$ (2)	High
	$t_{WDU(min)} < t_{pulse}$ (3)	Low	$V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)}$ (2)	High

(1) When V_{SENSE} has not entered the valid window.
(2) When V_{SENSE} is in the valid window.
(3) Where t_{pulse} is the time between falling edges on WDI.

7.4.1 V_{DD} is Below V_{POR} ($V_{DD} < V_{POR}$)

When V_{DD} is less than V_{POR}, $\overline{\text{RESET}}$ is undefined and can be either high or low. The state of $\overline{\text{RESET}}$ largely depends on the load that the $\overline{\text{RESET}}$ pin is experiencing.

7.4.2 Above Power-On-Reset But Less Than UVLO ($V_{POR} \le V_{DD} < V_{UVLO}$)

When V_{DD} is less than V_{UVLO}, and greater than or equal to V_{POR}, the $\overline{\text{RESET}}$ signal is asserted (logic low) regardless of the voltage on the SENSE pin. When $\overline{\text{RESET}}$ is asserted, the watchdog output $\overline{\text{WDO}}$ is in a high-impedance state regardless of the WDI signal that is input to the device.

7.4.3 Above UVLO But Less Than $V_{DD\ (min)}$ ($V_{UVLO} \le V_{DD} < V_{DD\ (min)}$)

When V_{DD} is less than $V_{DD\ (min)}$ and greater than or equal to V_{UVLO}, the $\overline{\text{RESET}}$ signal responds to changes on the SENSE pin, but the accuracy can be degraded.

7.4.4 Normal Operation ($V_{DD} \ge V_{DD\ (min)}$)

When V_{DD} is greater than or equal to $V_{DD\ (min)}$, the $\overline{\text{RESET}}$ signal is determined by V_{SENSE}. When $\overline{\text{RESET}}$ is asserted, $\overline{\text{WDO}}$ goes to a high-impedance state. $\overline{\text{WDO}}$ is then pulled high through the pullup resistor.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.1.1 CRST Delay

The TPS3850-Q1 features three options for setting the reset delay (t_{RST}): connecting a capacitor to the CRST pin, connecting a pullup resistor to VDD, and leaving the CRST pin unconnected. 図 8-1 shows a schematic drawing of all three options. To determine which option is connected to the CRST pin, an internal state machine controls the internal pulldown device and measures the pin voltage. This sequence of events takes 381 µs (t_{INIT}) to determine which timing option is used. Every time $\overline{RESET}$ is asserted, the state machine determines what is connected to the pin.

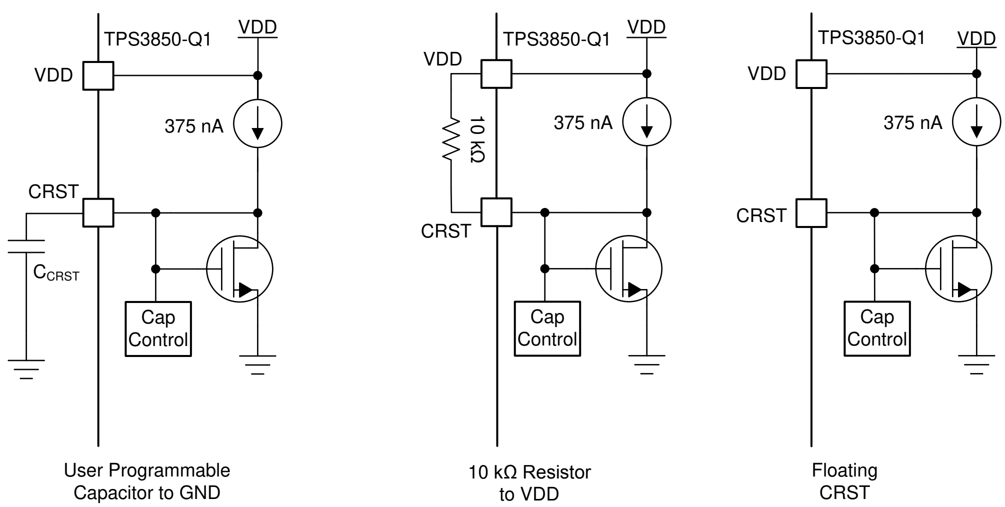


図 8-1. CRST Charging Circuit

8.1.1.1 Factory-Programmed Reset Delay Timing

To use the factory-programmed timing options, the CRST pin must either be left unconnected or pulled up to VDD through a 10-kΩ pullup resistor. Using these options enables a high-precision, 15% accurate reset delay timing, as shown in 表 8-1.

表 8-1. Reset Delay Time for Factory-Programmed Reset Delay Timing

CRST	$\overline{RESET}$ DELAY TIME (t_{RST})			UNIT
	MIN	TYP	MAX	
NC	170	200	230	ms
10 kΩ to VDD	8.5	10	11.5	ms

8.1.1.2 Programmable Reset Delay Timing

The TPS3850-Q1 uses a CRST pin charging current (I_{CRST}) of 375 nA. When using an external capacitor, the rising $\overline{\text{RESET}}$ delay time can be set to any value between 700 µs (C_{CRST} = 100 pF) and 3.2 seconds (C_{CRST} = 1 µF). The typical ideal capacitor value needed for a given delay time can be calculated using 式 3, where C_{CRST} is in microfarads and t_{RST} is in seconds:

$$t_{RST} = 3.22 \times C_{CRST} + 0.000381 \quad (3)$$

To calculate the minimum and maximum-reset delay time use 式 4 and 式 5, respectively.

$$t_{RST(min)} = 2.8862 \times C_{CRST} + 0.000324 \quad (4)$$

$$t_{RST(max)} = 3.64392 \times C_{CRST} + 0.000438 \quad (5)$$

The slope of 式 3 is determined by the time the CRST charging current (I_{CRST}) takes to charge the external capacitor up to the CRST comparator threshold voltage (V_{CRST}). When $\overline{\text{RESET}}$ is asserted, the capacitor is discharged through the internal CRST pulldown resistor. When the $\overline{\text{RESET}}$ conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor; when V_{CRST} = 1.21 V, $\overline{\text{RESET}}$ is unasserted. Note that to minimize the difference between the calculated $\overline{\text{RESET}}$ delay time and the actual $\overline{\text{RESET}}$ delay time, use a use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. 表 8-2 lists the reset delay time ideal capacitor values for C_{CRST}.

表 8-2. Reset Delay Time for Common Ideal Capacitor Values

C_{CRST}	$\overline{\text{RESET}}$ DELAY TIME (t_{RST})			UNIT
	MIN(1)	TYP	MAX(1)	
100 pF	0.61	0.70	0.80	ms
1 nF	3.21	3.61	4.08	ms
10 nF	29.2	32.6	36.8	ms
100 nF	289	323	364	ms
1 µF	2886	3227	3644	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

8.1.2 CWD Functionality

The TPS3850-Q1 features three options for setting the watchdog window: connecting a capacitor to the CWD pin, connecting a pullup resistor to VDD, and leaving the CWD pin unconnected. 図 8-2 shows a schematic drawing of all three options. If this pin is connected to VDD through a 10-kΩ pullup resistor or left unconnected (high impedance), then the factory-programmed watchdog timeouts are enabled; see the table. Otherwise, the watchdog timeout can be adjusted by placing a capacitor from the CWD pin to ground.

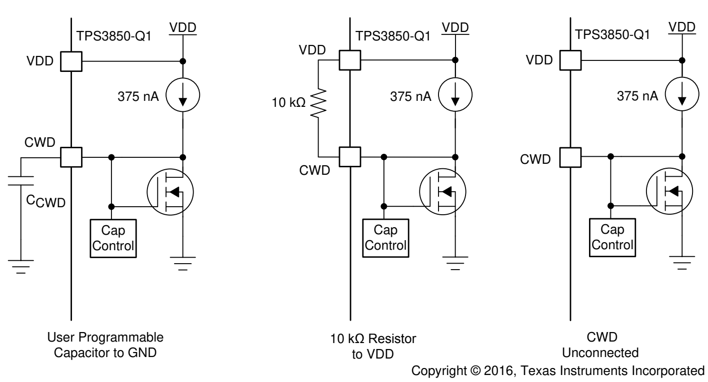


図 8-2. CWD Charging Circuit

8.1.2.1 Factory-Programmed Timing Options

If using the factory-programmed timing options (listed in 表 8-3), the CWD pin must either be unconnected or pulled up to VDD through a 10-kΩ pullup resistor. Using these options enables high-precision, factory programmed watchdog timing.

表 8-3. Factory-Programmed Watchdog Timing

INPUT			WATCHDOG LOWER BOUNDARY (t_{WDL})			WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
CWD	SET0	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
NC	0	0	19.1	22.5	25.9	46.8	55.0	63.3	ms
	0	1	1.48	1.85	2.22	23.375	27.5	31.625	ms
	1	0	Watchdog disabled			Watchdog disabled			
	1	1	680	800	920	1360	1600	1840	ms
10 kΩ to VDD	0	0	7.65	9.0	10.35	92.7	109.0	125.4	ms
	0	1	7.65	9.0	10.35	165.8	195.0	224.3	ms
	1	0	Watchdog disabled			Watchdog disabled			
	1	1	1.48	1.85	2.22	9.35	11.0	12.65	ms

8.1.2.2 Adjustable Capacitor Timing

Adjustable capacitor timing is achievable by connecting a capacitor to the CWD pin. If a capacitor is connected to CWD, then a 375-nA, constant-current source charges C_{CWD} until V_{CWD} = 1.21 V. The TPS3850-Q1 determines the window watchdog upper boundary with the formula given in 式 6, where C_{CWD} is in microfarads and t_{WDU} is in seconds.

$$t_{WDU(typ)} = 77.4 \times C_{CWD} + 0.055 \quad (6)$$

The TPS3850-Q1 is designed and tested using C_{CWD} capacitors between 100 pF and 1 µF. Note that 式 6 is for ideal capacitors. Capacitor tolerances cause the actual device timing to vary such that the minimum of t_{WDU} can decrease and the maximum of t_{WDU} can increase by the capacitor tolerance. To allow for a valid watchdog window, choose a capacitor with tolerance such that $t_{WDU(min)}$ and $t_{WDL(max)}$ do not overlap. For the most accurate timing, use ceramic capacitors with COG dielectric material. As shown in 表 8-4, when using the minimum capacitor of 100 pF, the watchdog upper boundary is 62.74 ms; whereas with a 1-µF capacitor, the watchdog upper boundary is 77.455 seconds. If a C_{CWD} capacitor is used, 式 6 can be used to set t_{WDU} the window watchdog upper boundary. The window watchdog lower boundary is dependent on the SET0 and SET1 pins because these pins set the window watchdog ratio of the lower boundary to upper boundary; 表 8-5 shows how t_{WDU} can be used to calculate t_{WDL} based on the SET0 and SET1 pins.

8.1.2.3

表 8-4. t_{WDU} Values for Common Ideal Capacitor Values

C_{CWD}	WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
	MIN(1)	TYP	MAX(1)	
100 pF	56.77	62.74	68.7	ms
1 nF	119.82	132.4	144.98	ms
10 nF	750	829	908	ms
100 nF	7054	7795	8536	ms
1 µF	70096	77455	84814	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

表 8-5. Programmable CWD Timing

INPUT			WATCHDOG LOWER BOUNDARY (t_{WDL})			WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
CWD	SET0	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
C_{CWD}	0	0	$t_{WDU(min)}$x 0.125	t_{WDU} x 0.125	$t_{WDU(max)}$ x 0.125	0.905 x $t_{WDU(typ)}$	$t_{WDU(typ)}$	1.095 x $t_{WDU(typ)}$	s
	0	1	$t_{WDU(min)}$ x 0.75	t_{WDU} x 0.75	$t_{WDU(max)}$ x 0.75	0.905 x $t_{WDU(typ)}$	$t_{WDU(typ)}$	1.095 x $t_{WDU(typ)}$	s
	1	0	Watchdog disabled			Watchdog disabled			
	1	1	$t_{WDU(min)}$ x 0.5	t_{WDU} x 0.5	$t_{WDU(max)}$ x 0.5	0.905 x $t_{WDU(typ)}$	$t_{WDU(typ)}$	1.095 x $t_{WDU(typ)}$	s

8.1.3 Adjustable SENSE Configuration

The TPS3850H01Q1 has an undervoltage supervisor that can monitor voltage rails greater than 0.4 V. 表 8-6 contains 1% resistor values for creating a voltage divider to monitor common rails from 0.5 V to 12 V with a threshold of 4% and 10%. These resistor values can be scaled to decrease the amount of current flowing through the resistor divider, but increasing the resistor values also decreases the accuracy of the resistor divider. General practice is for the current flowing through the resistor divider to be 100 times greater than the current going into the SENSE pin. This practice ensures the highest possible accuracy. 式 7 can be used to calculate the resistors required in the resistor divider. 図 8-3 shows the block diagram for adjustable operation.

$$V_{MON} = V_{IT(ADJ)} \times \left(1 + \frac{R_1}{R_2}\right) \tag{7}$$

表 8-6. SENSE Resistor Divider Values

INPUT VOLTAGE (V)	4% THRESHOLD			10% THRESHOLD		
	R_1 (kΩ)	R_2 (kΩ)	THRESHOLD VOLTAGE (V)	R_1 (kΩ)	R_2 (kΩ)	THRESHOLD VOLTAGE (V)
0.5	16.2	80.6	0.48	10	80.6	0.45
0.8	75	80.6	0.77	64.9	80.6	0.72
0.9	93.1	80.6	0.86	82.5	80.6	0.81
1.2	150	80.6	1.14	137	80.6	1.08
1.8	267	80.6	1.73	249	80.6	1.64
2.5	402	80.6	2.40	374	80.6	2.26
3	499	80.6	2.88	464	80.6	2.70
3.3	562	80.6	3.19	523	80.6	2.99
5	887	80.6	4.80	825	80.6	4.49
12	2260	80.6	11.62	2100	80.6	10.82

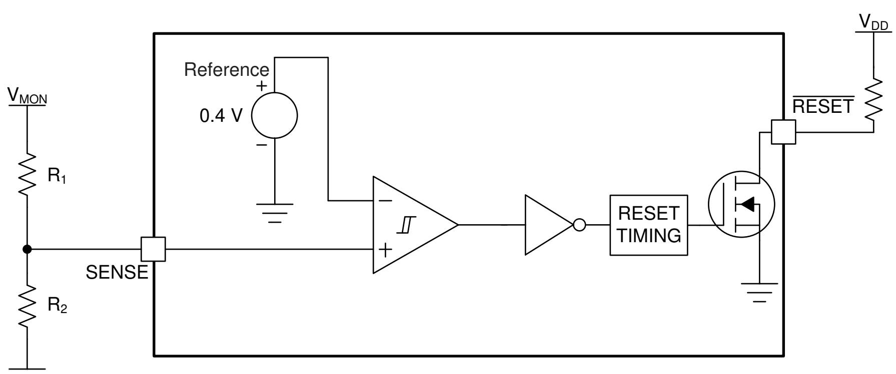


図 8-3. Adjustable Voltage Divider

8.1.4 Overdrive on the SENSE Pin

The propagation delay from exceeding the threshold to $\overline{\text{RESET}}$ being asserted is dependent on two conditions: the amplitude of the voltage on the SENSE pin relative to the threshold, (ΔV_1 and ΔV_2), and the length of time that the voltage is above or below the trip point (t_1 and t_2). If the voltage is just over the trip point for a long period of time, then $\overline{\text{RESET}}$ asserts and the output is pulled low. However, if the SENSE voltage is just over the trip point for a few nanoseconds, then the $\overline{\text{RESET}}$ does not assert and the output remains high. The time required for $\overline{\text{RESET}}$ to assert can be changed by increasing the time that the SENSE voltage goes over the trip point. 式 8 shows how to calculate the percentage overdrive.

$$\text{Overdrive} = |\ (V_{SENSE} / V_{ITx} - 1) \times 100\%\ | \tag{8}$$

In 式 8, V_{ITx} corresponds to the SENSE threshold trip point. If V_{SENSE} exceeds the positive threshold, then $V_{IT+(OV)}$ is used. $V_{IT-(UV)}$ is used when V_{SENSE} falls below the negative threshold. In 図 8-4, t_1 and t_2 correspond to the amount of time that the SENSE voltage is over the threshold. The response time versus overdrive for $V_{IT+(OV)}$ and $V_{IT-(UV)}$ is illustrated in 図 6-14 and 図 6-17, respectively.

The TPS3850-Q1 is relatively immune to short positive and negative transients on the SENSE pin because of the overdrive voltage curve; see 図 6-20 and 図 6-21.

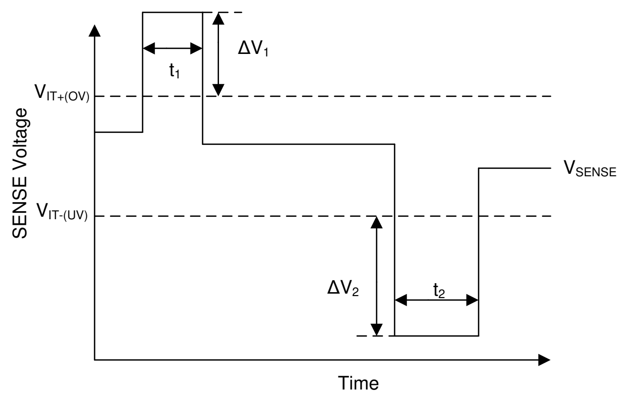


図 8-4. Overdrive Voltage on the SENSE Pin

8.2 Typical Applications

8.2.1 Design 1: Monitoring a 1.2-V Rail with Factory-Programmable Watchdog Timing

A typical application for the TPS3850-Q1 is shown in 図 8-5. The TPS3850G12Q1 is used to monitor the 1.2-V, V_{CORE} rail powering the microcontroller.

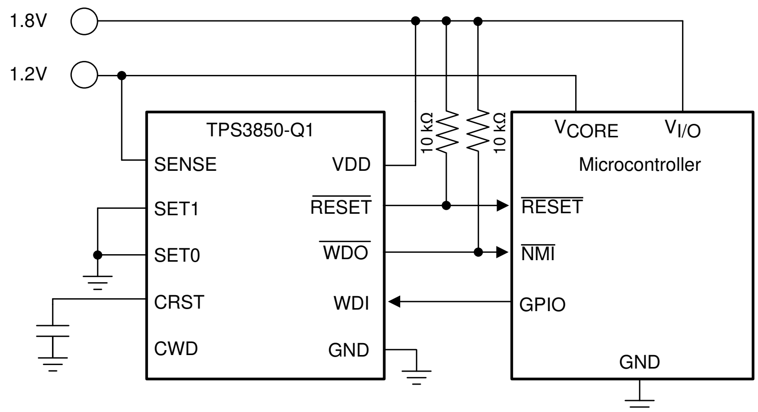


図 8-5. Monitoring Supply Voltage and Watchdog Supervision of a Microcontroller

8.2.1.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Reset delay	Minimum reset delay of 250 ms	Minimum reset delay of 260 ms, reset delay of 322 ms (typical)
Watchdog window	Functions with a 200-Hz pulse-width modulation (PWM) signal with a 50% duty cycle	Leaving the CWD pin unconnected with SET0 = 0 and SET1 = 1 produces a window with a $t_{WDL(max)}$ of 2.2 ms and a $t_{WDU(min)}$ of 22 ms
Output logic voltage	1.8-V CMOS	1.8-V CMOS
Monitored rail	1.2 V within ±5%	Worst-case $V_{IT+(OV)}$ 1.257 V (4.8%)
		Worst-case $V_{IT-(UV)}$ 1.142 V (4.7%)
Maximum device current consumption	200 µA	10 µA of current consumption, typical worst-case of 199 µA when $\overline{WDO}$ or $\overline{RESET}$ is asserted

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Monitoring the 1.2-V Rail

The window comparator allows for precise voltage supervision of common rails between 0.9 V and 5.0 V. This application calls for very tight monitoring of the rail with only ±5% of variation allowed on the rail. To ensure this requirement is met, the TPS3850G12Q1 was chosen for its ±4% thresholds. To calculate the worst-case for $V_{IT+(OV)}$ and $V_{IT-(UV)}$, the accuracy must also be taken into account. The worst-case for $V_{IT+(OV)}$ can be calculated by 式 9:

$$V_{IT+(OV)(Worst\text{-}Case)} = V_{IT+(OV)typ} \times 1.048 = 1.2 \times 1.048 = 1.257\ V \tag{9}$$

The worst case for $V_{IT-(UV)}$ can be calculated using 式 10:

$$V_{IT-(UV)(Worst\text{-}Case)} = V_{IT-(UV)typ} \times 0.952 = 1.2 \times 0.952 = 1.142\ V \tag{10}$$

8.2.1.2.2 Meeting the Minimum Reset Delay

The TPS3850-Q1 features three options for setting the reset delay: connecting a capacitor to the CRST pin, connecting a pullup resistor, and leaving the CRST pin unconnected. If the CRST pin is either unconnected or pulled up the minimum timing requirement cannot be met, thus an external capacitor must be connected to the CRST pin. Because a minimum time is required, the worst-case scenario is a supervisor with a high CRST charging current (I_{CRST}) and a low CRST comparator threshold (V_{CRST}). For applications with ambient temperatures ranging from –40°C to +125°C, C_{CRST} can be calculated using $I_{CRST(MAX)}$, $V_{CRST(MIN)}$, and solving for C_{CRST} in 式 11:

$$C_{RST(min)\_ideal} = \frac{t_{RST(min)} - 0.000324}{2.8862} = \frac{0.25 - 0.000324}{2.8862} \tag{11}$$

When solving 式 11, the minimum capacitance required at the CRST pin is 0.086 μF. If standard capacitors with ±10% tolerances are used, then the minimum CRST capacitor required can be found in 式 12:

$$C_{RST(min)} = \frac{C_{RST(min)\_ideal}}{1 - C_{tolerance}} = \frac{0.086\ \mu F}{1 - 0.1} \tag{12}$$

Solving 式 12 where $C_{tolerance}$ is 0.1 or 10%, the minimum C_{CRST} capacitor is 0.096 μF. This value is then rounded up to the nearest standard capacitor value, so a 0.1-μF capacitor must be used to achieve this reset delay timing. If voltage and temperature derating are being considered, then also include these values in $C_{tolerance}$.

8.2.1.2.3 Setting the Watchdog Window

In this application, the window watchdog timing options are based on the PWM signal that is provided to the TPS3850-Q1. A window watchdog setting must be chosen such that the falling edge of the PWM signal always falls within the window. A nominal window must be designed with $t_{WDL(max)}$ less than 5 ms and $t_{WDU(min)}$ greater than 5 ms. There are several options that satisfy this window option. An external capacitor can be placed on the CWD pin and calculated to have a sufficient window. Another option is to use one of the factory-programmed timing options. An additional advantage of choosing one of the factory-programmed options is the ability to reduce the number of components required, thus reducing overall BOM cost. Leaving the CWD pin unconnected (NC) with SET0 = 0 and SET1 = 1 produces a $t_{WDL(max)}$ of 2.22 ms and a $t_{WDU(min)}$ of 23.375 ms; see 図 8-10.

8.2.1.2.4 Calculating the $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ Pullup Resistor

The TPS3850-Q1 uses an open-drain configuration for the $\overline{\text{RESET}}$ circuit, as shown in 図 8-6. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below its maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage (V_{PU}), the recommended maximum $\overline{\text{RESET}}$ pin current (I_{RST}), and V_{OL}. The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with I_{RST} kept below 10 mA. For this example, with a V_{PU} of 1.8 V, a resistor must be chosen to keep I_{RST} below 200 µA because this value is the maximum consumption current allowed. To ensure this specification is met, a pullup resistor value of 10 kΩ was selected, which sinks a maximum of 180 µA when $\overline{\text{RESET}}$ or $\overline{\text{WDO}}$ is asserted. As illustrated in 図 6-12, the $\overline{\text{RESET}}$ current is at 180 µA and the low-level output voltage is approximately zero.

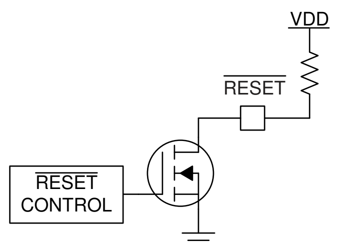


図 8-6. Open-Drain $\overline{\text{RESET}}$ Configuration

8.2.1.3 Application Curves

Unless otherwise stated, application curves were taken at T_A = 25°C.

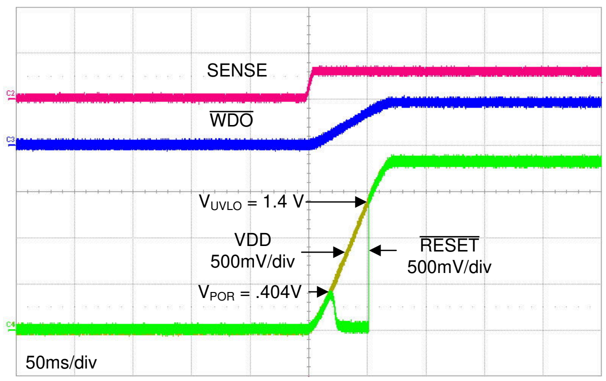


図 8-7. Startup Waveform

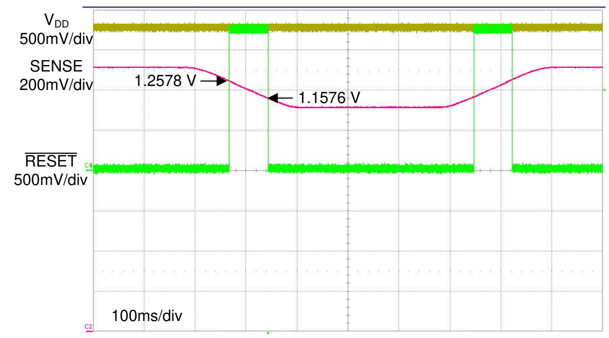


図 8-8. Window Comparator Thresholds Entering a Valid Window

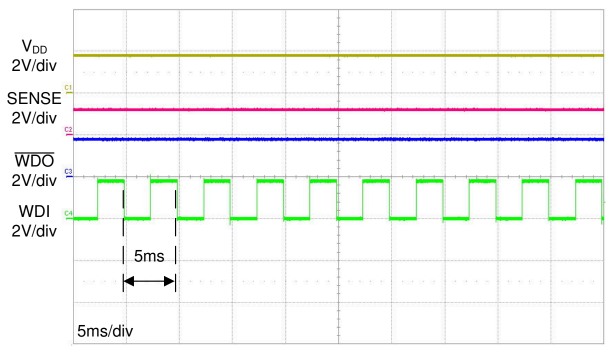


図 8-9. 200-Hz WDI Pulse

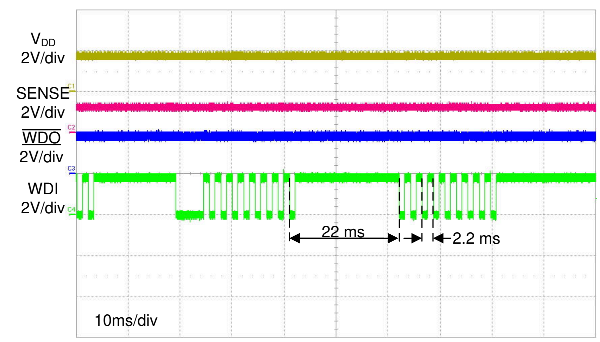


図 8-10. Window Watchdog Timing

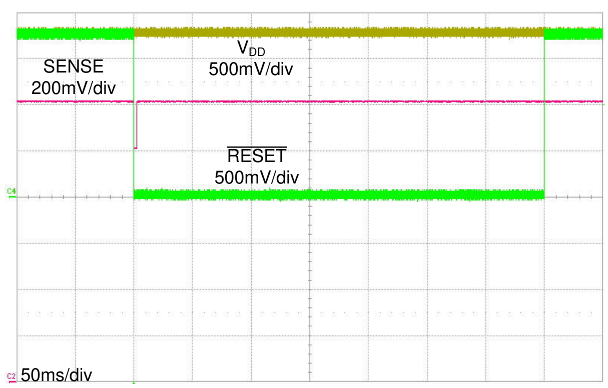


図 8-11. Typical $\overline{\text{RESET}}$ Delay Timing

8.2.2 Design 2: Using the TPS3850H01Q1 to Monitor a 0.7-V Rail With an Adjustable Window Watchdog Timing

A typical application for the TPS3850H01Q1 is shown in 図 8-12.

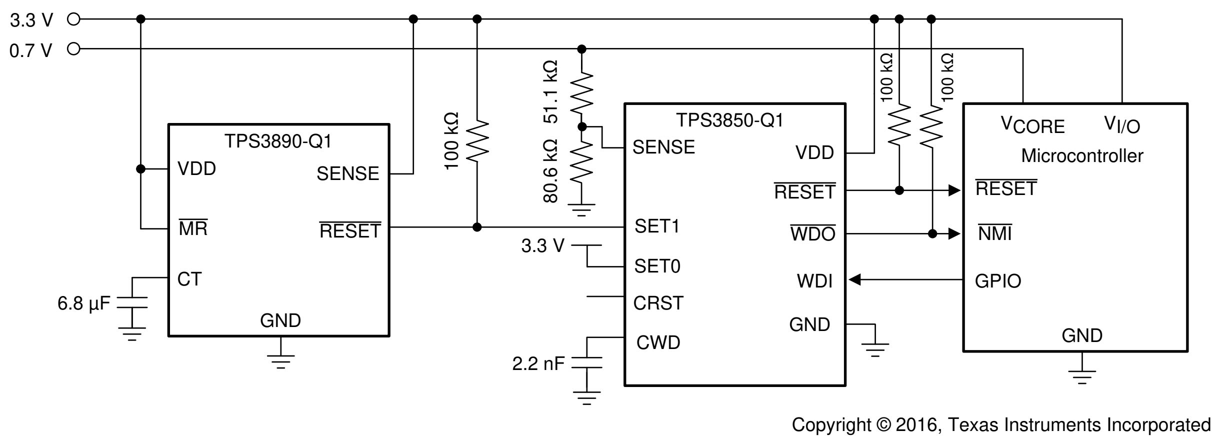


図 8-12. Monitoring Supply Voltage and Watchdog Supervision of a Microcontroller

8.2.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Reset delay	Minimum $\overline{\text{RESET}}$ delay of 150 ms	Minimum $\overline{\text{RESET}}$ delay of 170 ms
Watchdog disable for initialization period	Watchdog must remain disabled for 7 seconds until logic enables the watchdog timer	7.21 seconds (typ)
Watchdog window	250 ms, maximum	$t_{WDL(max)}$ = 135 ms, $t_{WDU(min)}$ = 181 ms
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Monitored rail	0.7 V, with 7% threshold	$V_{ITN\ (max)}$ 0.667 V (–4.7%)
		$V_{ITN\ (typ)}$ 0.65 V (–6.6%)
		$V_{ITN\ (min)}$ 0.641 V (–8.5%)
Maximum device current consumption	50 µA	10 µA of current consumption typical, worst-case of 52 µA when $\overline{\text{WDO}}$ or $\overline{\text{RESET}}$ is asserted(1)

(1) Only includes the current consumption of the TPS3850-Q1.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Meeting the Minimum Reset Delay

The design goal for the $\overline{\text{RESET}}$ delay time can be achieved by either using an external capacitor or the CRST pin can be left unconnected. To minimize component count, the CRST pin is left unconnected. For CRST = NC, the minimum delay is 170 ms, which is greater than the minimum required $\overline{\text{RESET}}$ delay of 150 ms.

8.2.2.2.2 Setting the Window Watchdog

As illustrated in 図 8-2, there are three options for setting the window watchdog. The design specifications in this application require the programmable timing option (external capacitor connected to CWD). When a capacitor is connected to the CWD pin, the window is governed by 式 13. 式 13 is only valid for ideal capacitors, any temperature or voltage derating must be accounted for separately.

$$C_{CWD}\left(\mu F\right) = \frac{t_{WDU} - 0.055}{77.4} = \frac{0.25 - 0.055}{77.4} = 0.0025\ \mu F \tag{13}$$

The nearest standard capacitor value to 2.5 nF is 2.2 nF. Selecting 2.2 nF for the C_{CWD} capacitor gives the following minimum and maximum timing parameters:

$$t_{WDU(MIN)} = 0.905 \times t_{WDU(TYP)} = 0.905 \times \left(77.4 \times 2.2 \times 10^{-3} + 0.055\right) = 203.88 \text{ ms} \tag{14}$$

$$t_{WDL(MAX)} = 0.5 \times t_{WDU(MAX)} = 0.5 \times \left[1.05 \times \left(77.4 \times 2.2 \times 10^{-3} + 0.055\right)\right] = 118 \text{ ms} \tag{15}$$

Capacitor tolerance also influences $t_{WDU(MIN)}$ and $t_{WDL(MAX)}$. Select a ceramic COG dielectric capacitor for high accuracy. For 2.2 nF, COG capacitors are readily available with a 5% tolerance, resulting in a 5% decrease in $t_{WDU(MIN)}$ and a 5% increase in $t_{WDL(MAX)}$, giving 181 ms and 135 ms, respectively. A falling edge must be issued within this window.

8.2.2.2.3 Watchdog Disabled During the Initialization Period

The watchdog is often needed to be disabled during startup to allow for an initialization period. When the initialization period is over, the watchdog timer is turned back on to allow the microcontroller to be monitored by the TPS3850-Q1. To achieve this setup, SET0 must start at VDD and SET1 must start at GND. In this design, SET0 is simply tied to VDD and SET1 is controlled by a TPS3890-Q1 supervisor. In this application, the TPS3890-Q1 was chosen to monitor V_{DD} as well, which means that $\overline{\text{RESET}}$ on the TPS3890-Q1 stays low until V_{DD} rises above V_{ITN}. When V_{DD} comes up, the delay time can be adjusted through the CT capacitor on the TPS3890-Q1. With this approach, the $\overline{\text{RESET}}$ delay can be adjusted from a minimum of 25 µs to a maximum of 30 seconds. For this design, a minimum delay of 7 seconds is needed until the watchdog timer is enabled. The CT capacitor calculation (see the TPS3890-Q1 data sheet) yields an ideal capacitance of 6.59 µF, giving a closest standard ceramic capacitor value of 6.8 µF. When connecting a 6.8-µF capacitor from CT to GND, the typical delay time is 7.21 seconds. 図 8-13 illustrates the typical startup waveform for this circuit when the watchdog input is off. 図 8-13 illustrates that when the watchdog is disabled, the $\overline{\text{WDO}}$ output remains high. See the TPS3890-Q1 data sheet for detailed information on the TPS3890-Q1.

8.2.2.2.4 Calculating the Sense Resistor

There are three key specifications to keep in mind when calculating the resistor divider values (R_1 and R_2, see 図 7-4 or 図 8-3): voltage threshold ($V_{IT(ADJ)}$), resistor tolerance, and the SENSE pin current (I_{SENSE}). To ensure that no accuracy is lost because of I_{SENSE}, the current through the resistor divider must be 100 times greater than I_{SENSE}. Starting with R_2 = 80.6 kΩ provides a 5-µA resistor divider current when V_{SENSE} = 0.4 V. To calculate the nominal resistor values, use 式 16:

$$V_{ITN} = V_{IT(ADJ)} + R_1 \frac{V_{IT(ADJ)}}{R_2} \tag{16}$$

where

- V_{ITN} is the monitored falling threshold voltage and
- $V_{IT(ADJ)}$ is the threshold voltage on the SENSE pin

Solving 式 16 for R_1 gives the nearest 1% resistor of 51.1 kΩ. Now, plug R_1 back into 式 16 to get the monitored threshold. With these resistor values, the nominal threshold is 0.65 V or 6.6%.

To calculate the minimum and maximum threshold variation including the tolerances of the resistors, threshold voltage, and sense current, use 式 17 and 式 18.

$$V_{ITN(min)} = V_{IT(ADJ)min} + R_{1(min)} \left(\frac{V_{IT(ADJ)min}}{R_{2(max)}} + I_{SENSE(min)} \right) = 0.641 \text{ V} \tag{17}$$

$$V_{ITN(max)} = V_{IT(ADJ)max} + R_{1(max)} \left(\frac{V_{IT(ADJ)max}}{R_{2(min)}} + I_{SENSE(max)} \right) = 0.667 \text{ V} \tag{18}$$

where

- V_{ITN} is the falling monitored threshold voltage
- $V_{IT(ADJ)}$ is the sense voltage threshold and
- I_{SENSE} is the sense pin current

The calculated tolerance on R_1 and R_2 is 1%.

8.2.2.3 Application Curves

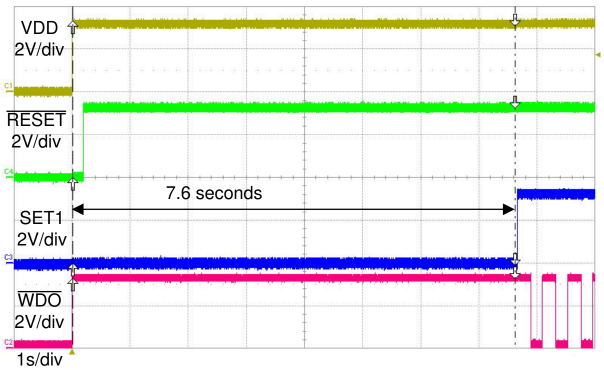


図 8-13. Startup Without a WDI Signal

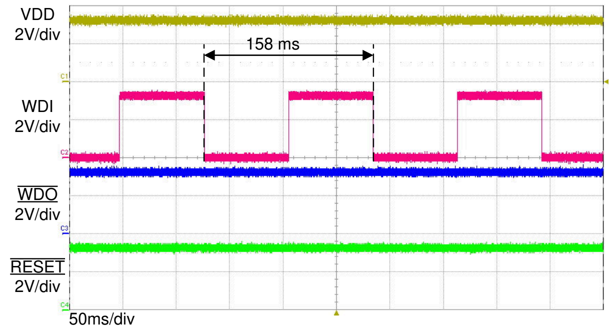


図 8-14. Typical WDI Signal

9 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.6 V and 6.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin.

10 Layout

10.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1-µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CRST pin, then minimize parasitic capacitance on this pin so the $\overline{\text{RESET}}$ delay time is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CRST} capacitor or pullup resistor is used, place these components as close as possible to the CRST pin. If the CRST pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- If a C_{CWD} capacitor or pullup resistor is used, place these components as close as possible to the CWD pin. If the CWD pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- Place the pullup resistors on $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ as close to the pin as possible.

10.2 Layout Example

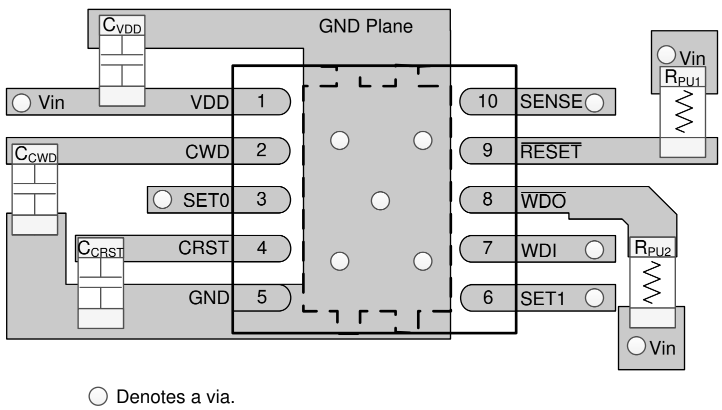


図 10-1. Typical Layout for the TPS3850-Q1

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

The *TPS3850EVM-781 Evaluation Module* can be used to evaluate this part.

11.1.2 Device Nomenclature

表 11-1. Device Nomenclature

DESCRIPTION	NOMENCLATURE	VALUE
TPS3850 (high-accuracy supervisor with window watchdog)	—	—
X (nominal thresholds as a percent of the nominal monitored voltage)	G	$V_{IT+(OV)}$ = 4%; $V_{IT-(UV)}$ = –4%
	H	$V_{IT+(OV)}$ = 7%; $V_{IT-(UV)}$ = –7%
yy(y) (nominal monitored voltage option)	01	0.4 V
	09	0.9 V
	115	1.15 V
	12	1.2 V
	18	1.8 V
	25	2.5 V
	30	3.0 V
	33	3.3 V
	50	5.0 V

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

-
- *TPS3890-Q1 Low Quiescent Current, 1% Accurate Supervisor with Programmable Delay*
- *Optimizing Resistor Dividers at a Comparator Input*
- *TPS3850EVM-781 Evaluation Module*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3850G09QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850BB
TPS3850G09QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850BB
TPS3850G12QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850CB
TPS3850G12QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850CB
TPS3850G18QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850DB
TPS3850G18QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850DB
TPS3850G25QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850EB
TPS3850G25QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850EB
TPS3850G30QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850FB
TPS3850G30QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850FB
TPS3850G33QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850GB
TPS3850G33QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850GB
TPS3850G50QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850HB
TPS3850G50QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850HB
TPS3850H01QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	(850AA, 850AB)
TPS3850H01QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(850AA, 850AB)
TPS3850H09QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850JB
TPS3850H09QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850JB
TPS3850H12QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850KB
TPS3850H12QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850KB
TPS3850H18QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850LB
TPS3850H18QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850LB
TPS3850H25QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850MB
TPS3850H25QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850MB
TPS3850H30QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850NB
TPS3850H30QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850NB
TPS3850H33QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850PB
TPS3850H33QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850PB
TPS3850H50QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	850RB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3850H50QDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	850RB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3850-Q1 :

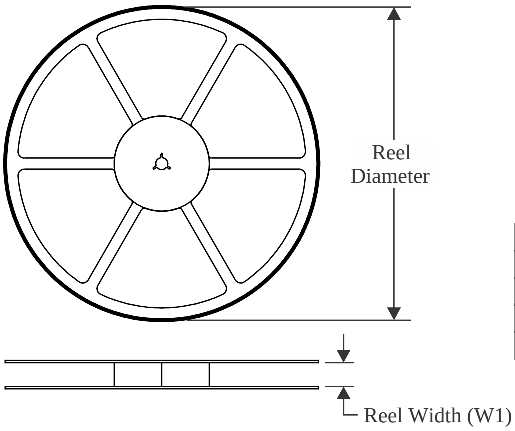
- Catalog : TPS3850

NOTE: Qualified Version Definitions:

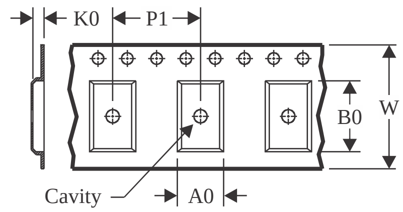
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

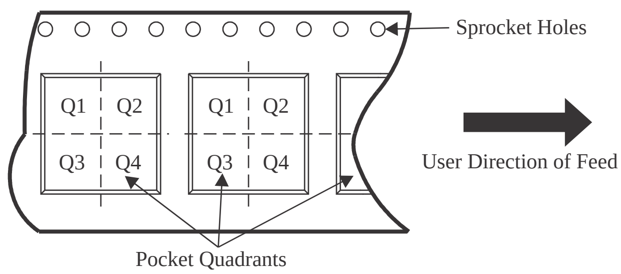


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

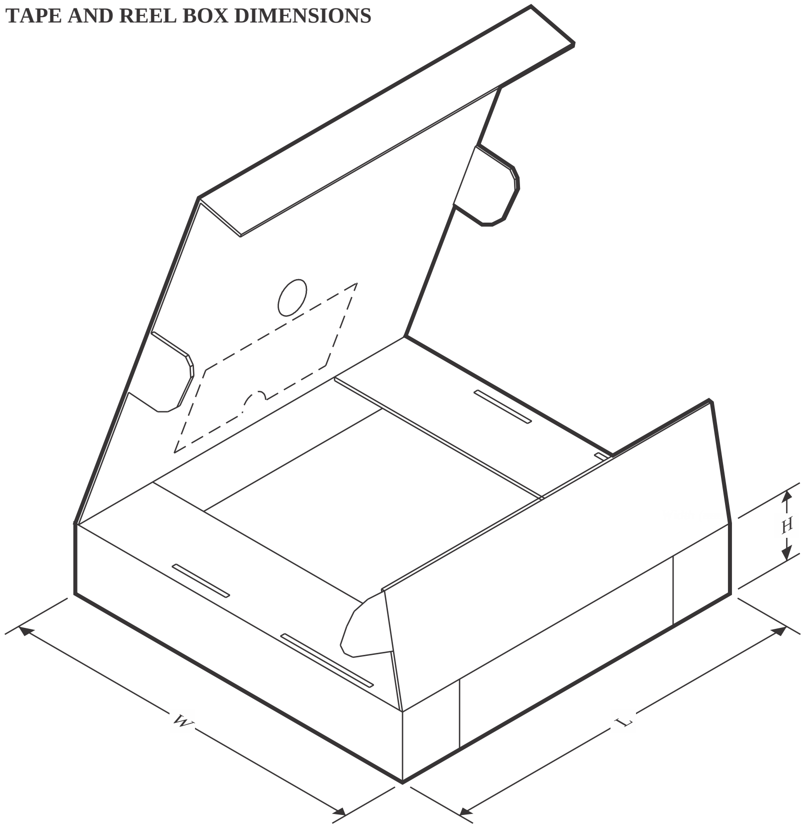
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3850G09QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G12QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G18QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G25QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G30QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G33QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G50QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H01QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H09QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H12QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H18QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H25QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H30QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H33QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H50QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3850G09QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G12QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G18QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G25QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G30QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G33QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G50QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H01QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H09QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H12QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H18QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H25QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H30QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H33QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H50QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0

重要なお知らせと免責事項