

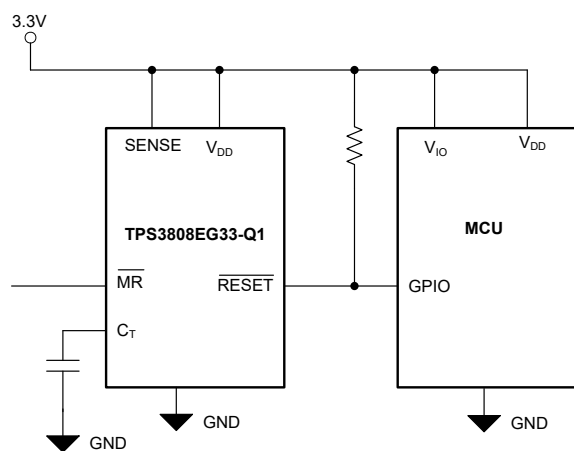
TPS3808E 低静止時電流、プログラマブル遅延監視回路

1 特長

- 電源レールの低電圧監視
 - 高いスレッショルド精度 (標準値 1%) による信頼性の高い監視
 - 0.9V～5V の固定電圧スレッショルド オプション
 - 可変電圧オプションを提供 (0.405)
 - 監視用のセンスピンと電力用の V_{DD} ピンを分離
 - デバイス温度グレード 1: -40°C ~ +125°C
- 超低消費電力の小型ソリューション
 - 静止電流: 0.6μA (代表値)
 - コンパクトな 6 ピン SOT-23 パッケージ (2.99mm × 1.6mm)
- 安全でない電源オンを防止する、高度に構成可能なリセット時間遅延
 - 1.25ms ~ 10s で可変
- オンデマンドで RESET 出力をアサートする個別のマニュアルリセット入力 (MR)

2 アプリケーション

- ラック・サーバー向けマザーボード
- 電気メータ
- DC 入力 BLDC モーター・ドライブ
- AC ドライブ電力段モジュール
- 外科用機器
- シングル・ボード・コンピュータ



代表的なアプリケーション

3 概要

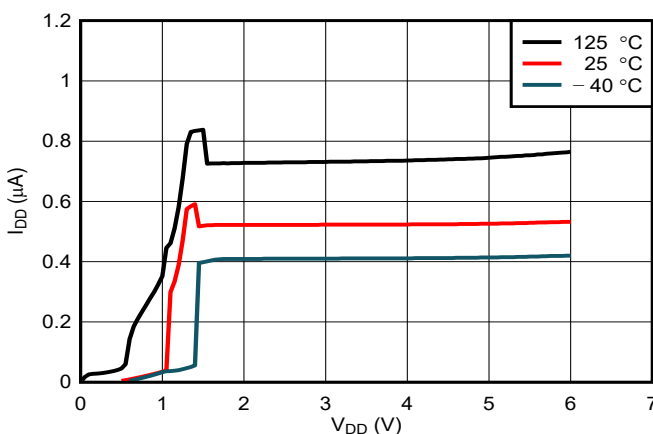
TPS3808E ファミリーはマイクロプロセッサ監視回路で、0.4V～5V のシステム電圧を監視でき、SENSE 電圧が設定済みのスレッショルドより低下したとき、またはマニュアルリセット (MR) ピンが論理 LOW に低下したとき、オープンドレインの RESET 信号をアサートします。RESET 出力は、SENSE 電圧とマニュアルリセット (MR) がそれぞれのスレッショルド以上に復帰した後も、ユーザーが設定した遅延時間だけ LOW に維持されます。

TPS3808E デバイスは、高精度の基準電圧を使用して、0.5% のスレッショルド精度を実現しています。リセット遅延時間は、 C_T ピンを未接続にすることで 20ms に設定でき、抵抗を使用して C_T ピンを V_{DD} に接続することで 300ms に設定できます。または、 C_T ピンを外部コンデンサに接続することで 1.25ms～10s の範囲でユーザーが調整することもできます。TPS3808E デバイスは、静止電流が 0.6μA (代表値) と非常に小さいため、バッテリー駆動のアプリケーション向けに設計されています。TPS3808E は SOT-23 (6) で供給され、-40°C～125°C (T_J) の温度範囲で完全に動作が規定されています。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
TPS3808E	SOT-23 (6)	2.90mm × 1.60mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



消費電流と電源電圧との関係



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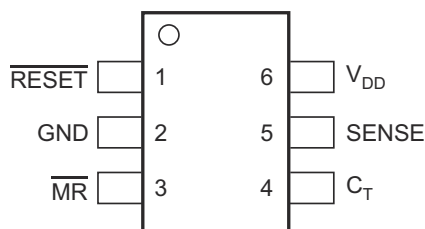
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4 Device Voltage Thresholds

The following table shows the nominal rail to be monitored and the corresponding threshold voltage of the device.

PART NUMBER	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE (V_{IT})
TPS3808EG01	Adjustable	0.405V
TPS3808EG09	0.9V	0.84V
TPS3808EG12	1.2V	1.12V
TPS3808EG125	1.25V	1.16V
TPS3808EG15	1.5V	1.40V
TPS3808EG18	1.8V	1.67V
TPS3808EG19	1.9V	1.77V
TPS3808EG25	2.5V	2.33V
TPS3808EG30	3V	2.79V
TPS3808EG33	3.3V	3.07V
TPS3808EG50	5V	4.65V

5 Pin Configuration and Functions



**図 5-1. DBV Package
6-Pin SOT-23
Top View**

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOT-23		
C_T	4	I	Reset period programming pin. Connecting this pin to V_{DD} through a 40k Ω to 200k Ω resistor or leaving it open results in fixed delay times. Connecting this pin to a ground referenced capacitor ≥ 130 pF gives a user-programmable delay time.
GND	2	—	Ground
$\overline{MR}$	3	I	Driving the manual reset pin ($\overline{MR}$) low asserts RESET. $\overline{MR}$ is internally tied to V_{DD} by a 90k Ω pull-up resistor.
RESET	1	O	RESET is an open-drain output that is driven to a low-impedance state when RESET is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the $\overline{MR}$ pin is set to a logic low). RESET remains low (asserted) for the reset period after both SENSE is above V_{IT} and $\overline{MR}$ is set to a logic high. A pull-up resistor from 10k Ω to 1M Ω must be used on this pin, this allows the reset pin to attain voltages higher than V_{DD} .
SENSE	5	I	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT} , then RESET is asserted.
V_{DD}	6	I	Supply voltage. For good analog design, place a 0.1 μ F ceramic capacitor close to this pin.

6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	V_{DD} , V_{CT} , V_{RESET} , V_{MR} , V_{SENSE}	-0.3	6.5	V
Current	I_{RESET}		±5	mA
Temperature ⁽²⁾	Operating junction temperature, T_J	-40	150	°C
	Operating free-air temperature, T_A	-40	150	°C
	Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.7		6	V
V_{SENSE}	Input pin voltage	0		6	V
V_{CT}	CT pin voltage			V_{DD}	V
V_{MR}	MR pin Voltage	0		6	V
V_{RESET}	Output pin voltage	0		6	V
I_{RESET}	Output pin current	0		5	mA
T_J	Junction temperature (free-air temperature)	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3808E	UNIT
		DBV (SOT23-6)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	131.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	67.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	91.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

At $1.7\text{ V} \leq V_{DD} \leq 6\text{ V}$, CT = MR = Open, RESET Voltage (V_{RESET}) = 100 k Ω to V_{DD} , RESET load = 50pF, and over the operating free-air temperature range of -40°C to 125°C, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		1.7		6	V
V_{POR}	Power on reset voltage ⁽²⁾	$V_{OL(max)} = 0.25\text{ V}$, $I_{OUT} = 15\text{ }\mu\text{A}$			1	V
$V_{IT-(UV)}$	Negative-going threshold accuracy	Fixed threshold TPS3808EG01	-2	± 1	2	%
$V_{IT-(UV)}$	Negative-going threshold accuracy		-1.5	± 0.5	1.5	%
V_{HYS}	Hysteresis Voltage ⁽¹⁾	Fixed Vth		1	2.5	%
V_{HYS}	Hysteresis Voltage ⁽¹⁾	Adjustable Vth		1	2.5	%
I_{DD}	Supply current	$V_{DD} = 3.3\text{ V}$		0.6	1.5	μA
I_{DD}	Supply current	$V_{DD} = 6\text{ V}$		0.6	1.5	μA
I_{SENSE}	Input current, SENSE pin	$V_{SENSE} = V_{IT}$, TPS3808EG01	-25		25	nA
I_{SENSE}	Input current, SENSE pin	$V_{SENSE} = 6\text{ V}$, Fixed Versions		0.75	1.25	μA
V_{OL}	Low level output voltage	$1.7\text{ V} \leq V_{DD} < 6\text{ V}$, $I_{OUT} = 1\text{ mA}$			400	mV
I_{LKG}	Open drain output leakage current	$V_{DD} = V_{RESET} = 6\text{ V}$			300	nA
V_{MR_L}	MR logic low input				0.3 V_{DD}	V
V_{MR_H}	MR logic high input		0.7 V_{DD}			V
R_{MR}	Manual reset Internal pullup resistance			90		K Ω

- (1) Hysteresis is with respect of the tripoint $V_{IT-(UV)}$.
(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state.

6.6 Timing Requirements

At $1.7\text{ V} \leq V_{DD} \leq 6\text{ V}$, $CT = MR = \text{Open}$, $\overline{\text{RESET}}$ Voltage ($V_{\overline{\text{RESET}}}$) = $100\text{ k}\Omega$ to V_{DD} , $\overline{\text{RESET}}$ load = 50 pF , and over the operating free-air temperature range of -40°C to 125°C , unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

			MIN	NOM	MAX	UNIT
t_D	Reset time delay	$CT = \text{Open}$	12	20	28	ms
t_D	Reset time delay	$CT = V_{DD}$	180	300	420	ms
t_D	Reset time delay	$CT = 130\text{ pF}$	0.75	1.25	1.75	ms
t_D	Reset time delay	$CT = 150\text{ nF}$		0.83		s
t_{PD}	Propagation detect delay ^{(1) (2)}			30	50	μs
t_{SD}	Startup delay ⁽³⁾			300		μs
$t_{GI}(\text{VIT-})$	Glitch Immunity undervoltage $V_{IT-(UV)}$, 5% Overdrive ⁽¹⁾			5		μs
$t_{GI}(\overline{\text{MR}})$	Glitch Immunity $\overline{\text{MR}}$ pin			50		ns
$t_{PD}(\overline{\text{MR}})$	Propagation delay from $\overline{\text{MR}}$ low to assert $\overline{\text{RESET}}$			500		ns

(1) 5% Overdrive from threshold. Overdrive % = $[V_{\text{SENSE}} - V_{IT}] / V_{IT}$; Where V_{IT} stands for $V_{IT-(UV)}$

(2) t_{PD} measured from threshold trip point ($V_{IT-(UV)}$ or $V_{IT+(OV)}$) to $\overline{\text{RESET}}$ V_{OL} voltage

(3) During the power-on sequence, V_{DD} must be at or above $V_{DD(MIN)}$ for at least $t_{SD} + t_D$ before the output is in the correct state.

6.7 Timing Diagram

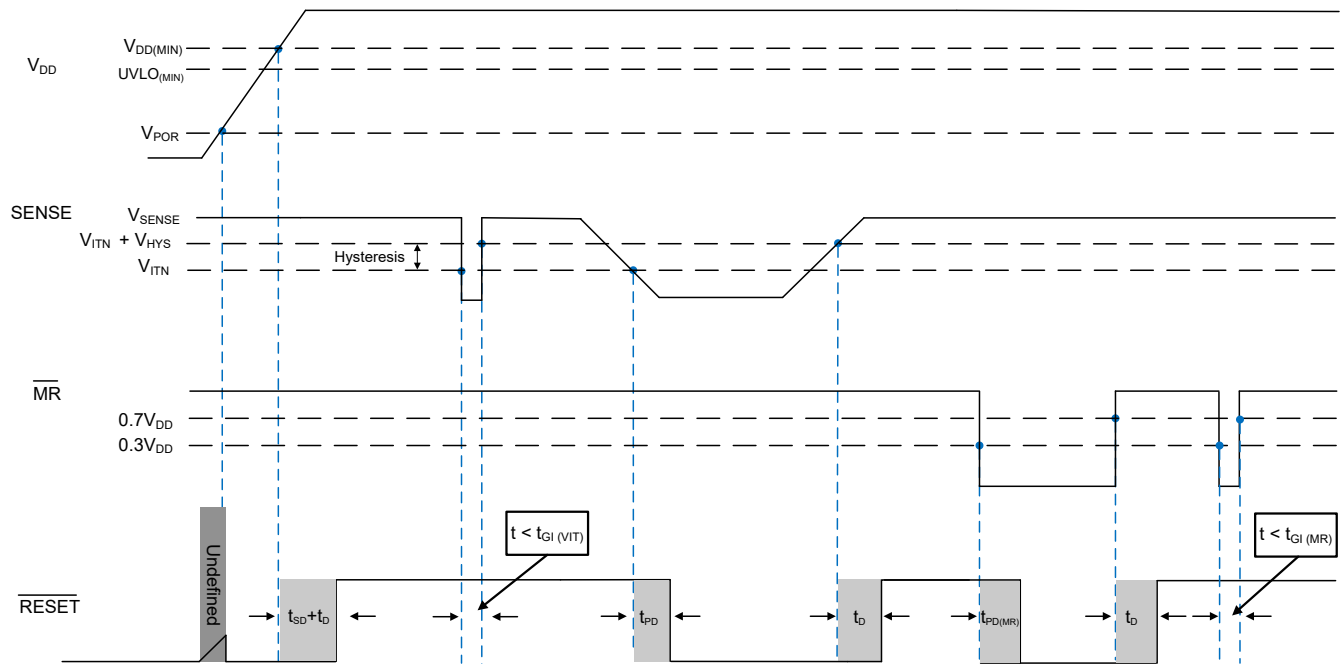


图 6-1. Timing Diagram

7 Typical Characteristics

At $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, $R_{LRESET} = 100\text{k}\Omega$, and $C_{LRESET} = 50\text{pF}$, unless otherwise noted.

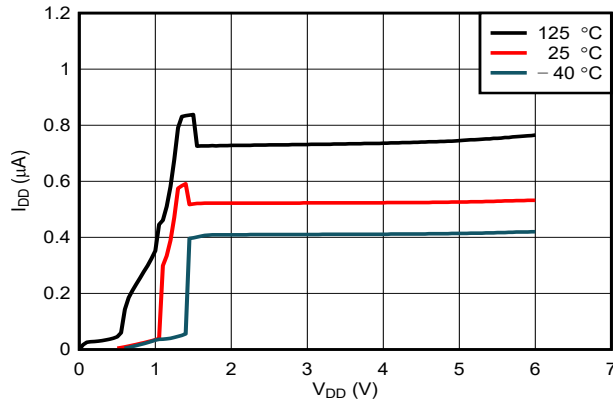


Figure 7-1. Supply Current vs Supply Voltage

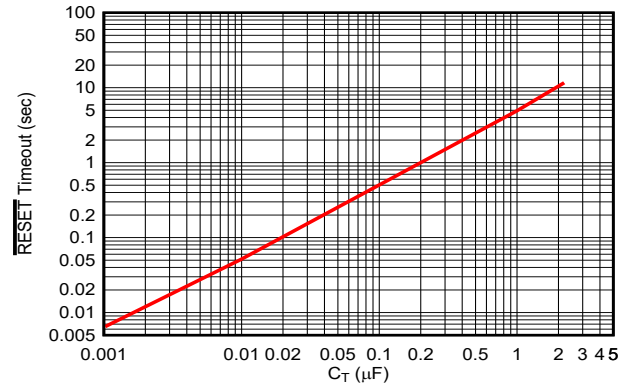


Figure 7-2. RESET Time-Out Period vs C_T

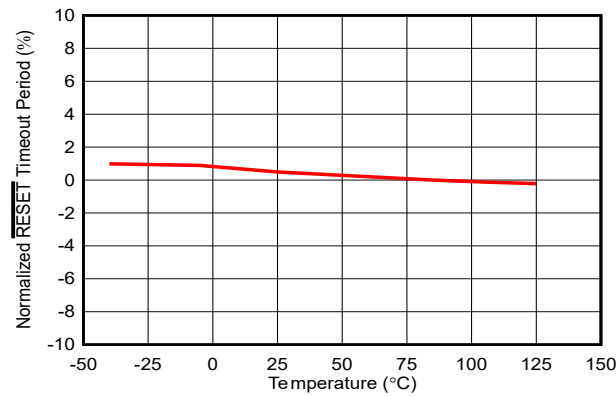


Figure 7-3. Normalized RESET Time-Out Period vs Temperature ($C_T = \text{Open}$, $C_T = V_{DD}$, $C_T = \text{Any}$)

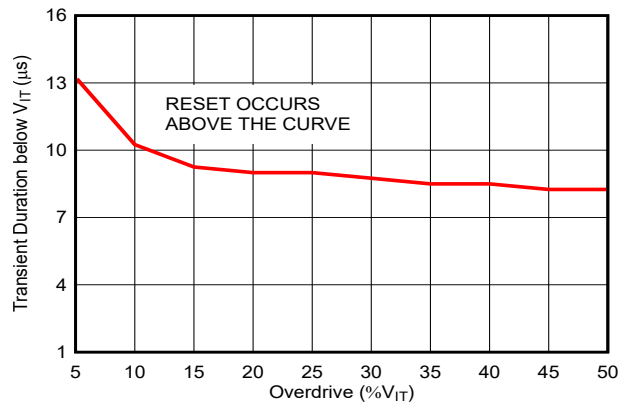


Figure 7-4. Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage

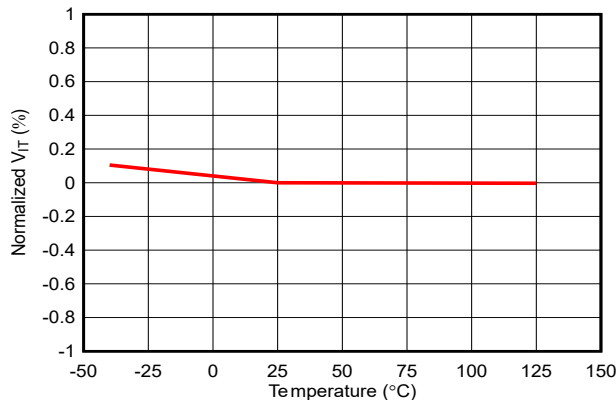


Figure 7-5. Normalized Sense Threshold Voltage (V_{IT}) vs Temperature

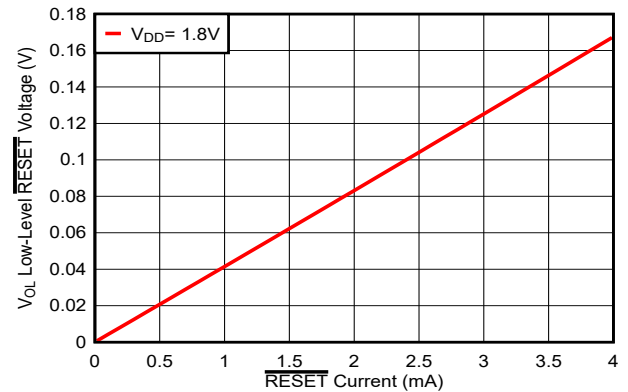


Figure 7-6. Low-Level RESET Voltage vs RESET Current

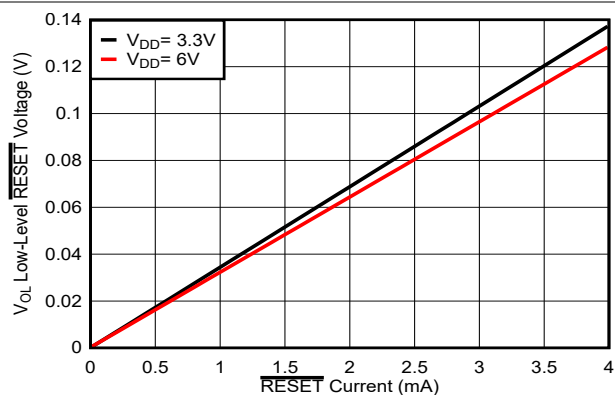


図 7-7. Low-Level RESET Voltage vs RESET Current

8 Detailed Description

8.1 Overview

The TPS3808E microprocessor supervisory product family is a low quiescent current single channel supervisor which has programmable delay time and manual reset features. TPS3808E is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{IT} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above their respective thresholds.

TPS3808E product family comes with fixed threshold options, which eliminates the need of external resistor divider and can monitor the standard voltage rails from 0.9V to 5V, and adjustable threshold option, which can monitor down to 0.4V with both high threshold accuracy. By connecting an external resistor divider, the adjustable version also can also monitor standard voltage rails.

8.2 Functional Block Diagram

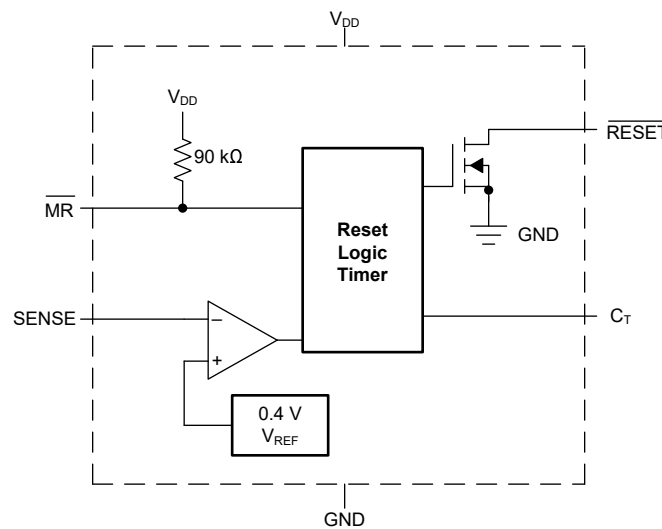


図 8-1. Adjustable Voltage Version

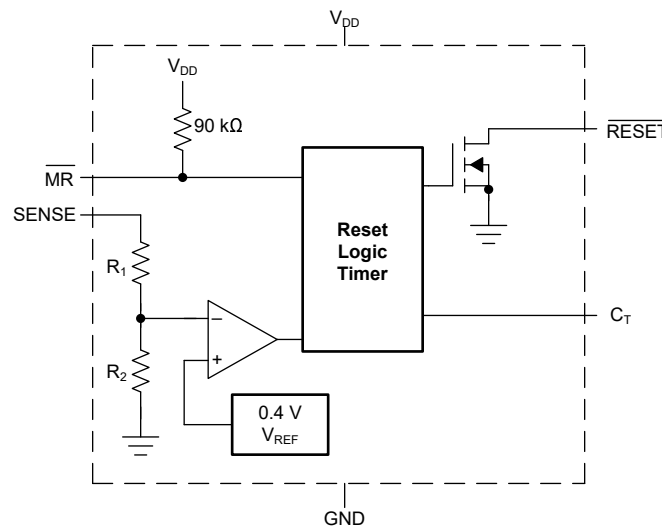


図 8-2. Fixed Voltage Version

8.3 Feature Description

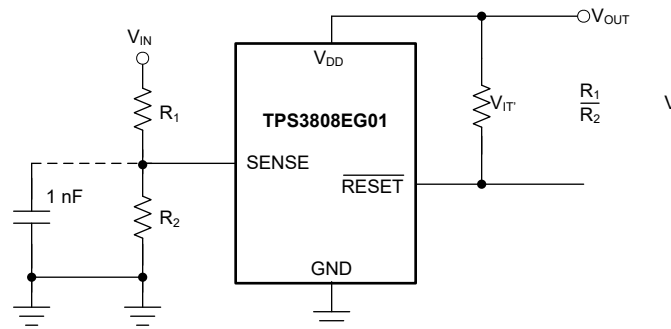
A broad range of voltage threshold and reset delay time adjustments are available for the TPS3808E device, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5V, while the adjustable variant can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300ms reset delay, whereas leaving the C_T pin open yields a 20ms reset delay. In addition, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25ms to 10s.

8.3.1 SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT} , then $\overline{\text{RESET}}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3808E device is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive.

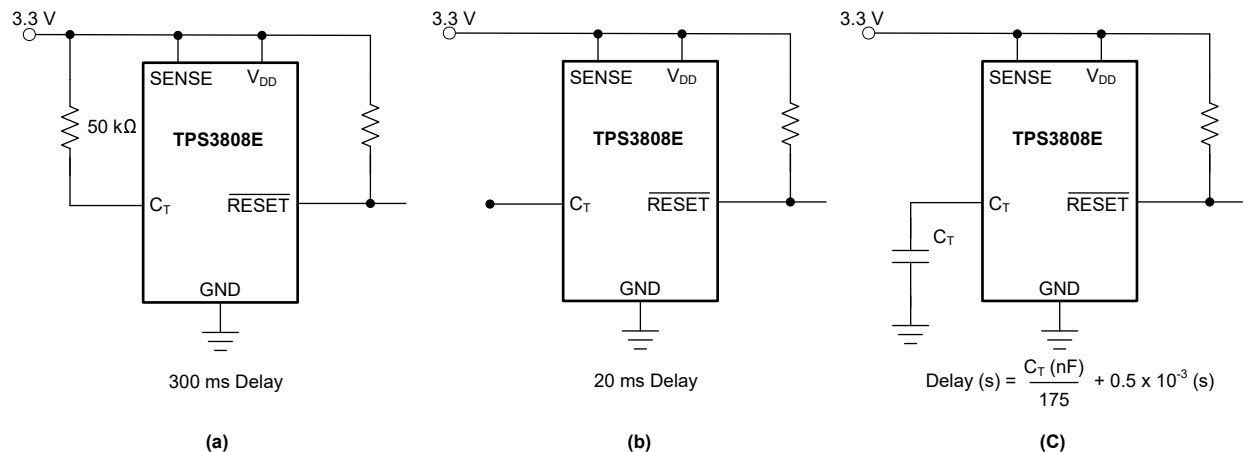
The adjustable variant can be used to monitor any voltage rail down to 0.405V using the circuit shown in 8-3.



8-3. Using the TPS3808EG01 to Monitor a User-Defined Threshold Voltage

8.3.2 Selecting the RESET Delay Time

The TPS3808E has three options for setting the $\overline{\text{RESET}}$ delay time as shown in 8-4. 8-4 (a) shows the configuration for a fixed 300ms typical delay time by tying C_T to V_{DD} ; a resistor from 40kΩ to 200kΩ must be used. Supply current is not affected by the choice of resistor. 8-4 (b) shows a fixed 20ms delay time by leaving the C_T pin open. 8-4 (c) shows a ground referenced capacitor connected to C_T for a user-defined program time between 1.25ms and 10s.



8-4. Configuration Used to Set the $\overline{\text{RESET}}$ Delay Time

The capacitor C_T must be $\geq 100\text{pF}$ nominal value for the TPS3808Exxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using 式 1.

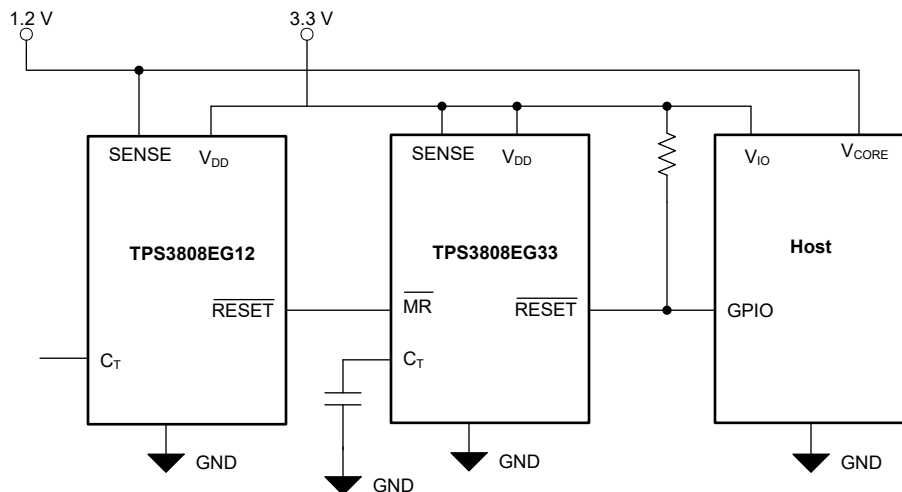
$$C_T (\text{nF}) = [t_D (\text{s}) - 0.5 \times 10^{-3} (\text{s})] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to the internal threshold. When a RESET is asserted, the capacitor is discharged. When the RESET conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches higher than the internal threshold, RESET is deasserted. Note that a low-leakage type capacitor such as a ceramic must be used, and that stray capacitance around this pin may cause errors in the reset delay time.

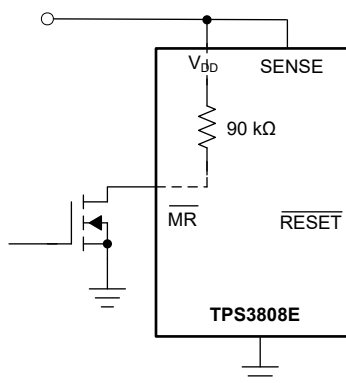
8.3.3 Manual RESET ($\overline{MR}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low ($0.3V_{\text{DD}}$) on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above the reset threshold, $\overline{\text{RESET}}$ is de-asserted after the user-defined reset delay expires. Note that $\overline{\text{MR}}$ is internally tied to V_{DD} using a 90k Ω resistor, so this pin can be left unconnected if $\overline{\text{MR}}$ is not used.

See [Fig. 8-5](#) for how $\overline{\text{MR}}$ can be used to monitor multiple system voltages. Note that if the logic signal driving $\overline{\text{MR}}$ does not go fully to V_{DD} , there is some additional current draw into V_{DD} as a result of the internal pullup resistor on $\overline{\text{MR}}$. To minimize current draw, a logic-level FET can be used as illustrated in [Fig. 8-6](#).



8-5. Using $\overline{\text{MR}}$ to Monitor Multiple System Voltages



8-6. Using an External MOSFET to Minimize I_{DD} When $\overline{MR}$ Signal Does Not Go to V_{DD}

8.3.4 RESET Output

$\overline{\text{RESET}}$ remains high (unasserted) as long as SENSE is above the threshold (V_{IT}) and the manual reset ($\overline{\text{MR}}$) is logic high. If either SENSE falls below V_{IT} or $\overline{\text{MR}}$ is driven low, $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to a low impedance.

Once $\overline{\text{MR}}$ is again logic high and SENSE is above $V_{IT} + V_{HYS}$ (the threshold hysteresis), a delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{\text{RESET}}$ pin goes to a high impedance state. The pullup resistor from the open-drain $\overline{\text{RESET}}$ to the supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than V_{DD} (up to 6V). The pullup resistor must be no smaller than 10k Ω as a result of the finite impedance of the $\overline{\text{RESET}}$ line.

8.4 Device Functional Modes

表 8-1. Truth Table

MR	SENSE > V_{IT}	RESET
L	0	L
L	1	L
H	0	L
H	1	H

8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{\text{RESET}}$ signal is determined by the voltage on the SENSE pin and the logic state of $\overline{\text{MR}}$.

- $\overline{\text{MR}}$ high: When the voltage on V_{DD} is greater than 1.7V for a time of the selected t_D , the $\overline{\text{RESET}}$ signal corresponds to the voltage on SENSE relative to V_{IT} .
- $\overline{\text{MR}}$ low: in this mode, $\overline{\text{RESET}}$ is held low regardless of the value of the SENSE pin.

8.4.2 Above Power-On Reset but Less Than $V_{DD(min)}$ ($V_{POR} < V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than the device $V_{DD(min)}$ voltage, and greater than the power-on reset voltage (V_{POR}), the $\overline{\text{RESET}}$ signal is asserted and low impedance, respectively, regardless of the voltage on the SENSE pin.

8.4.3 Below Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) needed to internally pull the asserted output to GND, $\overline{\text{RESET}}$ is undefined and should not be relied upon for proper device function.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

A typical application of the TPS3808E used with a 3.3V processor is shown in [Figure 9-1](#). The open-drain $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pullup resistor must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. The $\overline{\text{RESET}}$ output is undefined for voltage below 0.8V, but this characteristic is normally not a problem because most microprocessors do not function below this voltage.

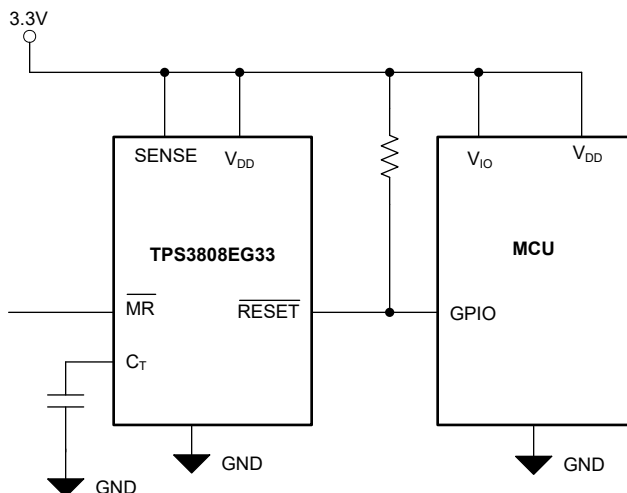


Figure 9-1. Typical Application of the TPS3808E With a C2000 Processor

9.2.1 Design Requirements

The TPS3808E is intended to drive the $\overline{\text{RESET}}$ input of a microprocessor. The $\overline{\text{RESET}}$ pin is pulled high with a 100k Ω resistor and the reset delay time is controlled by C_T depending on the reset requirement times of the microprocessor. In this case, C_T is left open for a typical reset delay time of 20ms.

9.2.2 Detailed Design Procedure

The primary constraint for this application is the reset delay time. In this case, because C_T is open, it is set to 20ms. A 0.1 μF decoupling capacitor is connected to the V_{DD} pin and a 100k Ω resistor is used to pull up the $\overline{\text{RESET}}$ pin high. The $\overline{\text{MR}}$ pin can be connected to an external signal if desired.

9.2.2.1 Immunity to SENSE Pin Voltage Transients

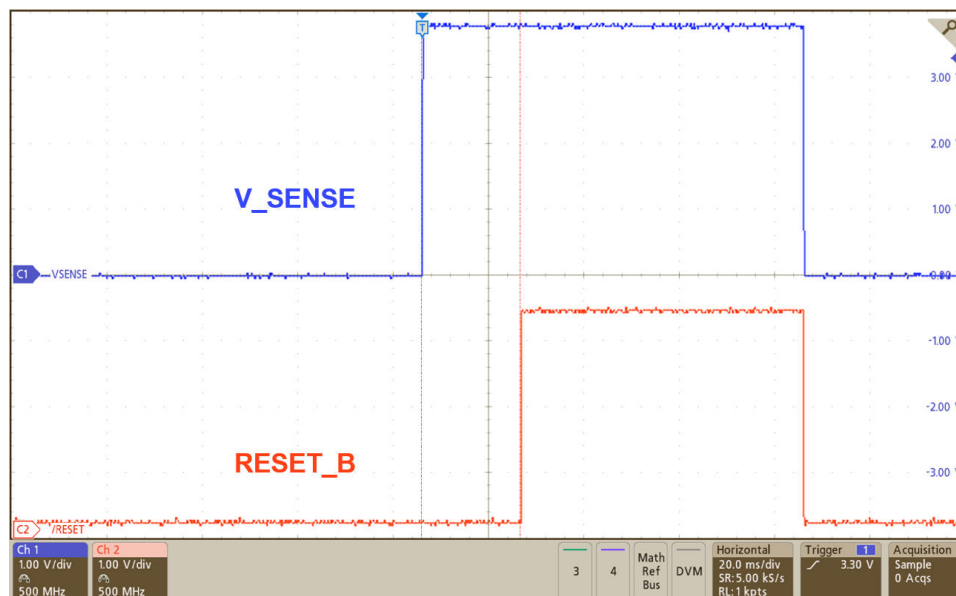
The TPS3808E is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients depends on threshold overdrive. Threshold overdrive is defined by how much the V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the RESET response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 2:

$$\text{Overdrive} = | (V_{\text{SENSE}} / V_{\text{IT}} - 1) \times 100\% | \quad (2)$$

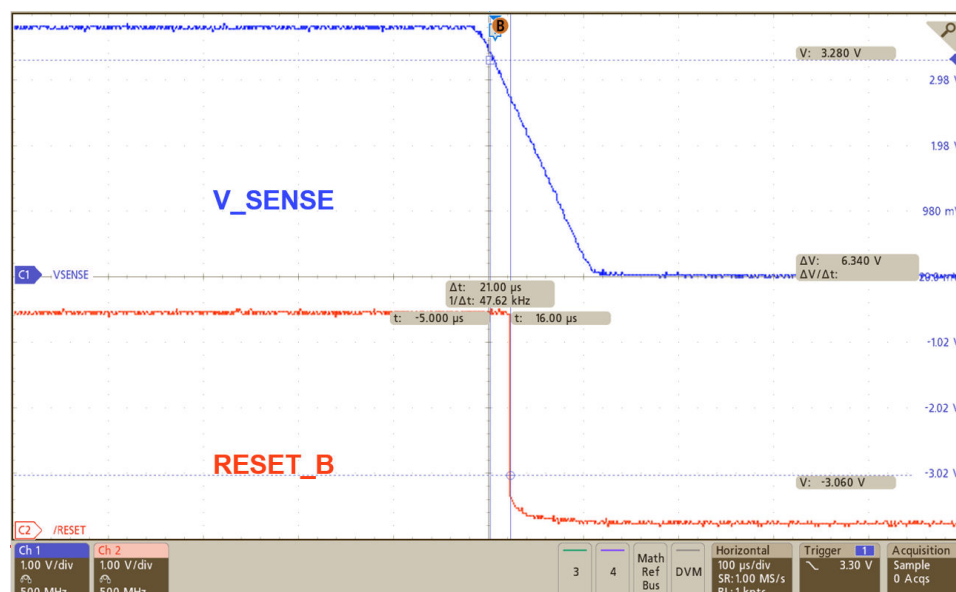
where:

- V_{IT} is the threshold voltage.

9.2.3 Application Curve



9-2. Reset Time Delay



9-3. Propagation Detect Delay

9.3 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.7V and 6V. Use a low-impedance power supply to eliminate inaccuracies caused by current changes during the voltage reference refresh.

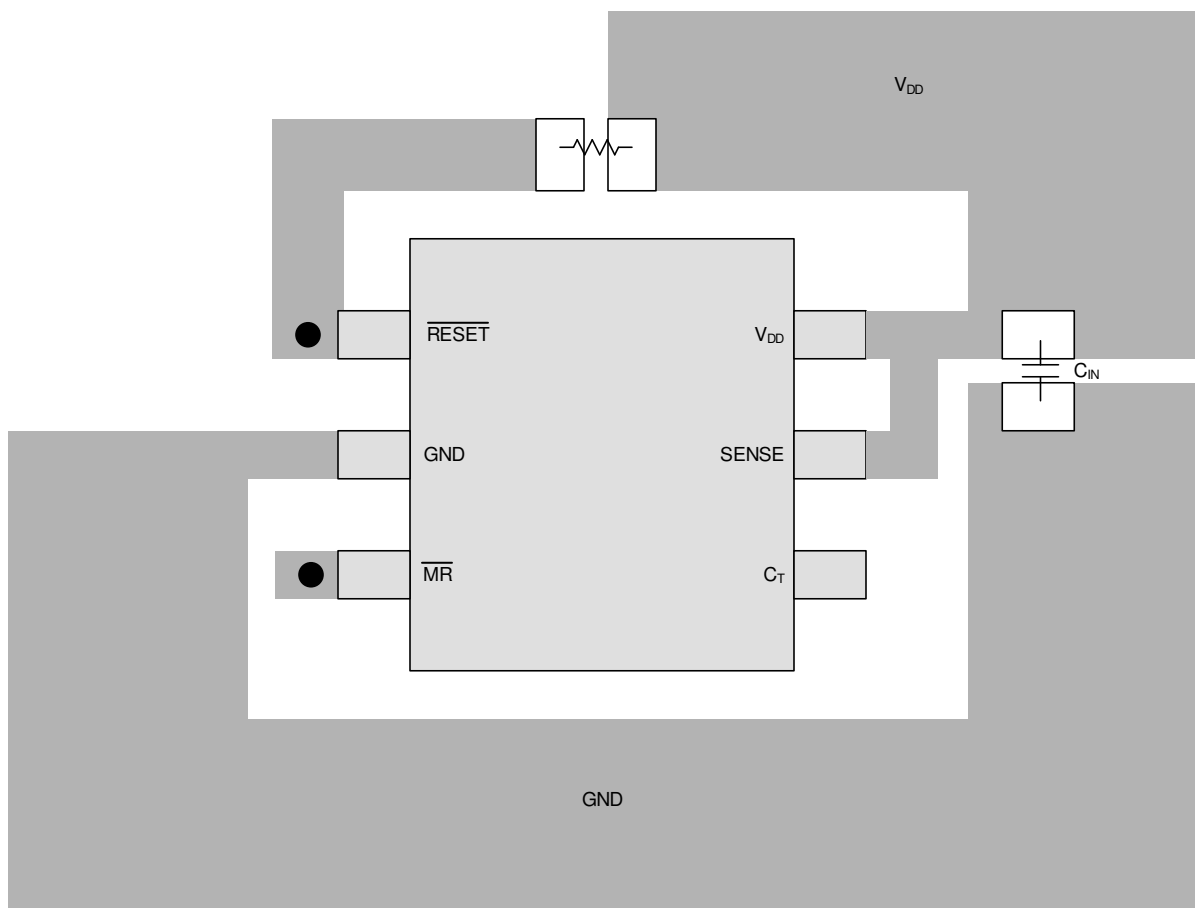
9.4 Layout

9.4.1 Layout Guidelines

Make sure the connection to the V_{DD} pin is low impedance. Place a 0.1 μ F ceramic capacitor near the V_{DD} pin. If no capacitor is connected to the C_T pin, parasitic capacitance on this pin must be minimized so the RESET delay time is not adversely affected.

9.4.2 Layout Example

The layout example in [Figure 9-4](#) shows how the TPS3808E is laid out on a printed circuit board (PCB) for a 20ms delay.



● Vias used to connect pins for application-specific connections

Figure 9-4. Layout Example for a 20ms Delay

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS3808E. The [TPS3808EG01DBVEVM evaluation module](#) can be requested at the Texas Instruments website through the product folders or purchased directly from the [TI eStore](#) and is compatible with the TPS3808E. TPS3808E sampled should be ordered and used to replace the existing TPS3808 device for testing.

10.2 Documentation Support

10.2.1 Related Documentation

The following related documents are available for download at www.ti.com:

- Application note. *Optimizing Resistor Dividers at a Comparator Input*. Literature number [SLVA450](#).
- Application note. *Sensitivity Analysis for Power Supply Design*. Literature number [SLVA481](#).
- TPS3808EG01DBVEVM Evaluation Module User Guide. Literature number [SBVU015](#).

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

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10.5 Trademarks

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10.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2023) to Revision B (December 2023)	Page
• 車載用の箇条書き項目を削除.....	1
• Removed Min and Max values for RMR.....	5

Changes from Revision * (May 2023) to Revision A (November 2023)	Page
• 量産データのリリース.....	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3808EG01DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG01
TPS3808EG01DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG01
TPS3808EG09DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG09
TPS3808EG09DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG09
TPS3808EG125DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	G125
TPS3808EG125DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	G125
TPS3808EG12DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG12
TPS3808EG12DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG12
TPS3808EG15DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG15
TPS3808EG15DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG15
TPS3808EG18DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG18
TPS3808EG18DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG18
TPS3808EG19DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG19
TPS3808EG19DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG19
TPS3808EG25DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG25
TPS3808EG25DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG25
TPS3808EG30DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG30
TPS3808EG30DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG30
TPS3808EG33DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG33
TPS3808EG33DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG33
TPS3808EG50DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	EG50
TPS3808EG50DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EG50

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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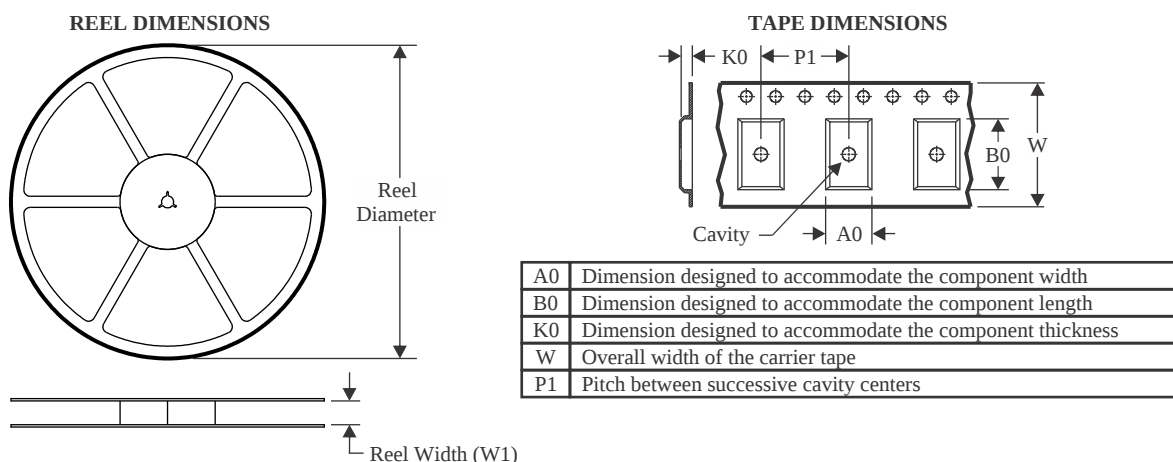
OTHER QUALIFIED VERSIONS OF TPS3808E :

- Automotive : [TPS3808E-Q1](#)

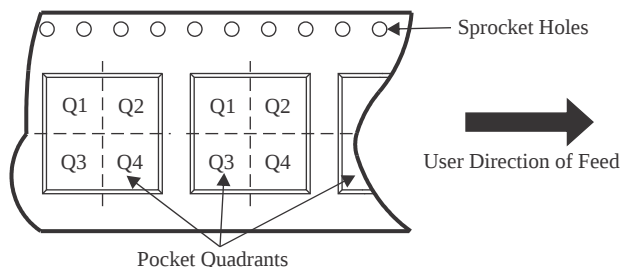
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808EG01DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG09DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG09DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG125DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG125DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG12DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG12DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG15DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG15DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG18DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG19DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG19DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG25DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG25DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG30DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG30DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808EG33DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG50DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808EG50DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808EG01DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG09DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG09DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG125DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG125DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG12DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG12DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG15DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG15DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG18DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG19DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG19DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG25DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG25DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG30DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG30DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG33DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3808EG50DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808EG50DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



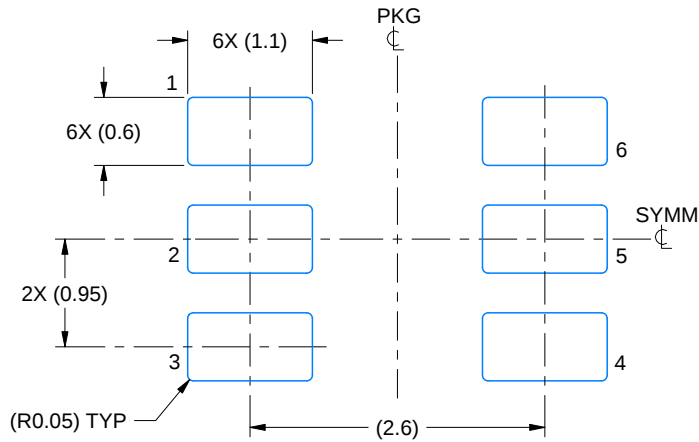
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

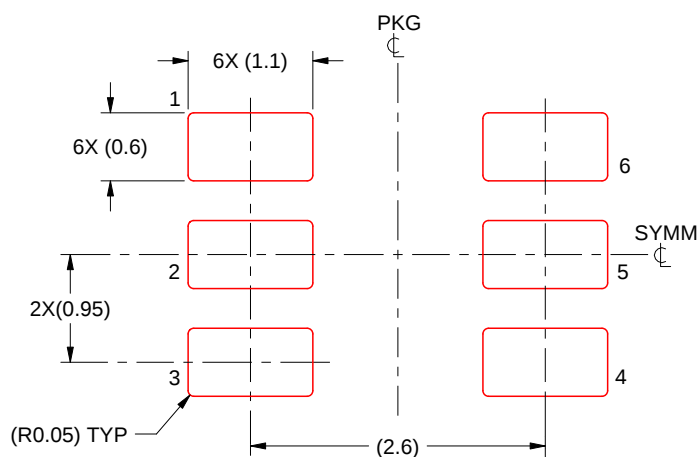
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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最終更新日：2025 年 10 月