

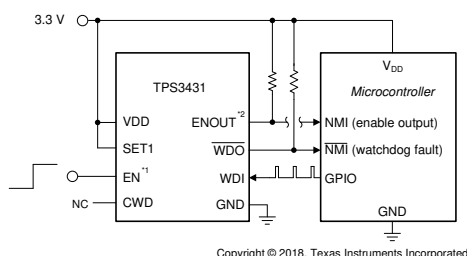
TPS3431-Q1 車載用、プログラム可能、イネーブル付き標準ウォッチドッグ・タイマ

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み:
 - デバイス温度グレード 1: $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ の動作時周囲温度範囲
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能
- 出荷時にプログラム可能な高精度ウォッチドッグ・タイマ
 - ウォッチドッグ・タイムアウト (WDT) の代表精度 $\pm 2.5\%$ (25°C)
- ウォッチドッグのディスエーブル機能
- ウォッチドッグのタイムアウトをユーザーがプログラム可能
- 入力電圧レンジ: $V_{\text{DD}} = 1.8\text{V} \sim 6.5\text{V}$
- 低い静止電流: $I_{\text{DD}} = 10\mu\text{A}$ (代表値)
- アクティブ LOW、オープン・ドレイン出力
- イネーブル入力 (EN) およびイネーブル出力 (ENOUT)
- 3mm × 3mm、8 ピン VSON の小型パッケージで供給
- 動作時の接合部温度範囲: $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$

2 アプリケーション

- 車載用センター情報ディスプレイ
- 車載ディスプレイ・モジュール
- デジタル・コックピット処理装置
- パワー・ディストリビューション・ボックス
- コンフォート・シート・モジュール
- 車載外部アンプ
- 二輪車向けインストルメント・クラス
- ボディ・コントロール・モジュール



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- EN はフローティング状態のままでかまいません。内部的に VDD にプルアップされます。
- ENOUT もフローティング状態にするか、または $\overline{\text{WDO}}$ に接続できます。

標準的なウォッチドッグ・タイマ回路

3 概要

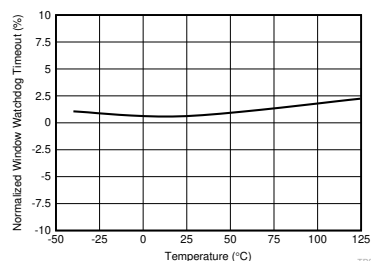
TPS3431-Q1 は、車載アプリケーションに適したイネーブル機能付き車載用標準プログラマブル・ウォッチドッグ・タイマです。ウォッチドッグ・タイムアウトは優れたタイミング精度を特長としています ($-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ で 15%、 25°C で 2.5% (標準値))。このウォッチドッグ・タイムアウトは、外付けのコンデンサと、出荷時にプログラムされるデフォルトの遅延設定のどちらかで設定できます。ウォッチドッグはイネーブル・ピンまたは SET ロジック・ピンにより無効化でき、開発プロセスで不要なウォッチドッグ・タイムアウトを避けられます。

TPS3431-Q1 は、3.00mm × 3.00mm の小型 8 ピン VSON パッケージで供給されます。TPS3431-Q1 では、光学検査を容易にするウェットアップ・フラングを採用しています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS3431-Q1	VSON (8)	3.00mm × 3.00mm

- 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



正規化されたウォッチドッグ・タイムアウト (t_{WD}) 精度 (SET1 = 1、CWD = NC)



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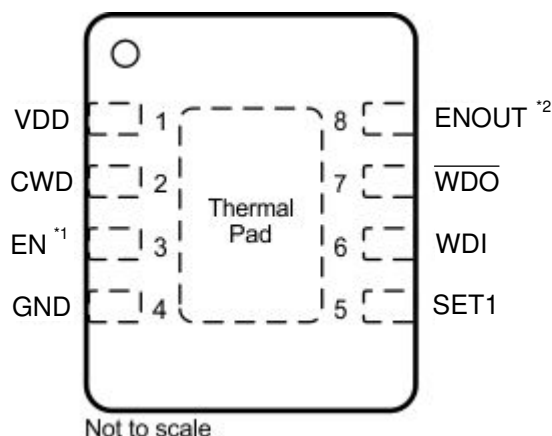
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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (July 2018) to Revision A (June 2021)	Page
・「ウォッチドッグ・タイムアウトおよびウォッチドッグ・リセット遅延の温度範囲全体にわたる $\pm 15\%$ の精度」を削除.....	1
・文書全体にわたって表、図、相互参照の採番方法を更新.....	1
・「機能安全対応」の箇条書き項目を追加.....	1
・「アプリケーション」セクションの Web リンクを更新.....	1
・「15%のタイミング精度 ($-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$)」を削除.....	1
・「TPS3431-Q1 では、光学検査を容易にするウェッタブル・フランクを採用しています」を追加.....	1
・Updated ESD Ratings.....	4
・Updated I_{CWD} min and max spec.....	5
・Updated V_{CWD} min and max spec.....	5
・Added a footnote to for t_{NIT}	6
・Updated t_{WDU} min and max boundry values from 0.85 and 1.15 to 0.905 and 1.095 respectively.....	13
・Updated t_{WDU} min and max values for all capacitors.....	13
・Updated the equations 3 and 4 with t_{WD} min and max boundry values from 0.85 and 1.15 to 0.905 and 1.095 respectively.....	17

5 Pin Configuration and Functions



- A. EN can also be left floating and is internally pulled-up to VDD
- B. ENOUT can also be left floating or tied to WDO

图 5-1. DRB Package: TPS3431
3-mm × 3-mm VSON-8
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	Supply voltage pin. For noisy systems, connecting a 0.1-μF bypass capacitor is recommended.
CWD	2	I	Programmable watchdog timeout input. The watchdog timeout is set by connecting a capacitor between this pin and ground. Connecting via a 10-kΩ resistor to VDD or leaving unconnected further enables the selection of the preset watchdog timeouts; see the CWD Functionality section. The TPS3431-Q1 determines the watchdog timeout using 式 1
EN	3	I	Enable input pin. This pin is internally pulled up to VDD and must be logic high or left floating. When EN goes logic low, ENOUT goes logic low and WDI is ignored and WDO remains logic high. When EN goes logic high, ENOUT goes high (asserts) after the watchdog reset delay time (t _{RST}). This pin can also be driven with an external push-button, transistor, or microcontroller.
GND	4	—	Ground pin
SET1	5	I	Logic input. Grounding the SET1 pin disables the watchdog timer. SET1 and CWD select the watchdog timeouts; see the SET1 section.
WDI	6	I	Watchdog input. A falling edge must occur at WDI before the timeout (t _{WD}) expires. When the watchdog is not in use, the SET1 pin can be used to disable the watchdog. WDI is ignored when WDO is low (asserted) and when the watchdog is disabled. If the watchdog is disabled, WDI cannot be left unconnected and must be driven to either VDD or GND.
WDO	7	O	Watchdog open-drain active-low output. Connect WDO with a 1-kΩ to 100-kΩ resistor to the correct pull-up voltage rail (V _{PU}). WDO goes low (asserts) when a watchdog timeout occurs. When a watchdog timeout occurs, WDO goes low (asserts) for the watchdog reset delay time (t _{RST}). When EN goes low, WDO is in a high-impedance state and will be pulled to logic high.
ENOUT	8	O	Enable open-drain active-high output. Connect ENOUT with a 1-kΩ to 100-kΩ resistor to the correct pull-up voltage rail (V _{PU}). When EN goes logic high, ENOUT goes high impedance and pulls logic high (asserts) due to the external pull-up resistor after the watchdog reset delay time (t _{RST}). When EN is forced logic low, ENOUT goes low after 200 ns and remains logic low as long as EN is logic low.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range	VDD	−0.3	7	V
Output voltage range	ENOUT, WDO	−0.3	7	V
Voltage ranges	SET1, WDI, EN	−0.3	7	V
	CWD	−0.3	VDD + 0.3 ⁽³⁾	
Output pin current	ENOUT, WDO		±20	mA
Input current (all pins)			±20	mA
Continuous total power dissipation		See セクション 6.4	See セクション 6.4	
Temperature	Operating junction, T _J ⁽²⁾	−40	150	°C
	Operating free-air temperature, T _A ⁽²⁾	−40	150	
	Storage, T _{stg}	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) T_J = T_A as a result of the low dissipated power in this device.
- (3) The absolute maximum rating is V_{DD} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±4000	V
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply pin voltage	1.8		6.5	V
V _{SET1}	SET1 pin voltage	0		6.5	V
C _{CWD}	Watchdog timing capacitor	0.1 ⁽¹⁾		1000 ⁽¹⁾	nF
CWD	Pullup resistor to VDD	9	10	11	kΩ
R _{PU}	Pullup resistor, ENOUT and WDO	1	10	100	kΩ
I _{EN}	EN pin current			10	mA
I _{WDO}	Watchdog output current			10	mA
T _J	Junction Temperature	−40		125	°C

- (1) Using a C_{CWD} capacitor of 0.1 nF or 1000 nF gives a t_{WDU(typ)} of 62.74 ms or 77.45 seconds, respectively.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3431-Q1	UNIT
		DRB (VSON)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	47.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.5	
R _{θJB}	Junction-to-board thermal resistance	22.2	
Ψ _{JT}	Junction-to-top characterization parameter	1.3	
Ψ _{JB}	Junction-to-board characterization parameter	22.3	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	4.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

at 1.8 V ≤ V_{DD} ≤ 6.5 V over the operating temperature range of –40°C ≤ T_J ≤ +125°C (unless otherwise noted); the open-drain pullup resistors are 10 kΩ; typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
V _{DD} ^{(2) (3)}	Supply voltage		1.8		6.5	V
I _{DD}	Supply current			10	19	μA
V _{POR} ⁽¹⁾	Power-on reset voltage	V _{OL(MAX)} = 0.25 V			0.8	V
WINDOW WATCHDOG FUNCTION						
I _{EN}	EN pin internal pullup current	V _{EN} = 0V	500	620	700	nA
I _{CWD}	CWD pin charge current	CWD = 0.5 V	347	375	403	nA
V _{CWD}	CWD pin threshold voltage		1.196	1.21	1.224	V
V _{OL}	ENOUT, $\overline{\text{WDO}}$ output low	VDD = 5 V, I _{SINK} = 3 mA			0.4	V
I _D	ENOUT, $\overline{\text{WDO}}$ output leakage current	VDD = 1.8 V, V _{WDO} = 6.5 V			1	μA
V _{IL}	Low-level input voltage (EN, SET1)				0.25	V
V _{IH}	High-level input voltage (EN, SET1)		0.8			V
V _{IL(WDI)}	Low-level input voltage (WDI)				0.3 × V _{DD}	V
V _{IH(WDI)}	High-level input voltage (WDI)		0.8 × V _{DD}			V

- (1) When V_{DD} falls below V_{POR}, WDI and ENOUT is undefined.
 (2) When V_{DD} falls below V_{DD,MIN}, WDI is ignored and ENOUT is driven low
 (3) During power-on, V_{DD} must be a minimum 1.8 V for at least 300 μs before WDI is active and ENOUT is high impedance.

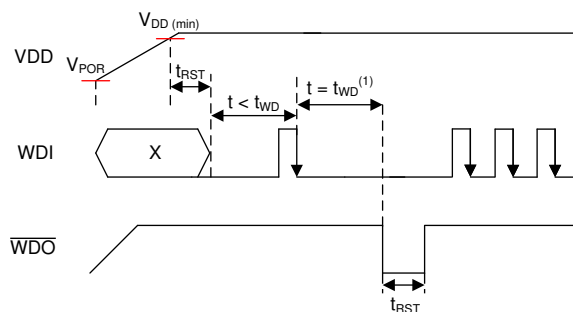
6.6 Timing Requirements

		MIN	TYP	MAX	UNIT	
GENERAL						
t _{INIT}	CWD pin evaluation period ⁽¹⁾		381		μs	
	EN, SET1 pin setup time		1		μs	
	Startup delay ⁽²⁾		300		μs	
DELAY FUNCTION						
t _{EN_ENOUT}	EN to ENOUT delay		200		ns	
t _{RST}	Watchdog reset delay	170	200	230	ms	
WINDOW WATCHDOG FUNCTION						
t _{WD}	Watchdog timeout	CWD = NC, SET1 = 1	1360	1600	1840	ms
		CWD = 10 kΩ to VDD, SET1 = 1	170	200	230	ms
		CWD = NC, SET1 = 0	Watchdog disabled			
		CWD = 10 kΩ to VDD, SET1 = 0	Watchdog disabled			
t _{WD-setup}	Setup time required for device to respond to changes on WDI after being enabled		150		μs	
	Minimum WDI pulse duration		50		ns	
t _{WD-del}	WDI to $\overline{\text{WDO}}$ delay		50		ns	

(1) Refer to [セクション 8.1.1.2](#).

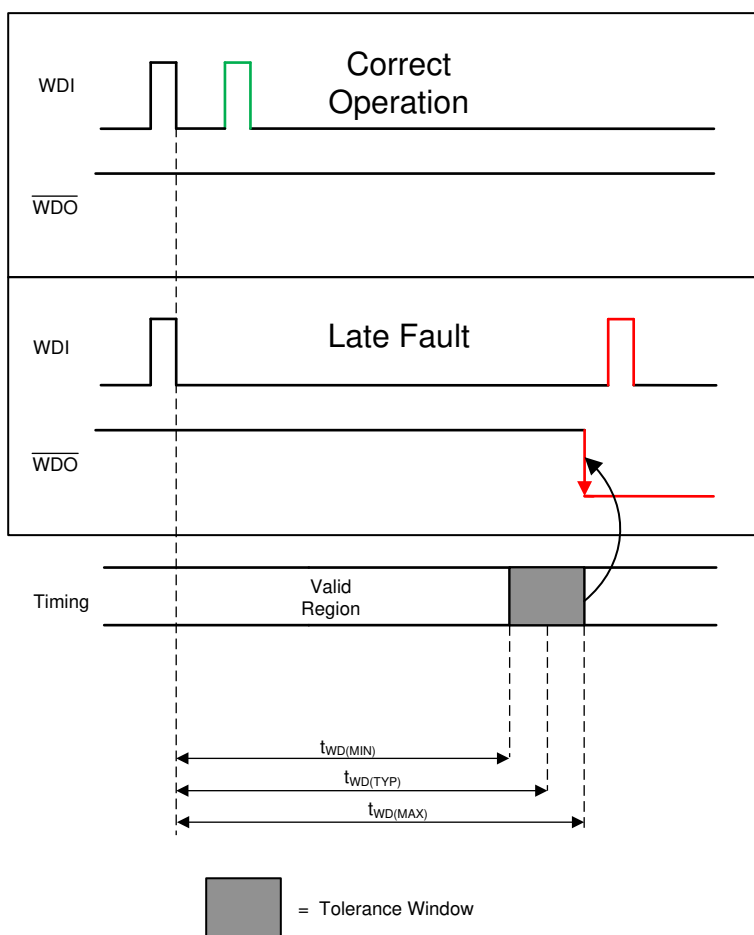
(2) During power-on, VDD must be a minimum 1.8 V for at least 300 μs before WDI is active and ENOUT is high impedance.

6.7 Timing Diagrams



6-1. Timing Diagram

A. See 6-2 for WDI timing requirements.



6-2. Watchdog Timing Diagram

6.8 Typical Characteristics

all typical characteristics curves are taken at 25°C with $1.8\text{ V} \leq V_{DD} \leq 6.5\text{ V}$ (unless other wise noted)

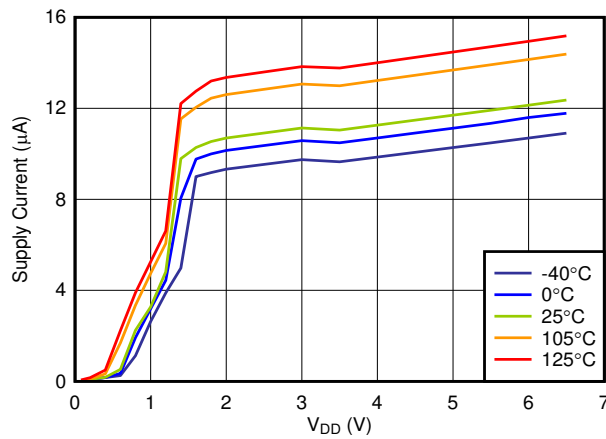


FIG 6-3. Supply Current vs V_{DD}

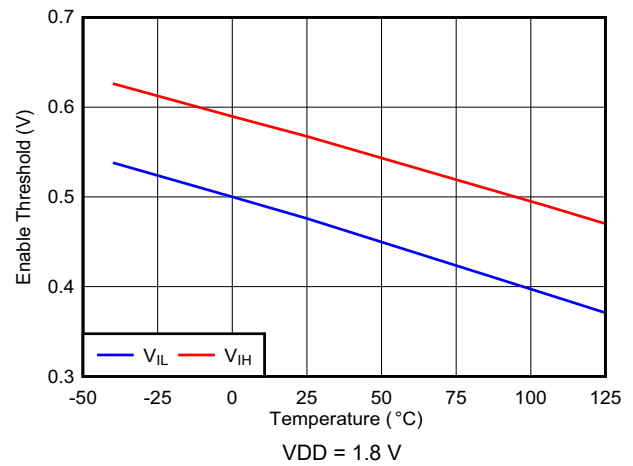


FIG 6-4. EN Threshold vs Temperature

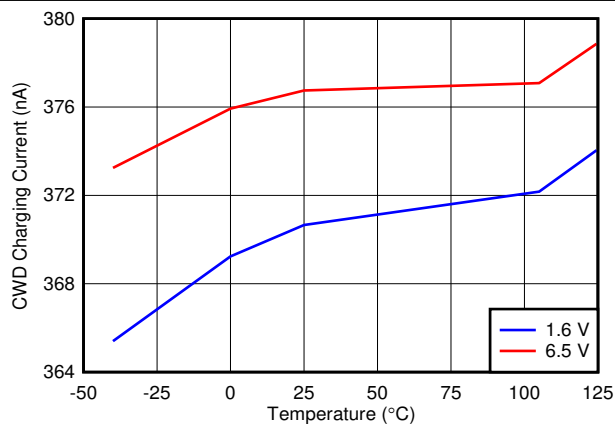


FIG 6-5. CWD Charging Current vs Temperature

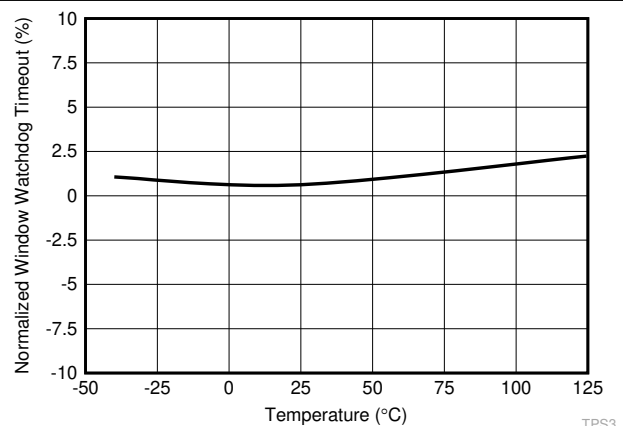


FIG 6-6. Normalized Watchdog Timeout (t_{WD}) Accuracy (SET1 = 1, CWD = NC)

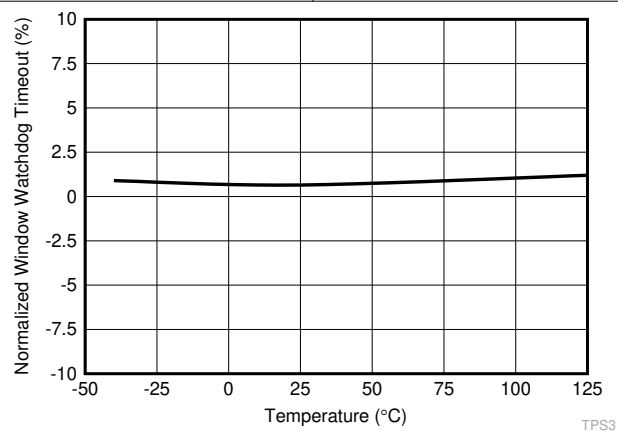


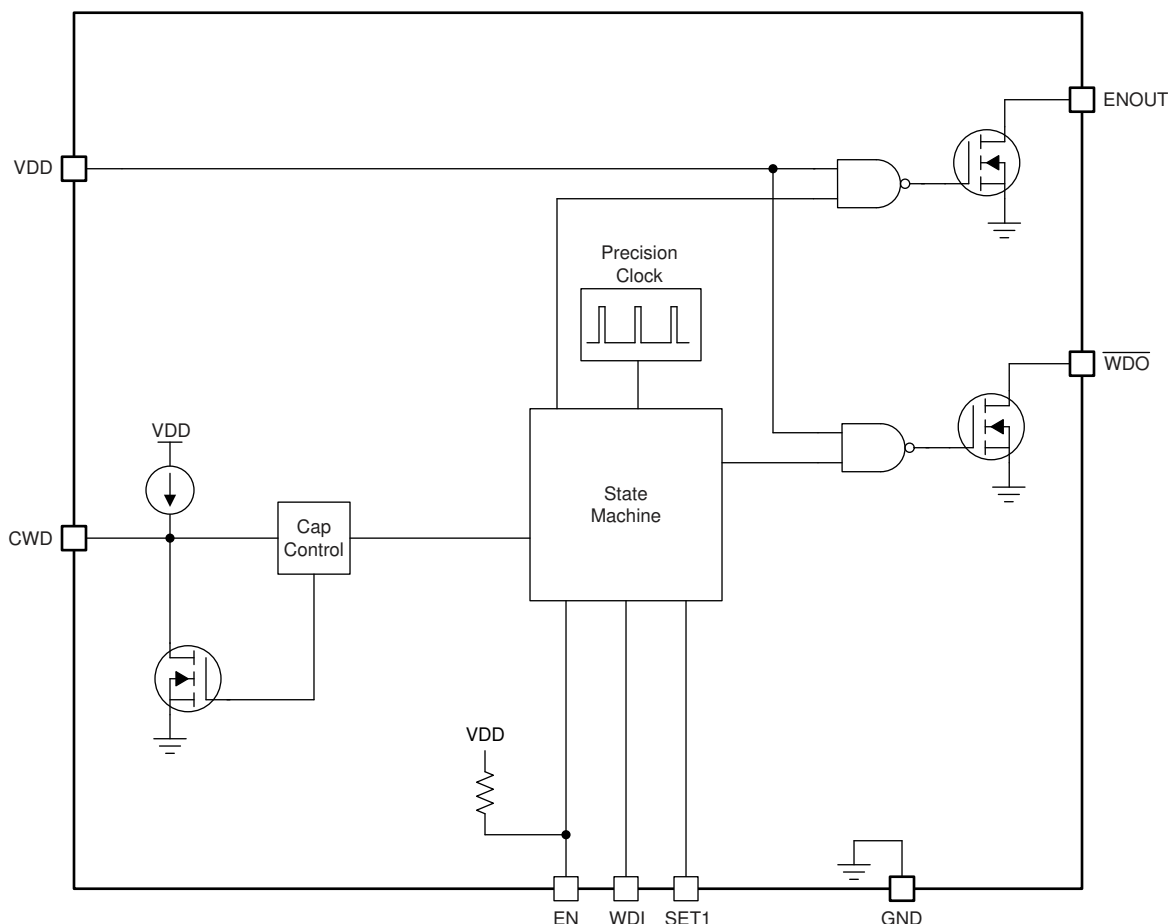
FIG 6-7. Normalized Watchdog Timeout (t_{WD}) Accuracy (SET1 = 1, CWD = 10kΩ)

7 Detailed Description

7.1 Overview

The TPS3431-Q1 is a standard programmable watchdog timer with enable/disable feature. This device includes a precision watchdog timer that achieves 15% timing accuracy over the specified temperature range of -40°C to $+125^{\circ}\text{C}$.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable Input (EN) and Enable Output (ENOUT)

The Enable (EN) input allows a processor or other logic circuits to initiate a single cycle watchdog reset by momentarily bringing Enable low, or a permanent disable by keeping Enable low. After EN goes to a logic high and V_{DD} is above $V_{DD(min)}$, ENOUT and \overline{WDO} go logic high after the watchdog reset delay time (t_{RST}). If EN is not controlled externally, then EN can either be connected to V_{DD} or left floating because the EN pin is internally pulled up to V_{DD} . When EN is forced logic low, ENOUT goes low after a propagation delay of 200 ns and \overline{WDO} goes high impedance and pulls to logic high due to the external pull-up resistor. Because \overline{WDO} and ENOUT are both open-drain outputs, these outputs can be tied together to create an OR logic function so that if either output pulls down to logic low, the other will also pull down logic low.

7.3.2 Watchdog Mode

This section provides information for the watchdog mode of operation.

7.3.2.1 CWD

The CWD pin provides the user the functionality of both high-precision, factory-programmed watchdog timing options and user-programmable watchdog timing. The TPS3431-Q1 features three options for setting the watchdog timer: connecting a capacitor to the CWD pin, connecting a pull-up resistor to VDD, and leaving the CWD pin unconnected. The configuration of the CWD pin is evaluated by the device every time V_{DD} rises above $V_{DD(min)}$. The pin evaluation is controlled by an internal state machine that determines which option is connected to the CWD pin. The sequence of events typically takes $381\ \mu s$ (t_{INIT}) to determine if the CWD pin is left unconnected, pulled-up through a resistor, or connected to a capacitor. If the CWD pin is being pulled up to VDD, a 10-k Ω resistor is required.

7.3.2.2 Watchdog Input WDI

WDI is the watchdog timer input that controls the \overline{WDO} output. The WDI input is triggered by the falling edge of the input signal. To ensure proper functionality of the watchdog timer, always issue the WDI pulse before $t_{WD(min)}$. If the pulse is issued in this region, then \overline{WDO} remains unasserted. Otherwise, the device asserts \overline{WDO} , putting the \overline{WDO} pin into a low-impedance state therefore \overline{WDO} will be logic low.

The watchdog input (WDI) is a digital pin. To ensure there is no increase in I_{DD} , drive the WDI pin to either VDD or GND at all times. Putting the pin to an intermediate voltage can cause an increase in supply current (I_{DD}) because of the architecture of the digital logic gates. When EN is logic low, the watchdog is disabled and all signals input to WDI are ignored. When EN is logic high, the device resumes normal operation and no longer ignores the signal on WDI. If the watchdog is disabled, drive the WDI pin to either VDD or GND. [Figure 7-1](#) shows the valid region for a WDI pulse to be issued to prevent \overline{WDO} from being triggered and pulled low.

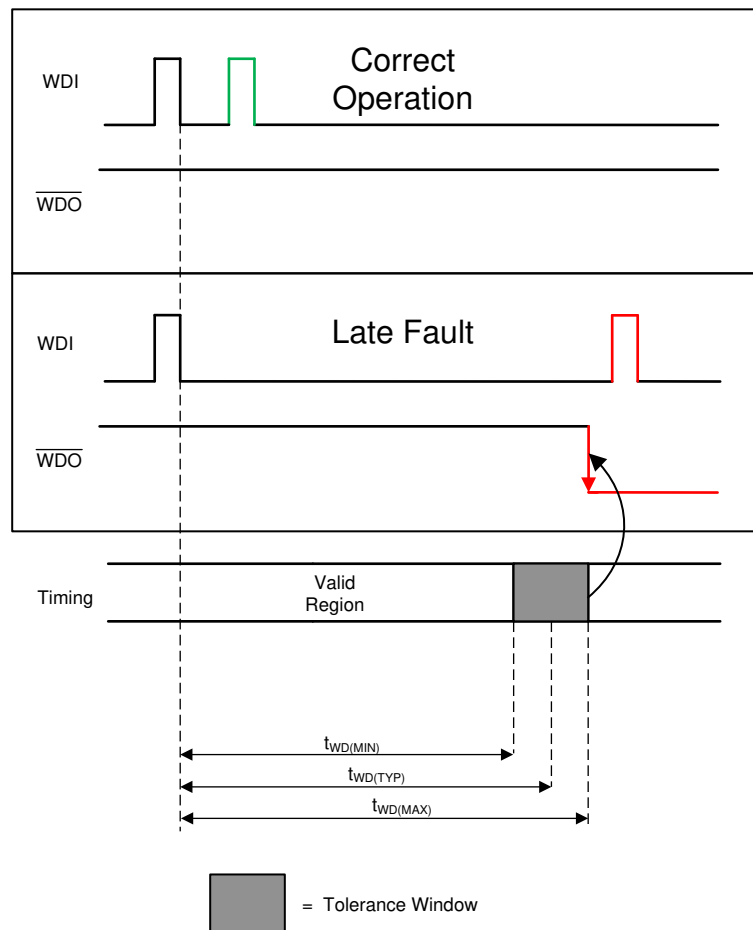


Figure 7-1. Watchdog Timing Diagram

7.3.2.3 Watchdog Output \overline{WDO}

The TPS3431-Q1 features an active-low open-drain watchdog output that asserts when a pulse on WDI fails to arrive within the watchdog timeout. When EN is logic high, the \overline{WDO} signal maintains normal operation. When the EN pin is logic low, the \overline{WDO} pin goes to a high-impedance state and pulls logic high due to the external pull-up resistor. Because \overline{WDO} and ENOUT are both open-drain outputs, these outputs can be tied together to create an OR logic function so that if either output pulls down to logic low, the other will also pull down logic low.

7.3.2.4 SET1

The SET1 pin can enable and disable the watchdog timer and should be used when disabling the watchdog timer for longer than one watchdog reset cycle. If SET1 is set to GND, the watchdog timer is disabled and WDI is ignored. If the watchdog timer is disabled, drive the WDI pin to either GND or VDD to ensure that there is no increase in I_{DD} . When SET1 is logic high, the watchdog operates normally. The SET1 pin can be changed dynamically; however, if the watchdog is going from disabled to enabled there is a 150 μ s setup time where the watchdog does not respond to changes on WDI, as shown in [Figure 7-2](#). Note: disabling using SET1 pin causes a delay defined by the fixed 150- μ s setup time when enabling again.

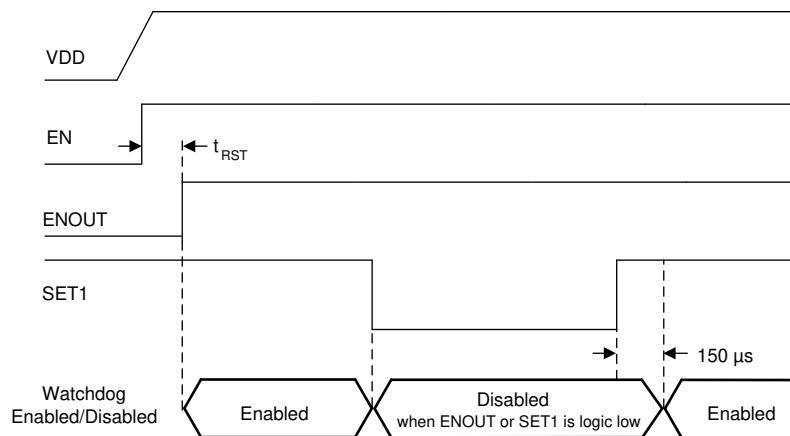


Figure 7-2. Enabling and Disabling the Watchdog

7.4 Device Functional Modes

[Table 7-1](#) summarizes the functional modes of the TPS3431-Q1.

Table 7-1. Device Functional Modes

V_{DD}	EN	ENOUT	WDI	\overline{WDO}
$V_{DD} < V_{POR}$	---	---	---	---
$V_{POR} \leq V_{DD} < V_{DD(min)}$	---	Low	Ignored	High
$V_{DD} > V_{DD(min)}$ ⁽¹⁾	High	High	$t_{PULSE} < t_{WD(min)}$ ⁽²⁾	High
$V_{DD} > V_{DD(min)}$ ⁽¹⁾	High	High	$t_{PULSE} > t_{WD(min)}$ ⁽²⁾	Low
$V_{DD} > V_{DD(min)}$ ⁽¹⁾	Low	Low	Ignored	High

(1) V_{DD} must be above $V_{DD(min)}$ for longer than 300 μ s.

(2) Where t_{pulse} is the time between the falling edges on WDI.

7.4.1 V_{DD} is Below V_{POR} ($V_{DD} < V_{POR}$)

When V_{DD} is less than V_{POR} , \overline{WDO} is undefined and can be either high or low. The state of \overline{WDO} largely depends on the load that the \overline{WDO} pin is experiencing.

7.4.2 Above Power-On-Reset, But Less Than $V_{DD(min)}$ ($V_{POR} \leq V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than $V_{DD(min)}$, and greater than or equal to V_{POR} , the \overline{WDO} signal is asserted (logic low). When EN is logic low, the watchdog output \overline{WDO} is in a high-impedance state and logic low regardless of the WDI signal that is input to the device.

7.4.3 Normal Operation ($V_{DD} \geq V_{DD(min)}$)

When V_{DD} is greater than or equal to $V_{DD(min)}$ and EN is logic high, the \overline{WDO} signal is determined by WDI. When WDI is within the watchdog timeout, the internal MOSFET turns off and \overline{WDO} is pulled high through external pull-up resistor. When WDI is not within the watchdog timeout, the internal MOSFET turns on and \overline{WDO} is pulled to logic low. When EN is logic low, ENOUT goes to logic low and \overline{WDO} goes to a high-impedance state and pulls to logic high due to the external pull-up resistor.

8 Application and Implementation

Note

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8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.1.1 CWD Functionality

The TPS3431-Q1 features three options for setting the watchdog timeout: connecting a capacitor to the CWD pin, connecting a pull-up resistor to VDD, and leaving the CWD pin unconnected. 図 8-1 shows a schematic drawing of all three options. If this pin is connected to VDD through a 10-k Ω pullup resistor or left unconnected (high impedance), then the factory-programmed watchdog timeouts are enabled; see the セクション 8.1.1.1 section. Otherwise, the watchdog timeout can be adjusted by placing a capacitor from the CWD pin to ground.

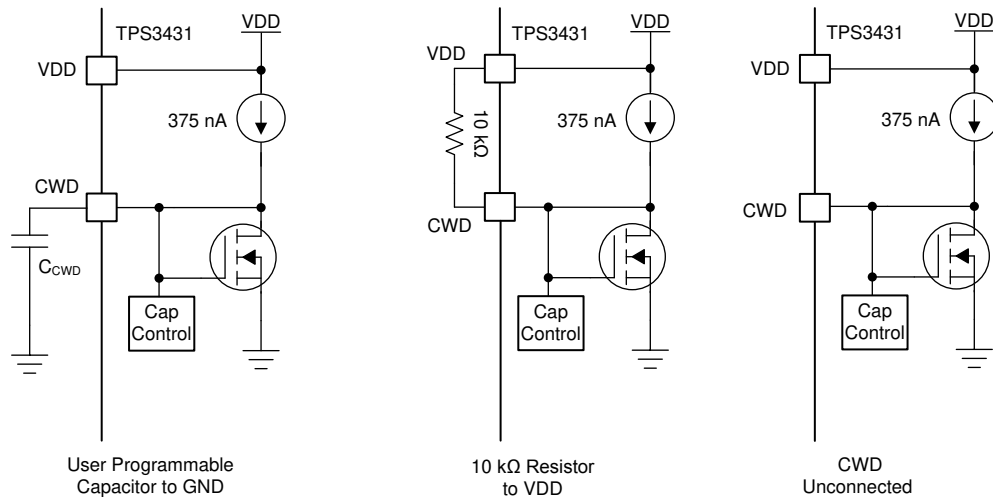


図 8-1. CWD Charging Circuit

8.1.1.1 Factory-Programmed Timing Options

If using the factory-programmed timing options (listed in 表 8-1), the CWD pin must either be unconnected or pulled up to VDD through a 10-k Ω pull-up resistor. Using these options enables high-precision, 15% accurate watchdog timing.

表 8-1. Factory Programmed Watchdog Timing

INPUT		STANDARD WATCHDOG TIMEOUT WDT (t_{WD})			UNIT
CWD	SET1	MIN	TYP	MAX	
NC	0	Watchdog disabled			
NC	1	1360	1600	1840	ms
10 k Ω to VDD	0	Watchdog disabled			
10 k Ω to VDD	1	170	200	230	ms

8.1.1.2 CWD Adjustable Capacitor Watchdog Timeout

Adjustable capacitor timing is achievable by connecting a capacitor to the CWD pin. If a capacitor is connected to CWD, then a 375-nA, constant-current source charges C_{CWD} until $V_{CWD} = 1.21$ V. 表 8-2 shows how to

calculate t_{WD} using 式 1 and the SET1 pin. The TPS3431-Q1 determines the watchdog timeout with the formulas given in 式 1, where C_{CWD} is in nanofarads and t_{WD} is in milliseconds.

$$t_{WD}(\text{ms}) = 77.4 \times C_{CWD}(\text{nF}) + 55 (\text{ms}) \quad (1)$$

The TPS3431-Q1 is designed and tested using C_{CWD} capacitors between 100 pF and 1 μF . Note that 式 1 is for ideal capacitors and capacitor tolerances vary the actual device timing. For the most accurate timing, use ceramic capacitors with COG dielectric material. If a C_{CWD} capacitor is used, 式 1 can be used to set t_{WD} for the watchdog timeout. 表 8-3 shows the minimum and maximum calculated t_{WD} values using an ideal capacitor.

表 8-2. Programmable CWD Timing

INPUT		WATCHDOG TIMEOUT WDT (t_{WD}) ⁽¹⁾			UNIT
CWD	SET1	MIN	TYP	MAX	
C_{CWD}	0	Watchdog disabled			
C_{CWD}	1	$t_{WD} \times 0.905$	t_{WD} 式 1	$t_{WD} \times 1.095$	ms

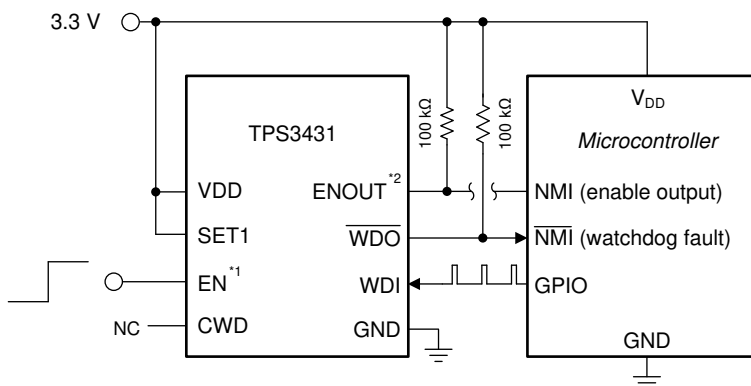
(1) Calculated from 式 1 using an ideal capacitor.

表 8-3. t_{WD} Values for Common Ideal Capacitor Values

C_{CWD}	WATCHDOG TIMEOUT WDT (t_{WD})			UNIT
	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	
100 pF	56.77	62.74	68.7	ms
1 nF	119.82	132.4	144.98	ms
10 nF	750	829	908	ms
100 nF	7054	7795	8536	ms
1 μF	70096	77455	84814	ms

(1) The minimum and maximum values are calculated using an ideal capacitor.

8.2 Typical Application



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- A. EN can also be left floating and is internally pulled-up to VDD
- B. ENOUT can also be left floating or tied to WDO

8-2. Monitoring a Microcontroller with Standard Watchdog Timer

8.2.1 Design 1 Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Output logic voltage	3.3V Open-Drain	3.3V Open-Drain
Watchdog Timeout	Leave CWD disconnected: 1.6 seconds (typical)	$t_{WD(min)} = 1360 \text{ ms}$, $t_{WD(TYP)} = 1600 \text{ ms}$, $t_{WD(max)} = 1840 \text{ ms}$
Maximum device current consumption	35 μA	33 μA when \overline{WDO} is asserted

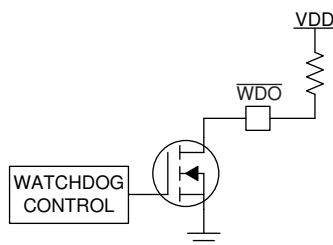
8.2.2 Detailed Design 1 Procedure

8.2.2.1 Calculating \overline{WDO} Pullup Resistor Design 1

The TPS3431-Q1 uses an open-drain configuration for the \overline{WDO} circuit, as shown in 8-3. When the internal MOSFET is off, the external pull-up resistor pulls the drain of the transistor to VDD and when the MOSFET is turned on, the MOSFET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below the maximum value.

To choose the proper pull-up resistor, there are three key specifications to keep in mind: the pull-up voltage (V_{PU}), the recommended maximum \overline{WDO} pin current ($I_{\overline{WDO}}$), and V_{OL} .

The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with $I_{\overline{WDO}}$ kept below 10 mA. For this example, with a V_{PU} of 3.3 V, a resistor must be chosen to keep $I_{\overline{WDO}}$ below 35 μA because this value is the maximum consumption current allowed. To ensure this specification is met, a pull-up resistor value of 100 k Ω was selected, which sinks a maximum of 33 μA when \overline{WDO} is asserted.



8-3. \overline{WDO} Open-Drain Configuration

8.2.2.2 Setting the Watchdog Design 1

As illustrated in [Figure 8-1](#) there are three options for setting the watchdog timer. The design specifications in this application allow for a factory-programmed timing option by leaving CWD floating. To ensure proper functionality, a falling edge must be issued before $t_{WD(min)}$ which is set for 1.36 seconds when CWD is not connected. [Figure 8-8](#) illustrates that a WDI signal with a period of 1 second keeps \overline{WDO} from asserting.

[Figure 8-4](#) shows \overline{WDO} asserting when the WDI signal has a period longer than $t_{WD(max)}$ which is 1.84 seconds when CWD is not connected. [Figure 8-5](#) shows a watchdog fault caused by missing WDI pulse followed by correct timing WDI pulses to deactivate \overline{WDO} .

8.2.3 Application Curves Design 1

Unless otherwise stated, application curves were taken at $T_A = 25^\circ\text{C}$.

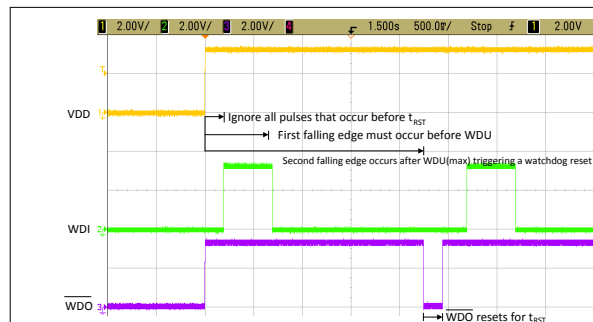


Figure 8-4. \overline{WDO} Fault Caused by WDI Pulse Arriving Too Late (After $t_{WD(max)}$)

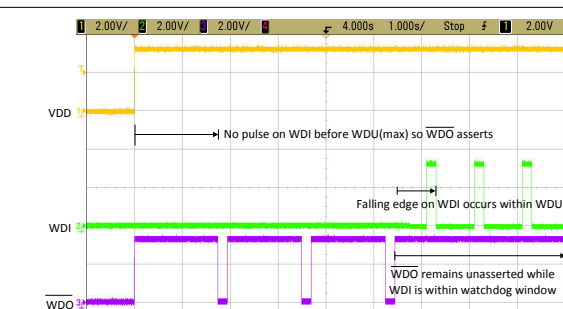
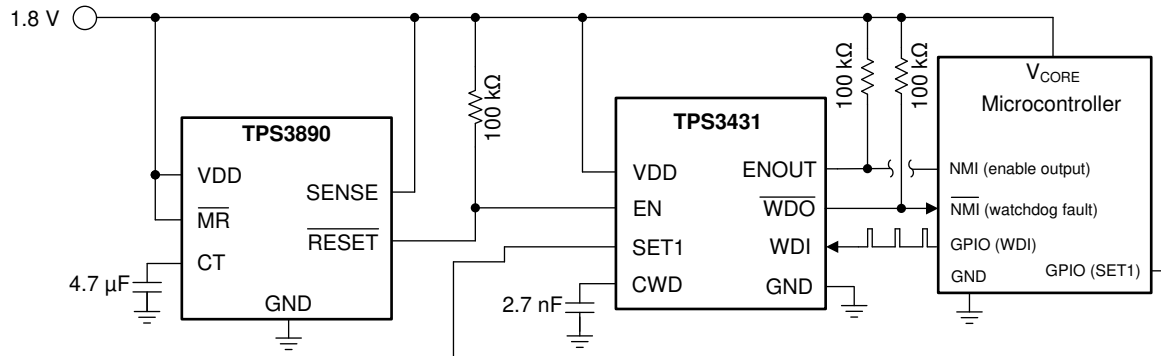


Figure 8-5. \overline{WDO} Fault Caused by missing WDI Pulses Followed by Correct Timing WDI Pulses

8.3 Programmable Application



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✎ 8-6. Monitoring the Supply Voltage and Watchdog Supervision of a Microcontroller

8.3.1 Design 2 Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Watchdog disable for initialization period	Watchdog must remain disabled for 5 seconds until logic enables the watchdog timer	5.02 seconds (typ)
Programmable disable feature	Microcontroller controls SET1 on TPS3431 via a GPIO	The Microcontroller can disable TPS3431 via SET1 and thus disable the watchdog for any reason.
Output logic voltage	1.8-V Open-Drain	1.8V Open-Drain
Monitored rail (TPS3890)	1.8 V with a 5% threshold and 1% accuracy	Worst-case $V_{ITN} = 1.714 \text{ V} - 4.7\%$
Watchdog timeout (TPS3431)	265 ms typical	$t_{WD(min)} = 213 \text{ ms}$, $t_{WD(TYP)} = 264 \text{ ms}$, $t_{WD(max)} = 319 \text{ ms}$
Maximum device current consumption	50 μA	37 μA when $\overline{\text{WDO}}$ is asserted

8.3.2 Detailed Design 2 Procedure

8.3.2.1 Calculating $\overline{\text{WDO}}$ Pullup Resistor Design 2

The TPS3431-Q1 uses an open-drain configuration for the $\overline{\text{WDO}}$ circuit. When the internal MOSFET is off, the external pull-up resistor pulls the drain of the transistor to VDD and when the MOSFET is turned on, the MOSFET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below the maximum value. To choose the proper pull-up resistor, there are three key specifications to keep in mind: the pull-up voltage (V_{PU}), the recommended maximum $\overline{\text{WDO}}$ pin current ($I_{\overline{\text{WDO}}}$), and V_{OL} . The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with $I_{\overline{\text{WDO}}}$ kept below 10 mA. For this example, with a V_{PU} of 1.8 V, a resistor must be chosen to keep $I_{\overline{\text{WDO}}}$ below 50 μA because this value is the maximum consumption current allowed. To ensure this specification is met, a pull-up resistor value of 100 k Ω was selected, which sinks a maximum of 18 μA when $\overline{\text{WDO}}$ is asserted.

8.3.2.2 Setting the Watchdog Design 2

As illustrated in ✎ 8-1 there are three options for setting the watchdog timer. The design specifications in this application require the programmable timing option (external capacitor connected to CWD). When a capacitor is connected to the CWD pin, the watchdog timer is governed by 式 1. This equation estimation is only valid for ideal capacitors and any temperature or voltage derating must be accounted for separately.

$$C_{CWD} \text{ (nF)} = (t_{WD}(\text{ms}) - 55) / 77.4 = (265 - 55) / 77.4 = 2.71 \text{ nF} \quad (2)$$

The nearest standard capacitor value is 2.7 nF. Selecting 2.7 nF for the C_{CWD} capacitor gives the following minimum and maximum timing parameters:

$$t_{WD(MIN)} = 0.905 \times t_{WD(TYP)} = 0.905 \times (77.4 \times 2.7 + 55) = 238.902 \text{ ms} \quad (3)$$

$$t_{WD(MAX)} = 1.095 \times t_{WD(TYP)} = 1.095 \times (77.4 \times 2.7 + 55) = 289.058 \text{ ms} \quad (4)$$

Capacitor tolerance also influences $t_{WD(MIN)}$ and $t_{WD(MAX)}$. Select a ceramic COG dielectric capacitor for high accuracy. For 2.7 nF, COG capacitors are readily available with 5% tolerances. This selection results in a 5% decrease in $t_{WD(MIN)}$ and a 5% increase in $t_{WD(MAX)}$, giving 213.16 ms and 318.75 ms, respectively. To ensure proper functionality, a falling edge must be issued before $t_{WD(min)}$. [Figure 8-8](#) illustrates that a WDI signal with a period of 260 ms keeps \overline{WDO} from asserting.

8.3.2.3 Watchdog Disabled During Initialization Period Design 2

The watchdog is often needed to be disabled during startup to allow for an initialization period. When the initialization period is over, the watchdog timer is turned back on to allow the microcontroller to be monitored by the TPS3431-Q1. To achieve this setup, EN on TPS3431 is controlled by [TPS3890](#) supervisor. In this application, the TPS3890 was chosen to monitor VDD as well, which means that the RESET on the TPS3890 stays low until VDD rises above V_{ITN} . When VDD comes up, the delay time can be adjusted through the CT capacitor on the TPS3890. With this approach, the RESET delay can be adjusted from a minimum of 25 μ s to a maximum of 30 seconds. For this design, a typical delay of 5 seconds is needed before the watchdog timer is enabled. The CT capacitor calculation (see the [TPS3890 data sheet](#)) yields an ideal capacitance of 4.67 μ F, giving a closest standard ceramic capacitor value of 4.7 μ F. When connecting a 4.7 μ F capacitor from CT to GND, the typical delay time is 5 seconds. [Figure 8-7](#) shows that when the watchdog is disabled, the \overline{WDO} output remains high. However when SET1 goes high and there is no WDI signal, \overline{WDO} begins to assert. See the [TPS3890](#) datasheet for detailed information on the TPS3890. The ENOUT pin on the TPS3431 reflects the status of the EN pin and can be connected to the microcontroller for monitoring or can be left floating if not being used. When the TPS3431 is disabled, ENOUT is logic low and \overline{WDO} is logic high so the user can also tie ENOUT to \overline{WDO} to force \overline{WDO} to logic low when TPS3431 is disabled.

8.3.2.4 Programmable Disable Feature Design 2

The watchdog is often needed to be disabled during operation to prevent false watchdog faults. When the watchdog is disabled, all pulses or lack of pulses on WDI are ignored and \overline{WDO} is high impedance as shown in [Figure 8-9](#). When the watchdog is re-enabled, the watchdog timer is turned back on after a watchdog start-up delay of 150 μ s to allow the microcontroller to be monitored by the TPS3431-Q1. To achieve this setup, SET1 on TPS3431 is controlled by a GPIO on the microcontroller and must be logic high to enable the watchdog. To disable the watchdog, the microcontroller sets the GPIO connected to SET1 to logic low. To re-enable the watchdog, the microcontroller sets the GPIO connected to SET1 back to logic high. This configuration is useful when another device or signal is already using the EN pin on TPS3431, and a programmable disable feature with minimal delay upon enable is still required. When the watchdog is disabled using SET1 instead of EN, ENOUT remains unaffected which is useful when needing to disable the watchdog but not causing another device connected to ENOUT to be disabled.

8.3.3 Application Curves Design 2

Unless otherwise stated, application curves were taken at $T_A = 25^\circ\text{C}$.

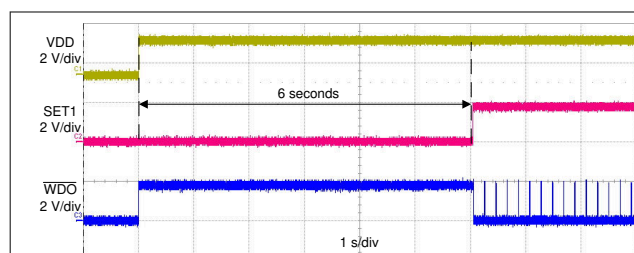


Figure 8-7. Startup Without a WDI Signal

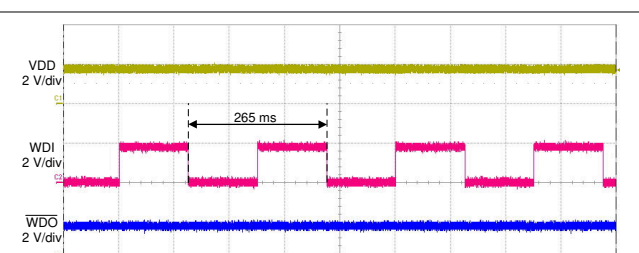


Figure 8-8. Typical WDI Signal

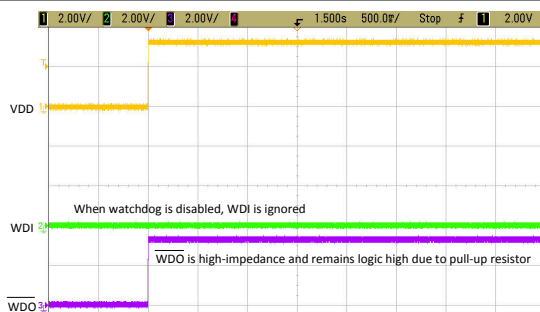


图 8-9. Watchdog Disabled With Missing WDI Pulse

9 Power Supply Recommendations

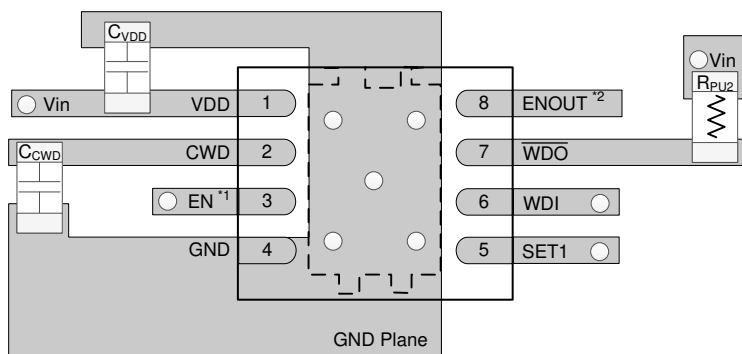
This device is designed to operate from an input supply with a voltage range between 1.8 V and 6.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1- μ F capacitor between the VDD pin and the GND pin.

10 Layout

10.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1- μ F ceramic capacitor as near as possible to the VDD pin.
- If a C_{CWD} capacitor or pull-up resistor is used, place these components as close as possible to the CWD pin. If the CWD pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- Place the pull-up resistor on \overline{WDO} as close to the pin as possible.

10.2 Layout Example



○ Denotes a via

- A. EN can also be left floating and is internally pulled-up to VDD
 B. ENOUT can also be left floating or tied to \overline{WDO}

10-1. TPS3431-Q1 Recommended Layout

11 Device and Documentation Support

11.1 Device Support

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- [TPS3890 Low Quiescent Current, 1% Accurate Supervisor with Programmable Delay](#) (SLVSD65)
- [TPS3431EVM-780 Evaluation Module](#) (SBVU033)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3431SQDRBRQ1	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	431DF
TPS3431SQDRBRQ1.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	431DF

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS3431-Q1 :

- Catalog : [TPS3431](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DRB 8

GENERIC PACKAGE VIEW

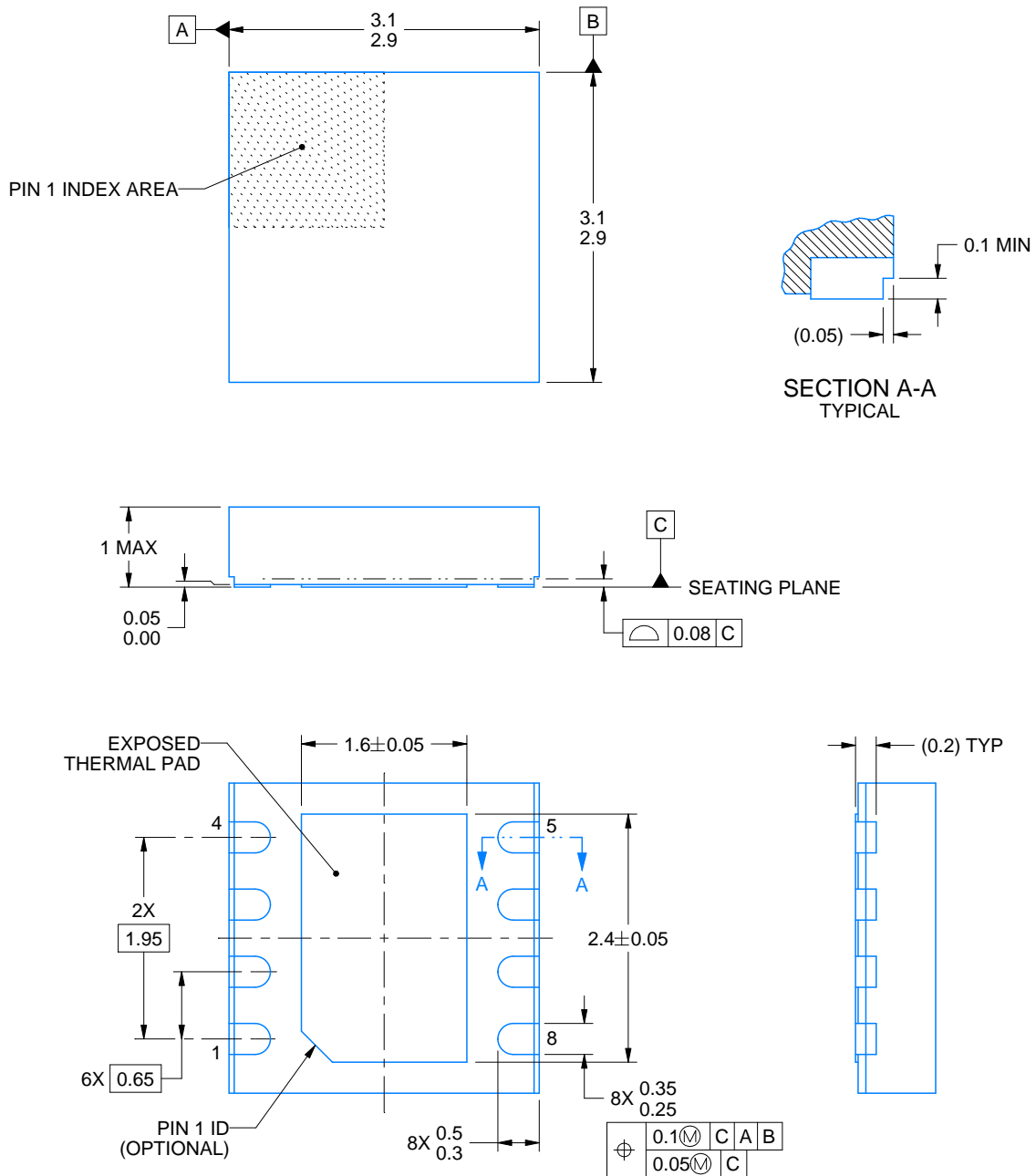
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L



4222121/C 10/2016

NOTES:

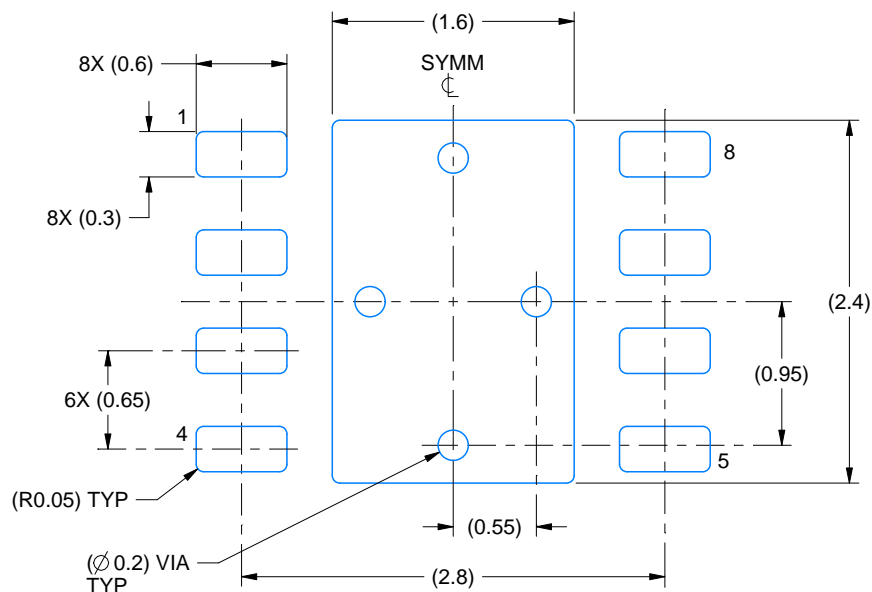
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

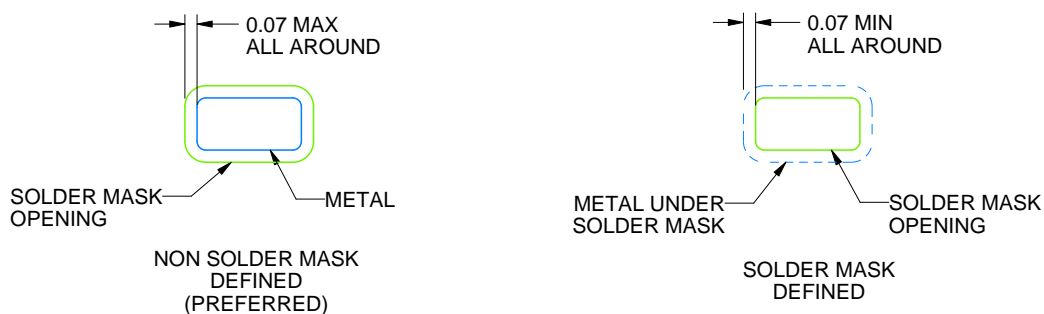
DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222121/C 10/2016

NOTES: (continued)

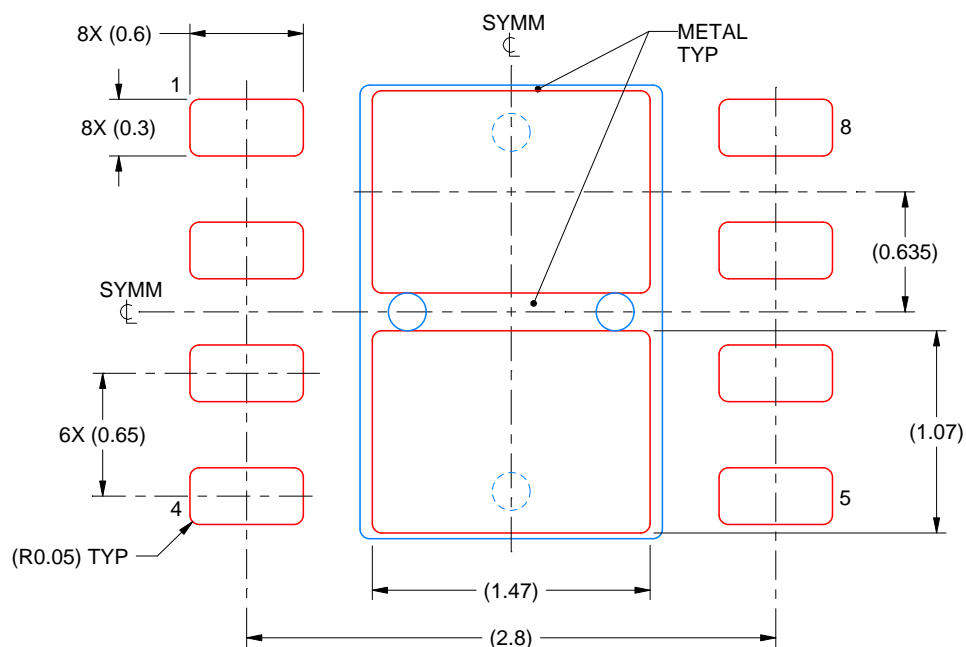
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



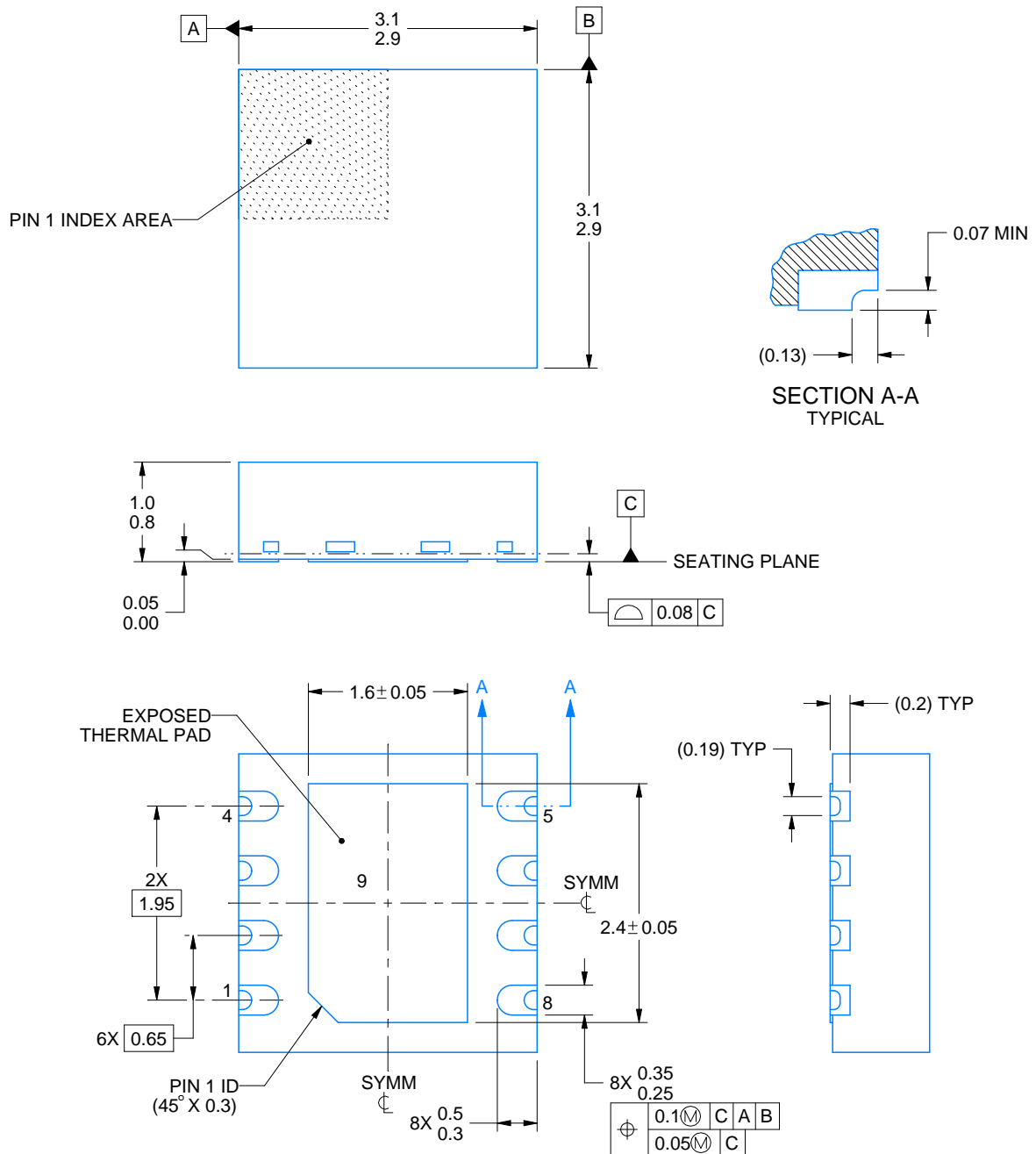
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222121/C 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4227074/D 08/2022

NOTES:

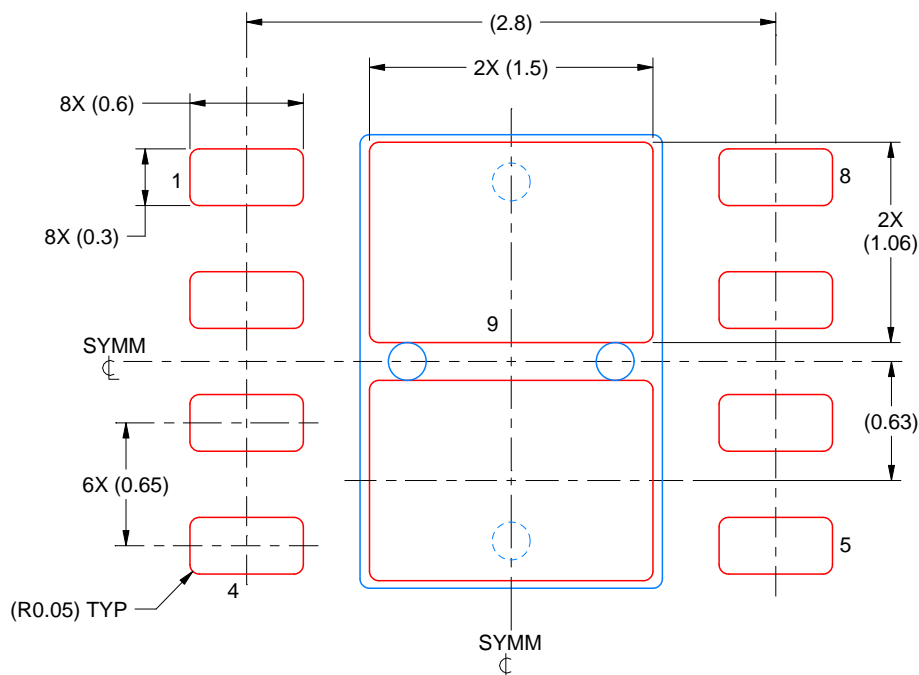
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

DRB0008K

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4227074/D 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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