TPS3430-Q1 車載用、ウィンドウ・ウォッチドッグ・タイマ、プログラム可能なリセット遅延付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - デバイス温度グレード 1：–40℃～+125℃の動作時周囲温度範囲
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 出荷時にプログラム可能な高精度ウォッチドッグ・タイマ
  - ウォッチドッグ・タイムアウトおよびウォッチドッグ・リセット遅延の 25℃での標準値の精度：±2.5%
- ウォッチドッグのディスエーブル機能
- ウォッチドッグのタイムアウトをユーザーがプログラム可能
- ウォッチドッグ・リセット遅延をユーザーがプログラム可能
- 入力電圧範囲：VDD = 1.6V～6.5V
- 低消費電流：I_{DD} = 10µA (標準値)
- オープン・ドレイン出力
- 小型の 3mm × 3mm、10 ピン VSON パッケージ
- 動作時の接合部温度範囲：
  –40℃～+125℃

2 アプリケーション

- 車載テレマティクス制御ユニット
- 運転支援 ECU
- 車載用フロント・カメラ
- 車載ゲートウェイ
- バッテリ管理システム (BMS)
- 車載ディスプレイ・モジュール
- アフターマーケット・テレマティクス

3 概要

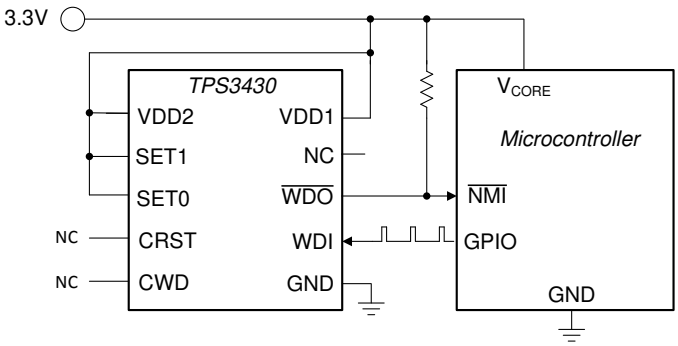
TPS3430-Q1 は、スタンドアロンの車載用ウィンドウ・ウォッチドッグ・タイマであり、車載用アプリケーション向けにウォッチドッグ・ウィンドウとウォッチドッグ・リセット遅延をプログラム可能です。TPS3430-Q1 ウィンドウ・ウォッチドッグは、25℃での標準値で 2.5% のタイミング精度を実現し、ウォッチドッグ出力 ($\overline{WDO}$) のリセット遅延は出荷時プログラムのデフォルト遅延設定により設定するか、外付けのコンデンサによりプログラムできます。開発プロセス中または電源オン時の不要なウォッチドッグ・タイムアウトを回避するため、SET ピンによりウォッチドッグを無効化できます。

TPS3430-Q1 は、3.00mm × 3.00mm の小型 10 ピン VSON パッケージで供給されます。TPS3430-Q1 では、光学検査を容易にするウェッタブル・フランクを採用しています。

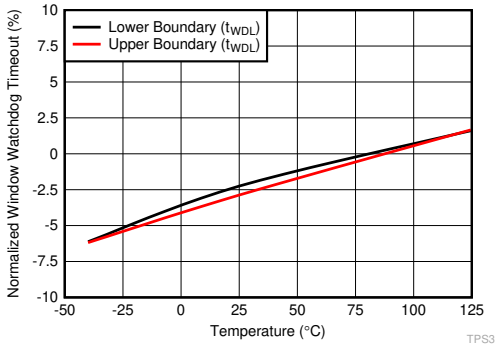
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS3430-Q1	VSON (10)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ウィンドウ・ウォッチドッグ・タイマの回路



温度範囲にわたる正規化されたウォッチドッグ・タイムアウト精度 (SET0 = 1、SET1 = 1、CWD = NC)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (July 2018) to Revision A (September 2021) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「ウォッチドッグ・タイムアウトおよびウォッチドッグ・リセット遅延の温度範囲全体にわたる精度:±15%」を削除 ... 1
- 「機能安全対応」の箇条書き項目を追加 ... 1
- 「アプリケーション」セクションを更新し、Web リンクを追加 ... 1
- 「–40℃～+125℃で 15%、」を削除 ... 1
- 「TPS3430-Q1 では、光学検査を容易にするウェッタブル・フランクを採用しています」を追加 ... 1
- Updated ESD Ratings ... 5
- Updated I_{CWD} min and max spec ... 6
- Updated V_{CWD} min and max spec ... 6
- Added a footnote to for t_{INIT} ... 7
- Changed minimum and maximum specifications of 2nd, 5th, 6th, and 8th rows of t_{WDL} parameter ... 7
- Changed minimum and maximum specifications of 2nd and last rows of t_{WDU} parameter ... 7
- Changed minimum and maximum specifications for NC SETx 01 setting for both upper and lower watchdog boundaries, 10 kΩ to VDD SETx 00 and 01 settings for lower watchdog boundary, and 10 kΩ to VDD SETx 11 setting for both upper and lower watchdog boundaries in *Factory-Programmed Watchdog Timing* table ... 19
- Updated t_{WDU} min and max values for all capacitors ... 19
- Updated t_{WDU} min and max boundry values from 0.85 and 1.15 to 0.905 and 1.095 respectively ... 19
- Updated t_{WDU} min and max values for all capacitors ... 20
- Updated t_{WDU} min and max boundry values from 0.85 and 1.15 to 0.905 and 1.095 respectively ... 20

5 Pin Configuration and Functions

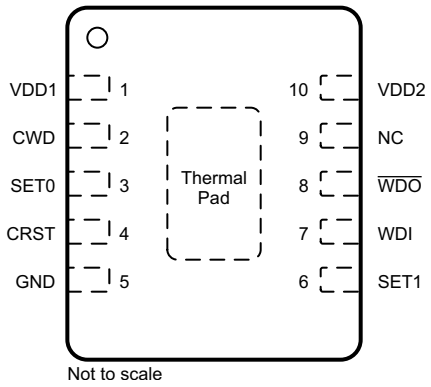

図 5-1. DRC Package 3-mm × 3-mm VSON-10 Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD1	1	I	Supply voltage pin. For noisy systems, connecting a 0.1-µF bypass capacitor is recommended.
CWD	2	I	Programmable watchdog timeout input. Watchdog timeout is set by connecting a capacitor between this pin and ground. Furthermore, this pin can also be connected by a 10-kΩ resistor to VDD, or leaving unconnected (NC) further enables the selection of the preset watchdog timeouts; see the *セクション 6.6* table. When using a capacitor, the TPS3430-Q1 determines the window watchdog upper boundary with 式 4. The lower watchdog boundary is set by the SET pins, see 表 8-7 and the *セクション 8.1.2* section for additional information.
SET0	3	I	Logic input. SET0, SET1, and CWD select the watchdog window ratios, timeouts, and disable the watchdog; see the *セクション 6.6* table.
CRST	4	I	Programmable watchdog reset delay pin. Connect a capacitor between this pin and GND to program the watchdog reset delay period. This pin can also be connected by a 10-kΩ pull-up resistor to VDD, or left unconnected (NC) for various factory programmed watchdog reset delay options; see the *セクション 8.1.1* section. When using an external capacitor, use 式 1 to determine the watchdog reset delay.
GND	5	—	Ground pin
SET1	6	I	Logic input. SET0, SET1, and CWD select the watchdog window ratios, timeouts, and disable the watchdog; see the *セクション 6.6* table.
WDI	7	I	Watchdog input. A falling transition (edge) must occur at this pin within the watchdog timeout between the lower ($t_{WDL(max)}$) and upper ($t_{WDU(min)}$) window boundaries in order for $\overline{WDO}$ to not assert. During power up, all pulses to WDI are ignored before t_{RST} expires and the watchdog is disabled. When the watchdog is not in use, the SET pins can be used to disable the watchdog. The input at WDI is ignored when $\overline{WDO}$ is low (asserted) and also when the watchdog is disabled. If the watchdog is disabled, then WDI cannot be left unconnected and must be driven to either VDD or GND.
$\overline{WDO}$	8	O	Watchdog open-drain active-low output. Connect $\overline{WDO}$ with a 1-kΩ to 100-kΩ resistor to VDD or another power supply. $\overline{WDO}$ goes low (asserts) when a watchdog timeout occurs. When a watchdog timeout occurs, $\overline{WDO}$ goes low (asserts) for the set $\overline{WDO}$ reset delay (t_{RST}). When the watchdog is disabled, $\overline{WDO}$ remains logic high regardless of WDI.
NC	9	NC	This pin is no-connect and should be left floating.
VDD2	10	I	Connect this pin to VDD1. The device will not function properly if VDD1 and VDD2 are not externally connected.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
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GND	5	—	Ground pin
SET1	6	I	Logic input. SET0, SET1, and CWD select the watchdog window ratios, timeouts, and disable the watchdog; see the *セクション 6.6* table.
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NC	9	NC	This pin is no-connect and should be left floating.
VDD2	10	I	Connect this pin to VDD1. The device will not function properly if VDD1 and VDD2 are not externally connected.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VDD1, VDD2	–0.3	7	V
Output voltage range	$\overline{WDO}$	–0.3	7	V
Voltage ranges	SET0, SET1, WDI,	–0.3	7	V
	CWD, CRST	–0.3	VDD + 0.3(3)	
Output pin current	$\overline{WDO}$		±20	mA
Input current (all pins)			±20	mA
Continuous total power dissipation		See セクション 6.4		
Temperature	Operating junction, T_J (2)	–40	150	°C
	Operating free-air temperature, T_A (2)	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $T_J = T_A$ as a result of the low dissipated power in this device.
(3) The absolute maximum rating is V_{DD} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±4000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD1, VDD2	Supply pin voltage	1.6		6.5	V
V_{SET0}	SET0 pin voltage	0		6.5	V
V_{SET1}	SET1 pin voltage	0		6.5	V
C_{CRST}	WD reset delay capacitor	0.1(1)		1000(1)	nF
R_{CRST}	Pull-up resistor to VDD	9	10	11	kΩ
C_{CWD}	Watchdog timing capacitor	0.1(2)		1000(2)	nF
CWD	Pull-up resistor to VDD	9	10	11	kΩ
R_{PU}	Pull-up resistor, $\overline{WDO}$	1	10	100	kΩ
I_{WDO}	Watchdog output current			10	mA
T_J	Junction Temperature	–40		125	°C

(1) Using a C_{CRST} capacitor of 0.1 nF or 1000 nF gives a reset delay of 703 µs or 3.22 seconds, respectively.
(2) Using a C_{CWD} capacitor of 0.1 nF or 1000 nF gives a $t_{WDU(typ)}$ of 62.74 ms or 77.45 seconds, respectively.

6.4 Thermal Information

THERMAL METRIC(1)		TPS3430-Q1 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.3	
ψ_{JT}	Junction-to-top characterization parameter	1.4	
ψ_{JB}	Junction-to-board characterization parameter	22.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at 1.6 V ≤ V_{DD} ≤ 6.5 V over the operating temperature range of –40°C ≤ T_J ≤ +125°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
VDD1,VDD2 (1) (3)	Supply voltage		1.6		6.5	V
I_{DD}	Supply current			10	19	µA
V_{POR} (2)	Power-on reset voltage	$V_{OL(MAX)}$ = 0.25 V			0.8	V
I_{CRST}	CRST pin charge current	CRST = 0.5 V	337	375	413	nA
V_{CRST}	CRST pin threshold voltage		1.192	1.21	1.228	V
WINDOW WATCHDOG FUNCTION						
I_{CWD}	CWD pin charge current	CWD = 0.5 V	347	375	403	nA
V_{CWD}	CWD pin threshold voltage		1.196	1.21	1.224	V
V_{OL}	$\overline{WDO}$ output low	VDD = 5 V, I_{SINK} = 3 mA			0.4	V
I_D	$\overline{WDO}$ output leakage current	VDD = 1.6 V, $V_{\overline{WDO}}$ = 6.5 V			1	µA
V_{IL}	Low-level input voltage (SET0, SET1)				0.25	V
V_{IH}	High-level input voltage (SET0, SET1)		0.8			V
$V_{IL(WDI)}$	$\overline{WDO}$ output low				0.3 × V_{DD}	V
$V_{IH(WDI)}$	$\overline{WDO}$ output leakage current		0.8 × V_{DD}			V

(1) When V_{DD} falls below V_{UVLO}, WDI is ignored
(2) When V_{DD} falls below V_{POR}, $\overline{WDO}$ is undefined.
(3) During power-on, V_{DD} must be a minimum 1.6 V for at least 300 µs.

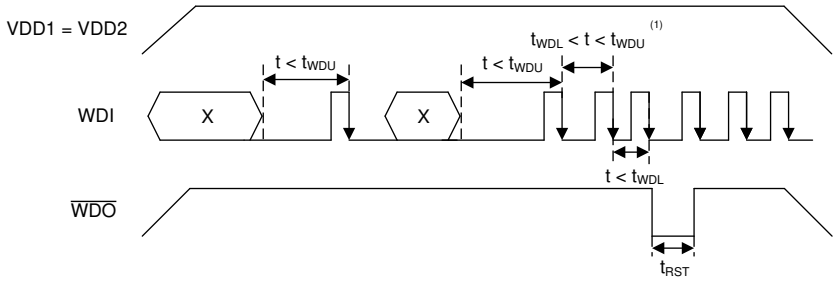
6.6 Timing Requirements

at 1.6 V ≤ V_{DD} ≤ 6.5 V over the operating temperature range of –40°C ≤ T_A, T_J ≤ +125°C (unless otherwise noted); the open-drain pullup resistors are 10 kΩ for each output; typical values are at T_J = 25°C

			MIN	TYP	MAX	UNIT
GENERAL						
t_{INIT}	CWD, CRST pin evaluation period(1)			381		µs
t_{SET}	Time required between changing SET0 and SET1 pins			500		µs
	SET0, SET1 pin setup time			1		µs
	Startup delay (3)			300		µs
DELAY FUNCTION						
t_{RST}	Watchdog reset delay	CRST = NC	170	200	230	ms
		CRST = 10 kΩ to VDD	8.5	10	11.5	ms
WINDOW WATCHDOG FUNCTION						
WD ratio	Window watchdog ratio of lower boundary to upper boundary	CWD = programmable, SET0 = 0, SET1 = 0(2)		1/8		
		CWD = programmable, SET0 = 1, SET1 = 1(2)		1/2		
		CWD = programmable, SET0 = 0, SET1 = 1(2) (4)		3/4		
t_{WDL}	Window watchdog lower boundary	CWD = NC, SET0 = 0, SET1 = 0	19.1	22.5	25.9	ms
		CWD = NC, SET0 = 0, SET1 = 1	1.48	1.85	2.22	ms
		CWD = NC, SET0 = 1, SET1 = 0		Watchdog disabled		
		CWD = NC, SET0 = 1, SET1 = 1	680	800	920	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 0	7.65	9.0	10.35	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 1	7.65	9.0	10.35	ms
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 0		Watchdog disabled		
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 1	1.48	1.85	2.22	ms
t_{WDU}	Window watchdog upper boundary	CWD = NC, SET0 = 0, SET1 = 0	46.8	55.0	63.3	ms
		CWD = NC, SET0 = 0, SET1 = 1	23.375	27.5	31.625	ms
		CWD = NC, SET0 = 1, SET1 = 0		Watchdog disabled		
		CWD = NC, SET0 = 1, SET1 = 1	1360	1600	1840	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 0	92.7	109.0	125.4	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 1	165.8	195.0	224.3	ms
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 0		Watchdog disabled		
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 1	9.35	11.0	12.65	ms
$t_{WD-setup}$	Setup time required for device to respond to changes on WDI after being enabled			150		µs
	Minimum WDI pulse duration			50		ns
t_{WD-del}	WDI to $\overline{WDO}$ delay			50		ns

(1) Refer to セクション 8.1.2.2
(2) 0 refers to VSET ≤ VIL, 1 refers to VSET ≥ VIH.
(3) During power-on, VDD must be a minimum 1.6 V for at least 300 µs
(4) If this watchdog ratio is used, then tWDL(max) can overlap tWDU(min).

6.7 Timing Diagrams



A. See 図 6-2 for WDI timing requirements.

図 6-1. Timing Diagram

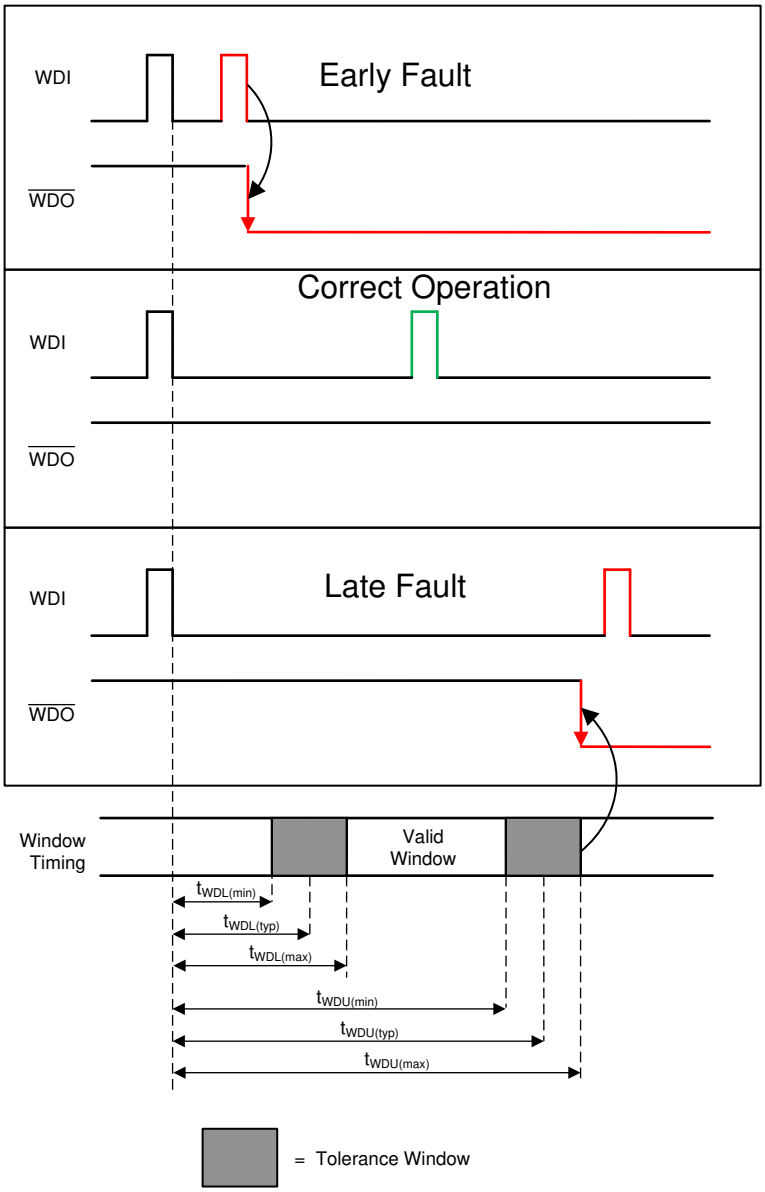


図 6-2. TPS3430-Q1 Window Watchdog Timing

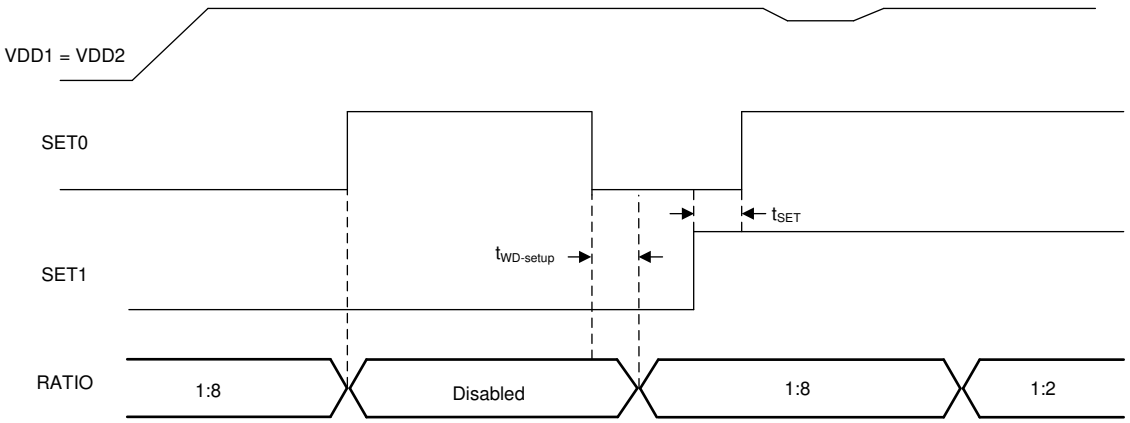


図 6-3. Changing SET0 and SET1 Pins

6.8 Typical Characteristics

all curves are taken at T_A = 25°C with 1.6 V ≤ V_{DD} ≤ 6.5 V (unless otherwise noted)

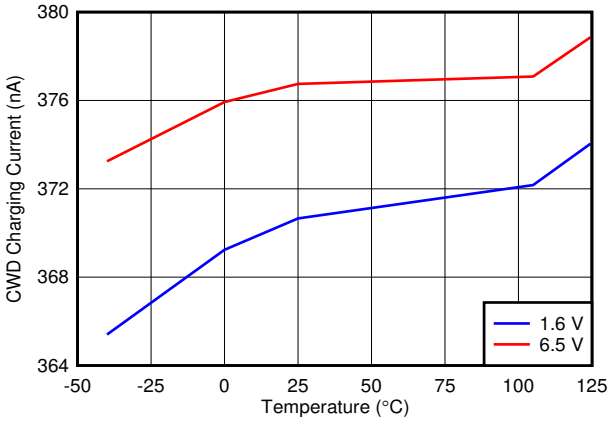


図 6-4. CWD Charging Current vs Temperature

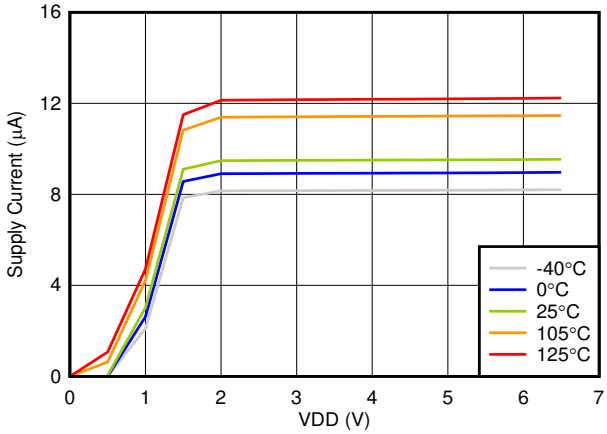


図 6-5. Supply Current vs Power-Supply Voltage

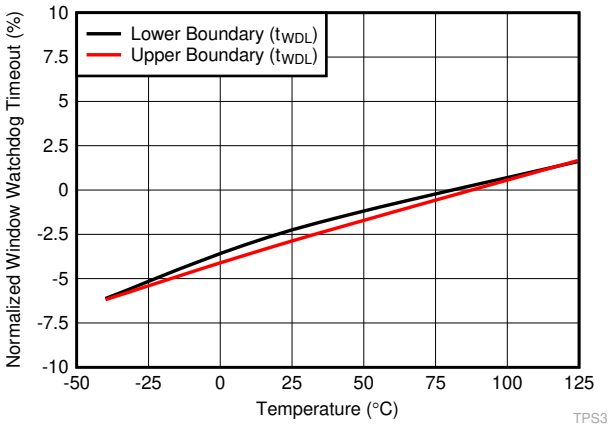


図 6-6. Normalized Watchdog Timeout Accuracy Over Temperature (SET0 = 1, SET1 = 1, CWD = NC)

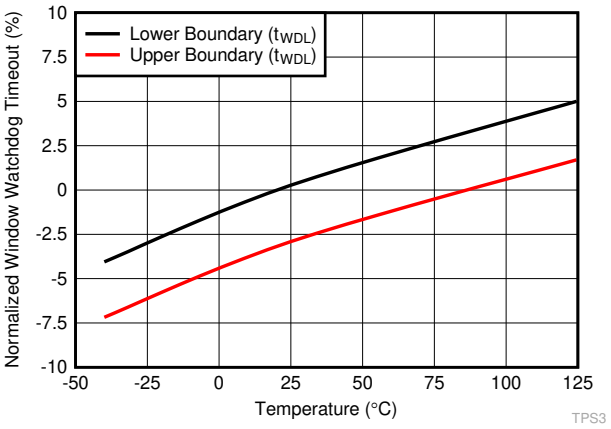


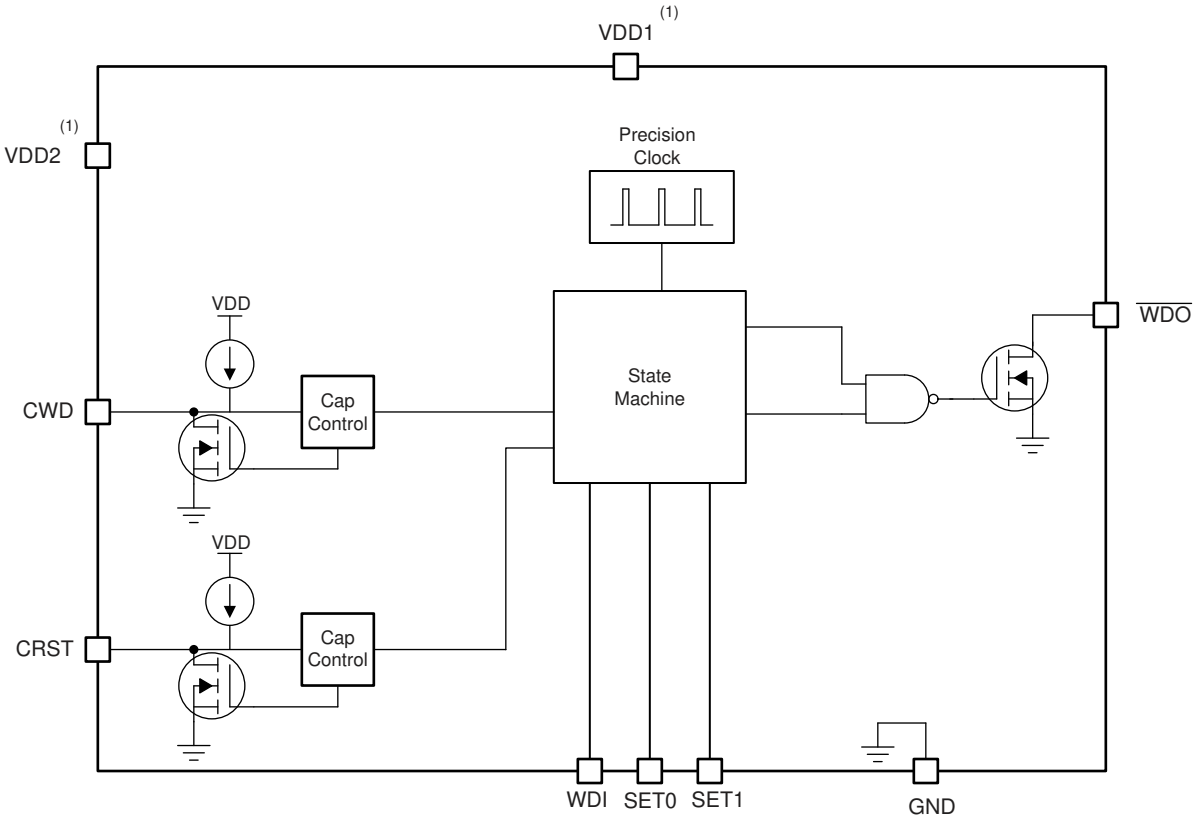
図 6-7. Normalized Watchdog Timeout Accuracy Over Temperature (SET0 = 1, SET1 = 1, CWD = 10kΩ to VDD)

7 Detailed Description

7.1 Overview

The TPS3430-Q1 is a high-accuracy programmable window watchdog timer with watchdog disable feature that achieves 15% watchdog timing accuracy over the specified temperature range of –40°C to +125°C.

7.2 Functional Block Diagrams



A. VDD1 and VDD2 are not internally connected and must be connected externally for the device to function.

図 7-1. TPS3430 Block Diagram

7.3 Feature Description

7.3.1 CRST

The CRST pin provides the user the functionality of both high-precision, factory-programmed watchdog reset delay timing options and user-programmable watchdog reset delay timing. The CRST pin can be pulled up to VDD through a resistor, have an external capacitor to ground, or can be left unconnected. The configuration of the CRST pin is re-evaluated by the device every time the voltage on VDD comes up. The pin evaluation is controlled by an internal state machine that determines which option is connected to the CRST pin. The sequence of events takes 381 µs (t_{INIT}) to determine if the CRST pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CRST pin is being pulled up to VDD, then a 10-kΩ pull-up resistor is required.

7.3.2 Window Watchdog

7.3.2.1 SET0 and SET1

When changing the SET0 or SET1 pins, there are two cases to consider: enabling and disabling the watchdog, and changing the SET0 or SET1 pins when the watchdog is enabled. In case 1 where the watchdog is being enabled or disabled, the changes take effect immediately. However, in case 2, a $\overline{WDO}$ fault event must occur in order for the changes to take place.

7.3.2.1.1 Enabling the Window Watchdog

The TPS3430-Q1 features the ability to enable and disable the watchdog timer. This feature allows the user to start with the watchdog timer disabled and then enable the watchdog timer using the SET0 and SET1 pins. The ability to enable and disable the watchdog is useful to avoid undesired watchdog trips during initialization and shutdown. When the SETx pins are changed to disable the watchdog timer, changes on the pins are responded to immediately (as shown in 図 7-2). When the watchdog goes from disabled to enabled, there is a 150 µs ($t_{WD-setup}$) transition period where the device does not respond to changes on WDI. After this 150-µs period, the device begins to respond to changes on WDI again.

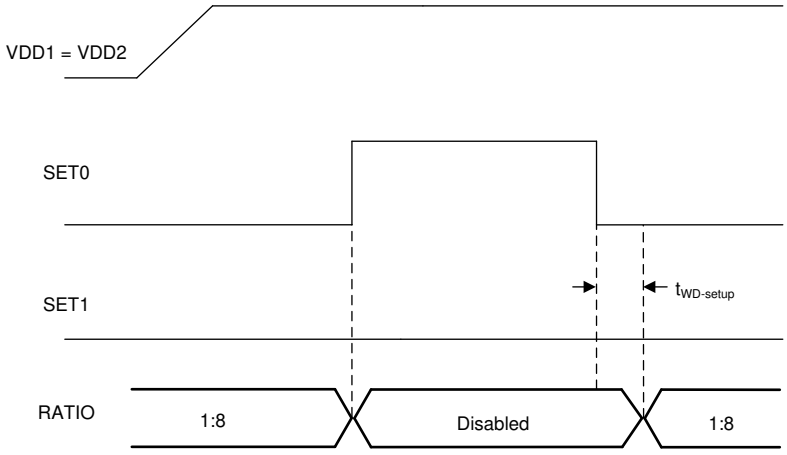
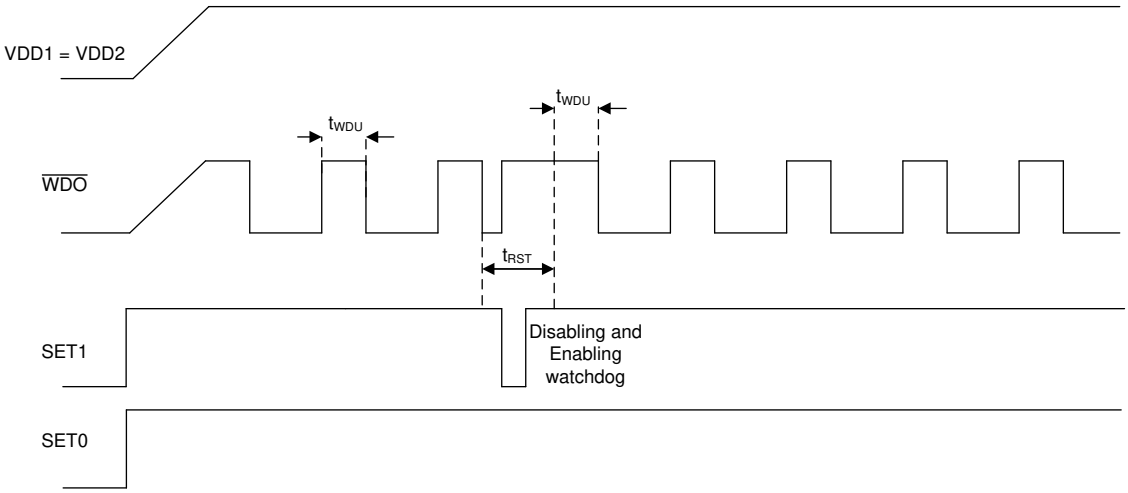


図 7-2. Enabling the Watchdog Timer

7.3.2.1.2 Disabling the Watchdog Timer When Using the CRST Capacitor

When using the TPS3430-Q1 with fixed timing options, if the watchdog is disabled and reenabled while $\overline{WDO}$ is asserted (logic low) the watchdog performs as described in the *セクション 7.3.2.1.1* section. However, if there is a capacitor on the CRST pin, and the watchdog is disabled and reenabled when $\overline{WDO}$ is asserted (logic low), then the watchdog behaves as shown in 図 7-3. When the watchdog is disabled, $\overline{WDO}$ goes high impedance (logic high). However, when the watchdog is enabled again, the t_{RST} period must expire before the watchdog resumes normal operation.



There is no WDI signal in this figure, WDI is always at GND.

図 7-3. Enabling and Disabling the Watchdog Timer During a WDO Reset Event

7.3.2.1.3 SET0 and SET1 During Normal Watchdog Operation

The SET0 and SET1 pins can be used to control the window watchdog ratio of the lower boundary to the upper boundary. There are four possible modes for the watchdog (see 表 8-7): disabled, 1:8 ratio, 3:4 ratio, and 1:2 ratio. If SET0 = 1 and SET1 = 0, then the watchdog is disabled. When the watchdog is disabled $\overline{WDO}$ does not assert, and the TPS3430-Q1 ignores all inputs to WDI. The SET0 and SET1 pins can be changed when the device is operational, but cannot be changed at the same time. If these pins are changed when the device is operational, then there must be a 500-µs (t_{SET}) delay between switching the two pins. If the SET0 and SET1 are used to change the reset timing, then a reset event must occur before the new timing condition is latched. This reset can be triggered by bringing VDD below V_{UVLO}. 図 7-4 shows how the SET0 and SET1 pins do not change the watchdog timing option until a reset event has occurred.

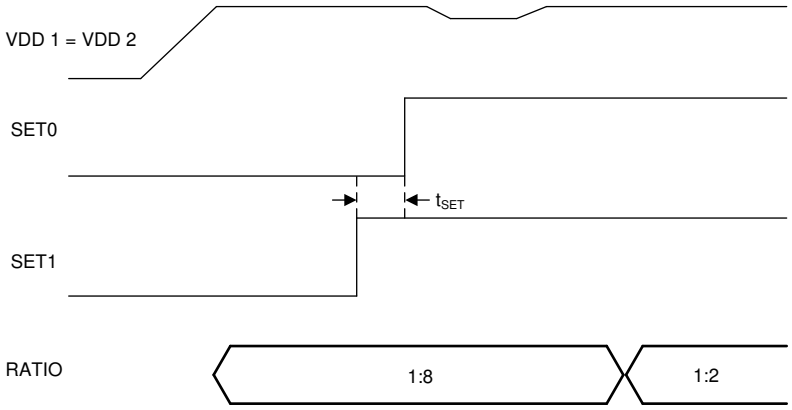


図 7-4. Changing SET0 and SET1 Pins

7.3.3 Window Watchdog Timer

This section provides information for the window watchdog modes of operation. A window watchdog is typically employed in safety critical applications where a traditional watchdog timer is inadequate. In a traditional watchdog, there is a maximum time in which a pulse must be issued to prevent the reset from occurring. However, in a window watchdog the pulse must be issued between a maximum lower window time ($t_{WDL(max)}$) and the minimum upper window time ($t_{WDU(min)}$) set by the CWD pin and the SET0 and SET1 pins. 表 8-7 describes how t_{WDU} can be used to calculate the timing of t_{WDL}. The t_{WDL} timing can also be changed by adjusting the SET0 and SET1 pins. 図 7-5 shows the valid region for a WDI pulse to be issued to prevent the $\overline{WDO}$ from being triggered and being pulled low.

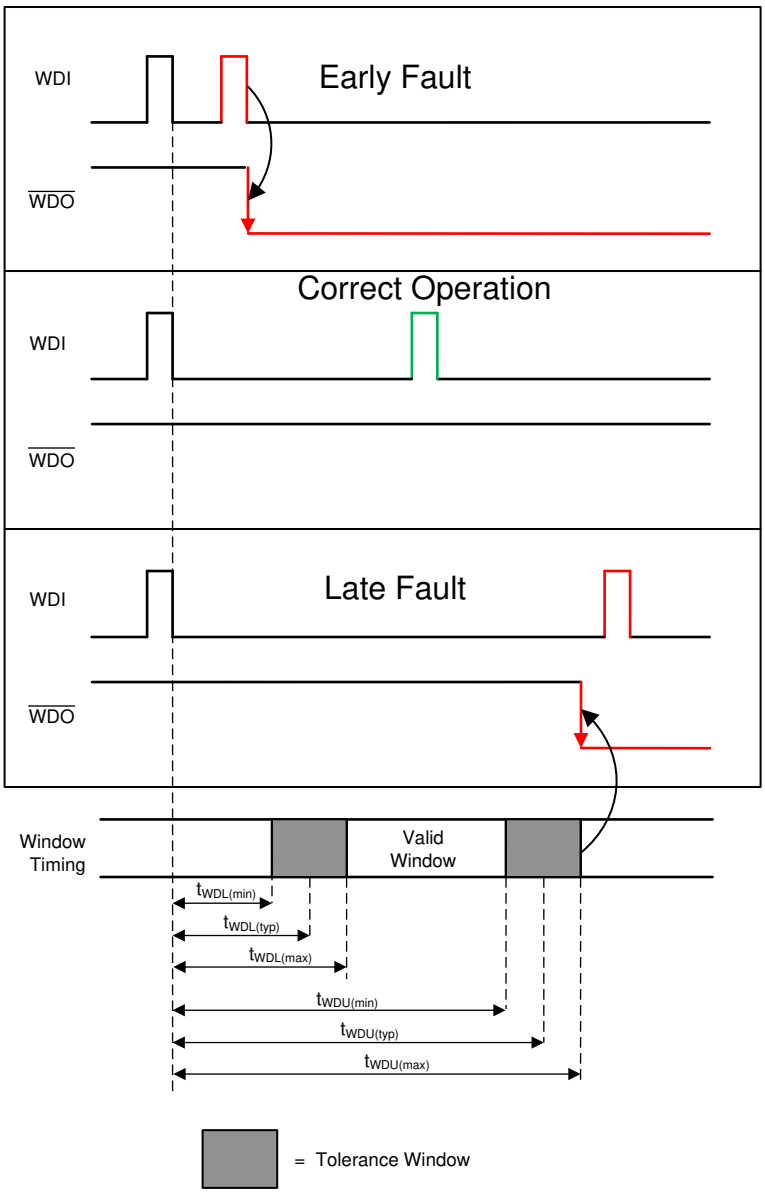


図 7-5. TPS3430-Q1 Window Watchdog Timing

7.3.3.1 CWD

The CWD pin provides the user the functionality of both high-precision, factory-programmed watchdog timeout options and user-programmable watchdog timeout. The TPS3430-Q1 features three options for setting the watchdog window: connecting a capacitor to the CWD pin, connecting CWD to a pull-up resistor to VDD, and leaving the CWD pin unconnected. The configuration of the CWD pin is evaluated by the device every time the voltage on VDD rises above $V_{DD\ (min)}$. The pin evaluation is controlled by an internal state machine that determines which option is connected to the CWD pin. The sequence of events takes 381 µs (t_{INIT}) to determine if the CWD pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CWD pin is being pulled up to VDD using a pull-up resistor, then a 10-kΩ resistor is required.

7.3.3.2 WDI Functionality

WDI is the watchdog timer input that controls the $\overline{WDO}$ output. The WDI input is triggered by the falling edge of the input signal. For the first pulse, the watchdog acts as a traditional watchdog timer; thus, the first pulse must be issued before $t_{WDU(min)}$. After the first pulse, to ensure proper functionality of the watchdog timer, always issue the WDI pulse within the window of $t_{WDL(max)}$ and $t_{WDU(min)}$. If the pulse is issued in this region, then $\overline{WDO}$ remains unasserted. Otherwise, the device asserts $\overline{WDO}$, putting the $\overline{WDO}$ pin into a low-impedance state.

The watchdog input (WDI) is a digital pin. To ensure there is no increase in I_{DD}, drive the WDI pin to either VDD or GND at all times. Putting the pin to an intermediate voltage can cause an increase in supply current (I_{DD}) because of the architecture of the digital logic gates. When $\overline{WDO}$ is asserted, the watchdog is disabled and all signals input to WDI are ignored until the $\overline{WDO}$ reset delay expires. When $\overline{WDO}$ is no longer asserted, the device resumes normal operation and no longer ignores the signal on WDI. If the watchdog is disabled, drive the WDI pin to either VDD or GND.

7.3.3.3 $\overline{WDO}$ Functionality

The TPS3430-Q1 features a programmable window watchdog timer with an programmable watchdog output ($\overline{WDO}$). The watchdog output can flag a fault whenever the watchdog input is outside of the watchdog window. When $\overline{WDO}$ is not asserted (high), the $\overline{WDO}$ signal maintains normal operation. When asserted, $\overline{WDO}$ remains down for t_{RST} and WDI is ignored during the watchdog reset delay. When the watchdog is disabled, $\overline{WDO}$ remains high regardless of WDI.

7.4 Device Functional Modes

表 7-1 summarizes the functional modes of the TPS3430-Q1.

表 7-1. Device Functional Modes

VDD	WDI	$\overline{WDO}$
$V_{DD} < V_{POR}$	—	—
$V_{POR} < V_{DD} < V_{DD\ (min)}$	Ignored	High
$V_{DD} \geq V_{DD\ (min)}$	$t_{WDL(max)} \leq t_{pulse}$ (1) $\leq t_{WDU(min)}$	High
	$t_{WDL(max)} > t_{pulse}$ (1)	Low
	$t_{WDU(min)} < t_{pulse}$ (1)	Low

(1) Where t_{pulse} is the time between falling edges on WDI.

7.4.1 V_{DD} is Below V_{POR} ($V_{DD} < V_{POR}$)

When V_{DD} is less than V_{POR}, $\overline{WDO}$ is undefined and can be either high or low. The state of $\overline{WDO}$ largely depends on the load that the $\overline{WDO}$ pin is experiencing.

7.4.2 V_{DD} is Above V_{POR} And Below $V_{DD\ (min)}$($V_{POR} < V_{DD} < V_{DD\ (min)}$)

When V_{DD} is above V_{POR} and below $V_{DD\ (min)}$, the watchdog is disabled, $\overline{WDO}$ is logic high and WDI is ignored.

7.4.3 Normal Operation ($V_{DD} \geq V_{DD\ (min)}$)

When V_{DD} is greater than or equal to $V_{DD\ (min)}$, the $\overline{WDO}$ signal is determined by WDI if the watchdog is enabled. During power up, the watchdog is disabled until t_{RST} expires. While the watchdog is enabled, the first falling edge on WDI must occur before $t_{WDU(max)}$ to prevent $\overline{WDO}$ from asserting. If the first falling edge on WDI occurs after $t_{WDU(max)}$, $\overline{WDO}$ is asserted (active and low) for t_{RST}. If any falling edge after the first falling edge occurs on WDI before $t_{WDU(min)}$ or after $t_{WDU(max)}$, $\overline{WDO}$ is asserted (active and low) for t_{RST}.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.1.1 CRST Delay

The TPS3430-Q1 features three options for setting the reset delay (t_{RST}): connecting a capacitor to the CRST pin, connecting a pull-up resistor to VDD, and leaving the CRST pin unconnected. 図 8-1 shows a schematic drawing of all three options. To determine which option is connected to the CRST pin, an internal state machine controls the internal pulldown device and measures the pin voltage. This sequence of events takes 381 µs (t_{INIT}) to determine which timing option is used. Every time $\overline{WDO}$ is asserted, the state machine determines what is connected to the pin.

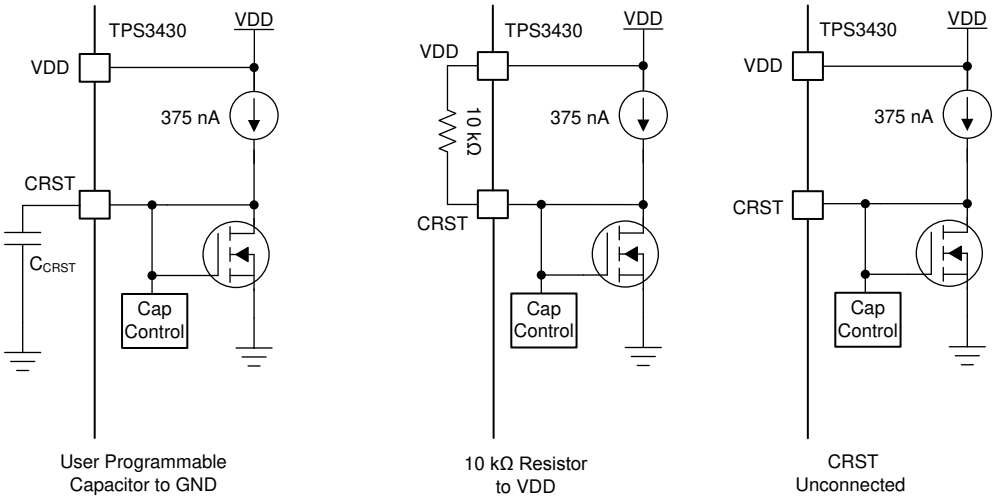


図 8-1. CRST Charging Circuit

8.1.1.1 Factory-Programmed Watchdog Reset Delay Timing

To use the factory-programmed timing options, the CRST pin must either be left unconnected or pulled up to VDD through a 10-kΩ pull-up resistor. Using these options enables a high-precision, 15% accurate reset delay timing, as shown in 表 8-1.

表 8-1. Watchdog Reset Delay Time for Factory-Programmed Timing

CRST	$\overline{WDO}$ DELAY TIME (t_{RST})			UNIT
	MIN	TYP	MAX	
NC	170	200	230	ms
10 kΩ to VDD	8.5	10	11.5	ms

8.1.1.2 CRST Programmable Watchdog Reset Delay

The TPS3430-Q1 uses a CRST pin charging current (I_{CRST}) of 375 nA. When using an external capacitor, the rising $\overline{WDO}$ delay time can be set to any value between 700 µs (C_{CRST} = 100 pF) and 3.2 seconds (C_{CRST} = 1

µF). The typical ideal capacitor value needed for a given delay time can be calculated using 式 1, where C_{CRST} is in microfarads and t_{RST} is in seconds:

$$t_{RST} = 3.22 \times C_{CRST} + 0.000381 \quad (1)$$

To calculate the minimum and maximum watchdog reset delay time use 式 2 and 式 3, respectively.

$$t_{RST(min)} = 2.8862 \times C_{CRST} + 0.000324 \quad (2)$$

$$t_{RST(max)} = 3.64392 \times C_{CRST} + 0.000438 \quad (3)$$

The slope of 式 1 is determined by the time the CRST charging current (I_{CRST}) takes to charge the external capacitor up to the CRST comparator threshold voltage (V_{CRST}). When $\overline{WDO}$ is asserted, the capacitor is discharged through the internal CRST pulldown resistor. When the $\overline{WDO}$ conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor; when V_{CRST} = 1.21 V, $\overline{WDO}$ is unasserted. Note to minimize the difference between the calculated $\overline{WDO}$ delay time and the actual $\overline{WDO}$ delay time, use a use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. 表 8-2 lists the watchdog reset delay time ideal capacitor values for C_{CRST}.

表 8-2. Watchdog Reset Delay Time for Common Ideal Capacitor Values

C_{CRST}	$\overline{WDO}$ DELAY TIME (t_{RST})			UNIT
	MIN(1)	TYP	MAX(1)	
100 pF	0.61	0.70	0.80	ms
1 nF	3.21	3.61	4.08	ms
10 nF	29.2	32.6	36.8	ms
100 nF	289	323	364	ms
1 µF	2886	3227	3644	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

8.1.2 CWD Functionality

The TPS3430-Q1 features three options for setting the watchdog window: connecting a capacitor to the CWD pin, connecting a pull-up resistor to VDD, and leaving the CWD pin unconnected. 図 8-2 shows a schematic drawing of all three options. If this pin is connected to VDD through a 10-kΩ pull-up resistor or left unconnected (high impedance), then the factory-programmed watchdog timeouts are enabled; see the *セクション 6.6* table. Otherwise, the watchdog timeout can be adjusted by placing a capacitor from the CWD pin to ground.

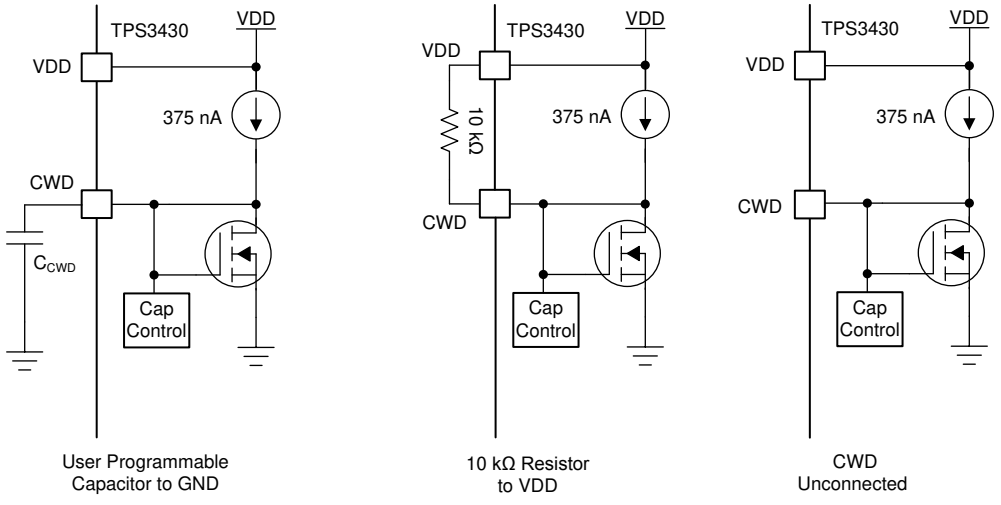


図 8-2. CWD Charging Circuit

8.1.2.1 Factory-Programmed Timing Options

If using the factory-programmed timing options (listed in 表 8-3), the CWD pin must either be unconnected or pulled up to VDD through a 10-kΩ pull-up resistor. Using these options enables high-precision, factory-programmed watchdog timing.

表 8-3. Factory-Programmed Watchdog Timing

INPUT			WATCHDOG LOWER BOUNDARY (t_{WDL})			WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
CWD	SET0	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
NC	0	0	19.1	22.5	25.9	46.8	55.0	63.3	ms
	0	1	1.48	1.85	2.22	23.375	27.5	31.625	ms
	1	0	Watchdog disabled			Watchdog disabled			
	1	1	680	800	920	1360	1600	1840	ms
10 kΩ to VDD	0	0	7.65	9.0	10.35	92.7	109.0	125.4	ms
	0	1	7.65	9.0	10.35	165.8	195.0	224.3	ms
	1	0	Watchdog disabled			Watchdog disabled			
	1	1	1.48	1.85	2.22	9.35	11.0	12.65	ms

8.1.2.2 CWD Adjustable Capacitor Watchdog Timeout

Adjustable capacitor timing is achievable by connecting a capacitor to the CWD pin. If a capacitor is connected to CWD, then a 375-nA constant-current source charges C_{CWD} until V_{CWD} = 1.21 V. The TPS3430-Q1 determines the window watchdog upper boundary with the formula given in 式 4, where C_{CWD} is in microfarads and t_{WDU} is in seconds.

$$t_{WDU(typ)} = 77.4 \times C_{CWD} + 0.055 \quad (4)$$

The TPS3430-Q1 is designed and tested using C_{CWD} capacitors between 100 pF and 1 µF. Note that 式 4 is for ideal capacitors, capacitor tolerances cause the actual device timing to vary. For the most accurate timing, use ceramic capacitors with COG dielectric material. As shown in 表 8-6, when using the minimum capacitor of 100 pF, the watchdog upper boundary is 62.74 ms; whereas with a 1-µF capacitor, the watchdog upper boundary is 77.455 seconds. If a C_{CWD} capacitor is used, 式 4 can be used to set t_{WDU} the window watchdog upper boundary. The window watchdog lower boundary is dependent on the SET0 and SET1 pins because these pins set the window watchdog ratio of the lower boundary to upper boundary; 表 8-7 shows how t_{WDU} can be used to calculate t_{WDL} based on the SET0 and SET1 pins.

表 8-4. t_{WDU} Values for Common Ideal Capacitor Values

C_{CWD}	WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
	MIN(1)	TYP	MAX(1)	
100 pF	56.77	62.74	68.7	ms
1 nF	119.82	132.4	144.98	ms
10 nF	750	829	908	ms
100 nF	7054	7795	8536	ms
1 µF	70096	77455	84814	ms

表 8-5. Programmable CWD Timing

INPUT			WATCHDOG LOWER BOUNDARY (t_{WDL})			WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
CWD	SET0	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
C_{CWD}	0	0	$t_{WDU(min)}$ x 0.125	t_{WDU} x 0.125	$t_{WDU(max)}$ x 0.125	0.905 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.095 x $t_{WDU(typ)}$	s
	0	1	$t_{WDU(min)}$ x 0.75	t_{WDU} x 0.75	$t_{WDU(max)}$ x 0.75	0.905 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.095 x $t_{WDU(typ)}$	s
	1	0	Watchdog disabled			Watchdog disabled			
	1	1	$t_{WDU(min)}$ x 0.5	t_{WDU} x 0.5	$t_{WDU(max)}$ x 0.5	0.905 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.095 x $t_{WDU(typ)}$	s

8.1.2.3

表 8-6. t_{WDU} Values for Common Ideal Capacitor Values

C_{CWD}	WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
	MIN(1)	TYP	MAX(1)	
100 pF	56.77	62.74	68.7	ms
1 nF	119.82	132.4	144.98	ms
10 nF	750	829	908	ms
100 nF	7054	7795	8536	ms
1 µF	70096	77455	84814	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

表 8-7. Programmable CWD Timing

INPUT			WATCHDOG LOWER BOUNDARY (t_{WDL})			WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
CWD	SET0	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
C_{CWD}	0	0	$t_{WDU(min)}$ x 0.125	t_{WDU} x 0.125	$t_{WDU(max)}$ x 0.125	0.905 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.095 x $t_{WDU(typ)}$	s
	0	1	$t_{WDU(min)}$ x 0.75	t_{WDU} x 0.75	$t_{WDU(max)}$ x 0.75	0.905 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.095 x $t_{WDU(typ)}$	s
	1	0	Watchdog disabled			Watchdog disabled			
	1	1	$t_{WDU(min)}$ x 0.5	t_{WDU} x 0.5	$t_{WDU(max)}$ x 0.5	0.905 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.095 x $t_{WDU(typ)}$	s

(1) Calculated from 式 4 using ideal capacitors.

8.2 Typical Applications

8.2.1 Monitoring Microcontroller with Watchdog Timer - Design 1

A basic application for the TPS3430-Q1 is shown in 図 8-8. The TPS3430-Q1 is used to monitor the activity of the microcontroller via the WDI pin. Design 1 utilizes the simplest TPS3430-Q1 configuration with factory-programmed timing options by leaving the CRST and CWD timing pins floating (NC - no connect)

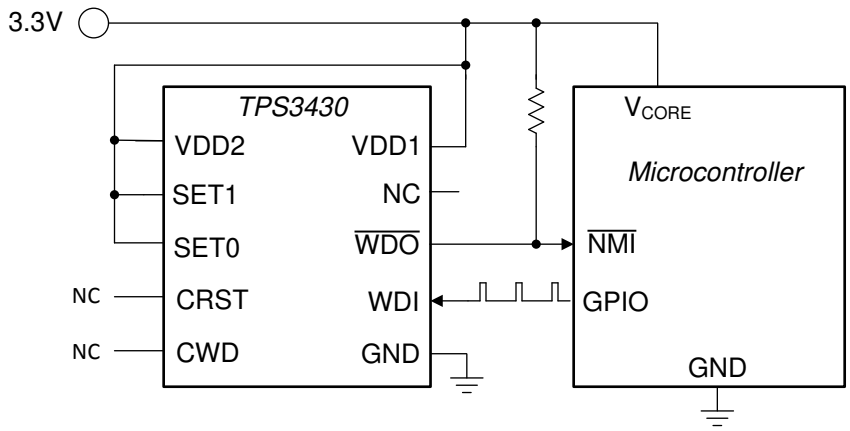


図 8-3. Monitoring Microcontroller using a Window Watchdog Timer

8.2.1.1 Design Requirements - Design 1

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Watchdog Reset delay	Reset delay of 200 ms	Use factory-programmed timing option by leaving CRST as NC. Watchdog reset delay: 170 ms (min), 200 ms (typ), 230 ms (max)
Watchdog window	Functions with a 1-Hz pulse-width modulation (PWM) signal with a 20% duty cycle	Leaving the CWD pin unconnected with SET0 = 1 and SET1 = 1 produces a window with a $t_{WDL(max)}$ of 920 ms and a $t_{WDU(min)}$ of 1360 ms
Output logic voltage	3.3-V Open-Drain	3.3-V Open-Drain
Maximum device current consumption	200 µA	10 µA of current consumption, typical worst-case of 199 µA when $\overline{WDO}$ is asserted

8.2.1.2 Detailed Design Procedure - Design 1

8.2.1.2.1 Meeting the Minimum Watchdog Reset Delay - Design 1

To achieve the 200 ms Watchdog Reset Delay requirement, this design simply leaves CRST pin floating (NC - No Connect) to set the Watchdog Reset Delay (t_{RST}) to the factory-programmed delay of 200 ms. Refer to section 8.1.1 CRST Delay to learn more about the factory-programmed timing options and how to program the Watchdog Reset Delay using an external capacitor.

In 図 8-4 below, the Watchdog Reset Delay of 200 ms is shown by causing a watchdog timing fault. No watchdog pulse comes on WDI within the Watchdog Timeout so $\overline{WDO}$ activates for t_{RST} of 200 ms. Then after three watchdog faults, a watchdog pulse at 1Hz and 20% duty cycle arrives on WDI causing $\overline{WDO}$ to deactive and remain high.

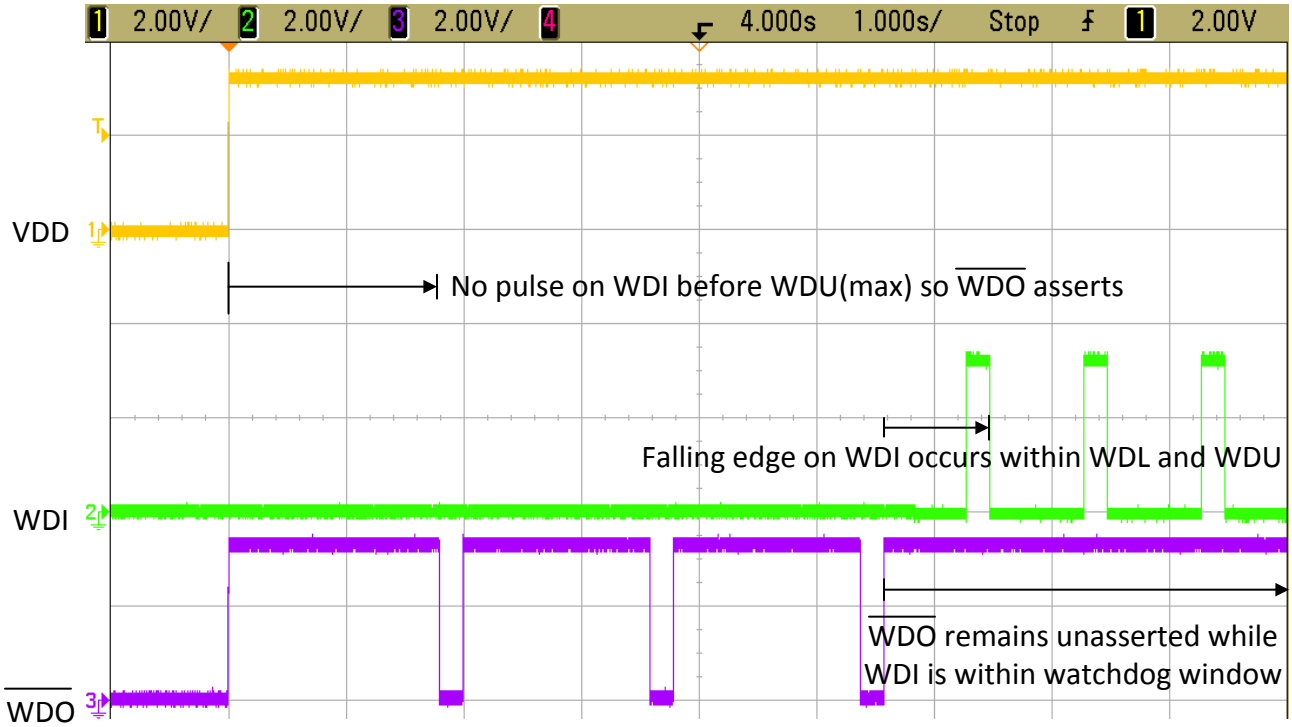


図 8-4. Watchdog Fault Caused by Missing WDI Pulse Until WDI pulses Arrive Within Watchdog Window to Deactivate WDO Fault

8.2.1.2.2 Setting the Watchdog Window - Design 1

The Watchdog Window is set via the CWD, SET0, and SET1 pin configurations. To achieve a Watchdog Timeout of 1 second, this design simply leaves CWD pin floating (NC - No Connect) and ties SET0 and SET1 to VDD to set these SET pins to logic high. With this configuration, the Watchdog Lower Boundary $t_{WDL\ (typ)}$ is set for 800ms and the Watchdog Upper Boundary $t_{WDU\ (typ)}$ is set for 1.6 seconds. Refer to Table 6.6 Timing Requirements to see the factory-programmed window watchdog timing configurations.

In 図 8-5 and 図 8-6 below, the watchdog window timing is shown by causing watchdog faults from pulses on WDI arriving too early and too late, respectively. When a pulse on WDI arrives too early, that is before $t_{WDL\ (min)}$ or too late, that is after $t_{WDU\ (max)}$, a watchdog fault occurs and $\overline{WDO}$ activates to logic low.

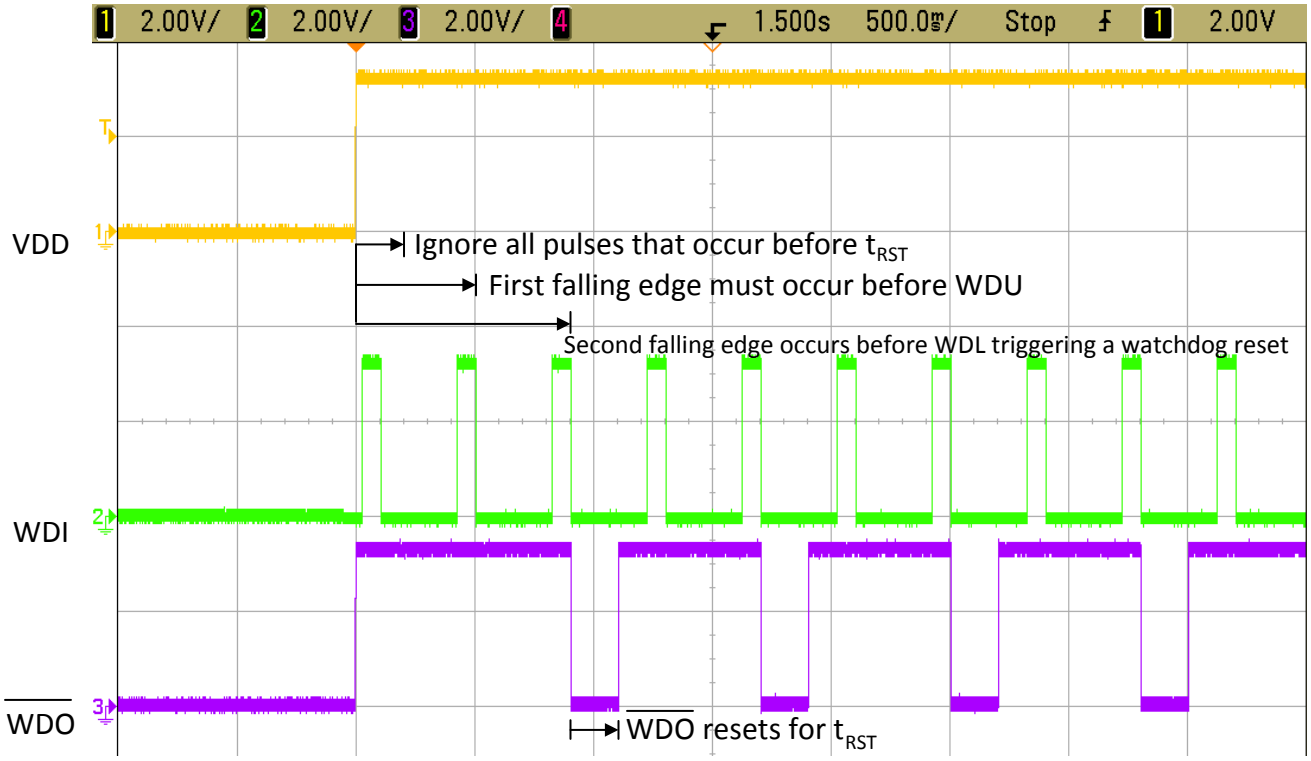


図 8-5. Watchdog Fault Caused by WDI Pulse Arriving Too Early (Before $t_{WDL\ (min)}$)

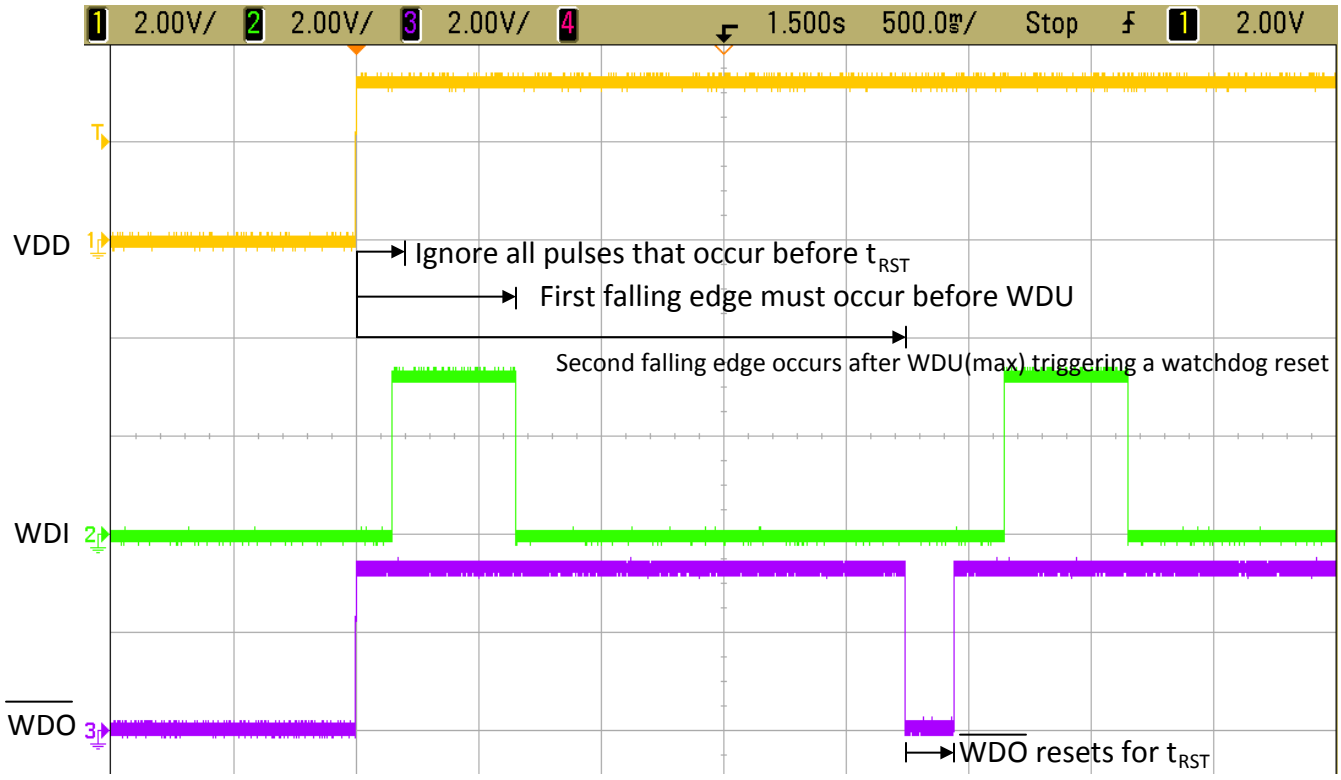


図 8-6. Watchdog Fault Caused by WDI Pulse Arriving Too Late (After $t_{WDU\ (max)}$)

8.2.1.2.3 Calculating the $\overline{\text{WDO}}$ Pull-up Resistor - Design 1

図 8-7 shows the TPS3430-Q1 uses an open-drain configuration for the $\overline{\text{WDO}}$ circuit. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below its maximum value. To choose the proper pull-up resistor, there are three key specifications to keep in mind: the pull-up voltage (V_{PU}), the recommended maximum $\overline{\text{WDO}}$ pin current (I_{WDO}), and V_{OL}. The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with I_{WDO} kept below 10 mA. For this example, with a V_{PU} of 3.3 V, a resistor must be chosen to keep I_{WDO} below 200 µA because this value is the maximum consumption current allowed. To ensure this specification is met, a pull-up resistor value of 16.5 kΩ is selected, which sinks a maximum of 200 µA when $\overline{\text{WDO}}$ is asserted. $\overline{\text{WDO}}$ current is at 200 µA and the low-level output voltage is approximately zero.

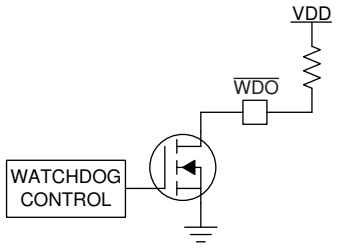


図 8-7. Open-Drain $\overline{\text{WDO}}$ Configuration

8.2.2 Monitoring Microcontroller with a Programmed Window Watchdog Timer - Design 2

A typical application for the TPS3430-Q1 is shown in 図 8-8. The TPS3430-Q1 is used to monitor the activity of the microcontroller via the WDI pin.

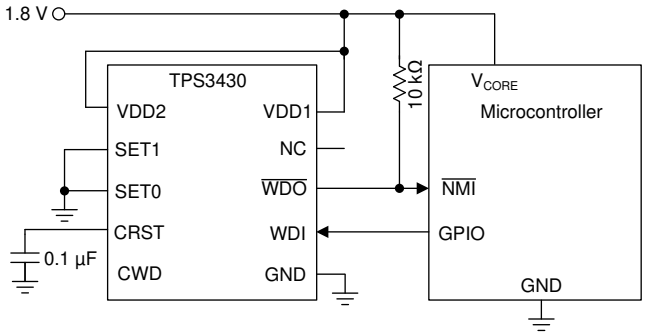


図 8-8. Monitoring Microcontroller Using a Window Watchdog Timer with Programmable Watchdog Reset Delay

8.2.2.1 Design Requirements - Design 2

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Watchdog Reset delay	Minimum reset delay of 250 ms	Minimum reset delay of 260 ms, reset delay of 322 ms (typical)
Watchdog window	Functions with a 30-Hz pulse-width modulation (PWM) signal with a 50% duty cycle	Leaving the CWD pin unconnected with SET0 = 0 and SET1 = 0 produces a window with a $t_{WDL(max)}$ of 25.9 ms and a $t_{WDU(min)}$ of 46.8 ms
Output logic voltage	1.8-V CMOS	1.8-V CMOS
Maximum device current consumption	200 µA	10 µA of current consumption, typical worst-case of 199 µA when $\overline{\text{WDO}}$ is asserted

8.2.2.2 Detailed Design Procedure - Design 2

8.2.2.2.1 Meeting the Minimum Watchdog Reset Delay - Design 2

The TPS3430-Q1 features three options for setting the watchdog reset delay: connecting a capacitor to the CRST pin, connecting a pull-up resistor, and leaving the CRST pin unconnected. If the CRST pin is either unconnected or pulled up the minimum timing requirement cannot be met, thus an external capacitor must be connected to the CRST pin. Because a minimum time is required, the worst-case scenario is a supervisor with a high CRST charging current (I_{CRST}) and a low CRST comparator threshold (V_{CRST}). For applications with ambient temperatures ranging from –40°C to +125°C, C_{CRST} can be calculated using $I_{CRST(MAX)}$, $V_{CRST(MIN)}$, and solving for C_{CRST} in 式 5:

$$C_{RST\,(MIN)} = \frac{I_{CRST\,(MAX)}}{V_{CRST\,(MIN)}} \times (t_{RST} - t_{INIT}) \tag{5}$$

When solving 式 5, the minimum capacitance required at the CRST pin is 0.086 µF. If standard capacitors with ±10% tolerances are used, then the minimum CRST capacitor required can be found in 式 6:

$$C_{RST(min)} = \frac{C_{RST(min)\_ideal}}{1 - C_{tolerance}} = \frac{0.086\ \mu F}{1 - 0.1} \tag{6}$$

Solving 式 6 where $C_{tolerance}$ is 0.1 or 10%, the minimum C_{CRST} capacitor is 0.096 µF. This value is then rounded up to the nearest standard capacitor value, so a 0.1-µF capacitor must be used to achieve this reset delay timing. If voltage and temperature derating are being considered, then also include these values in $C_{tolerance}$.

8.2.2.2.2 Setting the Watchdog Window - Design 2

In this application, the window watchdog timing options are based on the PWM signal that is provided to the TPS3430-Q1. A window watchdog setting must be chosen such that the falling edge of the PWM signal always falls within the window. A nominal window must be designed with $t_{WDL(max)}$ less than 33.33 ms and $t_{WDU(min)}$ greater than 33.33 ms. There are several options that satisfy this window option. An external capacitor can be placed on the CWD pin and calculated to have a sufficient window. Another option is to use one of the factory-programmed timing options. An additional advantage of choosing one of the factory-programmed options is the ability to reduce the number of components required, thus reducing overall BOM cost. Leaving the CWD pin unconnected (NC) with SET0 = 0 and SET1 = 0 produces a $t_{WDL(max)}$ of 25.9 ms and a $t_{WDU(min)}$ of 46.8 ms; see セクション 8.1.2.

8.2.2.2.3 Calculating the $\overline{WDO}$ Pull-up Resistor - Design 2

The TPS3430-Q1 uses an open-drain configuration for the $\overline{WDO}$ circuit, as shown in 図 8-7. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below its maximum value. To choose the proper pull-up resistor, there are three key specifications to keep in mind: the pull-up voltage (V_{PU}), the recommended maximum $\overline{WDO}$ pin current (I_{WDO}), and V_{OL}. The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with I_{WDO} kept below 10 mA. For this example, with a V_{PU} of 1.8 V, a resistor must be chosen to keep I_{WDO} below 200 µA because this value is the maximum consumption current allowed. To ensure this specification is met, a pull-up resistor value of 10 kΩ was selected, which sinks a maximum of 180 µA when $\overline{WDO}$ is asserted.

8.2.3 Monitoring Microcontroller with a Latching Window Watchdog Timer - Design 3

A safety critical application for the TPS3430-Q1 is shown in 図 8-9. The TPS3430-Q1 is used to monitor the activity of the microcontroller via the WDI pin and upon a watchdog fault, this design latches the $\overline{WDO}$ pin until the device VDD drops below $V_{DD\,(min)}$.

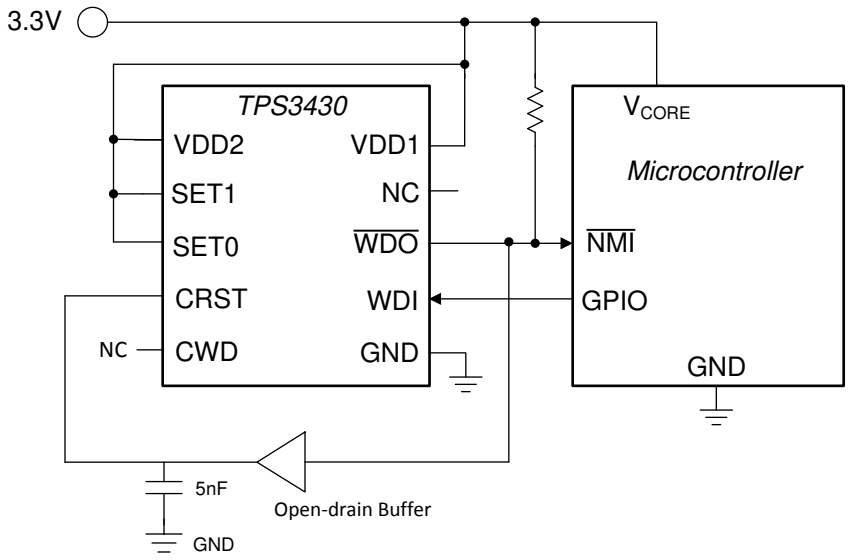


図 8-9. Monitoring Microcontroller Using a Latching Window Watchdog Timer

8.2.3.1 Design Requirements - Design 3

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Watchdog Reset delay	Latch $\overline{WDO}$ upon watchdog fault	Latching watchdog functionality that keeps $\overline{WDO}$ logic low when fault occurs
Watchdog window	Functions with a 1-Hz pulse-width modulation (PWM) signal with a 50% duty cycle	Leaving the CWD pin unconnected with SET0 = 1 and SET1 = 1 produces a window with a $t_{WDL(max)}$ of 920 ms and a $t_{WDU(min)}$ of 1360 ms
Output logic voltage	3.3-V Open-Drain	3.3-V Open-Drain
Maximum device current consumption	200 µA	10 µA of current consumption, typical worst-case of 199 µA when $\overline{WDO}$ is asserted

8.2.3.2 Detailed Design Procedure - Design 3

8.2.3.2.1 Meeting the Latching Output Requirement - Design 3

To achieve the latching watchdog feature, an open-drain buffer is connected from $\overline{WDO}$ to CRST with a small value capacitor connected from the Anode of the buffer connected to CRST to GND. The capacitor should be small value to prevent additional delay when triggering $\overline{WDO}$ to active low during watchdog fault. A capacitor between 150pF and 5nF is recommended.

In 図 8-10 below, the latching watchdog feature is shown by causing a watchdog fault and observing $\overline{WDO}$. Since no pulse arrive on WDI within the Watchdog Timeout, $\overline{WDO}$ activates and goes logic low and remains low. To reset the watchdog, the device must be restarted by dropping VDD below $V_{DD\ (min)}$.

8.2.3.2.2 Setting the Watchdog Window - Design 3

The Watchdog Window is set via the CWD, SET0, and SET1 pin configurations. To achieve a Watchdog Timeout of 1 second corresponding to a 1-Hz WDI signal, this design simply leaves CWD pin floating (NC - No Connect) and ties SET0 and SET1 to VDD to set the SET pins to logic high. With this configuration, the Watchdog Lower Boundary $t_{WDL\ (typ)}$ is set for 800 ms and the Watchdog Upper Boundary $t_{WDU\ (typ)}$ is set for 1.6 seconds. Refer to Table 6.6 Timing Requirements to see the factory-programmed window watchdog timing configurations.

8.2.3.3 Application Curve - Design 3

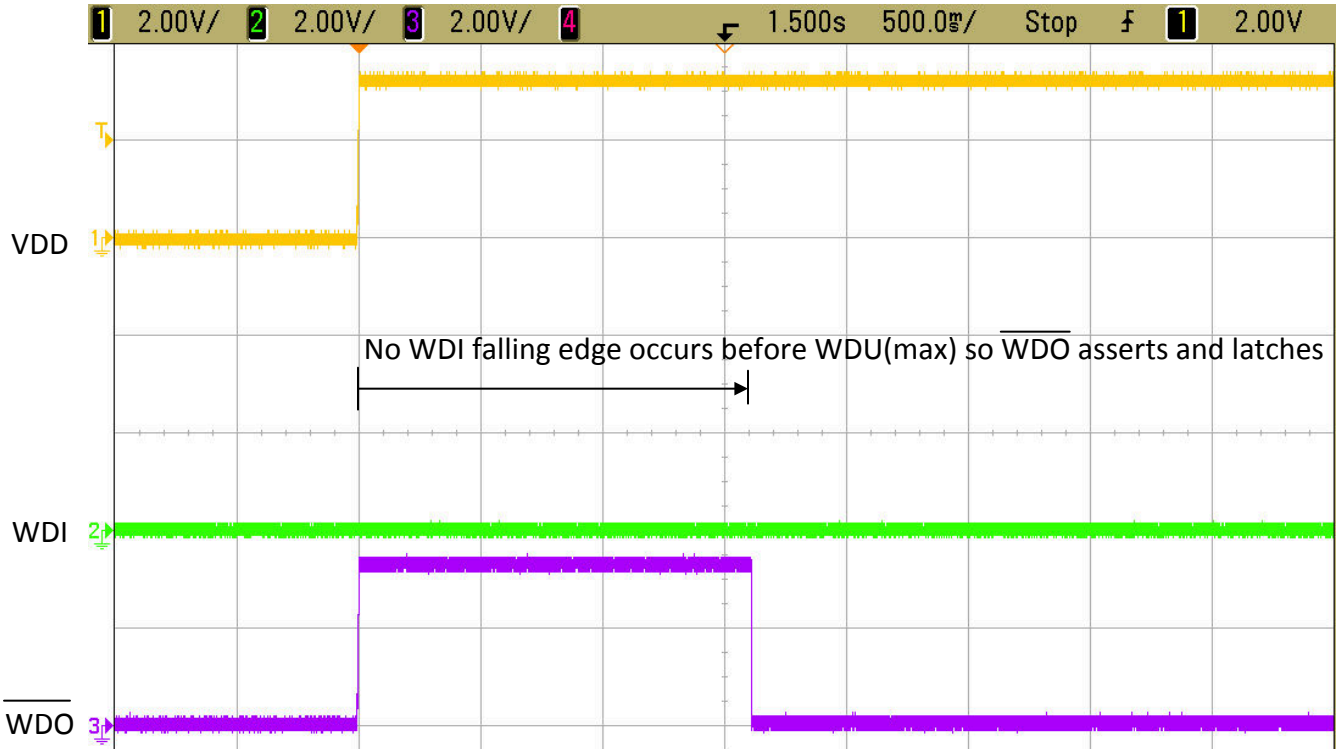


図 8-10. Watchdog Fault Caused by Missing WDI Pulse Shows $\overline{\text{WDO}}$ Latching

9 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.6 V and 6.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin. Please be sure to externally connect VDD1 to VDD2 as the device will not function if these pins are not connected.

10 Layout

10.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1-µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CRST pin, then minimize parasitic capacitance on this pin so the $\overline{WDO}$ delay time is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CRST} capacitor or pull-up resistor is used, place these components as close as possible to the CRST pin. If the CRST pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- If a C_{CWD} capacitor or pull-up resistor is used, place these components as close as possible to the CWD pin. If the CWD pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- Place the pull-up resistor on $\overline{WDO}$ as close to the pin as possible.

10.2 Layout Example

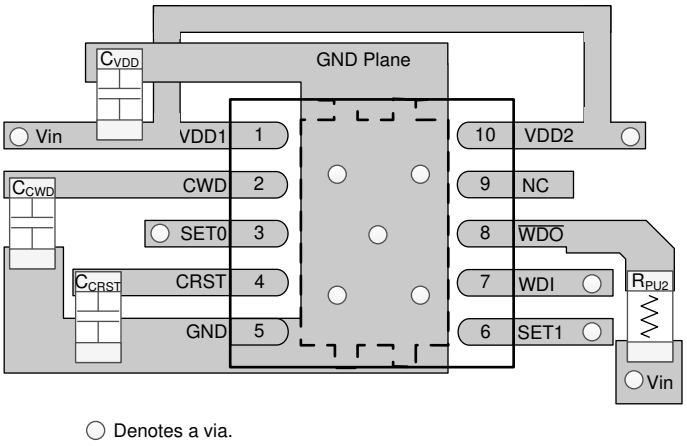


図 10-1. Typical Layout for the TPS3430-Q1

11 Device and Documentation Support

11.1 Device Support

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *TPS3430EVM Window Watchdog Timer with Programmable Timeout Delay User Guide*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3430WQDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	430AB
TPS3430WQDRCRQ1.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	430AB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS3430-Q1 :

- Catalog : TPS3430

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

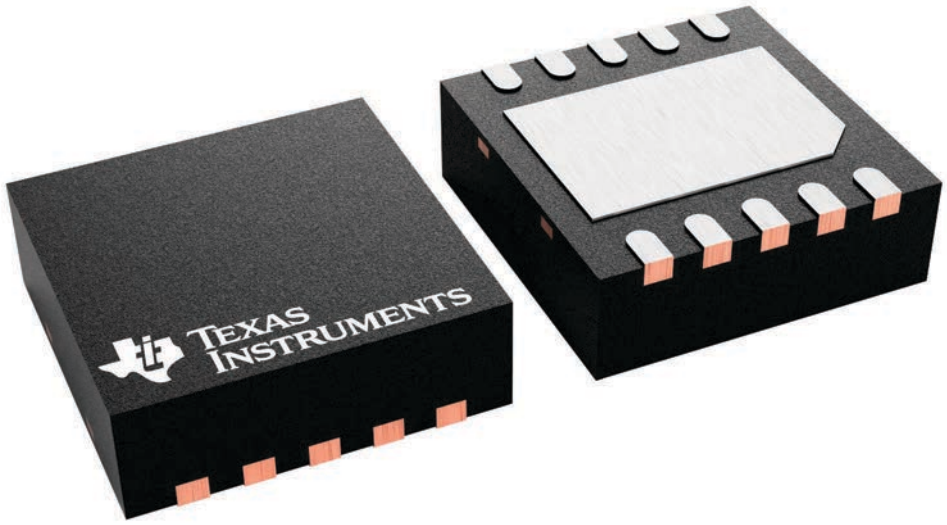
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

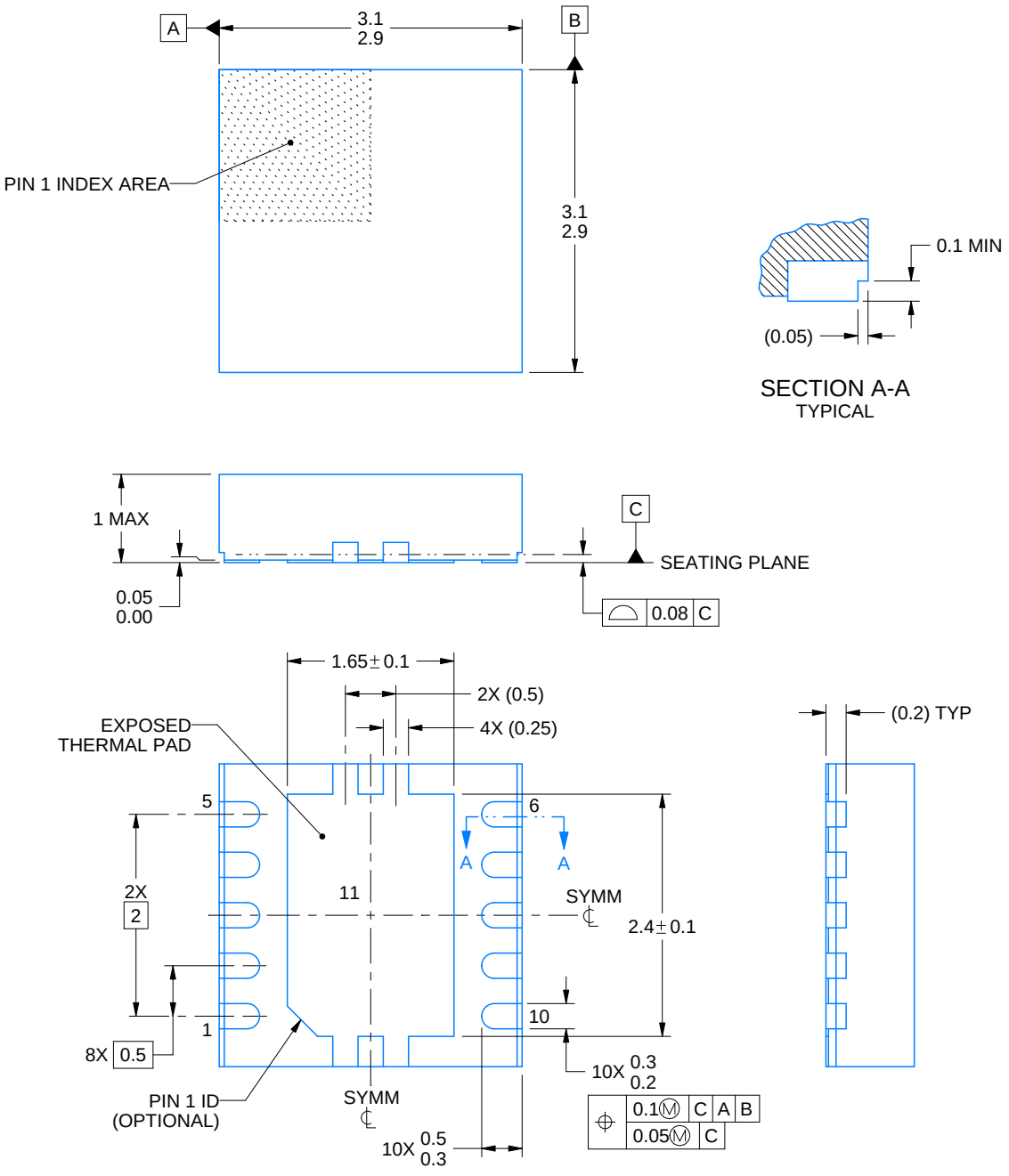
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



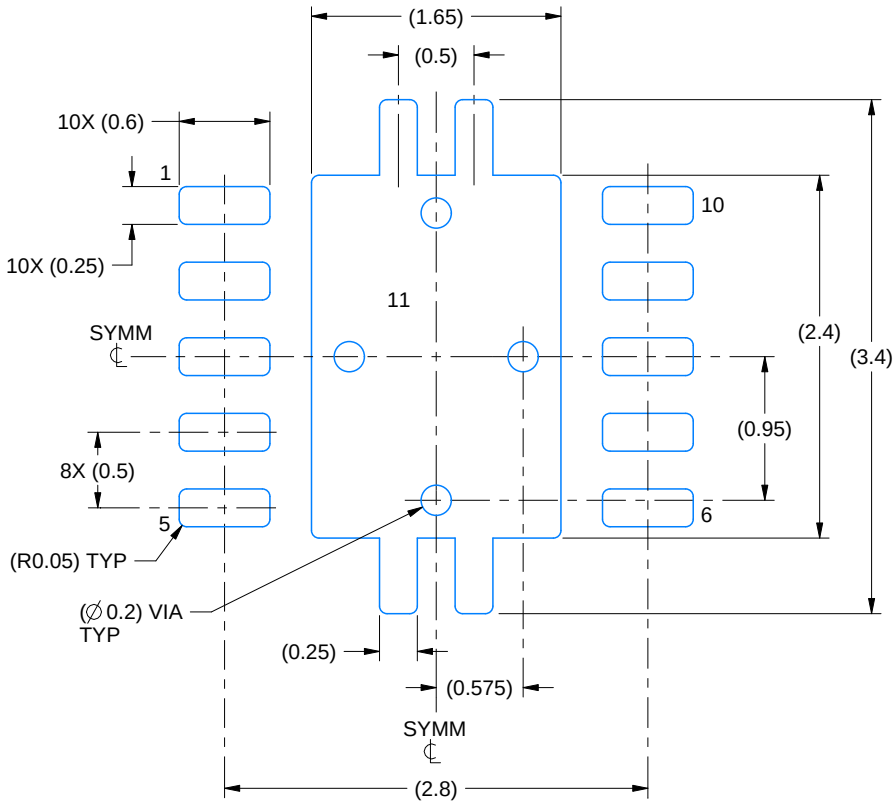
4226193/A

PLASTIC SMALL OUTLINE - NO LEAD

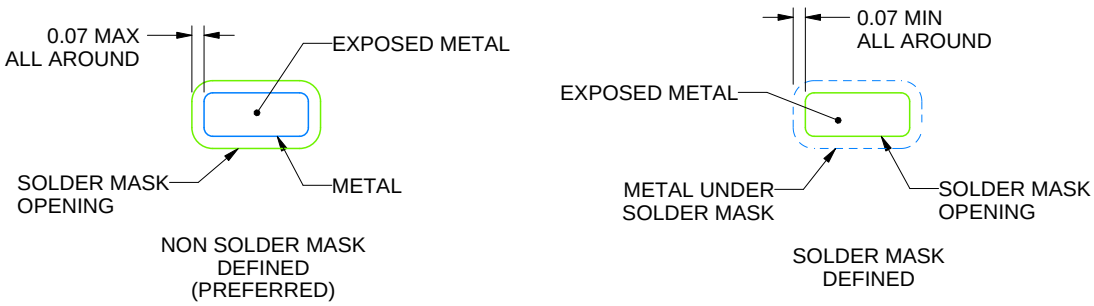


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

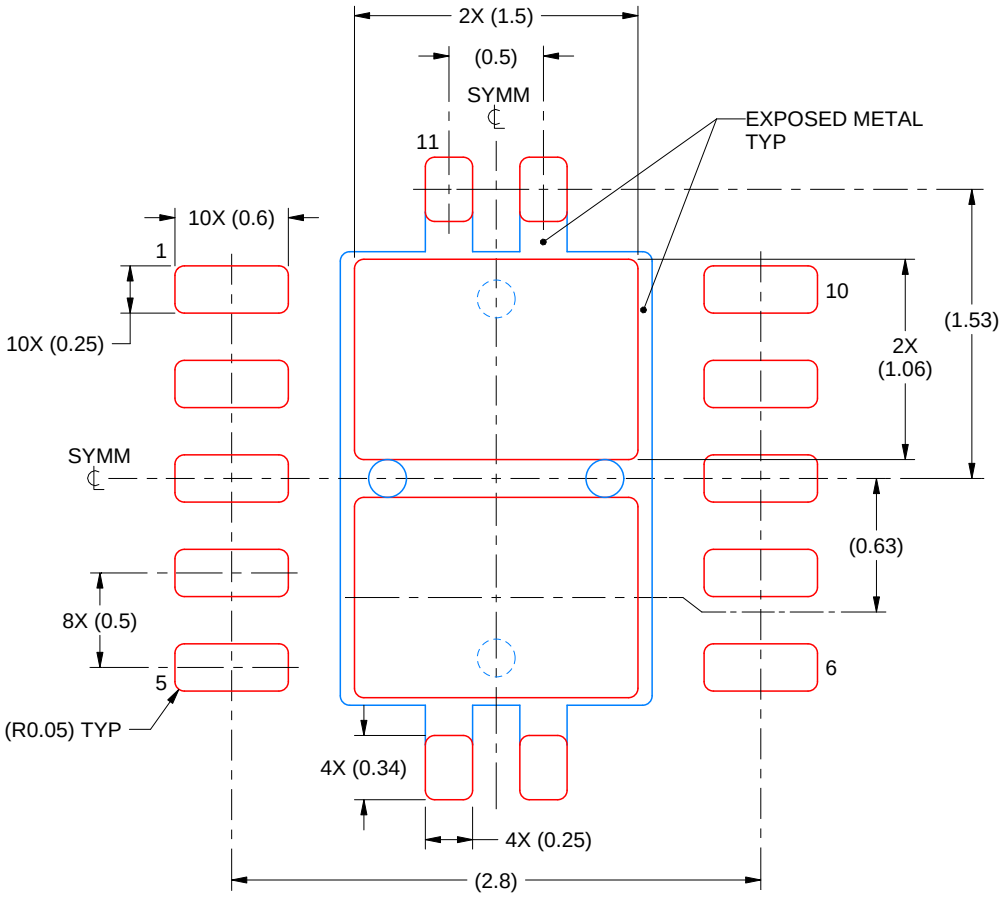


SOLDER MASK DETAILS

4223412/A 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



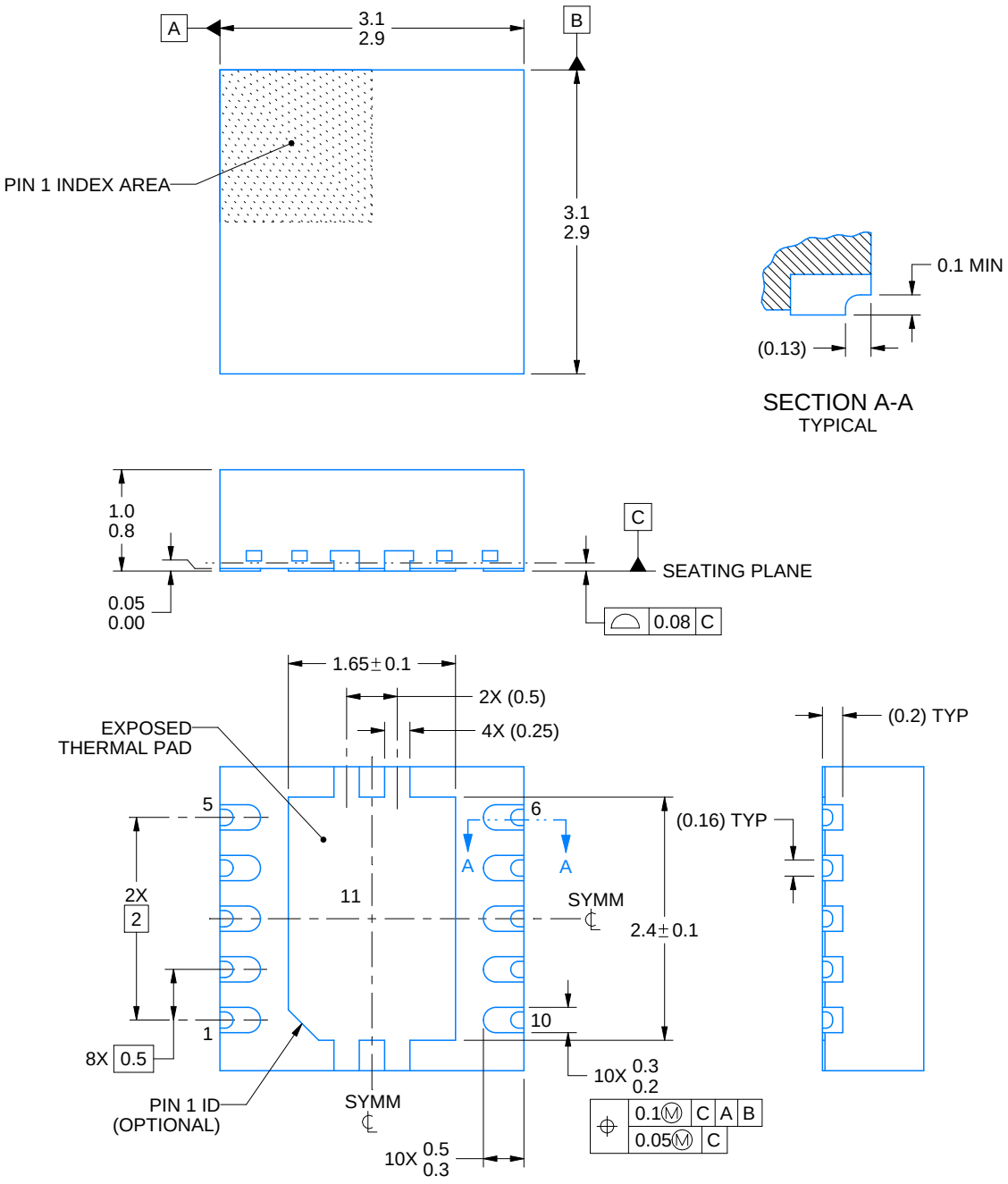
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4223412/A 01/2017

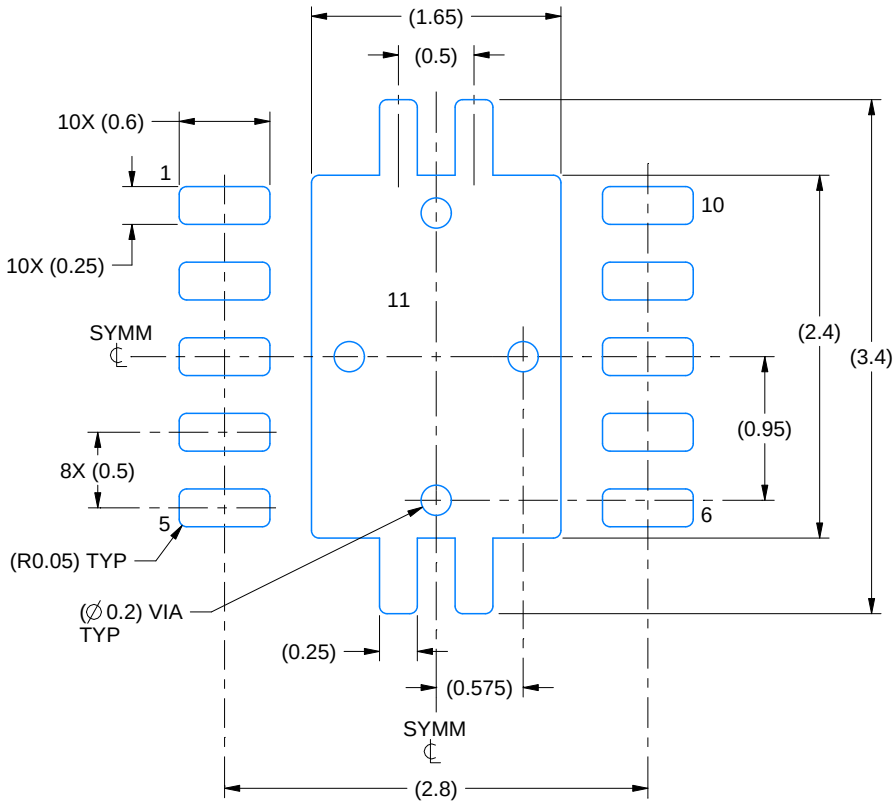
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

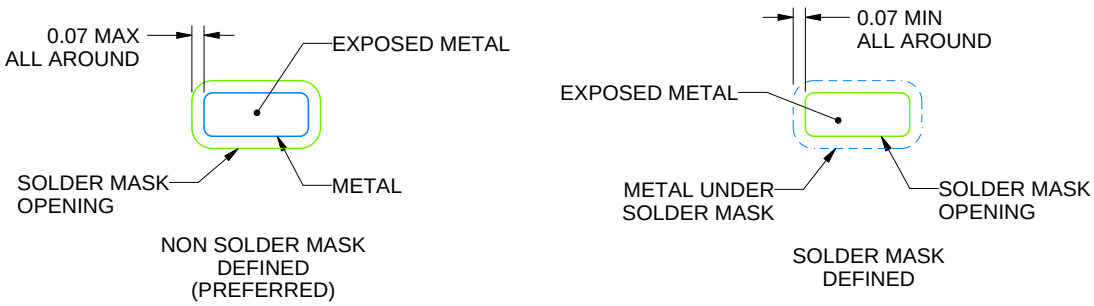


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

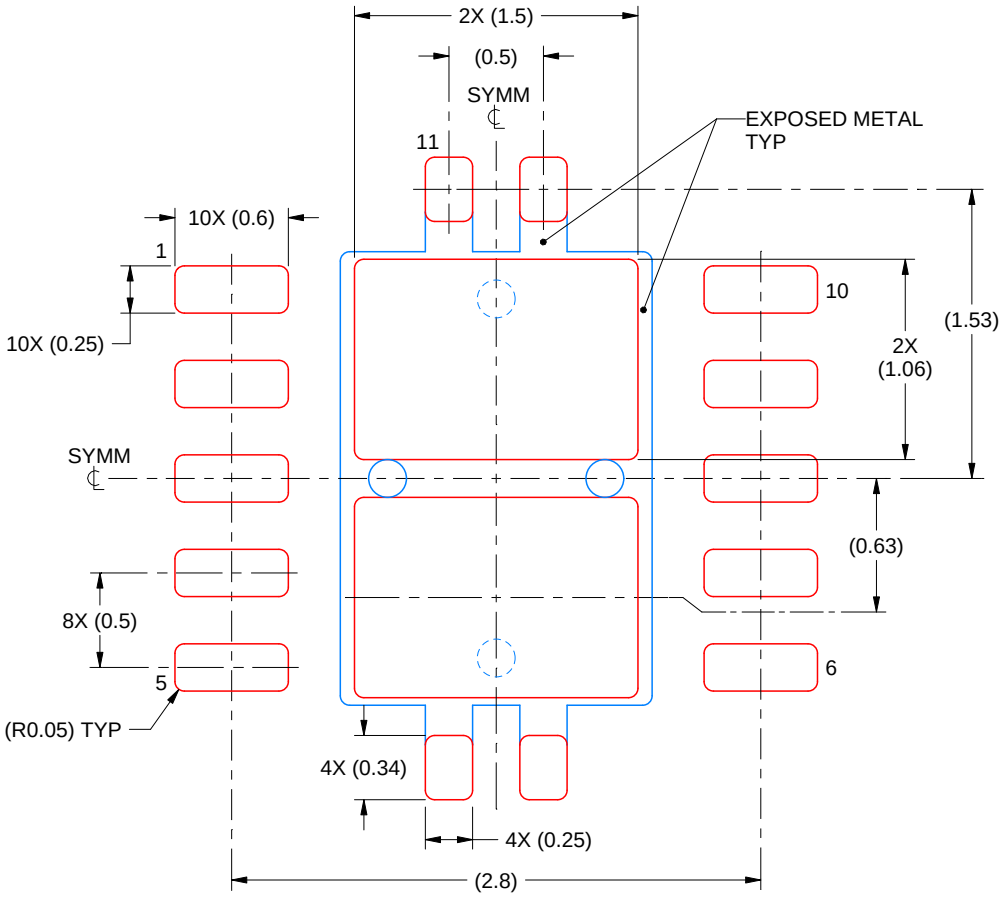


SOLDER MASK DETAILS

4225163/A 07/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4225163/A 07/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月