TEXAS INSTRUMENTS
TPS2HCS10-Q1
JAJSOU6 – OCTOBER 2023

TPS2HCS10-Q1 11mΩ、車載用デュアル・チャネルの SPI 制御ハイサイド・スイッチ、低静止電流オン・モード、I^2t ワイヤ保護内蔵

1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - 温度グレード 1:–40℃～125℃
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C5
  - 35V の負荷ダンプへの耐性
- 機能安全準拠開発
  - ASIL-B までの ISO 26262 システム設計を支援する安全メカニズムに関するドキュメントを製品リリース時に提供予定
- 25℃ の FET で 11mΩ の Rdson を標準値とするデュアル・チャネルの SPI 制御スマート・ハイサイド・スイッチ
- MCU を介さないワイヤ・ハーネス保護機能と SPI でプログラム可能なヒューズ曲線を内蔵
  - 持続的な過負荷状態からの保護
- SPI でプログラム可能な可変過電流保護によりシステム・レベルの信頼性を向上
  - 過電流保護スレッショルド:10～70 A
- 幅広い容量性入力 ECU の負荷電流ニーズに対応する SPI で構成可能な容量性充電モード
- 低静止電流 / 低消費電力オン状態で常時オンの負荷に電力を供給、MCU に対するウェーク信号によりウェイクオン時の負荷電流を自動的に供給
- 堅牢な出力保護機能を内蔵:
  - 熱保護機能を内蔵
  - グランド短絡からの保護
  - 逆電源電圧による FET の自動スイッチ・オンを含むバッテリ逆接続からの保護
  - バッテリおよびグランドの喪失時に自動シャットオフ
  - 誘導性負荷の逆起電圧の発生を防止する出力クランプを内蔵
- SPI によるデジタル・センス出力で以下を測定するように構成可能:
  - 負荷電流 (内蔵 ADC による高精度の測定)
  - 出力または電源電圧、FET 温度
- SPI インターフェイスによる完全なフォルト診断と FLT ピンによるフォルト表示
  - 開放負荷とバッテリ短絡の検出

2 アプリケーション

- 車載ゾーン ECU
- パワー・ディストリビューション・モジュール
- 車体制御モジュール

3 概要

TPS2HCS10-Q1 デバイスは、シリアル・ペリフェラル・インターフェイス (SPI) で制御されるデュアル・チャネルのスマート・ハイサイド・スイッチです。このデバイスには堅牢な保護機能が内蔵されており、短絡や過負荷の状態から出力ワイヤと負荷を確実に保護できます。このデバイスには、2 つの範囲のスレッショルドを SPI で構成可能な過電流保護機能が搭載されています。これにより、大きな突入電流を必要とする負荷をサポートする十分な柔軟性が得られると同時に、保護機能も強化されます。さらに、このデバイスには持続的な過負荷状態下でスイッチをオフにするプログラム可能なヒューズ・プロファイル (電流と時間) が内蔵されており、MCU のオーバーヘッドが軽減されます。これらの 2 つの機能を組み合わせた完全な保護機能により、あらゆる負荷プロファイルに対してワイヤ・ハーネスを最適化できます。

このデバイスは、パワー・ディストリビューション・スイッチ・アプリケーションの ECU 負荷用に、SPI で構成可能な容量性充電モードをサポートしています。また、このデバイスには低静止電流オン状態もあり、この状態でのピーク電流は最大 800mA、消費電流は約 10µA です。

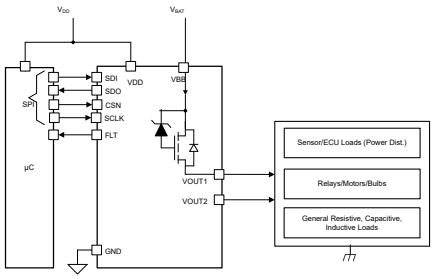
TPS2HCS10-Q1 デバイスは SPI による高精度のデジタル電流センスも備えているため、負荷の診断も強化されます。負荷電流、チャネル出力電圧、出力 FET 温度をシステムの MCU に報告することで、スイッチや負荷の障害を診断することができます。

TPS2HCS10-Q1 は、PCB の占有面積を減らすことができる HTSSOP パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
TPS2HCS10-Q1	PWP (HTSSOP、16)	5.0mm × 6.40mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2023	*	Initial Release

5 Pin Configuration and Functions

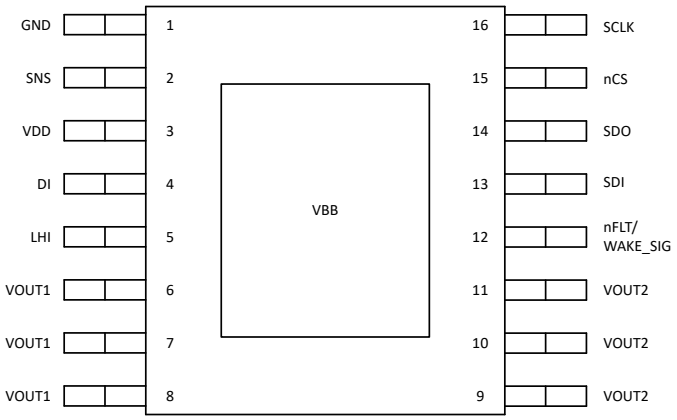

図 5-1. PWP Package, 16-Pin HTSSOP (Top View)

表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	GND	—	Device ground.
2	SNS	O	Sense current output. Use a parallel RC network to the GND pin of the IC.
3	VDD	P	Logic supply input. Closely decouple to the GND pin of the IC with a ceramic 1-µF capacitor.
4	DI	I	Sets the output behavior in the LIMP HOME mode, if configured as such. *The pin needs to be connected to MCU or other HI/LO source through a 10-kΩ resistor for protection and enabling the reverse polarity FET turn-on function.*
5	LHI	I	Externally enables the LIMP HOME mode.
6, 7, 8	VOUT1	O	Output of channel 1.
9,10, 11	VOUT2	O	Output of channel 2.
12	$\overline{\text{FLT}}$,$\overline{\text{WAKE\_SIG}}$	O	Fault output (active low), indicating faulton any (one or more) channel. Open drain, pull up with a 4.7-kΩ resistor to the VDD pin. Also functions as a wake signal to the MCU upon load current demand in Low Power Mode or the vehicle key-off mode.
13	SDI	I	SPI device (secondary) data input.
14	SDO	O	SPI data output from the device. Internally pulled up to VDD.
15	$\overline{\text{CS}}$	I	SPI interface chip select (active low). Internally pulled up to VDD.
16	SCLK	I	SPI interface clock input to the device.
Exposed pad	VBB	P	Power supply input.

(1) I = input, O = output, P = power

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5.1 Recommended Connections for Unused Pins

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum continuous supply voltage, V_{VBB}			28	V
Load dump voltage	ISO16750-2:2010(E)		36	V
Maximum transient voltage on VBB pin, (example during ISO 7637 pulse 2a transient) V_{BBt}			54	V
VOUT voltage		–30	V_{VS}+0.3	V
Reverse polarity voltage, continuous on VBB pin		–18		V
Low voltage supply pin voltage, V_{DD}		–0.3	5.5	V
Digital input pin voltages, V_{DIG}	SDI, SDO, SCLK, $\overline{CS}$	–0.3	5.5	V
Sense pin voltage, V_{SNS}		–0.3	5.5	V
$\overline{FLT}$ pin voltage, V_{FLT}		–0.3	5.5	V
Limp home activation pin voltage, V_{LHI}			V_{BB}	V
Limp home direct input pin voltages, V_{DI}		–0.3	5.5	V
Reverse ground current, I_{GND}	V_{BB} < 0 V		–50	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per AEC Q100-002 Classification Level H2	All pins including VBB and VOUTx	±2000	V
		Human-body model (HBM), per AEC Q100-002 Classification Level H3A(2)	VBB and VOUTx	±4000	
		Charged-device model (CDM), per AEC Q100-011 Classification Level C5	All pins	±750	

(1) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.
(2) ESD strikes are with reference from the pin mentioned to GND

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BB_NOM}	Nominal supply voltage		6	18	V
V_{BB_EXT}	Extended supply voltage	See the conditions in section 9.2, power supply recommendations, operating voltage range	3	28	V
V_{DD}	Low voltage supply voltage		3.0	5.5	V
V_{DIG}	All digital input pin voltage		–0.3	5.5	V
$V_{\overline{FLT}}$	$\overline{FLT}$ pin voltage		–0.3	5.5	V
V_{LHI}	Limp home activation pin voltage, LHI			V_{BB}	V
V_{DI}	Limp home direct pin input voltage, DI		–0.3	5.5	V

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6.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS2HCS10-Q1 PWP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the https://www.ti.com/lit/an/spra953c/spra953c.pdf application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{BB} = 6 V to 18 V, V_{DD} = 3.0 V to 5.5 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
V_{Clamp}	VDS clamp voltage	FET current = 10 mA VBB > 28 V	T_J = 25°C to 150°C	35	40	45	V
V_{Clamp}	VDS clamp voltage	FET current = 10 mA 12 V < VBB < 28 V	T_J = –40°C to 150°C	30	34	38	V
V_{Clamp}	VDS clamp voltage	FET current = 10 mA VBB = 3 V	T_J = –40°C to 150°C	27.5		36.5	V
V_{VBB_UVLOR}	V_{BB} undervoltage lockout rising	Measured with respect to the GND pin of the device, FETs can turn-on above this level, full switch functionality and OCP and TSD protection. Diagnostics only at > 6 V	Measured with respect to the GND pin of the device, FETs can turn-on above this level, full switch functionality and OCP and TSD protection. Diagnostics only at > 6 V	3.0	3.5	4.0	V
V_{VBB_UVLOF}	V_{BB} undervoltage lockout falling	Measured with respect to the GND pin of the device, FETs turn-off below this level.	Measured with respect to the GND pin of the device, FETs turn-off below this level.	2.6	2.8	3.0	V
$V_{BB\_UV\_WRN\_R}$	VBB voltage UV_WRN bit is set (rising threshold)	Measured with respect to the GND pin of the device. V_{BB} undervoltage at which diagnostics is turned ON.			4.9		V
$V_{BB\_UV\_WRN\_F}$	V_{BB} undervoltage at which diagnostics is turned OFF	Measured with respect to the GND pin of the device. V_{BB} undervoltage at which diagnostics are no longer available (turned OFF). Overcurrent and thermal protection is available till VBB_UVLO			4.5		V
V_{VDD_UVLOF}	V_{VDD} undervoltage lockout falling	SPI communication is lost		1.95		2.07	V
V_{VDD_UVLOR}	V_{VDD} undervoltage lockout rising	Measured with respect to the GND pin of the device		2.02		2.2	V
V_{VDD_UVLOH}	V_{VDD} undervoltage lockout hysteresis	$V_{UVLOR} – V_{UVLOF}$			0.09		V

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6.5 Electrical Characteristics (続き)

V_{BB} = 6 V to 18 V, V_{DD} = 3.0 V to 5.5 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IL_{NOM}	Continuous load current, per channel	All channels enabled, T_{AMB} = 85°C			7		A
		One channel enabled, T_{AMB} = 85°C			12		A
$I_{SLEEP,VBB}$	Sleep current (total device leakage including all MOSFET channels)	V_{BB} ≤ 18 V, device in SLEEP mode, V_{OUT} = 0 V	T_J = 25°C			0.3	µA
$I_{SLEEP,VBB}$	Sleep current (total device leakage including all MOSFET channels)	V_{BB} ≤ 18 V, device in SLEEP mode, V_{OUT} = 0 V	T_J = 85°C			1.8	µA
$I_{OUT(OFF)}$	Output leakage current (per channel) from the FET, ACTIVE mode	V_{BB} ≤ 18 V, V_{OUT} = 0 FET off, ACTIVE mode	T_J = –40 to 125°C			12	µA
I_{DD}	Active State VDD quiescent current, SCLK off, ACTIVE state,	6 V < V_{BB} ≤ 18 V, V_{DD} = 5.5 V				1.5	mA
I_{DD}	Active State VDD quiescent current, SCLK off, ACTIVE state	6 V < V_{BB} ≤ 18 V, V_{DD} = 3.0 V				60	µA
I_{DDQ}	Active State VDD quiescent current, SCLK ON, 10 MHz, ACTIVE state	6 V < V_{BB} ≤ 18 V, V_{DD} = 5.5 V				2	mA
V_{BB} I_Q	V_{BB} quiescent current, SCLK off, all diagnostics disabled,(OL_OFF, OL_ON, SHRT_VS, ISNS, ADC)	V_{BB} ≤ 18 V, V_{DD} = 5.5 V All channels enabled, I_{OUTx} = 0 A			2.35	2.75	mA
V_{BB} I_Q	V_{BB} quiescent current, SCLK off, all diagnostics disabled, (OL_OFF, OL_ON, SHRT_VS, ISNS, ADC)	V_{BB} ≤ 18 V, V_{DD} = 3.0 V All channels enabled, I_{OUTx} = 0 A			3.6	4.5	mA
V_{BB} I_Q	V_{BB} quiescent current, SCLK off, all diagnostics (ISNS, ADC) enabled	V_{BB} ≤ 18 V, V_{DD} = 3.0 V All channels enabled, I_{OUTx} = 0 A			4.9	6	mA
RON CHARACTERISTICS							
R_{ON}	On-resistance (Includes MOSFET and package)	6 V ≤ V_{BB} ≤ 28 V, I_{OUTx} = 1 A	T_J = 25°C		11.3		mΩ
R_{ON}	On-resistance (Includes MOSFET and package)	6 V ≤ V_{BB} ≤ 28 V, I_{OUTx} = 1 A	T_J = 150°C			22	mΩ
$R_{ON(REV)}$	On-resistance during reverse polarity	–18 V ≤ V_{BB} ≤ –7 V	T_J = 25°C		10		mΩ
			T_J = 150°C			25	mΩ
CURRENT SENSE CHARACTERISTICS							
K_{SNS}	Current sense ratio I_{OUTx} / I_{SNS}	I_{OUT} = 1.0 A, OL_ON_EN_CHx = 0	I_{OUT} = 1.0 A, OL_ON_EN_CHx = 0		5000		
K_{SNS}	Current sense ratio I_{OUTx} / I_{SNS}	I_{OUT} = 50 mA, OL_ON_EN_CHx = 1	I_{OUT} = 50 mA, OL_ON_EN_CHx = 1		1200		
I_{SNSI}	Current sense current	Channel current sense diagnostic ADC enabled, OL_ON_EN_CHx = 0	I_{OUT} = 10 A (±4% error)	1.92	2.00	2.08	mA
I_{SNSI}	Current sense current	Channel current sense diagnostic ADC enabled, OL_ON_EN_CHx = 0	I_{OUT} = 2 A (±4% error)	0.385	0.40	0.41	mA
I_{SNSI}	Current sense current	Channel current sense diagnostic ADC enabled, OL_ON_EN_CHx = 0	I_{OUT} = 500 mA (±6% error)	0.096	0.10	0.106	mA

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6.5 Electrical Characteristics (続き)

V_{BB} = 6 V to 18 V, V_{DD} = 3.0 V to 5.5 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SNSI}	Current sense current	Channel current sense diagnostic ADC enabled, OL_ON_EN_CHx = 1	I_{OUT} = 25 mA (15 % error)	0.018	0.021	0.024	mA
ADC CHARACTERISTICS							
$V_{ADCEFfHI}$	ADC reference voltage			2.76	2.8	2.84	V
Isample	Current sense sampling time	Including mux timing and ADC conversion time		50			µs
I_{ADC}	ADC current consumption					0.5	mA
SNS CHARACTERISTICS							
ADC $VOUT_{SNS\_CHx}$	ADC $VOUT_{SNS}$ output code	VOUT_CHx = 13.5 V	Includes buffer gain		459		
OVERCURRENT PROTECTION CHARCTERISTICS							
I_{OCth}	Overcurrent protection threshold, immediate shutdown mode	T_J = –40°C to 125°C	IOC setting = 62.5 A, VBB = 18 V dI/dt = 2 A / µs		65		A
I_{CL_ENPS}	Peak current enabling into permanent short, immediate shutdown	T_J = –40°C to 125°C	OCP setting = 62.5 A, Test setup per AEC Q100-12			70	A
CAP CHRG CURRENT LIMITATION							
I_{CL_Reg}	Regulation mode current	T_J = –40°C to 125°C dI/dt < 0.01 A/ms	SPI Setting (ILIM_CHx_SET) of 10 A, I_{ILIM} = 2 A	1.70	2.15	2.5	A
I_{CL_Reg}	Regulation mode current	T_J = –40°C to 125°C dI/dt < 0.01 A/ms	SPI Setting (ILIM_CHx_SET) of 20 A, I_{ILIM} = 4 A	3.35	3.8	4.55	A
CAPACITIVE CHARGING							
T_{DELAY_RANGE}	Range of Tdelay settings	SPI settting, Pulsed current mode		1		100	ms
dV_dt_{RANGE}	Range of dV/dt during Tdelay	SPI settting, dV/dt mode	VBB = 16V, Capacitance = 1 mF	0.33		1.6	V/ms
FAULT CHARACTERISTICS							
I_{OL_OFF}	Off state open-load (OL) detection internal pull-up current	Switch disabled, OL_OFF_EN_CHx = enabled	OL_PULLUP_STR=00	23	25	28	µA
			OL_PULLUP_STR=01	52	57	63	µA
			OL_PULLUP_STR=10	112	121	130	µA
			OL_PULLUP_STR=11	235	256	265	µA
R_{SHRT_VBB}	Off state short to VBB detection pulldown resistance	Channel disabled, off-state short_VBB diagnostics enabled		6	7.5	9	kΩ
$V_{OL\_OFF\_TH}$	Off state Open-load (OL) detection voltage	Channel Disabled, off-state open load diagnostics enabled, V_{OUTx}		1.9	2.5	2.95	V
T_{ABS}	Thermal shutdown			155	180	205	°C
T_{OTW}	Thermal shutdown warning			130	150	170	°C
T_{REL}	Relative thermal shutdown temperature				60		°C
T_{HYS}	Thermal shutdown hysteresis			20	25	30	°C
PWM CHARACTERISTICS							
PWM_{FREQ}	PWM Frequency	PWM_EN = 1	PWM_FREQ_CHx = 000	0.80	0.86	0.93	Hz
PWM_{FREQ}	PWM Frequency	PWM_EN = 1	PWM_FREQ_CHx = 111	1637	1770	1903	Hz

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6.5 Electrical Characteristics (続き)

V_{BB} = 6 V to 18 V, V_{DD} = 3.0 V to 5.5 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LOW POWER MODE CHARACTERISTICS							
R_{DSON}	RDSON Low Power Mode (LPM)	T_J = –40°C to 125°C	T_J = –40°C to 125°C		60		mΩ
$ILOAD_{EXIT}$	Load current when the channel exits LPM	Exit Threshold Setting = 00 (600 mA) Current ramp at 1 mA/µs		525	600	675	mA
IVDDLPM	IVDD in LPM mode both channels ON Iout = 0	VDD = 5.0 V	T_J = –40°C to 85°C		14		µA
IVBBLPM	IVBB per channel, both channels OFF, Iout = 0	VDD = 5.0 V	T_J = –40°C to 85°C		2.5		µA
IVBBLPM	IVBB per channel, one channel ON, Iout = 0	VDD = 5.0 V	T_J = –40°C to 85°C		3.6		µA
IVBBLPM	IVBB per channel, both channels ON, Iout = 0	VDD = 5.0 V	T_J = –40°C to 85°C		4.5		µA
DIGITAL INPUT PIN CHARACTERISTIC							
$V_{IH, DIG}$	Digital pin Input voltage high-level	3.0 V ≤ VDD ≤ 5.5 V		0.7 × V_{VDD}			V
$V_{IL, DIG}$	Digital pin Input voltage high-level	3.0 V ≤ VDD ≤ 5.5 V				0.3 × V_{VDD}	V
R_{DIGx}	Internal pulldown resistor			0.7	1.0	1.8	MΩ
$I_{IH, DIG}$	Input current high-level	V_{DIG} = 5 V			5		µA
DIGITAL OUTPUT PIN CHARACTERISTICS							
V_{OH_SDO}	Output logic high voltage drop	SDO pin current = 2 mA				0.2	V
V_{OL_FLT}	Output logic high voltage drop	$\overline{FLT}$ pin current = 4mA				0.5	V

6.6 SPI Timing Requirements

Over operating junction temperature T_J = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SPI}	SPI clock (SCLK) frequency	C_{SDO} = 30 pF, IO protection resistor 0.47 kΩ			8	MHz
t_{high}	High time: SCLK logic high-time duration		45			ns
t_{low}	Low time: SCLK logic low-time duration		45			ns
t_{sucs}	$\overline{CS}$ setup time: time delay between falling edge of $\overline{CS}$ and rising edge of SCLK		45			ns
t_{su_SDI}	SDI setup time: setup time of SDI before the falling edge of SCLK		15			ns
t_{h_SDI}	SDI hold time: hold time of SDI before the falling edge of SCLK		30			ns
t_{d_SDO}	Delay time: time delay from rising edge of SCLK to data valid at SDO				30	ns
t_{hcs}	Hold time: time between the falling edge of SCLK and rising edge of $\overline{CS}$		45			ns
t_{dis_cs}	$\overline{CS}$ disable time, $\overline{CS}$ high to SDO high impedance			10		ns
t_{hics}	SPI transfer inactive time (time between two transfers) during which $\overline{CS}$ must remain high		500			ns

6.7 Switching Characteristics

Over operating junction temperatures, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR1}	Channel turnon delay time	V_S = 13.5 V, R_L = 2 Ω, 50% of $\overline{CS}$ to 10% of VOUT, default slew rate	8	30	45	µs

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6.7 Switching Characteristics (続き)

Over operating junction temperatures, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DF1}	Channel turnoff delay time	V_S = 13.5 V, R_L = 2 Ω 50% of CS/EN to 90% of VOUT default slew rate	10	20	30	µs
SR_R	VOUT rising slew rate	V_{BB} = 13.5 V, 20% to 80% of V_{OUT}, R_L = 2 Ω Slew Rate Setting (SLRT_CHx) = 11		0.55		V/µs
		V_{BB} = 13.5 V, 20% to 80% of V_{OUT}, R_L = 2 Ω Slew Rate Setting (SLRT_CHx) = 10		0.45		V/µs
		V_{BB} = 13.5 V, 20% to 80% of V_{OUT}, R_L = 2 Ω Slew Rate Setting (SLRT_CHx) = 01		0.34		V/µs
		V_{BB} = 13.5 V, 20% to 80% of V_{OUT}, R_L = 2 Ω Slew Rate Setting (SLRT_CHx) = 00		0.25		V/µs
SR_F	VOUT falling slew rate	V_{BB} = 13.5 V, 80% to 20% of V_{OUT}, R_L = 2 Ω Slew Rate Setting (SLRT_CHx) = 11		0.56		V/µs
		V_{BB} = 13.5 V, 80% to 20% of V_{OUT}, R_L = 2 Ω Slew Rate Setting (SLRT_CHx) = 10		0.42		V/µs
		V_{BB} = 13.5 V, 80% to 20% of V_{OUT}, R_L = 2 Ω Slew Rate Setting (SLRT_CHx) = 01		0.30		V/µs
		V_{BB} = 13.5 V, 80% to 20% of V_{OUT}, R_L = 2 Ω Slew Rate Setting (SLRT_CHx) = 00		0.21		V/µs
t_{ON}	Channel turnon time	SLRT_CHx=10 (default)	40	53	70	µs
t_{OFF}	Channel turnoff time	SLRT_CHx=10 (default)	30	36	50	µs
t_{ON} - t_{OFF}	Turnon and off matching	1 ms ON time switch enable pulse, V_{BB} = 13.5 V, R_L = 2 Ω	–10		30	µs
		200-µs OFF time switch enable pulse, V_{BB} = 13.5 V, R_L = 2 Ω, frequency = 1 kHz	–20		20	µs
		200-µs ON time switch enable pulse, V_S = 13.5 V, R_L = 2 Ω, frequency = 1 kHz	–15	–4	5	µs
E_{ON}	Switching energy losses during turnon	V_S = 13.5 V, R_L = 2 Ω, 1 ms pulse - VOUT from 0 to VS Slew Rate Setting (SLRT_CHx) = 11		0.4		mJ
		V_S = 13.5 V, R_L = 2 Ω, 1 ms pulse - VOUT from 0 to VS Slew Rate Setting (SLRT_CHx) = 10		0.5		mJ
		V_S = 13.5 V, R_L = 2 Ω, 1 ms pulse - VOUT from 0 to VS Slew Rate Setting (SLRT_CHx) = 01		0.65		mJ
		V_S = 13.5 V, R_L = 2 Ω, 1 ms pulse - VOUT from 0 to VS Slew Rate Setting (SLRT_CHx) = 00		0.9		mJ
E_{OFF}	Switching energy losses during turnoff	V_S = 13.5 V, R_L = 2 Ω, 1 ms pulse - VOUT from VS to 0 Slew Rate Setting (SLRT_CHx) = 11		0.37		mJ
		V_S = 13.5 V, R_L = 2 Ω, 1 ms pulse - VOUT from VS to 0 Slew Rate Setting (SLRT_CHx) = 10		0.48		mJ
		V_S = 13.5 V, R_L = 2 Ω, 1 ms pulse - VOUT from VS to 0 Slew Rate Setting (SLRT_CHx) = 01		0.68		mJ
		V_S = 13.5 V, R_L = 2 Ω, 1 ms pulse - VOUT from VS to 0 Slew Rate Setting (SLRT_CHx) = 00		0.9		mJ

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7 Parameter Measurement Information

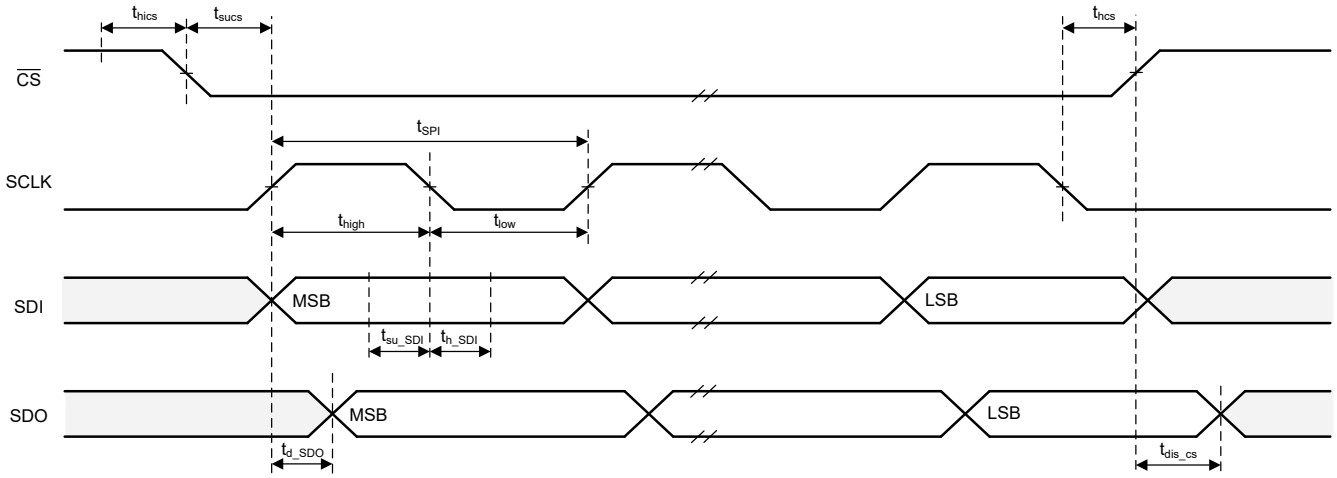

図 7-1. SPI Timing Characteristics Definitions

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8 Detailed Description

8.1 Overview

The TPS2HCS10-Q1 device is a dual-channel smart high-side switch intended for use with 12-V automotive batteries. The TPS2HCS10-Q1 device integrates SPI control and configuration as well digital readout with an ADC of key device and load diagnostics. The device incorporates all of the specific features needed for a power distribution switch as well as the traditional protective and diganostic functions seen in high side switches for actuator drive applications.

Diagnostics features include a digital current, output voltage and FET temperature sense output that can be read over the SPI serial interface. The high-accuracy load current sense allows for diagnostics of complex loads. The output voltage sense and FET temperature sense fearures in the device enables diagnosis of the switch and load failures.

This device includes protection through thermal shutdown, overcurrent protection, transient withstand, and reverse battery operation. In addition, the device also includes an SPI-configurable wire-harness protection function through a defined fuse or tme-current curve. The protection works in conjunction with an immediate switch-off overcurrent protection with an SPI-configurable threshold to fully protect against overload and short circuit faults.

The TPS2HCS10-Q1device also integrates a low quiescent current mode where the device can provide currents in the 100s of mA range while consuming only micro-amps of current. The device automatically switches to the high-current mode on an increase in load current and provide a wake signal to the MCU. Further, the device includes a capacitive charging mode that reduces the peak current load on the supply. Together, the two features support power distribution switch to off-board ECU applications.

For more details on the diagnosis, power distribution and protection features, refer to the *Feature Description* and *Application Information* sections of the document.

The TPS2HCS10-Q1 is one device in a family of TI high side switches. For each device, the part number indicates elements of the device behavior. 図 8-1 gives an example of the device nomenclature.

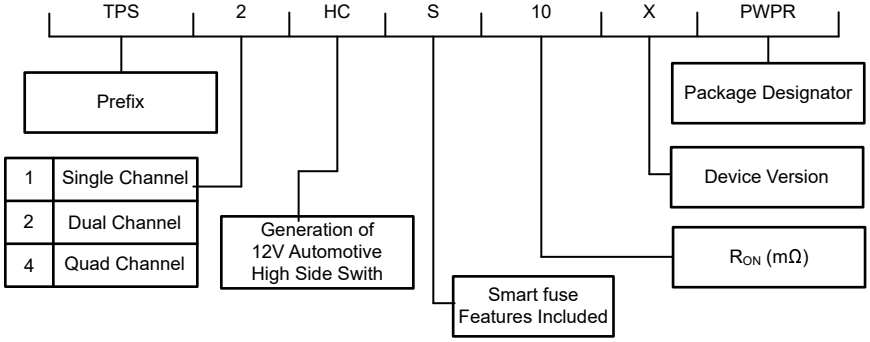
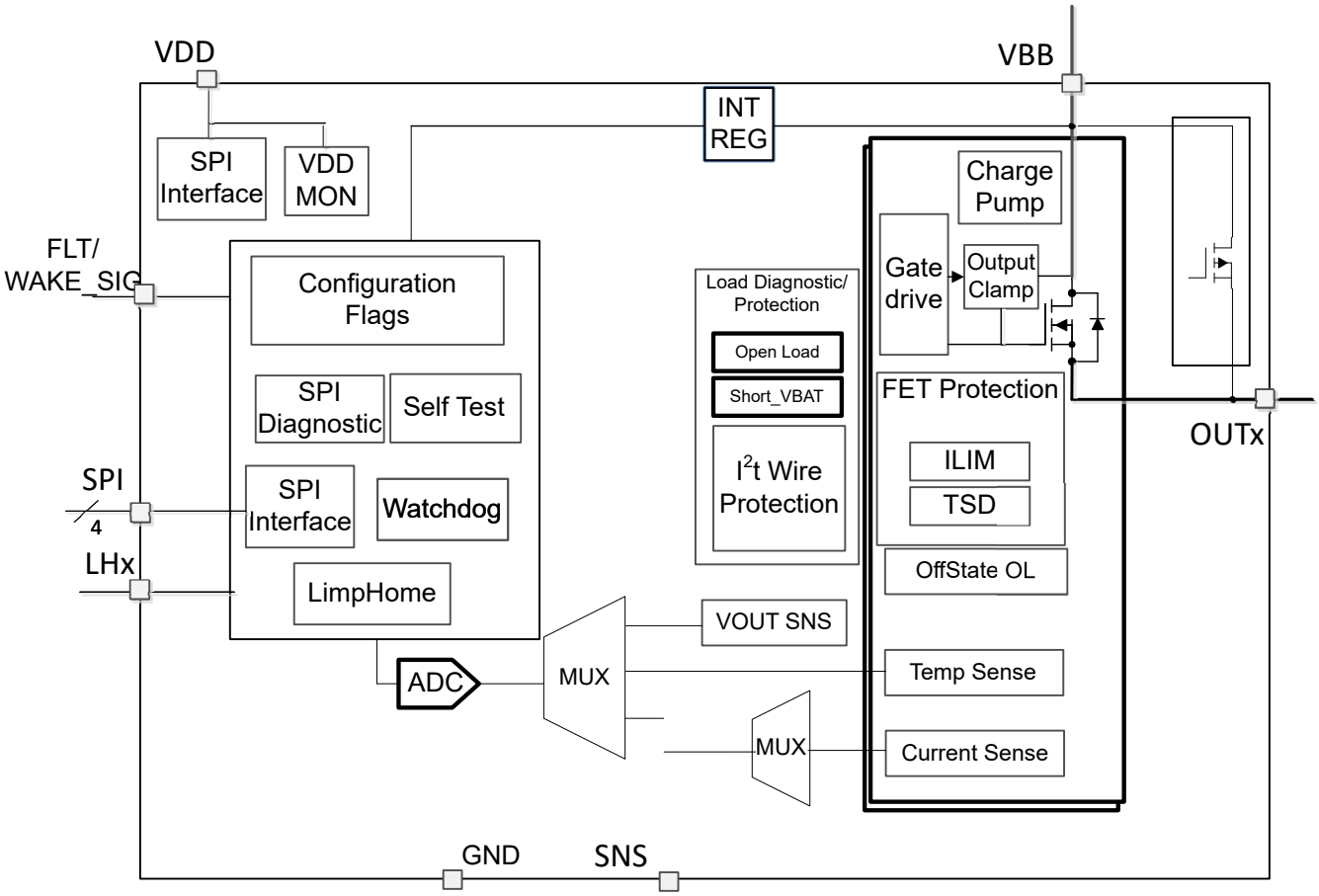


図 8-1. Naming Convention

8.2 Functional Block Diagram

The functional block diagram shown below.



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8.3 Feature Description

8.3.1 Protection Mechanisms

The TPS2HCS10-Q1device is designed to operate in the automotive environment. The protection mechanisms allow the device to be robust against many system-level events such as load dump, reverse battery, short-to-ground, overload and more.

There are three protection features which, if triggered, will cause the switch to automatically disable:

- Thermal Shutdown
- Overcurrent protection
- Fuse-like protection with a programmable time-current curve

When any of these protections are triggered, the affected channel will be turned off. While one of the switches is in fault turn-off, the fault indication will be available on the $\overline{FLT}$ pin (see the *Diagnostic Mechanisms* section of the data sheet for more details) and the faulted channel and the type of fault can be read back from the diagnostics registers over the SPI interface.

The ouput is no longer held off (FET and channel can be re-enabled) and the fault indication is reset when all of the below conditions are met:

- Programmed t_{RETRY} for the particular protection mode has expired or if set in the latch mode, unlatched through appropriate SPI writes.
- All faults are cleared (thermal shutdown, overcurrent protection, fuse protection).

8.3.1.1 Programmable Fuse Protection

The device includes a programmable fuse protection, that is based on a defined time-current curve and is commonly referred to as I2t protection in melting fuse data sheets. The intent is to match the switch turnoff behavior of a melting fuse. There are two parameters that can be configured (for each channel) in the I2T_CONFIG_CH1 and I2T_CONFIG_CH2 registers - that sets the time-current curve. One, the nomimal current (NOM_CUR_CHx), is the current below which the device can supply current indefinitely without turn-off. This is roughly equivalent to the fuse current rating of the melting fuses. The second parameter, I2T_TRIP_CHx, is the integral energy value above which the switch is turned off. Other parameters that define the region are (1) the maximum current that is measurable (ISWCL_CHx) that is determined by the current sense ratio (KSNS) of the device and the resistor chosen on the sense pin and (2) the SWCL_DLY_TMR_CHx that sets the time after which the channel shutdown when the current exceeds ISWCL_CHx. The channel remains off for a period set by TCLDN_CHx bits before retrying. The device can be configured to latch-off (retry only on MCU re-enable of the channel) by setting the two-bit TCLDN_CHx to 00.

The operational region for the fuse-based shutdown is shown in the 図 8-2 below. Exemplary values for the current values that bound the operational region is included.

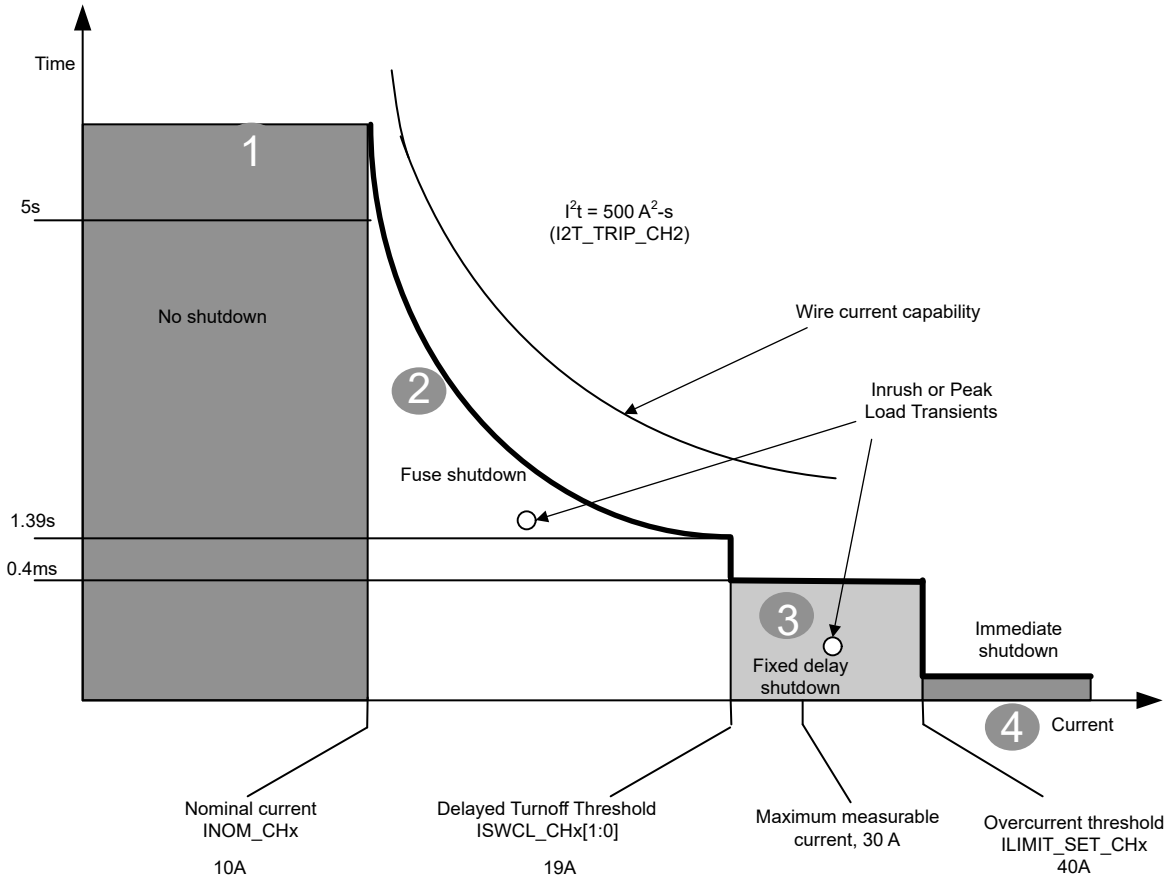

図 8-2. Current Operational Region of Fuse Based Switchoff

8.3.1.2 Thermal Shutdown

The TPS2HCS10-Q1 includes a temperature sensor on the power FET and also within the controller portion of the device. There are two cases that the device will consider to be a thermal shutdown fault:

- $T_{J,FET} > T_{ABS}$
- $(T_{J,FET} - T_{J,controller}) > T_{REL}$

After the fault is detected, the switch will turn off. If $T_{J,FET}$ exceeds T_{ABS}, the fault is cleared when the switch temperature decreases by the hysteresis value, T_{HYS}. If instead, the T_{REL} threshold is exceeded, the fault is cleared after T_{RETRY} passes.

8.3.1.3 Overcurrent Protection And Capacitive Load Charging

The device features overcurrent protection with an adjustable protection threshold programmed in the ILIM_CONFIG_CHx register. Additional programmability is introduced to account for capacitive loads and motor or lamp loads with a high inrush current. The type of load can be specified as capacitive or not using the CAP_CHRG_CHx bits in the ILIM_CONFIG_CHx register. A value other than 00 indicates capacitive load and the overcurrent protection as well as capacitive load charging behavior is defined for the time defined by the INRUSH_DURATION_CHx bits in the ILIM_CONFIG_CHx register. In these modes, the current is limited using the cap charging rate that is programmed using the ILIM_CONFIG_CHx register CAP_CHRG_DVDT [7:4] bits. A CAP_CHRG_CHx setting of 00 is used for a non-capacitive loads and here the overcurrent protection threshold is set using INRUSH_LIMIT_CHx for the time defined by the INRUSH_DURATION_CHx bits. Unlike the capacitive charging modes, the current is not limited but the channel is turned off immediately in case the threshold current is exceeded. In either type of load, the overcurrent protection is immediate turn-off once past the inrush duration phase. The normal load current behavior is shown in the 図 8-4 for the capacitive loads and in the 図 8-3 for the inductive or resistive loads (like heaters and motors).

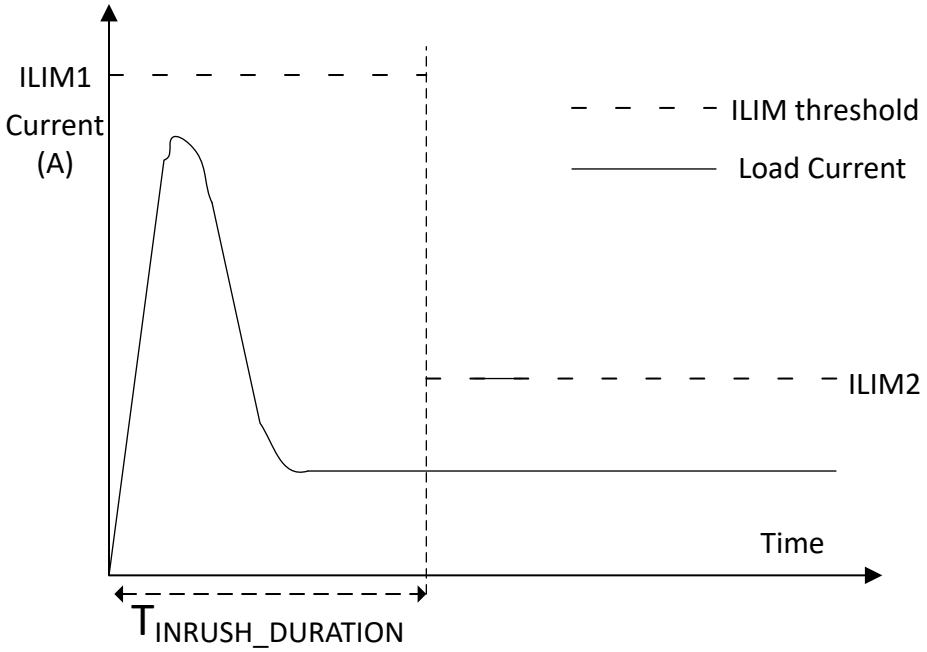

図 8-3. Normal load current on channel enable into resistive or inductive load and overcurrent thresholds (CAP_CHRG = 00)

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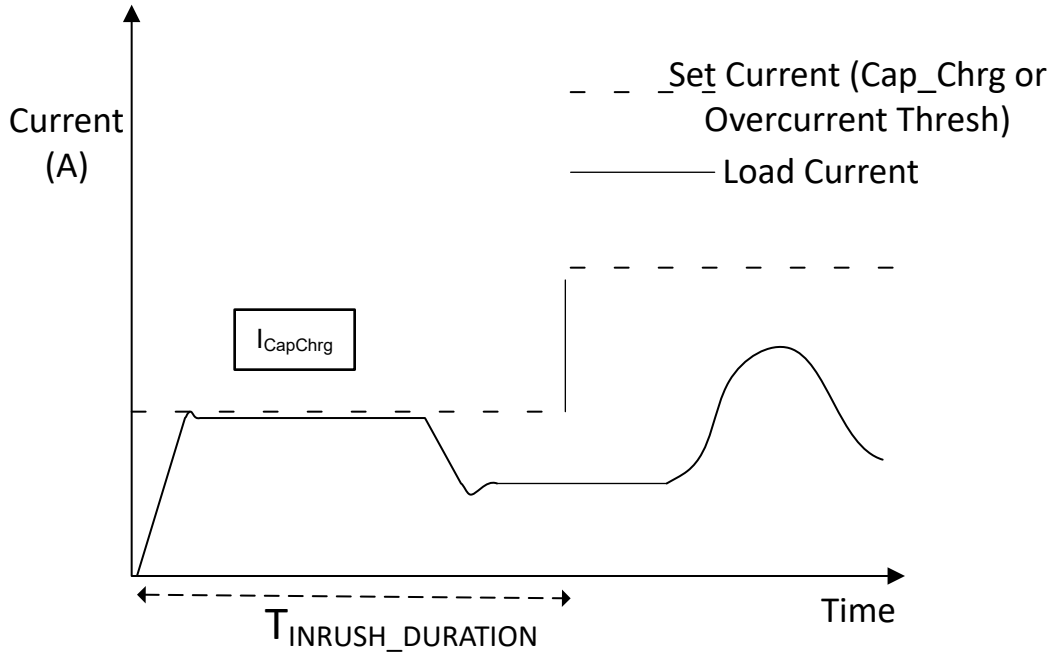

図 8-4. Normal load current behavior on channel enable into a capacitive load and overcurrent thresholds

An overcurrent protection event occurs when I_{OUTx} exceeds the programmed threshold level, I_{CL}. When I_{OUT} reaches the current limit threshold, ICL, the channel is immediately turned off. Please note that the current may peak at a higher value (I_{CL_pk}) than the programmed overcurrent threshold (I_{CL}). This is due to the limitation of the speed of the over-current protection response.

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図 8-5 shows the immediate overcurrent protection switch off behavior. The switch will retry after the fault is cleared and t_{RETRY} has expired. When the switch retries after a shutdown event, the fault indication will remain until V_{OUT} has risen to V_{BB} – 1.8 V. Once V_{OUT} has risen, the fault indication at the pin is reset and current sensing is available. If there is a short-to-ground and V_{OUT} is not able to rise, the fault indication will remain indefinitely.

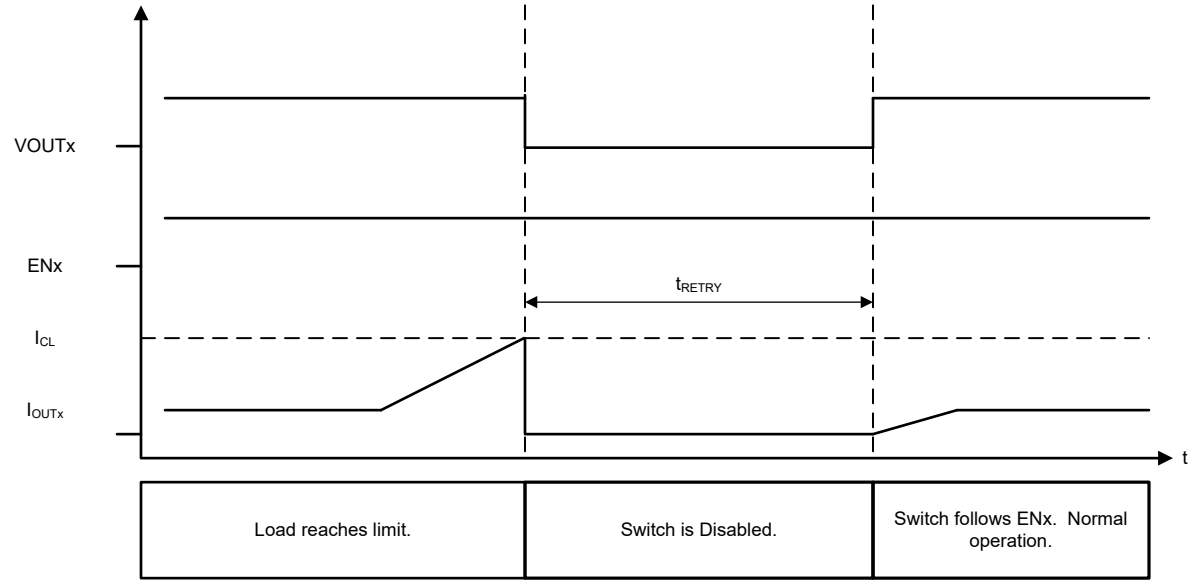

図 8-5. Overcurrent Protection Response

8.3.1.4 Reverse Battery

In the reverse battery condition, the switch will automatically be enabled regardless of the state of the output (set by the SW_STATE register) to prevent excess power dissipation inside the MOSFET body diode. In many applications (for example, resistive loads), the full load current may be present during reverse battery. In order to activate the automatic switch on feature, the DI pin must have a path to ground from either from the MCU or it needs to be tied to ground through R_{PROT} if unused.

There are two options for blocking reverse current in the system. The first option is to place a blocking device (FET or diode) in series with the battery supply, blocking all current paths. The second option is to place a blocking diode in series with the GND node of the high-side switch. This method will protect the controller portion of the switch (path 2), but it will not prevent current from flowing through the load (path 3). The diode used for the second option may be shared amongst multiple high-side switches.

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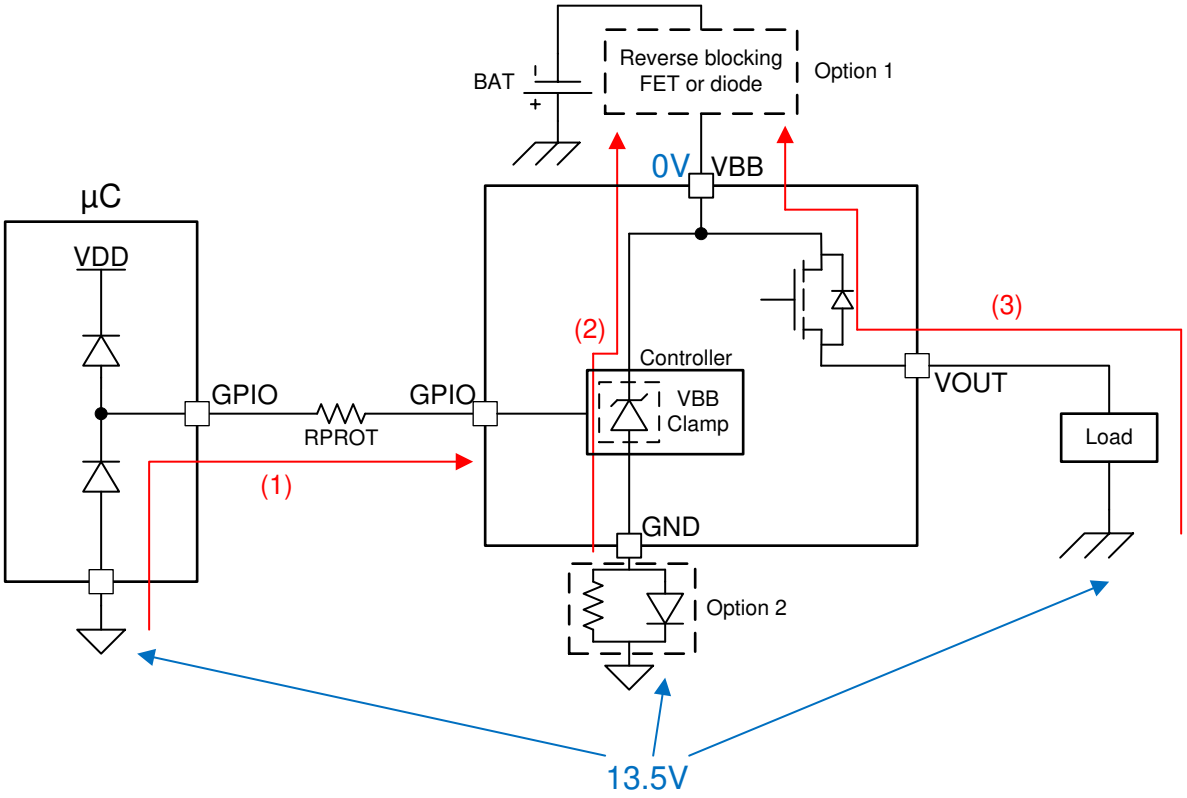


図 8-6. Current Path During Reverse Battery

For more information on reverse battery protection, refer to TI's *Reverse Battery Protection for High Side Switches* application note.

8.3.2 Diagnostic Mechanisms

8.3.2.1 VOUT Short-to-Battery and Open-Load

The TPS2HCS10-Q1 is capable of detecting short-to-battery and open-load events regardless of whether the channel output is turned on or off, however the two conditions use different methods.

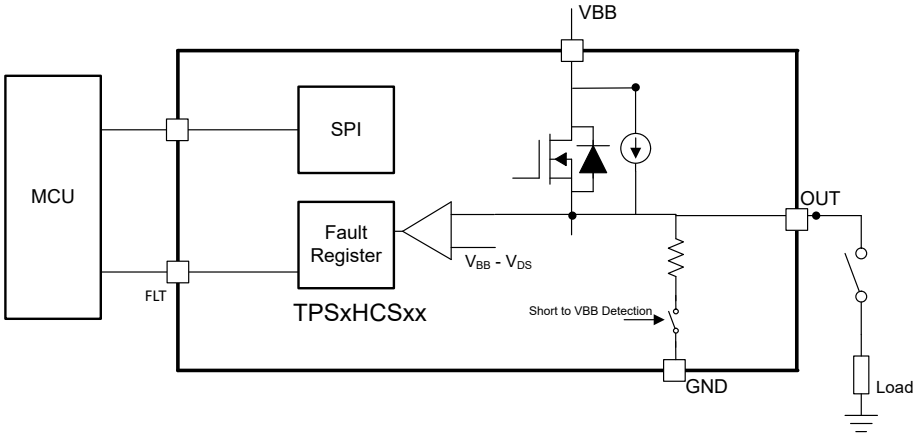
8.3.2.1.1 Detection With Channel Output (FET) Enabled

When the channel output is enabled and the FET is on, the VOUT short-to-battery and open-load conditions can be detected by the current sense feature. In both cases, the load current as measured using the current sense circuit and the ADC (available in the ADC_RESULT_CHx_I register, CH1 shown as example) as below the expected value. The current sense accuracy can be increased at low current levels by changing the current sense ratio from a nominal value of 5000 to a lower value of 1200. This is accomplished by setting the OL_ON_EN_CHx bit to 1 in the DIAG_CONFIG_CHx register (CH1 shown for example). However, the load current needs to be confirmed to be below 100 mA for this bit to take effect. In addition, the voltage input to the ADC can be scaled by a factor of 8 by setting the ISNS_SCALE_CHx bit in the same DIAG_CONFIG_CHx register (CH1 shown for example). This enables the ADC to measure the low load current with better resolution.

8.3.2.1.2 Detection With Channel Output Disabled

While the channel output is disabled (FET is off), and if the OL_OFF_EN_CHx bit in the DIAG_CONFIG_CHx register (CH1 shown as example) is set high, an internal comparator will detect the condition of V_{OUT}. The detection circuit is shown in 図 8-7. If the load is disconnected (open load condition) or there is a short to battery the V_{OUT} voltage will be higher than the open load threshold ($V_{OL,off}$) and a fault is indicated on the $\overline{FLT}$ pin unless masked in the FAULT_MASK register. The faulted channel can be determined by reading the FLT_STAT_CHx (CH1 shown as example) register with the OL_OFF_CHx bit set if there is a open load on that

channel. An internal pull-up current source of programmable value (through configuration bits OL_PU_STR in the DIAG_CONFIG_CHx register) is used, so no external component is required if an open load must be detected even with some on-board load and there is significant leakage or other current draw even when the load is disconnected. A pull-up resistor and switch can be added externally to set the V_{OUT} voltage above the $V_{OL,off}$ during open load conditions, if the internal pull-up is not sufficient.



This figure assumes that the device ground and the load ground are at the same potential. In a real system, there may be a ground shift voltage of the order of 1 V.

図 8-7. Short to Battery and Open Load Detection

While the switch is disabled and OL_OFF_EN_CHx bit in the DIAG_CONFIG_CHx is set high, the fault indication mechanism will continuously represent the present status. For example, if V_{OUT} decreases from greater than V_{OL} to less than V_{OL}, the fault indication is reset.

Further, to distinguish between an open load and short-to-battery condition, a second diagnostic can be enabled (in the off-state) by setting the SVBB_EN_CHx bit in the DIAG_CONFIG_CHx register (after the device detect either an open load or short-to-battery). The device then enables a pulldown on the output. If the short-to-battery condition exists, V_{OUT} voltage will remain higher than the open load threshold ($V_{OL,off}$) the the SHRT_VBB_CHx bit will be set high.

8.3.2.2 Digital Current Sense Output

The current sense circuit provide a current output that is proportional to the load current and this current will be sourced into an external resistor to create a voltage that is proportional to the load current. This voltage may be measured by either an external ADC or by the internal ADC. To ensure accurate sensing measurement, the sensing resistor should be connected to the IC GND pin if using the internal ADC. On the other hand, if using the MCU ADC, then the sensing resistor should be connected to the same ground potential as the microcontroller ADC.

The 10-bit digital current sense output can be read from the ADC_RESULT_CHx_I (H2 shown as example) register. The ISNS_RDY_CHx bit is set if the ADC conversion result is updated in the register from the last time the register was read.

8.3.2.2.1 R_{SNS} Value and Accuracy / Resolution of Current Measurement

The following factors should be considered when selecting the R_{SNS} value:

- Current sense ratio (K_{SNS})
- Largest and smallest diagnosable load current required for application operation
- Full-scale voltage of the ADC
- Tolerance of the resistor used

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At low current levels, the KSNS factor can be scaled up by a factor of around 4.17 using the configuration bit, OL_ON_EN_CHx, in the DIAG_CONFIG_CHx register to improve the accuracy of current measurement. In order to further improve the resolution at low current levels, the device offers the configuration bit ISNS_SCALE_CHx in the DIAG_CONFIG_CHx register that multiplies the input voltage to the ADC by a factor of 8. This enables the ADC to measure currents even of the order of 10 mA with sufficient bit resolution.

8.3.2.2.1.1 High Accuracy Load Current Sense

In many automotive ECUs, the high-side switch is need to provide diagnostic information about the downstream load current. With more complex loads, high accuracy sensing is required. A few examples follow:

- **LED lighting**: In many architectures, the body control module (BCM) must be compatible with both incandescent bulbs and also LED modules. The inacndescent lamp load may be relatively simple to diagnose. However, the LED module will consume less current and also can include multiple LED strings in parallel. The same BCM is used in both cases, so the high-side switch can accurately diagnose both load types.
- **Solenoid protection**: Often solenoids are precisely controlled by low-side switches. However, in a fault event, the low-side switch cannot disconnect the solenoid from the power supply. A high-side switch can be used to continuously monitor several solenoids. If the system current becomes higher than expected, the high-side switch can disable the module.

8.3.2.2.1.2 SNS Output Filter

To achieve the most accurate current sense value, it is recommended to filter the SNS output. There are two methods of filtering:

- Low-Pass RC filter between the SNS pin and the ADC input. This filter is illustrated in 図 9-1 with typical values for the resistor and capacitor. The designer should select a C_{SNS} capacitor value based on system requirements. A larger value will provide improved filtering but a smaller value will allow for faster transient response.
- The ADC and microcontroller can also be used for filtering. It is recommended that the ADC collects several measurements of the current sense output. The median value of this data set should be considered as the most accurate result. By performing this median calculation, the microcontroller can filter out any noise or outlier data.

8.3.2.3 Output Voltage and FET Temperature Sensing

The following voltage and temperature sense output are available as 10-bit digital outputs after ADC conversion.

- Channel output VOUTx voltage sensing available from ADC_RESULT_CHx_V register
- Channel FET temperature sensing available from ADC_RESULT_CHx_T register
- Supply voltage input sense available from ADC_RESULT_VBB register

The channel output voltage sensing circuit and the ADC MUX is shown in 図 8-8. The feature removes the need for external components and reduces the MCU ADC channel use in order to monitor the output voltage for diagnostic purposes.

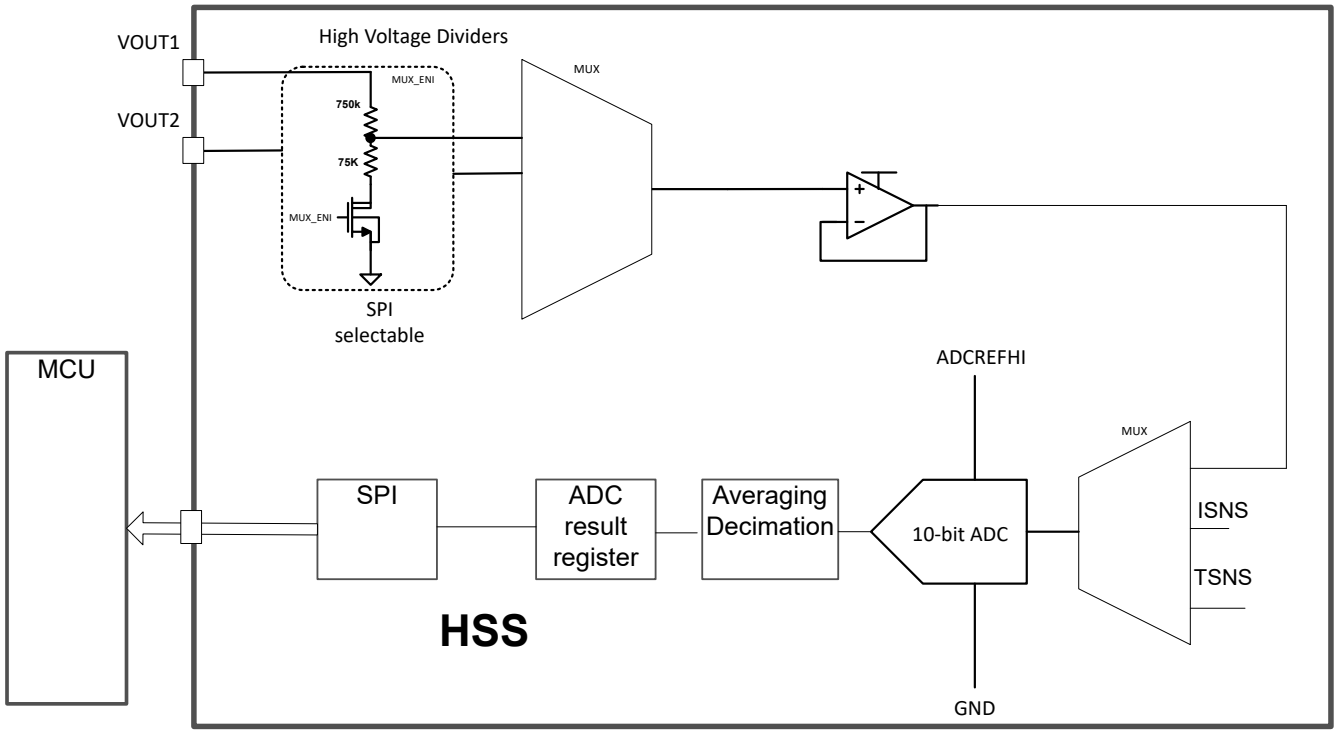

図 8-8. VOUT Voltage Sensing and ADC MUX

8.4 Device Functional Modes

8.4.1 State Diagram

The device has three main categories of states it can transition into and out of: low quiescent current, normal operation, and failsafe. Insdie of each of the categories are several states the device can be in. The state diagram for the device is shown in 図 8-9

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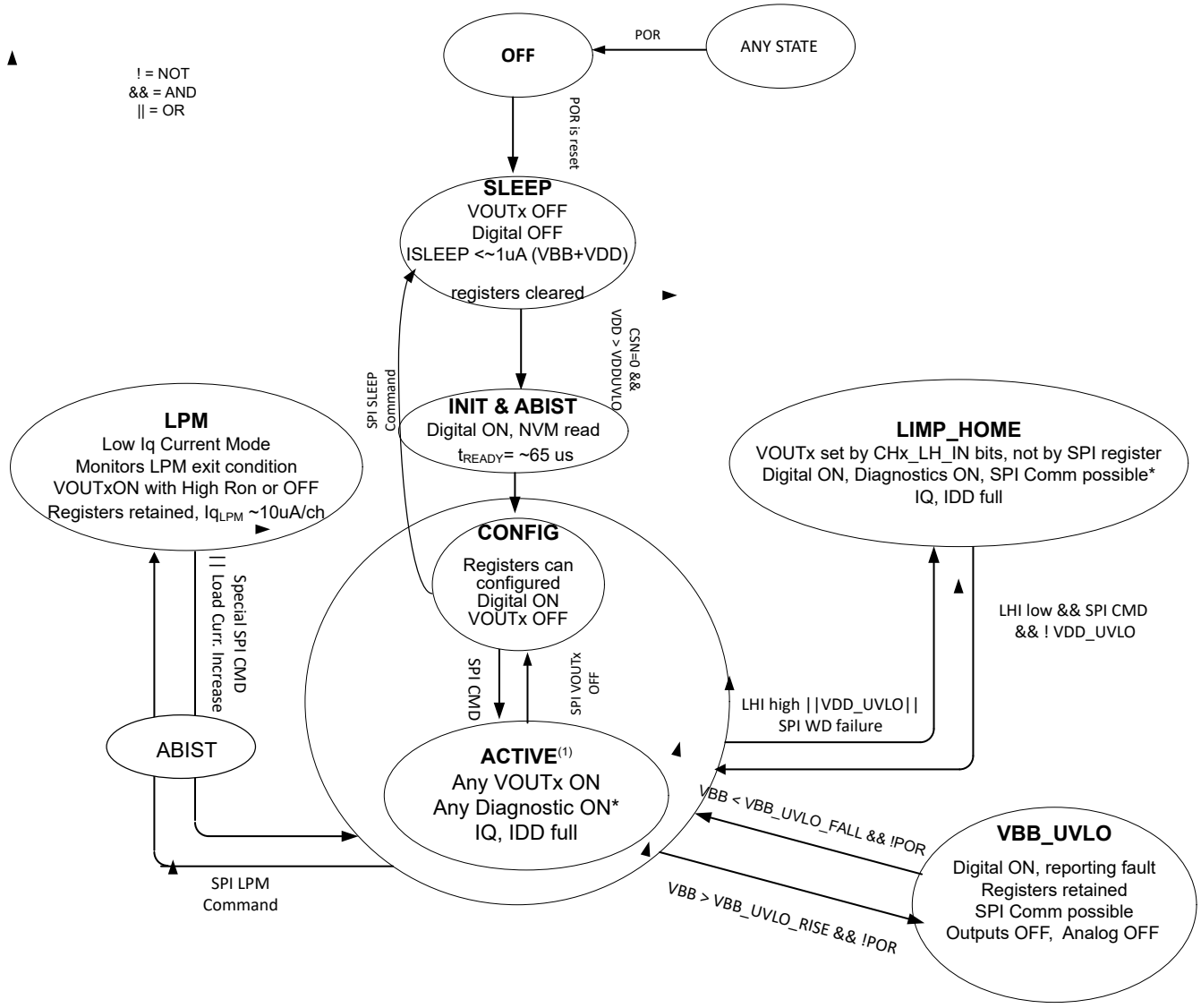

図 8-9. State Diagram

表 8-1. State Transition

Operating Mode	Entering Condition	Leaving Condition	Characteristics
Off (this is not an operating mode)	ANY STATE • On POR from loss of all supply	SLEEP • POR is RESET when supply input is available	Nothing powered
SLEEP	OFF • VBB > VBBPOR • ACTIVE – SLEEP SPI Command	CONFIG /ACTIVE through INIT & ABIST • $\overline{CS}$= 0 AND VDD > VDD_UVLOR A Dummy SPI command will wake the device from SLEEP	• VOUTx OFF • Digital OFF • Registers Lost • IVBB = IVBBSLEEP (~1's µA) • IVDD = IVDDSLEEP (~sub µA)

表 8-1. State Transition (続き)

Operating Mode	Entering Condition	Leaving Condition	Characteristics
CONFIG/ACTIVE	SLEEP through INIT & ABIST • $\overline{CS}$ = 0 AND • VDD > UVLOR LOW POWER MODE through ABIST • LPM Exit SPI OR • Load current increase LIMP HOME • VDD > UVLOR AND • "LH_STAT" = 1 AND • LHI pin is low	SLEEP • SPI SLEEP command LOW POWER MODE • LPM SPI Command LIMP HOME • VDD < UVLOF OR • SPI WD failure if set OR • LHI pin pulled HI	• All registers can be configured • VOUTx ON/OFF • On state diagnostics available – FLT reporting – OL on state – All ISNS, VSNS, TSNS • IVDD = Full IQ • IVBB = Full IQ
LOW POWER MODE (LPM)	ACTIVE • LPM SPI Command	ACTIVE through ABIST • LPM Exit SPI OR • Load current increase	• High RON • Digital mostly off • Register values held • IVDD = IDDLPM (~12 µA) • IVBB = IQLPM (~ 4 µA/ch)
VBB_UVLO	CONFIG/ACTIVE • VBB < UVLOF AND • !POR AND • VDD > UVLOR	CONFIG/ACTIVE • VBB > UVLOF AND • !POR AND • VDD > UVLOR	• VOUTx OFF • Digital ON • Register Values Kept • SPI communication and diagnostics not supported
LIMP HOME	CONFIG/ACTIVE • VDD < UVLOF OR • LHI pin HI OR • SPI WD failure, if set	CONFIG/ACTIVE • VDD > UVLOR AND • "LH_STAT" = 1 AND • LHI pin is low	• VOUTx set by LHI_IN or DIx • Digital ON • Register values kept, if initialized • SPI communication and diagnostics supported, if VDD high

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8.4.2 SLEEP

The TPS2HCS10-Q1 output channels are typically among a large number of channels in an ECU. The ECUs need to consume uAs of of current while the car is in park mode or key-off mode. The SLEEP mode is lowest current consumption mode of the IC with current consumption of the order of a uA per channel. In the key-off mode for the car, the TPS2HCS10-Q1 can be in either LPM mode when at least one channel has to supply a load ECU or in the SLEEP state where all the channels are OFF and the digital/ VDD circuits are all powered off. The SPI command as a write to the SLEEP register places the device in the SLEEP state. The VDD and VBB pins of the IC are expected to be powered in the SLEEP state.

In the SLEEP state the device is mostly powered off, so that the overall current consumption from VBAT of the ECU is minimized for a totality of the high-side switch channels. In this mode the a low nCS pin can wake up the device and place the device in the CONFIG state ready for SPI communication. However, SPI communication (actual data communication) can happen only after the t_{READY} period.

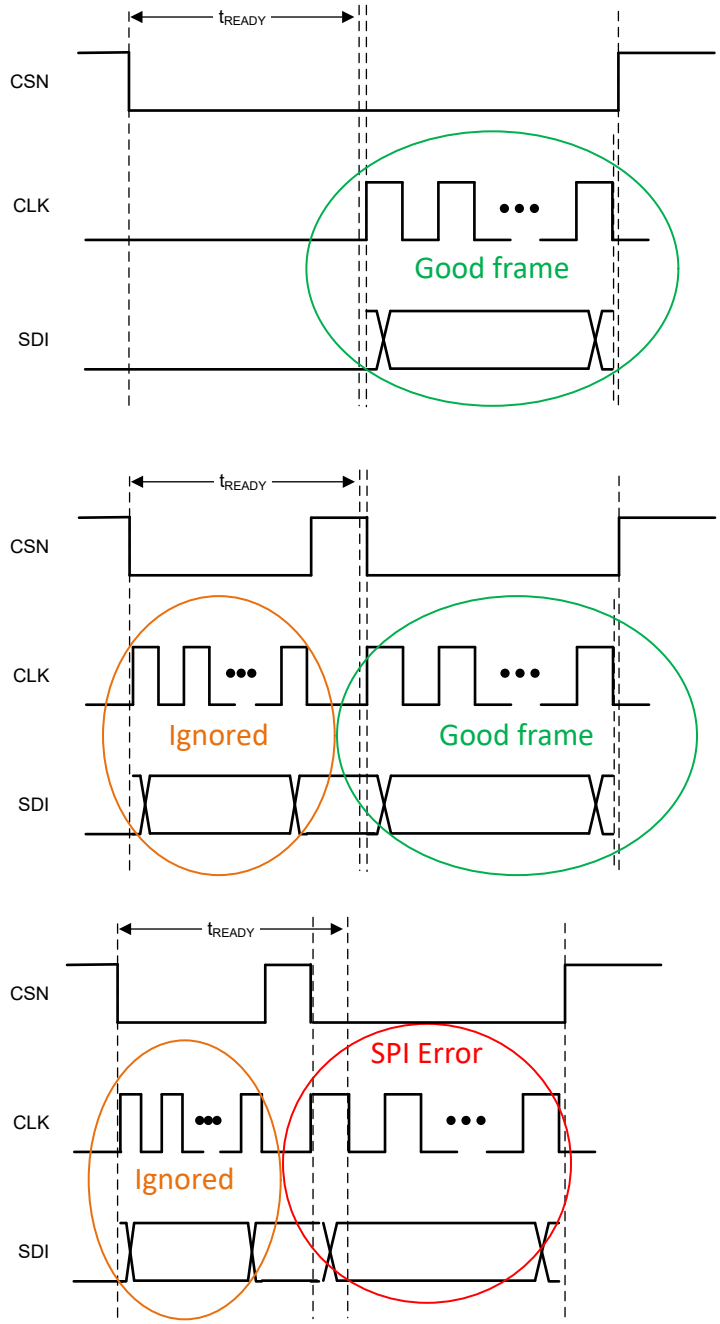

図 8-10. Startup Communication Timing

8.4.3 CONFIG/ACTIVE

The CONFIG/ACTIVE state is where the device stays during normal operation when the outputs are OFF (CONFIG) or ON (ACTIVE). The difference between the two is that in the CONFIG state (with the outputs OFF) all of the registers can be configured. In the ACTIVE state with the outputs ON, the parallel configuration of the channel cannot be changed (PARALLEL_12 bit in the DEVICE_CONFIG register). The configuration registers (especially ones needed for to successfully enable the channel) are expected to be written to before the outputs can be turned ON, when transitioning from the SLEEP state (and all the registers are lost). However, the configuration registers are retained while in the LPM state and so the device does not need to be reconfigured while tranisitioning from the LPM state to the ACTIVE state. The quiescent current for VBB, I_{QVBB}, and VDD,

I_{QVVD} is higher than in other states to support the load and device diagnostics. SPI communication and diagnostics check is fully supported in this state.

The device can be transitioned into the CONFIG state from the SLEEP state by the CSN pin going low (a dummy SPI command serves this purpose). The device completes the transition through all initializations and functional safety checks. The device transitions to and from the LIMP HOME state depending on the internal SPI watchdog monitor and the status of the LHI input pin. The device can transition into and out of the LPM state by a write to the LPM register.

8.4.4 Battery Supply Input (VBB) Under-voltage

The device includes a battery supply (VBB) under-voltage monitoring. Some of the internal reference and regulators and the output FETs are turned OFF when the VBB supply falls below the VBB_{UVLOF} threshold. When the input VBB supply is lost, the device relies on the low voltage supply input to keep the digital functions and registers alive. The SPI communication is also available as long as VDD input is supplied. The VBB UVLO error fault bits can be read over SPI from the CH_FLT_TYPE_FAULT_GLOBAL_TYPE register (VBB_UVLO bit). The following table indicates the device operation under a loss of supply condition.

表 8-2. Device operation under supply loss condition

	VDD < VDD_UVLO	VDD > VDD_UVLO
VBB < VBB_UVLO	• Channels are OFF • Registers are reset and digital core OFF • SPI communication not possible	• Channels are OFF • Registers are maintained and digital core is ON • SPI communication possible
VBB > VBB_UVLO	• Device is in LIMP HOME mode, channels set by LIMP_HOME mode programming • Registers are maintained and digital core is ON • SPI communication not possible	• Channels are controlled by SPI register writes • Registers are maintained and digital core is ON • SPI communication possible

The register information may be lost when both the VBB and VDD supplies are below the POR and UVLO conditions respectively. The device is able to indicate with a register read of the POR bit in the CH_FLT_TYPE_FAULT_GLOBAL_TYPE register that a reset of the digital has occurred. This will ensure that the SPI master can identify that the register contents are all lost and the configuration registers needs to be rewritten. It is recommended that the bit be read if any under-voltage fault is detected

8.4.5 LOW POWER MODE (LPM) State

This section discusses the implementation of the low current mode with a low quiescent current (Iq) feature in HCS-family devices.

Functionality

To supply ECUs that provide monitoring functions while the car is in the park mode (key-off mode), a low power mode (LPM) of operation is designed where the device consumes very low quiescent current even while the outputs are ON. The capabilities of the device are:

- Low quiescent current of the order of 10 uA from the battery input while delivering 100s of mAs of current with a maximum current of 800 mA per channel (limited only by wake threshold setting).
- Protection against short circuit at the output while in low power mode. In other words, if a short circuit were to occur with the output ON in low power mode, the device protects itself.
- Automatically respond to load current increase by transitioning to the ACTIVE state. The device provides a wake signal to the microcontroller (that is in sleep mode) to wake the system up through the $\overline{FLT}$ / WAKE_SIG pin.

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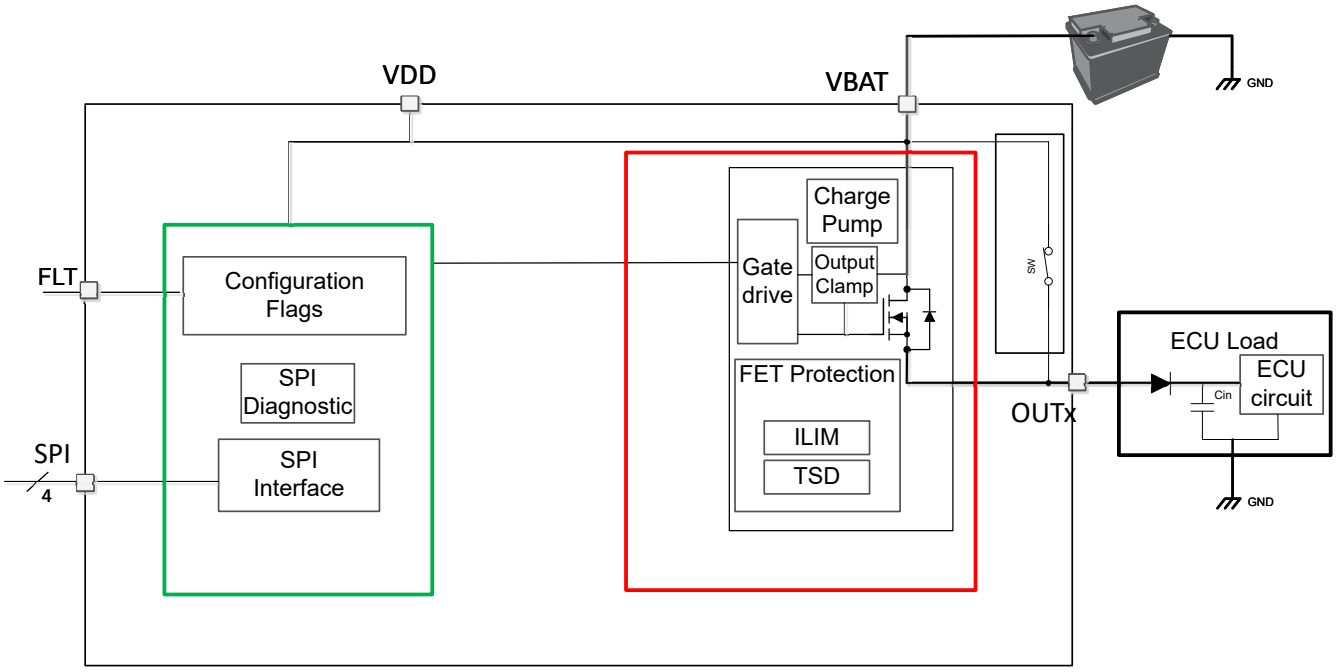

図 8-11. LPM Functional Block Diagram

Entry to and Exit from LPM

The device can be transitioned to the LPM state by writing to the LPM register. Any or both of the FETs can be ON in LPM, the set of channels to be ON is set by SW_STATE register (so needs to be written to before the write to the LPM register) and the command to go to LPM is received. Once in LPM the output state cannot be changed unless moved to ACTIVE state. The other requirement is that the switches that are enabled before the LPM mode bit is set, has to complete the inrush current phase before the transition to LPM is completed. All of the configuration registers are retained while the device is in the LPM state.

Please note that there is no output ON-to-OFF or OFF-to-ON tranistion possible during the ACTIVE to LPM transition. Only the channels that are already ON in ACTIVE state are allowed to be ON in LPM mode. The STATE has to be set to be ON in ACTIVE state and the channel must be fully ON before the LPM transition begins. Similarly, if the channel is OFF in the in LPM mode, that channel can be turned ON only in the ACTIVE state (after the transition to ACTIVE state is complete)

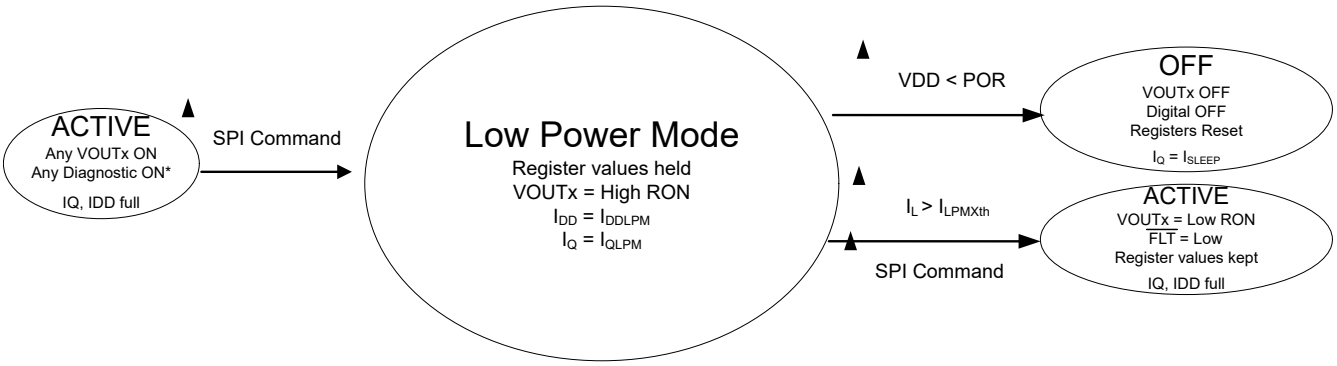

図 8-12. LPM Entry and Exit

Exiting from LPM

1. When the VDD supply is lost or the supply voltagae falls belows the POR threshold – the device transitions to OFF or SLEEP state where all register config is lost. The entry back to ACTIVE state is per the normal power up sequence including a wake signal from the MCU.
2. Special SPI command to write “0” to the LPM bit.
3. Current increase beyond the threshold set in the range from 200 mA to 800 mA using SPI configuration register LPM using register .

System Wake

The MCU or controller can write a special command to the LPM register setting the LPM bit to 0 to set the ICs in LPM state back to the ACTIVE state. When the digital core wakes up, the device interprets the command to go the ACTIVE state (if the special command is received). If the received command is not the SPI write to the LPM register, then the device stays in the LPM state. After the device is in the ACTIVE state – the MCU has to read to clear LPM bit to pull the $\overline{\text{FLT}}$ pin back up and clear any residual LPM condition.

Automatic Wake on Load Current Increase

The device takes the responsibility to wake the system and itself up when there is a load current increase beyond the programmed threshold. The threshold current (either ECU load current demand increase or an output short circuit) to activate the switch to the main MOSFET is in the range of 200 mA to 800 mA (programmable). The expectation is that the maximum current draw from the ECU while in low quiescent current mode (without the need to wake up) is lower than the programmed threshold. The additional load current demand and the transition to the active state is signaled to the MCU or the System Basis Chip (SBC) with a falling edge of the $\overline{\text{FLT}}$ or $\overline{\text{WAKE\_SIG}}$ (active low pull-up resistor to VDD) that can be used as an interrupt by the MCU or the SBC to wake up the system. The device can then be polled over SPI to see if the $\overline{\text{FLT}}$ or $\overline{\text{WAKE\_SIG}}$ pin transition was caused by the load ECU current demand or a short circuit. The device is in the ACTIVE state with full SPI diagnostic capability and the short circuit fault condition can be read back from the fault register. The device registers a FAULT and as over-current protection fault only if the overcurrent is confirmed in the ACTIVE state. After the device transitions to ACTIVE because of a load current increase, the LPM bit in the LPM register remains set to 1. To go to LPM state again, the LPM bit in the LPM register needs to be set to 0 and then 1 again.

The timing diagram of the device response to a load current increase to any of the output channels is shown in .

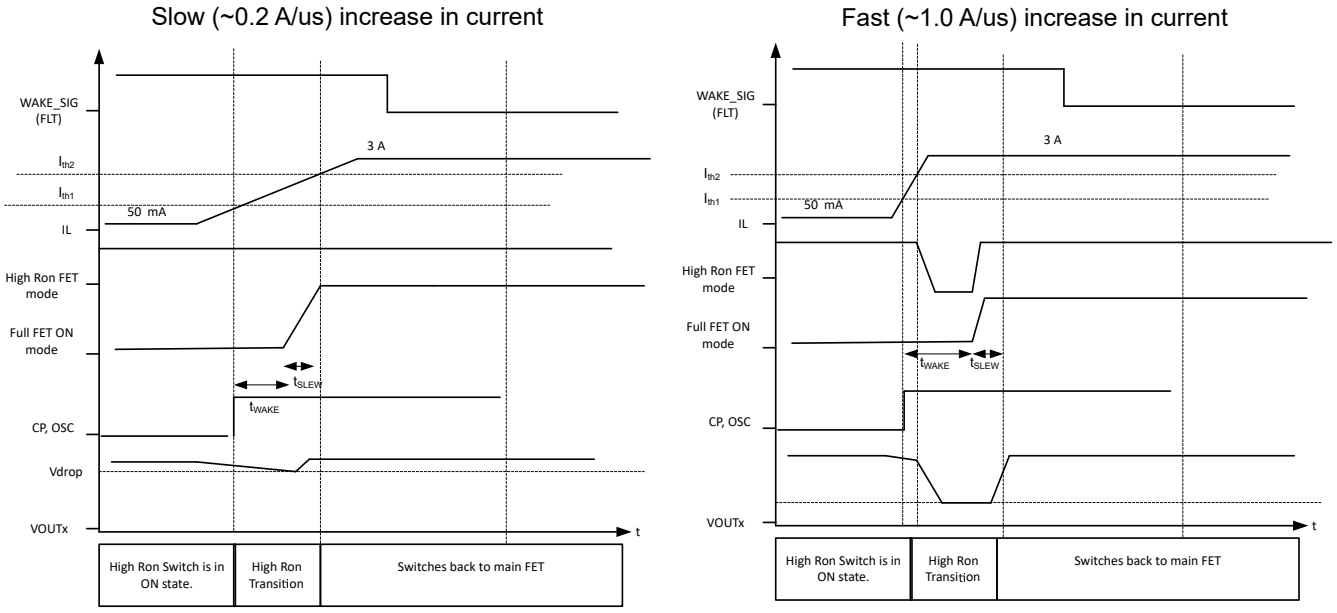

図 8-13. LPM to ACTIVE State Transition on Load Current Increase

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In the case of a slow increase in load current, the device detects a load current in excess of the programmed threshold for ACTIVE state transition. The channel output transitions smoothly to the low Ron FET state and achieve full load current capability with only a minor drop in the output voltage. However, in the case where the load current increases fast so that a second higher protection current threshold is reached before the FET is fully ON, the device switches off the channel. This is done to protect against potential short circuit at the output. The device then turns back on the channel in ACTIVE state and with the main FET ON. The output is then fully protected against a short and the channel either provides the full load current or stays in the overcurrent protection mode.

表 8-3. Wake Up Settings

LPM_EXIT_CURR_CHx in LPM register	Typ	Units
00 (default)	600	mA
01	800	mA
10	200	mA
11	400	mA

表 8-4. Low Power Mode Fault Conditions

Fault	Response
CHx that are commanded to go to LPM are in thermal shutdown or other FET turn-off (CH specific turn-off, not global fault)	The device transitions to LPM state with the affected channel OFF. In this case while in LPM, the channel is off even though the channel enable bit is set. We recommend that the all the faults are cleared before the command to transition to LPM state is sent. If the device exits the LPM to the active mode through SPI command, the channel is initially OFF and is enabled based on the programmed enable mode (cap charging or other).
Overtemperature	The FET temperature is not monitored – only current limit is enabled for protection and the assumption is that the device temperature stays low as long as the load current stays below the threshold for transition to active state.
VBB undervoltage	The outputs are turned off and recover as the supply is back ON.
Low VDD	If the VDD supply is lost the device transitions to the SLEEP state and all the register information is lost. The device needs to be configured again and transitioned to ACTIVE using the CSN (SPI) input.

8.4.6 LIMP HOME state

LIMP HOME state is intended to place the outputs in the desired safe state when there is a failure of SPI communication or VDD supply. When the ECU detects a system-level fault, the system controller raises the LHI pin high to signal to the device the need to go into the LIMP HOME state. Also, if the device detects a SPI watch dog timeout error and thus an SPI communication error, the device goes to the LIMP HOME state. In both cases, the output state is as specified in the CHx_LH_IN bits of the DEVICE_STAT register.

The register values are retained in the LIMP HOME state, which means that the appropriate overcurrent protection threshold values, duration and retry behavior are all set with the outputs corresponding to the state based on the CHx_LH_IN bits. Additionally, the "LIMPHOME_STAT " bit in the CH_FLT_TYPE_FAULT_GLOBAL_TYPE register is set which lets the MCU or controller know that the device is in the LIMP HOME state. The MCU cannot write to any of the registers until the device is out of the LIMP HOME state.

Transitioning out of the LIMP HOME state

Device transitions out of the LIMP HOME state when the LHI pin goes low and then SPI writes a 1 to the LIMPHOME_STAT bit in the CH_FLT_TYPE_FAULT_GLOBAL_TYPE register. The register settings are reatined while in LIMP HOME state and the device transitions back into normal operation in the ACTIVE state

LIMP HOME state exceptions

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- The device can receive an LHI signal during cap charging or inrush duration. If the desired state is ON, the device continues cap charging per programmed register values. If the desired state is OFF, then the channel is turned off.

DI Pin Functionality

The DI pin determines the output state when the device goes into LIMP HOME state, if the CHx_LH_IN bits are set to 00 in the DEVICE_STAT register.

- If DI is set HI, then CH1 = ON and CH2 = ON when in the LIMP HOME state
- If DI is set LOW, then CH1 = OFF and CH2 = OFF when in the LIMP HOME state

8.4.7 SPI Mode Operation

The TPS2HCS10-Q1 communicates with the host controller through a high-speed SPI serial interface. The interface has three logic inputs: clock (CLK), chip select ($\overline{CS}$), serial data in (SDI), and one data out (SDO). The SDO is tri-stated when the $\overline{CS}$ pin is high. The maximum SPI clock rate is 10MHz, but is limited in practice by the series protection resistor.

The device supports simple daisy chain SPI. This mode can be used with or without CRC.

The communication between the TPSHCS10 IC and the controller or MCU is through a SPI bus in a primary-secondary configuration. The external MCU is always an SPI primary device that sends command requests on the SDI pin of the TPS2HCS10-Q1 IC and receives device responses on the SDO pin of the IC. The TPS2HCS10-Q1 device is always an SPI secondary (or slave) device that receives command requests over the SDI line and sends responses (such as status and measured values) to the external MCU over the SDO line.

The TPS2HCS10-Q1 device can be connected to the primary MCU in the following formats:

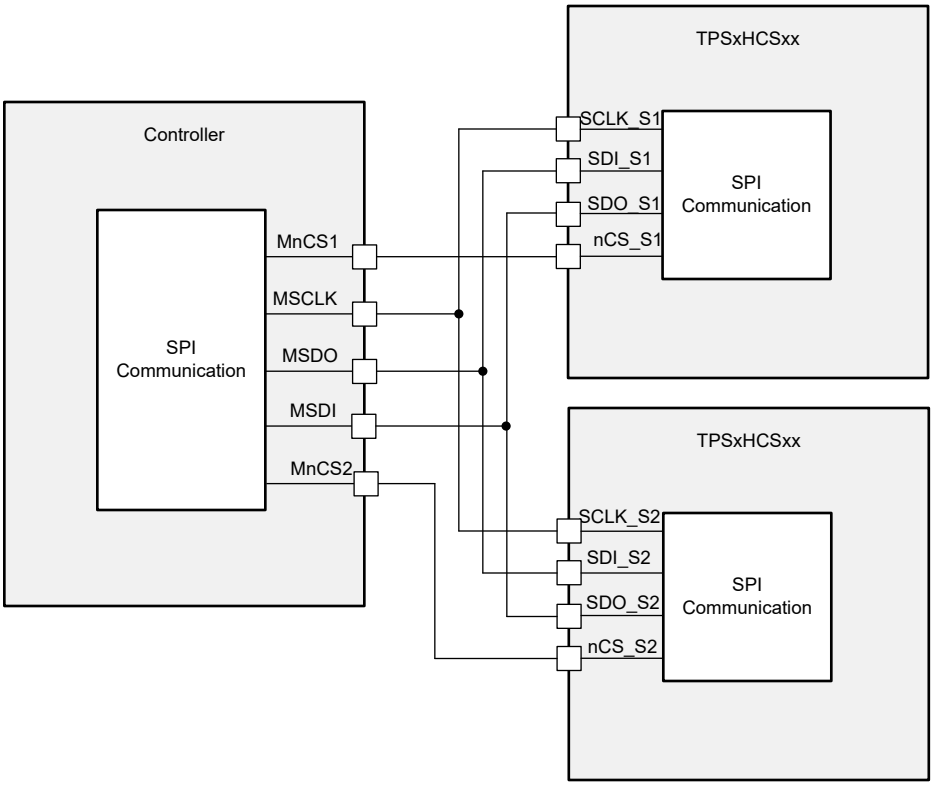

図 8-14. Independent Secondary Configuration (Separate nCS Signal)

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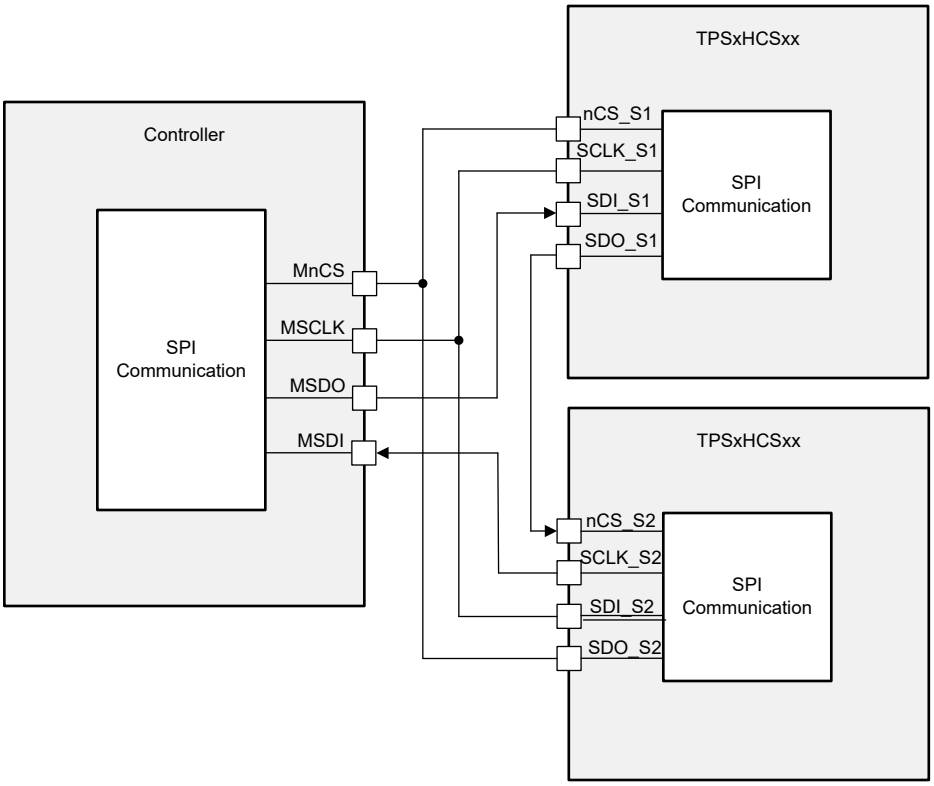

図 8-15. Daisy Chain Configuration

SPI interface

The SPI interface pin behavior is described in this section

Chip Select ($\overline{CS}$ or nCS)

The system microcontroller selects the TPS2HCS10-Q1 to receive communication using the $\overline{CS}$ pin. With the $\overline{CS}$ pin in a logic LOW state, command/configuration words may be sent to the TPS2HCS10-Q1 via the serial input (SDI) pin, and the device information can be retrieved by the microcontroller via the serial output (SDO) pin. The falling edge of the $\overline{CS}$ enables the SDO output and latches the content of the CH_FLT_TYPE/ FAULT_GLOBAL_TYPE register that will be sending out on SDO. The microcontroller may issue a READ command to retrieve information stored in the registers. Rising edge on the $\overline{CS}$ pin initiate following actions:

1. Addressed registers are updated if there is no SPI communication error and if it is an SPI write command.
2. Read clear register is cleared if a READ command to this register was issued during CS = LOW.

To avoid any corrupted data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic LOW state. A clean $\overline{CS}$ signal is needed to ensure no incomplete SPI words are sent to the device. This pin is internally pulled up to the VDD rail.

System Clock

The system clock (SCLK) pin clocks the internal shift register of the TPS2HCS10-Q1. The SDI data is latched into the input shift register on the falling edge of the SCLK signal. The SDO pin shifts the device stored information out on the rising edge of SCLK. The SDO data is available for the microcontroller to read on the falling edge of SCLK.

False clocking of the shift register must be avoided to ensure validity of data and it is essential the SCLK pin be in a logic LOW state whenever $\overline{CS}$ pin makes any transition. Therefore, it is recommended that the SCLK pin

gets pulled to a logic LOW state as long as the device is not accessed and the $\overline{CS}$ pin is at a logic HIGH state. When the $\overline{CS}$ is in a logic HIGH state, any signal on the SCLK and SDI pins will be ignored and the SDO pin remains as a high impedance output.

Serial Data In (SDI) and Serial Data Out (SDO)

The SDI pin is used for serial instruction data input. SDI information is latched into the input shift register on the falling edge of the SCLK when $\overline{CS}$ is low.

The SDO pin is the output from the internal shift register. This pin is internally pulled up to the VDD rail. SDO pin is HiZ when the $\overline{CS}$ pin is high. Each successive **rising** SCLK edge makes the next data bit available for the microcontroller to read on the **falling** edge of SCLK. SDO will go back to high-impedance when $\overline{CS}$ is high. $\overline{FLT}$

CRC Error Detection and Checking of clocks

Setting the CRC_EN bit high enables CRC error detection. A CRC-4-ITU-Normal Check Sequence (FCS) is then sent along with each serial transaction. The 4-bit CRC is based on the normal generator polynomial X4+X+1 with CRC starting value = 1111. When CRC is enabled, the TPS2HCS10-Q1 expects a check byte appended to the SDI program/configure data that it receives.

To program a complete word, exact bits of information (shown in following table) must be enter into the device. When CRC is disabled, the IC enables register write only if exactly bits have been clocked in. When CRC is enabled, the IC enables register write only if exactly bits have been clocked in with no CRC errors. In case the word length exceeds or does not meet the required length or there is CRC errors, the SPI_ERR bit in the CH_FLT_TYPE_FAULT_GLOBAL_TYPE is asserted to logic “1”,and the data received is considered invalid. Note the SPI_ERR bit is not flagged if SCLK is not present. The SPI_ERR will be sent back to SPI Main device on SDO during next chip access. **Note that clear on read applies only when there is no SPI error when the register is read.**

SPI Frame Format

The device uses a 24-bit frame width (when CRC is not used) with the format as shown in 図 8-16. Please note that the 16-bit wide "Data Out" in the SDO output is always for the previous SPI command frame (Read or Write).

		Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		R(0)	RA6	RA5	RA4	RA3	RA2	RA1	RA0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	SDI	Read	register address							Don't care								Don't care							
		Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Daisy =1 CRCEN=0		F15	F14	F13	F12	F11	F10	F9	F8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	SDO	CH_FLT_TYPE								Data out								Data out							

		Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		W(1)	RA6	RA5	RA4	RA3	RA2	RA1	RA0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	SDI	Write	register address							Data in								Data in							
		Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Daisy =1 CRCEN=0		F15	F14	F13	F12	F11	F10	F9	F8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	SDO	CH_FLT_TYPE								DataOut								DataOut							

図 8-16. 24-bit Read or Write, CRC_EN=0

8.5 TPS2HC10S Registers

表 8-5 lists the memory-mapped registers for the TPS2HC10S registers. All register offset addresses not listed in 表 8-5 should be considered as reserved locations and the register contents should not be modified.

表 8-5. TPS2HC10S Registers

Offset	Acronym	Register Name	Section
1h	CRC_CONFIG	Configure CRC	Go
2h	SLEEP	Sets to go into SLEEP sate from ACTIVE or STANDBY state	Go
3h	LPM	Sets to go in or out of Low power mode (LPM STATE)	Go
4h	CH_FLT_TYPE_FAULT_GLOBAL_TYPE	Faults for any channel and global faults	Go
5h	FAULT_MASK	Mask the reporting of the faults on the fault pin	Go
6h	ABIST_RESULT	ABIST Diagniostic result	Go
7h	SW_STATE	Turn on/off OUTx	Go
8h	DEVICE_SAF	Device BIST, LIMPHOME, and locking set by SPI	Go
9h	DEV_CONFIG	Device Configureable settings register	Go
Ah	ADC_CONFIG	ADC configuration - disable ADC conversions or ADC entirely	Go
Bh	ADC_RESULT_VBB	ADC conversion result VBB	Go
Dh	FLT_STAT_CH1	Status of the channels and channel faults	Go
Eh	PWM_CH1	Set all PWM configurations for channel 1	Go
Fh	ILIM_CONFIG_CH1	Set all current limit configuration for channel 1	Go
10h	DIAG_CONFIG_CH1	Configuration register for channel 1	Go
11h	ADC_RESULT_CH1_I	ADC conversion result load current sense CH1	Go
12h	ADC_RESULT_CH1_T	ADC conversion result TJ sense CH1	Go
13h	ADC_RESULT_CH1_V	ADC conversion result VOUT sense CH1	Go
14h	I2T_CONFIG_CH1	Set all I2T configuration bits	Go
15h	FLT_STAT_CH2	Status of the channels and channel faults	Go
16h	PWM_CH2	Set all PWM configurations for channel 2	Go
17h	ILIM_CONFIG_CH2	Set all current limit configuration for channel 2	Go
18h	DIAG_CONFIG_CH2	Configuration register for channel 2	Go
19h	ADC_RESULT_CH2_I	ADC conversion result load current sense CH2	Go
1Ah	ADC_RESULT_CH2_T	ADC conversion result TJ sense CH2	Go
1Bh	ADC_RESULT_CH2_V	ADC conversion result VOUT sense CH2	Go
1Ch	I2T_CONFIG_CH2	Set all I2T configuration bits	Go

Complex bit access types are encoded to fit into small table cells. 表 8-6 shows the codes that are used for access types in this section.

表 8-6. TPS2HC10S Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

表 8-6. TPS2HC10S Access Type Codes (続き)

Access Type	Code	Description
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WC	W C	Write to Clear
Reset or Default Value		
-n		Value after reset or the default value

8.5.1 CRC_CONFIG Register (Offset = 1h) [Reset = 0000h]

CRC_CONFIG is shown in 表 8-7.

Return to the Summary Table.

表 8-7. CRC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	CRC_EN	R/W	0h	Set this bit to 1 to enable CRC check of SPI command frame. 0h = No CRC check of SPI command frame 1h = CRC check of SPI command frame enabled

8.5.2 SLEEP Register (Offset = 2h) [Reset = 0000h]

SLEEP is shown in 表 8-8.

Return to the Summary Table.

表 8-8. SLEEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	SLEEP	R/W	0h	Setting this bit to 1 puts the device into SLEEP mode where everything shuts off

8.5.3 LPM Register (Offset = 3h) [Reset = 0000h]

LPM is shown in 表 8-9.

Return to the Summary Table.

表 8-9. LPM Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8-7	RESERVED	R	0h	Reserved
6-5	RESERVED	R	0h	Reserved
4-3	LPM_EXIT_CURR_CH2	R/W	0h	Set the threshold for exit from LPM mode due to load current increase - CH2. 0h = 600 mA 1h = 800 mA 2h = 200 mA 3h = 400 mA
2-1	LPM_EXIT_CURR_CH1	R/W	0h	Set the threshold for exit from LPM mode due to load current increase - CH1. 0h = 600 mA 1h = 800 mA 2h = 200 mA 3h = 400 mA
0	LPM	R/W	0h	Setting this bit to 1 puts the device into LPM mode with the channels enabled as per the device

8.5.4 CH_FLT_TYPE_FAULT_GLOBAL_TYPE Register (Offset = 4h) [Reset = 0347h]

CH_FLT_TYPE_FAULT_GLOBAL_TYPE is shown in 表 8-10.

Return to the Summary Table.

表 8-10. CH_FLT_TYPE_FAULT_GLOBAL_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2T_FLT	R	0h	The bit is set if there is a I2T fault due to overcurrent in any one of the channels. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition no longer exists.
14	LPM_FLT	R	0h	The bit is set if there is a fault during low power mode and the chip comes back to the active state. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition no longer exists
13	CHAN_TSD	R	0h	The bit is set if there is a thermal shutdown fault due to thermal overload in any one of the channels. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition no longer exists. 0h = no thermal shutdown fault in any of the channels 1h = thermal shutdown fault in one of the channels
12	ILIMIT_FLT	R	0h	The bit is set if there is a FET turn-off fault due to overcurrent in any one of the channels. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition no longer exists. 0h = no overcurrent fault in any of the channels 1h = overcurrent fault in one of the channels
11	SHRT_VBB_FLT	R	0h	The bit is set if there is a short to VBB supply in the off-state fault in any one of the channels. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition no longer exists 0h = no off-state short to VBB fault in any of the channels 1h = off-state short to VBB fault in one of the channels
10	OL_FLT	R	0h	The bit is set if either there is a wire break in the on or off-state fault in any one of the channels. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition no longer exists 0h = no on or off-state open laod detection fault in any of the channels 1h = on or off-state open load detection fault in one of the channels
9	SUPPLY_FLT	R	1h	The bit is set if either the VDD_UVLO or VBB_UV are faults occur. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition no longer exists. 0h = no UV fault in VDD, VINT or VBB 1h = UV fault in VDD, VINT or VBB
8	GLOBAL_ERR_WRN	R	1h	The bit is set if there is a global fault reported in the FLT_GLOBAL_TYPE register (Bits [7:0] : SPI error, watchdog error, VBB_UV, VBB_UV_WRN, VDD_UVLO, POR fault or LIMPHOME_STAT bit is set. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_GLOBAL_TYPE register is read and the fault condition no longer exists. 0h = no global fault 1h = One of the following errors have occurred: SPI error, watchdog error, VBB_UV, VBB_UV_WRN, VDD_UVLO, POR fault or LIMPHOME_STAT bit is set
7	LIMPHOME_STAT	W1C	0h	This bit is set high if the device is currently in the limp home mode.

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表 8-10. CH_FLT_TYPE_FAULT_GLOBAL_TYPE Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
6	POR	R/WC	1h	The bit is indicative of whether a power on reset has occurred. 0h = There is no power-on reset anytime after the last register read The register bit is cleared on read, so if read again and the bit is 0, means that no power-on reset has occurred since the read. 1h = A power-on reset has occurred since the last register read.
5	RESERVED	R	0h	Reserved
4	SPI_ERR	R/WC	0h	The bit is set if there is an SPI communication error either from format, clock or CRC errors.The fault bit is latched and cleared only after read and the error is removed. 0h = No SPI communication error fault 1h = SPI communication error either from format, clock or CRC has occurred
3	WD_ERR	R/WC	0h	The bit is set if the watchdog timer is enabled and there has not been an acceptable SPI command in the watchdog timeout window. The fault bit is latched and cleared only after read and the error is removed. 0h = No SPI interface watchdog error 1h = SPI watchdog timeout error has occurred
2	VDD_UVLO	R/WC	1h	The bit is set if VDD supply is below the UVLO threshold at any time. The fault bit is cleared if the GLOBAL_FAULT_TYPE register is read and the UVLO condition is removed 0h = No VDD UVLO fault 1h = VDD UVLO fault
1	VBB_UV_WRN	R/WC	1h	The bit is set if VBB supply is below the UV warning (UV_WRN) threshold at any time. The fault bit is cleared if the GLOBAL_FAULT_TYPE register is read and the UV condition is removed 0h = No VBB UV_WRN fault 1h = VBB UV_WRN fault
0	VBB_UVLO	R/WC	1h	The bit is set if VBB supply is below the UV threshold at any time. The fault bit is cleared if the GLOBAL_FAULT_TYPE register is read and the UV condition is removed 0h = No VBB UV fault 1h = VBB UV fault

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8.5.5 FAULT_MASK Register (Offset = 5h) [Reset = 0000h]

FAULT_MASK is shown in 表 8-11.

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表 8-11. FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6	MASK_ILIMIT	R/W	0h	The bit is set to mask the signaling overcurrent protection fault on the FLT pin 0h = Fault is signaled on the FLT pin on overcurrent FET turn-off occuring 1h = Overcurrent protection fault is not signaled (masked from) on the FLT pin
5	MASK_SHRT_VBB	R/W	0h	The bit is set to mask the signaling off-state Short to VBB fault on the FLT pin 0h = Short to VBB Fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = Short to VBB fault is not signaled (masked from) on the FLT pin
4	MASK_OL_OFF	R/W	0h	The bit is set to mask the signaling off-state open load fault on the FLT pin 0h = Off-state wire-break fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = Off-state wire-break fault is not signaled (masked from) on the FLT pin
3	MASK_OL_ON	R/W	0h	The bit is set to mask the signaling on-state open load fault on the FLT pin 0h = On-state wire-break fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = On-state wire-break fault is not signaled (masked from) on the FLT pin
2	MASK_SPI_ERR	R/W	0h	The bit is set to mask the SPI error (SPI_ERR) signaling in the FLT pin output and FAULT_TYPE_STAT register 0h = SPI error is signaled in FAULT_TYPE_STAT register and FLT pin 1h = FAULT_TYPE_STAT register and FLT pin not impacted by SPI error
1	MASK_WD_ERR	R/W	0h	The bit is set to mask the SPI watchdog error (WD_ERR) signaling in the FLT pin output and FAULT_TYPE_STAT register 0h = SPI watchdog error is signaled in FAULT_TYPE_STAT register and FLT pin 1h = FAULT_TYPE_STAT register and FLT pin not impacted by SPI watchdog error
0	MASK_VBB_UVLO	R/W	0h	The bit is set to mask the supply voltage VBB UVLO fault signaling on the FLT pin output. 0h = VBB UV fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = VBB UV fault is not signaled (masked from) on the FLT pin

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8.5.6 ABIST_RESULT Register (Offset = 6h) [Reset = 0000h]

ABIST_RESULT is shown in 表 8-12.

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表 8-12. ABIST_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	ADC_GOOD	R	0h	This says whether or not the ABIST for the ADC passed (not implemented in the present release) 0h = ABIST for ADC Passed 1h = ABIST for ADC Failed
2	ISNS_GOOD	R	0h	This says whether or not the ABIST for the ISNS passed (not implemented in the present release) 0h = ABIST for ISNSPassed 1h = ABIST for ISNS Failed
1	VBB_UVP_GOOD	R	0h	This says whether or not the ABIST for the VBB passed (not implemented in the present release) 0h = ABIST for VBB Passed 1h = ABIST for VBB Failed
0	BG_GOOD	R	0h	This says whether or not the ABIST for the Bandgap passed (not implemented in the present release) 0h = ABIST for BG Passed 1h = ABIST for BG Failed

8.5.7 SW_STATE Register (Offset = 7h) [Reset = 0000h]

SW_STATE is shown in 表 8-13.

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表 8-13. SW_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	CH2_ON	R/W	0h	Set this bit to 1 to turn on the FET and CH2 output ON 0h = CH2 Output set to OFF (FET is OFF). 1h = CH2 Output set to ON (FET is ON).
0	CH1_ON	R/W	0h	Set this bit to 1 to turn on the FET and CH1 output ON 0h = CH1 Output set to OFF (FET is OFF). 1h = CH1 Output set to ON (FET is ON).

8.5.8 DEVICE_SAF Register (Offset = 8h) [Reset = 0000h]

DEVICE_SAF is shown in 表 8-14.

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表 8-14. DEVICE_SAF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-11	RESERVED	R	0h	Reserved
10-9	RESERVED	R	0h	Reserved
8-7	CH2_LH_IN	R/W	0h	Decides what to do with the output for LH mode. Either on, off, keep or use associated DI pin 0h = DI control output when in LHM 1h = keep output as it enter LHM 2h = output will be off during LHM 3h = output will be on during LHM
6-5	CH1_LH_IN	R/W	0h	Decides what to do with the output for LH mode. Either on, off, keep or use associated DI pin 0h = DI control output when in LHM 1h = keep output as it enter LHM 2h = output will be off during LHM 3h = output will be on during LHM
4	ADC_ABIST_RUN	R/W	0h	Run the ABIST diaagnostics for the ADC good signal and update the DIAG_RESULT register with the result. Not available in current silicon, but will be in the production version. Not available with in I2T loop. Reset bit back to 0 after ABIST has been run 0h = ABIST not Running 1h = ABIST for ADC Running
3	ISNS_ABIST_RUN	R/W	0h	Run the ABIST diaagnostics for the ISNS good signal and update the DIAG_RESULT register with the result. Not available when in I2T loop. Reset bit back to 0 after ABIST has been run 0h = ABIST not Running 1h = ABIST for ISNS Running
2	RESERVED	R	0h	Reserved
1	BG_ABIST_RUN	R/W	0h	Run the ABIST diaagnostics for the Band Gap good signal and update the DIAG_RESULT register with the result. Reset bit back to 0 after ABIST has been run 0h = ABIST not Running 1h = ABIST for BG Running
0	ADC_EN	R/W	0h	Setting this bit to 1, enables the ADC function 0h = ADC function disabled 1h = ADC enabled

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8.5.9 DEV_CONFIG Register (Offset = 9h) [Reset = 0000h]

DEV_CONFIG is shown in 表 8-15.

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表 8-15. DEV_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6	PWM_SHIFT_DIS	R/W	0h	Set this bit to 1 to disable the PWM delay between channels. 0h = PWM rising edges delayed by 100 us on the first rising edge 1h = PWM delay (offset) is disabled so rising edges are aligned
5	RESERVED	R	0h	Reserved
4	PARALLEL_12	R/W	0h	Set this bit to 1 to signal that channels 1 and 2 (CH1 and CH2) are paralleled. Write to this bit is valid only when all SW_STATE Channel enable bits are 0 and not rewritten to 1 in the same frame. 0h = CH1 and CH2 are not paralleled together 1h = CH1 and CH2 are paralleled together
3	WD_EN	R/W	0h	The bit is set to enable the watchdog function. The watchdog is triggered if there is not a valid SPI command in the watchdog timeout window 0h = Watchdog is disabled 1h = Watchdog function is enabled
2-1	WD_TO	R/W	0h	Sets the timeout period for the SPI watchdog monitor. The watchdog timeout is triggered if there is not a valid SPI command in the watchdog timeout window 0h = Watchdog timeout 400 us 1h = Watchdog timeout is 400 ms 2h = Watchdog timeout is 800 ms 3h = Watchdog timeout is 1200 ms
0	FLT_LTCH_DIS	R/W	0h	Set this bit to 1 to not latch the fault bits in the register and cleared on read. 0h = Fault bits in FAULT_TYPE_STAT register latched and cleared only on read 1h = Fault bits in FAULT_TYPE_STAT register not latched, cleared when the fault disappears

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8.5.10 ADC_CONFIG Register (Offset = Ah) [Reset = 001Ah]

ADC_CONFIG is shown in 表 8-16.

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表 8-16. ADC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	ADC_VSNS_DIS	R/W	1h	Set this bit to 1 to disable VOUT sense functionality, exclude VOUT conversion in the ADC conversion sequence. 0h = VOUTSNS ADC functionality enabled, include VOUT_SNS ADC conversion in the sequence 1h = VOUTSNS ADC functionality is disabled
3	ADC_TSNS_DIS	R/W	1h	Set this bit to 1 to disable TEMP sense functionality, exclude TSNS conversion in the ADC conversion sequence. 0h = TSNS ADC functionality enabled, include TSNS ADC conversion in the sequence 1h = TSNS ADC functionality is disabled
2	ADC_ISNS_DIS	R/W	0h	Set this bit to 1 to disable ISNS functionality, exclude ISNS conversion in the ADC conversion sequence. 0h = ISNS ADC functionality enabled, include ISNS ADC conversion in the sequence 1h = ISNS ADC functionality is disabled
1	ADC_VBB_DIS	R/W	1h	Set this bit to 1 to disable VBB_SNS functionality, exclude supply voltage V_VBB conversion in the ADC conversion sequence. 0h = VBB_SNS ADC functionality is enabled, Include supply voltage V_VBB ADC conversion in the sequence 1h = VBB_SNS ADC functionality is disabled
0	RESERVED	R	0h	Reserved

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8.5.11 ADC_RESULT_VBB Register (Offset = Bh) [Reset = 0000h]

ADC_RESULT_VBB is shown in 表 8-17.

Return to the Summary Table.

表 8-17. ADC_RESULT_VBB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	VBB_RDY	R	0h	Making sure the ADC conversion is new from the last time this was read 0h = VBB ADC Value not updated 1h = New VBB ADC Value Ready
9-0	ADC_RESULT_VBB	R	0h	ADC result (10-bits) from the conversion of the VBB voltage

8.5.12 FLT_STAT_CH1 Register (Offset = Dh) [Reset = 0000h]

FLT_STAT_CH1 is shown in 表 8-18.

Return to the Summary Table.

表 8-18. FLT_STAT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	LATCH_STAT_CH1	R	0h	The bit is high if the channel has been latched off after a fault that shut down the channel. Clears when the channel is toggled back on 0h = CH1 is not latched off 1h = CH1 is currently latched off
10	FLT_CH1	R	0h	The bit is set if any type of real time fault (reverse current, thermal shutdown, open load (on/off-state) or short to supply) occurs in CH1 0h = No fault in CH1 1h = One or more fault has occurred in CH1
9	SW_STATE_STAT_CH1	R	0h	Current state of the channel no matter which mode the device is in as long as SPI is readable 0h = CH1 is OFF 1h = CH1 is ON
8	RESERVED	R	0h	Reserved
7	I2T_FLT_CH1	R	0h	The bit is set if there is a fault from I2T setting (overcurrent). Only can go high if I2T_EN is high and an associated fault occurs on that channel. Cleared when FLT_STAT_CH1 register is read and fault condition does not exist anymore 0h = no I2T fault or I2T is not enabled 1h = I2T fault has occurred on CH1
6	LPM_WAKE_CH1	R	0h	This bit is set if this channel was the reason the device came out of LPM regardless of why 0h = The device was not in LPM or this channel was not the one that cause the device to come out of LPM 1h = This channel was the reason the device came out of LPM
5	THERMAL_SD_CH1	R	0h	The bit is set if the thermal shutdown has occurred at any time in CH1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and channel temperature has fallen below the thermal shutdown reset threshold. 0h = No thermal shutdown fault in CH1 1h = Thermal shutdown has occurred in CH1
4	ILIMIT_CH1	R	0h	The bit is set if FET turn-off due to overcurrent has occurred at any time in CH1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and fault condition does not exist anymore. Disabled if I2T mode is enabled 0h = No overcurrent protection fault in CH1 1h = FET turn-off due to overcurrent fault has occurred in CH1
3	SHRT_VBB_CH1	R	0h	The bit is set if short to VBB has occurred at any time in CH1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and fault condition does not exist anymore. OL_SHRTVBB_DIFF_CH1 must have been enabled previously 0h = No Short to VBB fault in CH1 or short to VBB in OFF state not enabled 1h = Short to VBB Fault
2	OL_OFF_CH1	R	0h	The bit is set if the open load off state threshold been triggered. Only valid if OL_OFF_EN_CH1 is active. Device is pulled up with the threshold set by OL_PULLUP_STR 0h = No off state open load fault in CH1 or OL detection in OFF state not enabled 1h = Off State Open Load Fault

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表 8-18. FLT_STAT_CH1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	OL_ON_CH1	R	0h	Has the open load on state threshold been triggered? Only valid if OL_ON_EN_CH1 is active. Device is in high resistance mode 0h = No on state open load fault in CH1 or OL detection in OFF state not enabled 1h = On State Open Load Fault
0	THERMAL_WRN_CH1	R	0h	The bit is set if FET temperature is above the overtemperature warning threshold in CH1. The bit is cleared when over-temperature earning condition does not exist anymore. 0h = FET temperatire below over-temperature warning threshold in CH1 1h = FET temperatire above over-temperature warning threshold in CH1

8.5.13 PWM_CH1 Register (Offset = Eh) [Reset = 0000h]

PWM_CH1 is shown in 表 8-19.

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表 8-19. PWM_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-9	PWM_FREQ_CH1	R/W	0h	Set the PWM frequency 0h = 0.8 Hz 1h = 3.4 Hz 2h = 13.8 Hz 3h = 111 Hz 4h = 221 Hz 5h = 443 Hz 6h = 885 Hz 7h = 1770 Hz
8-1	PWM_DTY_CH1	R/W	0h	8 bit to set duty cycle for PWM operation of CH1. Each bit ~0.39% duty cycle, linearly up to 100% dutycycle.
0	PWM_EN_CH1	R/W	0h	Enable PWMing of the output if on cycle of PWM is >200us. If not return error in FLT_STAT_CH1 register. PWM mode cannot be enabled unless CAP_CHRGx [1:0] = 00 0h = Output follows SW_STATE behavior (ON/OFF) 1h = Output is PWMing according to duty cycle and frequency set if SW_STATE CH1 is ON

8.5.14 ILIM_CONFIG_CH1 Register (Offset = Fh) [Reset = 0088h]

ILIM_CONFIG_CH1 is shown in 表 8-20.

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表 8-20. ILIM_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	OCP_INRUSH_CH1	R/W	0h	When CAP_CHRG=11, sets the overcurrent turn-off threshold during inrush phase and thus the peak current of the current pulse. 0h = Sets overcurrent turn-off and peak current to 47.5A 1h = Sets overcurrent turn-off and peak current to 55 A Ah = Sets overcurrent turn-off and peak current to 62.5 A Bh = Sets overcurrent turn-off and peak current to 70 A
13-12	CAP_CHRG_CH1	R/W	0h	Puts the part into the capacitive load driving mode. Turns on the INRUSH_LIMIT_CH1 bits to set the overcurrent protection or cap charging levels within the INRUSH_DURATION period and during that time there is no PWM or I2T 0h = No cap charging mode (immediate shutdown only) 1h = Cap charging mode dV/dt 2h = Cap charging mode current limit regulation mode. 3h = Cap charging mode - current pulse method
11	I2T_EN_CH1	R/W	0h	Enables the I2T functionality for Channel 1. I2T can be enabled before the channel is enabled or charges up, but the I2T calculation will start after the cap charge period ends If the cap charging mode is enabled (CAP_CHRG_CH1 [1:0] ne 00) . 0h = I2T functionality not enabled 1h = I2T functionality is enabled
10-8	INRUSH_DURATION_CH1	R/W	0h	Sets the delay period during with inrush current limit level applies. 0h = 0 1h = 2 2h = 4 3h = 6 4h = 10 5h = 20 6h = 50 7h = 100 ms
7-4	INRUSH_LIMIT_CH1_OR_CAP_CHRG_DVDT	R/W	8h	Overcurrent protection thresholds if CAP_CHRG_CH1 = 00. Becomes cap charging mode control bits when in cap charging mode. This means instead of having an overcurrent protection threshold setting for an inrush period, the bits are used to set the cap charging control bits setting either the dV/dt rate (CAP_CHRG_CH1 = 01), current limit (regulation) level (CAP_CHRG_CH1 = 10) or pulsed current mode parameters. (CAP_CHRG_CH1 = 11). When CAP_CHRG_CH1 = 00, then the same table as ILIMIT_SET_CH1 applies for overcurrent protection threshold during the INRUSH_DURATION. When CAP_CHRG_CH1 = 10, then the current limit threshold is below table with the value divided by 5. When CAP_CHRG_CH1 = 01, 4-bits will be used to set the dV/dt or voltage ramp rate per the table below. Only the specified bit settings are supported. 3h = 2.22 V/ms 5h = 1.0 V/ms 6h = 1.33 V/ms 7h = 1.66 V/ms 9h = 0.67 V/ms Ah = 0.89 V/ms Bh = 1.1 V/ms Ch = 0.33 V/ms Dh = 0.50 V/ms

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表 8-20. ILIM_CONFIG_CH1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-0	ILIMIT_SET_CH1	R/W	8h	Setting the overcurrent protection threshold after the INRUSH_DURATION period. 0h = 10 A 1h = 12.5 A 2h = 15 A 3h = 17.5 A 4h = 20 A 5h = 22.5 A 6h = 25 A 7h = 32.5 A 8h = 40 A 9h = 47.5 A Ah = 55 A Bh = 62.5 A Ch = 70 A Other settings are not supported.

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8.5.15 DIAG_CONFIG_CH1 Register (Offset = 10h) [Reset = C002h]

DIAG_CONFIG_CH1 is shown in 表 8-21.

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表 8-21. DIAG_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VSNS_DIS_CH1	R/W	1h	Set this bit to 1 to disable the VSNS ADC functionality for this channel 0h = VSNS ADC functionality enabled 1h = VSNS ADC functionality is disabled
14	TSNS_DIS_CH1	R/W	1h	Set this bit to 1 to disable the ADC TSNS functionality for this channel 0h = TSNS ADC functionality enabled 1h = TSNS ADC functionality is disabled
13	ISNS_DIS_CH1	R/W	0h	Set this bit to 1 to disable ISNS ADC functionality for this channel 0h = ISNS ADC functionality enabled 1h = ISNS ADC functionality is disabled
12-11	OL_ON_THLD_CH1	R/W	0h	Sets the open load detection threshold in the on state. 2 bits to set the open load detection threshold, not implemented in current silicon revision 0h = TBD 1h = TBD 2h = TBD 3h = TBD
10	ISNS_SCALE_CH1	R/W	0h	Turns on 8x scaling of voltage input to the ADC to improve the current sense resolution 0h = ADC input voltage scale equals 1 1h = ADC input voltage scale equals 8
9	OL_ON_EN_CH1	R/W	0h	Turns on a more accurate open load detection in the on state with KSNS ratio scaled to lower value. This will set the FET into high Rdson mode therefore this cannot be enabled if there is an existing fault on the channel or the current is too high 0h = KSNS ratio and FET Rdson unchanged 1h = Enable Open Load Detection with a lower KSNS ratio and higher Rdson
8-7	OL_SVBB_BLANK_CH1	R/W	0h	Sets the blanking time for open load (ON-state and OFF-state) and the short_to_VBB faults before the fault is registered. 0h = Blanking time is 0.4 ms 1h = Blanking time is 1.0 ms 2h = Blanking time is 2.0 ms 3h = Blanking time is 4.0 ms
6-5	OL_PU_STR_CH1	R/W	0h	Sets the pullup current value (at the OUTx pins) by the off-state open load detection circuit. 0h = I_pu is 32 uA 1h = I_pu is 64 uA 2h = I_pu is 128 uA 3h = I_pu is 256 uA
4	OL_OFF_EN_CH1	R/W	0h	Turns on the pull up to see if there is an open load in the off state. Cannot bet set high if channel is on or fault exists
3	SVBB_EN_CH1	R/W	0h	Turns on the pull down to see if there is a short to VBB in the off state. Cannot bet set high if channel is on or fault exists
2	LATCH_CH1	R/W	0h	If fault occurs that channel shuts down, this bit sets if the channel auto retries or latches off 0h = Auto retry after tRETRY and Thys 1h = latch off until SW_STATE register is written to again
1-0	SLRT_CH1	R/W	2h	Slew Rate set for ouput of CH1. 4 different slew rate values for adjustable slew rate per electrical characteristics table

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8.5.16 ADC_RESULT_CH1_I Register (Offset = 11h) [Reset = 0000h]

ADC_RESULT_CH1_I is shown in 表 8-22.

Return to the Summary Table.

表 8-22. ADC_RESULT_CH1_I Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	ISNS_RDY_CH1	R	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH1_I	R	0h	ADC result (10-bits) from the conversion of the current in CH1

8.5.17 ADC_RESULT_CH1_T Register (Offset = 12h) [Reset = 0000h]

ADC_RESULT_CH1_T is shown in 表 8-23.

Return to the Summary Table.

表 8-23. ADC_RESULT_CH1_T Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	TSNS_RDY_CH1	R	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH1_T	R	0h	ADC result (10-bits) from the conversion of the temperature in CH1

8.5.18 ADC_RESULT_CH1_V Register (Offset = 13h) [Reset = 0000h]

ADC_RESULT_CH1_V is shown in 表 8-24.

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表 8-24. ADC_RESULT_CH1_V Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	VSNS_RDY_CH1	R	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH1_V	R	0h	ADC result (10-bits) from the conversion of the output voltage in CH1

8.5.19 I2T_CONFIG_CH1 Register (Offset = 14h) [Reset = 0000h]

I2T_CONFIG_CH1 is shown in 表 8-25.

Return to the Summary Table.

表 8-25. I2T_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TCLDN_CH1	R/W	0h	2bits to Set cool down time for I2T functionality for Channel 1 (time to retry after I2T shutdown. 0h = Latch mode (or no retry) 1h = 0.8 s 2h = 2.0 s 3h = 4.0 s
13-11	RESERVED	R	0h	Reserved
10-9	SWCL_DLY_TMR_CH1	R/W	0h	2-bits to set delayed turn-off timer for Channel 1. Sets the time after which the channel shuts down when the current exceeds ISWCL. 0h = 0.2 ms 1h = 0.4 ms 2h = 1.0 ms 3h = 2.0 ms
8-7	ISWCL_CH1	R/W	0h	2bits to set delayed turn-off current threshold value for I2T functionality for Channel 1. The threshold should be set below the maximum current sensed with the sense resistor chosen. The current threshold assumes a sense resistor of 700 Ωs, otherwise scale the current with the resistor value relative to 700 Ωs 0h = 19.55 1h = 17.6 2h = 16.05 3h = 13.3
6-3	I2T_TRIP_CH1	R/W	0h	4bits to Set Trip value for I2T functionality for Channel 1. Assumes sense resistor of 700 Ωs, otherwise scale the current with the resistor value relative to 700 Ωs and the threshold changes by the square of the current. 0h = 8.8 A2s 1h = 13.1 A2s 2h = 26.3 A2s 3h = 39.4 A2s 4h = 52.5 A2s 5h = 65.6 A2s 6h = 78.8 A2s 7h = 91.9 A2s 8h = 109.4 A2s 9h = 126.9 A2s Ah = 144.4 A2s Bh = 166.3 A2s Ch = 192.5 A2s Dh = 218.8 A2s Eh = 262.5 A2s Fh = 350 A2s
2-0	NOM_CUR_CH1	R/W	0h	3 bits to set the nomial current value of Channel 1. Assumes sense resistor of 700 Ωs, otherwise scale the current with the resistor value relative to 700 Ωs 0h = 4.0 A 1h = 5.0 A 2h = 5.7 A 3h = 6.5 A 4h = 7.5 A 5h = 9.0 A 6h = 12.0 A 7h = 15.0 A

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8.5.20 FLT_STAT_CH2 Register (Offset = 15h) [Reset = 0000h]

FLT_STAT_CH2 is shown in 表 8-26.

Return to the Summary Table.

表 8-26. FLT_STAT_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	LATCH_STAT_CH2	R	0h	The bit is high if the channel has been latched off after a fault that shut down the channel. Clears when the channel is toggled back on 0h = CH2 is not latched off 1h = CH2 is currently latched off
10	FLT_CH2	R	0h	The bit is set if any type of real time fault (reverse current, thermal shutdown, open load (on/off-state) or short to supply) occurs in CH2 0h = No fault in CH2 1h = One or more fault has occurred in CH2
9	SW_STATE_STAT_CH2	R	0h	Current state of the channel no matter which mode the device is in as long as SPI is readable 0h = CH2 is OFF 1h = CH2 is ON
8	RESERVED	R	0h	Reserved
7	I2T_FLT_CH2	R	0h	The bit is set if there is a fault from I2T setting (overcurrent). Only can go high if I2T_EN is high and an associated fault occurs on that channel. Cleared when FLT_STAT_CH2 register is read and fault condition does not exist anymore 0h = no I2T fault or I2T is not enabled 1h = I2T fault has occurred on CH2
6	LPM_WAKE_CH2	R	0h	This bit is set if this channel was the reason the device came out of LPM regardless of why 0h = The device was not in LPM or this channel was not the one that cause the device to come out of LPM 1h = This channel was the reason the device came out of LPM
5	THERMAL_SD_CH2	R	0h	The bit is set if the thermal shutdown has occurred at any time in CH2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and channel temperature has fallen below the thermal shutdown reset threshold. 0h = No thermal shutdown fault in CH2 1h = Thermal shutdown has occurred in CH2
4	ILIMIT_CH2	R	0h	The bit is set if FET turn-off due to overcurrent has occurred at any time in CH2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and fault condition does not exist anymore. 0h = No overcurrent rprotection fault in CH2 1h = FET turn-off due to overcurrent fault has occurred in CH2
3	SHRT_VBB_CH2	R	0h	The bit is set if short to VBB has occurred at any time in CH2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and fault condition does not exist anymore. OL_SHRTVBB_DIFF_CH2 must have been enabled previously 0h = No Short to VBB fault in CH2 or short to VBB in OFF state not enabled 1h = Short to VBB Fault
2	OL_OFF_CH2	R	0h	Has the open load off state threshold been triggered? Only valid if OL_OFF_EN_CH2 is active. Device is pulled up with the threshold set by OL_PULLUP_STR 0h = No off state open load fault in CH2 or OL detection in OFF state not enabled 1h = Off State Open Load Fault

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表 8-26. FLT_STAT_CH2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	OL_ON_CH2	R	0h	Has the open load on state threshold been triggered? Only valid if OL_ON_EN_CH2 is active. Device is in high resistance mode 0h = No on state open load fault in CH2 or OL detection in OFF state not enabled 1h = On State Open Load Fault
0	THERMAL_WRN_CH2	R	0h	The bit is set if FET temperature is above the overtemperature warning threshold in CH2. The bit is cleared when over-temperature earning condition does not exist anymore. 0h = FET temperatire below over-temperature warning threshold in CH2 1h = FET temperatire above over-temperature warning threshold in CH2

8.5.21 PWM_CH2 Register (Offset = 16h) [Reset = 0000h]

PWM_CH2 is shown in 表 8-27.

Return to the Summary Table.

表 8-27. PWM_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-9	PWM_FREQ_CH2	R/W	0h	Set the PWM frequency 0h = 0.8 Hz 1h = 3.4 Hz 2h = 13.8 Hz 3h = 111 Hz 4h = 221 Hz 5h = 443 Hz 6h = 885 Hz 7h = 1770 Hz
8-1	PWM_DTY_CH2	R/W	0h	8 bit to set duty cycle for PWM operation of CH2. Each bit ~0.39% duty cycle
0	PWM_EN_CH2	R/W	0h	Enable PWMing of the output if on cycle of PWM is >200us. If not return error in FLT_STAT_CH2 register. PWM mode cannot be enabled unless CAP_CHRGx [1:0] = 00 0h = Output follows SW_STATE behavior (ON/OFF) 1h = Output is PWMing according to duty cycle and frequency set if SW_STATE CH2 is ON

8.5.22 ILIM_CONFIG_CH2 Register (Offset = 17h) [Reset = 0088h]

ILIM_CONFIG_CH2 is shown in 表 8-28.

Return to the Summary Table.

表 8-28. ILIM_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	OCP_INRUSH_CH2	R/W	0h	When CAP_CHRG=11, sets the overcurrent turn-off threshold during inrush phase and thus the peak current of the current pulse. 0h = Sets overcurrent turn-off and peak current to 47.5A 1h = Sets overcurrent turn-off and peak current to 55 A Ah = Sets overcurrent turn-off and peak current to 62.5 A Bh = Sets overcurrent turn-off and peak current to 70 A
13-12	CAP_CHRG_CH2	R/W	0h	Puts the part into the capacitive load driving mode. Turns on the INRUSH_LIMIT_CH2 bits to set the overcurrent protection or cap charging levels within the INRUSH_DURATION period and during that time there is no PWM or I2T 0h = No cap charging mode (immediate shutdown only) 1h = Cap charging mode dV/dt 2h = Cap charging mode current limit regulation mode. 3h = Cap charging mode - current pulse method
11	I2T_EN_CH2	R/W	0h	Enables the I2T functionality for Channel 2. I2T can be enabled before the channel is enabled or charges up, but the I2T calculation will start after the cap charge period ends If the cap charging mode is enabled (CAP_CHRG_CH2 [1:0] ne 00) .
10-8	INRUSH_DURATION_CH2	R/W	0h	Sets the delay period during with inrush current limit level applies. See table of delay settings in the datasheet. 0h = 0 1h = 2 2h = 4 3h = 6 4h = 10 5h = 20 6h = 50 7h = 100 ms
7-4	INRUSH_LIMIT_CH2_OR_CAP_CHRG_DVDT	R/W	8h	Overcurrent protection thresholds if CAP_CHRG_CH1 = 00. Becomes cap charging mode control bits when in cap charging mode. This means instead of having an overcurrent protection threshold setting for an inrush period, the bits are used to set the cap charging control bits setting either the dV/dt rate (CAP_CHRG_CH1 = 01), current limit (regulation) level (CAP_CHRG_CH1 = 10) or pulsed current mode parameters. (CAP_CHRG_CH1 = 11). When CAP_CHRG_CH1 = 00, then the same table as ILIMIT_SET_CH1 applies for overcurrent protection threshold during the INRUSH_DURATION. When CAP_CHRG_CH1 = 10, then the current limit threshold is below table with the value divided by 5. When CAP_CHRG_CH1 = 01, 4-bits will be used to set the dV/dt or voltage ramp rate per the table below. Only the specified bit settings are supported. 3h = 2.22 V/ms 5h = 1.0 V/ms 6h = 1.33 V/ms 7h = 1.66 V/ms 9h = 0.67 V/ms Ah = 0.89 V/ms Bh = 1.1 V/ms Ch = 0.33 V/ms Dh = 0.50 V/ms

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表 8-28. ILIM_CONFIG_CH2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-0	ILIMIT_SET_CH2	R/W	8h	Setting the overcurrent protection threshold after the INRUSH_DURATION period. 0h = 10 A 1h = 12.5 A 2h = 15 A 3h = 17.5 A 4h = 20 A 5h = 22.5 A 6h = 25 A 7h = 32.5 A 8h = 40 A 9h = 47.5 A Ah = 55 A Bh = 62.5 A Ch = 70 A Other settings are not supported.

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8.5.23 DIAG_CONFIG_CH2 Register (Offset = 18h) [Reset = C002h]

DIAG_CONFIG_CH2 is shown in 表 8-29.

Return to the Summary Table.

表 8-29. DIAG_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VSNS_DIS_CH2	R/W	1h	Set this bit to 1 to disable the VSNS ADC functionality for this channel 0h = VSNS ADC functionality enabled 1h = VSNS ADC functionality is disabled
14	TSNS_DIS_CH2	R/W	1h	Set this bit to 1 to disable the ADC TSNS functionality for this channel 0h = TSNS ADC functionality enabled 1h = TSNS ADC functionality is disabled
13	ISNS_DIS_CH2	R/W	0h	Set this bit to 1 to disable ISNS ADC functionality for this channel 0h = ISNS ADC functionality enabled 1h = ISNS ADC functionality is disabled
12-11	OL_ON_THLD_CH2	R/W	0h	Sets the open load detection threshold in the on state. 2 bits to set the open load detection threshold, not implemented in current silicon revision 0h = TBD 1h = TBD 2h = TBD 3h = TBD
10	ISNS_SCALE_CH2	R/W	0h	Turns on 8x scaling of voltage input to the ADC to improve the current sense resolution 0h = ADC input voltage scale equals 1 1h = ADC input voltage scale equals 8
9	OL_ON_EN_CH2	R/W	0h	Turns on a more accurate open load detection in the on state with KSNS ratio scaled to lower value. This will set the FET into high Rdson mode therefore this cannot be enabled if there is an existing fault on the channel or the current is too high 0h = KSNS ratio and FET Rdson unchanged 1h = Enable more accurate Open Load Detection with a lower KSNS ratio and higher Rdson
8-7	OL_SVBB_BLANK_CH2	R/W	0h	Sets the blanking time for open load (ON-state and OFF-state) and the short_to_VBB faults before the fault is registered. 0h = Blanking time is 0.4 ms 1h = Blanking time is 1.0 ms 2h = Blanking time is 2.0 ms 3h = Blanking time is 4.0 ms
6-5	OL_PU_STR_CH2	R/W	0h	Sets the pullup current value (at the OUTx pins) by the off-state open load detection circuit. 0h = I_pu is 32 uA 1h = I_pu is 64 uA 2h = I_pu is 128 uA 3h = I_pu is 256 uA
4	OL_OFF_EN_CH2	R/W	0h	Turns on the pull up to see if there is an open load in the off state. Cannot bet set high if channel is on or fault exists
3	SVBB_EN_CH2	R/W	0h	Turns on the pull down to see if there is a short to VBB in the off state. Cannot bet set high if channel is on or fault exists
2	LATCH_CH2	R/W	0h	If fault occurs that channel shuts down, this bit sets if the channel auto retries or latches off 0h = Auto retry after tRETRY and Thys 1h = latch off until SW_STATE register is written to again
1-0	SLRT_CH2	R/W	2h	Slew Rate set for ouput of CH1. 4 different slew rate values for adjustable slew rate per electrical characteristics table

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8.5.24 ADC_RESULT_CH2_I Register (Offset = 19h) [Reset = 0000h]

ADC_RESULT_CH2_I is shown in 表 8-30.

Return to the Summary Table.

表 8-30. ADC_RESULT_CH2_I Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	ISNS_RDY_CH2	R	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH2_I	R	0h	ADC result (10-bits) from the conversion of the current in CH2

8.5.25 ADC_RESULT_CH2_T Register (Offset = 1Ah) [Reset = 0000h]

ADC_RESULT_CH2_T is shown in 表 8-31.

Return to the Summary Table.

表 8-31. ADC_RESULT_CH2_T Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	TSNS_RDY_CH2	R	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH2_T	R	0h	ADC result (10-bits) from the conversion of the temperature in CH2

8.5.26 ADC_RESULT_CH2_V Register (Offset = 1Bh) [Reset = 0000h]

ADC_RESULT_CH2_V is shown in 表 8-32.

Return to the Summary Table.

表 8-32. ADC_RESULT_CH2_V Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	VSNS_RDY_CH2	R	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH2_V	R	0h	ADC result (10-bits) from the conversion of the output voltage in CH2

8.5.27 I2T_CONFIG_CH2 Register (Offset = 1Ch) [Reset = 0000h]

I2T_CONFIG_CH2 is shown in 表 8-33.

Return to the Summary Table.

表 8-33. I2T_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TCLDN_CH2	R/W	0h	2bits to Set cool down time for I2T functionality for Channel 2 (time to retry after I2T shutdown. 0h = Latch mode (or no retry) 1h = 0.8 s 2h = 2.0 s 3h = 4.0 s
13-11	RESERVED	R	0h	Reserved
10-9	SWCL_DLY_TMR_CH2	R/W	0h	2-bits to set delayed turn-off timer for Channel 2. Sets the time after which the channel shuts down when the current exceeds ISWCL. 0h = 0.2 ms 1h = 0.4 ms 2h = 1.0 ms 3h = 2.0 ms
8-7	ISWCL_CH2	R/W	0h	2-bits to set delayed turn-off current threshold value for I2T functionality for Channel 2. The threshold should be set below the maximum current sensed with the sense resistor chosen. The current threshold assumes a sense resistor of 700 Ωs, otherwise scale the current with the resistor value relative to 700 Ωs 0h = 19.55 1h = 17.6 2h = 16.05 3h = 13.3
6-3	I2T_TRIP_CH2	R/W	0h	4-bits to Set Trip value for I2T functionality for Channel 1. Assumes sense resistor of 700 Ωs, otherwise scale the current with the resistor value relative to 700 Ωs and the threshold changes by the square of the current. 0h = 8.8 A2s 1h = 13.1 A2s 2h = 26.3 A2s 3h = 39.4 A2s 4h = 52.5 A2s 5h = 65.6 A2s 6h = 78.8 A2s 7h = 91.9 A2s 8h = 109.4 A2s 9h = 126.9 A2s Ah = 144.4 A2s Bh = 166.3 A2s Ch = 192.5 A2s Dh = 218.8 A2s Eh = 262.5 A2s Fh = 350 A2s
2-0	NOM_CUR_CH2	R/W	0h	3 bits to set the nomial current value of Channel 2. Assumes sense resistor of 700 Ωs, otherwise scale the current with the resistor value relative to 700 Ωs 0h = 4.0 A 1h = 5.0 A 2h = 5.7 A 3h = 6.5 A 4h = 7.5 A 5h = 9.0 A 6h = 12.0 A 7h = 15.0 A

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

図 9-1 shows the schematic of a typical application of the TPS2HC10S. It includes all standard external components. This section of the data sheet discusses the considerations in implementing commonly required application functionality. The circuit assumes no reverse polarity protection on the input supply, so additional components for protection are required.

Special Note on Prototype Silicon

The prototype silicon is not the final production silicon and is offered as preview. The following limitations exist in the prototype version.

1. There is a variation of ADC output in the range of +/-12 codes (for current sense) or +/- 4 codes for voltage sensing for a constant load current or output voltage and can affect the ADC readings at the low end of ADC range. The reason is due to excessive noise on the ADC supply input, which will be corrected in the production release.
2. The prototype device does not reliably support turn-off of the outputs (FETs) in case of a loss of GND. The production version will support FET turn-off with loss-of-GND.
3. The prototype device may see a high current flow and potential pin damage into the device upon unclamped negative transient similar to ISO-7637 Pulse 1 at the VBB supply input. The production version will be robust against these transients.

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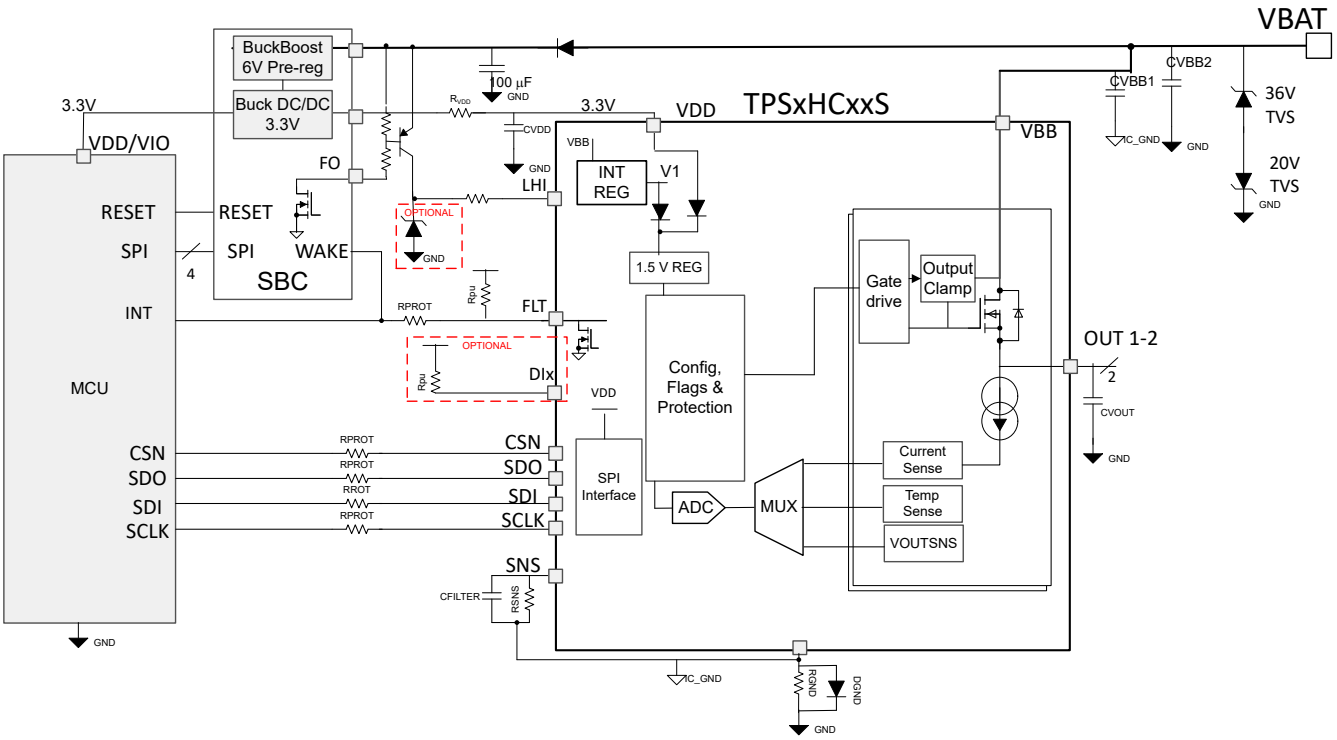

With the ground protection network, the device ground will be offset relative to the micro-controller ground. The same power supply (5 V (recommended) or 3.3V) source should be used for the controller (MCU) I/O as well as the VDD supply input to the TPS2HCS10-Q1 device.

図 9-1. System Diagram

表 9-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{PROT1}	1 – 2.2 kΩ	Protect micro-controller and device SPI pins
R_{PROT2}	10 kΩ	Protect micro-controller and device GPIO pins
R_{SNS}	1 kΩ	Translate the sense current into sense voltage for ADC input
C_{SNS}	1 nF - 4.7 nF	Low-pass filter for the ADC input.
Input TVS	+36 V and –20 V	Suppress voltage transients (one for the module)
D_{GND},	BAS21 / Schottky Diode	Limit Current during reverse voltage on supply events. A low forward voltage diode is recommended and a Schottky diode is suggested when the low voltage supply VDD is 3.3V. (Note that we recommend 5V supply for the prototype silicon)
R_{GND}	4.7 kΩ	Maintain ground potential during negative output voltage excursions
R_{VDD}	220 Ω	Limit current to the device during transients
C_{VDD}	470 nF	VDD supply voltage stability to system ground.
C_{VBB1}	4.7 nF to Device GND	Filtering of transients (for example, ESD, ISO7637-2) and improved emissions.
C_{VBB2}	100 – 2200-nF to Module GND	Stabilize the input supply and filter out low frequency noise.
C_{OUT}	22 nF	Filtering of voltage transients (for example, ESD, ISO7637-2).

9.2 Typical Application

This application example demonstrates how the TPS2HC10S-Q1 device can be used to power ECU loads with large input capacitance. This is just one example of the many applications where this device can fit.

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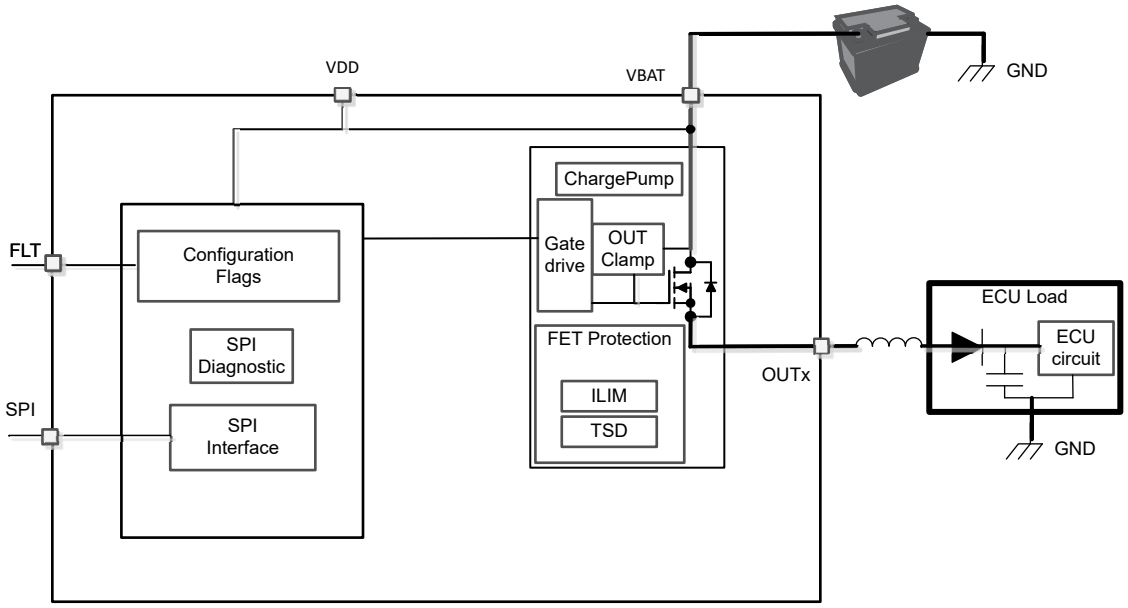

図 9-2. Block Diagram for Powering an ECU load with Input Capacitance

9.2.1 Design Requirements

For this design example, use the input parameters shown in 表 9-2.

表 9-2. Design Parameters

DESIGN PARAMETER	Case 1	Case 2
V_{BB} range	8 V to 16 V	8 V to 16 V
Input Capacitance of the ECU load	600 uF	1500 uF
Maximum parallel load during the charging phase	3 A	0.4 A
Time to charge	2 ms	40 ms
Ambient temperature	85°C	85°C

9.2.2 Detailed Design Procedure

9.2.2.1 Thermal Considerations

The output voltage ramps while the load capacitance is being charged. During this period, the power dissipation in the FET is high due to the large drain-to-source voltage. The power dissipation and the resultant increase in the silicon junction temperature limits the capacitance that can be charged before the device hits thermal shutdown. In general, lower the charging rate (current), the higher the value of capacitance that can be charged. But if a lower charging current is used, the charging time will be higher. In the application cases considered here, it is expected that the FET junction temperature will not reach the thermal shutdown threshold.

9.2.2.2 Configuring the Capacitive Charging Mode

The configuration parameters for the two channels are in the ILIM_CONFIG_CH1 and ILIM_CONFIG_CH2 registers respectively. The device can be configured in the capacitive charging mode that is the best choice for the capacitance and the parallel load current draw. The device offers two options - a constant current charging mode designed for cases where there is a significant load current during charging phase (Case 1) or a fixed dV/dt rate charging mode that is designed for very large capacitive loads that needs to be charged with a very low charging current (Case 2). For both modes, the charging rate is set by the

INRUSH_LIMIT_CH1_OR_CAP_CHRG_DVDT bits ([7:4]) in the ILIM_CONFIG_CH1 or ILIM_CONFIG_CH2 registers. The INRUSH_DURATION_CHx bits should be set such that the worst case expected capacitive charge time is below the programmed inrush duration. The recommended choice of bit settings for each application case is listed in the table below.

表 9-3. Setting Capacitive Charging Mode Parameters

Bit Field in the ILIM_CONFIG_CHx Register	Case 1	Case 2
CAP_CHRG_CHx	0x02h	0x01h
INRUSH_DURATION_CHx	0x02h	0x06h
INRUSH_LIMIT_CH1_OR_CAP_CHRG_DVDT	0x04h	0x0Ah

9.3 Power Supply Recommendations

The device is designed to operate in a 12-V automotive system. The device works with two power supply inputs – a typically 12V battery input and a low voltage supply input (5V or 3.3V) typically generated with a DC-DC converter (recommended to reduce quiescent current draw from the battery) or LDO external to the IC from the battery.

The nominal supply voltage range is 6 V to 18 V as measured at the V_{BB} pin with respect to the GND pin of the device. In this range the device meets full parametric specifications as listed in the *Electrical Characterisitcs* table. The device is also designed to withstand voltage transients beyond this range like load dump. When operating outside of the nominal voltage range but within the operating voltage range, the device will exhibit normal functional behavior.

表 9-4. Operating Voltage Range

V_{BB} VOLTAGE RANGE	NOTE
3 V to 6 V	Extended lower 12-V automotive battery operation such as cold crank and start-stop. Device is fully functional and protected but some parametrics such as RON, current sense accuracy, over-current thresholds and timing parameters can deviate from specifications. Check the individual specifications in the Electrical Characteristics to confirm the voltage range it is applicable for,
6 V to 18 V	Nominal supply voltage, all parametric specifications apply. The device is completely short-circuit protected up to 125°C.
18 V to 24 V	Extended upper 12-V automotive battery operation such as double battery. Device is fully functional and protected but some parametrics such as RON, current sense accuracy, over-current thresholds, and timing parameters can deviate from specifications. Check the individual specifications in the Electrical Characteristics to confirm the voltage range it is applicable for.
24 V to 35 V	Load dump voltage. Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.

9.4 Layout

9.4.1 Layout Guidelines

To achieve optimal thermal performance, connect the exposed thermal pad (connected to VBB pin) to a large broken copper pour. On the top PCB layer, the pour can extend beyond the package dimensions as shown in the example below. In addition to this, TI recommends to also have a V_{BB} plane either on one of the internal PCB layers or on the bottom layer.

Vias must connect this plane to the top V_{BB} pour. TI recommends that the IO pins that connect to the controller be routed through a via and internal or bottom PCB layer.

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9.4.2 Layout Example

A PCB layout example is shown with the top layer copper for VBB input to the device and the VOUTx pins. The IO connected to the MCU is shown in another PCB layer with vias from the device pin connections. .

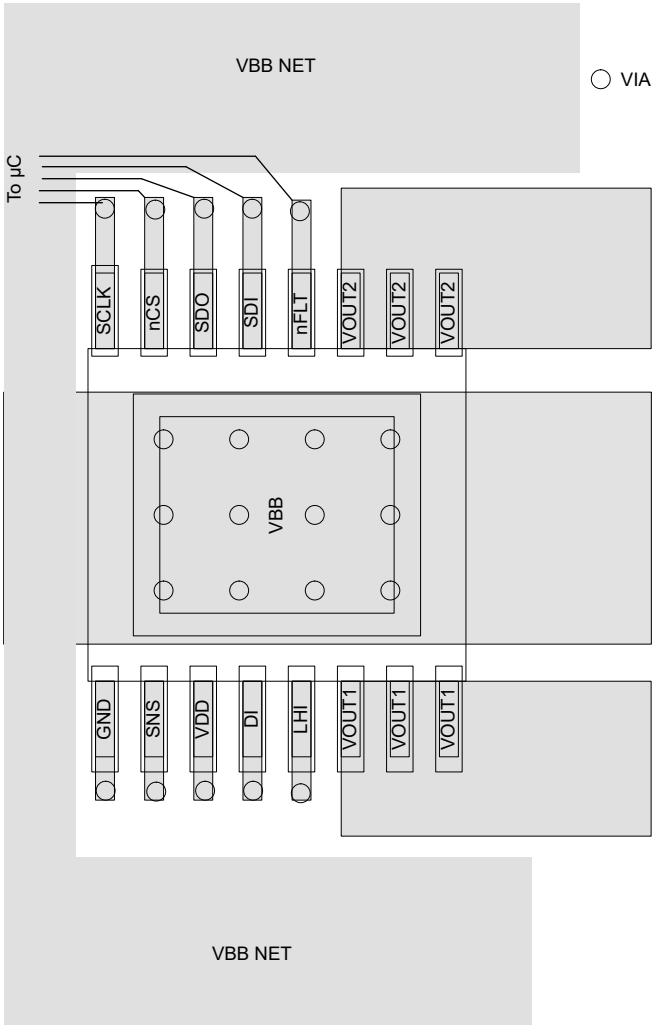

図 9-3. 16-PWP Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS2HCS10-Q1 Configurator GUI*
- Texas Instruments, *TPS2HCS10-Q1 Source Release*
- Texas Instruments, *Smart Fuse Evaluation Module* user's guide
- Texas Instruments, *Short-Circuit Reliability Test for Smart Power Switch* application report
- Texas Instruments, *Reverse Battery Protection for High Side Switches* application report
- Texas Instruments, *How To Drive Inductive, Capacitive, and Lighting Loads with Smart High Side Switches* application report

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.4 Trademarks

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10.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

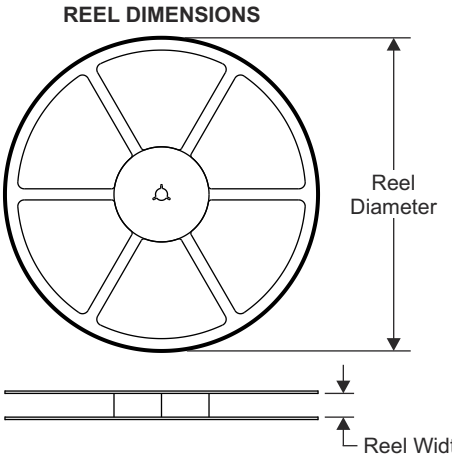
テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

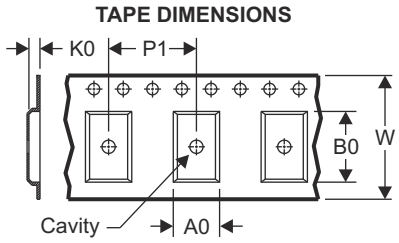
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

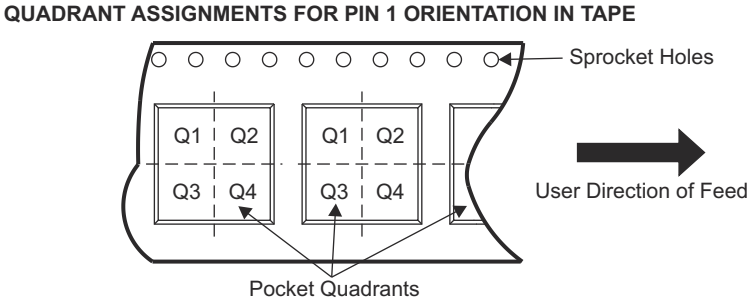
ADVANCE INFORMATION

11.1 Tape and Reel Information





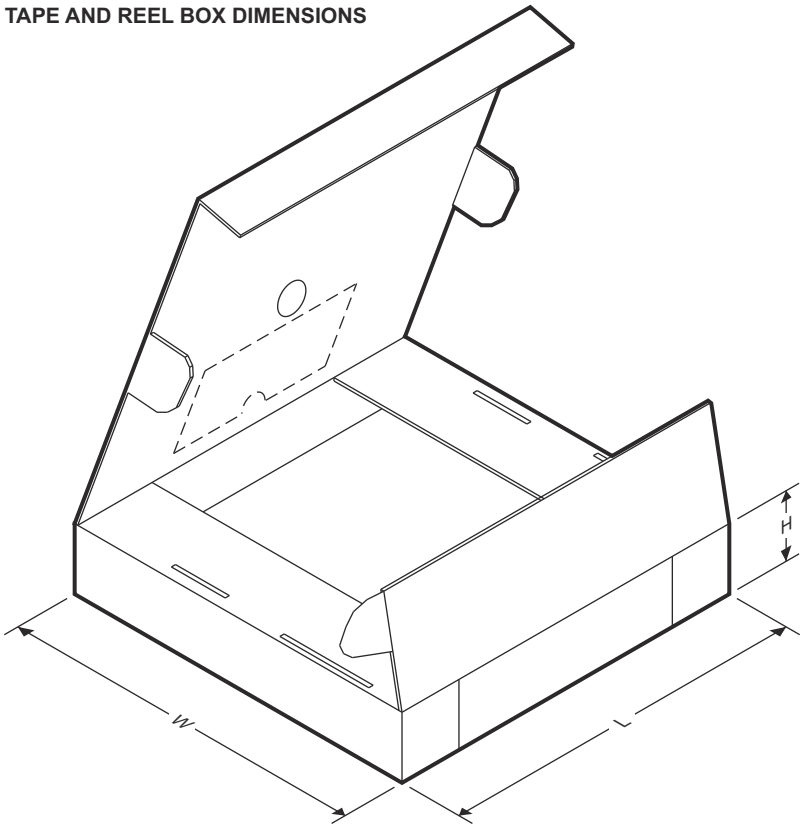
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS2HCS10AQPWPRQ1	HTSSOP	PWP	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



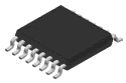
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS2HCS10AQPWPRQ1	HTSSOP	PWP	16	3000	367.0	367.0	38.0

ADVANCE INFORMATION

ADVANCE INFORMATION

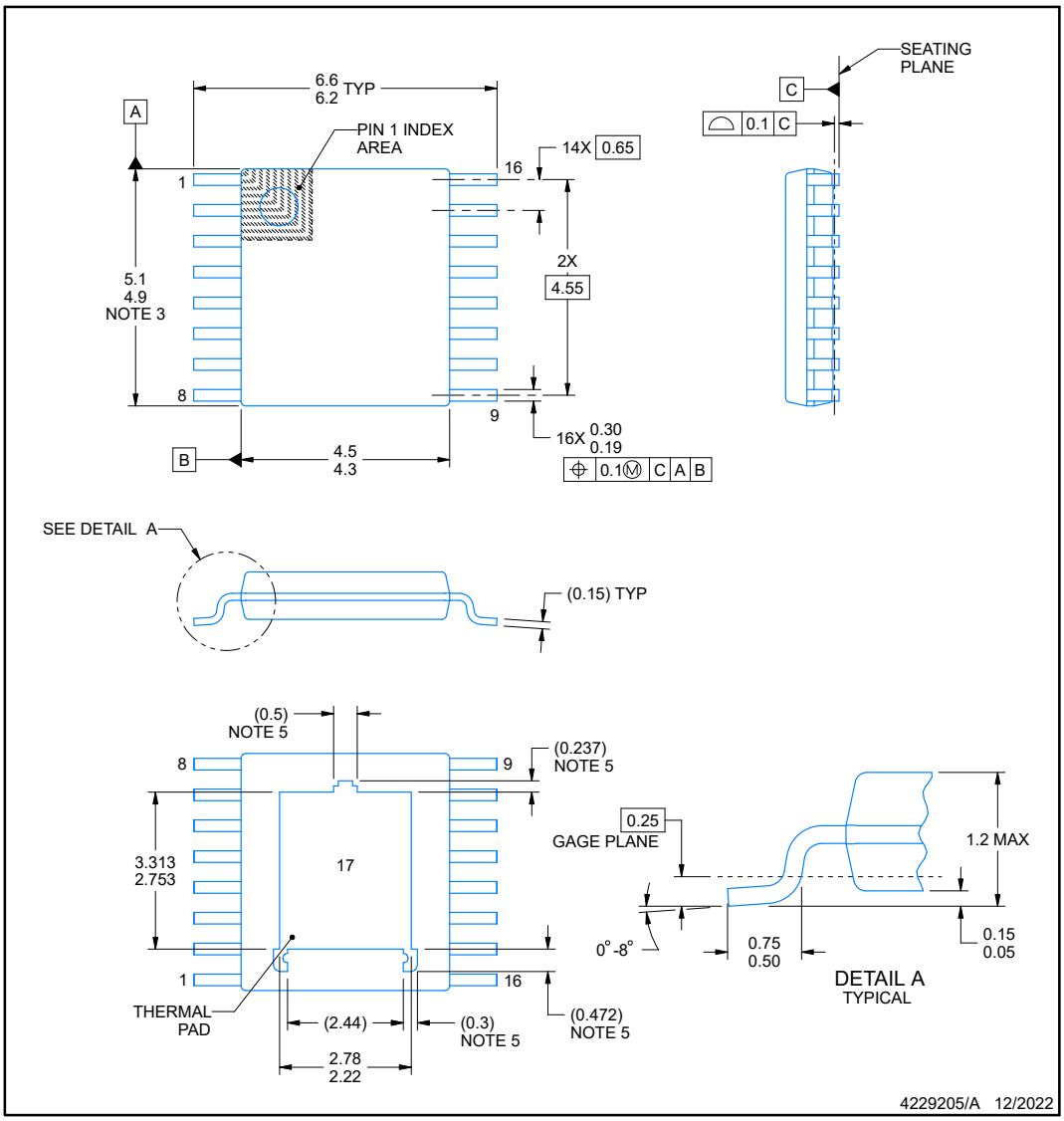
PACKAGE OUTLINE

PWP0016P



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

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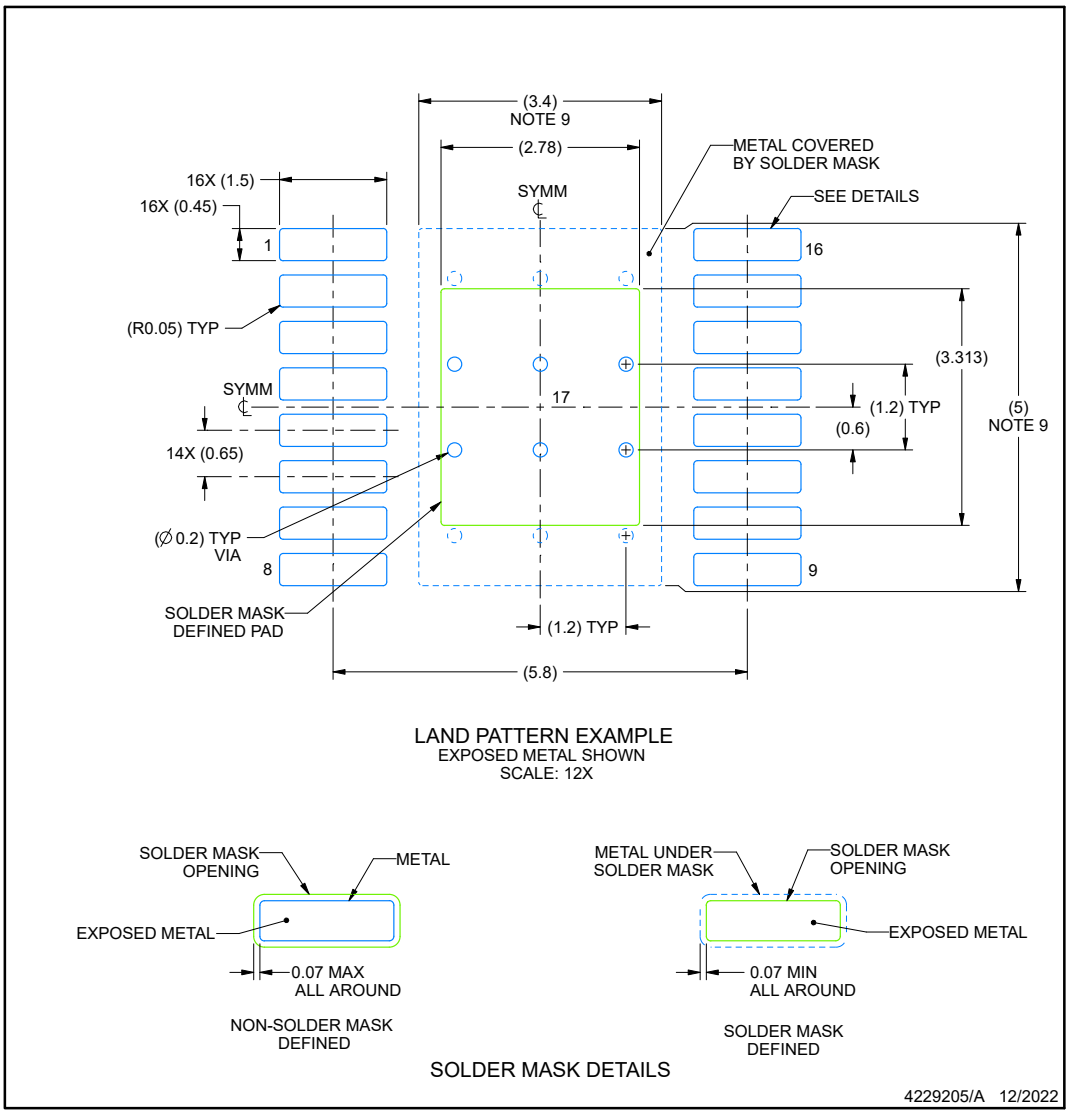
EXAMPLE BOARD LAYOUT

PWP0016P — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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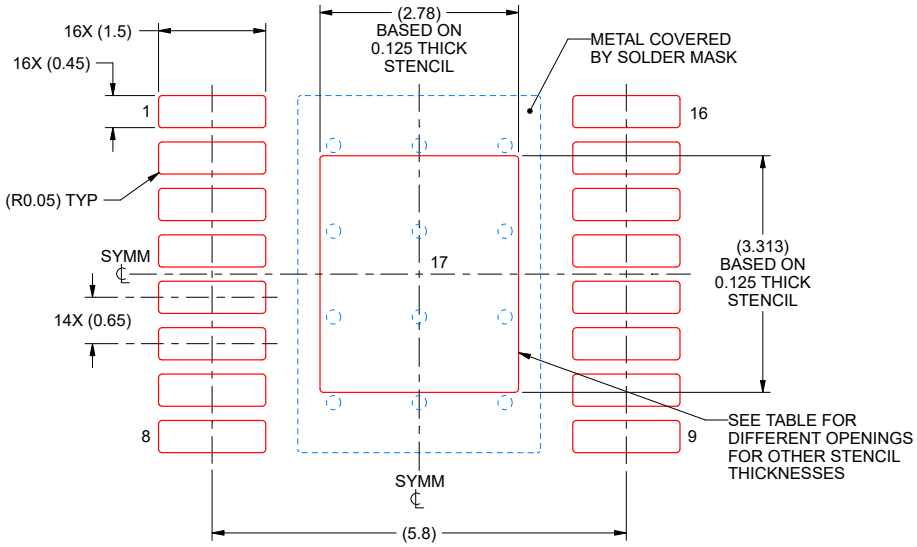
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PWP0016P — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.11 X 3.70
0.125	2.78 X 3.31 (SHOWN)
0.15	2.54 X 3.02
0.175	2.35 X 2.80

4229205/A 12/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS2HCS10AQPWPRQ1	Active	Preproduction	HTSSOP (PWP) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS2HCS10AQPWPRQ1.A	Active	Preproduction	HTSSOP (PWP) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS2HCS10AQPWPRQ1.B	Active	Preproduction	HTSSOP (PWP) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

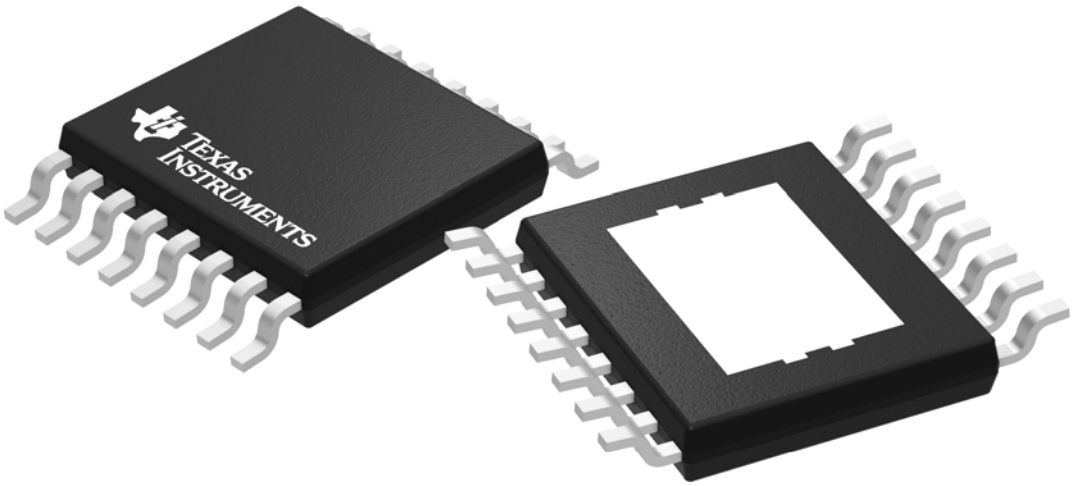
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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