TEXAS INSTRUMENTS
TPS28225-Q1
JAJSN42D – DECEMBER 2011 – REVISED DECEMBER 2021

TPS28225-Q1 車載用、高周波、4A シンク、同期 MOSFET ドライバ

1 特長

- 車載アプリケーション向けに認定済み
- 2 つの N チャネル MOSFET を 14ns の適応型デッド・タイムで駆動
- 広いゲート駆動電圧範囲:4.5V～8.8V (7V～8V で最大効率)
- 広いパワー・システム・トレイン入力電圧範囲:3V～27V
- 広い PWM 入力信号範囲:2V～13.2V の振幅
- 1 相あたり 40A 以上の電流で MOSFET を駆動可能
- 高周波動作:14ns の伝播遅延、10ns の立ち上がり / 立ち下がり時間により、
  最大 2MHz の F_{SW} を実現
- 30ns 未満の入力 PWM パルスを伝搬可能
- ローサイド・ドライバ・シンク・オン抵抗 (0.4Ω) により、dV/dt に関連する貫通電流を防止
- パワー段をシャットダウンするための 3 ステート PWM 入力
- 同じピンを共有する省スペースのイネーブル (入力) 信号とパワー・グッド (出力) 信号
- サーマル・シャットダウン
- UVLO 保護
- 内蔵ブートストラップ・ダイオード
- 安価な SOIC-8 パッケージと放熱性に優れた 3mm × 3mm VSON-8 パッケージ
- 一般的な 3 ステート入力ドライバに対する高性能な代替品

2 アプリケーション

- アナログまたはデジタル制御付きのマルチフェーズ DC-DC コンバータ
- 絶縁型ポイント・オブ・ロード向け同期整流
- ワイヤレス充電トランスミッタ

3 概要

TPS28225-Q1 は、適応型デッド・タイム制御機能を備えた、N チャネル相補型パワー MOSFET 用の高速ドライバです。さまざまな種類の 1 相および多相の高電流 DC-DC コンバータとともに使用できるよう最適化されています。TPS28225-Q1 は高効率であり、小さいソリューション・サイズと EMI 放射を特長としています。

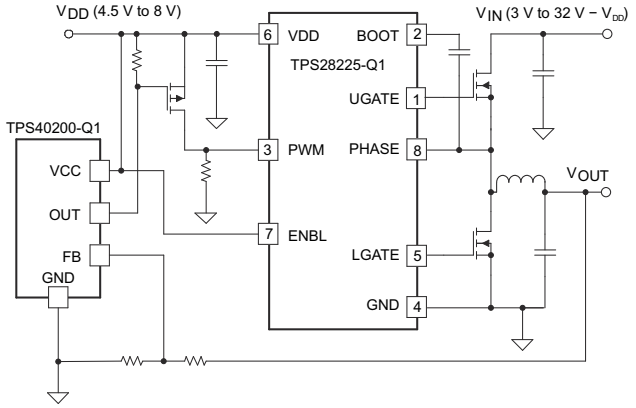
TPS28225-Q1 デバイスは、最大 8.8V のゲート駆動電圧、14ns の適応型デッド・タイム制御、14ns の伝播遅延、2A ソース / 4A シンクの高電流駆動能力などの優れた機能を備えています。ローサイド・ゲート・ドライバの 0.4Ω のインピーダンスによってパワー MOSFET のゲートをスレッショルド未満に保持し、高い dV/dt でノードが遷移した場合でも貫通電流が生じないようにしています。ブートストラップ・コンデンサは内蔵ダイオードで充電されるため、N チャネル MOSFET をハーフブリッジ構成で使用できます。

TPS28225-Q1 は安価な SOIC-8 パッケージと、放熱性に優れた小型 VSON パッケージで供給されます。本ドライバは –40℃～105℃の温度範囲で動作するように設計されており、接合部温度の絶対最大定格は 150℃です。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS28225-Q1	SOIC (8)	5.00mm × 6.20mm
	VSON (8)	3.00mm × 3.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2016) to Revision D (December 2021) — **Page**

- テキサス・インスツルメンツの最新のデータシート規格を反映するようにデータシートを更新 (タイトルへの「車載用」の追加を含む) ... 1
- Deleted the operating ambient temperature from the *Absolute Maximum Ratings* table ... 4

Changes from Revision B (April 2015) to Revision C (October 2016) — **Page**

- TPS25226-Q1 デバイスへの残りの参照を削除 ... 1
- 「*特長*」セクションから AEC-Q100 認定済みの特長 (デバイスの温度グレードと HBM および CDM ESD 分類) を削除 ... 1
- 「*特長*」一覧の DFN-8 を VSON-8 に変更 ... 1
- 「*ESD 定格*」表、「*概要*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーション情報*」セクション、「*電源に関する推奨事項*」セクション、「*ドキュメントの更新通知を受け取る方法*」セクションを追加 ... 1
- 「*概要*」セクションを更新 ... 1
- 8 ピン VSON (DRB) パッケージをデータシートに追加 ... 1
- Deleted the lead temperature parameter from the *Absolute Maximum Ratings* table ... 4
- Deleted the input supply voltage parameter for the TPS28226-Q1 device in the *Recommended Operating Conditions* table ... 4
- Added resistors between UGATE and PHASE, and LGATE and GND in the *Functional Block Diagram* ... 11
- Deleted the *TPS28225-Q1 3-State Exit Mode* section ... 12
- Added document reference to Figure 28 and *Related Documentation* section ... 18
- Deleted the *List of Materials* table ... 22
- Deleted references to Q8, Q9, and Q10 MOSFETs, and the rising and falling edge switching waveforms ... 24
- Changed *Layout Example* figure ... 24

5 Pin Configuration and Functions

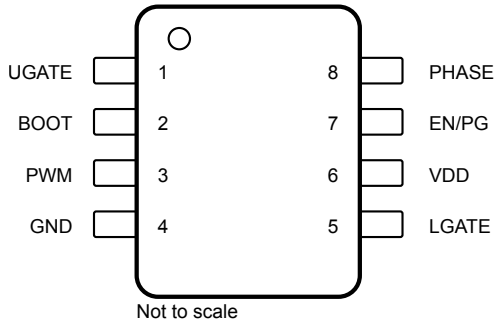


図 5-1. D Package 8-Pin SOIC Top View

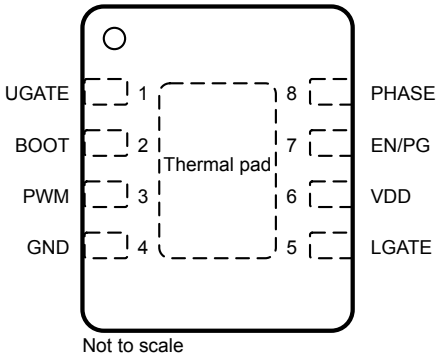


図 5-2. DRB Package 8-Pin VSON With Exposed Thermal Pad Top View

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	SOIC-8	VSON-8		
BOOT	2	2	I	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
EN/PG	7	7	I	Enable and Power Good input-output pin with 1-MΩ impedance. Connect this pin HIGH to enable and LOW to disable the device. When disabled, the device draws less than 350-µA bias current. If the V_{DD} voltage is below the UVLO threshold or overtemperature shutdown occurs, this pin is internally pulled low.
GND	4	4	GND	Ground pin. All signals are referenced to this node.
LGATE	5	5	I	Lower gate-drive sink and source output. Connect to the gate of the low-side power N-Channel MOSFET.
PHASE	8	8	I	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.
PWM	3	3	—	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the *セクション 7.3.4* section for more details. Connect this pin to the PWM output of the controller.
UGATE	1	1	I/O	Upper gate-drive sink and source output. Connect to gate of high-side power N-Channel MOSFET.
VDD	6	6	PWR	Connect this pin to a 5-V bias supply. Place a high quality bypass capacitor from this pin to GND.
Thermal pad		Exposed die pad	O	Connect directly to GND for better thermal performance and EMI.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Input supply voltage	V_{DD}	–0.3	8.8	V
	Boot voltage	V_{BOOT}	–0.3	33	V
	Phase voltage	V_{PHASE}, DC	–2	32 or V_{BOOT} + 0.3 – V_{DD} whichever is less	V
		V_{PHASE}, pulse < 400 ns, E = 20 µJ	–7	33.1 or V_{BOOT} + 0.3 – V_{DD} whichever is less	V
	Input voltage	V_{PWM}, $V_{EN/PG}$	–0.3	13.2	V
	Output voltage	V_{UGATE}, (V_{BOOT} – V_{PHASE} < 8.8)	V_{PHASE} – 0.3	V_{BOOT} + 0.3	V
		V_{UGATE}, Pulse < 100 ns, E = 2 µJ, (V_{BOOT} – V_{PHASE} < 8.8)	V_{PHASE} – 2	V_{BOOT} + 0.3	V
		V_{LGATE}	–0.3	V_{DD} + 0.3	V
		V_{LGATE}, Pulse < 100 ns, E = 2 µJ	–2	V_{DD} + 0.3	V
T_J	Operating virtual junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Data book for thermal limitations and considerations of packages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input supply voltage	4.5	7.2	8	V
V_{IN}	Power input voltage	3		32 – V_{DD}	V
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS28225-Q1		UNIT
		DRB (VSON)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.2	123.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.5	77	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.9	63.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	27.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26	63	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{DD} = 7.2 V, EN/PG pulled up to V_{DD} by 100-kΩ resistor, T_A = –40°C to 105°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDER VOLTAGE LOCKOUT						
	Rising threshold	V_{PWM} = 0 V	3.2	3.5	3.8	V
		V_{PWM} = 0 V, T_A = 25°C		3.5		
	Falling threshold	V_{PWM} = 0 V	2.7			V
		V_{PWM} = 0 V, T_A = 25°C		3		
	Hysteresis	T_A = 25°C		0.5		V
BIAS CURRENTS						
$I_{DD(off)}$	Bias supply current	$V_{EN/PG}$ = low, PWM pin floating, T_A = 25°C		350		µA
I_{DD}	Bias supply current	$V_{EN/PG}$ = high, PWM pin floating, T_A = 25°C		500		µA
INPUT (PWM)						
I_{PWM}	Input current	V_{PWM} = 5 V, T_A = 25°C		185		µA
		V_{PWM} = 0 V, T_A = 25°C		–200		µA
	PWM 3-state rising threshold[2]	T_A = 25°C		1		V
	PWM 3-state falling threshold	V_{PWM} PEAK = 5 V	3.4		4	V
		V_{PWM} PEAK = 5 V, T_A = 25°C		3.8		
t_{HLD_R}	3-state shutdown hold-off time	T_A = 25°C		250		ns
T_{MIN}	PWM minimum pulse to force U_{GATE} pulse	C_L = 3 nF at U_{GATE}, V_{PWM} = 5 V		30		ns
ENABLE/POWER GOOD (EN/PG)						
	Enable high rising threshold	PG FET OFF			2.1	V
		PG FET OFF, T_A = 25°C		1.7		
	Enable low falling threshold	PG FET OFF	0.8			V
		PG FET OFF, T_A = 25°C		1		
	Hysteresis	T_A = 25°C	0.35			V
				0.7		
	Power good output	V_{DD} = 2.5 V			0.2	V
UPPER GATE DRIVER OUTPUT (UGATE)						
	Source resistance	500-mA source current			2	Ω
		500-mA source current, T_A = 25°C		1		
	Source current[2]	$V_{UGATE-PHASE}$ = 2.5 V, T_A = 25°C		2		A

6.5 Electrical Characteristics (continued)

V_{DD} = 7.2 V, EN/PG pulled up to V_{DD} by 100-kΩ resistor, T_A = –40°C to 105°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RU}	Rise time	C_L = 3 nF, T_A = 25°C		10		ns
	Sink resistance	500-mA sink current			2	Ω
		500-mA sink current, T_A = 25°C		1		
	Sink current(2)	$V_{UGATE-PHASE}$ = 2.5 V, T_A = 25°C		2		A
t_{FU}	Fall time	C_L = 3 nF, T_A = 25°C		10		ns
LOWER GATE DRIVER OUTPUT (LGATE)						
	Source resistance	500-mA source current			2	Ω
		500-mA source current, T_A = 25°C		1		
	Source current(2)	V_{LGATE} = 2.5 V, T_A = 25°C		2		A
t_{RL}	Rise time(2)	C_L = 3 nF, T_A = 25°C		10		ns
	Sink resistance	500-mA sink current			1	Ω
		500-mA sink current, T_A = 25°C		0.4		
	Sink current(2)	V_{LGATE} = 2.5 V, T_A = 25°C		4		A
	Fall time(2)	C_L = 3 nF, T_A = 25°C		5		ns
BOOTSTRAP DIODE						
V_F	Forward voltage	Forward bias current 100 mA, T_A = 25°C		1		V
THERMAL SHUTDOWN						
	Rising threshold(2)		150		170	°C
		T_A = 25°C		160		
	Falling threshold(2)		130		150	°C
		T_A = 25°C		140		
	Hysteresis	T_A = 25°C		20		°C

(1) Typical values for T_A = 25°C
(2) Not production tested

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING TIME						
t_{DLU}	UGATE turn-off propagation delay	C_L = 3 nF		14		ns
t_{DLL}	LGATE turn-off propagation delay	C_L = 3 nF		14		ns
t_{DTU}	Dead time LGATE turnoff to UGATE turnon	C_L = 3 nF		14		ns
t_{DTL}	Dead time UGATE turnoff to LGATE turnon	C_L = 3 nF		14		ns

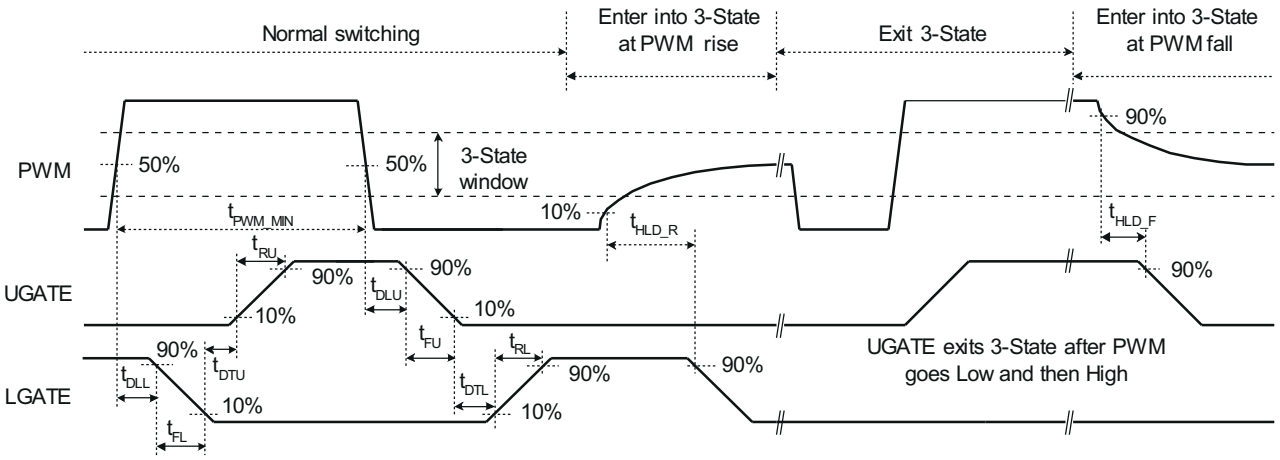
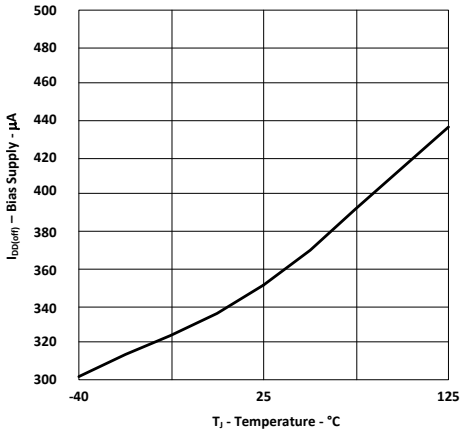


図 6-1. Timing Diagram

6.7 Typical Characteristics



$V_{EN/PG}$ = Low PWM Input Floating V_{DD} = 7.2 V

図 6-2. Bias Supply Current vs Temperature

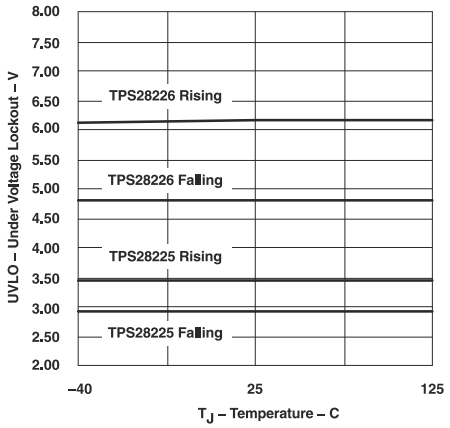
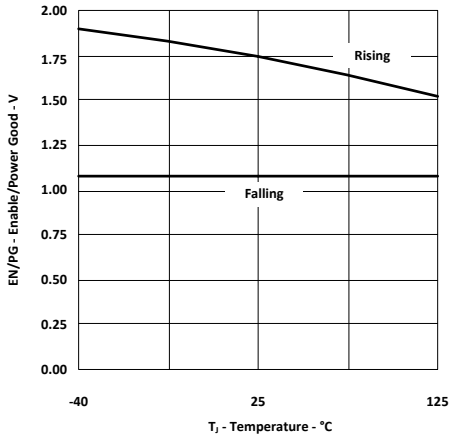
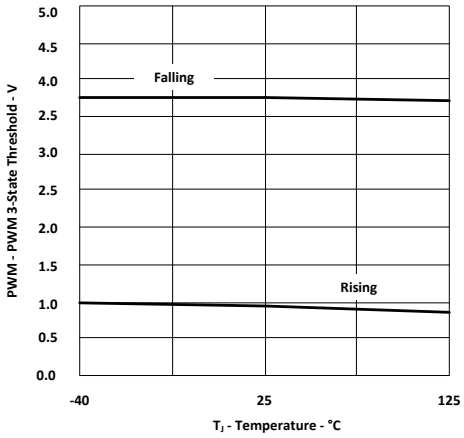


図 6-3. Undervoltage Lockout Threshold vs Temperature



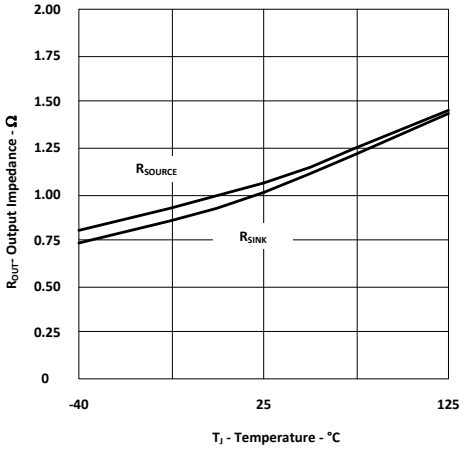
V_{DD} = 7.2 V

図 6-4. Enable/Power Good Threshold vs Temperature



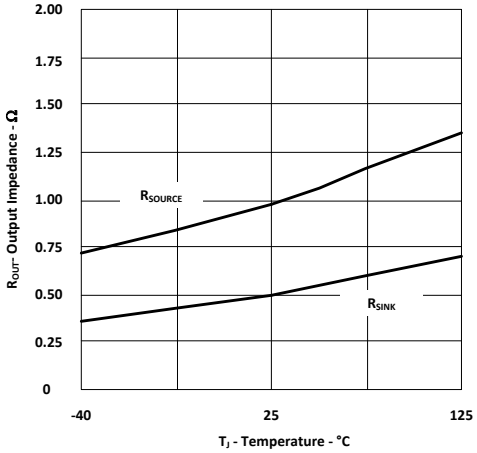
V_{DD} = 7.2 V

図 6-5. PWM 3-State Thresholds (5-V Input Pulses) vs Temperature



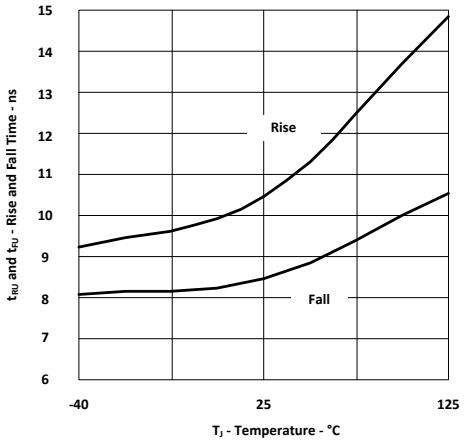
V_{DD} = 7.2 V

図 6-6. UGATE DC Output Impedance vs Temperature



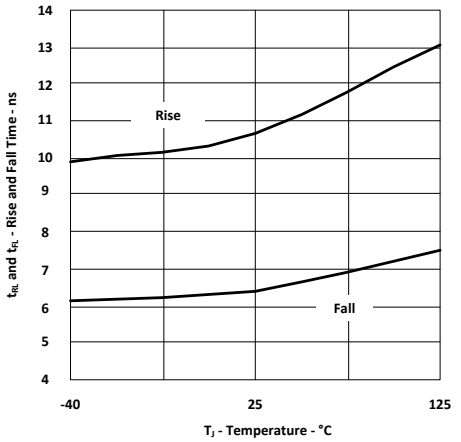
V_{DD} = 7.2 V

図 6-7. LGATE DC Output Impedance vs Temperature



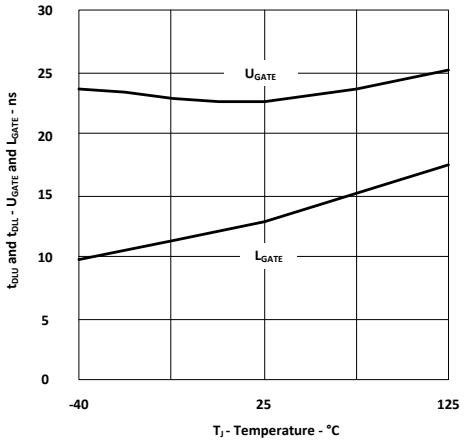
V_{DD} = 7.2 V C_{LOAD} = 3 nF

図 6-8. UGATE Rise and Fall Time vs Temperature



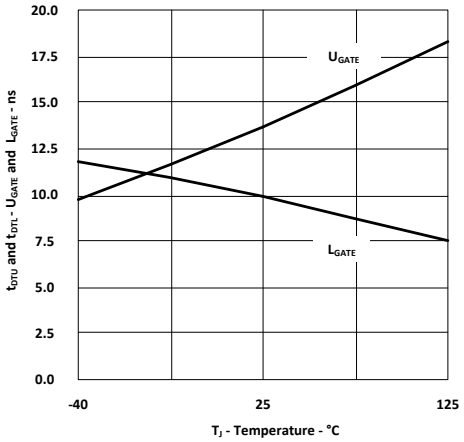
V_{DD} = 7.2 V C_{LOAD} = 3 nF

図 6-9. LGATE Rise and Fall Time vs Temperature



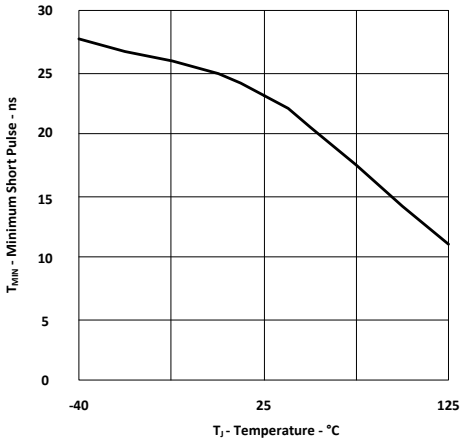
V_{DD} = 7.2 V C_{LOAD} = 3 nF

図 6-10. UGATE and LGATE (Turning OFF Propagation Delays) vs Temperature



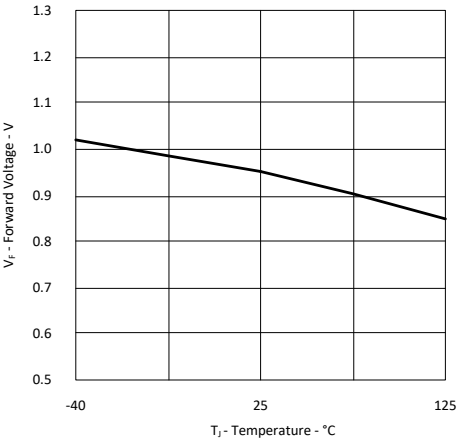
V_{DD} = 7.2 V C_{LOAD} = 3 nF

図 6-11. UGATE and LGATE (Dead Time) vs Temperature



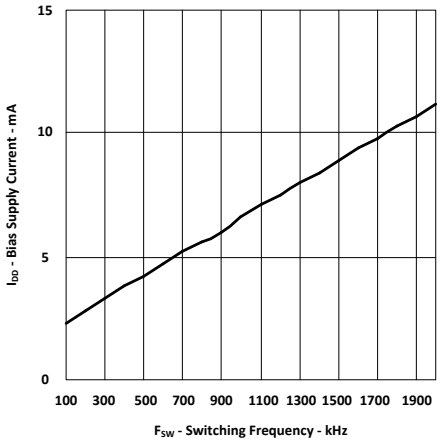
V_{DD} = 7.2 V C_{LOAD} = 3 nF

図 6-12. UGATE Minimum Short Pulse vs Temperature



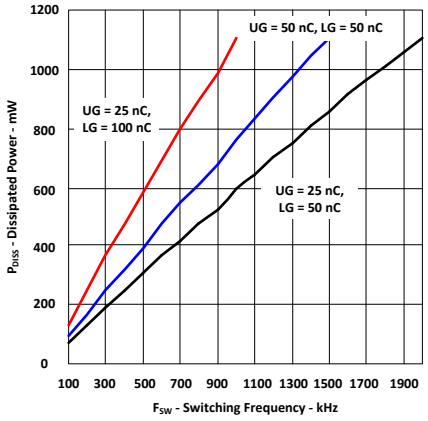
V_{DD} = 7.2 V I_F = 100 mA

図 6-13. Bootstrap Diode Forward Voltage vs Temperature



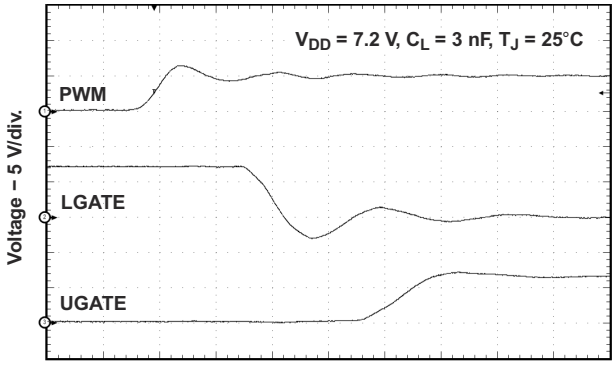
V_{DD} = 7.2 V No Load T_J = 25°C

図 6-14. Bias Supply Current vs Switching Frequency



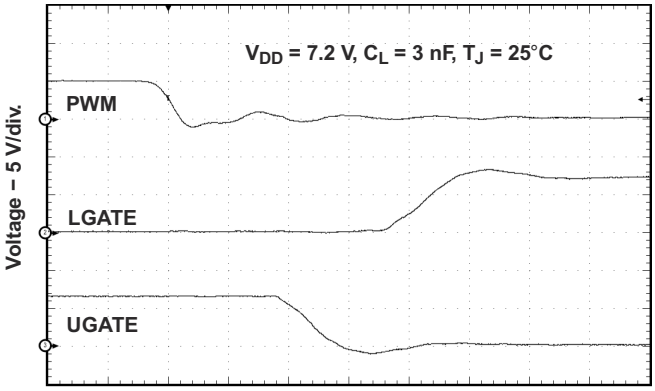
Different load charge V_{DD} = 7.2 V T_J = 25°C

図 6-15. Driver Dissipated Power vs Switching Frequency



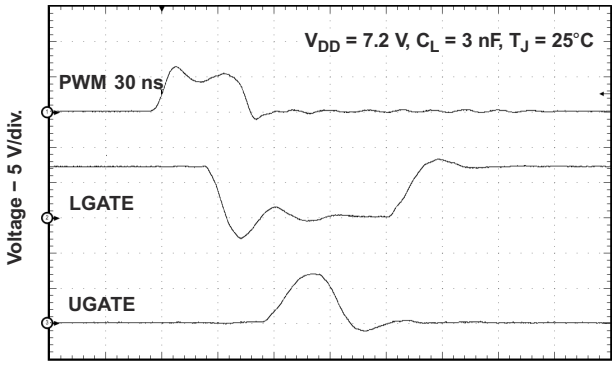
t – Time – 10 ns/div.

図 6-16. PWM Input Rising Switching Waveforms



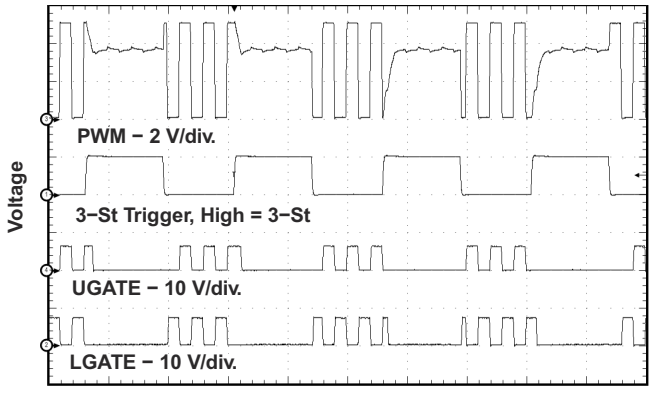
t – Time – 10 ns/div.

図 6-17. PWM Input Falling Switching Waveforms



t – Time – 20 ns/div.

図 6-18. Minimum UGATE Pulse Switching Waveforms



t – Time – 5 µs/div.

図 6-19. Normal and Three-State Operation ENTER/ EXIT Conditions

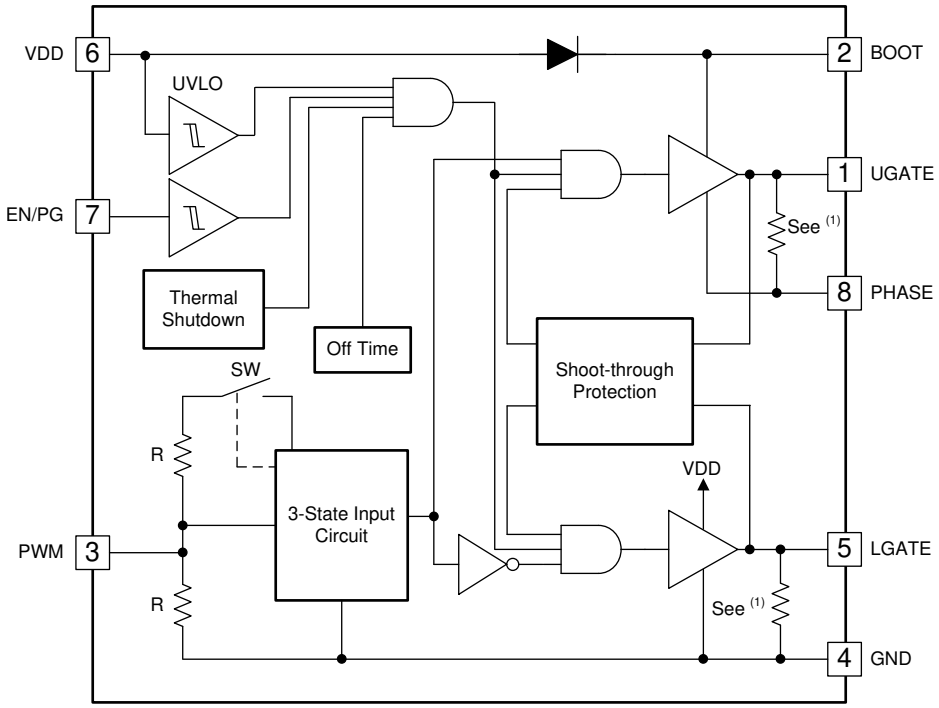
7 Detailed Description

7.1 Overview

The TPS28225-Q1 device features a 3-state PWM input compatible with all multi-phase controllers employing 3-state output feature. As long as the input stays within 3-state window for the 250-ns hold-off time, the driver switches both outputs low. This shutdown mode protects a load from the reversed output-voltage.

The other features include undervoltage lockout, thermal shutdown, and two-way enable/power good signal. Systems without 3-state featured controllers can use enable/power good input/output to hold both outputs low during shutting down.

7.2 Functional Block Diagram



A. See セクション 7.3.2.

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS28225-Q1 device incorporates an undervoltage lockout circuit that keeps the driver disabled and external power FETs in an OFF state when the input supply voltage V_{DD} is insufficient to drive external power FETs reliably. During power up, both gate drive outputs remain low until voltage V_{DD} reaches UVLO threshold, typically 3.5 V. When the UVLO threshold is reached, the condition of gate drive outputs is defined by the input PWM and EN/PG signals. During power down the UVLO threshold is set lower, typically 3 V. The 0.5-V hysteresis is selected to prevent the driver from turning ON and OFF while the input voltage crosses UVLO thresholds, especially with low slew rate. The TPS28225-Q1 has the ability to send a signal back to the system controller that the input supply voltage V_{DD} is insufficient by internally pulling down the EN/PG pin. The TPS28225-Q1 releases EN/PG pin immediately after the V_{DD} has risen above the UVLO threshold.

7.3.2 Output Active Low

The output active low circuit effectively keeps the gate outputs low even if the driver is not powered up. This prevents open gate conditions on the external power FETs and accidental turn ON when the main power stage supply voltage is applied before the driver is powered up. For the simplicity, the output active low circuit is shown

in the セクション 7.2 as the resistor connected between LGATE and GND pins with another one connected between UGATE and PHASE pins.

7.3.3 Enable/Power Good

The Enable/Power Good circuit allows the TPS28225-Q1 to follow the PWM input signal when the voltage at EN/PG pin is above 2.1 V maximum. This circuit has a unique two-way communication capability. This is illustrated by 図 7-1.

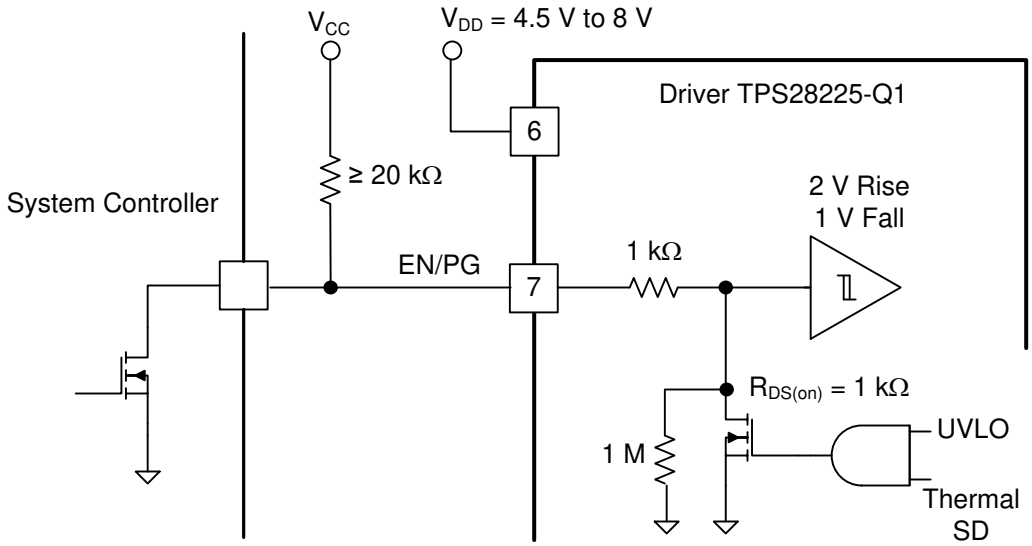


図 7-1. Enable/Power Good Circuit

The EN/PG pin has approximately 1-kΩ internal series resistor. Pulling EN/PG high by an external ≥ 20-kΩ resistor allows two-way communication between controller and driver. If the input voltage V_{DD} is below UVLO threshold or thermal shut down occurs, the internal MOSFET pulls EN/PG pin to GND through 1-kΩ resistor. The voltage across the EN/PG pin is now defined by the resistor divider comprised by the external pull up resistor, 1-kΩ internal resistor and the internal FET having 1-kΩ $R_{DS(on)}$. Even if the system controller allows the driver to start by setting its own enable output transistor OFF, the driver keeps the voltage at EN/PG low. Low EN/PG signal indicates that the driver is not ready yet because the supply voltage V_{DD} is low or that the driver is in thermal shutdown mode. The system controller can arrange the delay of PWM input signals coming to the driver until the driver releases EN/PG pin. If the input voltage V_{DD} is back to normal, or the driver is cooled down below its lower thermal shutdown threshold, then the internal MOSFET releases the EN/PG pin and normal operation resumes under the external Enable signal applied to EN/PG input. Another feature includes an internal 1-MΩ resistor that pulls EN/PG pin low and disables the driver in case the system controller accidentally loses connection with the driver. This could happen if, for example, the system controller is located on a separate PCB daughter board.

The EN/PG pin can serve as the second pulse input of the driver additionally to PWM input. The delay between EN/PG and the UGATE going high, provided that PWM input is also high, is only about 30ns. If the PWM input pulses are synchronized with EN/PG input, then when PWM and EN/PG are high, the UGATE is high and LGATE is low. If both PWM and EN/PG are low, then UGATE and LGATE are both low as well. This means the driver allows operation of a synchronous buck regulator as a convertional buck regulator using the body diode of the low side power MOSFET as the freewheeling diode. This feature can be useful in some specific applications to allow startup with a pre-biased output or, to improve the efficiency of buck regulator when in power saving mode with low output current.

7.3.4 3-State Input

As soon as the EN/PG pin is set high and input PWM pulses are initiated (see Note below). The dead-time control circuit ensures that there is no overlapping between UGATE and LGATE drive outputs to eliminate shoot

through current through the external power FETs. Additionally to operate under periodical pulse sequencing, the TPS28225-Q1 has a self-adjustable PWM 3-state input circuit. The 3-state circuit sets both gate drive outputs low, and thus turns the external power FETs OFF if the input signal is in a high impedance state for at least 250 ns typical. At this condition, the PWM input voltage level is defined by the internal 27-kΩ to 13-kΩ resistor divider shown in the block diagram. This resistor divider forces the input voltage to move into the 3-state window. Initially the 3-state window is set between 1.0-V and 2.0-V thresholds. The lower threshold of the 3-state window is always fixed at about 1.0 V. The higher threshold is adjusted to about 75% of the input signal amplitude. The self-adjustable upper threshold allows shorter delay if the input signal enters the 3-state window while the input signal was high, thus keeping the high-side power FET in ON state just slightly longer than 250 ns time constant set by an internal 3-state timer. Both modes of operation, PWM input pulse sequencing and the 3-state condition, are illustrated in the timing diagrams shown in 図 6-1. The self-adjustable upper threshold allows operation in wide range amplitude of input PWM pulse signals. The waveforms in 図 7-2 and 図 7-3 illustrates the TPS28225-Q1 operation at normal and 3-state mode with the input pulse amplitudes 6 V and 2.5 V accordingly. After entering into the 3-state window and staying within the window for the hold-off time, the PWM input signal level is defined by the internal resistor divider and, depending on the input pulse amplitude, can be pulled up above the normal PWM pulse amplitude (図 7-3) or down below the normal input PWM pulse (図 7-2).

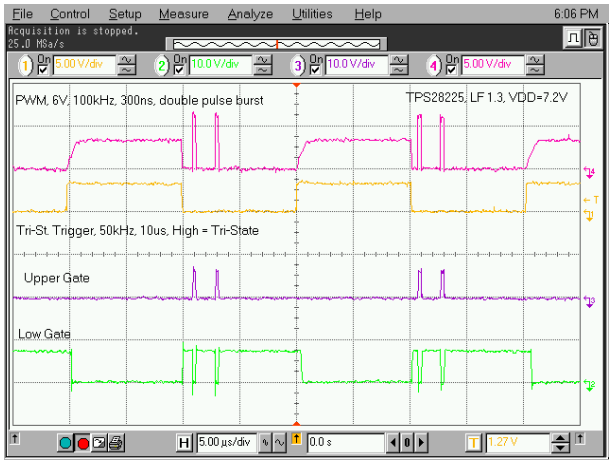


図 7-2. 6-V Amplitude PWM Pulse (TPS28225-Q1)

図 7-3. 2.5-V Amplitude PWM Pulse (TPS28225-Q1)

Note

The driver sets UGATE low and LGATE high when PWM is low. When the PWM goes high, UGATE goes high and LGATE goes low.

Note

Any external resistor between PWM input and GND with the value lower than 40 kΩ can interfere with the 3-state thresholds. If the driver is intended to operate in the 3-state mode, any resistor below 40 kΩ at the PWM and GND should be avoided. A resistor lower than 3.5 kΩ connected between the PWM and GND completely disables the 3-state function. In such case, the 3-state window shrinks to zero and the lower 3-state threshold becomes the boundary between the UGATE staying low and LGATE being high and vice versa depending on the PWM input signal applied. It is not necessary to use a resistor <3.5 kΩ to avoid the 3-state condition while using a controller that is 3-state capable. If the rise and fall time of the input PWM signal is shorter than 250 ns, then the driver never enter into the 3-state mode.

In the case where the low-side MOSFET of a buck converter stays on during shutdown, the 3-state feature can be fused to avoid negative resonant voltage across the output capacitor. This feature also can be used during start up with a pre-biased output in the case where pulling the output low during the startup is not allowed due to

system requirements. If the system controller does not have the 3-state feature and never goes into the high-impedance state, then setting the EN/PG signal low will keep both gate drive outputs low and turn both low- and high-side MOSFETs OFF during the shut down and start up with the pre-biased output.

The self-adjustable input circuit accepts wide range of input pulse amplitudes (2 V up to 13.2 V) allowing use of a variety of controllers with different outputs including logic level. The wide PWM input voltage allows some flexibility if the driver is used in secondary side synchronous rectifier circuit. The operation of the TPS28225-Q1 with a 12-V input PWM pulse amplitude, and with V_{DD} = 7.2 V and V_{DD} = 5 V respectively is shown in 図 7-4 and 図 7-5.

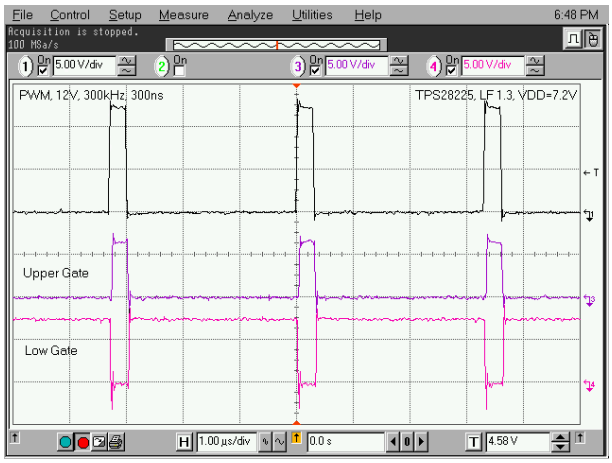


図 7-4. 12-V PWM Pulse at V_{DD} = 7.2 V

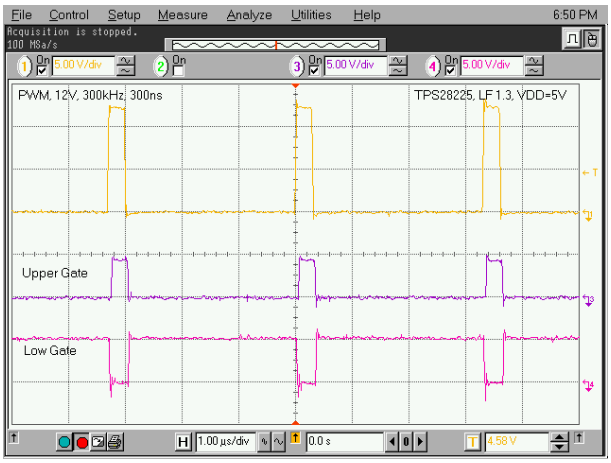


図 7-5. 12-V PWM Pulse at V_{DD} = 5 V

7.3.5 Bootstrap Diode

The bootstrap diode provides the supply voltage for the UGATE driver by charging the bootstrap capacitor connected between BOOT and PHASE pins from the input voltage VDD when the low-side FET is in ON state. At the very initial stage when both power FETs are OFF, the bootstrap capacitor is precharged through this path including the PHASE pin, output inductor and large output capacitor down to GND. The forward voltage drop across the diode is only 1.0 V at bias current 100 mA. This allows quick charge restore of the bootstrap capacitor during the high-frequency operation.

7.3.6 Upper and Lower Gate Drivers

The upper and lower gate drivers charge and discharge the input capacitance of the power MOSFETs to allow operation at switching frequencies up to 2 MHz. The output stage consists of a P-channel MOSFET providing source output current and an N-channel MOSFET providing sink current through the output stage. The ON state resistances of these MOSFETs are optimized for the synchronous buck converter configuration working with low duty cycle at the nominal steady state condition. The UGATE output driver is capable of propagating PWM input pulses of less than 30-ns while still maintaining proper dead time to avoid any shoot through current conditions. The waveforms related to the narrow input PWM pulse operation are shown in 図 7-5.

7.3.7 Dead-Time Control

The dead-time control circuit is critical for highest efficiency and no shoot through current operation throughout the whole duty cycle range with the different power MOSFETs. By sensing the output of driver going low, this circuit does not allow the gate drive output of another driver to go high until the first driver output falls below the specified threshold. This approach to control the dead time is called adaptive dead time. The overall dead time also includes the fixed portion to ensure that overlapping never exists. The typical dead time is around 14 ns, although it varies over the driver internal tolerances, layout and external MOSFET parasitic inductances. The proper dead time is maintained whenever the current through the output inductor of the power stage flows in the forward or reverse direction. Reverse current could happen in a buck configuration during the transients or while dynamically changing the output voltage on the fly, as some microprocessors require. Because the dead time does not depend on inductor current direction, this driver can be used both in buck and boost regulators or in

any bridge configuration where the power MOSFETs are switching in a complementary manner. Keeping the dead time at short optimal level boosts efficiency by 1% to 2% depending on the switching frequency.

Large non-optimal dead time can cause duty cycle modulation of the dc-to-dc converter during the operation point where the output inductor current changes its direction right before the turn ON of the high-side MOSFET. This modulation can interfere with the controller operation and it impacts the power stage frequency response transfer function. As the result, some output ripple increase can be observed. The TPS28225-Q1 driver is designed with the short adaptive dead time having fixed delay portion that eliminates risk of the effective duty cycle modulation at the described boundary condition.

7.3.8 Thermal Shutdown

If the junction temperature exceeds 160°C, the thermal shutdown circuit will pull both gate driver outputs low and thus turning both, low-side and high-side power FETs OFF. When the junction temperature of the driver cools down below 140°C after a thermal shutdown, then it resumes its normal operation and follows the PWM input and EN/PG signals from the external control circuit. While in thermal shutdown state, the internal MOSFET pulls the EN/PG pin low, thus setting a flag indicating the driver is not ready to continue normal operation. Normally the driver is located close to the MOSFETs, and this is usually the hottest spots on the PCB. Thus, the thermal shutdown feature of TPS28225-Q1 can be used as an additional protection for the whole system from overheating.

7.4 Device Functional Modes

表 7-1 lists the conditions under which the LGATE and UGATE pins are asserted high or low with respect to the voltage level present at VDD, EN/PG, and PWM pins.

表 7-1. Device State Table

PIN	V_{DD} RISING < 3.5 V OR T_J > 160°C	V_{DD} FALLING > 3 V AND T_J < 150°C			
		EN/PG RISING < 1.7 V	EN/PG FALLING > 1.0 V		
			PWM < 1 V	PWM > 1.5 V AND T_{RISE}/T_{FALL} < 200 ns	PWM SIGNAL SOURCE IMPEDANCE >40 kΩ FOR > 250 ns (3-STATE)(1)
LGATE	Low	Low	High	Low	Low
UGATE	Low	Low	Low	High	Low
EN/PG	Low				

(1) To exit the 3-state condition, the PWM signal should go low. One Low PWM input signal followed by one High PWM input signal is required before re-entering the 3-state condition.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

To effect fast switching of power devices and reduce associated switching power losses, a powerful MOSFET driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, MOSFET drivers are indispensable when it is impossible for the PWM controller to directly drive the MOSFETs of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. MOSFET drivers effectively combine both the level-shifting and buffer-drive functions.

MOSFET drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

8.2 Typical Application

図 8-1, 図 8-2, and 図 8-3 illustrate typical implementations of the TPS28225-Q1 in step-down power supplies.

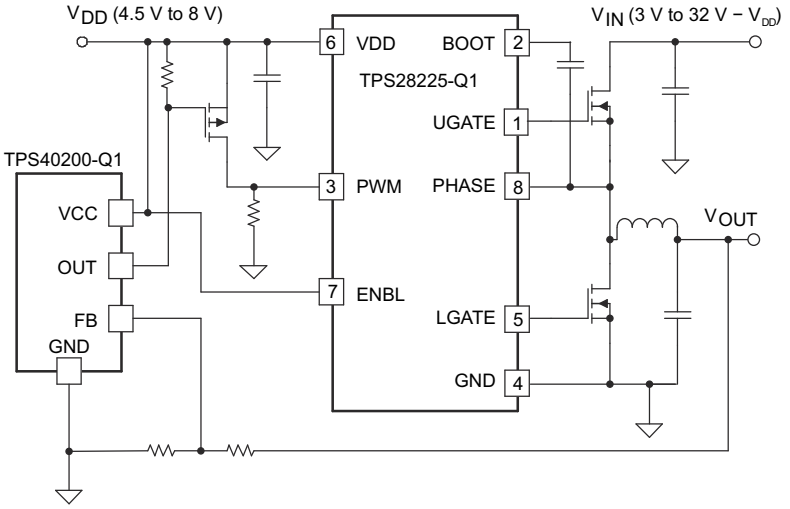


図 8-1. One-Phase POL Regulator

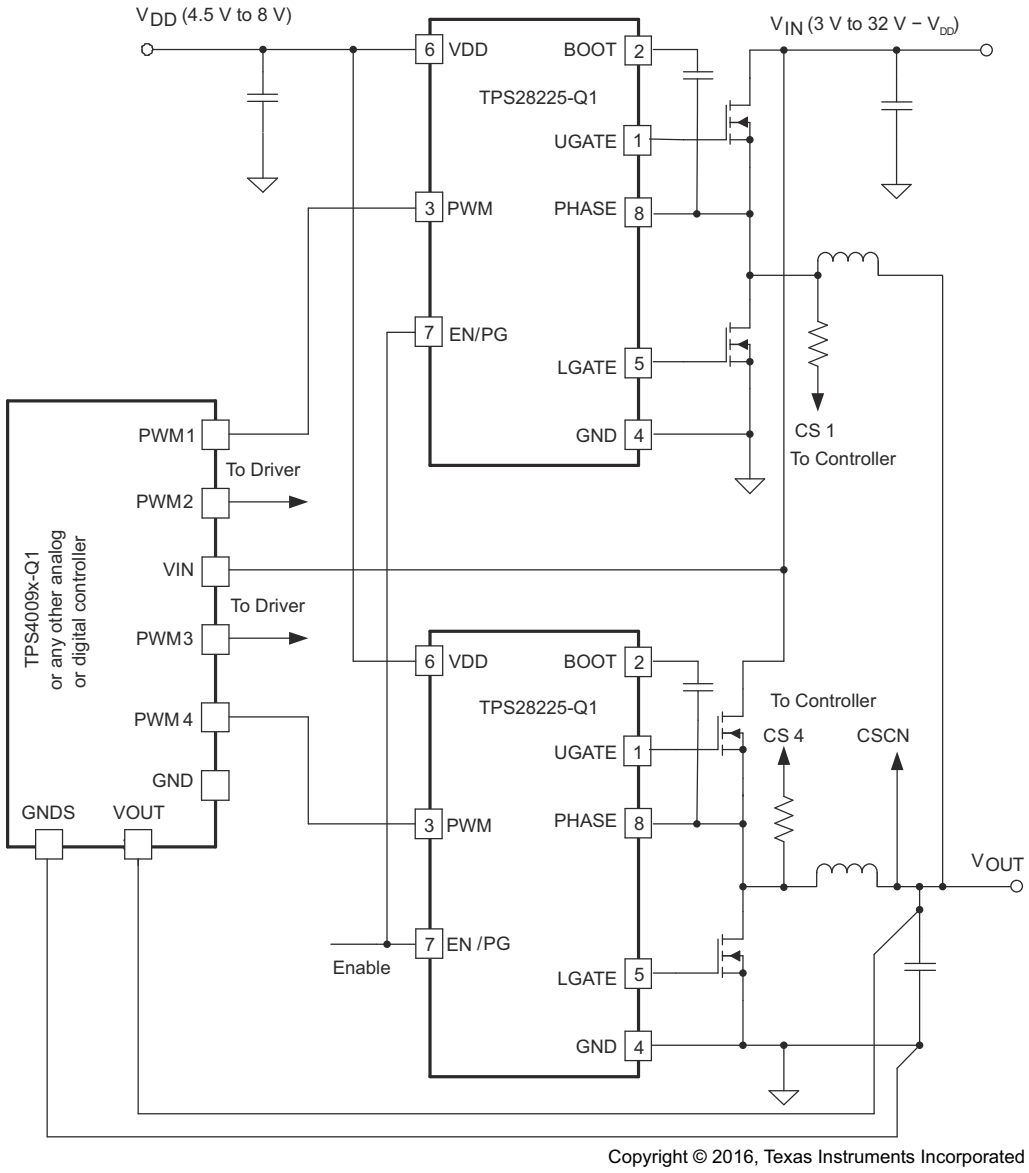


図 8-2. Multi-Phase Synchronous Buck Converter

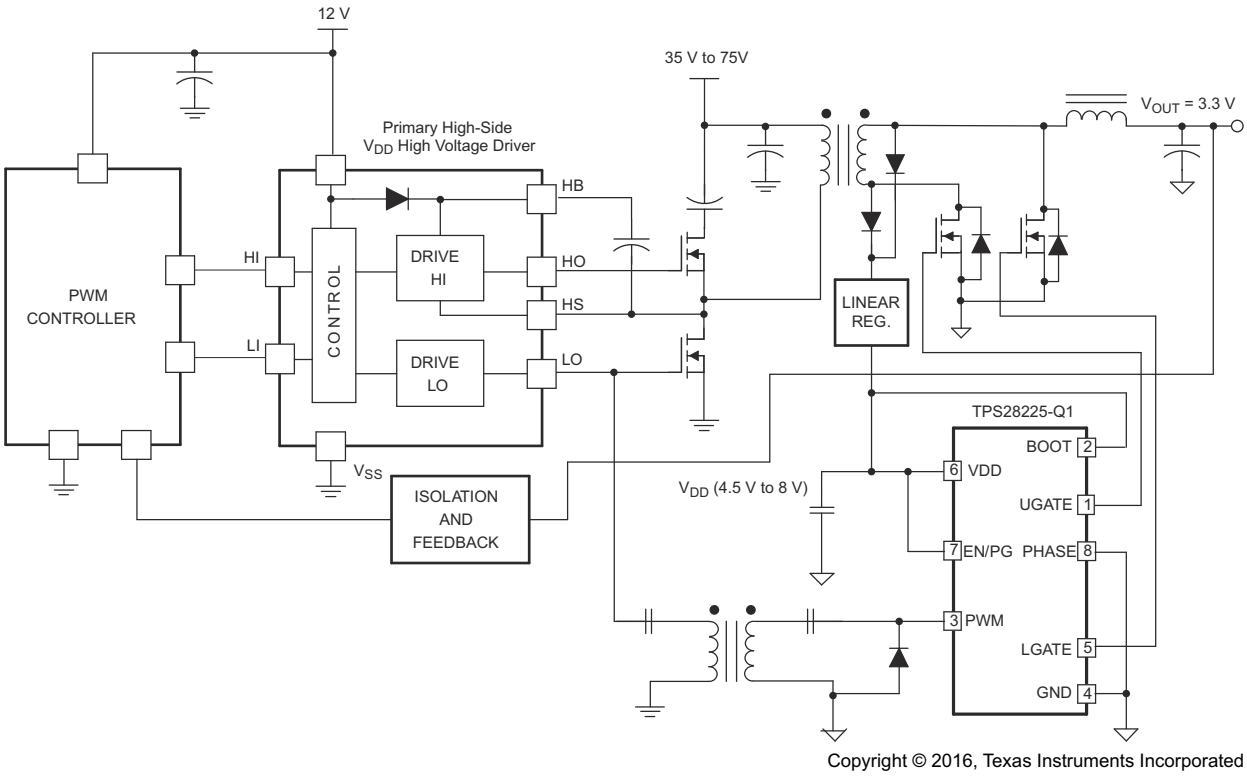


図 8-3. Driver for Synchronous Rectification with Complementary Driven MOSFETs

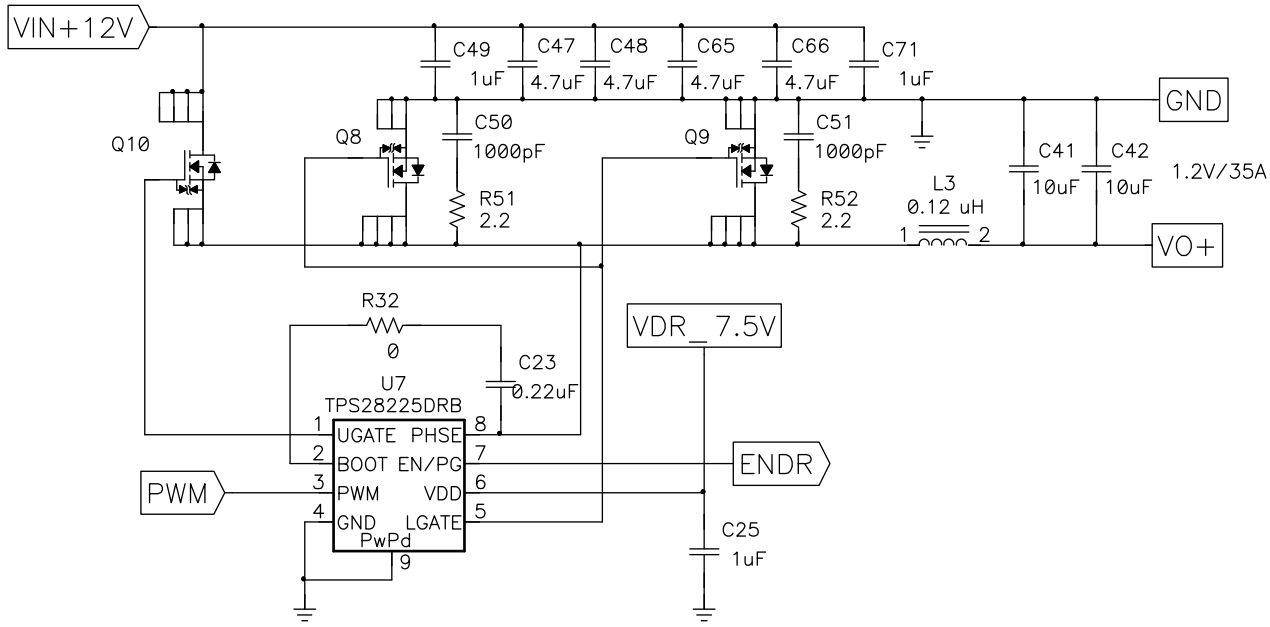
8.2.1 Design Requirements

The DC-DC converter in 図 8-4 displays the schematic of the TPS28225 in a multiphase high-current step-down power supply (only one phase is shown). This example schematic uses a single high-side MOSFET and two low-side MOSFETs the latter connected in parallel. The TPS28225 is controlled by multiphase buck DC/DC controller like TPS40090-Q1. As TPS28225 has internal shoot-through protection, only one PWM control signal is required for each channel.

The VRM example schematic is capable of driving 35 A per phase. In this example it has a nominal input voltage of 12 V within a tolerance range of ±5%. The switching frequency is 500 kHz. The nominal duty cycle is 10%, therefore the low-side MOSFETs are conducting 90% of the time. By choosing lower $R_{DS(on)}$ the conduction losses of the switching elements are minimized. The TPS28225 is controlled by multiphase buck DC/DC controller like TPS40090-Q1.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Supply Voltage	12 V ± 5%
Output Voltage	0.83 V to 1.6 V
Frequency	500 kHz
Efficiency	87%
Peak-to-peak voltage on load current (0 A –90 A)	<160 mV



Additional information is available in *What MOSFET Driver Can Do to Boost the Performance of VRM Design*.

図 8-4. One of Four Phases Driven by TPS28225 Driver in 4-phase VRM Example Schematic for Efficiency Measurement

8.2.2 Detailed Design Procedure

The output component selection considers the requirement of a fast transient response. For output capacitors small capacitance values are chosen because of rapid changes of the output voltage. These changes also require an inductor with low inductance. Due to the small duty cycle the low-side MOSFETs conduct a long time. Two low-side MOSFETs are selected to increase both thermal performance and efficiency.

8.2.2.1 Switching the MOSFETs

Driving the MOSFETs efficiently at high switching frequencies requires special attention to layout and the reduction of parasitic inductances. Efforts must occur at the PCB layout level to keep the parasitic inductances as low as possible. 図 8-5 shows the main parasitic inductances and current flow during turning ON and OFF of the MOSFET by charging its C_{GS} gate capacitance.

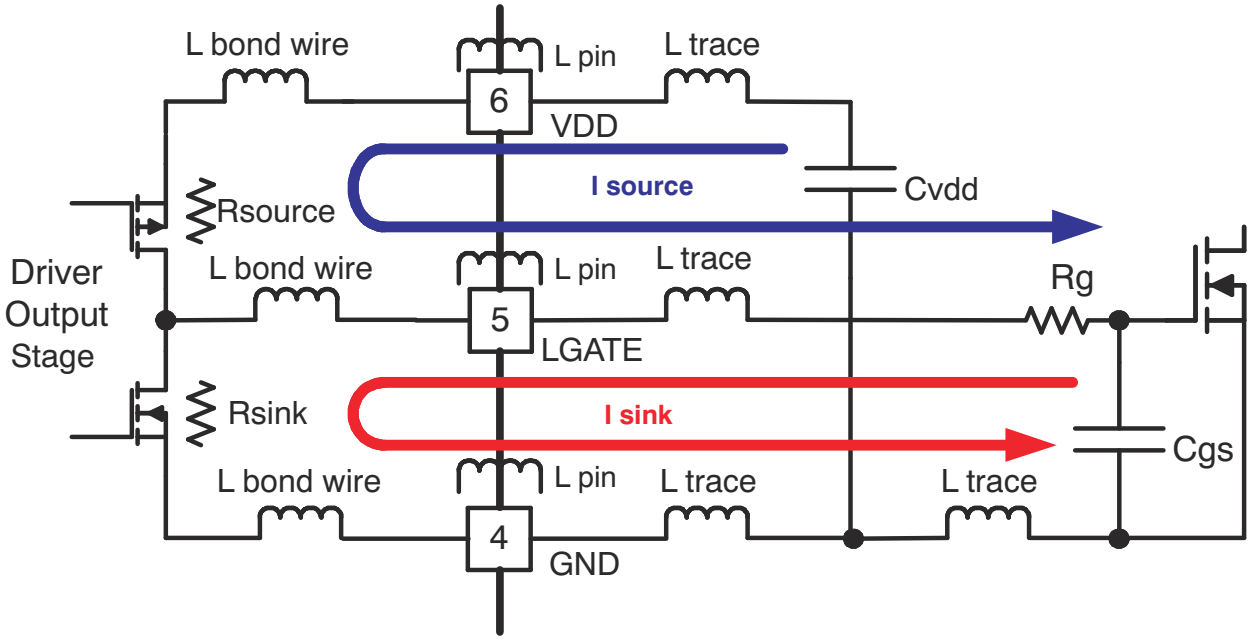


図 8-5. MOSFET Drive Paths and Main Circuit Parasitics

The I_{SOURCE} current charges the gate capacitor and the I_{SINK} current discharges it. The rise and fall time of voltage across the gate defines how quickly the MOSFET can be switched. The timing parameters specified in data sheet for both upper and lower driver are shown in 図 8-6 and 図 8-7 where 3-nF load capacitor has been used for the characterization data. Based on these actual measurements, the analytical curves in 図 8-6 and 図 8-7 show the output voltage and current of upper and low side drivers during the discharging of load capacitor. The left waveforms show the voltage and current as a function of time, while the right waveforms show the relation between the voltage and current during fast switching. These waveforms show the actual switching process and its limitations because of parasitic inductances. The static V_{OUT}/ I_{OUT} curves shown in many data sheets and specifications for the MOSFET drivers do not replicate actual switching condition and provide limited information for the user.

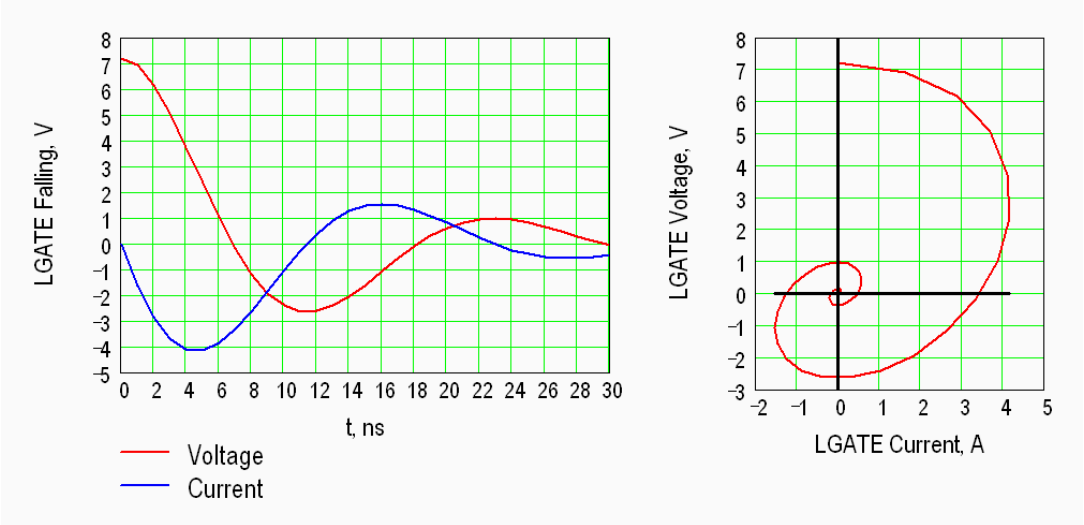


図 8-6. LGATE Turning Off Voltage and Sink Current vs Time (Related Switching Diagram [Right])

Turning Off of the MOSFET needs to be done as fast as possible to reduce switching losses. For this reason, the TPS28225-Q1 driver has very low output impedance specified as 0.4 Ω typ for lower driver and 1 Ω typ for upper driver at dc current. Assuming 8-V drive voltage and no parasitic inductances, one can expect an initial sink

current amplitude of 20 A and 8 A respectively for the lower and upper drivers. With pure R-C discharge circuit for the gate capacitor, the voltage and current waveforms are expected to be exponential. However, because of parasitic inductances, the actual waveforms have some ringing and the peak current for the lower driver is about 4 A and about 2.5 A for the upper driver (図 8-6 and 図 8-7). The overall parasitic inductance for the lower drive path is estimated as 4 nH and for the upper drive path as 6 nH. The internal parasitic inductance of the driver, which includes inductances of bonded wires and package leads, can be estimated for SOIC-8 package as 2 nH for lower gate and 4 nH for the upper gate. Use of VSON-8 package reduces the internal parasitic inductances by approximately 50%.

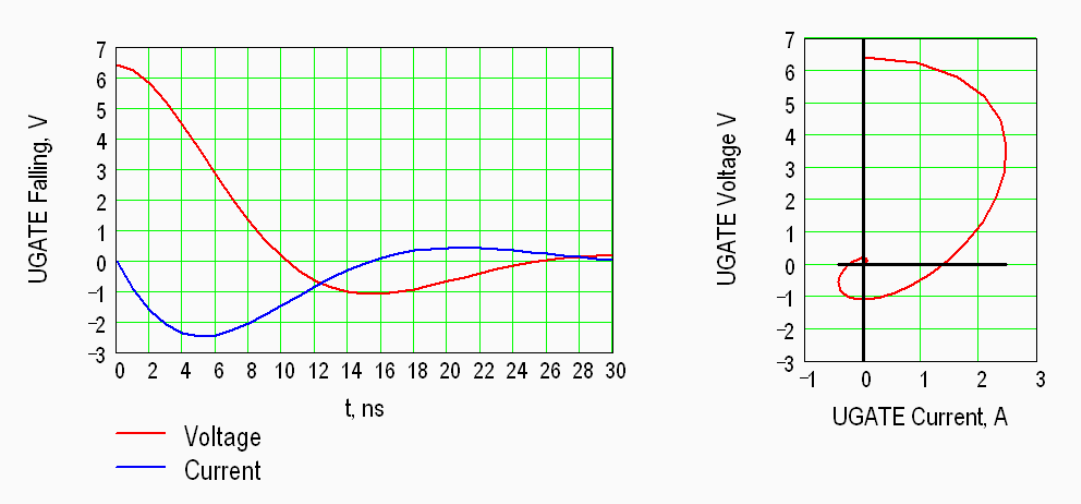


図 8-7. UGATE Turning Off Voltage and Sink Current vs Time (Related Switching Diagram [Right])

8.2.3 Application Curves

Example is the same for the TPS28225-Q1. The efficiency in this example was achieved using TPS28225 driver with 8-V drive at different switching frequencies as in 図 8-4 is shown in 図 8-8, 図 8-9, 図 8-10, 図 8-11, and 図 8-12.

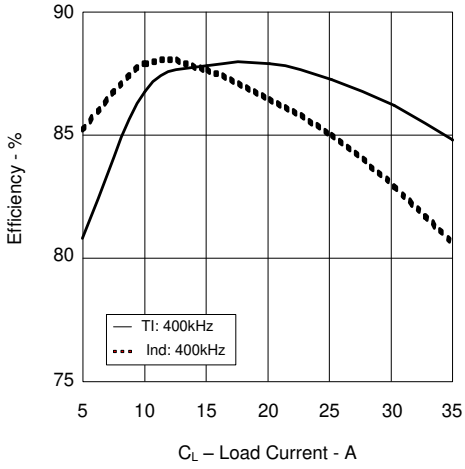


図 8-8. Efficiency vs Load Current

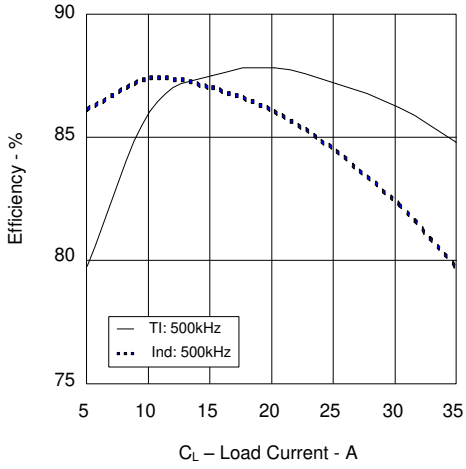


図 8-9. Efficiency vs Load Current

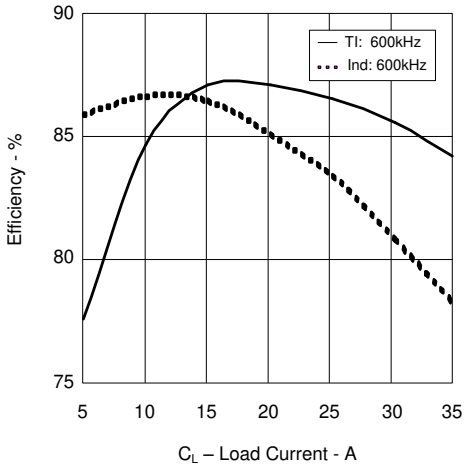


図 8-10. Efficiency vs Load Current

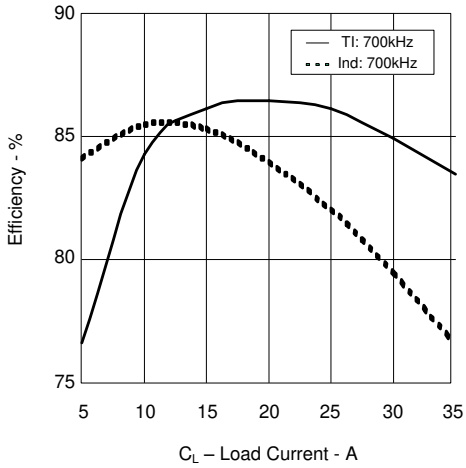


図 8-11. Efficiency vs Load Current

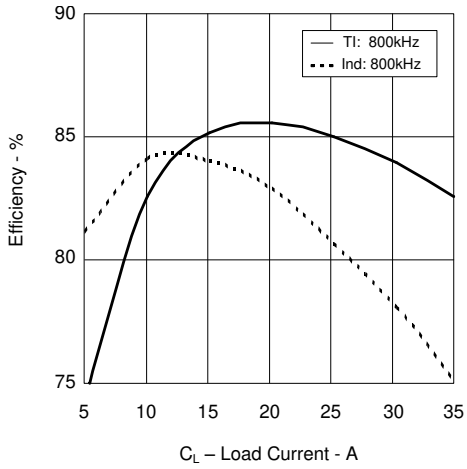
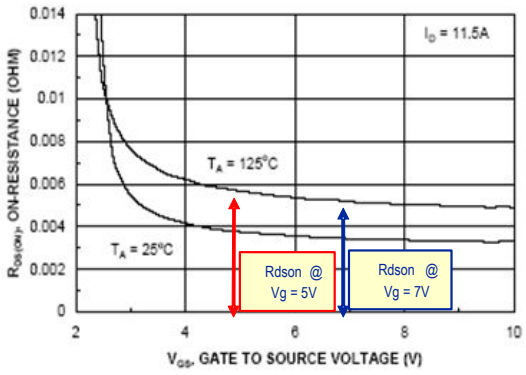


図 8-12. Efficiency vs Load Current

When using the same power stage in 図 8-4, the driver with the optimal drive voltage and optimal dead time can boost efficiency up to 5%. The optimal 8-V drive voltage versus 5-V drive contributes 2% to 3% efficiency increase and the remaining 1% to 2% can be attributed to the reduced dead time. The 7-V to 8-V drive voltage is optimal for operation at switching frequency range above 400 kHz and can be illustrated by observing typical $R_{DS(on)}$ curves of modern FETs as a function of their gate drive voltage. This is shown in 図 8-13.



On-Resistance Variation with Gate-to-Source Voltage

図 8-13. $R_{DS(on)}$ of MOSFET as Function of V_{GS}

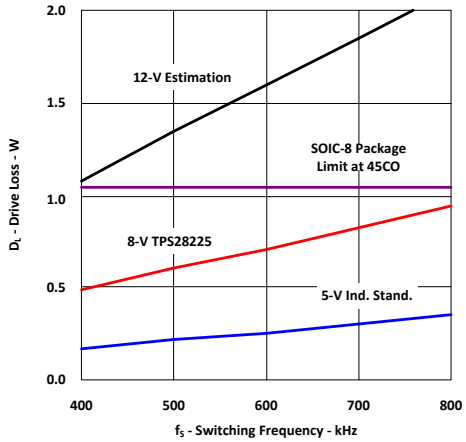


図 8-14. Drive Power as Function of V_{GS} and F_{SW}

図 8-13 and 図 8-14 show that the $R_{DS(on)}$ at 5-V drive is substantially larger than at 7 V and above that the $R_{DS(on)}$ curve is almost flat. This means that moving from 5-V drive to an 8-V drive boosts the efficiency because of lower $R_{DS(on)}$ of the MOSFETs at 8 V. Further increase of drive voltage from 8 V to 12 V only slightly decreases the conduction losses but the power dissipated inside the driver increases dramatically (by 125%). The power dissipated by the driver with 5-V, 8-V, and 12-V drive as a function of switching frequency from 400 kHz to 800 kHz. It should be noted that the 12-V driver exceeds the maximum dissipated power allowed for an SOIC-8 package even at 400-kHz switching frequency.

9 Power Supply Recommendations

The supply voltage range for operation is 4.5 to 8 V. The lower end of this range is governed by the under-voltage lockout thresholds. The UVLO disables the driver and keeps the power FETs OFF when V_{DD} is too low. A lows ESR ceramic decoupling capacitor in the range of 0.22 µF to 4.7 µF between V_{DD} and GND is recommended.

10 Layout

10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules need to be followed.

- Place the driver as close as possible to the MOSFETs.
- Place the V_{DD} and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. Use the thermal pad of the DFN-8 package as the GND by connecting it to the GND pin. The GND trace or pad from the driver goes directly to the source of the MOSFET but should not include the high current path of the main current flowing through the drain and source of the MOSFET.
- Use a similar rule for the PHASE node as for the GND.
- Use wide traces for UGATE and LGATE closely following the related PHASE and GND traces. Eighty to 100 mils width is preferable where possible.
- Use at least 2 or more vias if the MOSFET driving trace needs to be routed from one layer to another. For the GND the number of vias are determined not only by the parasitic inductance but also by the requirements for the thermal pad.
- Avoid PWM and enable traces going close to the PHASE node and pad where high dV/dT voltage can induce significant noise into the relatively high impedance leads.

It should be taken into account that poor layout can cause 3% to 5% less efficiency versus a good layout design and can even decrease the reliability of the whole system.

10.2 Layout Example

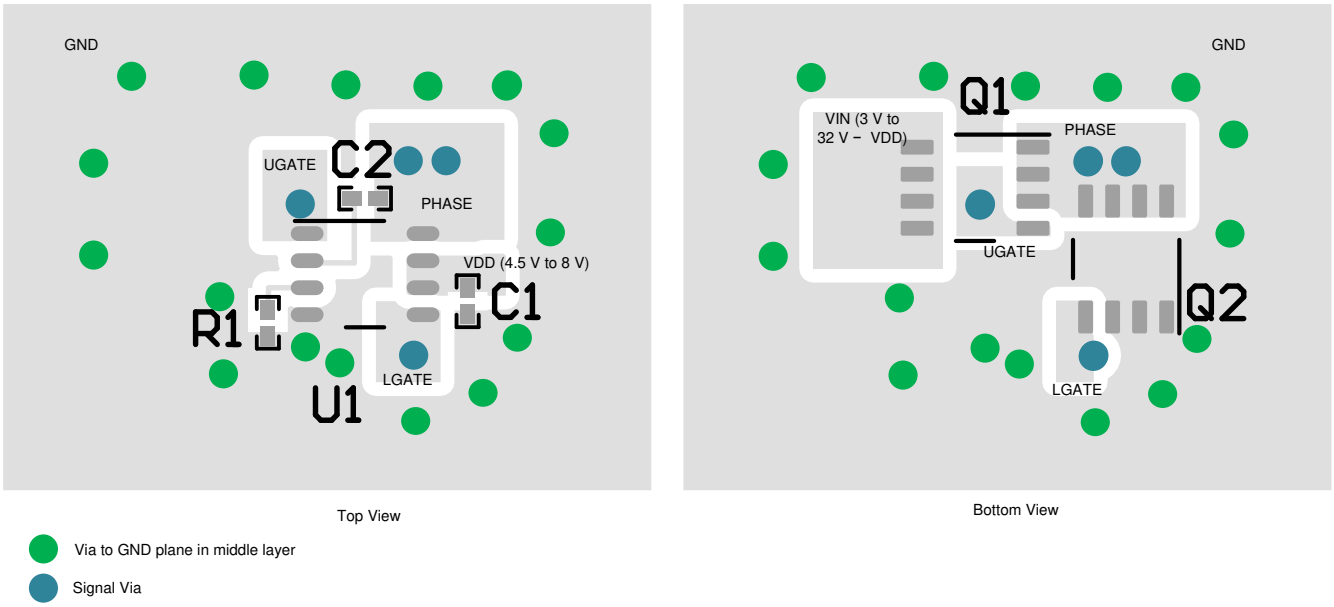


図 10-1. Layout Example Using TPS28225-Q1

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *High-Frequency Multiphase Controller*
- *What MOSFET Driver Can Do to Boost the Performance of VRM Design*, Power Electronics Technology Exhibition and Conference (Miftakhutdinov 2006)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document. section

11.4 サポート・リソース

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS28225TDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	PXND
TPS28225TDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	PXND
TPS28225TDRBRQ1.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	PXND
TPS28225TDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	28225T
TPS28225TDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	28225T
TPS28225TDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	28225T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS28225-Q1 :

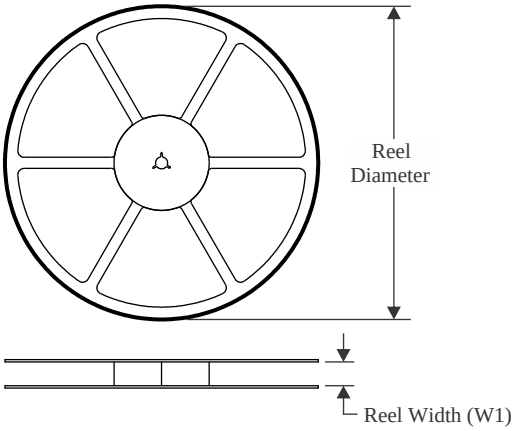
- Catalog : TPS28225

NOTE: Qualified Version Definitions:

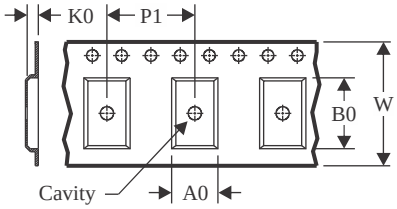
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

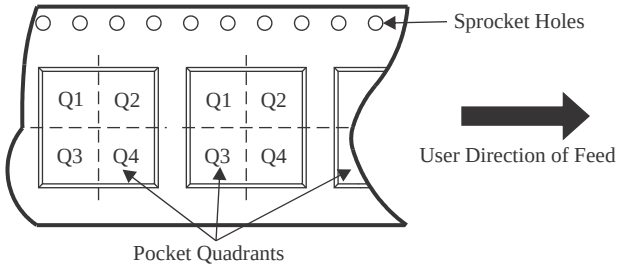


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

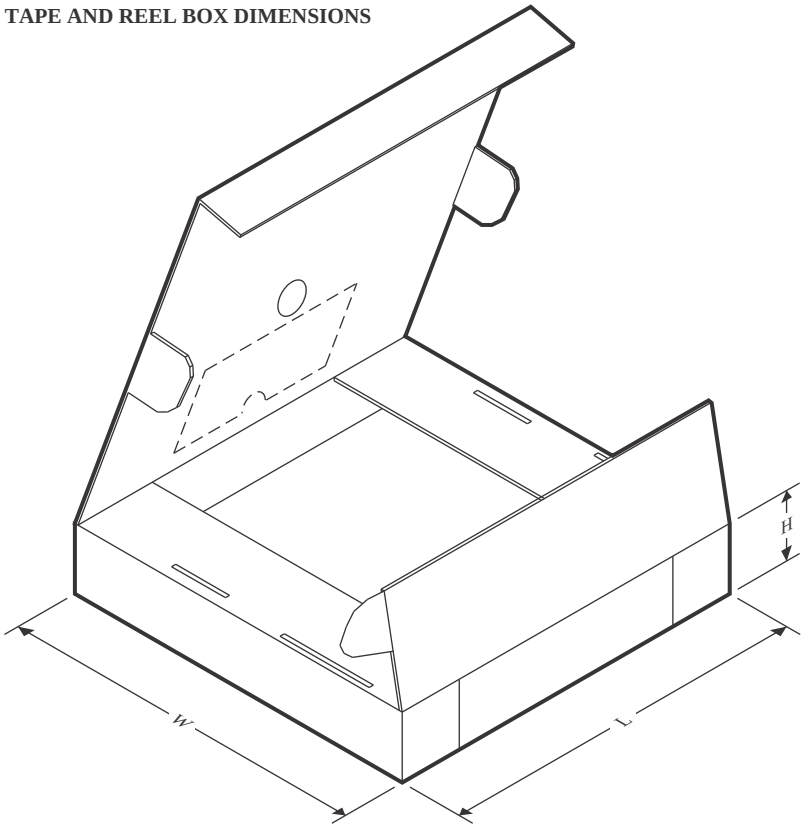
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS28225TDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS28225TDRBRQ1	SON	DRB	8	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

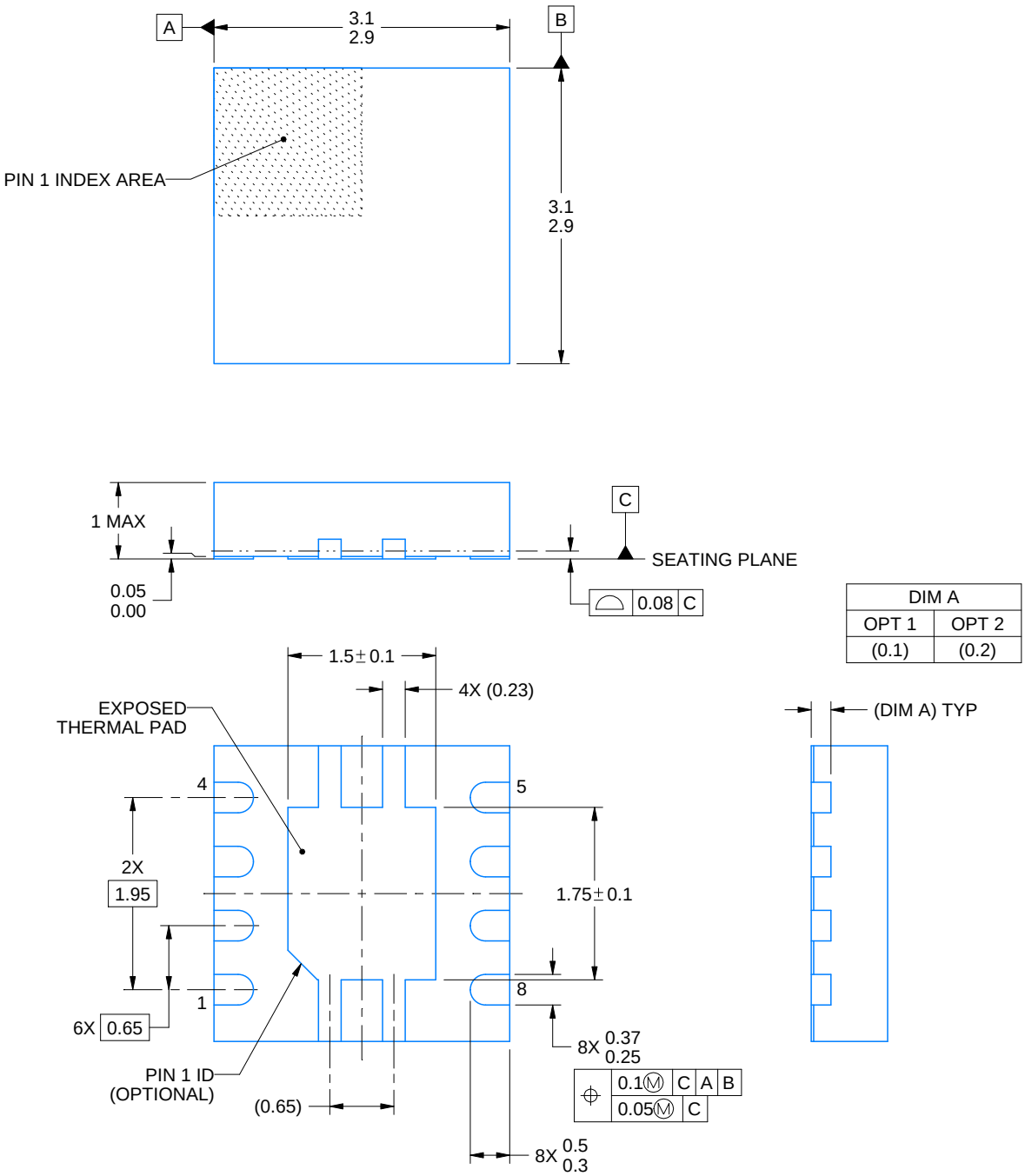
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

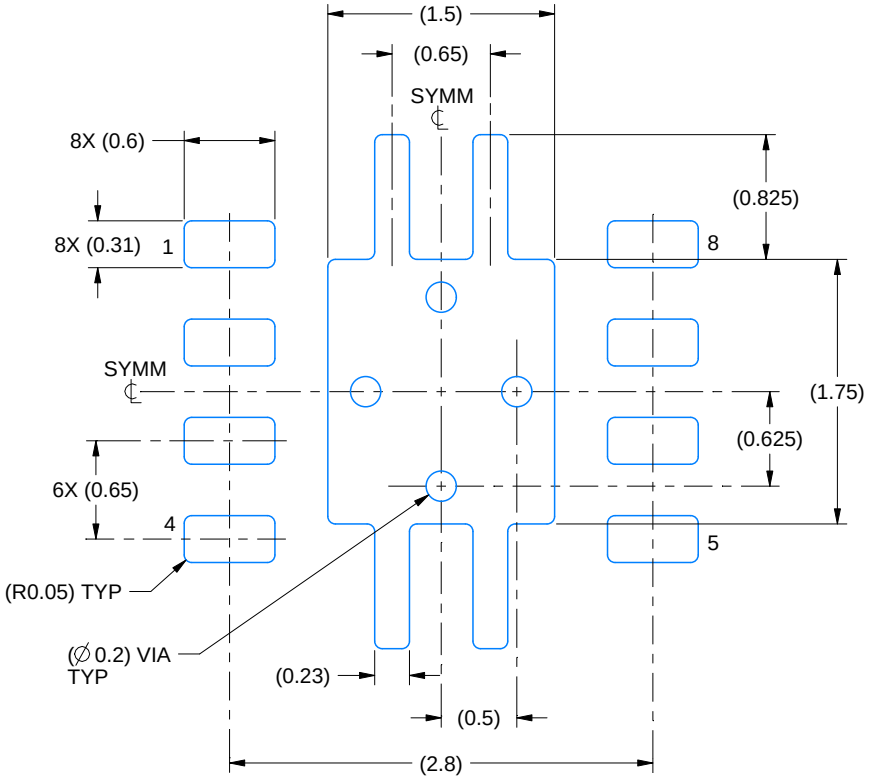
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

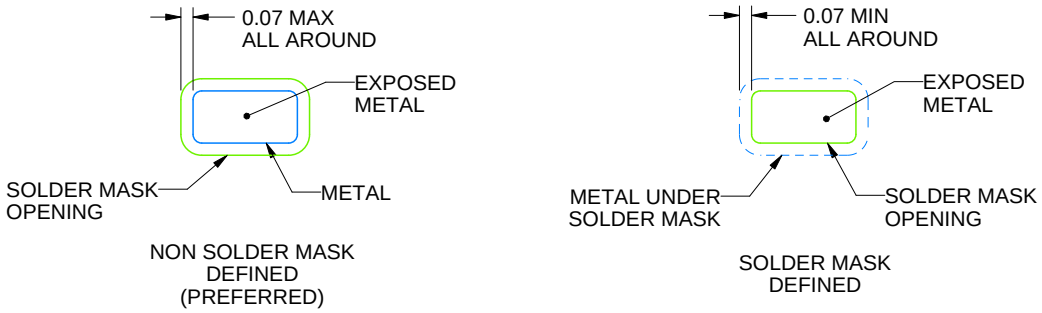
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

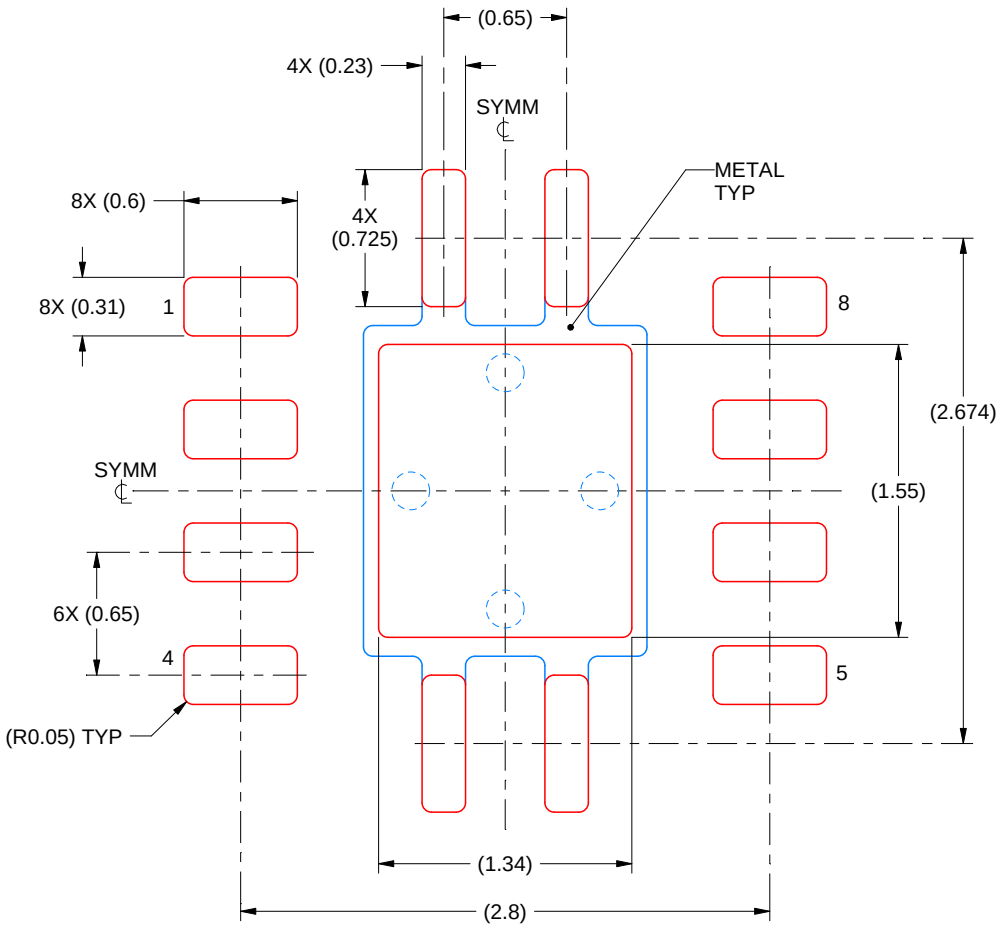


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



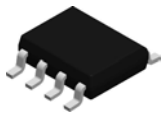
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

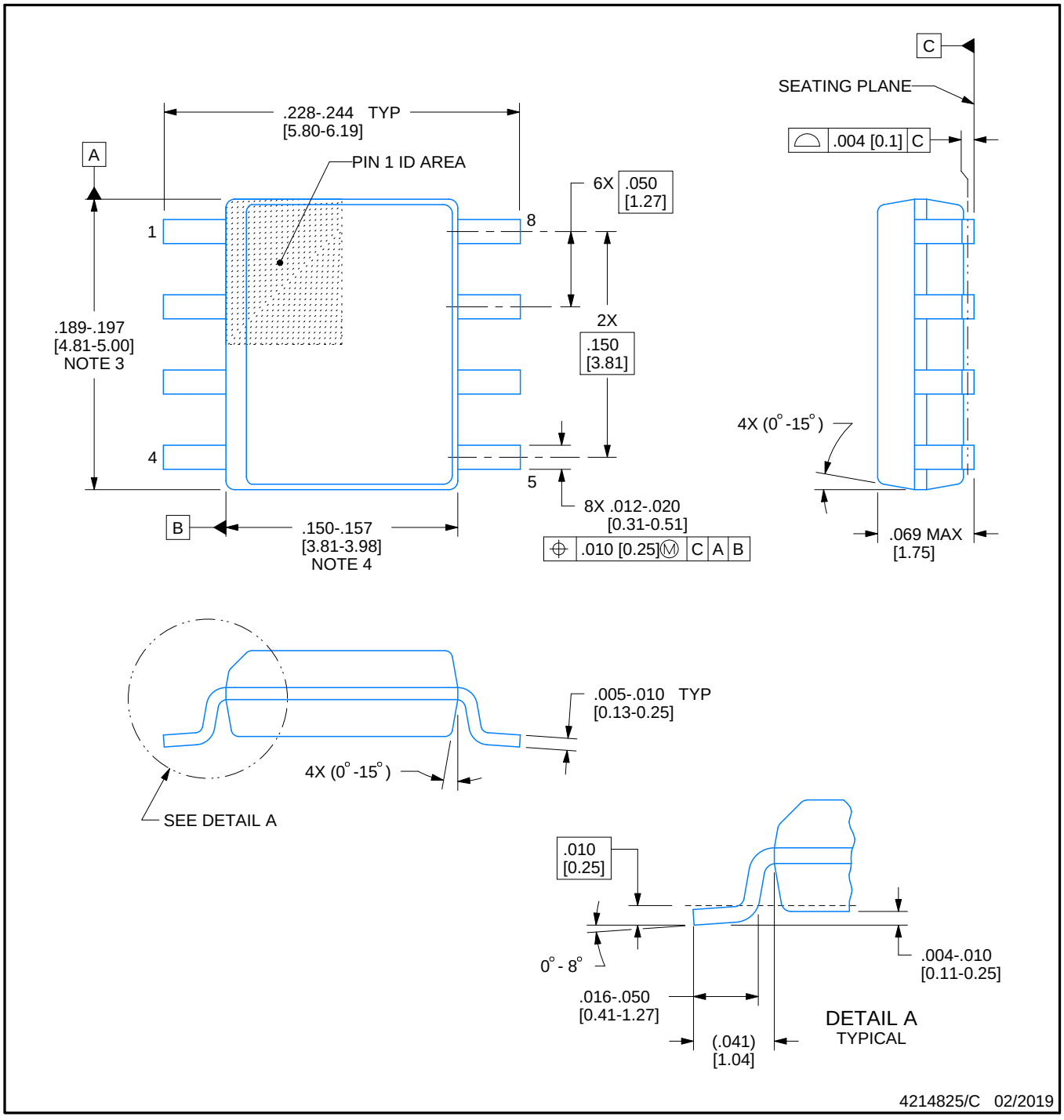


PACKAGE OUTLINE

D0008A

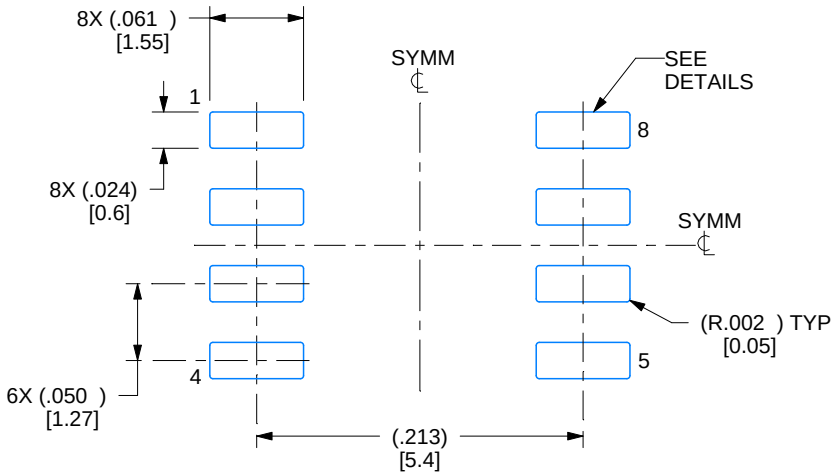
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

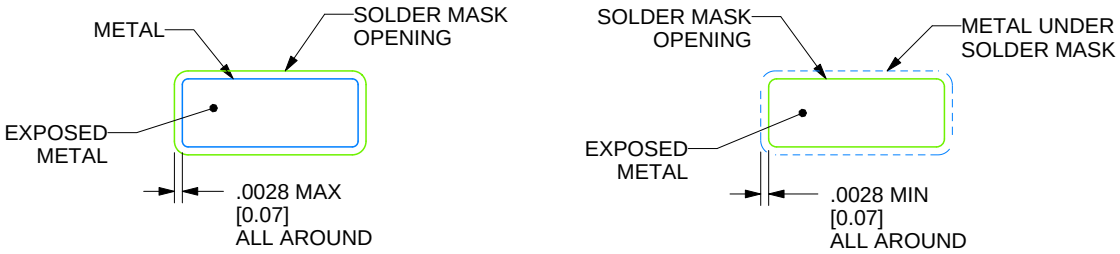


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

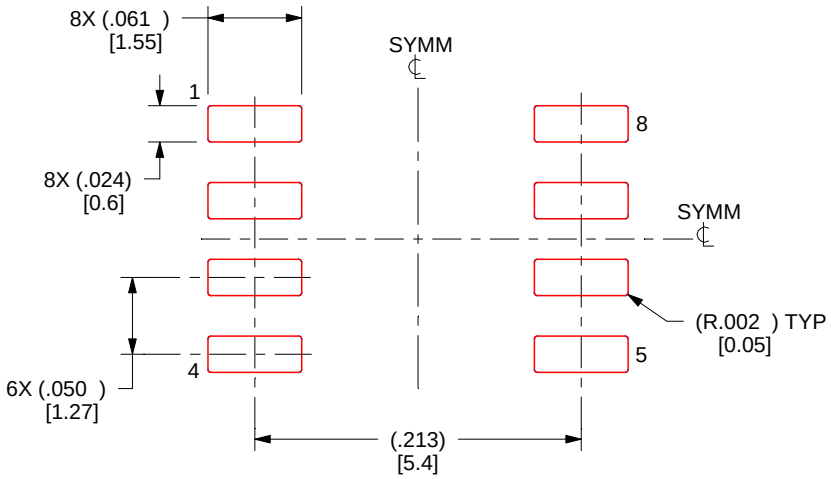
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月