

TPS28225 高周波、4A シンク、同期 MOSFET ドライバ

1 特長

- 14ns の適応型デッド タイムで 2 個の N チャネル MOSFET を駆動
- 広いゲート駆動電圧範囲: 4.5V ~ 8.8V (7V ~ 8V で最大効率)
- 広いパワー システムトレイン入力電圧範囲: 3V ~ 27V
- 広い入力 PWM 信号範囲: 2.0V ~ 13.2V 振幅
- 1 相あたり 40A 以上の電流で MOSFET を駆動可能
- 高周波動作: 14ns の伝搬遅延と 10ns の立ち上がり / 立ち下がり時間により、 $F_{SW} = 2\text{MHz}$ が可能
- 30ns 未満の入力 PWM パルスを伝播可能
- ローサイドドライバのシンク オン抵抗 (0.4Ω) により、 dV/dt に起因する貫通電流を防止
- 3 ステート PWM 入力による電源段のシャットダウン
- イネーブル(入力)信号とパワー グッド(出力)信号を同じピンに割り当てることでスペースを節約
- サーマル シャットダウン
- UVLO 保護
- 内部ブートストラップ ダイオード
- 経済的な SOIC-8 および放熱強化された 3mm × 3mm VSON-8 パッケージ
- 一般的な 3 ステート入力ドライバを高性能で置き換え可能

2 アプリケーション

- アナログまたはデジタル制御の多相 DC-DC コンバータ
- デスクトップ/サーバー VRM および EVRD
- ポータブルおよびノートブック用レギュレータ
- 絶縁型電源の同期整流

3 概要

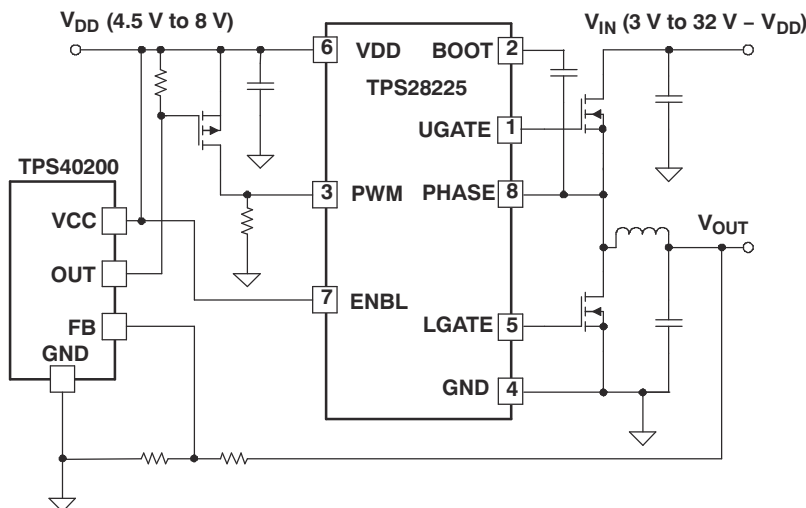
TPS28225 は、適応型デッド タイム制御機能を備えた、N チャネル相補型パワー MOSFET 用の高速ドライバです。さまざまな種類の 1 相および多相の高電流 DC-DC コンバータとともに使用できるよう最適化されています。TPS28225 は、高効率、小型、低 EMI 放射を実現するソリューションです。

この効率は、最大 8.8V のゲート駆動電圧、14ns の適応型デッド タイム制御、14ns の伝播遅延、2A ソースおよび 4A シンクの高電流駆動能力によって実現されています。ローサイド ゲートドライバの 0.4Ω のインピーダンスによってパワー MOSFET のゲートをスレッショルド未満に保持し、高い dV/dt 位相ノード遷移で貫通電流が生じないようにしています。内部ダイオードによって充電されるブートストラップ コンデンサにより、N チャネル MOSFET をハーフブリッジ構成で使用することができます。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
TPS28225	D (SOIC 8)	4.90mm × 3.91mm
	DRB (VSON 8)	3.00mm × 3.00mm

(1) 供給されているすべてのパッケージについては、[セクション 12](#) を参照してください。



概略回路図



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4 Pin Configuration and Functions

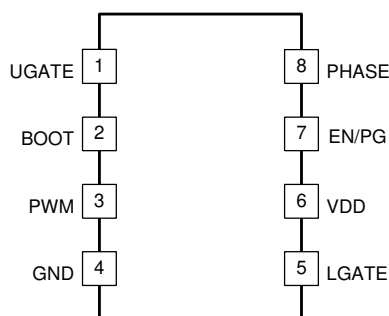


図 4-1. D Package 8-Pin SOIC Top View

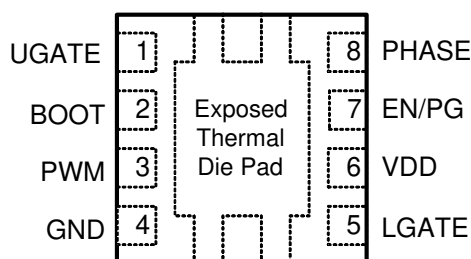


図 4-2. DRB Package 8-Pin VSON Top View

表 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOIC	VSON		
BOOT	2	2	I/O	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the Phase pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
EN/PG	7	7	I/O	Enable/power good input/output pin with 1-MΩ impedance. Connect this pin to High to enable and Low to disable the device. When disabled, the device draws less than 350-μA bias current. If the V _{DD} is below UVLO threshold or over temperature shutdown occurs, this pin is internally pulled low.
GND	4	4	–	Ground pin. All signals are referenced to this node.
LGATE	5	5	O	Lower gate drive sink and source output. Connect to the gate of the low-side power N-Channel MOSFET.
PHASE	8	8	I	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.
PWM	3	3	I	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the 3-state PWM Input section under DETAILED DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
Thermal pad		Exposed die pad	–	Connect directly to the GND for better thermal performance and EMI.
UGATE	1	1	O	Upper gate drive sink/source output. Connect to gate of high-side power N-Channel MOSFET.
VDD	6	6	I	Connect this pin to a 5-V bias supply. Place a high quality bypass capacitor from this pin to GND.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

		MIN	MAX	UNIT
Input supply voltage range, V_{DD} ⁽²⁾		−0.3	8.8	V
Boot voltage, V_{BOOT}		−0.3	33	V
Phase voltage, V_{PHASE}	DC	−2	32 or $V_{BOOT} + 0.3 - V_{DD}$ whichever is less	V
	Pulse < 400 ns, E = 20 μ J	−7	33.1 or $V_{BOOT} + 0.3 - V_{DD}$ whichever is less	V
Input voltage range, V_{PWM} , $V_{EN/PG}$		−0.3	13.2	V
Output voltage range, V_{UGATE}		$V_{PHASE} - 0.3$	$V_{BOOT} + 0.3$, ($V_{BOOT} - V_{PHASE} < 8.8$)	V
	Pulse < 100 ns, E = 2 μ J	$V_{PHASE} - 2$	$V_{BOOT} + 0.3$, ($V_{BOOT} - V_{PHASE} < 8.8$)	V
Output voltage range, V_{LGATE}		−0.3	$V_{DD} + 0.3$	V
	Pulse < 100 ns, E = 2 μ J	−2	$V_{DD} + 0.3$	V
Continuous total power dissipation		See セクション 5.4		
Operating virtual junction temperature range, T_J		−40	150	°C
Lead temperature (soldering, 10 sec.)			300	°C
Storage temperature, T_{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Data book for thermal limitations and considerations of packages.
- (3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input supply voltage	4.5	7.2	8	V
V_{IN}	Power input voltage	3	32 V– V_{DD}		V
T_J	Operating junction temperature range	−40		125	°C

5.4 Thermal Information

THERMAL METRIC		TPS28225		UNIT
		VSON (DRB)	SOIC (D)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.2	123.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.5	77.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.9	63.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	27.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.0	63.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.5	N/A	°C/W

5.5 Electrical Characteristics

$V_{DD} = 7.2\text{ V}$, EN/PG pulled up to V_{DD} by 100-k Ω resistor, $T_A = T_J = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
UNDER VOLTAGE LOCKOUT						
	Rising threshold	$V_{PWM} = 0\text{ V}$	3.2	3.5	3.8	V
	Falling threshold	$V_{PWM} = 0\text{ V}$	2.7	3.0		V
	Hysteresis			0.5		V
BIAS CURRENTS						
$I_{DD(off)}$	Bias supply current	$V_{EN/PG} = \text{low}$, PWM pin floating		350		μA
I_{DD}	Bias supply current	$V_{EN/PG} = \text{high}$, PWM pin floating		500		μA
INPUT (PWM)						
I_{PWM}	Input current	$V_{PWM} = 5\text{ V}$		185		μA
		$V_{PWM} = 0\text{ V}$		–200		μA
	PWM 3-state rising threshold ⁽²⁾			1.0		V
	PWM 3-state falling threshold	$V_{PWM\text{ PEAK}} = 5\text{ V}$	3.4	3.8	4.0	V
t_{HLD_R}	3-state shutdown Hold-off time			250		ns
T_{MIN}	PWM minimum pulse to force U_{GATE} pulse	$C_L = 3\text{ nF}$ at U_{GATE} , $V_{PWM} = 5\text{ V}$		30		ns
ENABLE/POWER GOOD (EN/PG)						
	Enable high rising threshold	PG FET OFF		1.7	2.1	V
	Enable low falling threshold	PG FET OFF	0.8	1.0		V
	Hysteresis		0.35	0.70		V
	Power good output	$V_{DD} = 2.5\text{ V}$			0.2	V
UPPER GATE DRIVER OUTPUT (UGATE)						
	Source resistance	500 mA source current		1.0	2.0	Ω
	Source current ⁽²⁾	$V_{UGATE\text{-}PHASE} = 2.5\text{ V}$		2.0		A
t_{RU}	Rise time	$C_L = 3\text{ nF}$		10		ns
	Sink resistance	500 mA sink current		1.0	2.0	Ω
	Sink current ⁽²⁾	$V_{UGATE\text{-}PHASE} = 2.5\text{ V}$		2.0		A
t_{FU}	Fall time	$C_L = 3\text{ nF}$		10		ns

5.5 Electrical Characteristics (続き)

$V_{DD} = 7.2\text{ V}$, EN/PG pulled up to V_{DD} by 100-k Ω resistor, $T_A = T_J = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
LOWER GATE DRIVER OUTPUT (LGATE)					
Source resistance	500 mA source current		1.0	2.0	Ω
Source current ⁽²⁾	$V_{LGATE} = 2.5\text{ V}$		2.0		A
t_{RL} Rise time ⁽²⁾	$C_L = 3\text{ nF}$		10		ns
Sink resistance	500 mA sink current		0.4	1.0	Ω
Sink current ⁽²⁾	$V_{LGATE} = 2.5\text{ V}$		4.0		A
Fall time ⁽²⁾	$C_L = 3\text{ nF}$		5		ns
BOOTSTRAP DIODE					
V_F Forward voltage	Forward bias current 100 mA		1.0		V
THERMAL SHUTDOWN					
Rising threshold ⁽²⁾		150	160	170	$^\circ\text{C}$
Falling threshold ⁽²⁾		130	140	150	$^\circ\text{C}$
Hysteresis			20		$^\circ\text{C}$

(1) Typical values for $T_A = 25^\circ\text{C}$

(2) Not production tested.

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING TIME					
t_{DLU} UGATE turn-off propagation Delay	$C_L = 3\text{ nF}$		14		ns
t_{DLL} LGATE turn-off propagation Delay	$C_L = 3\text{ nF}$		14		ns
t_{DTU} Dead time LGATE turn off to UGATE turn on	$C_L = 3\text{ nF}$		14		ns
t_{DTL} Dead time UGATE turn off to LGATE turn on	$C_L = 3\text{ nF}$		14		ns

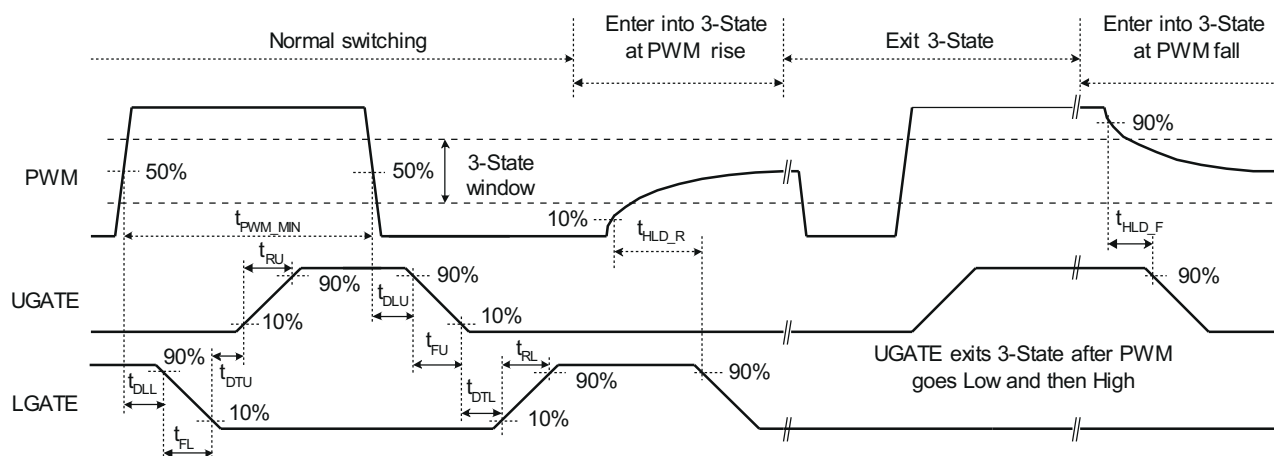
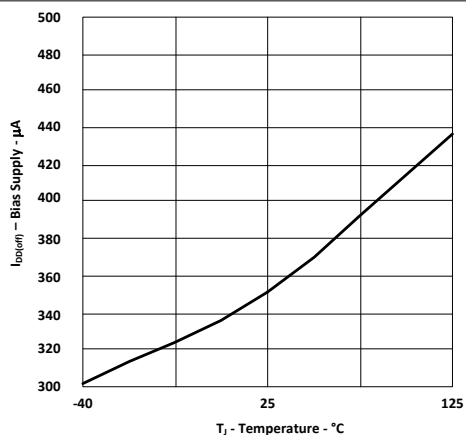
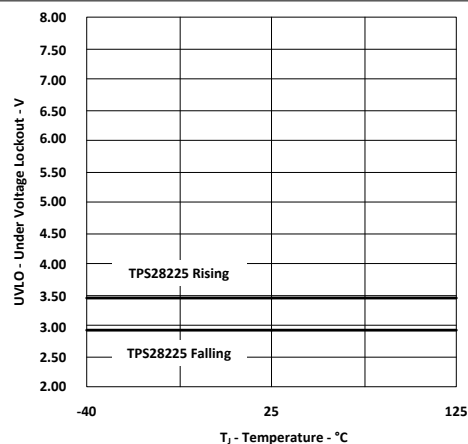


図 5-1. TPS28225 Timing Diagram

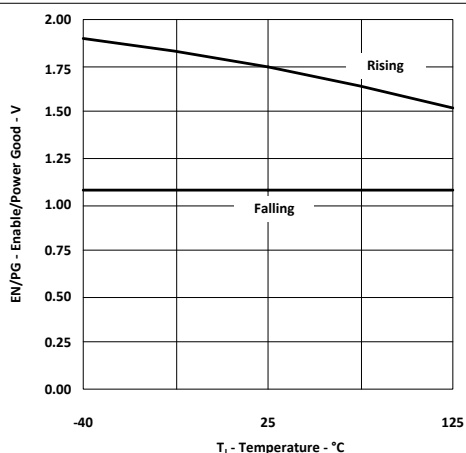
5.7 Typical Characteristics



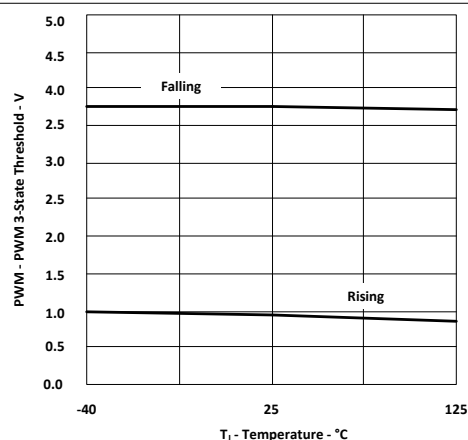
5-2. Bias Supply Current vs Temperature



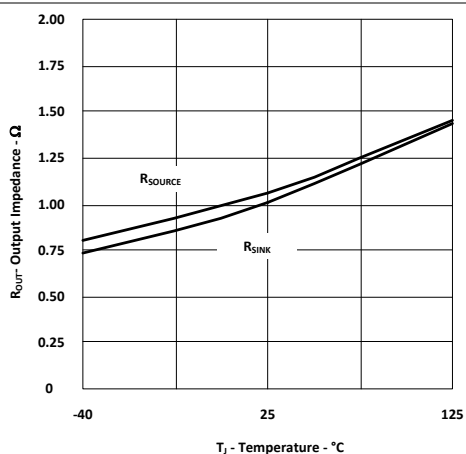
5-3. Undervoltage Lockout Threshold vs Temperature



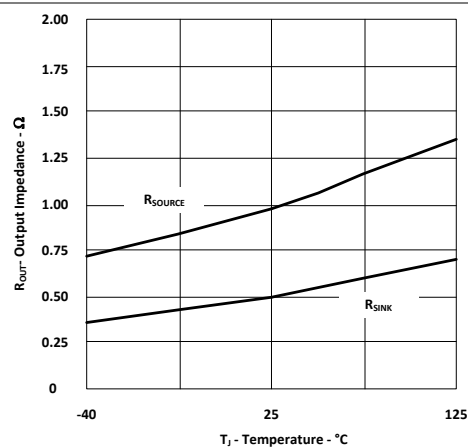
5-4. Enable/Power Good Threshold vs Temperature



5-5. PWM 3-State Thresholds, (5-V Input Pulses) vs Temperature



5-6. UGATE DC Output Impedance vs Temperature



5-7. LGATE DC Output Impedance vs Temperature

5.7 Typical Characteristics (continued)

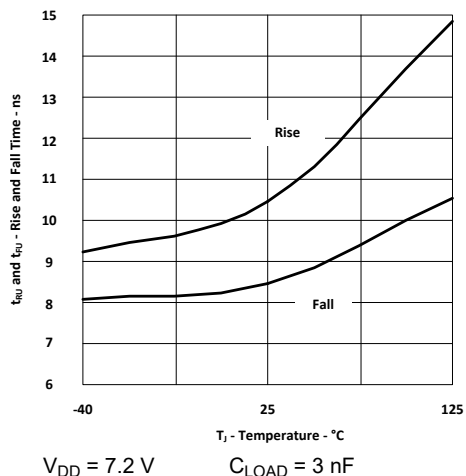


図 5-8. UGATE Rise and Fall Time vs Temperature

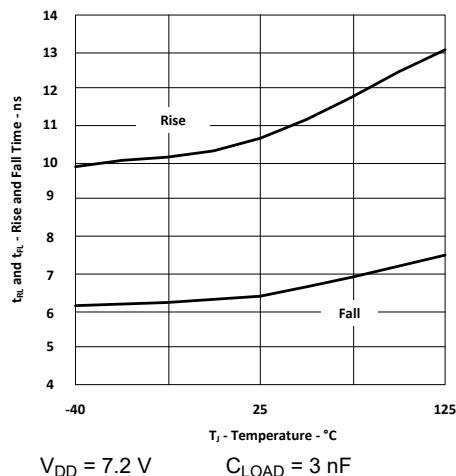


図 5-9. LGATE Rise and Fall Time vs Temperature

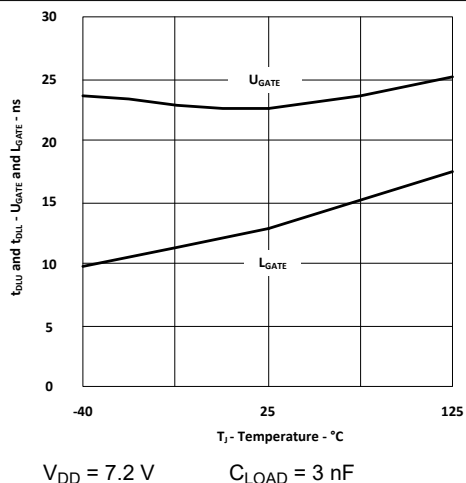


図 5-10. UGATE and LGATE (Turning OFF Propagation Delays) vs Temperature

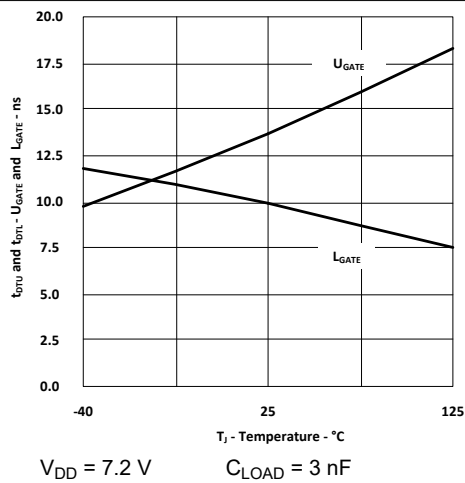


図 5-11. UGATE and LGATE (Dead Time) vs Temperature

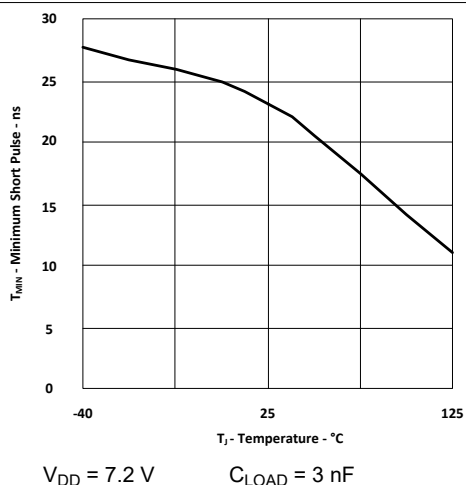


図 5-12. UGATE Minimum Short Pulse vs Temperature

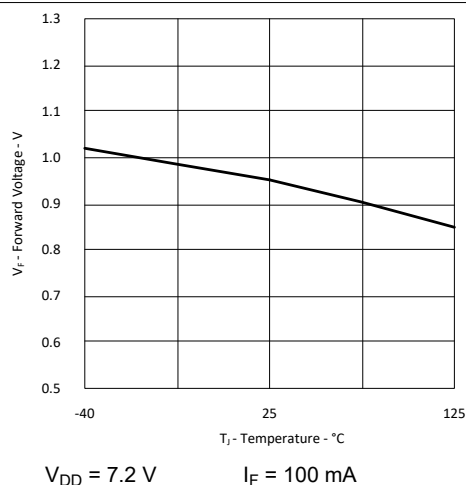
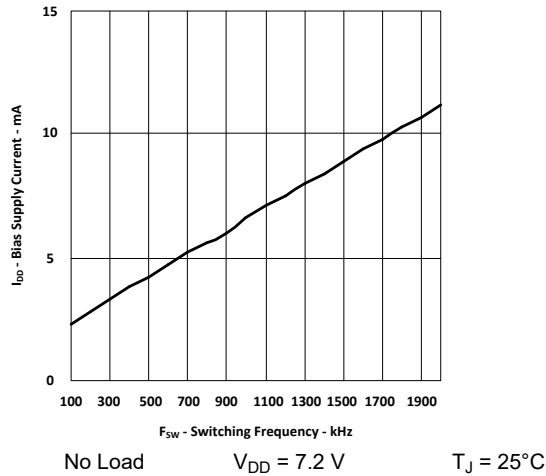
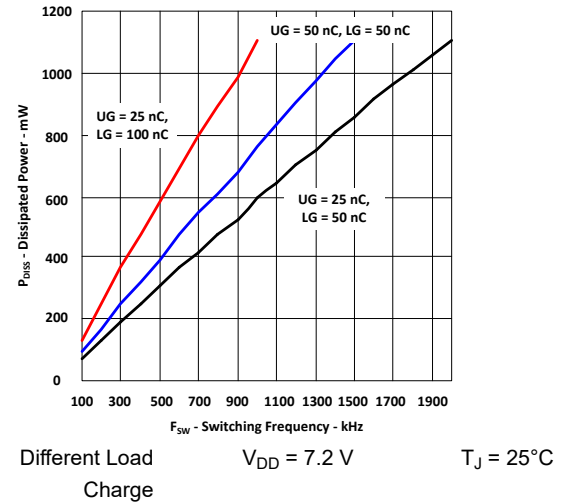


図 5-13. Bootstrap Diode Forward Voltage vs Temperature

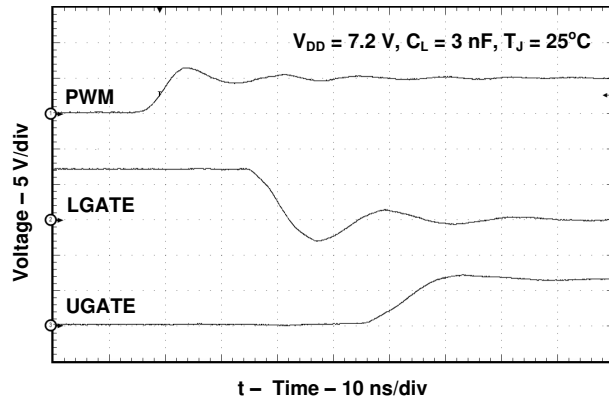
5.7 Typical Characteristics (continued)



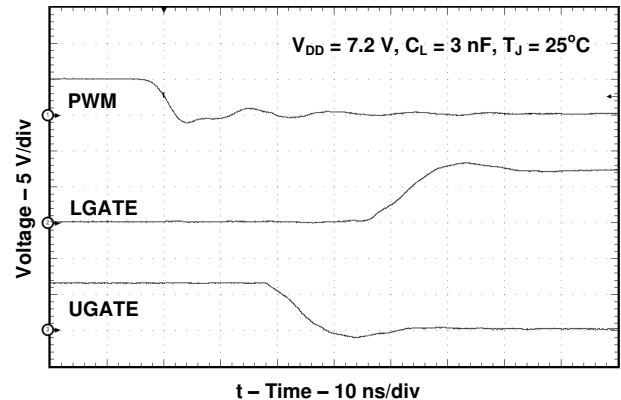
5-14. Bias Supply Current vs Switching Frequency



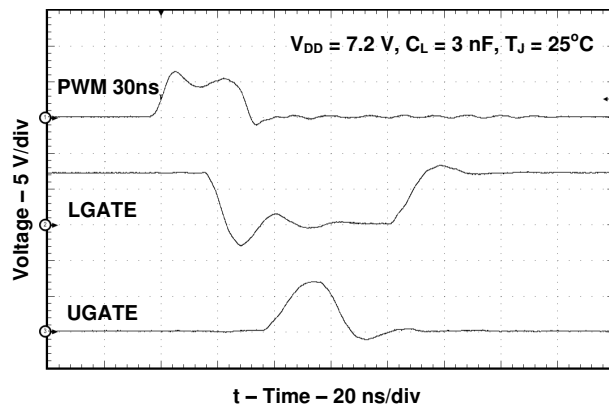
5-15. Driver Dissipated Power vs Switching Frequency



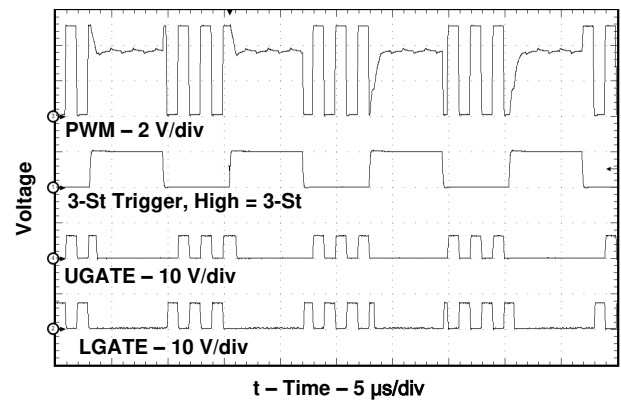
5-16. PWM Input Rising Switching Waveforms



5-17. PWM Input Falling Switching Waveforms



5-18. Minimum UGATE Pulse Switching Waveforms



5-19. Normal and 3-State Operation Enter/Exit Conditions

6 Detailed Description

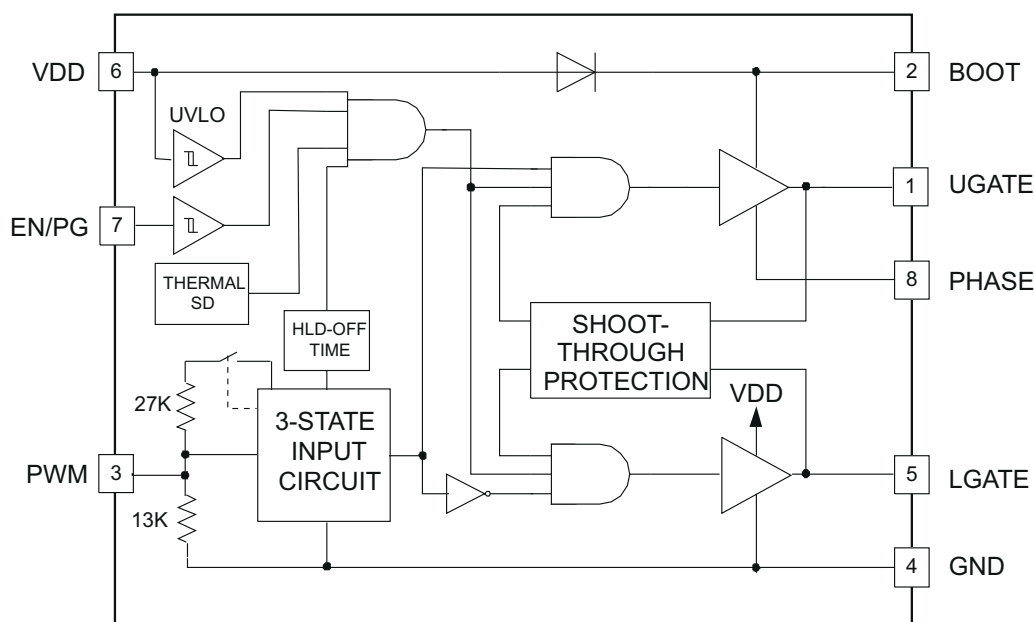
6.1 Overview

The TPS28225 features a 3-state PWM input compatible with all multi-phase controllers employing 3-state output feature. As long as the input stays within 3-state window for the 250-ns hold-off time, the driver switches both outputs low. This shutdown mode prevents a load from the reversed- output-voltage.

The other features include undervoltage lockout, thermal shutdown and two-way enable/power good signal. Systems without 3-state featured controllers can use enable/power good input/output to hold both outputs low during shutting down.

The TPS28225 is offered in an economical SOIC-8 and thermally enhanced low-size Dual Flat No-Lead (DFN-8) packages. The driver is specified in the extended temperature range of -40°C to 125°C with the absolute maximum junction temperature 150°C .

6.2 Functional Block Diagram



For the TPS28225DRB the thermal PAD on the bottom side of package must be soldered and connected to the GND pin and to the GND plane of the PCB in the shortest possible way.

6.3 Feature Description

6.3.1 Undervoltage Lockout (UVLO)

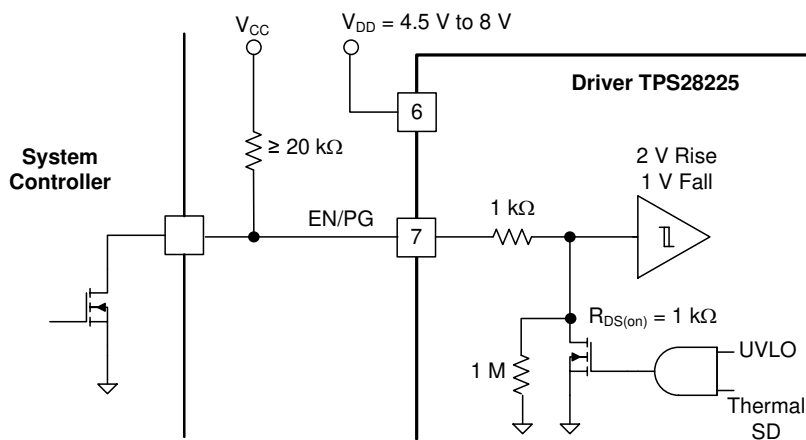
The TPS28225 incorporates an under voltage lockout circuit that keeps the driver disabled and external power FETs in an OFF state when the input supply voltage V_{DD} is insufficient to drive external power FETs reliably. During power up, both gate drive outputs remain low until voltage V_{DD} reaches UVLO threshold, typically 3.5 V. Once the UVLO threshold is reached, the condition of the gate drive outputs is defined by the input PWM and EN/PG signals. During power down the UVLO threshold is set lower, typically 3.0 V. The 0.5 V for the TPS28225 hysteresis is selected to prevent the driver from turning ON and OFF while the input voltage crosses UVLO thresholds, especially with low slew rate. The TPS28225 has the ability to send a signal back to the system controller that the input supply voltage V_{DD} is insufficient by internally pulling down the EN/PG pin. The TPS28225 releases EN/PG pin immediately after the V_{DD} has risen above the UVLO threshold.

6.3.2 Output Active Low

The output active-low circuit effectively keeps the gate outputs low even if the driver is not powered up. This prevents open-gate conditions on the external power FETs and accidental turn on when the main power-stage supply voltage is applied before the driver is powered up. For the simplicity, the output active low circuit is shown in a block diagram as the resistor connected between LGATE and GND pins with another one connected between UGATE and PHASE pins.

6.3.3 Enable/Power Good

The Enable/Power Good circuit allows the TPS28225 to follow the PWM input signal when the voltage at EN/PG pin is above 2.1 V maximum. This circuit has a unique two-way communication capability. This is illustrated by [Figure 6-1](#).



🔧 6-1. Enable/Power Good Circuit

The EN/PG pin has approximately 1-k Ω internal series resistor. Pulling EN/PG high by an external $\geq 20\text{-k}\Omega$ resistor allows two-way communication between controller and driver. If the input voltage V_{DD} is below UVLO threshold or thermal shut down occurs, the internal MOSFET pulls EN/PG pin to GND through 1-k Ω resistor. The voltage across the EN/PG pin is now defined by the resistor divider comprised by the external pull up resistor, 1-k Ω internal resistor and the internal FET having 1-k Ω $R_{DS(on)}$. Even if the system controller allows the driver to start by setting its own enable output transistor OFF, the driver keeps the voltage at EN/PG low. Low EN/PG signal indicates that the driver is not ready yet because the supply voltage V_{DD} is low or that the driver is in thermal shutdown mode. The system controller can arrange the delay of PWM input signals coming to the driver until the driver releases EN/PG pin. If the input voltage V_{DD} is back to normal, or the driver is cooled down below its lower thermal shutdown threshold, then the internal MOSFET releases the EN/PG pin and normal operation resumes under the external Enable signal applied to EN/PG input. Another feature includes an internal 1-M Ω resistor that pulls EN/PG pin low and disables the driver in case the system controller accidentally loses connection with the driver. This could happen if, for example, the system controller is located on a separate PCB daughter board.

The EN/PG pin can serve as the second pulse input of the driver additionally to PWM input. The delay between EN/PG and the UGATE going high, provided that PWM input is also high, is only about 30 ns. If the PWM input pulses are synchronized with EN/PG input, then when PWM and EN/PG are high, the UGATE is high and LGATE is low. If both PWM and EN/PG are low, then UGATE and LGATE are both low as well. This means the driver allows operation of a synchronous buck regulator as a conventional buck regulator using the body diode of the low-side power MOSFET as the freewheeling diode. This feature can be useful in some specific applications to allow startup with a pre-biased output or, to improve the efficiency of buck regulator when in power saving mode with low output current.

6.3.4 3-State Input

As soon as the EN/PG pin is set high and input PWM pulses are initiated (see Note below). The dead-time control circuit ensures that there is no overlapping between UGATE and LGATE drive outputs to eliminate shoot through current through the external power FETs. Additionally to operate under periodical pulse sequencing, the TPS28225 has a self-adjustable PWM 3-state input circuit. The 3-state circuit sets both gate drive outputs low, and thus turns the external power FETs OFF if the input signal is in a high impedance state for at least 250 ns typical. At this condition, the PWM input voltage level is defined by the internal 27-k Ω to 13-k Ω resistor divider shown in the block diagram. This resistor divider forces the input voltage to move into the 3-state window. Initially the 3-state window is set between 1.0-V and 2.0-V thresholds. The lower threshold of the 3-state window is always fixed at about 1.0 V. The higher threshold is adjusted to about 75% of the input signal amplitude. The self-adjustable upper threshold allows shorter delay if the input signal enters the 3-state window while the input signal was high, thus keeping the high-side power FET in ON state just slightly longer than 250 ns time constant set by an internal 3-state timer. Both modes of operation, PWM input pulse sequencing and the 3-state condition, are illustrated in the timing diagrams shown in 図 5-19. The self-adjustable upper threshold allows operation in wide range amplitude of input PWM pulse signals. The waveforms in 図 6-2 and 図 6-3 illustrates the TPS28225 operation at normal and 3-state mode with the input pulse amplitudes 6 V and 2.5 V accordingly. After entering into the 3-state window and staying within the window for the hold-off time, the PWM input signal level is defined by the internal resistor divider and, depending on the input pulse amplitude, can be pulled up above the normal PWM pulse amplitude (図 6-3) or down below the normal input PWM pulse (図 6-2).

6.3.4.1 TPS28225 3-State Exit Mode

- To exit the 3-state operation mode, the PWM signal should go low and then high at least once.

This is necessary to restore the voltage across the bootstrap capacitor that could be discharged during the 3-state mode if the 3-state condition lasts long enough.

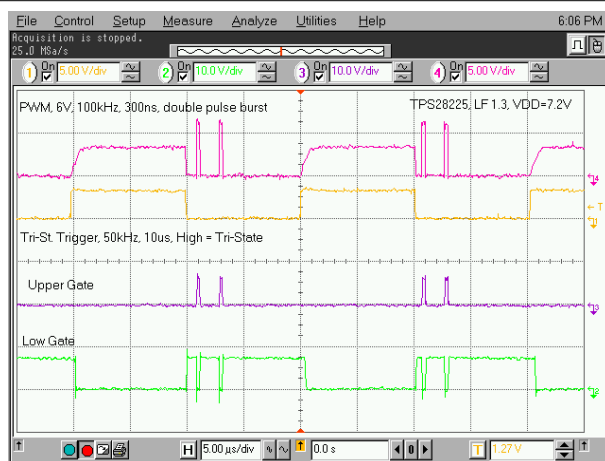


図 6-2. 6-V Amplitude PWM Pulse



図 6-3. 2.5-V Amplitude PWM Pulse

注

The driver sets UGATE low and LGATE high when PWM is low. When the PWM goes high, UGATE goes high and LGATE goes low.

6.3.4.2 External Resistor Interference

Any external resistor between PWM input and GND with the value lower than 40 k Ω can interfere with the 3-state thresholds. If the driver is intended to operate in the 3-state mode, any resistor below 40 k Ω at the PWM and GND should be avoided. A resistor lower than 3.5 k Ω connected between the PWM and GND completely

disables the 3-state function. In such case, the 3-state window shrinks to zero and the lower 3-state threshold becomes the boundary between the UGATE staying low and LGATE being high and vice versa depending on the PWM input signal applied. It is not necessary to use a resistor $<3.5\text{ k}\Omega$ to avoid the 3-state condition while using a controller that is 3-state capable. If the rise and fall time of the input PWM signal is shorter than 250 ns, then the driver never enters into the 3-state mode.

In the case where the low-side MOSFET of a buck converter stays on during shutdown, the 3-state feature can be fused to avoid negative resonant voltage across the output capacitor. This feature also can be used during start up with a pre-biased output in the case where pulling the output low during the startup is not allowed due to system requirements. If the system controller does not have the 3-state feature and never goes into the high-impedance state, then setting the EN/PG signal low will keep both gate drive outputs low and turn both low- and high-side MOSFETs OFF during the shut down and start up with the pre-biased output.

The self-adjustable input circuit accepts wide range of input pulse amplitudes (2 V up to 13.2 V) allowing use of a variety of controllers with different outputs including logic level. The wide PWM input voltage allows some flexibility if the driver is used in secondary side synchronous rectifier circuit. The operation of the TPS28225 with a 12-V input PWM pulse amplitude, and with $V_{DD} = 7.2\text{ V}$ and $V_{DD} = 5\text{ V}$ respectively is shown in [Figure 6-4](#) and [Figure 6-5](#).

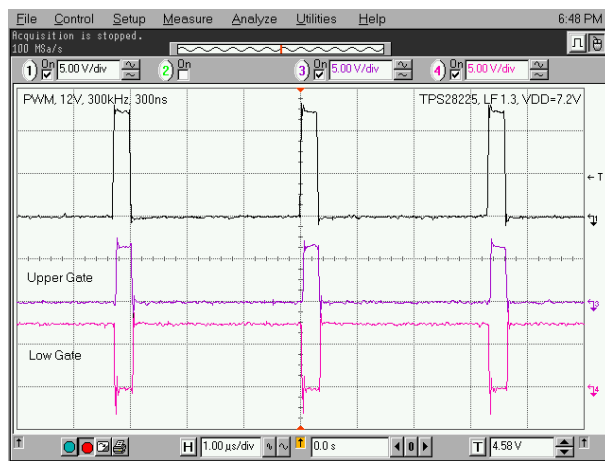


Figure 6-4. 12-V PWM Pulse at $V_{DD} = 7.2\text{ V}$



Figure 6-5. 12-V PWM Pulse at $V_{DD} = 5\text{ V}$

6.3.5 Bootstrap Diode

The bootstrap diode provides the supply voltage for the UGATE driver by charging the bootstrap capacitor connected between BOOT and PHASE pins from the input voltage VDD when the low-side FET is in ON state. At the very initial stage when both power FETs are OFF, the bootstrap capacitor is pre-charged through this path including the PHASE pin, output inductor and large output capacitor down to GND. The forward voltage drop across the diode is only 1.0 V at bias current 100 mA. This allows quick charge restore of the bootstrap capacitor during the high-frequency operation.

6.3.6 Upper and Lower Gate Drivers

The upper and lower gate drivers charge and discharge the input capacitance of the power MOSFETs to allow operation at switching frequencies up to 2 MHz. The output stage consists of a P-channel MOSFET providing source output current and an N-channel MOSFET providing sink current through the output stage. The ON state resistances of these MOSFETs are optimized for the synchronous buck converter configuration working with low duty cycle at the nominal steady state condition. The UGATE output driver is capable of propagating PWM input pulses of less than 30-ns while still maintaining proper dead time to avoid any shoot through current conditions. The waveforms related to the narrow input PWM pulse operation are shown in [Figure 5-18](#).

6.3.7 Dead-Time Control

The dead-time control circuit is critical for highest efficiency and no shoot through current operation throughout the whole duty cycle range with the different power MOSFETs. By sensing the output of driver going low, this circuit does not allow the gate drive output of another driver to go high until the first driver output falls below the specified threshold. This approach to control the dead time is called adaptive. The overall dead time also includes the fixed portion to ensure that overlapping never exists. The typical dead time is around 14 ns, although it varies over the driver internal tolerances, layout and external MOSFET parasitic inductances. The proper dead time is maintained whenever the current through the output inductor of the power stage flows in the forward or reverse direction. Reverse current could happen in a buck configuration during the transients or while dynamically changing the output voltage on the fly, as some microprocessors require. Because the dead time does not depend on inductor current direction, this driver can be used both in buck and boost regulators or in any bridge configuration where the power MOSFETs are switching in a complementary manner. Keeping the dead time at short optimal level boosts efficiency by 1% to 2% depending on the switching frequency. Measured switching waveforms in one of the practical designs show 10-ns dead time for the rising edge of PHASE node and 22 ns for the falling edge ([Figure 9-1](#) and [Figure 9-2](#) in the Application Section of the data sheet).

Large non-optimal dead time can cause duty cycle modulation of the DC-to-DC converter during the operation point where the output inductor current changes its direction right before the turn ON of the high-side MOSFET. This modulation can interfere with the controller operation and it impacts the power stage frequency response transfer function. As the result, some output ripple increase can be observed. The TPS28225 driver is designed with the short adaptive dead time having fixed delay portion that eliminates risk of the effective duty cycle modulation at the described boundary condition.

6.3.8 Thermal Shutdown

If the junction temperature exceeds 160°C, the thermal shutdown circuit will pull both gate driver outputs low and thus turning both, low-side and high-side power FETs OFF. When the driver cools down below 140°C after a thermal shutdown, then it resumes its normal operation and follows the PWM input and EN/PG signals from the external control circuit. While in thermal shutdown state, the internal MOSFET pulls the EN/PG pin low, thus setting a flag indicating the driver is not ready to continue normal operation. Normally the driver is located close to the MOSFETs, and this is usually the hottest spots on the PCB. Thus, the thermal shutdown feature of the TPS28225 can be used as an additional protection for the whole system from overheating.

6.4 Device Functional Modes

TPS28225 device functional mode truth table.

表 6-1. Truth Table

PIN	V_{DD} RISING < 3.5 V OR T_J > 160°C	V_{DD} FALLING > 3 V AND T_J < 150°C			
		EN/PG RISING < 1.7 V	EN/PG FALLING > 1.0 V		
			PWM < 1 V	PWM > 1.5 V AND T_{RISE}/T_{FALL} < 200 ns	PWM SIGNAL SOURCE IMPEDANCE >40 kΩ FOR > 250 ns (3-State) ⁽¹⁾
LGATE	Low	Low	High	Low	Low
UGATE	Low	Low	Low	High	Low
EN/PG	Low	–	–	–	–

(1) To exit the 3-state condition, the PWM signal should go low. One Low PWM input signal followed by one High PWM input signal is required before re-entering the 3-state condition.

7 Application and Implementation

注

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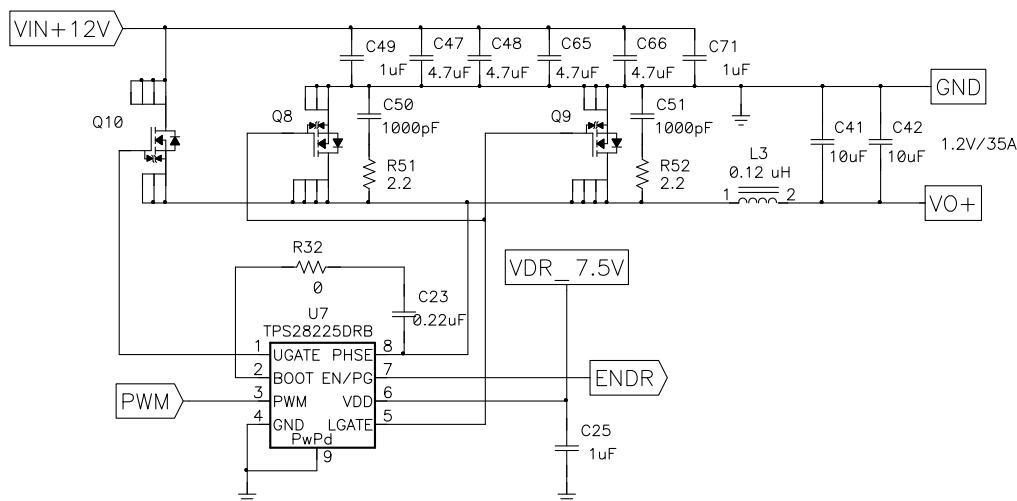
7.1 Application Information

To effect fast switching of power devices and reduce associated switching power losses, a powerful MOSFET driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, MOSFET drivers are indispensable when it is impossible for the PWM controller to directly drive the MOSFETs of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. MOSFET drivers effectively combine both the level-shifting and buffer-drive functions.

MOSFET drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

7.2 Typical Application

The DC-DC converter in [Figure 7-1](#) displays the schematic of the TPS28225 in a multiphase high-current step-down power supply (only one phase is shown). This design uses a single high-side MOSFET Q10 and two low-side MOSFETs Q8 and Q9, the latter connected in parallel. The TPS28225 is controlled by multiphase buck DC-to-DC controller like [TPS40090](#). As TPS28225 has internal shoot-through protection only one PWM control signal is required for each channel.



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Figure 7-1. One of Four Phases Driven by TPS28225 Driver in 4-Phase VRM Reference Design

7.2.1 Design Requirements

The VRM Reference Design is capable of driving 35 A per phase. In this example it has a nominal input voltage of 12 V within a tolerance range of $\pm 5\%$. The switching frequency is 500 kHz. The nominal duty cycle is 10%, therefore the low-side MOSFETs are conducting 90% of the time. By choosing lower $R_{DS(on)}$ the conduction losses of the switching elements are minimized.

表 7-1. VRM Reference Design Requirements

DESIGN PARAMETER	VALUE
Supply voltage	12 V $\pm 5\%$
Output voltage	0.83 V to 1.6 V
Frequency	500 kHz
Peak-to-peak output voltage variation on load current transient (0 A to 100 A) within 1 μ s	<160 mV
Dynamic output voltage change slew rate	12.25 mV per 5 μ s

7.2.2 Detailed Design Procedure

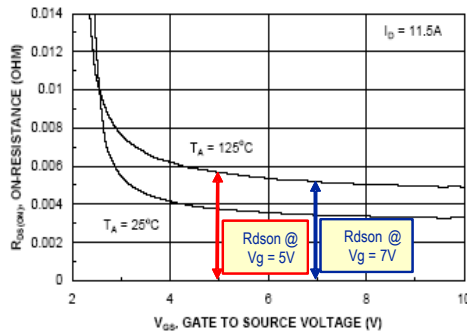
The bootstrap current can be limited by changing R32 to prevent overcharging of the bootstrap capacitor and to slow the turn-on transition of the high-side MOSFET. This reduces the peak amplitude and ringing of the switching node. Furthermore it minimizes the possibility of Cdv/dt -induced shoot-through of the low-side MOSFETs. The snubbers composed of C50 with R51 and C51 with R52 help to reduce switching noise.

The output component selection considers the requirement of a fast transient response. For output capacitors small capacitance values are chosen because of rapid changes of the output voltage. These changes also require an inductor with low inductance. Due to the small duty cycle the low-side MOSFETs conduct a long time. Two low-side MOSFETs are selected to increase both thermal performance and efficiency.

7.2.2.1 Four Phases Driven by TPS28225 Driver

When using the same power stage [7-1], the driver with the optimal drive voltage and optimal dead time can boost efficiency up to 5%. The optimal 8-V drive voltage versus 5-V drive contributes 2% to 3% efficiency increase and the remaining 1% to 2% can be attributed to the reduced dead time. The 7-V to 8-V drive voltage is optimal for operation at switching frequency range above 400 kHz and can be illustrated by observing typical $R_{DS(on)}$ curves of modern FETs as a function of their gate-drive voltage. This is shown in [7-2].

[7-2] and [7-3] show that the $R_{DS(on)}$ at 5-V drive is substantially larger than at 7 V and above that the $R_{DS(on)}$ curve is almost flat. This means that moving from 5-V drive to an 8-V drive boosts the efficiency because of lower $R_{DS(on)}$ of the MOSFETs at 8 V. Further increase of drive voltage from 8 V to 12 V only slightly decreases the conduction losses but the power dissipated inside the driver increases dramatically (by 125%). The power dissipated by the driver with 5-V, 8-V and 12-V drive as a function of switching frequency from 400 kHz to 800 kHz. It should be noted that the 12-V driver exceeds the maximum dissipated power allowed for an SOIC-8 package even at 400-kHz switching frequency.



On-Resistance Variation with Gate-to-Source Voltage.

Figure 7-2. $R_{DS(on)}$ of MOSFET as Function of V_{GS}

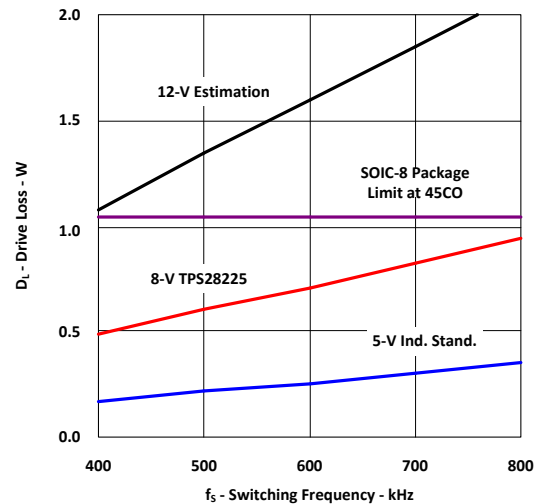


Figure 7-3. Drive Power as Function of V_{GS} and F_{sw}

7.2.2.2 Switching The MOSFETs

Driving the MOSFETs efficiently at high switching frequencies requires special attention to layout and the reduction of parasitic inductances. Efforts need to be done both at the driver's die and package level and at the PCB layout level to keep the parasitic inductances as low as possible. [Figure 7-4](#) shows the main parasitic inductances and current flow during turning ON and OFF of the MOSFET by charging its C_{GS} gate capacitance.

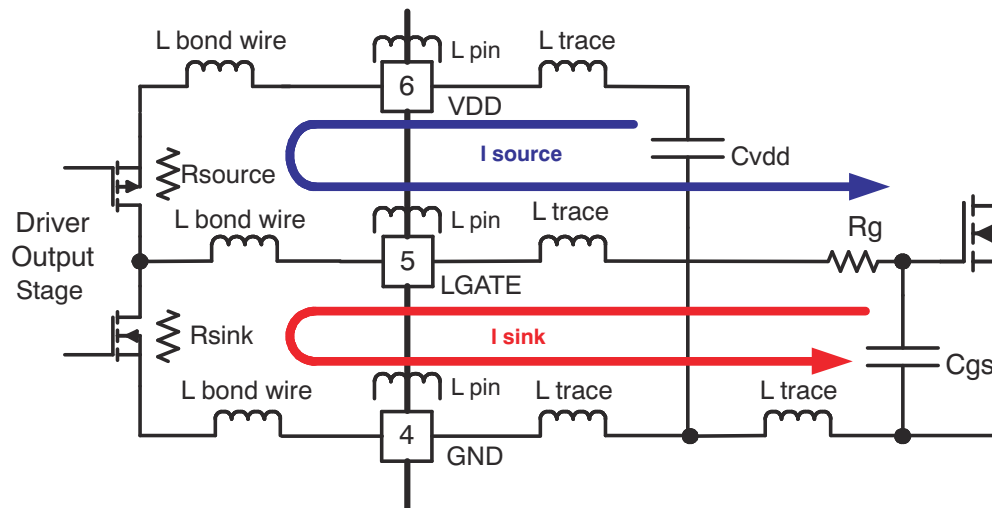


Figure 7-4. MOSFET Drive Paths and Main Circuit Parasitics

The I_{SOURCE} current charges the gate capacitor and the I_{SINK} current discharges it. The rise and fall time of voltage across the gate defines how quickly the MOSFET can be switched. The timing parameters specified in datasheet for both upper and lower driver are shown in [Figure 5-16](#) and [Figure 5-17](#) where 3-nF load capacitor has been used for the characterization data. Based on these actual measurements, the analytical curves in [Figure 7-5](#) and [Figure 7-6](#) show the output voltage and current of upper and low side drivers during the discharging of load capacitor. The left waveforms show the voltage and current as a function of time, while the right waveforms show the relation between the voltage and current during fast switching. These waveforms show the actual switching process and its limitations because of parasitic inductances. The static V_{OUT}/I_{OUT} curves shown in many datasheets and specifications for the MOSFET drivers do not replicate actual switching condition and provide limited information for the user.

Turning Off of the MOSFET needs to be done as fast as possible to reduce switching losses. For this reason the TPS28225 driver has very low output impedance specified as $0.4\ \Omega$ typical for lower driver and $1\ \Omega$ typical for upper driver at DC current. Assuming 8-V drive voltage and no parasitic inductances, one can expect an initial sink current amplitude of 20 A and 8 A respectively for the lower and upper drivers. With pure R-C discharge circuit for the gate capacitor, the voltage and current waveforms are expected to be exponential. However, because of parasitic inductances, the actual waveforms have some ringing and the peak current for the lower driver is about 4 A and about 2.5 A for the upper driver ([Figure 7-5](#) and [Figure 7-6](#)). The overall parasitic inductance for the lower drive path is estimated as 4 nH and for the upper drive path as 6 nH. The internal parasitic inductance of the driver, which includes inductances of bonded wires and package leads, can be estimated for SOIC-8 package as 2 nH for lower gate and 4 nH for the upper gate. Use of DFN-8 package reduces the internal parasitic inductances by approximately 50%.

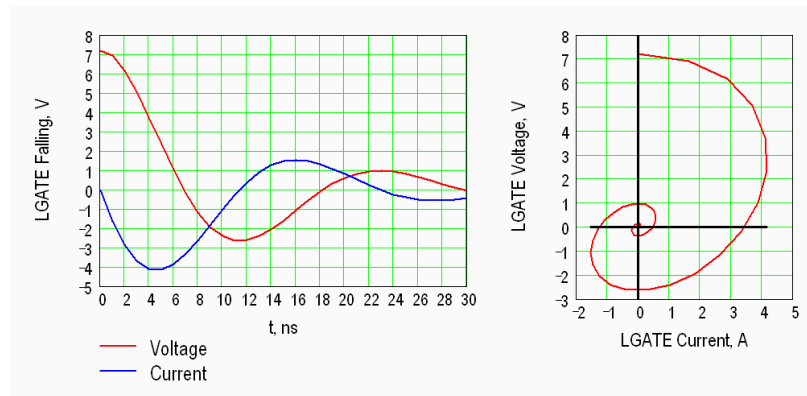


Figure 7-5. LGATE Turning Off Voltage and Sink Current vs Time (Related Switching Diagram (right))

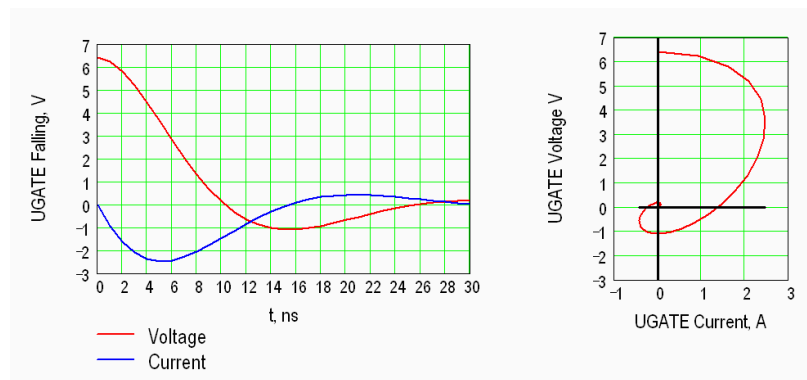


Figure 7-6. UGATE Turning Off Voltage and Sink Current vs Time (Related Switching Diagram (right))

7.2.2.3 List of Materials

For this specific example see [表 7-2](#). The component vendors are not limited to those shown in the table below. It should be noted that in this example, the power MOSFET packages were chosen with drains on top. The decoupling capacitors C47, C48, C65, and C66 were chosen to have low profiles. This allows the designer to meet good layout rules and place a heatsink on top of the FETs using an electrically isolated and thermally conductive pad.

表 7-2. List of Materials

REF DES	COUNT	DESCRIPTION	MANUFACTURE	PART NUMBER
C47, C48, C65, C66	4	Capacitor, ceramic, 4.7 μ F, 16 V, X5R 10%, low profile 0.95 mm, 1206	TDK	C3216X5R1C475K
C41, C42	2	Capacitor, ceramic, 10 μ F, 16 V, X7R 10%, 1206	TDK	C3216X7R1C106K
C50, C51	2	Capacitor, ceramic, 1000 pF, 50 V, X7R, 10%, 0603	Std	Std
C23	1	Capacitor, ceramic, 0.22 μ F, 16 V, X7R, 10%, 0603	Std	Std
C25, C49, C71	3	Capacitor, ceramic, 1 μ F, 16 V, X7R, 10%, '0603	Std	Std
L3	1	Inductor, SMT, 0.12 μ H, 31 A, 0.36 m Ω , 0.400 x 0.276	Pulse	PA0511-101
Q8, Q9	2	Mosfet, N-channel, V_{DS} 30 V, R_{DS} 2.4 m Ω , I_D 45 A, LFPAK-i	Renesas	RJK0301DPB-I
Q10	1	Mosfet, N-channel, V_{DS} 30 V, R_{DS} 6.2 m Ω , I_D 30 A, LFPAK-i	Renesas	RJK0305DPB-I
R32	1	Resistor, chip, 0 Ω , 1/10 W, 1%, '0805	Std	Std
R51, R52	2	Resistor, chip, 2.2 Ω , 1/10 W, 1%, '0805	Std	Std
U7	1	Device, High Frequency 4-A Sink Synchronous Buck MOSFET Driver, DFN-8	Texas Instruments	TPS28225DRB

7.2.3 Application Curves

Efficiency achieved using TPS28225 driver with 8-V drive at different switching frequencies a similar industry 5-V driver using the power stage in [図 7-1](#) is shown in [図 7-7](#), [図 7-8](#), [図 7-9](#), [図 7-10](#) and [図 7-11](#).

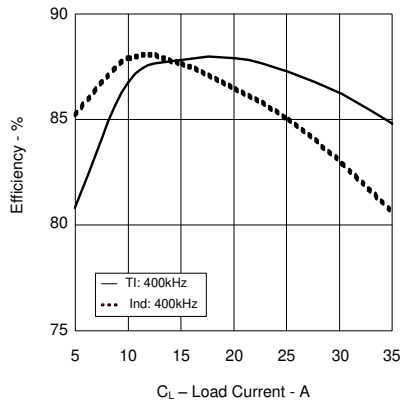


図 7-7. Efficiency vs Load Current

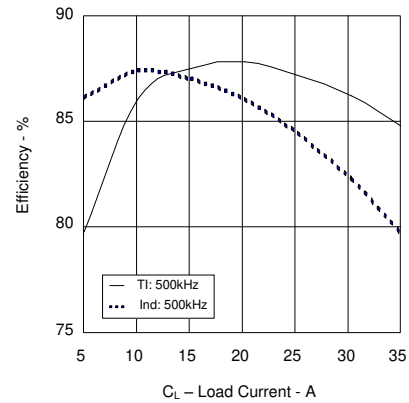


図 7-8. Efficiency vs Load Current

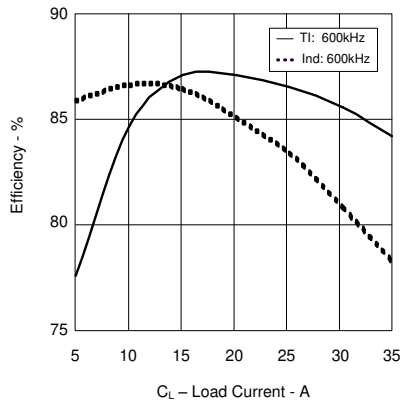


図 7-9. Efficiency vs Load Current

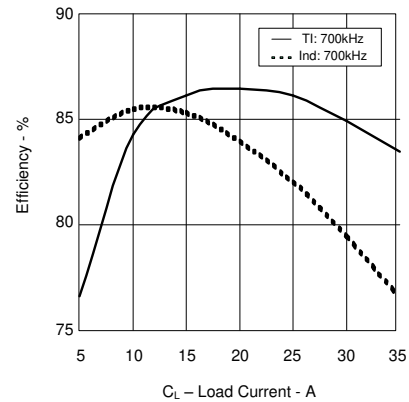


図 7-10. Efficiency vs Load Current

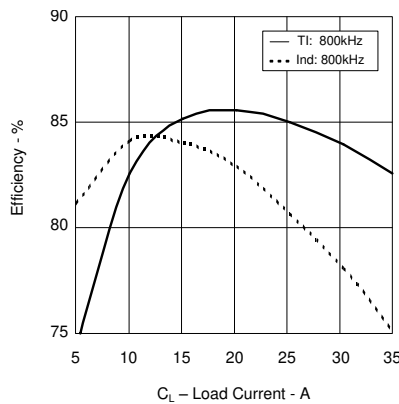
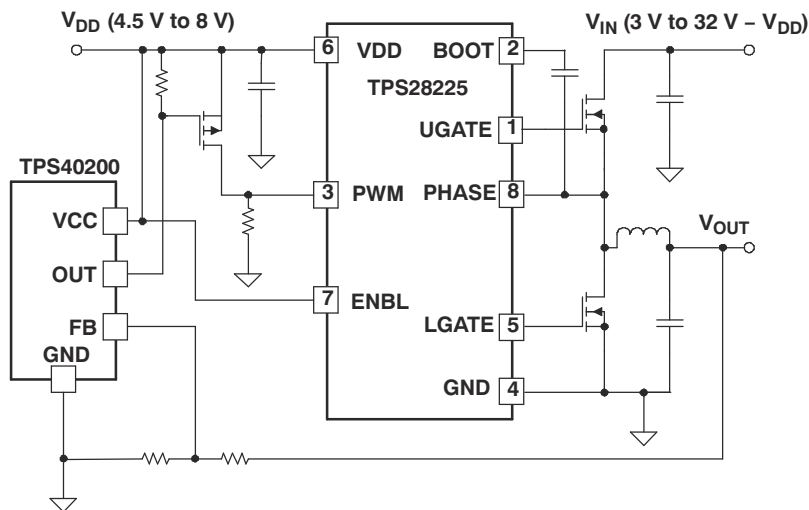


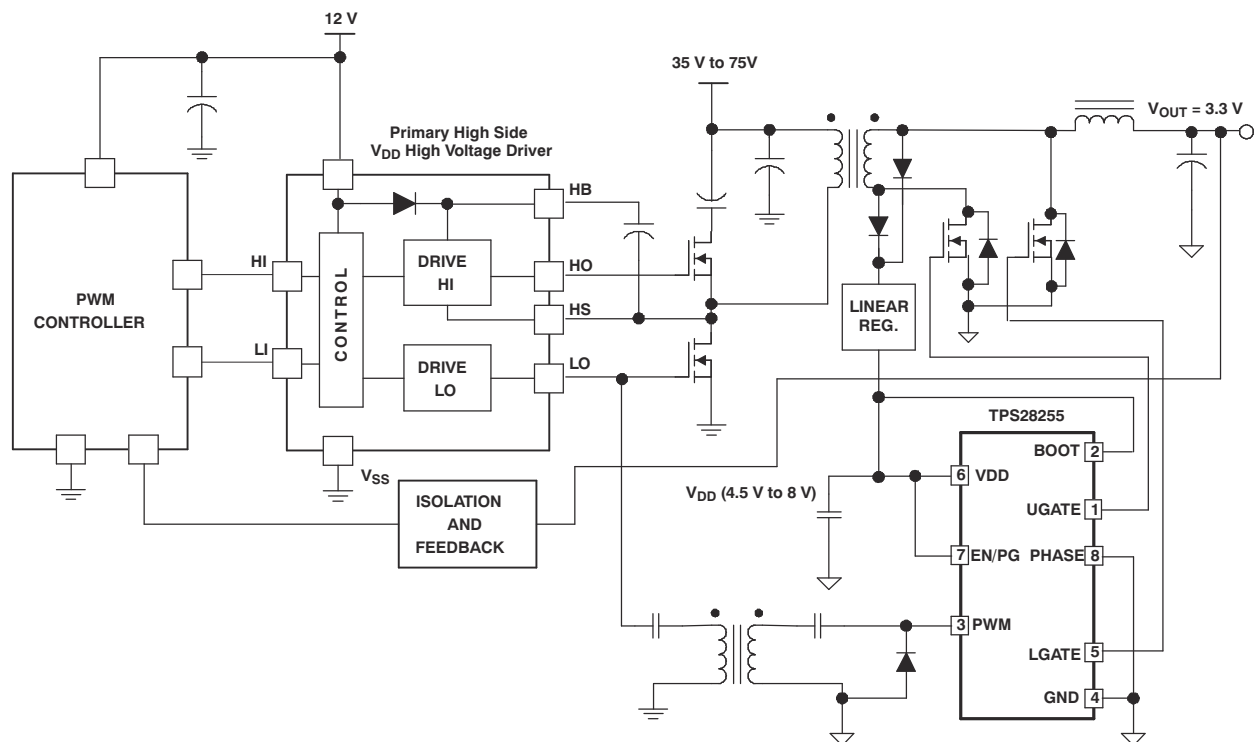
図 7-11. Efficiency vs Load Current

7.3 System Examples

Figure 7-12, Figure 7-13 and Figure 7-14 below illustrate typical implementations of the TPS28225 in step-down power supplies.



7-12. One-Phase POL Regulator



7-13. Driver for Synchronous Rectification with Complementary Driven MOSFETs

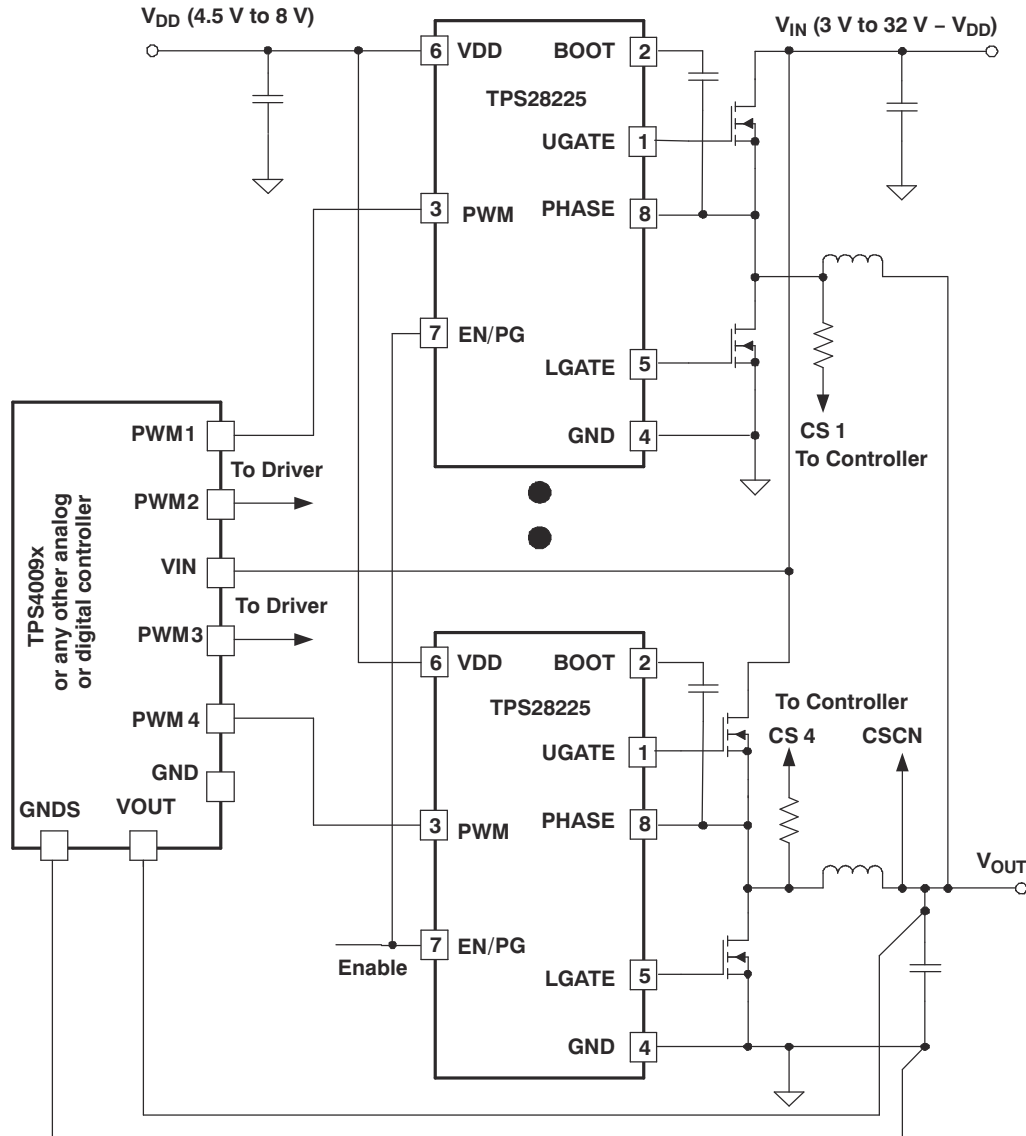


図 7-14. Multi-Phase Synchronous Buck Converter

8 Power Supply Recommendations

The supply voltage range for operation is 4.5 to 8 V. The lower end of this range is governed by the under-voltage lockout thresholds. The UVLO disables the driver and keeps the power FETs OFF when V_{DD} is too low. A low ESR ceramic decoupling capacitor in the range of 0.22 μF to 4.7 μF between V_{DD} and GND is recommended.

9 Layout

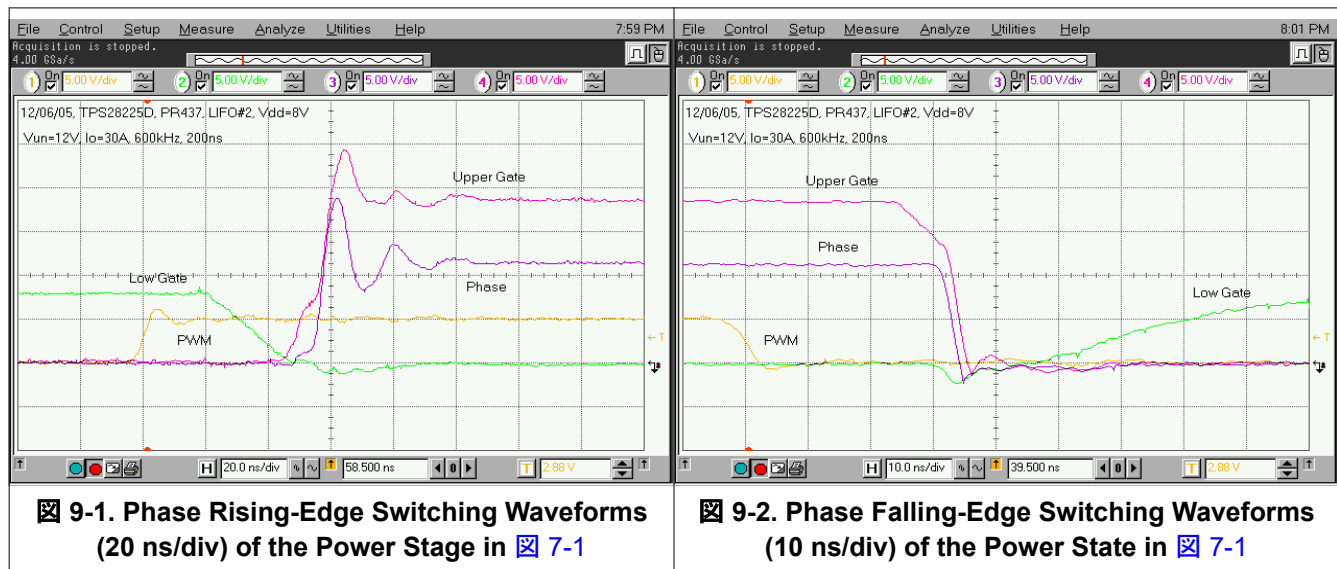
9.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules need to be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. Use the thermal pad of the DFN-8 package as the GND by connecting it to the GND pin. The GND trace or pad from the driver goes directly to the source of the MOSFET but should not include the high current path of the main current flowing through the drain and source of the MOSFET.
- Use a similar rule for the PHASE node as for the GND.
- Use wide traces for UGATE and LGATE closely following the related PHASE and GND traces. Eighty to 100 mils width is preferable where possible.
- Use at least 2 or more vias if the MOSFET driving trace needs to be routed from one layer to another. For the GND the number of vias are determined not only by the parasitic inductance but also by the requirements for the thermal pad.
- Avoid PWM and enable traces going close to the PHASE node and pad where high dV/dT voltage can induce significant noise into the relatively high impedance leads.

It should be taken into account that poor layout can cause 3% to 5% less efficiency versus a good layout design and can even decrease the reliability of the whole system.

The schematic of one of the phases in a multi-phase synchronous buck regulator and the related layout are shown in [Figure 7-1](#) and [Figure 9-3](#). These help to illustrate good design practices. The power stage includes one high-side MOSFET Q10 and two low-side MOSFETs (Q8 and Q9). The driver (U7) is located on bottom side of PCB close to the power MOSFETs. The related switching waveforms during turning ON and OFF of upper FET are shown in [Figure 9-1](#) and [Figure 9-2](#). The dead time during turning ON is only 10 ns ([Figure 9-1](#)) and 22 ns during turning OFF ([Figure 9-2](#)).



9.2 Layout Example

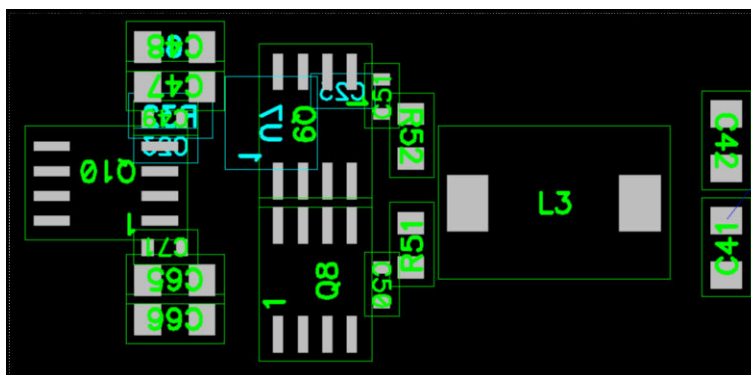


図 9-3. Component Placement Based on Schematic in 図 7-1

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.2 Documentation Support

10.2.1 Related Documentation

- TPS40090, TPS40091 2/3/4-Phase Multi-Phase Controller, ([SLUS578](#))

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

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10.5 Trademarks

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10.6 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2015) to Revision E (January 2024) Page

- Deleted ambient temperature from Absolute Maximum Ratings..... 4

Changes from Revision C (April 2010) to Revision D (September 2015) Page

- 「ピン構成および機能」セクション、「取り扱いに関する定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加..... 1
- TPS28226 デバイスを削除。..... 1

Changes from Revision B (July 2007) to Revision C (April 2010) Page

- Changed FUNCTIONAL BLOCK DIAGRAM..... 3

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS28225D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	28225
TPS28225DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28225
TPS28225DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28225
TPS28225DR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28225
TPS28225DRBR	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8225 65166
TPS28225DRBR.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8225 65166
TPS28225DRBR.B	Active	Production	SON (DRB) 8	3000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8225 65166
TPS28225DRBRG4	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8225 65166
TPS28225DRBRG4.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8225 65166
TPS28225DRBT	Active	Production	SON (DRB) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8225 65166
TPS28225DRBT.A	Active	Production	SON (DRB) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8225 65166
TPS28225DRBT.B	Active	Production	SON (DRB) 8	250 SMALL T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8225 65166
TPS28225DRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28225
TPS28225DRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28225
TPS28225DRG4.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28225
TPS28226D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	28226
TPS28226DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28226
TPS28226DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28226
TPS28226DR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28226
TPS28226DRBR	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8226
TPS28226DRBR.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8226
TPS28226DRBR.B	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8226
TPS28226DRBT	Obsolete	Production	SON (DRB) 8	-	-	Call TI	Call TI	-40 to 125	8226

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS28225 :

- Automotive : [TPS28225-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

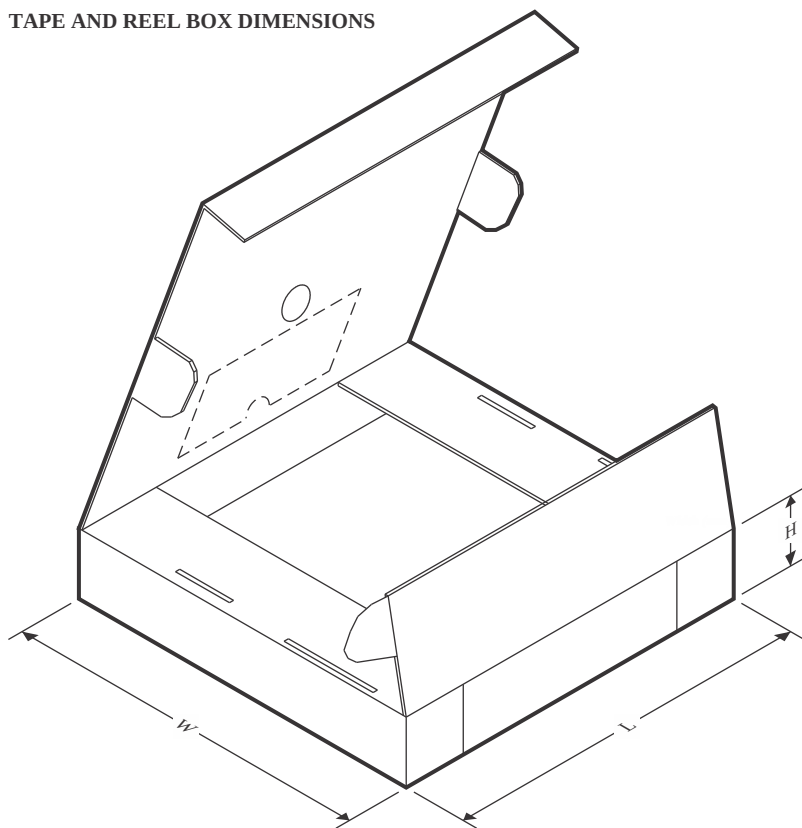
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS28225DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS28225DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS28225DRBG4	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS28225DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS28225DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS28226DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS28226DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

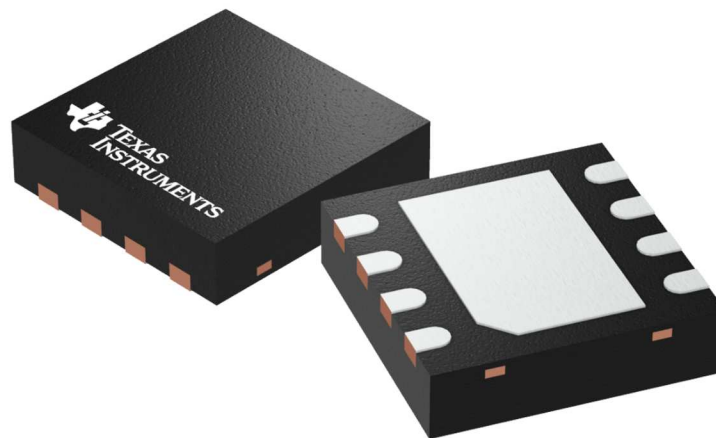
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS28225DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS28225DRBR	SON	DRB	8	3000	346.0	346.0	33.0
TPS28225DRBG4	SON	DRB	8	3000	346.0	346.0	33.0
TPS28225DRBT	SON	DRB	8	250	182.0	182.0	20.0
TPS28225DRG4	SOIC	D	8	2500	353.0	353.0	32.0
TPS28226DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS28226DRBR	SON	DRB	8	3000	353.0	353.0	32.0

DRB 8

GENERIC PACKAGE VIEW

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



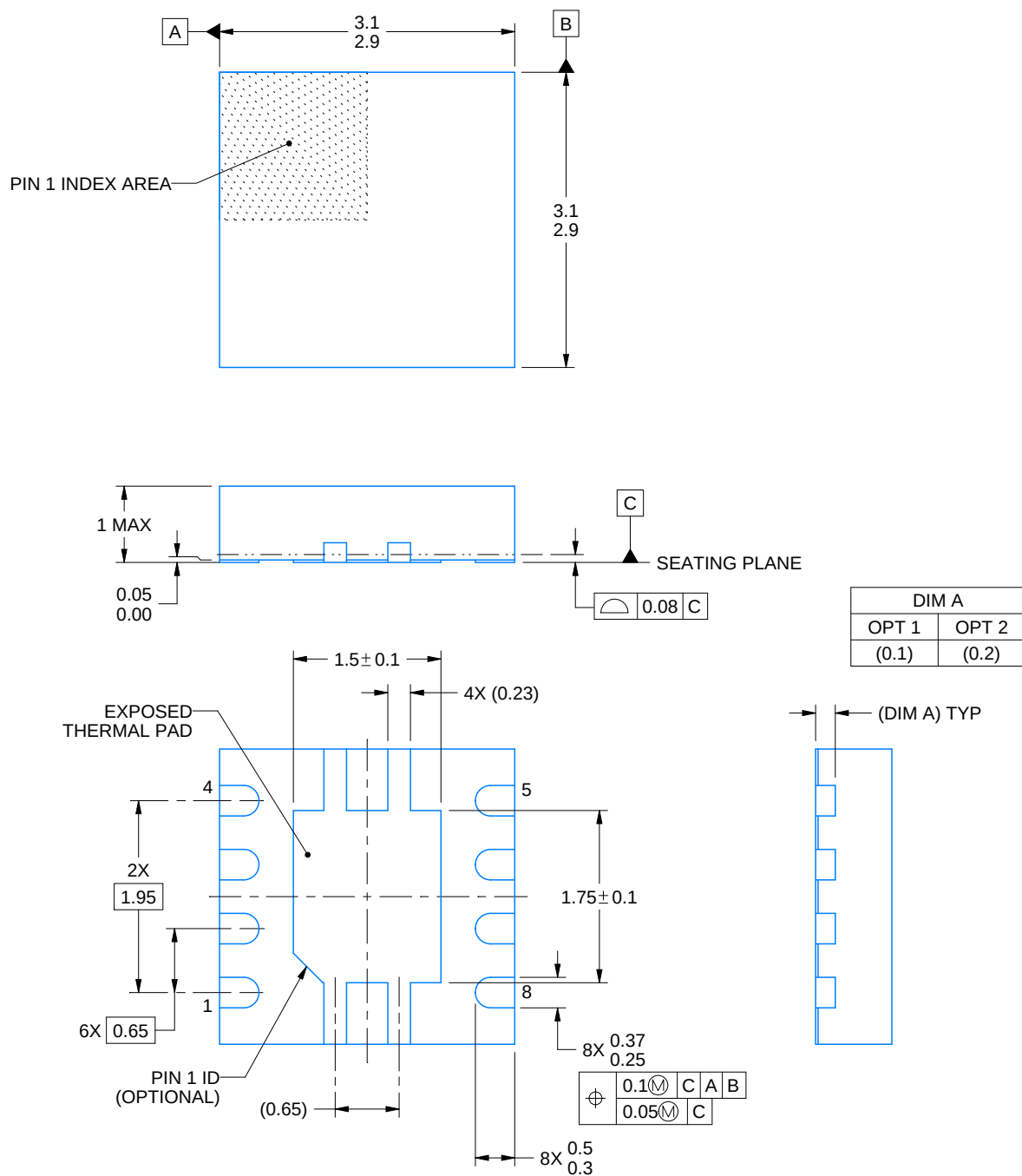
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L



VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



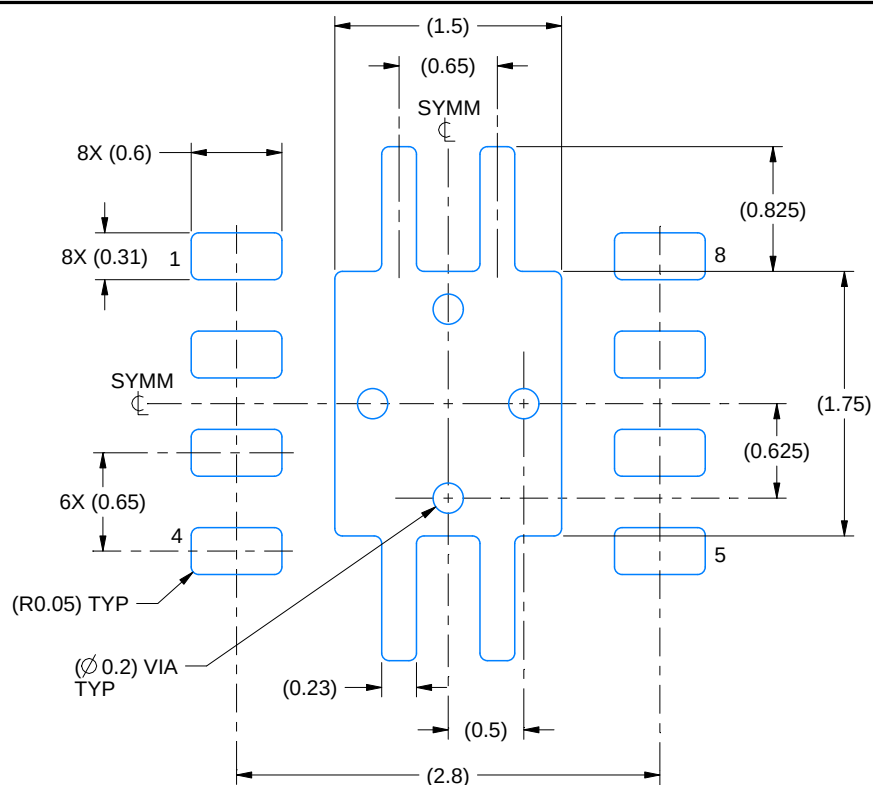
4218875/A 01/2018

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

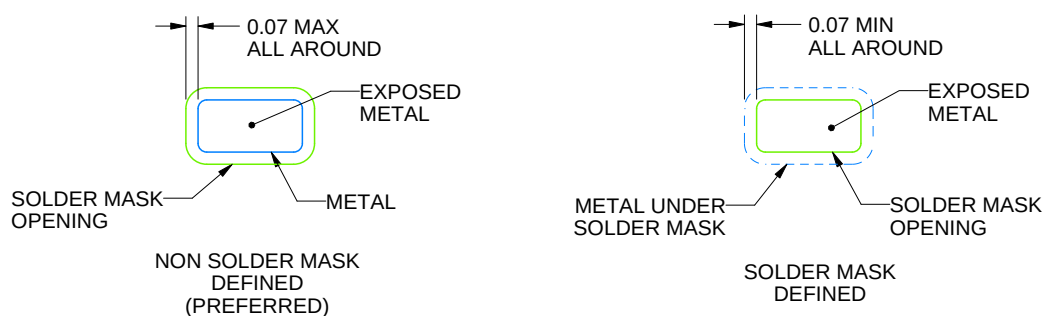
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

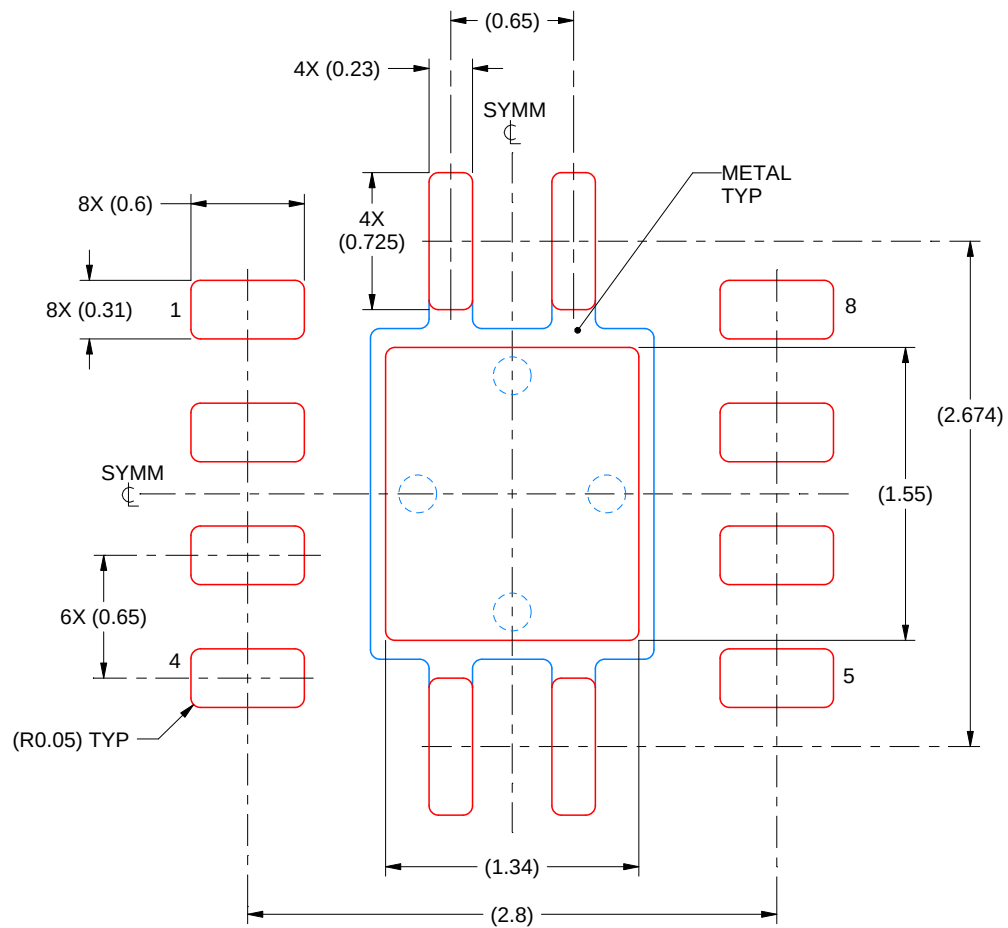
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



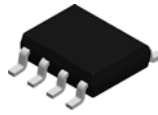
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

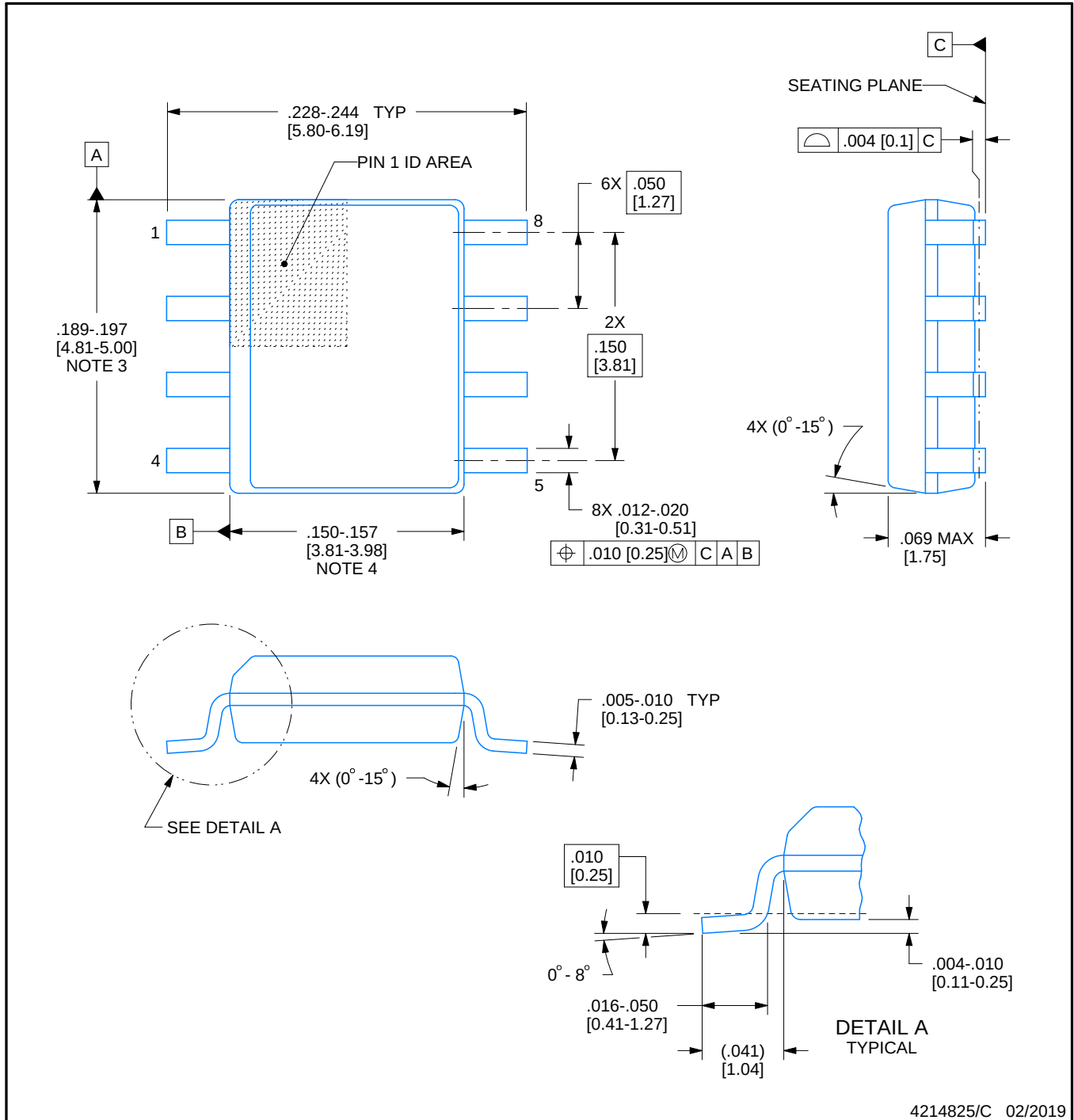


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

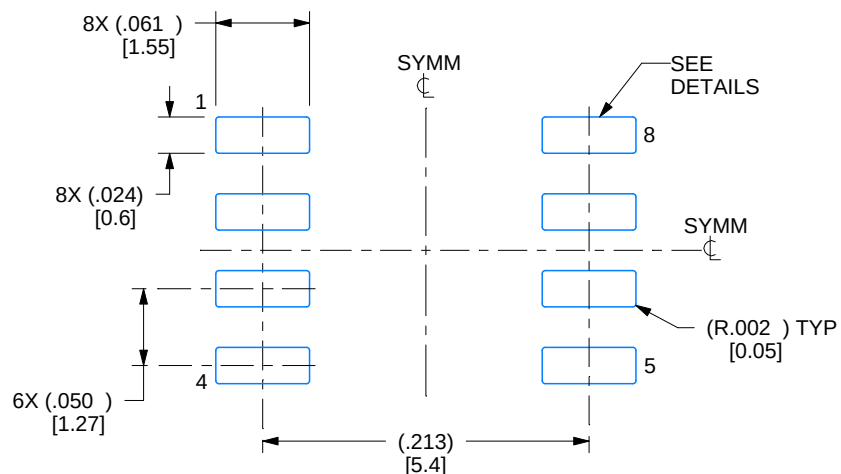
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

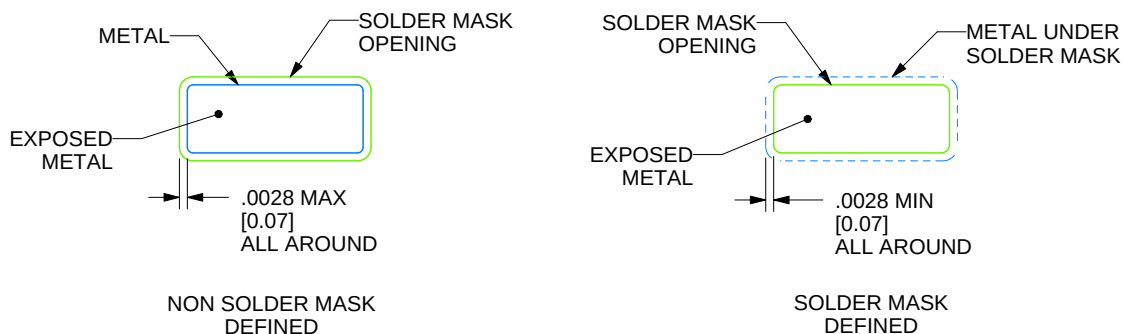
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

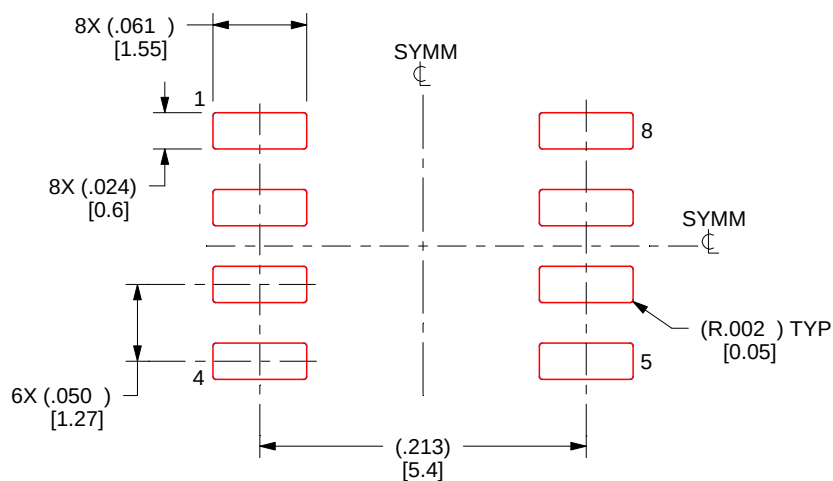
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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