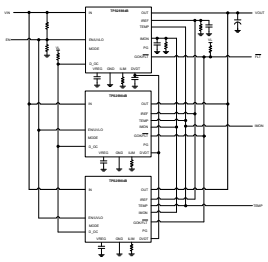
TPS25984Bx、4.5V～16V、0.8mΩ、70A、スタッカブル内蔵型ホットスワップ (eFuse)、高精度で高速な電流モニタ搭載

1 特長

- 動作入力電圧範囲:4.5V～16V
  - 絶対最大値:20V DC、23.5V 過渡
  - 出力側で最大 -1V の負電圧に対応
- FET 内蔵、非常に低い R_{DSON}:0.8mΩ (標準値)
- 定格 RMS 電流:55A、ピーク電流:70A
- 複数の eFuse の並列接続をサポートし、大電流を供給可能
  - 起動中の電流バランスの制御
- 堅牢な過電流保護機能
  - 過電流スレッショルド (I_{OCP}) を調整可能:±5% の精度で 10A～80A
  - 内蔵過渡過電流ブランキング タイマを使用した定常状態動作時のサーキット ブレーカの応答により、ピーク電流をサポート
  - 起動時のアクティブ電流制限 (I_{LIM}) を調整可能
- 堅牢な短絡保護機能
  - 出力短絡イベントに対する高速トリップ応答 (200ns 未満)
  - 可変 (2 × I_{OCP}) および固定のスレッショルド
  - 電源ライン過渡への耐性 - 不要なトリップなし
- 高精度なアナログ負荷電流監視機能
  - 精度:±1.4%、帯域幅:500kHz 超
- 高速な過電圧保護 (18.4V 固定のスレッショルド)
- 突入電流からの保護のために出力スルーレート制御 (dVdt) を調整可能
- アクティブ HIGH のイネーブル入力、低電圧誤動作防止 (UVLO) を設定可能
- 過熱保護 (OTP)
  - FET SOA:10W√s
- FET の健全性監視および報告機能を内蔵
- アナログ ダイ温度モニタ出力 (TEMP)
- 専用のフォルト表示ピン (GOK/$\overline{FLT}$)
- パワー グッド表示ピン (PG)
- 小さい占有面積:QFN-32、5mm x 5mm
- 100% 鉛フリー



概略回路図

2 アプリケーション

- 入力ホットスワップおよびホットプラグ
- サーバーおよび高性能コンピューティング
- ネットワーク インターフェイス カード
- グラフィックスおよびハードウェア アクセラレータ カード
- データ センターのスイッチおよびルーター
- ファン トレイ

3 概要

TPS25984Bx は、小型パッケージの大電流スタッカブル統合型ホットスワップ保護 (eFuse) デバイスです。このデバイスは、非常に少数の外付け部品で複数の保護モードを提供し、過負荷、短絡、および過剰な突入電流に対して堅牢な保護を行います。

特定の突入電流要件を持つアプリケーションでは、単一の外付けコンデンサにより出力スルー レートを設定できます。出力電流制限レベルは、システムの必要に応じてユーザーが設定できます。内蔵の過電流ブランキング タイマを使用すると、システムは eFuse をトリップせずに、負荷電流の過渡ピークに対応できます。

複数の TPS25984Bx デバイスを並列にスタックして、大電力システム用に合計電流容量を拡大できます。すべてのデバイスがスタートアップ時に電流を共有することで、一部のデバイスに過大なストレスがかかることを防ぎます。このようなストレスは、並列チェーンの早期または部分的なシャットダウンを引き起こす可能性があります。

高速で高精度の検出を行う内蔵のアナログ負荷電流モニタにより、予知保全と高度な動的プラットフォーム電力管理手法 (Intel® PSYS および PROCHOT™ など) が容易になり、システム スループットと電源使用率を最大化できます。

これらのデバイスは、-40℃～+125℃の接合部温度範囲で動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS25984B0RZJ	RZJ (QFN、32)	5mm × 5mm
TPS25984B1RZJ		
TPS25984B2RZJ		
TPS25984B3RZJ		

(1) 供給されているすべてのパッケージについては、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

Table of Contents

4 Device Comparison Table

PART NUMBER	FAULT RESPONSE	OVERCURRENT BLANKING TIMER
TPS25984B0RZJ	Latch off	400µs (typ)
TPS25984B1RZJ	Auto-retry	
TPS25984B2RZJ	Configurable based on MODE pin	
TPS25984B3RZJ	Latch off	3.2ms (typ)

5 Pin Configuration and Functions

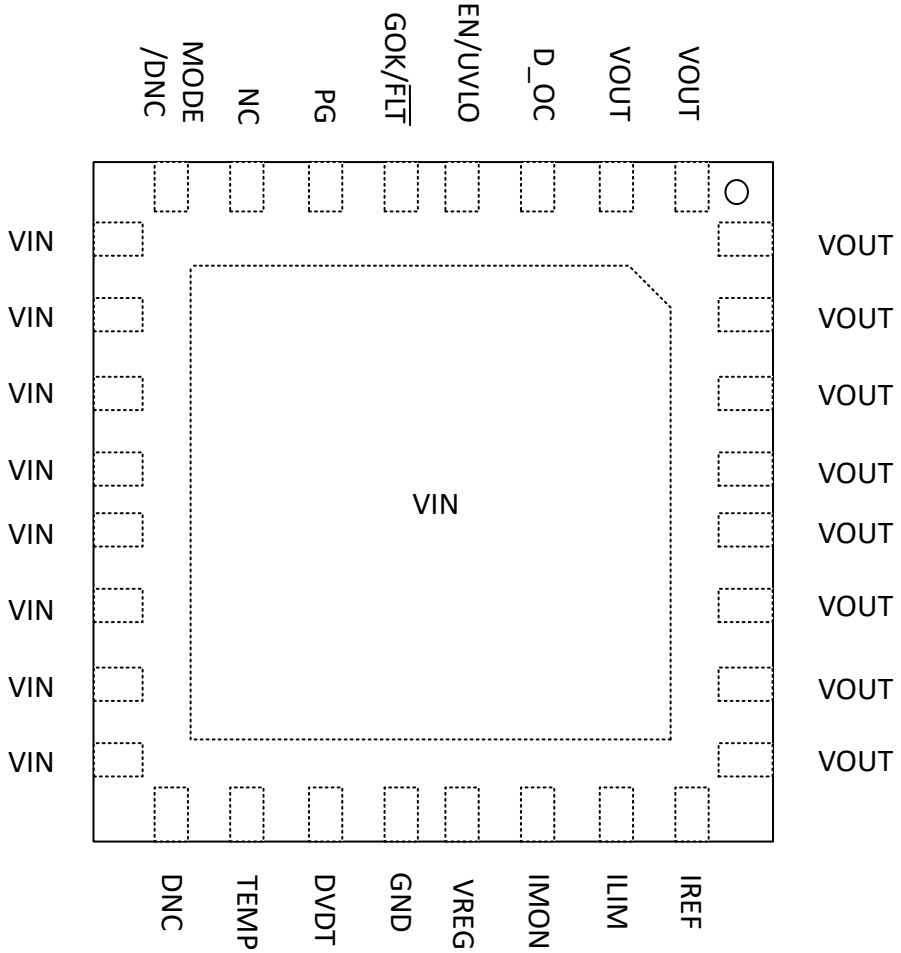


図 5-1. TPS25984Bx RZJ Package, 32-pin QFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUT	1, 2, 25, 26, 27, 28, 29, 30, 31, 32	O	Power output. Must be soldered to output power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.
D_OC	3	O	Open-drain signal to indicate overcurrent event.
EN/UVLO	4	I	Active high enable input. Connect resistor divider from input supply to set the undervoltage threshold. *Do not leave floating.*
GOK/$\overline{\text{FLT}}$	5	I/O	Open-drain active low fault indication. Also acts as an input for synchronizing faults between parallel devices. *Do not leave floating*.
PG	6	O	Open-drain active high Power Good indication. This pin is recommended to be pulled up externally to a logic level supply.
NC	7	N/A	No connect. Can be left floating or connected to input supply.
MODE	8	I	TPS25984B2: Retry mode selection pin.
DNC			TPS25984B0/1/3: Do not connect anything to this pin.

表 5-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN	9, 10, 11, 12, 13, 14, 15, 16, Exposed Pad	P	Power input. Must be soldered to input power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.
DNC	17	I/O	Internal test mode pin. Do not force a voltage on this pin externally.
TEMP	18	O	Die junction temperature monitor analog voltage output. Can be tied together with TEMP outputs of multiple devices in a parallel configuration to indicate the peak temperature of the chain.
DVDT	19	O	Start-up output slew rate control pin. Leave this pin open to allow fastest start-up. Connect capacitor to ground to slow down the slew rate to manage inrush current.
GND	20	G	Device ground reference pin. Connect to system ground.
VREG	21	O	Internal LDO output. Decouple with a capacitor to GND.
IMON	22	O	An external resistor from this pin to GND sets the voltage gain for the analog output load current monitor signal during steady-state.
ILIM	23	O	An external resistor from this pin to GND sets the current limit threshold during start-up as well as circuit-breaker and fast-trip threshold during steady-state. This pin also acts as analog load current monitor during start-up and steady-state. *Do not leave floating.*
IREF	24	I/O	Reference voltage for overcurrent and short-circuit protection blocks. Can be generated using internal current source and resistor on this pin, or can be driven from external voltage source. *Do not leave floating.*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{INMAX}	Maximum Input Voltage Range	IN	–0.3	20	V
$V_{INMAX,PLS}$	Maximum Input Voltage Range (10µs, $T_A \geq 0℃$)	IN	–0.3	Min(23.5, V_{OUT} + 23)	V
$V_{INMAX, SLEW}$	Maximum Slew Rate at Input Pin	IN		30	V/µs
V_{OUTMAX}	Maximum Output Voltage Range	OUT	–1	Min(20, V_{IN} + 0.3)	
$V_{IREFMAX}$	Maximum IREF Pin Voltage Range	IREF		5.5	V
$V_{DVDTMAX}$	Maximum DVDT Pin Voltage Range	DVDT		5.5	V
$V_{MODEMAX}$	Maximum MODE Pin Voltage Range	MODE	Internally Limited		V
V_{DOCMAX}	Maximum D_OC Pin Voltage Range	D_OC		5.5	V
I_{DOCMAX}	Maximum D_OC Pin Sink Current	D_OC		10	mA
V_{ENMAX}	Maximum Enable Pin Voltage Range	EN/UVLO		20	V
$V_{FLTBMAX}$	Maximum GOK/$\overline{FLT}$ Pin Voltage Range	GOK/$\overline{FLT}$		5.5	V
$I_{FLTBMAX}$	Maximum GOK/$\overline{FLT}$ Pin Sink Current	GOK/$\overline{FLT}$		10	mA
V_{PGMAX}	Maximum PG Pin Voltage Range	PG		5.5	V
I_{PGMAX}	Maximum PG Pin Sink Current	PG		10	mA
$V_{TEMPMAX}$	Maximum TEMP Pin Voltage Range	TEMP		5.5	V
$V_{ILIMMAX}$	Maximum ILIM pin voltage	ILIM	Internally Limited		V
$V_{IMONMAX}$	Maximum IMON pin voltage	IMON	Internally Limited		V
V_{REGMAX}	Maximum VREG pin voltage	VREG	Internally Limited		V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_{JMAX}	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Soldering Temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	4.5	16	V
V_{OUT}	Output Voltage Range	OUT	0	V_{IN}	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO	0	Min(V_{DD} + 1 V, V_{IN} + 1 V)	V
V_{DVDT}	DVDT Pin Cap Voltage Rating	DVDT	4		V
V_{PG}	PG Pin Pull-up Voltage Range	PG	0	5	V
V_{FLTB}	GOK/$\overline{FLT}$ Pin Pull-up Voltage Range	GOK/$\overline{FLT}$	0	5	V
V_{DOC}	D_OC Pin Pull-up Voltage Range	D_OC	2.5	5	V
I_{REG}	VREG pin sourcing current	VREG		1	mA
V_{IREF}	IREF Pin Voltage Range	IREF	0.3	1.8	V
V_{ILIM}	ILIM Pin Voltage Range	ILIM	0	3	V
V_{IMON}	IMON Pin Voltage Range	IMON	0	3	V
I_{MAX}	RMS Switch Current, $T_J \le 125℃$	IN to OUT	0	55	A
$I_{MAX, PLS}$	Peak Switch Current, $T_J \le 125℃$	IN to OUT	0	70	A
C_{IN}	Cap at Pin 7	Pin 7 to GND		100	nF
T_J	Junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1] [2]		TPS25984BX RZJ (QFN) 32 PINS	UNIT
$R_{\theta JA(eff)}$	Junction-to-ambient thermal resistance (effective)	16.5[2]	°C/W
		25.2[3]	°C/W
$\Psi_{JT(eff)}$	Junction-to-top characterization parameter (effective)	0.3[2] [3]	°C/W
$\Psi_{JB(eff)}$	Junction-to-board characterization parameter (effective)	4.4[2]	°C/W
		4.9[3]	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 8-layer PCB (4s4p) with 9 thermal vias under the device
(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with 9 thermal vias under the device

6.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12V, OUT = Open, $V_{EN/UVLO}$ = 2V, D_OC = 10kΩ pull-up to 5V, R_{ILIM} = 1.1kΩ, R_{IMON} = 1.1kΩ, V_{IREF} = 1V, DVDT = Open, GOK/$\overline{FLT}$ = 10kΩ pull-up to 5V, PG = 10kΩ pull-up to 5V, TEMP = Open, MODE = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (IN)						
V_{IN}	VIN input operating voltage range		4.5		16	V
$V_{UVPIN(R)}$	V_{IN} undervoltage protection threshold	V_{IN} Rising	4	4.25	4.5	V
$V_{UVPIN(F)}$	V_{IN} undervoltage protection threshold	V_{IN} Falling	3.9	4.15	4.4	V
$I_{QON(IN)}$	IN ON state quiescent current	V_{EN} ≥ $V_{UVLO(R)}$		3500	4420	µA
$I_{QOFF(IN)}$	IN OFF state current	V_{EN} < $V_{UVLO(F)}$		110	165	µA
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO)						
$V_{UVLO(R)}$	EN/UVLO pin voltage rising threshold for turning on	EN/UVLO Rising	1.35	1.40	1.52	V
$V_{UVLO(F)}$	EN/UVLO pin voltage falling threshold for turning off and engaging output discharge (primary device)	EN/UVLO Falling, MODE = Open	1.16	1.20	1.23	V
	EN/UVLO pin voltage threshold for turning off and engaging QOD (secondary device)	EN/UVLO Falling, MODE = GND		0.2		V
$V_{SD(F)}$	EN/UVLO pin voltage threshold for entering full shutdown	EN/UVLO Falling	0.5	0.8		V
I_{ENLKG}	EN/UVLO pin leakage current		–0.1		0.1	µA
OVERVOLTAGE PROTECTION (IN)						
$V_{OVP(R)}$	Input overvoltage protection threshold (rising)	V_{IN} rising	17.78	18.4	18.74	V
$V_{OVP(F)}$	Input overvoltage protection threshold (falling)	V_{IN} falling	17.17	17.7	18	V
ON-RESISTANCE (IN - OUT)						
R_{ON}	ON resistance	I_{OUT} = 8A, T_J = 25°C		0.80	0.95	mΩ
		I_{OUT} = 8A, T_J = –40 to 125°C			1.5	mΩ
OVERCURRENT PROTECTION REFERENCE (IREF)						
V_{IREF}	IREF pin recommended voltage range		0.3		1.8	V
I_{IREF}	IREF pin internal sourcing current		9.73	10	10.26	µA
CIRCUIT-BREAKER AND CURRENT LIMIT (ILIM)						
$G_{ILIM(LIN)}$	ILIM current monitor gain (ILIM:IOUT)	Device in Steady State (PG asserted)	7.28	7.5	7.76	µA/A
$CL_{REF(LIN)\%}$	Ratio of steady-state overcurrent protection threshold (IOCP) to Overcurrent protection reference voltage (VIREF)	V_{OUT} > V_{FB}, PG asserted		75		%
$CL_{REF(SAT)\%}$	Ratio of start-up current limit threshold (ILIM) to steady-state overcurrent protection threshold (IOCP)	V_{OUT} > V_{FB}, PG not asserted		53.3		%
$DOC_{REF\%}$	Ratio of steady state IOUT to at which overcurrent warning (D_OC) gets asserted to steady-state overcurrent protection threshold reference (IOCP)	PG asserted		85		%
I_{LIM}	Start-up current limit regulation threshold	R_{ILIM} = 1.1kΩ, V_{IREF} = 0.835V, V_{OUT} > V_{FB}	28	39.47	52	A
		R_{ILIM} = 1.1kΩ, V_{IREF} = 0.714V, V_{OUT} > V_{FB}	25	34.62	45	A
		R_{ILIM} = 1.1kΩ, V_{IREF} = 0.3V, V_{OUT} > V_{FB}	10.5	14	17.5	A

6.5 Electrical Characteristics (続き)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12V, OUT = Open, $V_{EN/UVLO}$ = 2V, D_OC = 10kΩ pull-up to 5V, R_{ILIM} = 1.1kΩ, R_{IMON} = 1.1kΩ, V_{IREF} = 1V, DVDT = Open, GOK/$\overline{FLT}$ = 10kΩ pull-up to 5V, PG = 10kΩ pull-up to 5V, TEMP = Open, MODE = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Foldback voltage			1.98		V
OUTPUT CURRENT MONITOR (IMON)						
G_{IMON}	IMON current monitor gain (IMON:IOUT)	Device in steady state (PG asserted)	9.78	10	10.25	µA/A
I_{OCP}	Steady-state overcurrent protection (Circuit-Breaker) threshold	R_{ILIM} = 2kΩ, V_{IREF} = 1.4V	65.8	70	74.2	A
		R_{ILIM} = 2kΩ, V_{IREF} = 1V	47.11	50.10	52.85	A
		R_{ILIM} = 2kΩ, V_{IREF} = 0.5V	24.18	25.08	25.95	A
		R_{ILIM} = 2kΩ, V_{IREF} = 0.24V	11.6	12.03	12.5	A
SHORT-CIRCUIT PROTECTION						
I_{FFT}	Fixed fast-trip threshold in steady-state	PG asserted High		148		A
$SFT_{REF(LIN)\%}$	Scalable fast-trip threshold (ILIM) to overcurrent protection threshold reference (IOCP) ratio during steady-state	PG asserted High		200		%
$SFT_{REF(SAT)\%}$	Scalable fast-trip threshold (ILIM) to overcurrent protection threshold reference (IOCP) ratio during start-up	PG de-asserted Low		80		%
INTERNAL LDO OUTPUT (VREG)						
V_{REG}	V_{REG} pin internal LDO voltage	I_{REG} = 0mA	2.8	3.15	3.6	V
V_{REG}	V_{REG} pin Internal LDO voltage	Resistor = 1k from V_{REG} to GND	2.2	2.58	3	V
INRUSH CURRENT PROTECTION (DVDT)						
I_{DVDT}	DVDT pin charging current	TPS25984B0/1/3 variants	1.85	2.5	3.22	µA
		TPS25984B2 variant	5.5	6.6	7.5	µA
G_{DVDT}	DVDT gain			20		V/V
R_{DVDT}	DVDT pin to GND discharge resistance			526		Ω
$R_{ON(GHI)}$	R_{ON} when PG is asserted		0.5	0.92	1.6	mΩ
QUICK OUTPUT DISCHARGE (OUT)						
I_{QOD}	Quick output discharge internal pull-down current	$V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$, –40 < T_J < 125°C		21.43		mA
TEMPERATURE SENSOR OUTPUT (TEMP)						
G_{TMP}	TEMP sensor gain		2.58	2.65	2.72	mV/°C
V_{TMP}	TEMP pin output voltage	T_J = 25°C	676	679	684	mV
I_{TMPSRC}	TEMP pin sourcing current			91.9		µA
I_{TMPSNK}	TEMP pin sinking current			10		µA
OVERTEMPERATURE PROTECTION						
TSD	Thermal shutdown threshold	T_J Rising		150		°C
TSD_{HYS}	Thermal shutdown hysteresis	T_J Falling		12.5		°C

6.6 Logic Interface

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL OVERCURRENT INDICATION (D_OC)						
R_{DOC}	D_OC pin pull-down resistance	D_OC de-asserted Low		9		Ω
I_{DOCLKG}	D_OC pin leakage current	D_OC asserted High	–2		2	µA

6.6 Logic Interface (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FAULT INDICATION (GOK/$\overline{FLT}$)						
R_{FLTB}	GOK/$\overline{FLT}$ pin pull-down resistance	GOK/$\overline{FLT}$ sserted Low		9		Ω
$I_{FLTBLKG}$	GOK/$\overline{FLT}$ in leakage current	GOK/$\overline{FLT}$ de-asserted High	–2		2	µA
POWER GOOD INDICATION (PG)						
R_{PG}	PG pin pull-down resistance	PG de-asserted Low		9		Ω
I_{PGKG}	PG pin leakage current	PG asserted High	–2		2	µA

6.7 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP}	Overvoltage protection response time	V_{IN} > $V_{OVP(R)}$ to V_{OUT} ↓		1.57		µs
t_{INSDLY}	Insertion delay	V_{IN} > $V_{UVP(R)}$ to DVDT ↑		13.7		ms
t_{FFT}	Fixed Fast-Trip response time	I_{OUT} > 1.5 × I_{FFT} to I_{OUT} ↓		200		ns
t_{SFT}	Scalable Fast-Trip response time	I_{OUT} > 3 × I_{OCP} to I_{OUT} ↓		400		ns
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.5 × I_{OCP} to I_{OUT} ↓ (TPS25984B0/1/2 variants)		400		µs
		I_{OUT} = 1.5 × I_{OCP} to I_{OUT} ↓ (TPS25984B3 variants)		3.2		ms
t_{RST}	Auto-Retry Interval	Auto-retry variant		105		ms
$t_{EN(DG)}$	EN/UVLO de-glitch time			6		µs
t_{SU_TMR}	Start-up timeout interval	SWEN ↑ to FLT ↓		215		ms
t_{QOD}	QOD enable timer	$V_{SD(F)}$ < $V_{EN/UVLO}$ < $V_{UVLO(F)}$		4.66		ms
$t_{Discharge}$	QOD discharge time (90% to 10% of V_{OUT})	$V_{SD(F)}$ < $V_{EN/UVLO}$ < $V_{UVLO(F)}$, V_{IN} = 12V, C_{OUT} = 1mF		588		ms
t_{PGA}	PG assertion delay			20		µs

6.8 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. V_{IN} = 12V, R_{OUT} = 500Ω, C_{OUT} = 1mF

PARAMETER		C_{dVdt} = 3.3 nF	C_{dVdt} = 33 nF	UNITS
SR_{ON}	Output rising slew rate B0/1/3 variant	13.54	1.65	V/ms
SR_{ON}	Output rising slew rate B2 variant	12.35	4.15	V/ms
$t_{D,ON}$	Turn on delay B0/1/3 variant	0.37	1.71	ms
$t_{D,ON}$	Turn on delay B2 variant	0.375	0.713	ms
t_R	Rise time B0/1/3 variant	0.71	5.83	ms
t_R	Rise time B2 variant	0.72	2.313	ms
t_{ON}	Turn on time B0/1/3 variant	1.078	7.541	ms
t_{ON}	Turn on time B2 variant	1.096	3.026	ms
$t_{D,OFF}$	Turn off delay	1.124	1.124	µs
t_F	Fall time	Depends on R_{OUT} and C_{OUT}		µs

6.9 Typical Characteristics

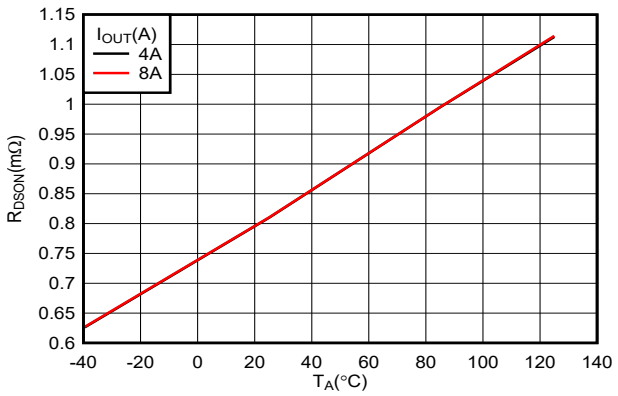


図 6-1. ON Resistance vs Temperature

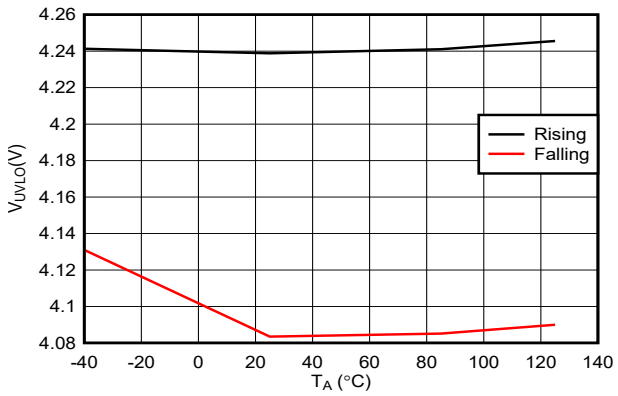


図 6-2. VIN Undervoltage Thresholds vs Temperature

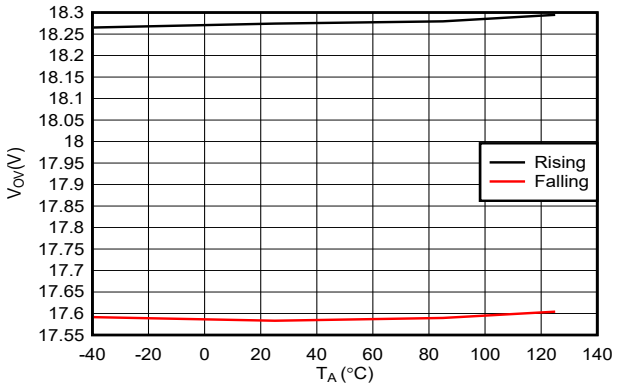


図 6-3. VIN Overvoltage Protection vs Temperature

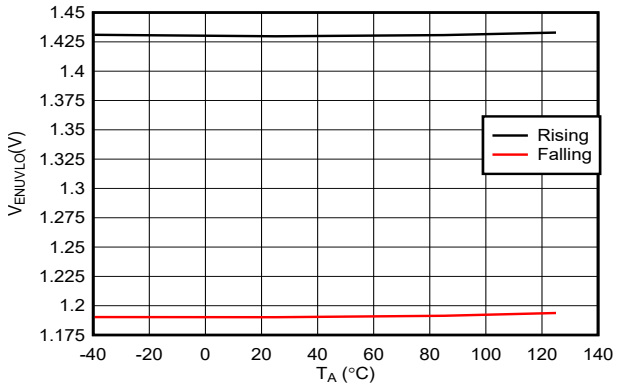


図 6-4. EN/UVLO Thresholds for FET turn-off vs Temperature

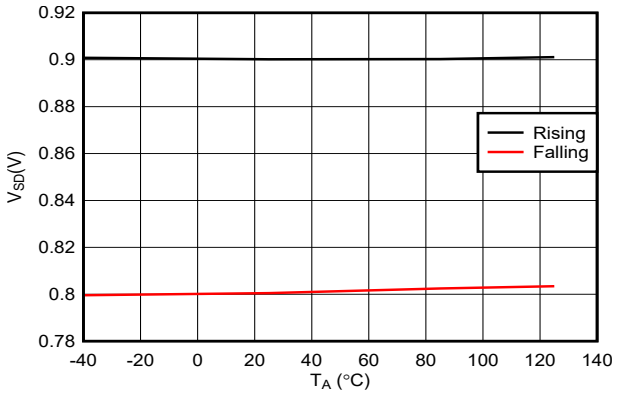


図 6-5. EN/UVLO Based Thresholds for Device Shutdown vs Temperature

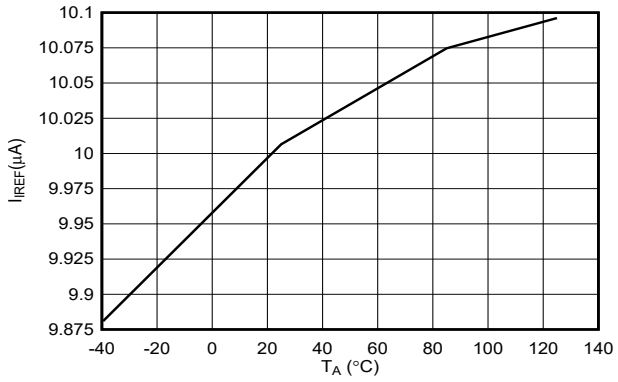


図 6-6. IREF Charging Current vs Temperature

6.9 Typical Characteristics (continued)

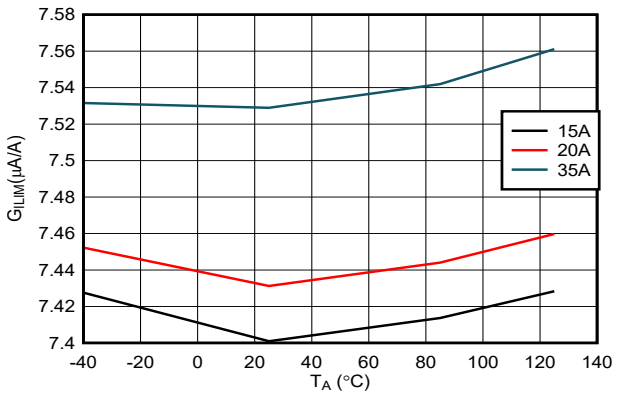


図 6-7. ILIM Gain at different Load Currents vs Temperature

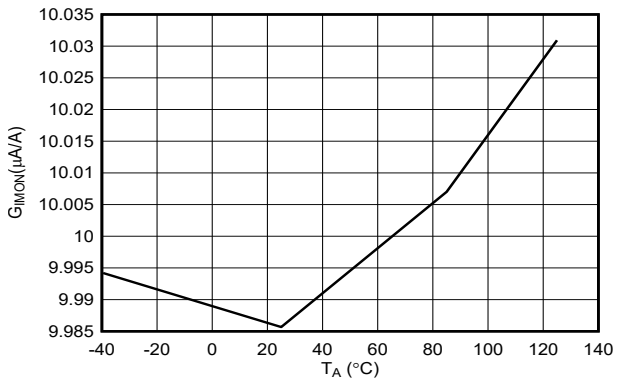


図 6-8. IMON Gain vs Temperature

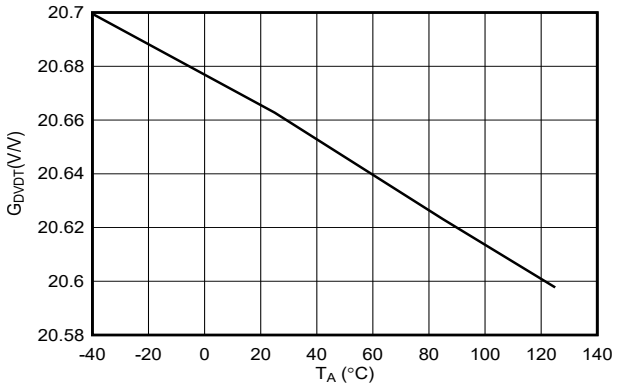


図 6-9. DVDT Gain vs Temperature

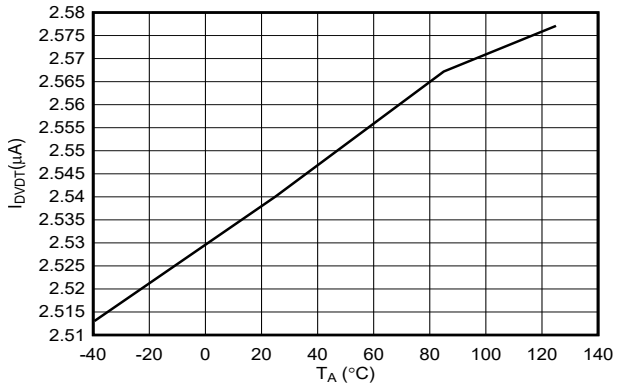


図 6-10. DVDT Charging Current vs Temperature

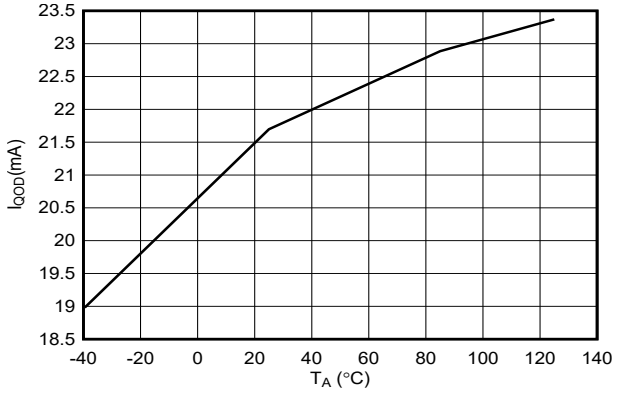


図 6-11. QOD Sink Current vs Temperature

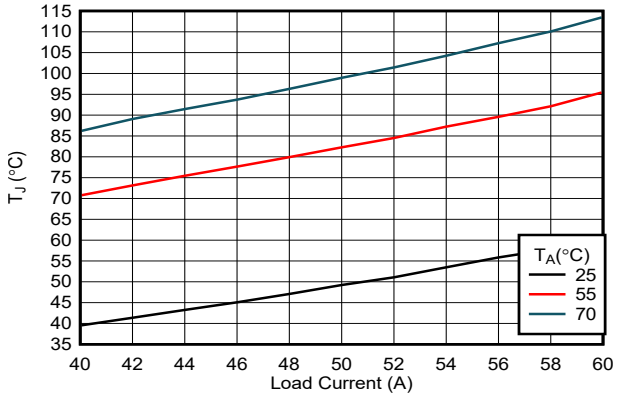


図 6-12. Junction Temperature vs Load Current (No Air Flow)

6.9 Typical Characteristics (continued)

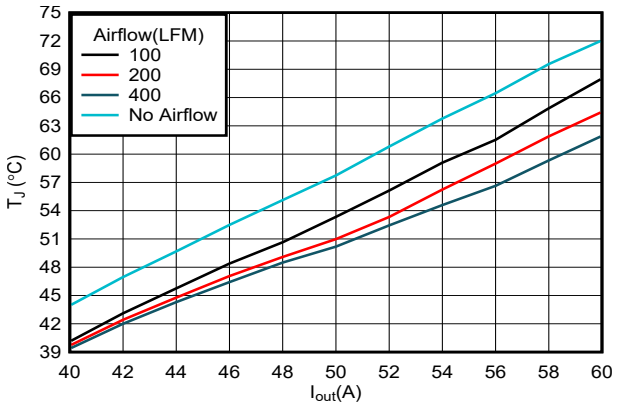


図 6-13. Junction Temperature vs Load Current (T_A = 25ºC, with Air-flow)

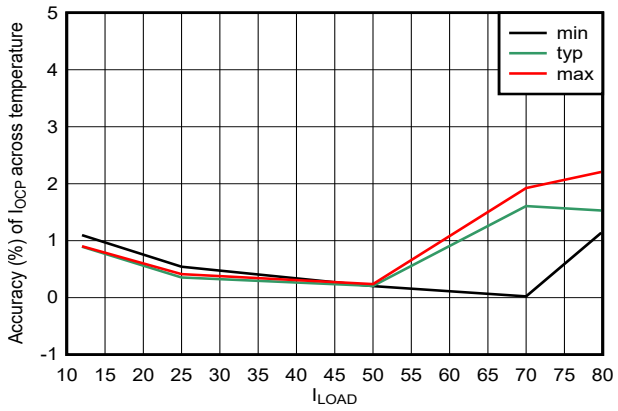


図 6-14. I_{OCP} Accuracy vs Load Current

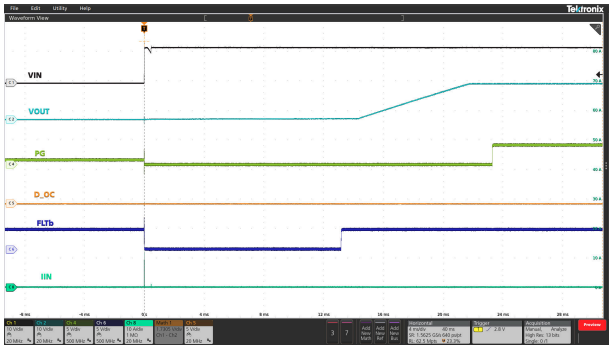


図 6-15. Input Hot-Plug With Insertion Delay for B0/1/3 Variants

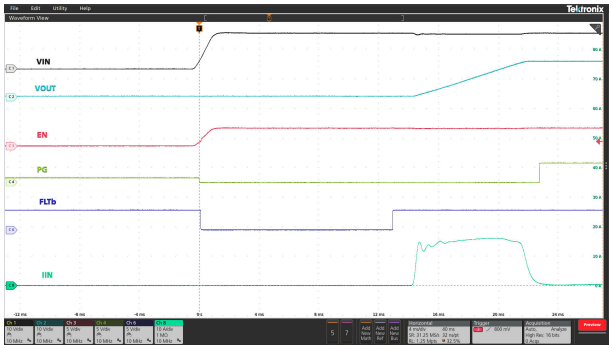


図 6-16. Power Up Control Using Input Supply

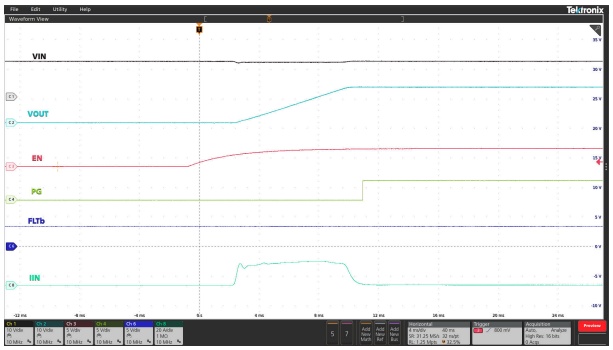


図 6-17. Power-Up Control Using EN/UVLO Pin for B0/1/3 Variants

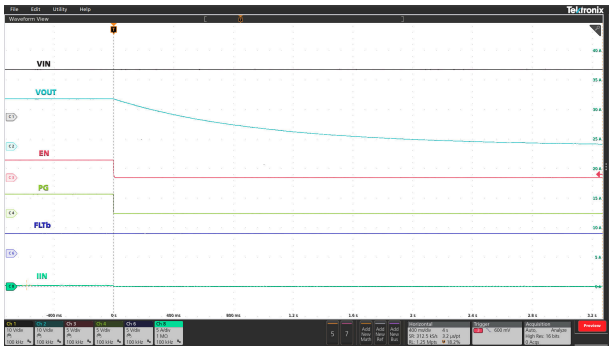
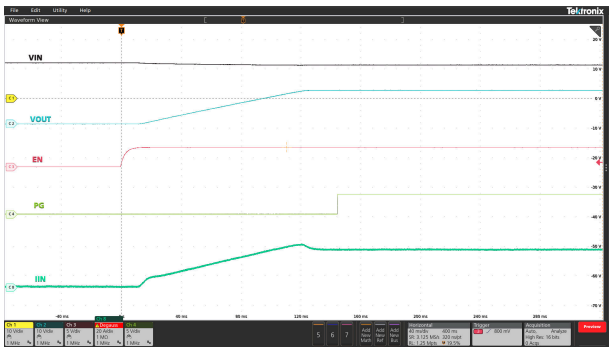


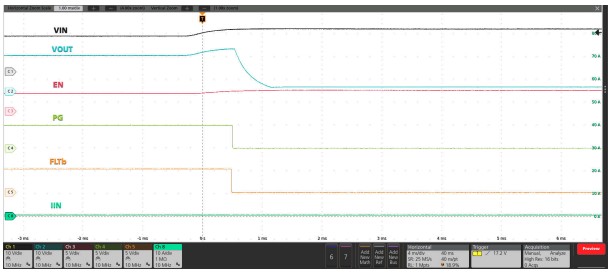
図 6-18. Power-Down Control Using EN/UVLO Pin

6.9 Typical Characteristics (continued)



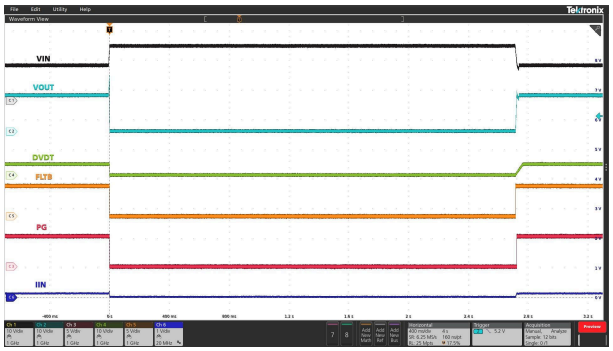
TPS25984B0 variant. C_{OUT} = 8mF, C_{DVDT} = 33nF

図 6-19. Inrush Current Control With Capacitive Load



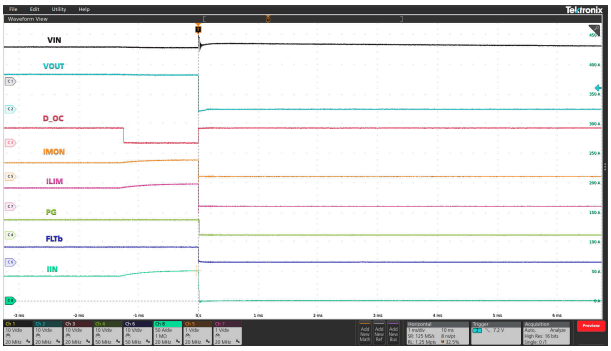
Input supply ramped up above $V_{OVP(R)}$.

図 6-20. Input Overvoltage Protection Response



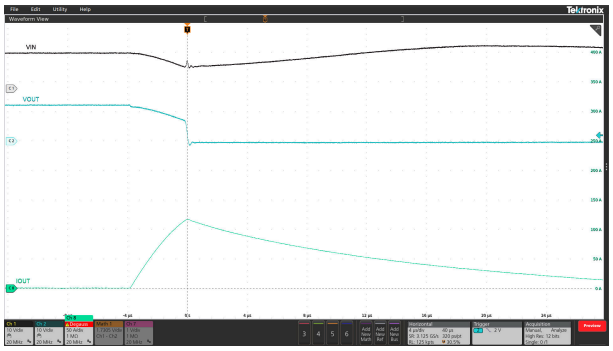
Input supply ramped up above $V_{OVP(R)}$ trigger OVP response and ramped down below $V_{OVP(F)}$.

図 6-21. Input Overvoltage Protection Response Followed by Recovery



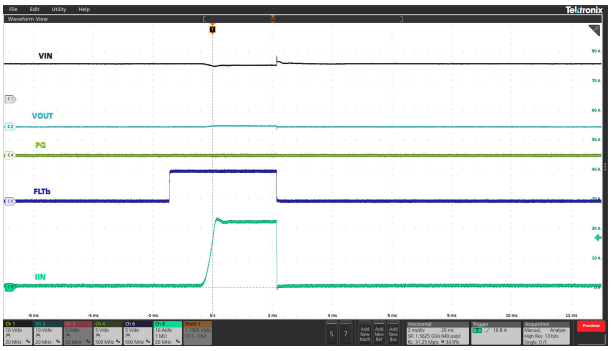
I_{OCP} = 55A. I_{OUT} stays above I_{OCP} threshold persistently to trigger circuit-breaker response for the B0/1/2 variants.

図 6-22. Overcurrent Protection Response (Circuit-Breaker) for B0/1/2 Variants



I_{OCP} = 55A. Output hard short to GND while in steady-state. I_{OUT} rises above 2×I_{OCP} triggers fast-trip response.

図 6-23. Short-Circuit Protection Response



Device turned on using EN/UVLO pin with output hard-short to GND. Device limits the current with foldback and then hits thermal shutdown.

図 6-24. Power-Up Into Short-Circuit

7 Detailed Description

7.1 Overview

The TPS25984Bx is an integrated hotswap protection (eFuse) device that is used to manage load voltage and load current. The device starts its operation by monitoring IN bus. When V_{IN} exceeds the Undervoltage Protection (UVP) threshold, the device waits for the insertion delay timer duration to allow the supply to stabilize before starting up. Next the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low, the internal MOSFET is turned off.

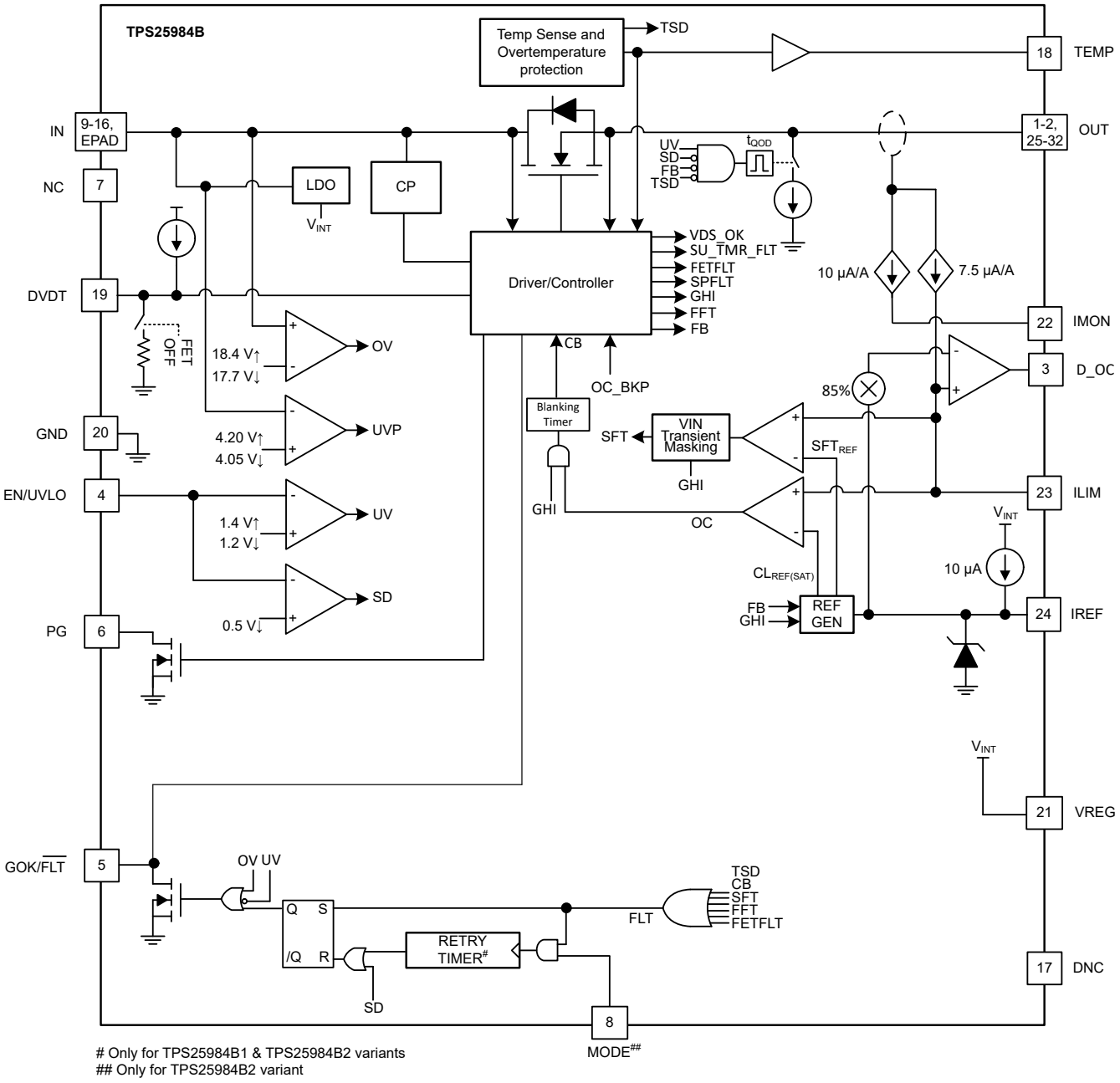
After a successful start-up sequence, the TPS25984Bx device now actively monitors its load current and input voltage, and controls the internal FET to ensure that the programmed overcurrent threshold is not exceeded and input overvoltage spikes are cut off. This action keeps the system safe from harmful levels of voltage and current. At the same time, a fixed internal overcurrent blanking timer allows the system to pass transient peaks in the load current profile without tripping the eFuse. Similarly, voltage transients on the supply line are intelligently masked to prevent nuisance trips. This feature ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device has integrated high accuracy and high bandwidth analog load current monitor, which allows the system to precisely monitor the load current in steady state as well as during transients. This feature facilitates the implementation of advanced dynamic platform power management techniques such as Intel® PSYS to maximize system power usage and throughput without sacrificing safety and reliability.

For systems needing higher load current support, multiple TPS25984Bx eFuses can be connected in parallel. All devices share current during start-up to avoid over-stressing some of the devices more than others which can result in premature or partial shutdown of the parallel chain.

The device has integrated protection circuits to ensure device safety and reliability under recommended operating conditions. The internal FET SOA is protected at all times using the thermal shutdown mechanism, which turns off the FET whenever the junction temperature (T_J) becomes too high for the FET to operate safely.

7.2 Functional Block Diagram



Only for TPS25984B1 & TPS25984B2 variants
Only for TPS25984B2 variant

7.3 Feature Description

The TPS25984Bx eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

7.3.1 Undervoltage Protection

The TPS25984Bx implements undervoltage lockout on VIN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage lockout has a default internal threshold of V_{UVPIN} on VIN. Alternatively, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. 図 7-1 and 式 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

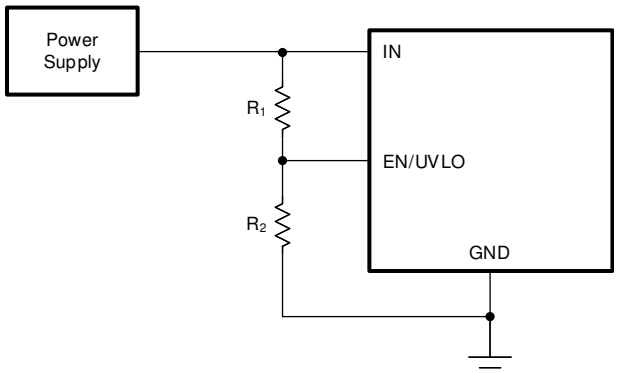


図 7-1. Adjustable Undervoltage Protection

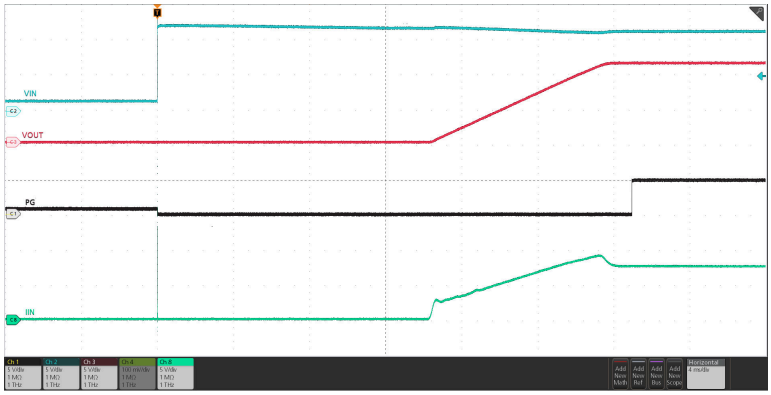
$$V_{IN(UV)} = V_{UVLO(R)}\frac{R_1 + R_2}{R_2} \quad (1)$$

The EN/UVLO pin implements a bi-level threshold.

1. $V_{EN} > V_{UVLO(R)}$: Device is fully ON.
2. $V_{SD(F)} < V_{EN} < V_{UVLO(F)}$: The FET along with most of the controller circuitry is turned OFF, except for some critical bias and digital circuitry. Holding the EN/UVLO pin in this state for > t_{QOD} activates the Output Discharge function.
3. $V_{EN} < V_{SD(F)}$: All active circuitry inside the part is turned OFF and it retains no digital state memory. It also resets any latched faults. In this condition, the device quiescent current consumption is minimal.

7.3.2 Insertion Delay

The TPS25984Bx implements insertion delay at start-up to ensure the supply has stabilized before the device tries to turn on the power to the load. The device initially waits for the VIN supply to rise above the UVP threshold and all the internal bias voltages to settle. After that, the device remains off for an additional delay of t_{INSDLY} irrespective of the EN/UVLO pin condition. This action helps to prevent any unexpected behavior in the system if the device tries to turn on before the card has made firm contact with the backplane or if there is any supply ringing or noise during start-up.



Input supply stepped up from 0V to 12V. Device waits for t_{INSDLY} for input supply to stabilize before it turns on the output.

図 7-2. Insertion Delay

7.3.3 Overvoltage Protection

The TPS25984Bx implements overvoltage lockout to protect the load from input overvoltage conditions. The OVP comparator on the IN pin uses a fixed internal overvoltage protection threshold. If the input voltage on IN exceeds the OVP rising threshold ($V_{OVP(R)}$), the power FET is turned OFF within t_{OVP}. After the voltage on IN falls below the OVP falling threshold ($V_{OVP(F)}$), the FET is turned ON in a dVdt controlled manner.

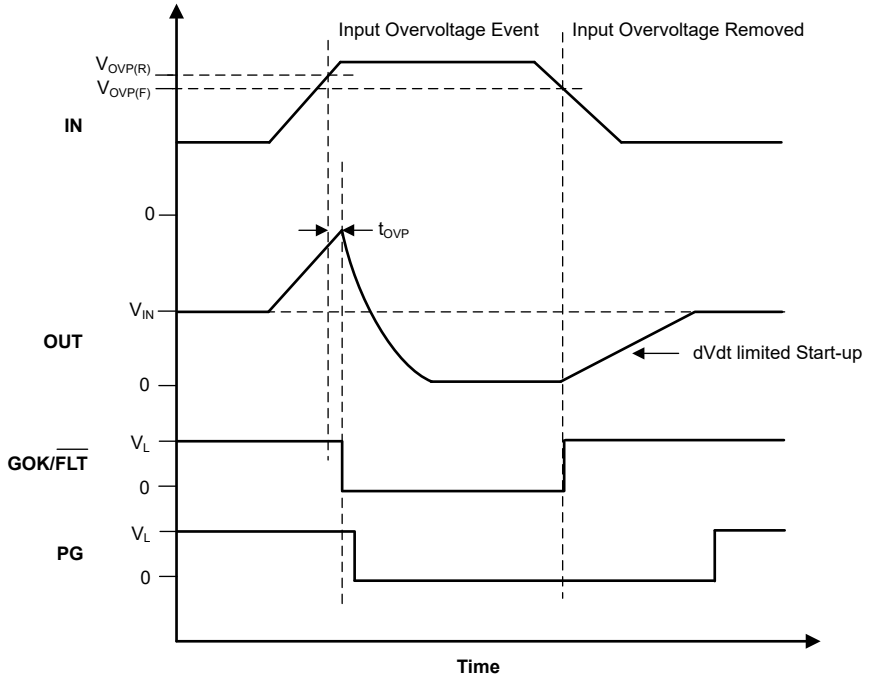


図 7-3. Input Overvoltage Protection Response

7.3.4 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS25984Bx incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Active current limit with an adjustable threshold (I_{LIM}) for overcurrent protection during start-up
3. Circuit-breaker with an adjustable threshold (I_{OCP}) and fixed internal blanking timer (t_{ITIMER}) for overcurrent protection during steady-state
4. Fast-trip response to severe overcurrent faults with an adjustable threshold (I_{SFT} = 2 × I_{OCP}) to quickly protect against severe short-circuits under all conditions, as well as a fixed threshold (I_{FFT}) during steady state

7.3.4.1 Slew Rate (dVdt) and Inrush Current Control

During hot plug events or while trying to charge a large output capacitance, there can be a large inrush current. If the inrush current is not managed properly, the inrush current can damage the input connectors and cause the system power supply to droop. This action can lead to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. 式 2 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{LOAD}):

$$SR(V/ms) = \frac{I_{INRUSH}(A)}{C_{LOAD}(mF)} \quad (2)$$

A capacitor can be added to the dVdt pin to control the rising slew rate and lower the inrush current during turn-on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using 式 3.

For B0/1/3 variants:

$$C_{DVDT}(pF) = \frac{51300}{SR(V/ms)} \quad (3)$$

For B2 variant:

$$C_{DVDT}(pF) = \frac{135000}{SR(V/ms)} \quad (4)$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

注

1. High input slew rates in combination with high input power path inductance can result in oscillations during start-up. This can be mitigated using one or more of the following steps:
   a. Reduce the input inductance.
   b. Increase the capacitance on VIN pin.
   c. Increase the dVdt pin capacitance to reduce the slew rate or increase the start-up time. TI recommends using a minimum start-up time of 5ms.

7.3.4.1.1 Start-Up Time Out

If the start-up is not completed, that is, the FET is not fully turned on within a certain timeout interval (t_{SU_TMR}) after the device is enabled, the device registers it as a fault. GOK/$\overline{FLT}$ is asserted low and the device goes into latch-off or auto-retry mode depending on the device configuration.

7.3.4.2 Steady-State Overcurrent Protection (Circuit-Breaker)

The TPS25984Bx responds to output overcurrent conditions during steady-state by performing a circuit-breaker action after an internal transient fault blanking interval. This action allows the device to support a higher peak current for a short interval but also ensures robust protection in case of persistent output faults.

The device constantly senses the output load current and provides an analog current output (I_{ILIM}) on the ILIM pin which is proportional to the load current, which in turn produces a proportional voltage (V_{ILIM}) across the ILIM pin resistor (R_{ILIM}) as per 式 5.

$$V_{ILIM} = I_{OUT} \times G_{ILIM} \times R_{ILIM} \quad (5)$$

Where G_{ILIM} is the current monitor gain (I_{ILIM} : I_{OUT})

The overcurrent condition is detected by comparing this voltage against the voltage on the IREF pin as a reference. The reference voltage (V_{IREF}) can be controlled in two ways, which sets the overcurrent protection threshold (I_{OCP}) accordingly.

- The internal current source interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage as shown in 式 6.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (6)$$

- It is also possible to drive the IREF pin from an external low impedance reference voltage source.

The overcurrent protection threshold during steady-state (I_{OCP}) can be calculated using 式 7.

$$I_{OCP} = \frac{0.75 \times V_{IREF}}{G_{ILIM} \times R_{ILIM}} \quad (7)$$

注

Maintain V_{IREF} within the recommended voltage range to ensure proper operation of the overcurrent detection circuit.

TI recommends to add a 150pF capacitor from IREF pin to GND for improved noise immunity.

After an overcurrent condition is detected, that is the load current exceeds the programmed current limit threshold (I_{OCP}), but stays lower than the short-circuit threshold (2 × I_{OCP} or I_{FFT} whichever is lower), the device starts an internal blanking timer. If the load current drops below the current limit threshold before the timer expires, the circuit-breaker action is not engaged. This action allows transient load pulses to pass through the device without tripping the circuit. If the overcurrent condition persists for longer than the timer duration (t_{ITIMER}), the circuit-breaker action turns off the FET immediately.

式 8 can be used to calculate the R_{ILIM} value for the desired overcurrent threshold.

$$R_{ILIM} = \frac{0.75 \times V_{IREF}}{G_{ILIM} \times I_{OCP}} \quad (8)$$

図 7-4 illustrates the overcurrent response for TPS25984Bx eFuse. After the part shuts down due to a circuit-breaker fault, it either stays latched off (TPS25984B2 variant with MODE pin floating or TPS25984B0/3 variants) or restarts automatically after a fixed delay (TPS25984B2 variant with MODE pin connected to GND or TPS25984B1 variant).

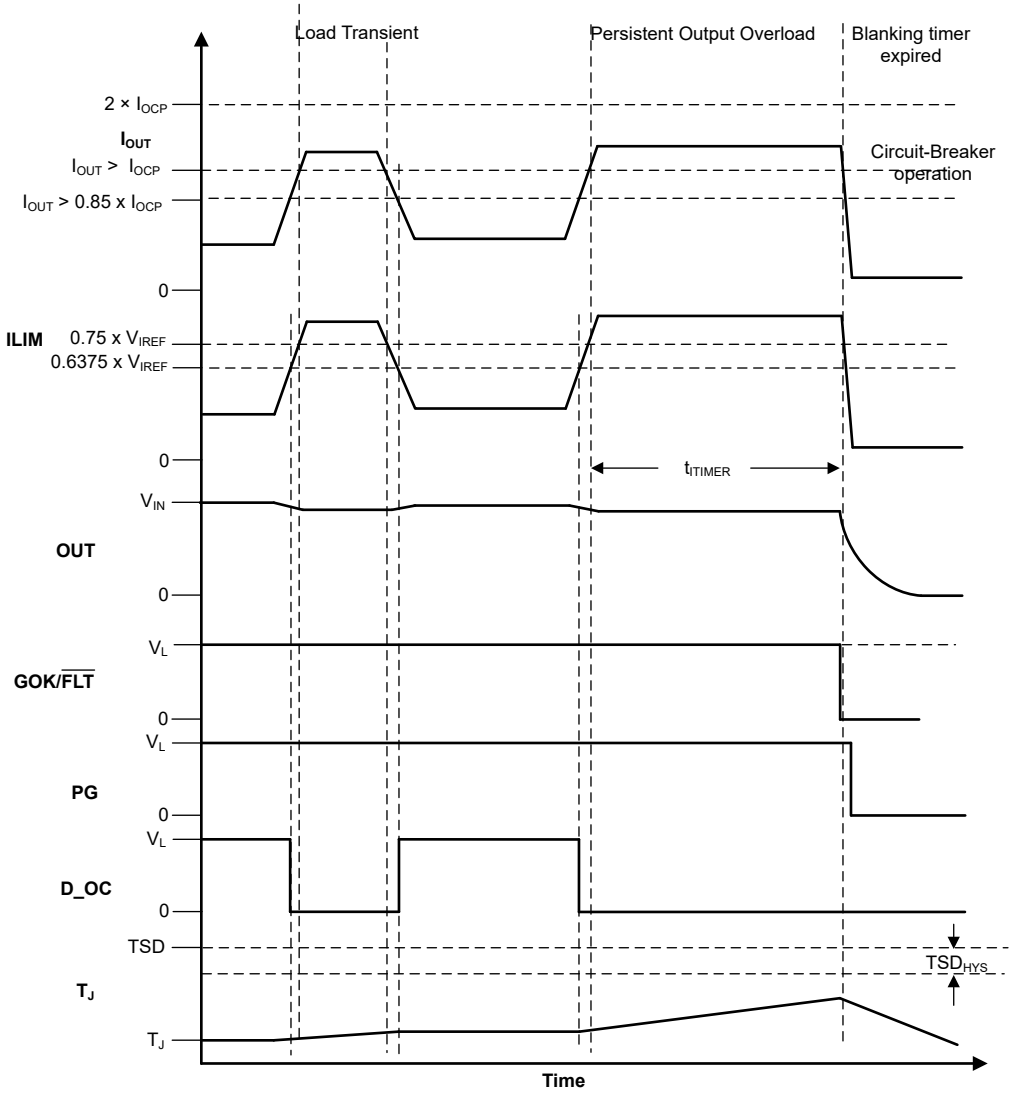


図 7-4. Steady-State Overcurrent (Circuit-Breaker) Response

7.3.4.3 Active Current Limiting During Start-Up

The TPS25984Bx responds to output overcurrent conditions during start-up by actively limiting the current. The device constantly senses the current flowing through each one (I_{DEVICE}) and provides an analog current output (I_{ILIM}) on the ILIM pin, which in turn produces a proportional voltage (V_{ILIM}) across the ILIM pin resistor (R_{ILIM}) as per 式 9.

$$V_{ILIM} = I_{DEVICE} \times G_{ILIM} \times R_{ILIM} \quad (9)$$

Where G_{ILIM} is the current monitor gain (I_{ILIM} : I_{DEVICE})

The overcurrent condition is detected by comparing this voltage against a threshold which is a scaled voltage ($CLREF_{SAT}$) derived from the reference voltage (V_{IREF}) on the IREF pin as presented in 式 10.

$$CLREF_{SAT} = 0.4 \times V_{IREF} \quad (10)$$

The reference voltage (V_{IREF}) can be controlled in two ways, which sets the start-up current limit threshold (I_{LIM}) accordingly.

1. In the standalone mode of operation, the internal current source interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage as shown in 式 11.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (11)$$

The active current limit (I_{LIM}) threshold during start-up can be calculated using 式 12.

$$I_{ILIM} = \frac{CLREF_{SAT}}{G_{ILIM} \times R_{ILIM}} \quad (12)$$

When the load current through the device during start-up exceeds I_{LIM}, the device tries to regulate and hold the load current at I_{LIM}.

During current regulation, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the FET is turned off. After the part shuts down due to a TSD fault, it either stays latched off (TPS25984B2 variant with MODE pin floating or TPS25984B0/3 variants) or restarts automatically after a fixed delay (TPS25984B2 variant with MODE pin connected to GND or TPS25984B1 variant). See *Overtemperature protection* section for more details on device response to overtemperature.

注

The active current limit block employs a foldback mechanism during start-up based on the output voltage (V_{OUT}). When V_{OUT} is below the foldback threshold (V_{FB}), the current limit threshold is further lowered.

7.3.4.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When an output short-circuit is detected, the internal fast-trip comparator triggers a fast protection sequence to prevent the current from building up further and causing any damage or excessive input supply droop. The fast-trip comparator employs a scalable threshold (I_{SFT}) which is equal to 2 × I_{OCP} during steady-state and 1.5 × I_{LIM} during inrush. This action enables the user to adjust the fast-trip threshold as per system rating, rather than using a high fixed threshold which can not be suitable for all systems. After the current exceeds the fast-trip threshold, the TPS25984Bx turns off the FET within t_{SFT}. The device also employs a higher fixed fast-trip threshold (I_{FFT}) to provide fast protection against hard short-circuits during steady-state (FET in linear region). After the current exceeds I_{FFT}, the FET is turned off completely within t_{FFT}. 図 7-5 illustrates the short-circuit response for TPS25984Bx eFuse.

In some of the systems, for example blade servers and telecom equipment which house multiple hot-pluggable blades or line cards connected to a common supply backplane, there can be transients on the supply due to switching of large currents through the inductive backplane. This can result in current spikes on adjacent cards which can potentially be large enough to trigger the fast-trip comparator of the eFuse. The TPS25984Bx uses a proprietary algorithm to avoid nuisance tripping in such cases thereby facilitating uninterrupted system operation.

After the part shuts down due to a short-circuit fault, it either stays latched off (TPS25984B2 variant with MODE pin floating or TPS25984B0/3 variants) or restarts automatically after a fixed delay (TPS25984B2 variant with MODE pin connected to GND or TPS25984B1 variant).

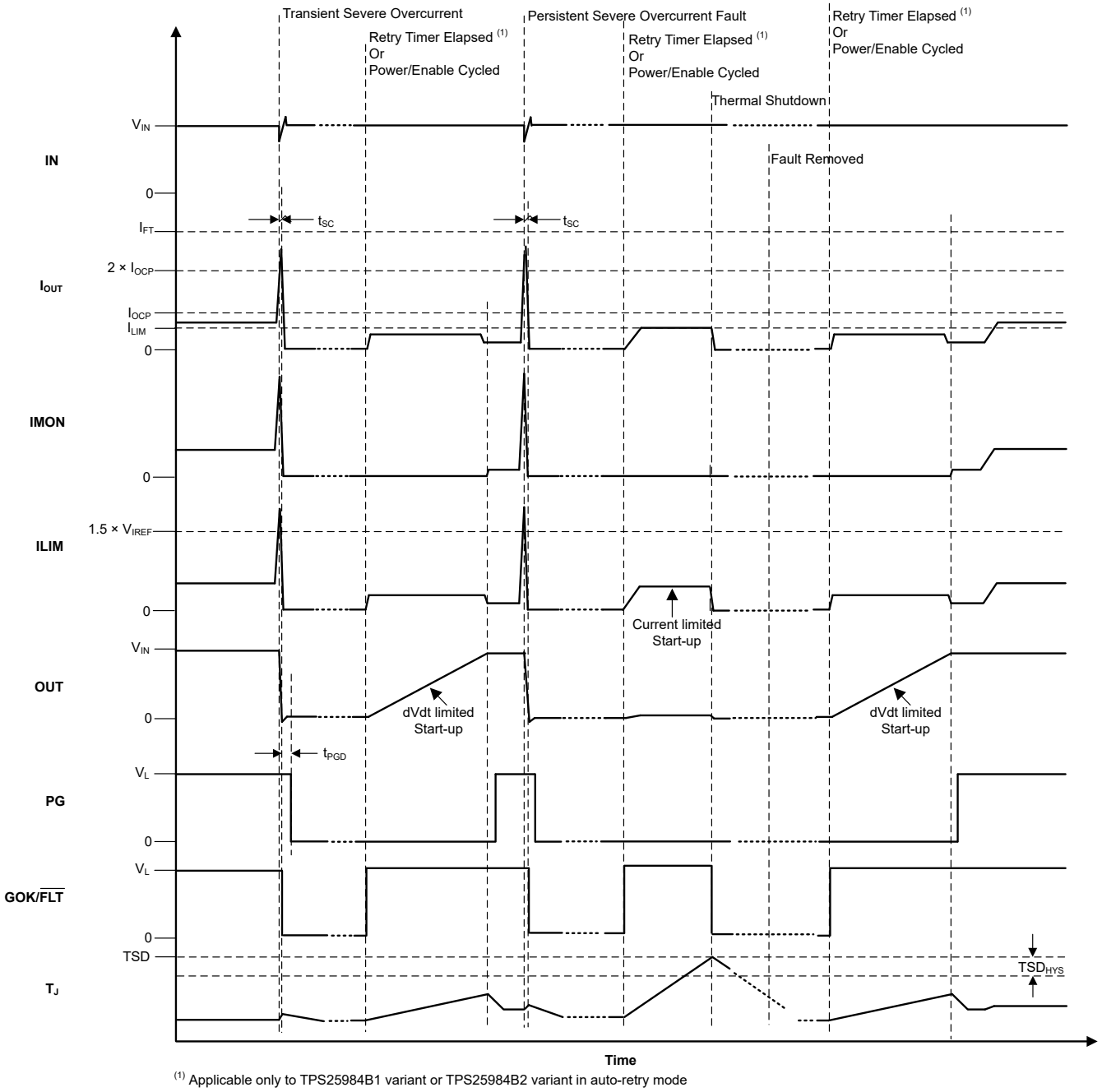


図 7-5. Short-Circuit Response

7.3.5 Analog Load Current Monitor (IMON)

The TPS25984Bx allows the system to monitor the output load current accurately by providing an analog current on the IMON pin which is proportional to the current through the FET. The benefit of having a current output is that the signal can be routed across a board without adding significant errors due to voltage drop or noise coupling from adjacent traces. The current output also allows the IMON pins of multiple TPS25984Bx devices to be tied together to get the total current of the system in a parallel eFuse configuration. The IMON signal can be converted to a voltage by dropping it across a resistor at the point of monitoring. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current using 式 13.

$$I_{OUT} = \frac{V_{IMON}}{G_{IMON} \times R_{IMON}} \quad (13)$$

The TPS25984Bx IMON circuit is designed to provide high bandwidth and high accuracy across load and temperature conditions, irrespective of board layout and other system operating conditions. This design allows the IMON signal to be used for advanced dynamic platform power management techniques such as PROCHOT ™ or Intel PSYS™ to maximize system power usage and platform throughput without sacrificing safety or reliability.

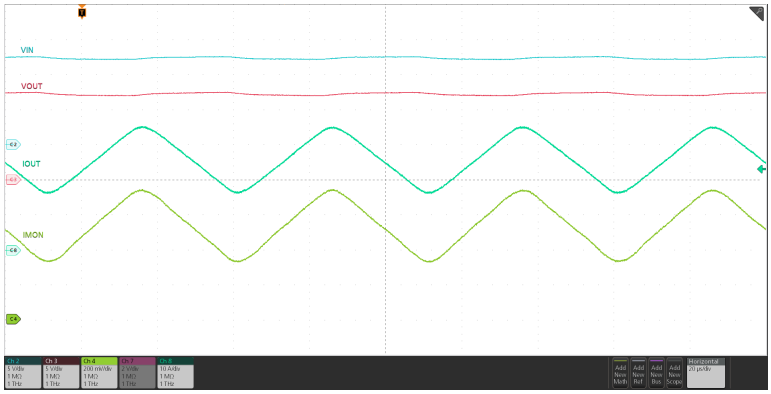


図 7-6. Analog Load Current Monitor Response

注

1. TI recommends using the IMON pin for load current monitoring information only during steady-state. During inrush, the IMON pin reports load current with higher error.
2. The IMON pins of multiple TPS25984Bx devices can be tied together to monitor the total system current even if the eFuses are operating independently, or in other words not connected together in a stacked or parallel configuration.
3. The ILIM pin reports the individual device load current at all times and can also be used as an analog load current monitor for each individual device.
4. Care must be taken to minimize parasitic capacitance on the ILIM pin to avoid any impact on the start-up current limit protection and short-circuit protection timing.

7.3.6 Mode Selection (MODE)

This pin can be used to configure the fault response beahvior for the TPS25984B2 variants.

Leaving the pin open configures it as a latch-off device. Connecting this pin to GND configures it as a auto-retry device.

7.3.7 Digital Overcurrent Indication (D_OC)

This is an active low output which is asserted low to indicate when the device has detected an overcurrent condition. The overcurrent detection is based on whether the load current exceeds 85% of the OCP threshold.

7.3.8 Stacking Multiple eFuses for Scalability

For systems needing higher current than supported by a single TPS25984Bx, multiple TPS25984Bx devices can be connected in parallel to deliver the total system current.

This configuration is achieved by connecting all the devices as follows:

1. DVDT is connected through capacitor to GND.
2. IREF is connected through resistor to GND.
3. IMON is connected through resistor to GND.
4. ILIM is connected through resistor to GND.

The following pins of all devices must be connected together:

1. IN
2. OUT
3. EN/UVLO
4. DVDT
5. D_OC
6. IMON
7. IREF
8. GOK/$\overline{\text{FLT}}$
9. TEMP

7.3.8.1 Current Balancing During Start-Up

The TPS25984Bx implements a proprietary current balancing mechanism during start-up, which allows multiple TPS25984Bx devices connected in parallel to share the inrush current and distribute the thermal stress across all the devices. This feature helps to complete a successful start-up with all the devices and avoid a scenario where some of the eFuses hit thermal shutdown prematurely. This in effect increases the inrush current capability of the parallel chain. The improved inrush performance makes it possible to support very large load capacitors on high current platforms without compromising the inrush time or system reliability.

7.3.9 Analog Junction Temperature Monitor (TEMP)

The device allows the system to monitor the junction temperature (T_J) accurately by providing an analog voltage on the TEMP pin which is proportional to the temperature of the die. This voltage can be connected to the ADC input of a host controller or eFuse with digital telemetry. In a multi-device parallel configuration, the TEMP outputs of all devices can be tied together. In this configuration, the TEMP signal reports the temperature of the hottest device in the chain.

注

1. The TEMP pin voltage is used only for external monitoring and does not interfere with the overtemperature protection scheme of each individual device which is based purely on the internal temperature monitor.
2. TI recommends to add a capacitance (not exceeding 100nF) on the TEMP pin to filter out glitches during system transients.
3. Adding resistive load to TEMP pin may lead to deviation from the specified VTEMP pin gain value.

7.3.10 Overtemperature Protection

The TPS25984Bx employs an internal thermal shutdown mechanism to protect itself when the internal FET becomes too hot to operate safely. When the TPS25984B0/3 or TPS25984B2 (with MODE pin left floating) detects thermal overload, it shuts down and remains latched-off until the device is power cycled or re-enabled. When the TPS25984B1 or TPS25984B2 (with MODE pin connected to GND) detects thermal overload, it remains off until it has cooled down sufficiently. Thereafter, the device remains off for an additional delay of t_{RST} after which it automatically retries to turn on if it is still enabled.

表 7-1. Overtemperature Protection Summary

Device	Enter TSD	Exit TSD
TPS25984B0/3 (Latch-Off) or TPS25984B2 (with MODE pin left floating)	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ VDD cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$
TPS25984B1 (Auto-Retry) or TPS25984B2 (with MODE pin connected to GND)	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ t_{RST} timer expired or VDD cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$

7.3.11 Fault Response and Indication (GOK/$\overline{FLT}$)

GOK/$\overline{FLT}$ pin acts as an fault indicator output and also as an input to sense and synchronize faults between parallel eFuses.

表 7-2 summarizes the device response to various fault conditions.

表 7-2. Fault Summary

Event or Condition	Device Response	Fault Latched Internally	GOK/$\overline{FLT}$ Pin Status	Delay
Steady-state	None	N/A	H	
Inrush	None	N/A	H	
Overtemperature	Shutdown	Y	L	
Undervoltage (EN/UVLO)	Shutdown	N	L	
Undervoltage (VIN UVP) at startup	Shutdown	N	L	Till Insertion Delay
Undervoltage (VIN UVP) in steady state	Shutdown	N	H	
Overvoltage (VIN OVP)	Shutdown	N	L	
Transient overcurrent	None	N	H	
Persistent overcurrent (steady-state)	Circuit-Breaker	Y	L	t_{ITIMER}
Persistent overcurrent (start-up)	Current Limit	N	L	
Short-circuit	Fast-trip	Y	L	t_{FT}
Start-up timeout	Shutdown	Y	L	t_{SU_TMR}
FET health fault (G-S)	Shutdown	Y	L	10 µs
FET health fault (G-D)	Shutdown	Y	L	

注

GOK/$\overline{FLT}$ is an open-drain pin and must be pulled up to an external supply.

For faults that are latched internally, power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD(F)}$ clears the fault and the pin is de-asserted. This action also clears the t_{RST} timer (auto-retry mode only). Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition. This is true for both latch-off and auto-retry modes of operation.

7.3.12 Power-Good Indication (PG)

Power-Good indication is an active high output which is asserted high to indicate when the device is in steady-state and capable of delivering maximum power.

表 7-3. PG Indication Summary

Event or Condition	FET Status	PG Pin Status	PG Delay
Undervoltage ($V_{EN} < V_{UVLO}$)	OFF	L	t_{PGD}
$V_{IN} < V_{UVP}$	OFF	L	
Overvoltage ($V_{IN} > V_{OVP}$)	OFF	L	t_{PGD}
Steady-state	ON	H	t_{PGA}
Inrush	ON	L	t_{PGA}

表 7-3. PG Indication Summary (続き)

Event or Condition	FET Status	PG Pin Status	PG Delay
Transient overcurrent	ON	H	N/A
Circuit-breaker (persistent overcurrent followed by blanking timer expiry)	OFF	L	t_{PGD}
Fast-trip	OFF	L	t_{PGD}
Overtemperature	Shutdown	L	t_{PGD}

After power up, PG is pulled low initially. The device initiates an inrush sequence in which the gate driver circuit starts charging the gate capacitance from the internal charge pump. When the FET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the device is capable of delivering full power, the PG pin is asserted HIGH after a de-glitch time (t_{PGA}).

The PG is de-asserted if the FET is turned off at any time during normal operation. The PG de-assertion de-glitch time is t_{PGD}.

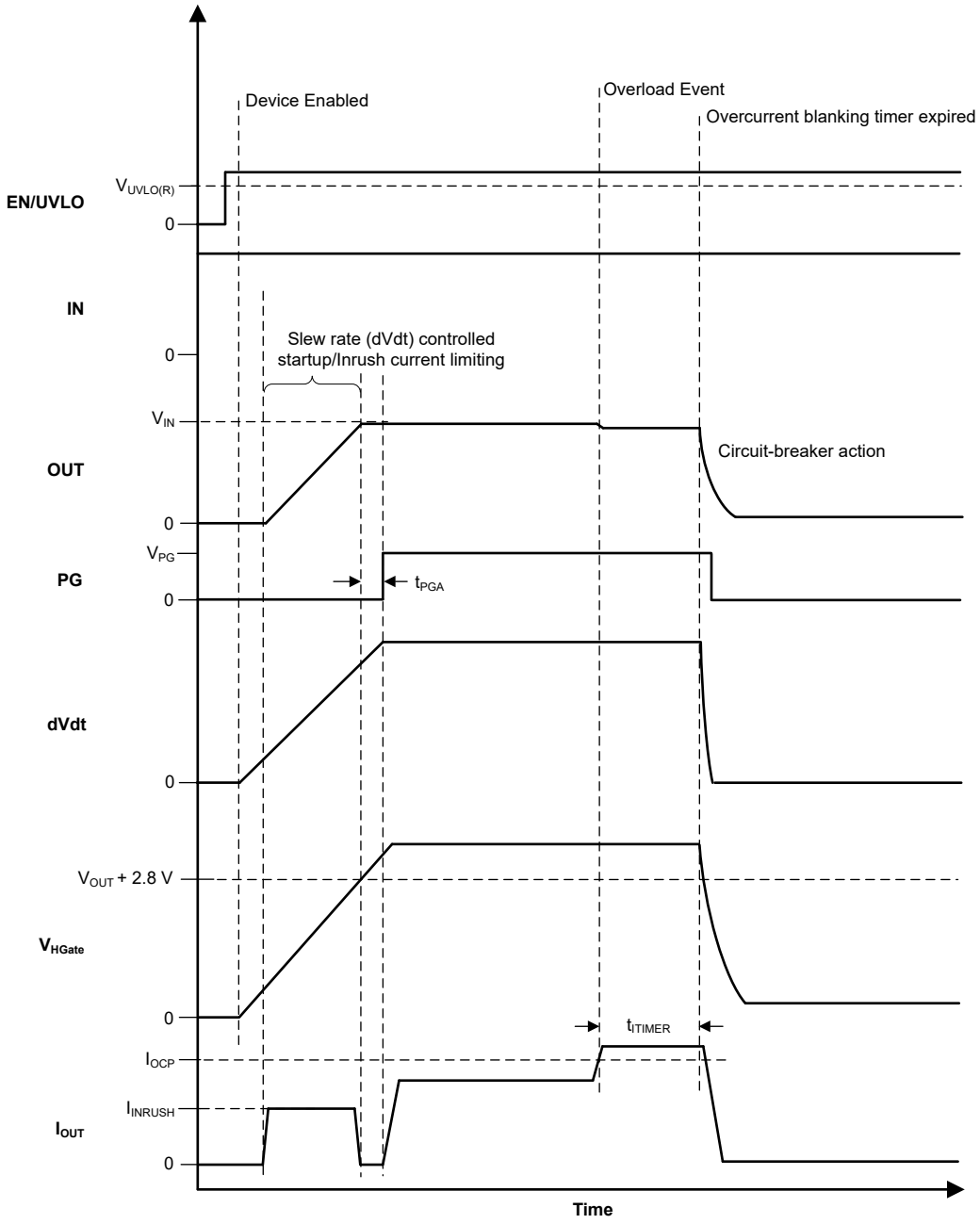


図 7-7. TPS25984Bx PG Timing Diagram

注

The PG is an open-drain output and is recommended to be pulled up to an external supply.

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

7.3.13 Output Discharge

The device has an integrated output discharge function which discharges the capacitors on the OUT pin using an internal constant current (I_{QOD}) to GND. The output discharge function is activated when the EN/UVLO is held low ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$) for a minimum interval (t_{QOD}). The output discharge function helps to rapidly remove the residual charge left on large output capacitors and prevents the bus from staying at some undefined voltage for extended periods of time. The output discharge is disengaged when V_{OUT} < V_{FB} or if the device detects a fault.

The output discharge function can result in excessive power dissipation inside the device leading to an increase in junction temperature (T_J). The output discharge is disabled if the junction temperature (T_J) crosses TSD to avoid long-term degradation of the part.

7.3.14 FET Health Monitoring

The TPS25984Bx can detect and report certain conditions which are indicative of a failure of the power path FET. If undetected or unreported, these conditions can compromise system performance by not providing power to the load correctly or by not providing the necessary level of protection. After a FET failure is detected, the TPS25984Bx tries to turn off the internal FET by pulling the gate low and asserts the GOK/$\overline{FLT}$ pin.

- **G-D short:** The TPS25984Bx detects this kind of FET failure at all times by checking if the gate voltage is close to V_{IN} even when the internal control logic is trying to hold the FET in OFF condition.
- **G-S short:** The TPS25984Bx detects this kind of FET failure during start-up by checking if the FET G-S voltage fails to reach the necessary overdrive voltage within a certain timeout period (t_{SU_TMR}) after the gate driver is turned ON. While in steady-state, if the G-S voltage becomes low before the controller logic has signaled to the gate driver to turn off the FET, it is latched as a fault.

7.4 Device Functional Modes

The features of the device depend on the operating mode. 表 7-4 and 表 7-5 summarize the device functional modes.

表 7-4. Device Functional Modes Based on EN/UVLO Pin

Pin: EN/UVLO	Device State	Output Discharge
> $V_{UVLO(R)}$	Fully ON	Disabled
> $V_{SD(F)}$, < $V_{UVLO(F)}$ (< t_{QOD})	FET OFF	Disabled
> $V_{SD(F)}$, < $V_{UVLO(F)}$ (> t_{QOD})	FET OFF	Enabled
< $V_{SD(F)}$	Shutdown	Disabled

表 7-5. Device Functional Modes Based on MODE Pin (Only for TPS25984B2 variant)

Pin: MODE	Device Configuration
Open	Latch-off
GND	Auto-retry

8 Application and Implementation

注

以下のアプリケーション情報は、テキサス・インスツルメンツの製品仕様に含まれるものではなく、テキサス・インスツルメンツはその正確性も完全性も保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS25984Bx is a high-current eFuse that is typically used for power rail input protection applications. The device operates from 4.5V to 16V with input overvoltage and adjustable undervoltage protection. The device provides the ability to control inrush current and offers protection against overcurrent and short-circuit conditions. The device can be used in a variety of systems such as server motherboards, add-on cards, graphics cards, accelerator cards, enterprise switches, routers, and so forth. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirements. Additionally, a spreadsheet design tool *TPS25984Bx Design Calculator* is available.

8.1.1 Single Device, Standalone Operation

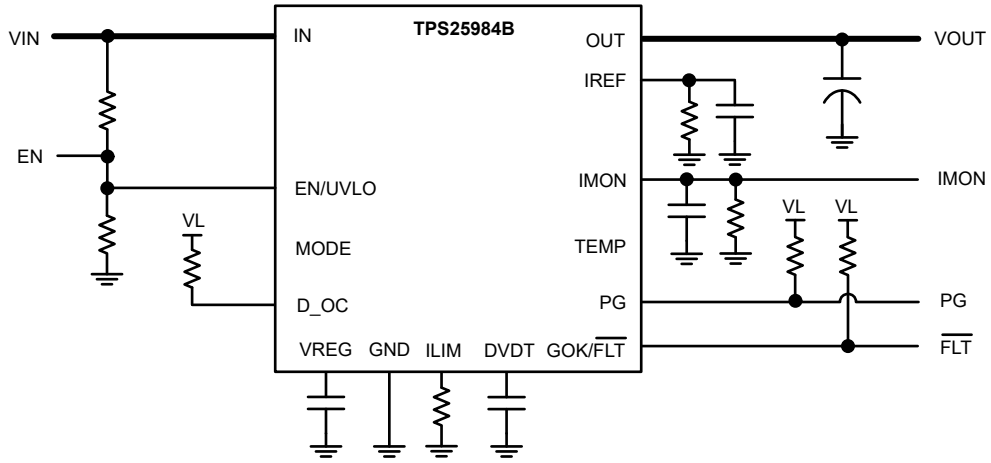


図 8-1. Single Device, Standalone Operation

Other variations:

1. The IREF pin can be driven from an external reference voltage source.
2. In a host MCU controlled system, EN/UVLO can be connected to a GPIO pin to control the device. IMON pin voltage can be monitored using an ADC. The host MCU can use a DAC to drive IREF to change the current limit threshold dynamically.
3. The device can be used as a simple high current load switch without adjustable overcurrent or fast-trip protection by tying the ILIM pin to GND and leaving the IREF pin open. The inrush current protection, fixed fast-trip and internal fixed overcurrent protection are still active in this condition.

8.1.2 Multiple Devices, Parallel Connection

Applications which need higher current capability can use two or more TPS25984Bx devices connected in parallel as shown in 図 8-2.

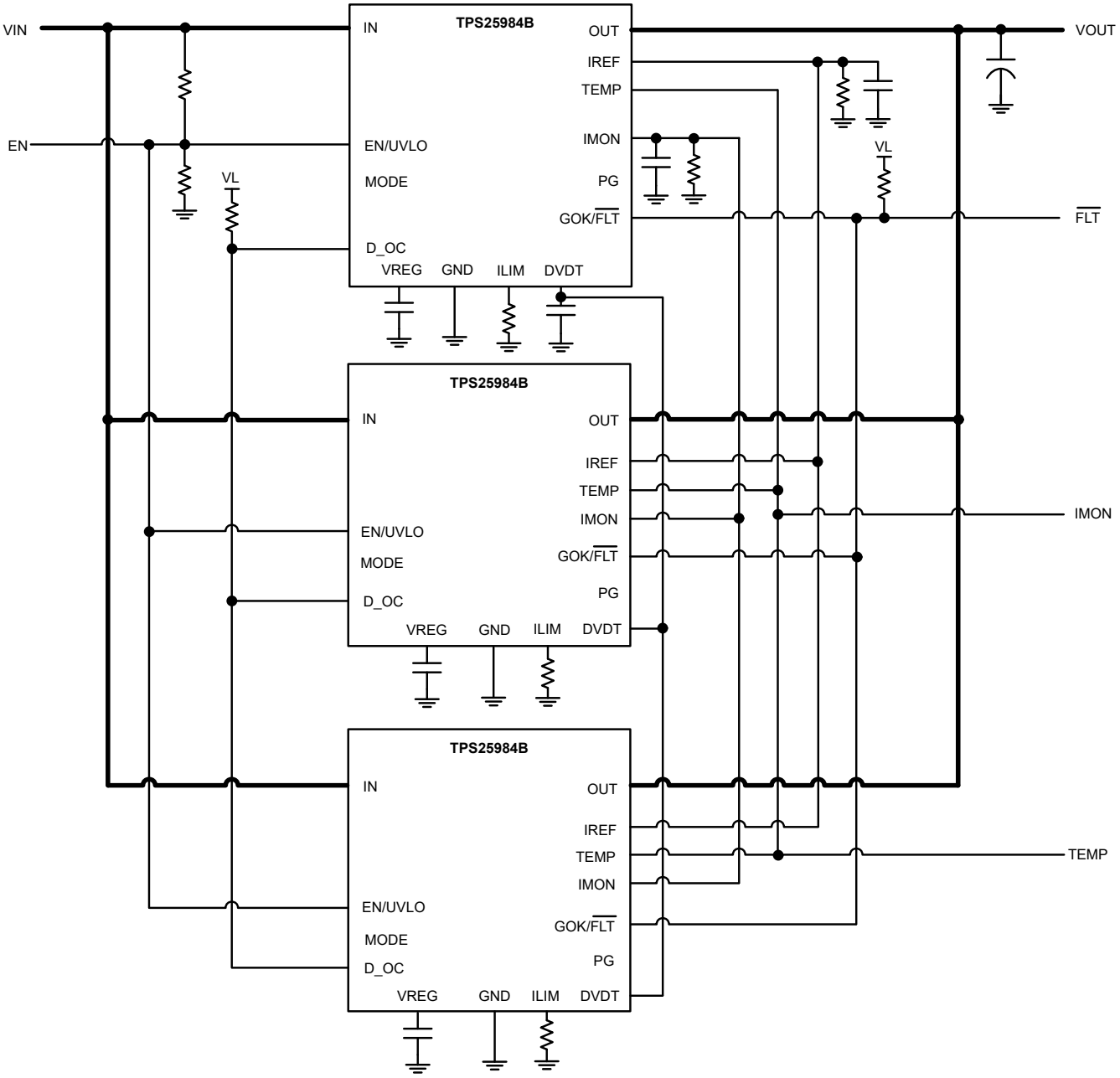


図 8-2. Devices Connected in Parallel for Higher Current Capability

This configuration is achieved by connecting all the devices as follows:

1. DVDT is connected through capacitor to GND.
2. IREF is connected through resistor to GND.
3. IMON is connected through resistor to GND.
4. ILIM is connected through resistor to GND.

The following pins of all devices must be connected together:

1. IN
2. OUT
3. EN/UVLO
4. DVDT
5. D_OC
6. IMON
7. IREF
8. GOK/$\overline{\text{FLT}}$

In this configuration, all the devices are powered up and enabled simultaneously.

Inrush: During inrush, because the DVDT pins are tied together to a single DVDT capacitor all the devices turn on the output with the same slew rate (SR). Choose the common DVDT capacitor (C_{DVDT}) as per the following 式 14 and 式 15.

$$SR(V/ms) = \frac{I_{INRUSH}(A)}{C_{LOAD}(mF)} \quad (14)$$

$$C_{DVDT}(pF) = \frac{N \times k}{SR(V/ms)} \quad (15)$$

Where N = number of parallel devices and k = 51300 for B0/1/3 variants, and k = 135000 for B2 variant.

In this condition, the internal balancing circuit ensures that the load current is shared among all devices during start-up. This action prevents a situation where some devices turn on faster than others and experience more thermal stress as compared to other devices. This can potentially result in premature or partial shutdown of the parallel chain, or even SOA damage to the devices. The current balancing scheme ensures the inrush capability of the chain scales according to the number of devices connected in parallel, thereby ensuring successful start-up with larger output capacitances or higher loading during start-up.

Steady-state: During steady-state, all devices share current based on the respective device R_{DSON} and path resistance to distribute current across all the devices in the parallel chain.

Overcurrent during steady-state: The R_{ILIM} value for each individual eFuse must be selected based on the following 式 16.

$$R_{ILIM} = \frac{N \times 0.75 \times V_{IREF}}{G_{ILIM} \times I_{OCP(TOT)}} \quad (16)$$

Where N = number of devices in parallel, and $I_{OCP(TOT)}$ = Total system circuit-breaker threshold

The reference voltage can be generated by connecting appropriate resistor R_{IREF} on the IREF pin.

$$V_{IREF} = N \times I_{IREF} \times R_{IREF} \quad (17)$$

Other variations:

The IREF pin can be driven from an external voltage reference (V_{IREF}).

Severe overcurrent (short-circuit): If there is a severe fault at the output (for example, output shorted to ground with a low impedance path) during steady-state operation, the current builds up rapidly to a high value and triggers the fast-trip response in each device. The devices use two thresholds for fast-trip protection – a user-adjustable threshold (I_{SFT} = 2 × I_{OCP} in steady-state or I_{SFT} = 1.5 × I_{LIM} during inrush) as well as a fixed threshold (I_{FFT} only during steady-state). After the fast-trip, the devices enter into a latch-off fault condition till the device is power cycled or re-enabled (for TPS25984B0/3 variants) or the auto-retry timer expires (only for TPS25984B1 variant or for TPS25984B2 variant with MODE pin connected to GND).

8.1.3 Digital Telemetry Using External Microcontroller

Systems which need digital telemetry, control, and configurability along with high current eFuse functionality can use TPS25984Bx devices in conjunction with a microcontroller as shown in 図 8-3.

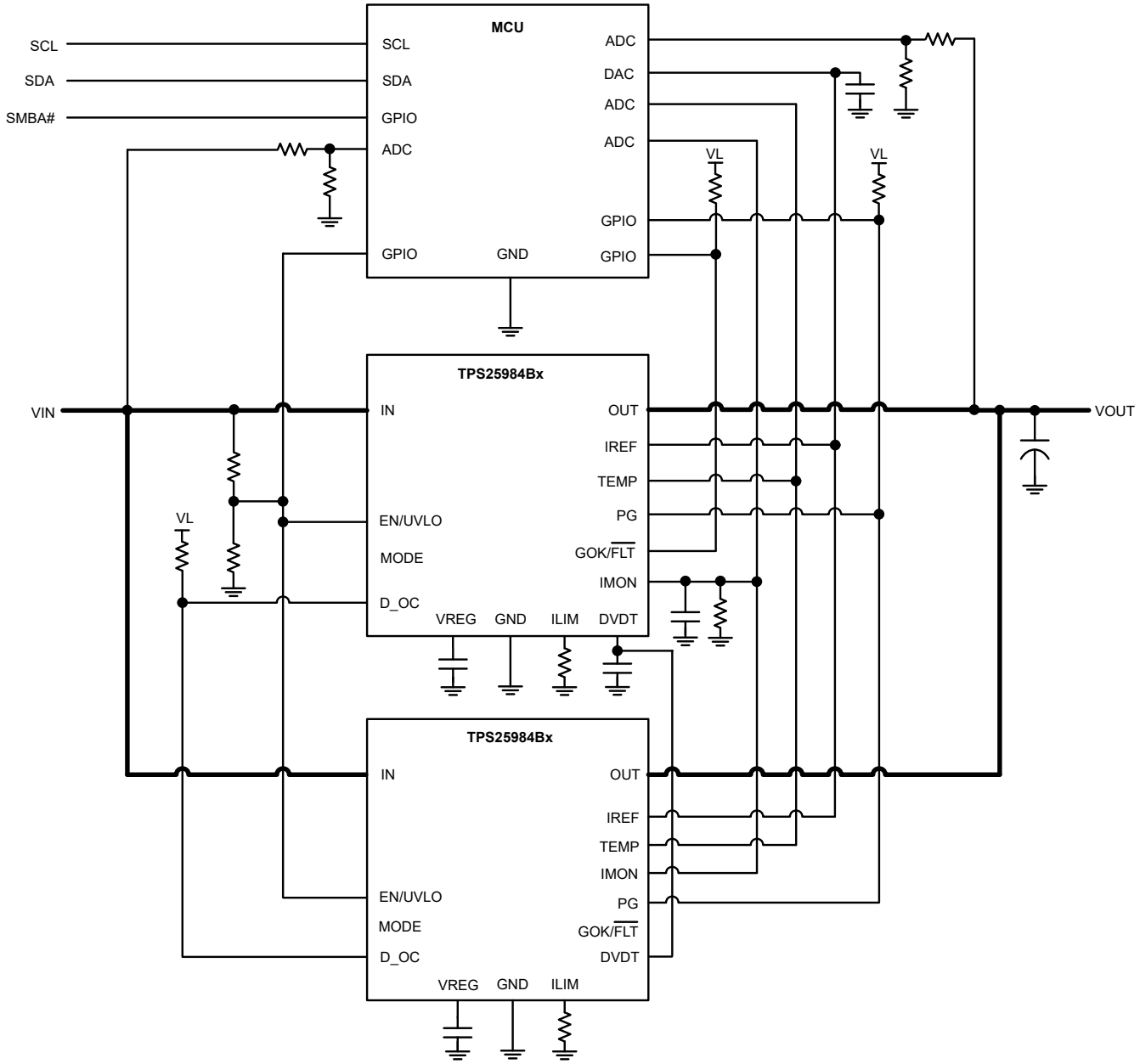


図 8-3. Digital Telemetry Using External Microcontroller

The basic circuit connections for the eFuses are the same for the single or multiple parallel device configuration. In addition, the following connections can be made to the microcontroller:

- EN/UVLO is connected to GPIO of microcontroller to allow digital ON and OFF control of the eFuse.
- PG and GOK/$\overline{\text{FLT}}$ pins are connected to GPIO of microcontroller to allow digital monitoring of the eFuse status.
- VIN and VOUT rails are connected to the ADC inputs of microcontroller (through resistor ladder to appropriately step down the voltage) for monitoring the bus voltages.

- IMON is connected to an ADC input of microcontroller for monitoring the load current.
- TEMP is connected to an ADC input of microcontroller for monitoring the eFuse die temperature.
- IREF can be optionally connected to a DAC output of the microcontroller to dynamically change the reference voltage for overcurrent and short-circuit current thresholds.

注

1. The GOK/$\overline{\text{FLT}}$ pin must be pulled up to an appropriate supply voltage as per the *Recommended Operating Conditions* table.

8.2 Typical Application: 12V, 3.3kW Power Path Protection in Data Center Servers

8.2.1 Application

This design example considers a 12V system operating voltage with a tolerance of ±10%. The maximum steady-state load current is 275A. If the load current exceeds 480A for persistent overloads lasting longer than the fixed blanking timer of 0.4ms, the eFuse circuit must break the circuit and then latch-off. The eFuse circuit must charge a bulk capacitance of 40mF and support approximately 10% of the steady-state load during start-up. 図 8-4 shows the application schematic for this design example.

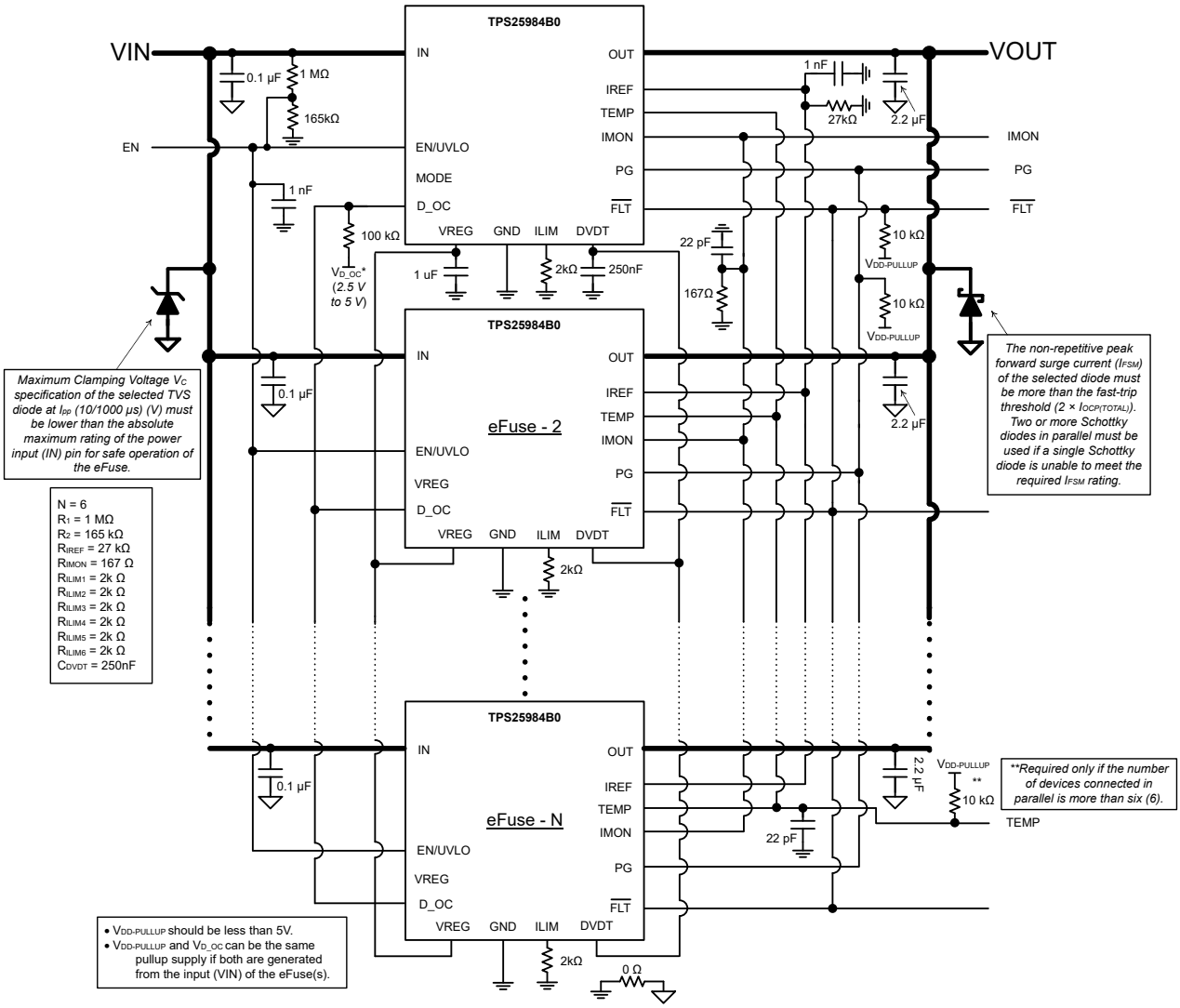


図 8-4. Application Schematic for a 12V, 3.3kW Power Path Protection Circuit

8.2.2 Design Requirements

表 8-1 shows the design parameters for this application example.

表 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range (V_{IN})	10.8V – 13.2V
Maximum DC load current ($I_{OUT(max)}$)	275A
Maximum output capacitance (C_{LOAD})	40mF
Are all the loads off until the PG is asserted?	No
Load at start-up ($R_{LOAD(Startup)}$)	0.48 Ω (equivalent to approximately 10% of the maximum steady-state load)
Maximum ambient temperature	55°C
Transient overload blanking timer	0.25ms (min)
Output turn on (soft-start) time	10ms
Output voltage slew rate	1.2V/ms
Need to survive a “Hot-Short” on output condition ?	Yes
Need to survive a “power up into short” condition?	Yes
Can a board be hotplugged in or power cycled?	Yes
Load current monitoring needed?	Yes
Fault response	Latch-off

8.2.3 Detailed Design Procedure

- **Determining the number of eFuse devices to be used in parallel**

  By factoring in a small variation in the junction to ambient thermal resistance ($R_{\theta JA}$), a single TPS25984Bx eFuse is rated at a maximum steady state DC current of 55A at an ambient temperature of 70°C. Therefore, 式 18 can be used to calculate the number of devices (N) to be in parallel to support the maximum steady state DC load current ($I_{LOAD(max)}$), for which the solution must be designed.

$$N \geq \frac{I_{OUT(max)}\,(A)}{55A} \tag{18}$$

  According to 表 8-1, $I_{OUT(max)}$ is 275A. Therefore, six (6) TPS25984Bx eFuses are connected in parallel.

- **Selecting the C_{DVDT} capacitor to control the output slew rate and start-up time**

  For a robust design, the junction temperature of the device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Typically, dynamic power stresses are orders of magnitude greater than static stresses, so it is crucial to establish the right start-up time and inrush current limit for the capacitance in the system and the associated loads to avoid thermal shutdown during start-up.

  表 8-2 summarizes the formulas for calculating the average inrush power loss on the eFuses in the presence of different loads during start-up if the power good (PG) signal is not used to turn on all the downstream loads.

表 8-2. Calculation of Average Power Loss During Inrush

Type of Loads During Start-Up	Expressions to Calculate the Average Inrush Power Loss
Only output capacitor of C_{LOAD} (µF)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}}$ (19)
Output capacitor of C_{LOAD} (µF) and constant resistance of $R_{LOAD(Startup)}$ (Ω) with turn-ON threshold of V_{RTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}} + \frac{V_{IN}^2}{R_{LOAD(Startup)}}\left[\frac{1}{6} - \left\{\frac{1}{2}\left(\frac{V_{RTH}}{V_{IN}}\right)^2\right\} + \left\{\frac{1}{3}\left(\frac{V_{RTH}}{V_{IN}}\right)^3\right\}\right]$ (20)
Output capacitor of C_{LOAD} (µF) and constant current of $I_{LOAD(Startup)}$ (A) with turn-ON threshold of V_{CTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}} + V_{IN} I_{LOAD(Startup)}\left[\frac{1}{2} - \left(\frac{V_{CTH}}{V_{IN}}\right) + \left\{\frac{1}{2}\left(\frac{V_{CTH}}{V_{IN}}\right)^2\right\}\right]$ (21)
Output capacitor of C_{LOAD} (µF) and constant power of $P_{LOAD(Startup)}$ (W) with turn-ON threshold of V_{PTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}} + P_{LOAD(Startup)}\left[\ln\left(\frac{V_{PTH}}{V_{IN}}\right) + \left(\frac{V_{PTH}}{V_{IN}}\right) - 1\right]$ (22)

Where V_{IN} is the input voltage and T_{ss} is the start-up time.

With the different combinations of loads during start-up, the total average inrush power loss (P_{INRUSH}) can be calculated using the formulas described in 表 8-2. For a successful start-up, the system must satisfy the condition stated in 式 23.

$$P_{INRUSH}(W)\sqrt{T_{ss}(s)} < 10 \times N \quad (23)$$

Where N denotes the number of eFuses in parallel and 10W√s is the SOA limit of a single TPS25984Bx eFuse. This equation can be used to obtain the maximum allowed T_{ss}.

注

TI recommends to use a T_{ss} in the range of 5ms to 120ms to prevent start-up issues.

A capacitor (C_{DVDT}) must be added at the DVDT pin to GND to set the required value of T_{ss} as calculated above. The following equations are used to compute the value of C_{DVDT}. The DVDT pins of all the eFuses in a parallel chain must be connected together.

For B0/1/3 variants:

$$C_{DVDT}(pF) = \frac{51300 \times N}{SR(V/ms)} \quad (24)$$

For B2 variant:

$$C_{DVDT}(pF) = \frac{135000 \times N}{SR(V/ms)} \quad (25)$$

In this design example, C_{LOAD} = 40mF, $R_{LOAD(Startup)}$ = 0.48Ω, V_{RTH} = 0V, V_{IN} = 12V, and T_{ss} = 10ms. P_{INRUSH} is calculated to be 340W using the equations provided in the 表 8-2. It can be verified that the system satisfies condition stated in 式 23 and therefore capable of a successful start-up. If 式 23 does not hold true, start-up loads or T_{ss} must be tuned to prevent chances of thermal shutdown during start-up. Using V_{IN} = 12V, T_{ss} = 10ms, the required C_{DVDT} value can be calculated to be 258nF. The closest standard value of C_{DVDT} is 250nF with 10% tolerance and DC voltage rating of 25V.

注

In some systems, there can be active load circuits (for example, DC-DC converters) with low turn-on threshold voltages which can start drawing power before the eFuse has completed the inrush sequence. This action can cause additional power dissipation inside the eFuse during start-up and can lead to thermal shutdown. TI recommends using the Power Good (PG) pin of the eFuse to enable and disable the load circuit. This action ensures that the load is turned on only when the eFuse has completed its start-up and is ready to deliver full power without the risk of hitting thermal shutdown.

- **Selecting the R_{IREF} resistor to set the reference voltage for overcurrent protection**

  In this parallel configuration, the IREF internal current source (I_{IREF}) of all the eFuse interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage (V_{IREF}) for the overcurrent protection blocks. When the voltage at the IMON pin (V_{IMON}) is used as an input to an ADC to monitor the system current or to implement the Platform Power Control (Intel® PSYS) functionality inside the VR controller, V_{IREF} must be set to half of the maximum voltage range of the ISYS_IN input of the controller. This action provides the necessary headroom and dynamic range for the system to accurately monitor the load current up to the fast-trip threshold (2 × I_{OCP}). 式 26 is used to calculate the value of R_{IREF}.

$$V_{IREF} = I_{IREF} \times R_{IREF} \times N \quad (26)$$

  In this design example, V_{IREF} is set at 1.62V. With I_{IREF} = 10µA (typical), we can calculate the target R_{IREF} to be 27kΩ. The closest standard value of R_{IREF} is 27kΩ with 0.1% tolerance and power rating of 100mW. For improved noise immunity, place a 1000pF ceramic capacitor from the IREF pin to GND. The IREF pins of all the eFuses in a parallel chain must be connected together.

注

Maintain V_{IREF} within the recommended voltage to ensure proper operation of overcurrent detection circuit.

- **Selecting the R_{IMON} resistor to monitor current through each eFuse**

  TPS25984Bx eFuse continuously monitors the current flowing through it (I_{DEVICE}) and outputs a proportional analog output current on its own ILIM pin. This in turn produces a proportional voltage (VILIM) across the respective ILIM pin resistor (R_{IMON}), which is expressed as:

$$V_{IMON} = I_{OUT} \times G_{IMON} \times N \times R_{IMON} \quad (27)$$

  G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT}), whose typical value is 10µA/A

- **Selecting the R_{ILIM} resistor to set the overcurrent (circuit-breaker) and fast-trip thresholds during steady state and inrush current during startup**

  TPS25984Bx eFuse responds to the output overcurrent conditions during steady-state by turning off the output after a fixed transient fault blanking interval. This eFuse continuously senses the total system current (I_{OUT}) and produces a proportional analog current output (I_{ILIM}) on the ILIM pin. This generates a voltage (V_{ILIM}) across the ILIM pin resistor (R_{ILIM}) in response to the load current, which is defined as 式 27.

$$V_{ILIM} = I_{OUT} \times G_{ILIM} \times R_{ILIM} \quad (28)$$

  G_{ILIM} is the current monitor gain (I_{ILIM} : I_{OUT}), whose typical value is 7.5µA/A. The overcurrent condition is detected by comparing the V_{ILIM} against the V_{IREF} as a threshold. The circuit-breaker threshold during steady-state (I_{OCP}) can be calculated using 式 29.

$$I_{OCP} = \frac{0.75 \times V_{IREF}}{G_{ILIM} \times R_{ILIM}} \quad (29)$$

In this design example, I_{OCP} is set at 480A, and R_{ILIM} can be calculated to be 2kΩ with G_{ILIM} as 7.5 µA/A and V_{IREF} as 1.62V. The nearest value of R_{ILIM} is 2kΩ with 0.1% tolerance and power rating of 100 mW.

- ***Overcurrent limit during start-up***: During inrush, the overcurrent condition for each device is detected by comparing its own load current information (V_{ILIM}) with a scaled reference voltage as depicted in 式 30.

$$CLREF_{SAT} = 0.4 \times V_{IREF} \tag{30}$$

The current limit threshold during start-up can be calculated using 式 31.

$$I_{ILIM(Startup)} = \frac{CLREF_{SAT}}{G_{ILIM} \times R_{ILIM}} \tag{31}$$

By using a R_{ILIM} value of 2kΩ for each device, the start-up current is limited to around 43A for each device.

- **Selecting the resistors to set the undervoltage lockout threshold**

The undervoltage lockout (UVLO) threshold is adjusted by employing the external voltage divider network of R_1 and R_2 connected between IN, EN/UVLO, and GND pins of the device as described in セクション 7.3.1. The resistor values required for setting up the UVLO threshold are calculated using 式 32.

$$V_{IN(UV)} = V_{UVLO(R)} \frac{R_1 + R_2}{R_2} \tag{32}$$

To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R_1 and R_2. The current drawn by R_1 and R_2 from the power supply is $I_{R12} = V_{IN} / (R_1 + R_2)$. However, the leakage currents due to external active components connected to the resistor string can add errors to these calculations. So, the resistor string current, I_{R12} must be 20 times greater than the leakage current at the EN/UVLO pin (I_{ENLKG}). From the device electrical specifications, I_{ENLKG} is 0.1µA (maximum) and UVLO rising threshold $V_{UVLO(R)}$ = 1.52V (max). From the design requirements, V_{INUVLO} = 10.8 V. First choose the value of R_1 = 1MΩ and use Equation 13 to calculate R_2 >163.79 kΩ. Use the closest standard 1 % resistor values: R_1 = 1MΩ and R_2 = 165kΩ. For noise reduction, place a 1000pF ceramic capacitor across the EN/UVLO pin and GND.

- **Selecting the pullup resistors and power supplies for PG and GOK/$\overline{\text{FLT}}$ pins**

GOK/$\overline{\text{FLT}}$ and PG are open-drain outputs. If these logic signals are used, the corresponding pins must be pulled up to the appropriate voltages (< 5V) through 10kΩ pullup resistances.

注

GOK/$\overline{\text{FLT}}$ pin must be pulled up to a voltage in the range of 2.5V to 5V through a 100kΩ resistance.

- **Selection of TVS diode at input and Schottky diode at output**

In the case of a short circuit and overload current limit when the device interrupts a large amount of current instantaneously, the input inductance generates a positive voltage spike on the input, whereas the output inductance creates a negative voltage spike on the output. The peak amplitudes of these voltage spikes (transients) are dependent on the value of inductance in series with the input or output of the device. Such transients can exceed the absolute maximum ratings of the device and eventually lead to failures due to electrical overstress (EOS) if appropriate steps are not taken to address this issue. Typical methods for addressing this issue include:

1. Minimize lead length and inductance into and out of the device.
2. Use a large PCB GND plane.
3. Addition of the transient voltage suppressor (TVS) diodes to clamp the positive transient spike at the input.
4. Using Schottky diodes across the output to absorb negative spikes.

Refer to *TVS Clamping in Hot-Swap Circuits* and *Selecting TVS Diodes in Hot-Swap and ORing Applications* for details on selecting an appropriate TVS diode and the number of TVS diodes to be in parallel to effectively clamp the positive transients at the input below the absolute maximum ratings of the IN pin (20V). These TVS diodes also help to limit the transient voltage at the IN pin during the hot-plug event. Four (4) SMDJ12A are used in parallel in this design example.

注

Maximum clamping voltage V_C specification of the selected TVS diode at I_{pp} (10/1000 µs) (V) must be lower than the absolute maximum rating of the power input (IN) pin for safe operation of the eFuse.

Selection of the Schottky diodes must be based on the following criteria:

– The non-repetitive peak forward surge current (I_{FSM}) of the selected diode must be more than the fast-trip threshold ($2 \times I_{OCP(TOTAL)}$). Two or more Schottky diodes in parallel must be used if a single Schottky diode is unable to meet the required I_{FSM} rating. 式 33 calculates the number of Schottky diodes ($N_{Schottky}$) that must be in parallel.

$$N_{Schottky} > \frac{2 \times I_{OCP(TOTAL)}}{I_{FSM}} \quad (33)$$

– Forward Voltage Drop (V_F) at near to I_{FSM} must be as small as possible. Ideally, the negative transient voltage at the OUT pin must be clamped within the absolute maximum rating of the OUT pin (–1V).
– DC Blocking Voltage (V_{RM}) must be more than the maximum input operating voltage.
– Leakage current (I_R) must be as small as possible.

Three (3) SBR10U45SP5 are used in parallel in this design example.

- **Selecting C_{IN} and C_{OUT}**

TI recommends to add ceramic bypass capacitors to help stabilize the voltages on the input and output. The value of C_{IN} must be kept small to minimize the current spike during hot-plug events. For each device, 0.1µF of C_{IN} is a reasonable target. Because C_{OUT} does not get charged during hot-plug, a larger value such as 2.2µF can be used at the OUT pin of each device.

8.2.4 Application Curves

All the waveforms below are captured on an evaluation setup with six (6) TPS25984Bx eFuses in parallel. All the pullup supplies are derived from a separate standby rail.

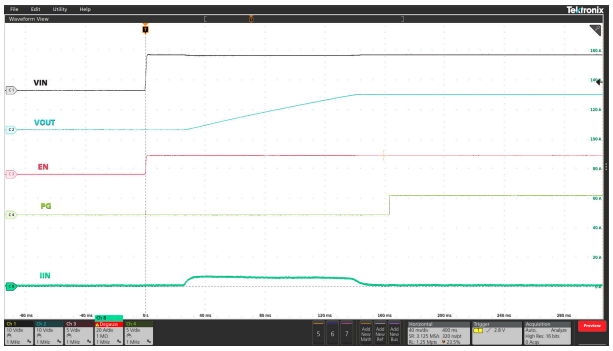


図 8-5. Input Hot Plug: V_{IN} Stepped Up from 0V to 12V, C_{LOAD} = 40mF, C_{DVDT} = 43nF, and R_{ILIM} on Each Device = 2kΩ

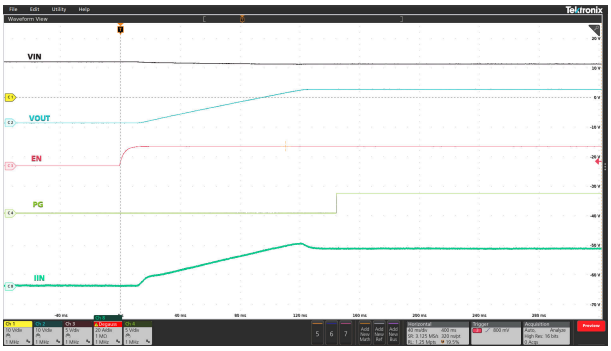


図 8-6. Start-up with EN/UVLO: V_{IN} = 12V, EN/UVLO Stepped Up From 0V to 3V, C_{LOAD} = 40mF, $R_{LOAD(Start-up)}$ = 0.48Ω, C_{DVDT} = 43nF, and R_{ILIM} on Each Device = 2kΩ

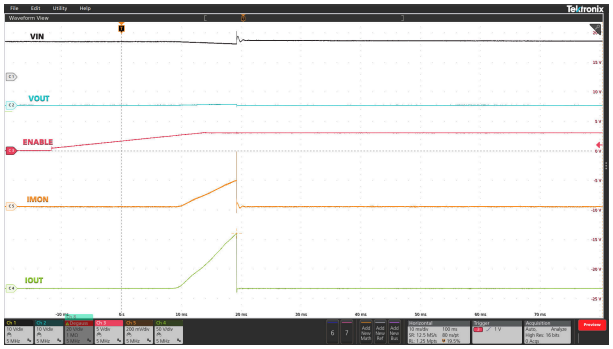


図 8-7. Power Up into Short: V_{IN} = 12V, EN/UVLO Stepped Up From 0V to 3V, R_{IREF} = 27kΩ, R_{ILIM} on Each Device = 2kΩ, and OUT Shorted to GND

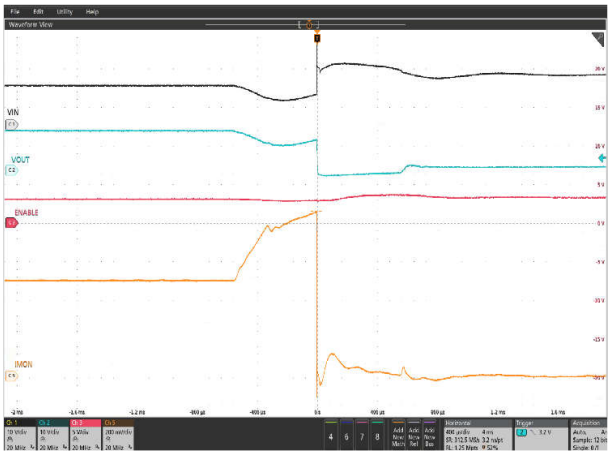


図 8-8. Circuit-Breaker Response: V_{IN} = 12V, C_{LOAD} = 40mF, R_{IMON} = 167Ω, R_{IREF} = 27kΩ, and Load Current Stepped up From 250A to 510A

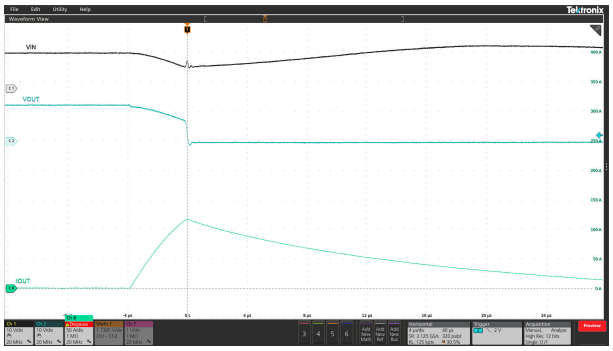


図 8-9. Output Hot-Short Response: V_{IN} = 12V, R_{IMON} = 167Ω, R_{IREF} = 27kΩ, and OUT Shorted to GND

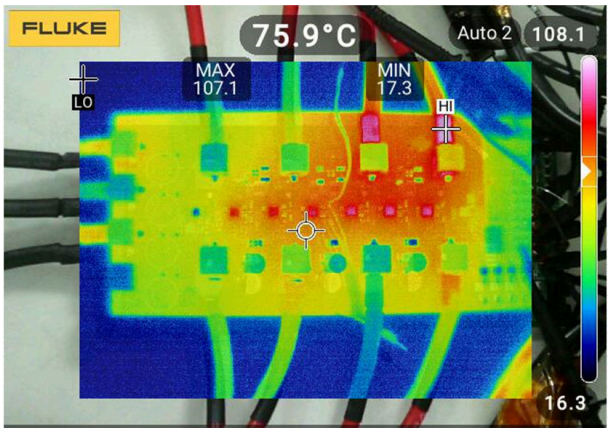


図 8-10. Six Devices in Parallel Temperature Rise with 300A total DC Current at Room Temperature (No Air-Flow)

8.3 Power Supply Recommendations

The TPS25984Bx devices are designed for a supply voltage in the range of 4.5V to 16V on the IN pin. TI recommends using a minimum capacitance of 0.1µF on the IN pin of each device in parallel chain to avoid coupling of high slew rates during hot plug events.

8.3.1 Transient Protection

In the case of a short-circuit or circuit-breaker event when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor of 2.2µF or higher at the OUT pin very close to the device.
- Connect a ceramic capacitor C_{IN} = 0.1µF or higher at the IN pin very close to the device to dampen the rise time of input transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

The approximate value of input capacitance can be estimated with 式 34.

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (34)$$

where

V_{IN} is the nominal supply voltage.

I_{LOAD} is the load current.

L_{IN} equals the effective inductance seen looking into the source.

C_{IN} is the capacitance present at the input.

- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive

energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

The circuit implementation with optional protection components is shown in 図 8-11.

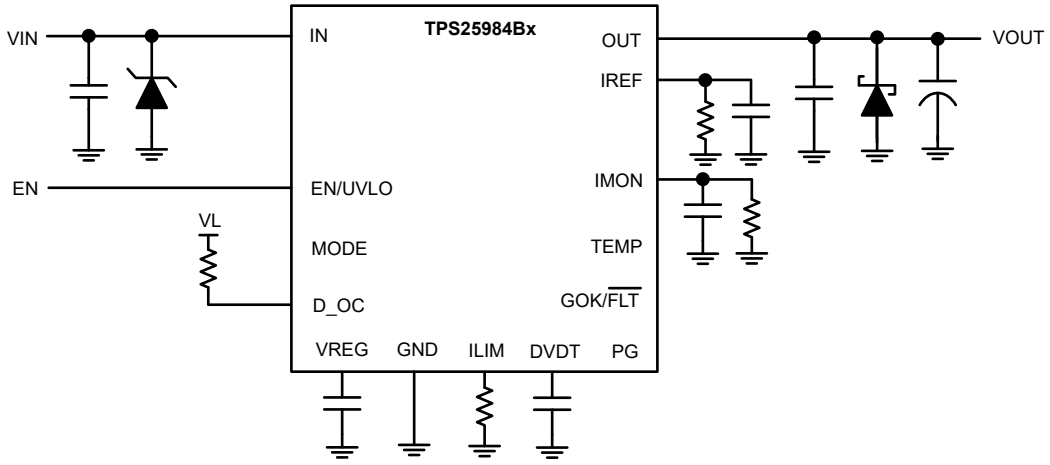


図 8-11. Circuit Implementation with Optional Protection Components

8.3.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.4 Layout

8.4.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- For all applications, TI recommends a ceramic decoupling capacitor of 2.2 µF or greater between the OUT terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure below for a PCB layout example.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- The IN and OUT pins are used for Heat Dissipation. Connect to as much copper area as possible with thermal vias.
- Locate the following support components close to their connection pins:
  - R_{ILIM}

  - R_{IMON}
  - R_{IREF}
  - C_{dVdT}
  - C_{VREG}
  - C_{IN}
  - C_{OUT}
  - Resistors for the EN/UVLO pin
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the C_{IN}, C_{OUT}, R_{IREF}, R_{ILIM}, R_{IMON}, C_{VREG} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit and soft-start timing. These traces must not have any coupling to switching signals on the board.
- Because the ILIM and IREF pins directly control the overcurrent protection behavior of the device, the PCB routing of these nodes must be kept away from any noisy (switching) signals.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.

8.4.2 Layout Example

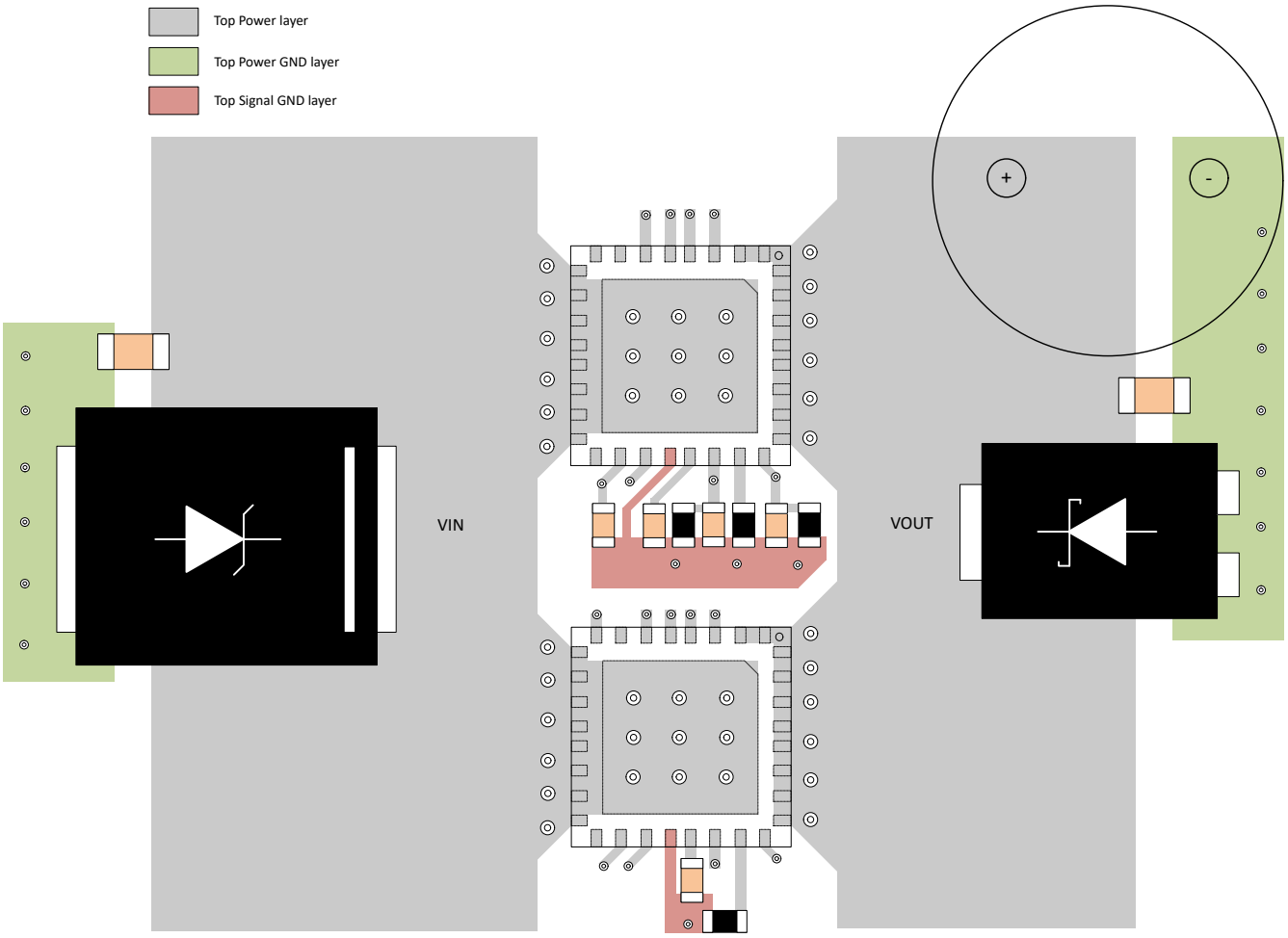


図 8-12. TPS25984Bx Two Parallel Devices Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- *TPS25984BEVM eFuse Evaluation Board User Guide*
- *TPS25984Bx Design Calculator*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.4 Trademarks

PROCHOT™ and Intel PSYS™ are trademarks of Intel.
テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
Intel® is a registered trademark of Intel.
is a registered trademark of intel.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25984B0RZJR	Active	Production	WQFN-FCRLF (RZJ) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25984B0
TPS25984B1RZJR	Active	Production	WQFN-FCRLF (RZJ) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25984B1
TPS25984B2RZJR	Active	Production	WQFN-FCRLF (RZJ) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25984B2
TPS25984B3RZJR	Active	Production	WQFN-FCRLF (RZJ) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25984B3

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

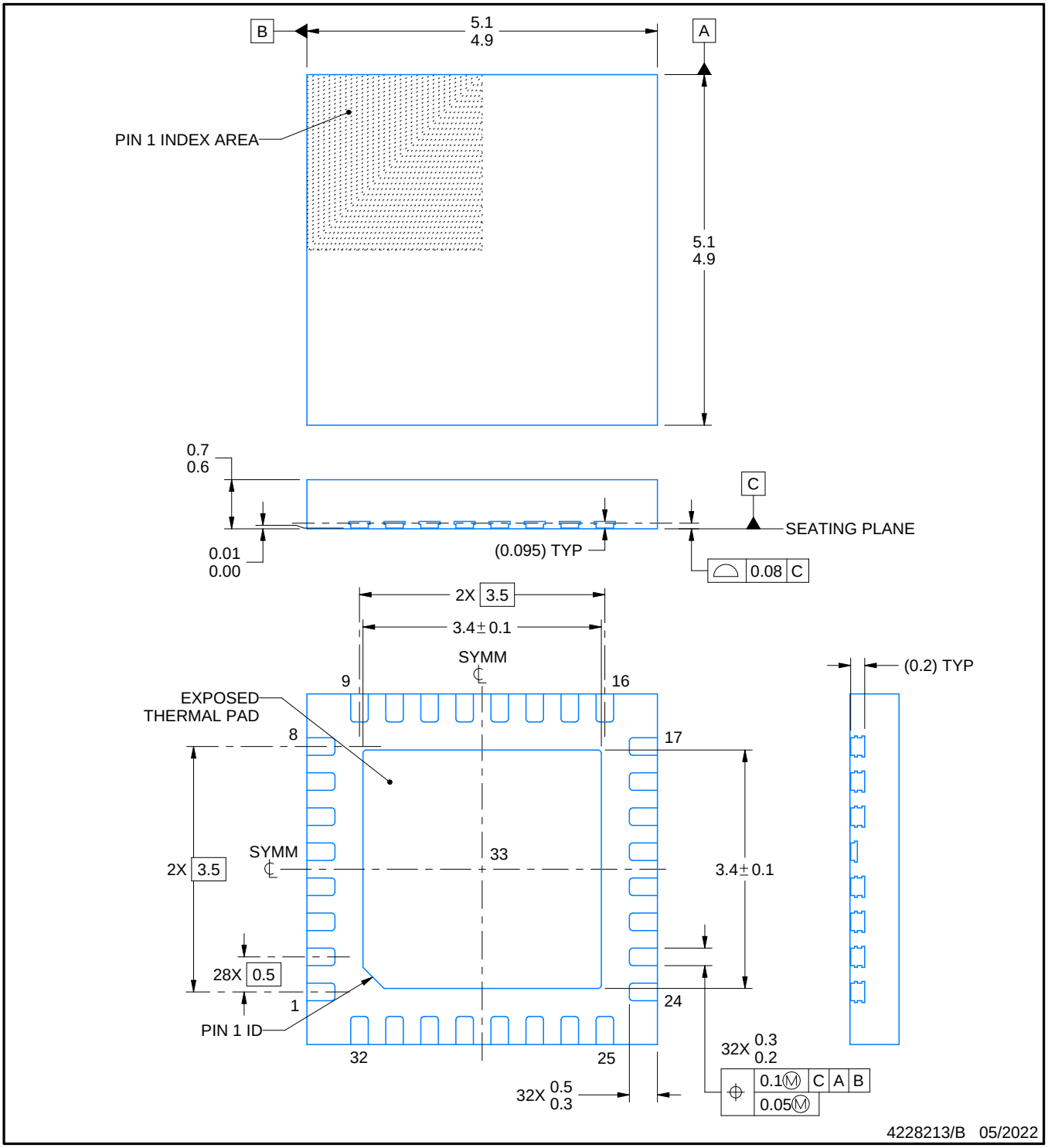
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

RZJ0032A

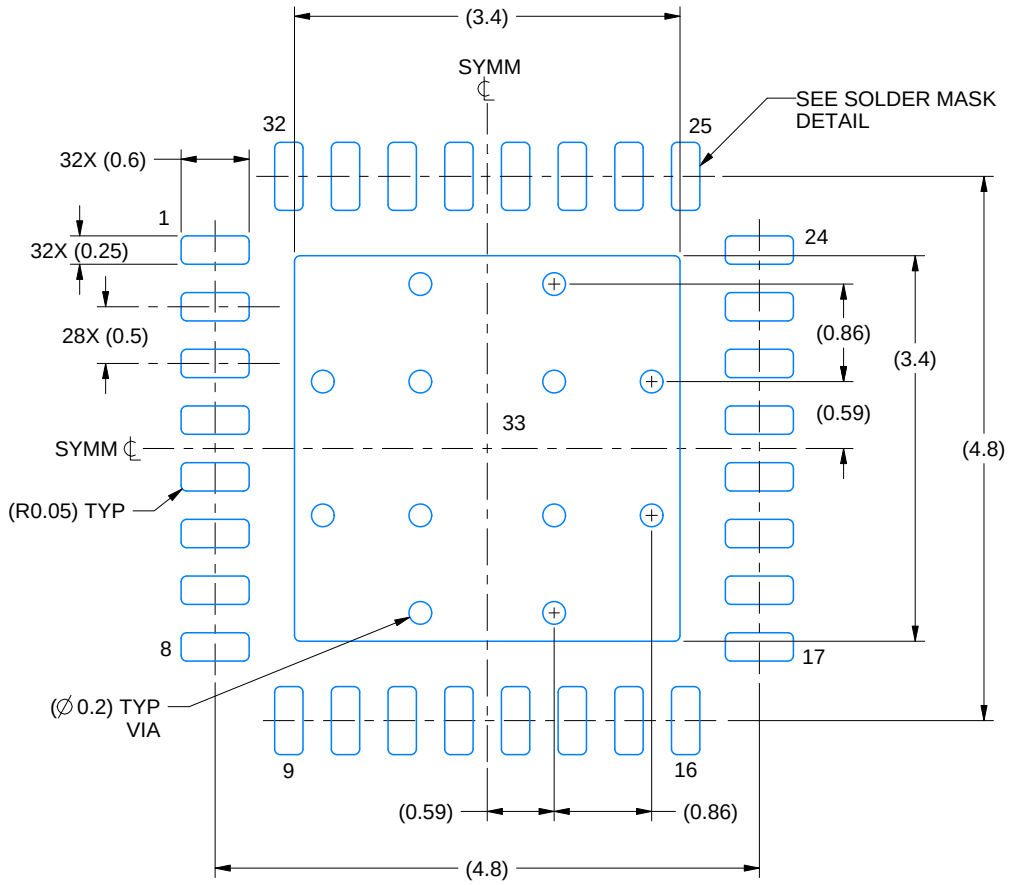
WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

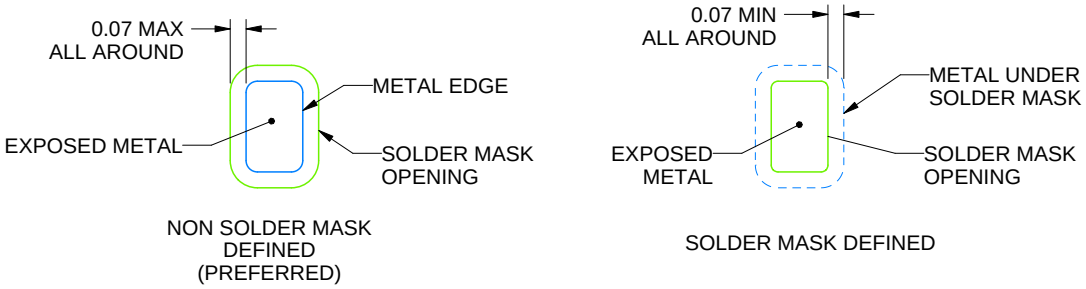


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

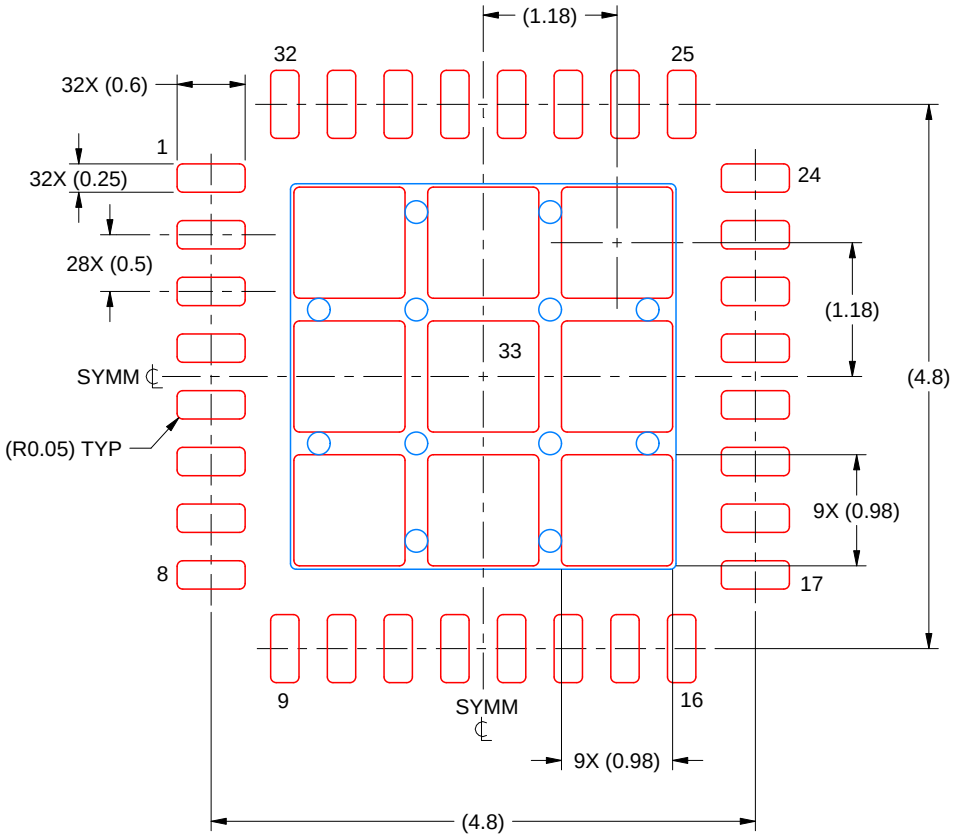


SOLDER MASK DETAILS

4228213/B 05/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 33
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4228213/B 05/2022

NOTES: (continued)

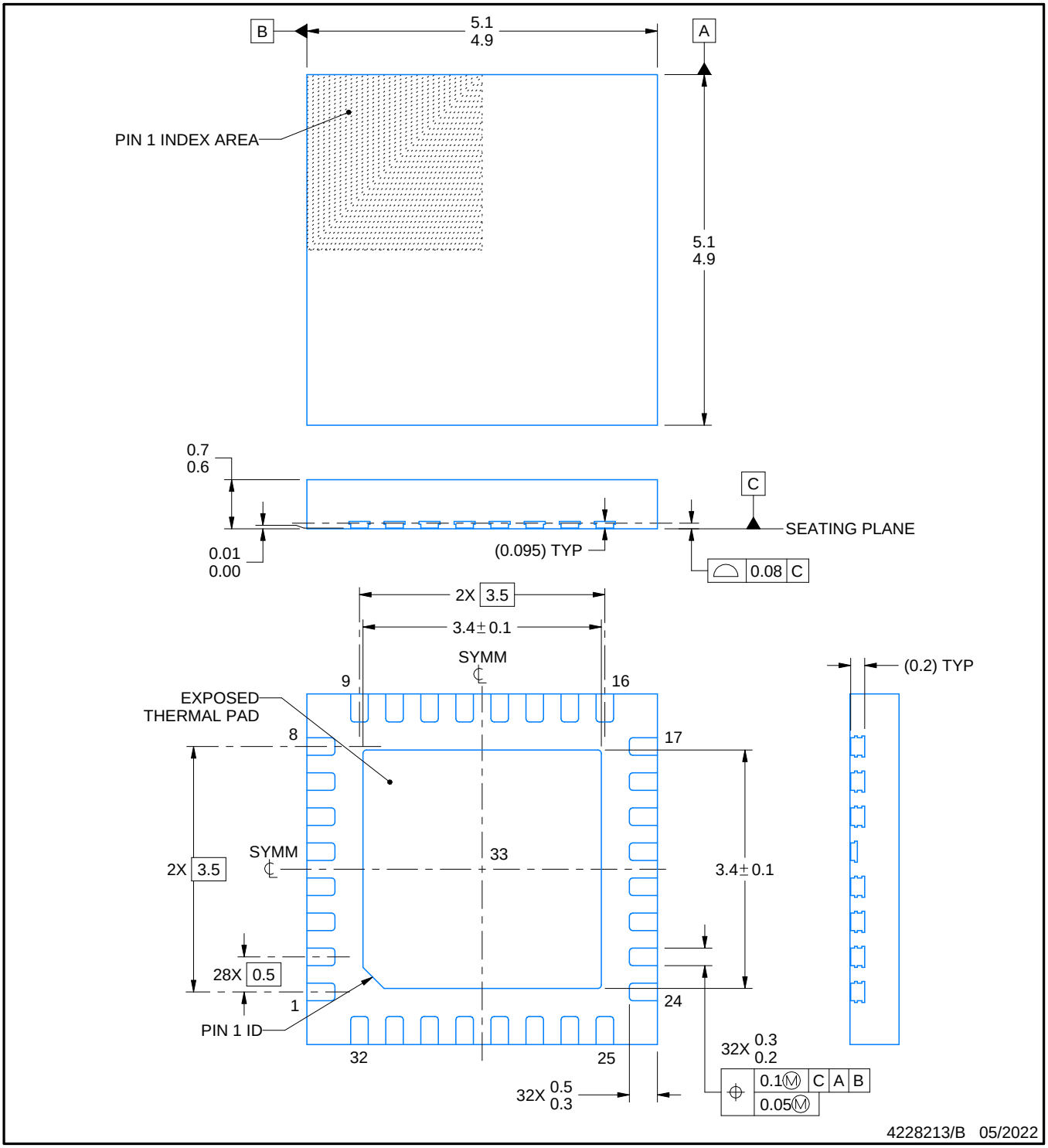
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RZJ0032A

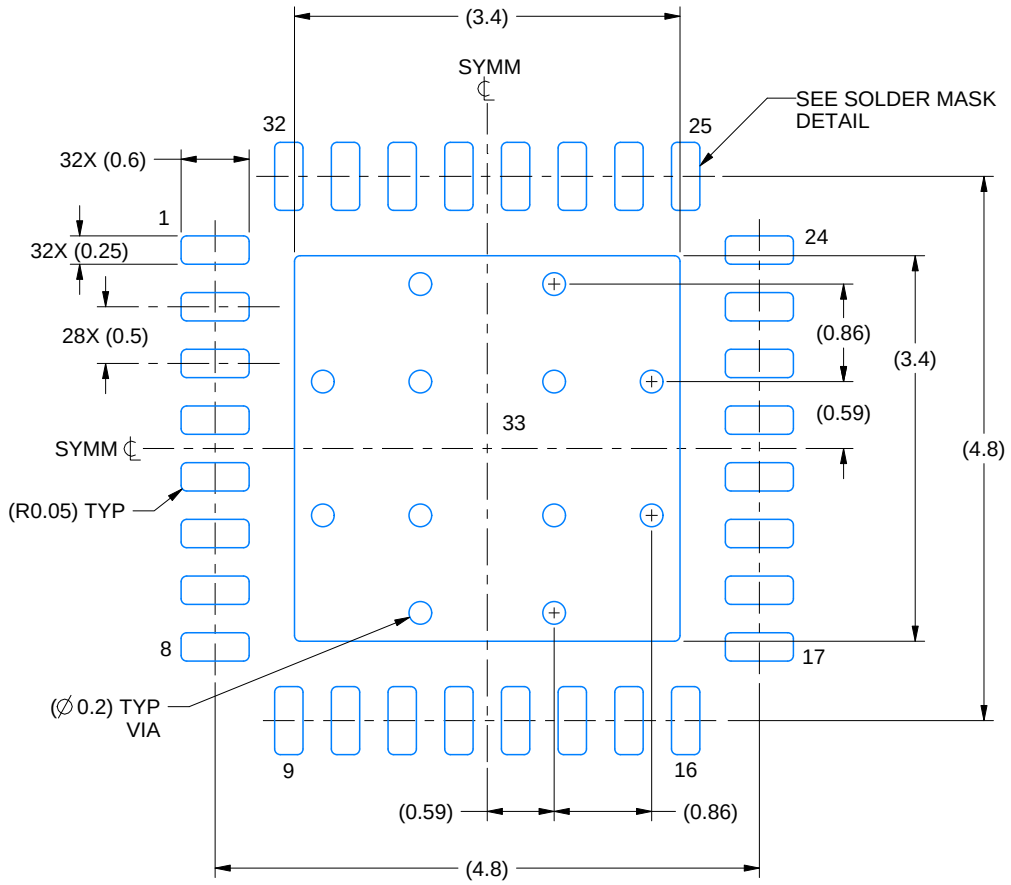
WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

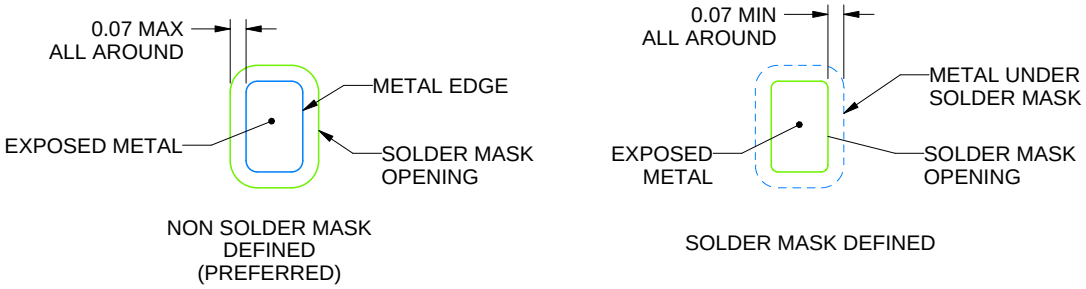


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

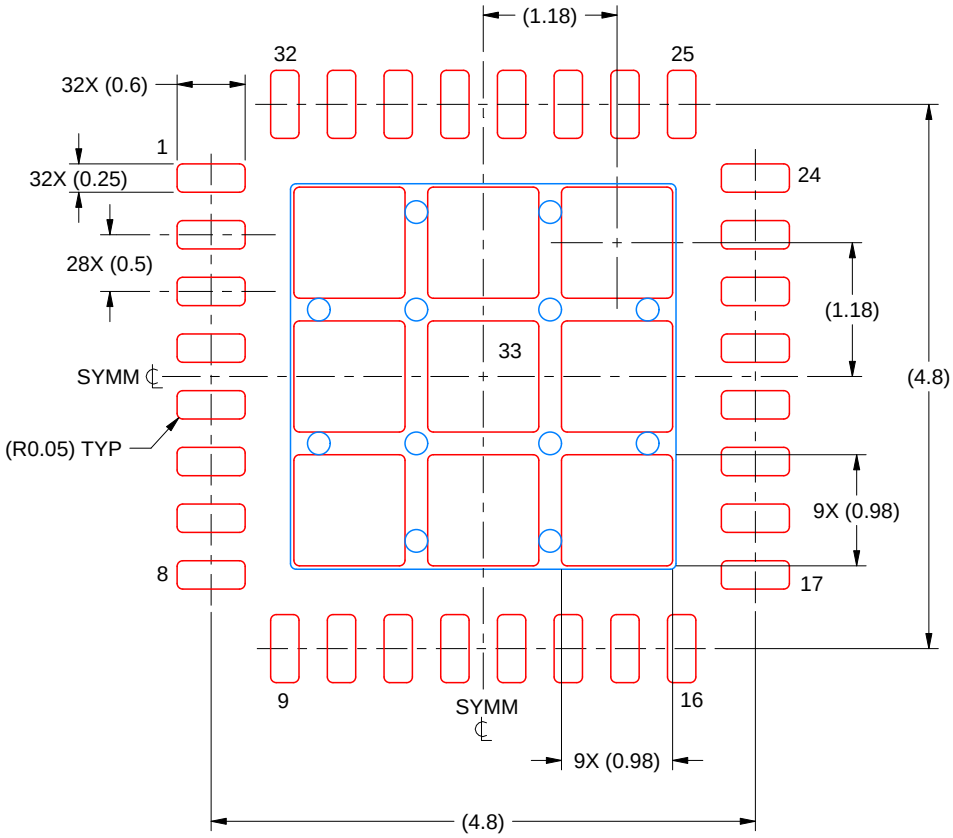


SOLDER MASK DETAILS

4228213/B 05/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 33
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4228213/B 05/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月