TPS2596 高精度の電流モニタと高速な過電圧保護を搭載した 2.7～19V、0.13～2A、85mΩ の eFuse

1 特長

- 広い入力電圧範囲：2.7V～19V
  - 絶対最大定格:21V
- 低いオン抵抗：Ron = 85mΩ (標準値)
- アクティブ HIGH のイネーブル入力、低電圧誤動作防止 (UVLO) を設定可能
- 高速な過電圧保護クランプ (3.8V、5.7V、13.7V をピンで選択可能)、応答時間 5µs (標準値)
- OR 調整可能な過電圧誤動作防止 (OVLO)
- 可変の電流制限と負荷電流監視出力 (ILM)
  - 電流範囲:0.13A～2A
  - 電流制限の精度:±8% (最大値)
    - 25˚Cで±5%
- 電気的高速過渡 (IEC 61000-4-4) 耐性
- 可変の出力スルー・レート (dVdt) 制御
- 過熱保護 (OTP)
- フォルト表示ピン ($\overline{FLT}$)
- UL 2367 認定 (申請中)
- 単一点障害時の安全性テスト (IEC62368-1) (申請中)
- 小さなフットプリント：4.91mm × 3.9mm の SOIC パッケージ

2 アプリケーション

- 電力量計
- 冷蔵庫
- 食器洗い機
- 洗濯機および乾燥機
- セット・トップ・ボックス
- IP ネットワーク・カメラ

3 概要

TPS2596xx ファミリの eFuse (統合 FET ホットスワップ・デバイス) は、小さなパッケージに搭載され、高度に統合された回路保護および電力管理ソリューションです。このデバイスは、非常に少ない数の外付け部品で複数の保護モードを提供し、過負荷、短絡、電圧サージ、および過剰な突入電流に対して堅牢な保護を行います。出力電流制限レベルは、単一の外付け抵抗により設定できます。また、電流制限抵抗の両端で電圧降下を測定することにより、出力負荷電流を正確に検出可能です。特定の突入電流要件を持つアプリケーションでは、単一の外付けコンデンサにより出力スルー・レートを設定できます。

TPS25962x バリアントでは、入力過電圧が発生した場合、内部のクランプ回路により出力が安全な固定最大電圧 (ピンで選択可能) に制限され、外付けの部品は必要ありません。TPS25963x バリアントには、ユーザー定義の過電圧カットオフ・スレッショルドを設定するオプションがあります。

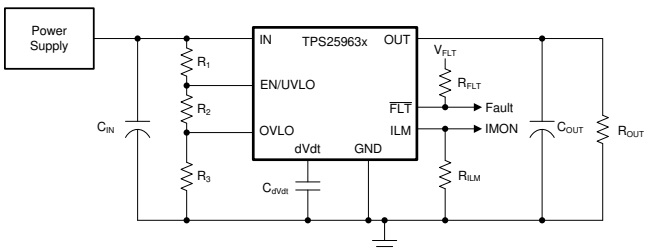
これらのデバイスは、-40℃～+125℃の接合部温度範囲で動作が規定されています。

製品情報(1)

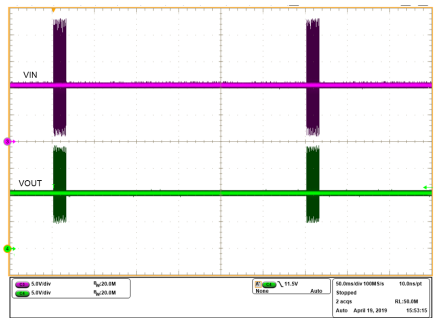
型番	パッケージ	本体サイズ(公称)
TPS259620DDA (プレビュー)	SOIC (8)	4.91mm × 3.9mm
TPS259621DDA (プレビュー)	SOIC (8)	4.91mm × 3.9mm
TPS259630DDA (プレビュー)	SOIC (8)	4.91mm × 3.9mm
TPS259631DDA (プレビュー)	SOIC (8)	4.91mm × 3.9mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



TPS25963x の 1kV EFT 応答



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4 改訂履歴

日付	リビジョン	注
2019 年 5 月	*	初版

5 デバイス比較表

型番	過電圧応答	サーマル・シャットダウン (TSD) への応答
TPS259620	OVC - 3.8V、5.7V、13.7V (ピンで選択可能)	ラッチオフ
TPS259621	OVC - 3.8V、5.7V、13.7V (ピンで選択可能)	自動再試行
TPS259630	可変 OVLO	ラッチオフ
TPS259631	可変 OVLO	自動再試行

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6 Pin Configuration and Functions

DDA Package
8-Pin SOIC
Top View

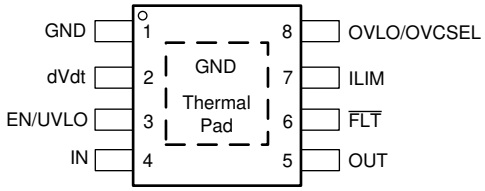

Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	Ground	Ground
dVdt	2	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate.
EN/UVLO	3	Analog Input	Active High Enable for the Device. A resistor divider can be used to adjust the Undervoltage Lockout threshold. Do not leave floating.
IN	4	Power	Power Input
OUT	5	Power	Power Output
$\overline{\text{FLT}}$	6	Digital Output	Active Low indicator which will be pulled low when a fault is detected. It is an open drain output that requires an external pull-up resistance.
ILM	7	Analog Output	This is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit. The pin voltage can also be used to monitor the output load current.
OVLO (TPS25963x)	8	Analog Input	A resistor divider can be used to adjust the Overvoltage Lockout threshold. Do not leave floating.
OVCSEL (TPS25962x)			Overvoltage Clamp voltage select pin. Refer to Overvoltage Clamp for more details.
Thermal pad		Ground	The Exposed Pad is used primarily for heat dissipation and must be connected to system ground plane.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		PIN	MIN	MAX	UNITS
V_{IN}	Maximum Input Voltage Range	IN	–0.3	21	V
	Maximum Input Voltage Range (T_A = 25 ℃)			22	V
V_{OUT}	Maximum Output Voltage Range	OUT	–0.3	min (21, V_{IN} + 0.3)	V
$V_{EN/UVLO}$	Maximum Enable Pin Voltage Range	EN/UVLO	–0.3	7	V
V_{OV}	Maximum OVCSEL/OVLO Pin Voltage Range	OVCSEL/OVLO	–0.3	7	V
V_{dVdT}	Maximum dVdT Pin Voltage Range	DVDT		2.5	V
V_{FLTB}	Maximum FLTb Pin Voltage Range	$\overline{FLT}$	–0.3	7	V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_J	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Lead Temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PIN	MIN	MAX	UNITS
V_{IN}	Input Voltage Range	IN	2.7	19(1)	V
V_{OUT}	Output Voltage Range	OUT		V_{IN} + 0.3	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		6(2)	V
V_{OV}	OVLO Pin Voltage Range (TPS25963x Only)	OVLO	0.5	2	V
V_{dVdT}	dVdT Pin Capacitor Voltage Rating	DVDT	4		V
V_{FLTB}	FLTB Pin Voltage Range	$\overline{FLT}$		6	V
R_{ILM}	ILM Pin Resistance	ILM	453	7869	Ω
I_{MAX}	Continuous Switch Current	IN to OUT		2	A
T_J	Junction temperature		–40	125	°C

(1) For TPS25962x, the input voltage should be limited to the selected Output Voltage Clamp Option as listed in the Electrical Characteristics section
(2) For supply voltages below 6V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 6V, it is recommended to use an appropriate resistor divider between IN, EN and GND to ensure the voltage at the EN pin is within the specified limits.

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7.4 Thermal Information

THERMAL METRIC(1)		TPS2596X DDA (SOIC-EP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.7(2)	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.8(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.9(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.5(3)	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	27.1(2)	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	68.1(3)	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) With exposed pad soldered to PCB
(3) Without exposed pad soldered to PCB

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V , R_{ILM} = 453 Ω , C_{dVdT} = Open, OUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
I_Q	IN quiescent current	TPS25963x		189	270	µA
		TPS25962x		196	280	µA
I_{SD}	IN Shutdown Current	$V_{EN/UVLO}$ < V_{SD}		1	2	µA
$V_{UVP(R)}$	IN Undervoltage Protection threshold	V_{IN} Rising	2.44	2.54	2.64	V
$V_{UVP(F)}$		V_{IN} Falling	2.33	2.43	2.53	V
OUTPUT VOLTAGE CLAMP (OUT) - TPS25962X						
V_{OVC}	Overvoltage Clamp Threshold	R_{OVCSEL} = Short to GND		3.8		V
		R_{OVCSEL} = 400 KΩ to GND		5.7		V
		R_{OVCSEL} = OPEN		13.7		V
V_{CLAMP}	Output Voltage During Clamping	R_{OVCSEL} = Short to GND		3.4		V
		R_{OVCSEL} = 400 KΩ to GND		5.2		V
		R_{OVCSEL} = OPEN		13		V
OUTPUT CURRENT LIMIT AND MONITOR (ILM)						
G_{IMON}	Current monitor gain as measured on ILM pin (I_{ILM} / I_{OUT})	I_{OUT} = 0.25 A		660		µA/A
		I_{OUT} = 2 A		660		µA/A
I_{LIM}	I_{OUT} Current Limit	R_{ILM} = 453 Ω		2.01		A
		R_{ILM} = 909 Ω		1.01		A
		R_{ILM} = 3.83 KΩ		0.25		A
		R_{ILM} = 7.87 KΩ		0.13		A
		R_{ILM} = OPEN		0		A
I_{CB}	I_{OUT} Circuit Breaker Threshold during R_{ILM} Short condition	R_{ILM} = Short to GND (Single Point Failure Test IEC 62368-1)		1		A

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Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V , R_{ILM} = 453 Ω , C_{dVdT} = Open, OUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ON-RESISTANCE (IN TO OUT)						
R_{ON}	ON State Resistance	V_{IN} < 4 V, I_{OUT} = 0.2 A, T_J = 25 ℃		90	100	mΩ
		V_{IN} < 4 V, I_{OUT} = 0.2 A, T_J = -40 to 85 ℃			128	mΩ
		V_{IN} < 4 V, I_{OUT} = 0.2 A, T_J = -40 to 105 ℃			137	mΩ
		V_{IN} < 4 V, I_{OUT} = 0.2 A, T_J = -40 to 125 ℃			148	mΩ
		V_{IN} > 4 V, I_{OUT} = 0.2 A, T_J = 25 ℃		85	93	mΩ
		V_{IN} > 4 V, I_{OUT} = 0.2 A, T_J = -40 to 85 ℃			118	mΩ
		V_{IN} > 4 V, I_{OUT} = 0.2 A, T_J = -40 to 105 ℃			126	mΩ
		V_{IN} > 4 V, I_{OUT} = 0.2 A, T_J = -40 to 125 ℃			134	mΩ
ENABLE/UNDERVOLTAGE LOCK OUT (EN/UVLO)						
$V_{UVLO(R)}$	UVLO Threshold	V_{EN} Rising	1.13	1.2	1.27	V
$V_{UVLO(F)}$		V_{EN} Falling	1.03	1.1	1.17	V
V_{SD}	V_{EN} threshold for lowest shutdown current	V_{EN} Falling		0.6		V
I_{ENLKG}	EN leakage current		–0.1		0.1	µA
OVERVOLTAGE LOCK OUT - TPS25963X						
$V_{OVLO(R)}$	OVLO Threshold	V_{OVLO} Rising	1.13	1.2	1.27	V
$V_{UVLO(F)}$		V_{OVLO} Falling	1.03	1.1	1.17	V
I_{OVLKG}	OVLO pin leakage current	0.5 ≤ V_{OVLO} ≤1.5V	–0.1		0.1	uA
FAULT INDICATION ($\overline{FLT}$)						
R_{FLTB}	$\overline{FLT}$ Internal Pull-down resistance	$\overline{FLT}$ asserted		12		Ω
I_{FLTLKG}	$\overline{FLT}$ pin leakage current	$\overline{FLT}$ de-asserted	–0.1		0.1	µA
OVERTEMPERATURE PROTECTION (OTP)						
TSD	Thermal Shutdown Rising Threshold	T_J Rising		156		°C
TSD_{HYS}	Thermal Shutdown Hysteresis	T_J Falling		10		°C
DVDT						
I_{DVDT}	dVdt Pin Charging Current			2		µA

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7.6 Timing Requirements

Typical Values are taken at T_J = 25°C unless specifically noted otherwise.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{LIM}	Current limit response time	I_{OUT} > 20% over I_{LIM} to I_{OUT} ≤ I_{LIM}		87		µs
t_{SC}	Short circuit response time	I_{OUT} > I_{SC} to I_{OUT} ≤ I_{LIM}		5		µs
t_{OVLO}	Overvoltage lockout response time	TPS25963x Only		1.3		µs
t_{OVC}	Output clamp response time	TPS25962x Only , I_{OUT} = 2 A		5		µs
$t_{TSD,RST}$	Thermal Shutdown Auto-Retry Interval	TPS2596x1 Only		110		ms

7.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The fall time, however, is dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled.Typical Values are taken at T_J = 25°C unless specifically noted otherwise. R_{OUT} = 100 Ω, C_{OUT} = 1 µF

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 3300pF	UNIT
SR_{ON}	Output Rising slew rate	2.7 V	28.9	11.0	V/ms
		5 V	42.7	12	
		12 V	75.1	12.9	
$t_{D,ON}$	Turn on delay	2.7 V	77.5	241.1	µs
		5 V	78.9	269.8	
		12 V	82.9	337.9	
t_R	Rise time	2.7 V	74.7	196.9	µs
		5 V	94.1	333.8	
		12 V	128.4	747	
t_{ON}	Turn on time	2.7 V	152.2	438	µs
		5 V	173	603.6	
		12 V	211.3	1084.9	
$t_{D,OFF}$	Turn off delay	2.7 V	12.2	12.3	µs
		5 V	11.6	11.9	
		12 V	10.3	10.4	

ADVANCE INFORMATION

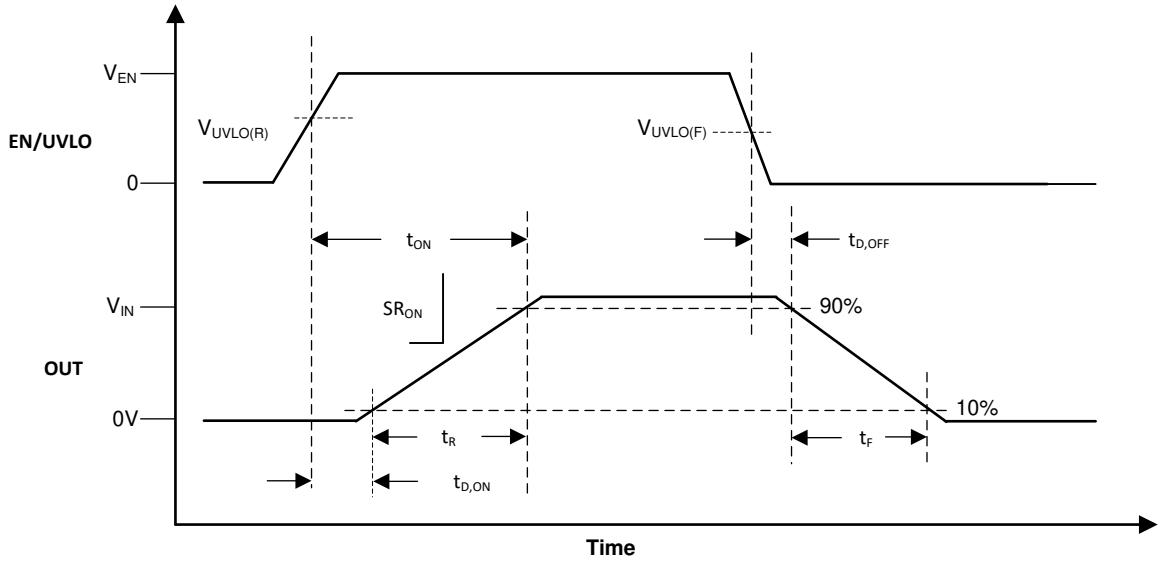
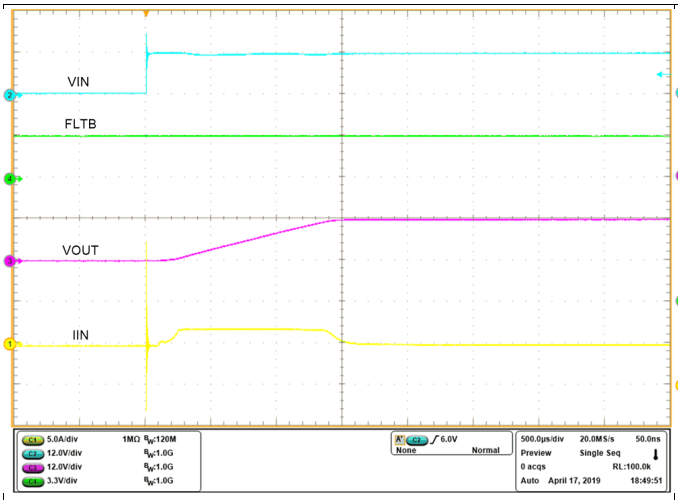


図 1. TPS2596xx Switching Times

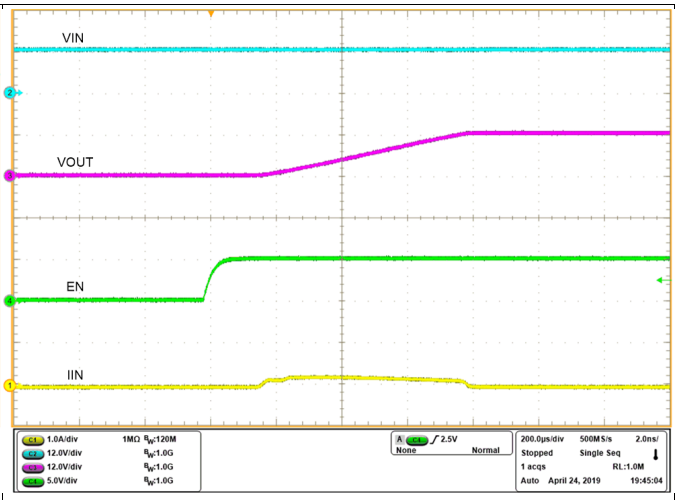
ADVANCE INFORMATION

7.8 Typical Characteristics



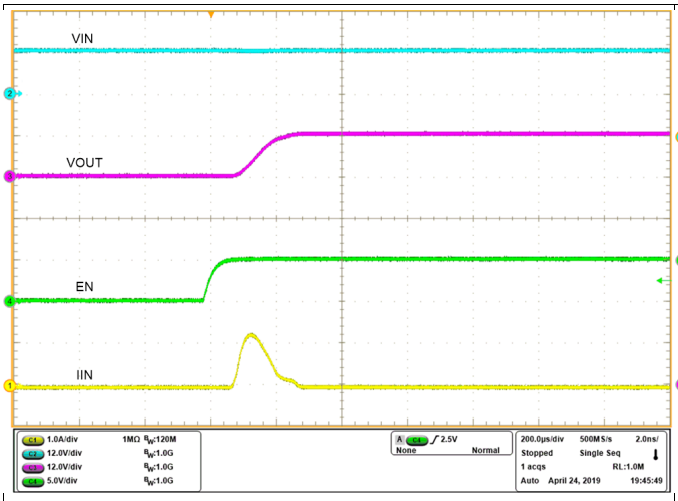
V_{IN} = 12 V, C_{OUT} = 220 µF, R_{ILM} = 453 Ω

図 2. Input Hotplug Response



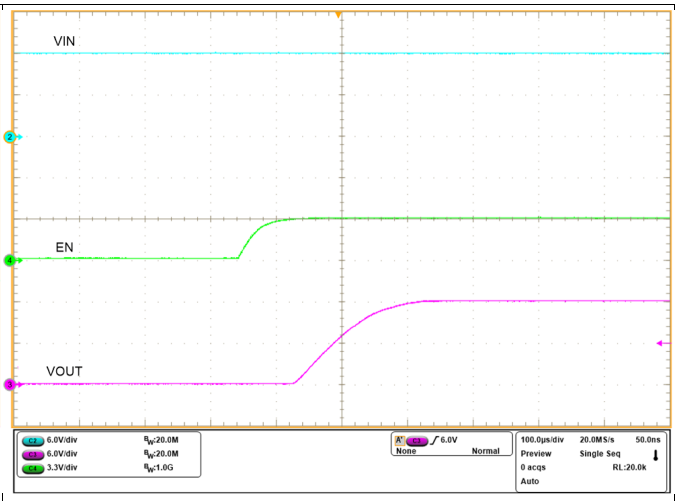
V_{IN} = 12 V, C_{OUT} = 10 µF, R_{ILM} = 453 Ω, C_{DVDT} = 2200 pF

図 3. Output Voltage Ramp and Inrush Current at Start Up, C_{dVdT} = 2200 pF



V_{IN} = 12 V, C_{OUT} = 10 µF, R_{ILM} = 453 Ω, C_{DVDT} = OPEN

図 4. Output Voltage Ramp and Inrush Current at Start Up, C_{dVdT} = OPEN

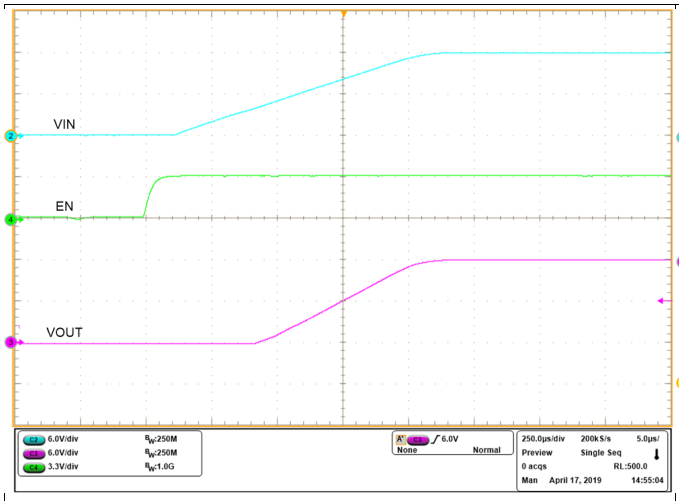


V_{IN} = 12 V, V_{EN} = 3.3 V

図 5. Turn ON with EN

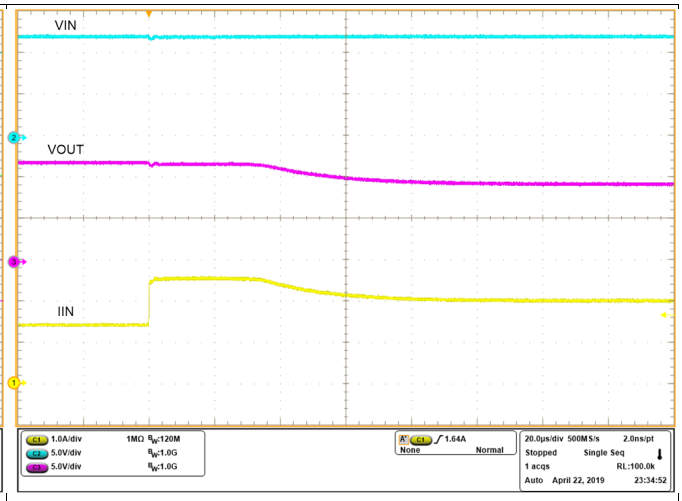
ADVANCE INFORMATION

Typical Characteristics (continued)



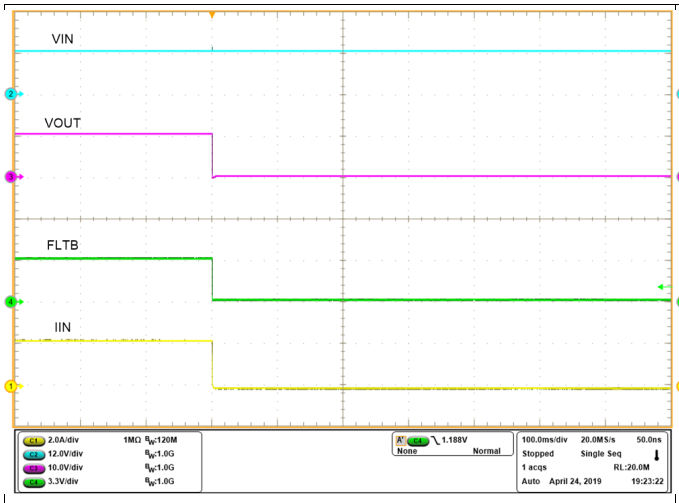
V_{IN} = 12 V, V_{EN} = 3.3 V

図 6. Turn ON with VIN



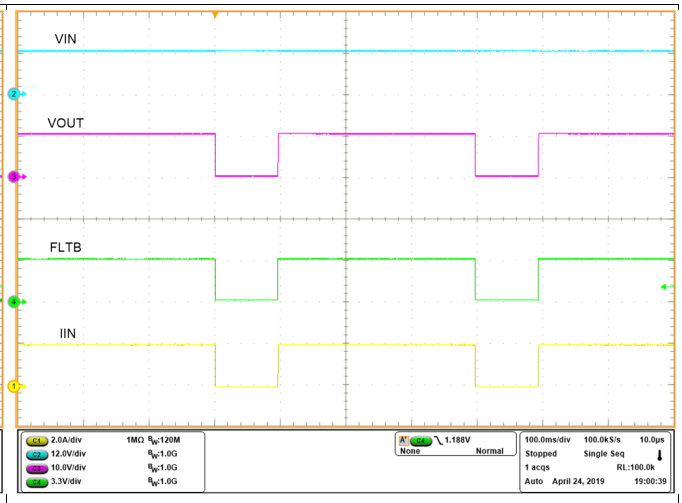
V_{IN} = 12 V, R_{ILM} = 453 Ω, R_{OUT} Varied From 8.33 Ω to 4.54 Ω

図 7. Overcurrent Response



V_{IN} = 12 V, R_{ILM} = 453 Ω, R_{OUT} = 5 Ω

図 8. Thermal Shutdown Latch-off Response - TPS2596x0

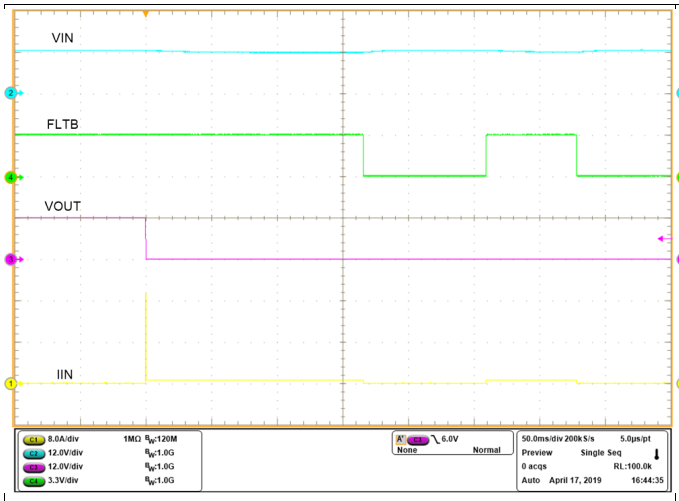


V_{IN} = 12 V, R_{ILM} = 453 Ω, R_{OUT} = 5 Ω

図 9. Thermal Shutdown Auto-Retry Response - TPS2596x1

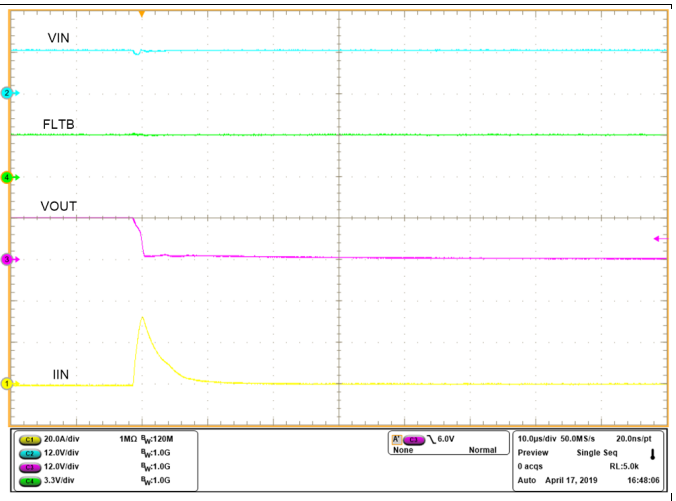
ADVANCE INFORMATION

Typical Characteristics (continued)



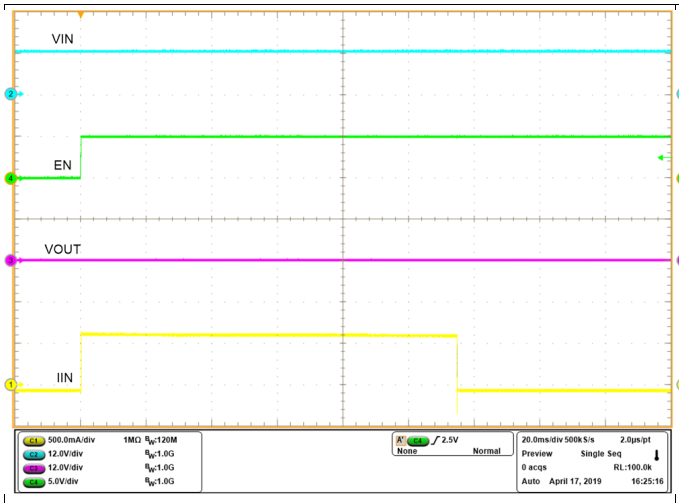
V_{IN} = 12 V, R_{ILM} = 453 Ω

図 10. Short-Circuit While ON Response



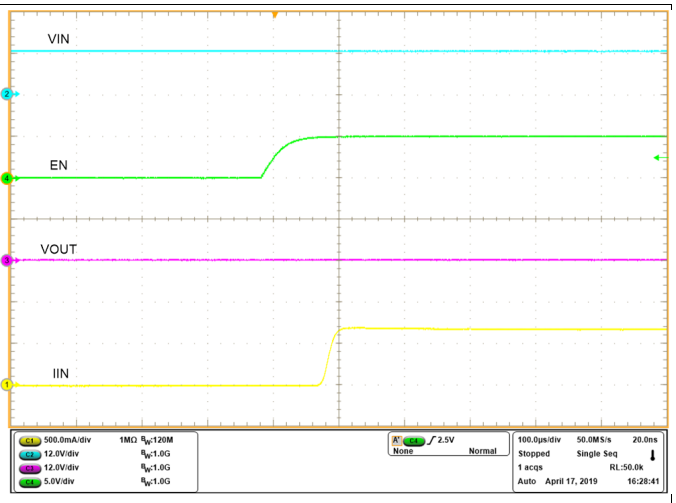
V_{IN} = 12 V, R_{ILM} = 453 Ω

図 11. Short-Circuit While ON Response (Zoomed In)



V_{IN} = 12 V, R_{ILM} = 453 Ω

図 12. Power Up Into Short-Circuit

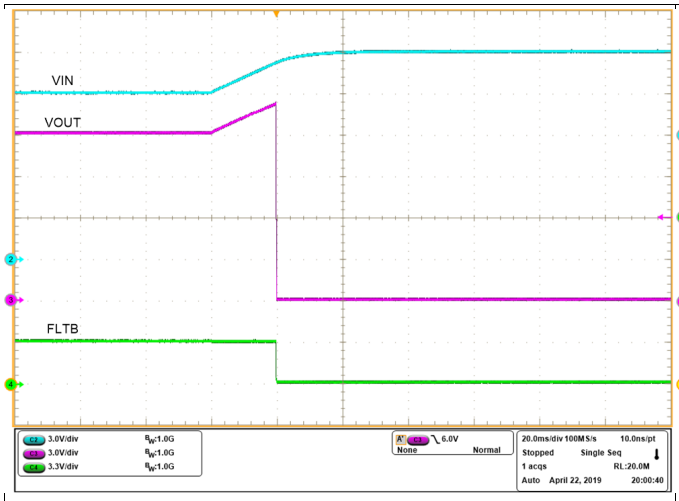


V_{IN} = 12 V, R_{ILM} = 453 Ω

図 13. Power Up Into Short-Circuit (Zoomed In)

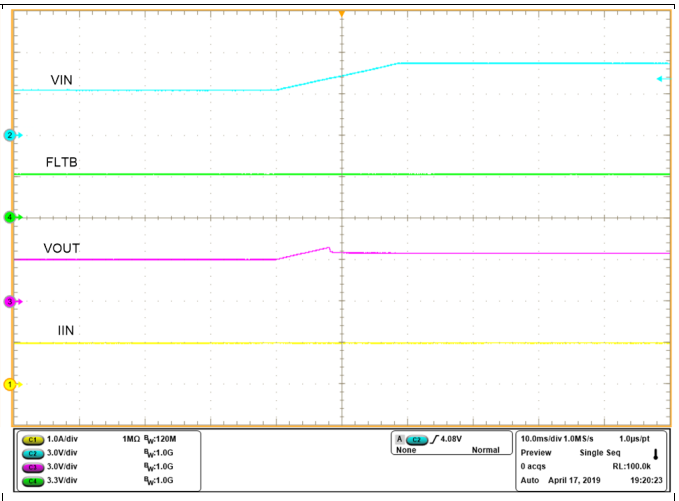
ADVANCE INFORMATION

Typical Characteristics (continued)



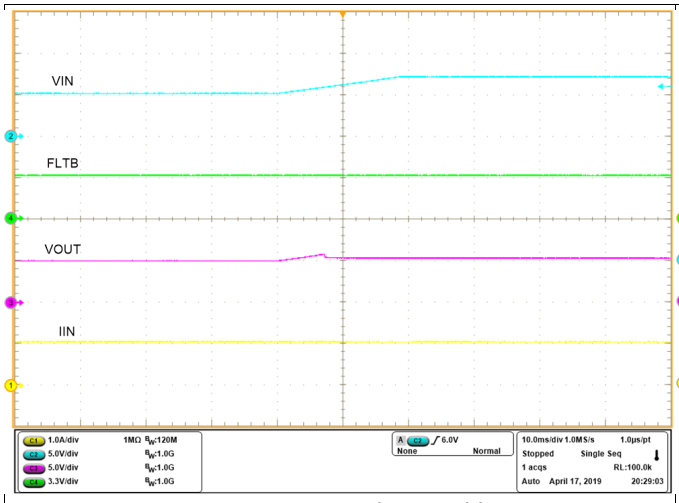
V_{IN} increased from 12 V to 15 V

図 14. TPS25963x Overvoltage Lockout Response



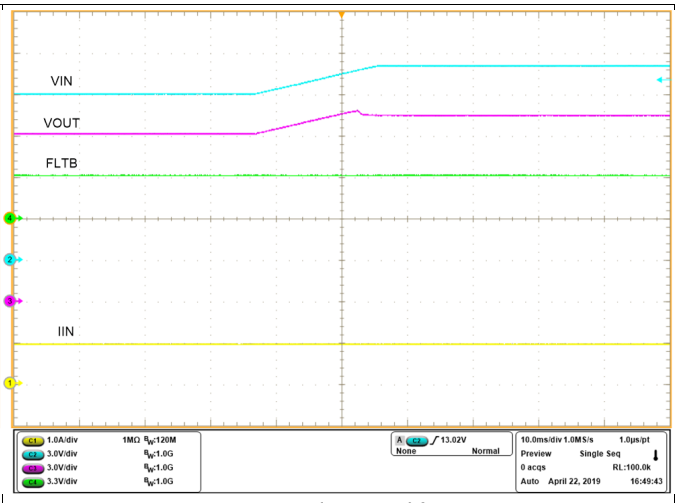
OVCSEL = Shorted to GND, V_{IN} increased from 3 V to 5 V

図 15. TPS25962x Overvoltage Clamp Response



OVCSEL = 400 KΩ to GND, V_{IN} increased from 5 V to 7 V

図 16. TPS25962x Overvoltage Clamp Response



OVCSEL = OPEN, V_{IN} increased from 12 V to 14 V

図 17. TPS25962x Overvoltage Clamp Response

ADVANCE INFORMATION

8 Detailed Description

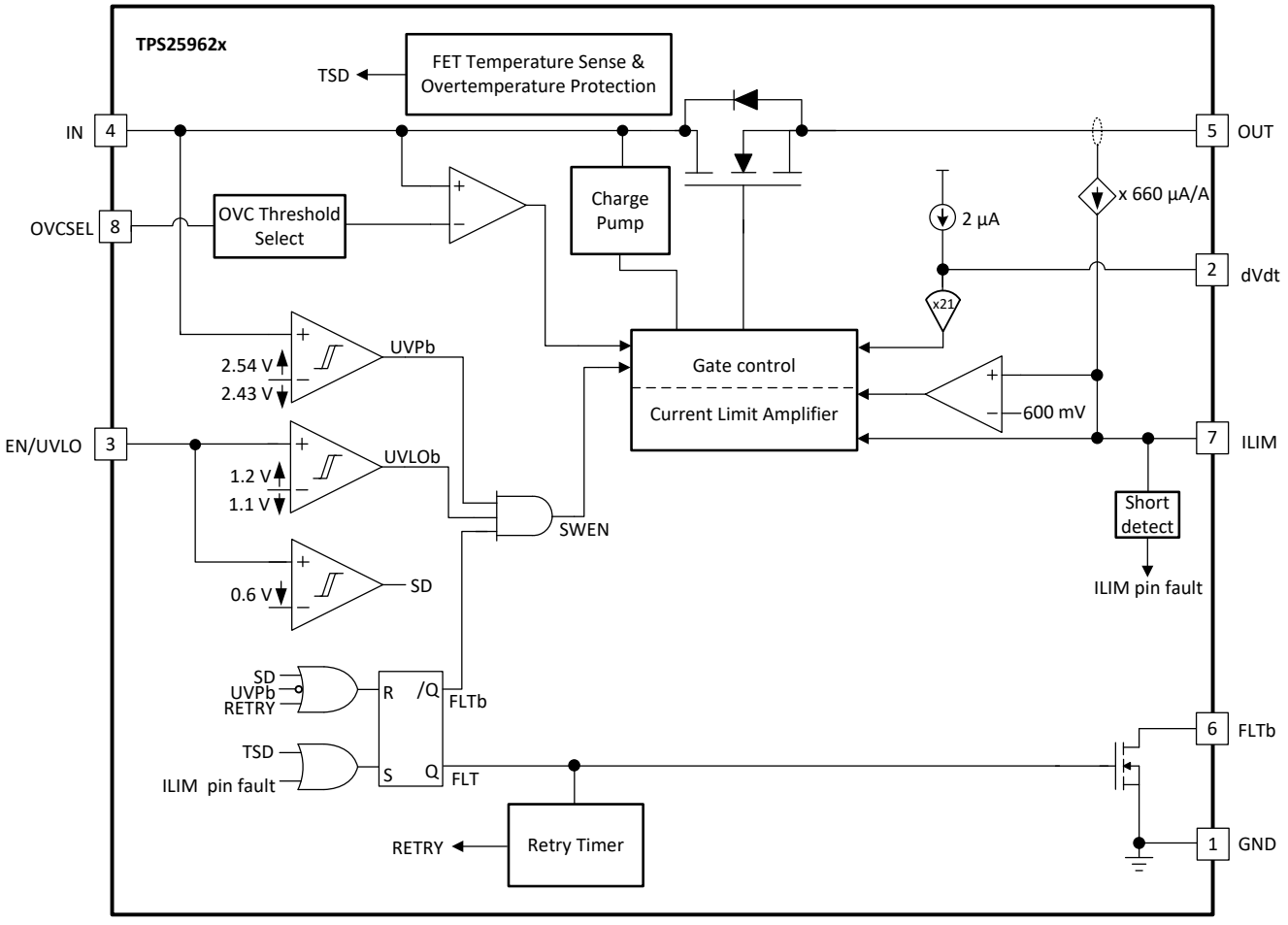
8.1 Overview

8.2 Feature Description

The TPS2596xx is an integrated eFuse device that is used to manage load voltage and load current. The device provides various factory programmed settings and user manageable settings, which allow device configuration for handling different transient and steady state supply and load fault conditions, thereby protecting the input supply and the downstream circuits connected to the device. The device also uses an in-built thermal shutdown mechanism to protect itself during these fault events.

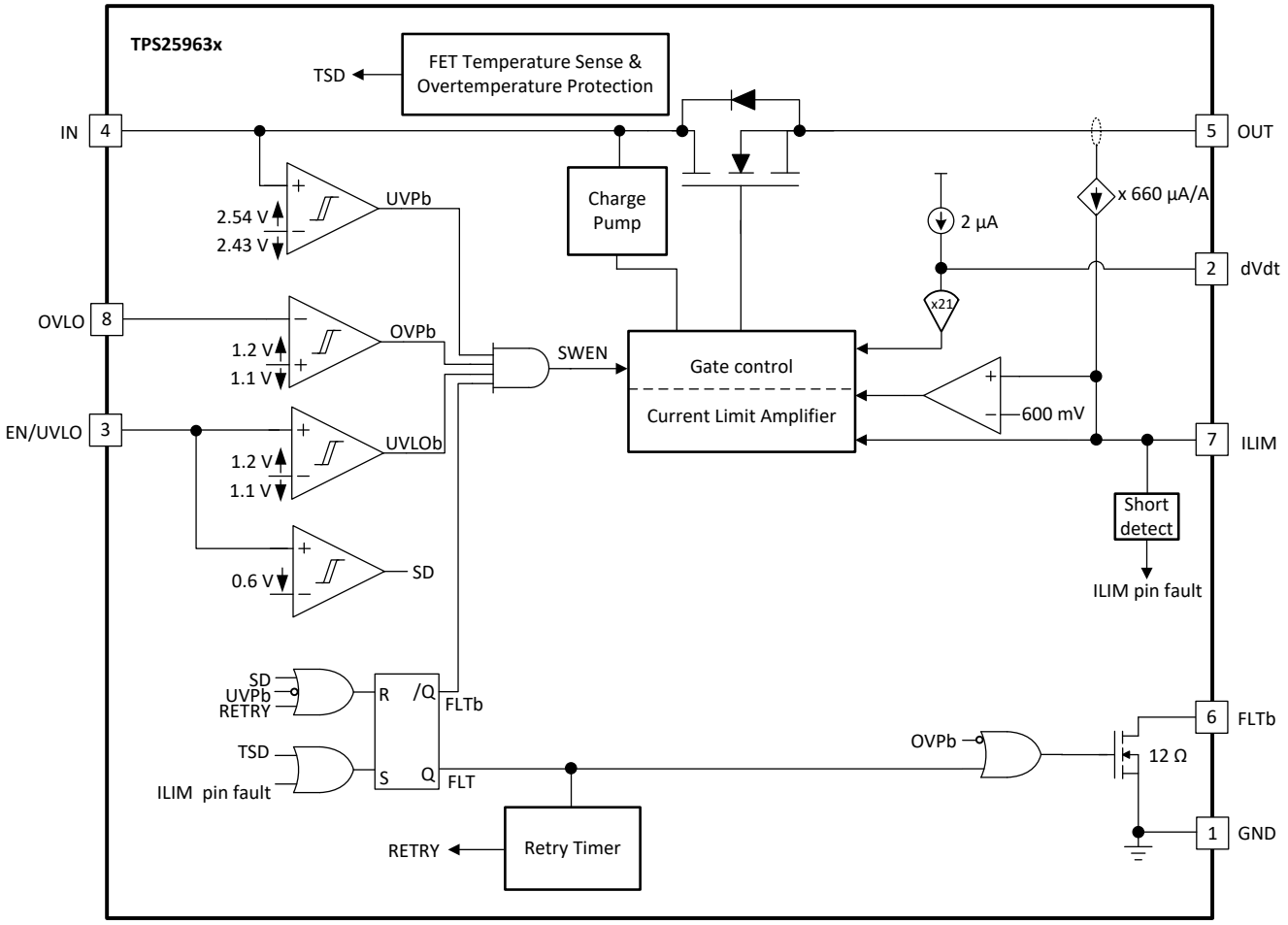
8.3 Functional Block Diagram

図 18. TPS25962x Block Diagram



Functional Block Diagram (continued)

図 19. TPS25963x Block Diagram



8.4 Feature Description

8.4.1 Undervoltage Protection (UVP) and Undervoltage Lockout (UVLO)

TPS2596xx constantly monitors the input supply to ensure that the load is powered up only when the voltage is at a sufficient level. During the start-up condition, the device waits for the input supply to rise above an internal fixed threshold $V_{UVP(R)}$ before it proceeds to turn ON the FET. Similarly, during the ON condition, if the input supply falls below the UVP threshold $V_{UVP(F)}$, the FET is turned OFF. The UVP rising and falling thresholds are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The TPS2596xx devices also provide an user programmable UVLO mechanism to ensure that the load is powered up only when the voltage is at a sufficient level. This can be achieved by dividing the input supply and feeding it to the EN/UVLO pin. Whenever the voltage at the EN/UVLO pin falls below a threshold $V_{UVLO(F)}$, the device turns OFF the FET. The FET is turned ON again when the voltage rises above the threshold $V_{UVLO(R)}$. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The user must choose the resistor divider values appropriately to map the desired input undervoltage level to the UVLO threshold of the part.

ADVANCE INFORMATION

Feature Description (continued)

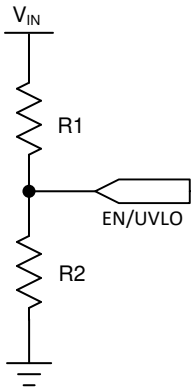


図 20. Programmable Undervoltage Lockout

$$V_{IN(UV)} = V_{UVLO(F)} \times \frac{(R1 + R2)}{R2} \quad (1)$$

8.4.2 Overvoltage Protection

The TPS2596xx devices provide 2 ways to handle an input overvoltage condition.

8.4.2.1 Overvoltage Lockout

The TPS25963x device provides an user programmable OVLO mechanism to ensure that the supply to the load is cut off if the input supply voltage exceeds a certain level. This can be achieved by dividing the input supply and feeding it to the OVLO pin. Whenever the voltage at the OVLO pin rises above a threshold $V_{OVLO(R)}$, the device turns OFF the FET. When the voltage at the OVLO pin falls below the threshold $V_{OVLO(F)}$, the FET is turned ON again. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

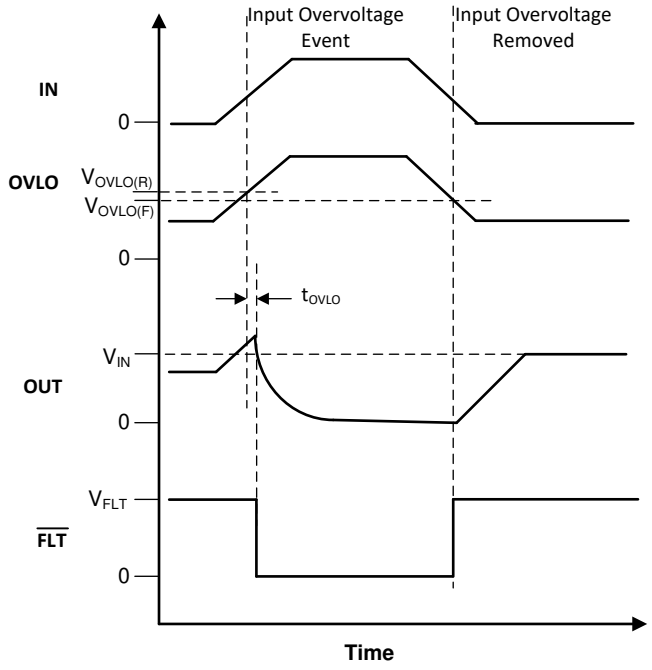


図 21. TPS25963x Overvoltage Lockout Response

Feature Description (continued)

The user should choose the resistor divider values appropriately to map the desired input overvoltage level to the OVLO threshold of the part.

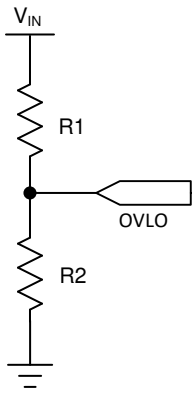


図 22. TPS25963x Programmable Overvoltage Lockout

$$V_{IN(OV)} = V_{OVLO(R)} \times \frac{(R1 + R2)}{R2} \quad (2)$$

8.4.2.2 Overvoltage Clamp

The TPS25962x devices provide a mechanism to clamp the output voltage to a user-selectable level quickly if the input voltage crosses a certain threshold. This ensures the load is not exposed to high voltages during any input overvoltage events and lowers the dependence on external protection devices (such as TVS/Zener diodes) in this condition. Once the input supply voltage rises above the OVC threshold voltage V_{OVC}, the device responds by clamping the voltage to V_{CLAMP} within a very short response time t_{OVC}. As long as an overvoltage condition is present on the input, the output voltage will be clamped to V_{CLAMP}. When the input drops below the output clamp threshold V_{OVC}, the clamp releases the output voltage. See 図 23.

ADVANCE INFORMATION

Feature Description (continued)

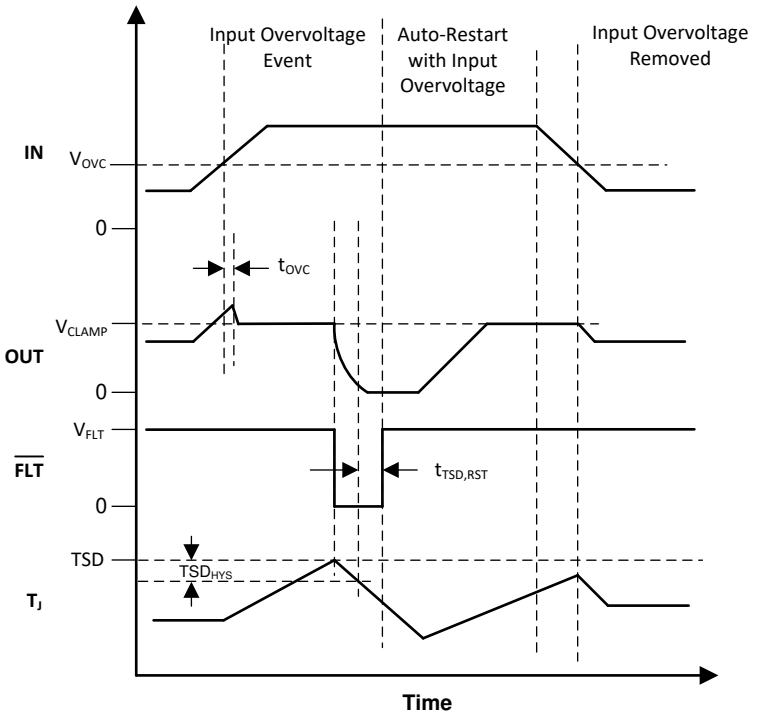


図 23. TPS25962x Overvoltage Clamp Response

The OVC threshold can be configured to one of 3 pre-defined levels by connecting the OVCSEL pin as shown in 表 2.

表 2. TPS25962x Overvoltage Threshold Selection

OVCSEL Pin Connection	OVC Threshold (typ)
Shorted to GND	3.8 V
Connected to GND through 400 KΩ resistor	5.7 V
Open	13.7 V

During the overvoltage clamp condition, there could be significant heat dissipation in the internal FET depending on the V_{IN} - V_{OUT} voltage drop and the current through the FET leading to a thermal shutdown if the condition persists for an extended period of time. In this case, the device would either stay latched-off or start an auto-retry cycle as explained in the Overtemperature Protection (OTP) section.

8.4.3 Inrush Current, Overcurrent and Short Circuit Protection

The TPS2596xx devices incorporate three levels of protection against overcurrent:

- Adjustable slew rate for inrush current control (dVdt)
- Active current limiting (I_{LIM}) for overcurrent protection
- A fast short circuit limit (I_{SC}) to protect against hard short circuits.

8.4.3.1 Slew Rate and Inrush Current Control (dVdt)

The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. 式 3 can be used to find the slew rate SR_{ON} required to limit the inrush current I_{INRUSH} for a given load capacitance C_{OUT}.

$$SR(mV/\mu s) = \frac{I_{INRUSH}(mA)}{C_L(\mu F)} \quad (3)$$

For loads requiring a slower rising slew rate, a capacitance can be added to the dVdt pin to adjust the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using 式 4.

$$C_{dVdt}(pF) = \frac{42000}{SR(mV/\mu s)} \quad (4)$$

8.4.3.2 Active Current Limiting

The load current is monitored during start-up and normal operation. When the load current exceeds the current limit I_{LIM} programmed by R_{ILM} resistor, the device regulates the current to the set limit I_{LIM} within t_{LIM}. The device exits current limiting when the load current falls below I_{LIM}. 式 5 can be used to find the R_{ILM} value for a desired current limit.

$$R_{ILM}(\Omega) = \frac{905}{I_{LIM(A)} - 0.015} \quad (5)$$

In the current limiting state, the output voltage drops resulting in increased power dissipation in the internal FET leading to a thermal shutdown if the condition persists for an extended period of time. In this case, the device either stays latched-off or starts an auto-retry cycle as explained in the Overtemperature Protection (OTP) section.

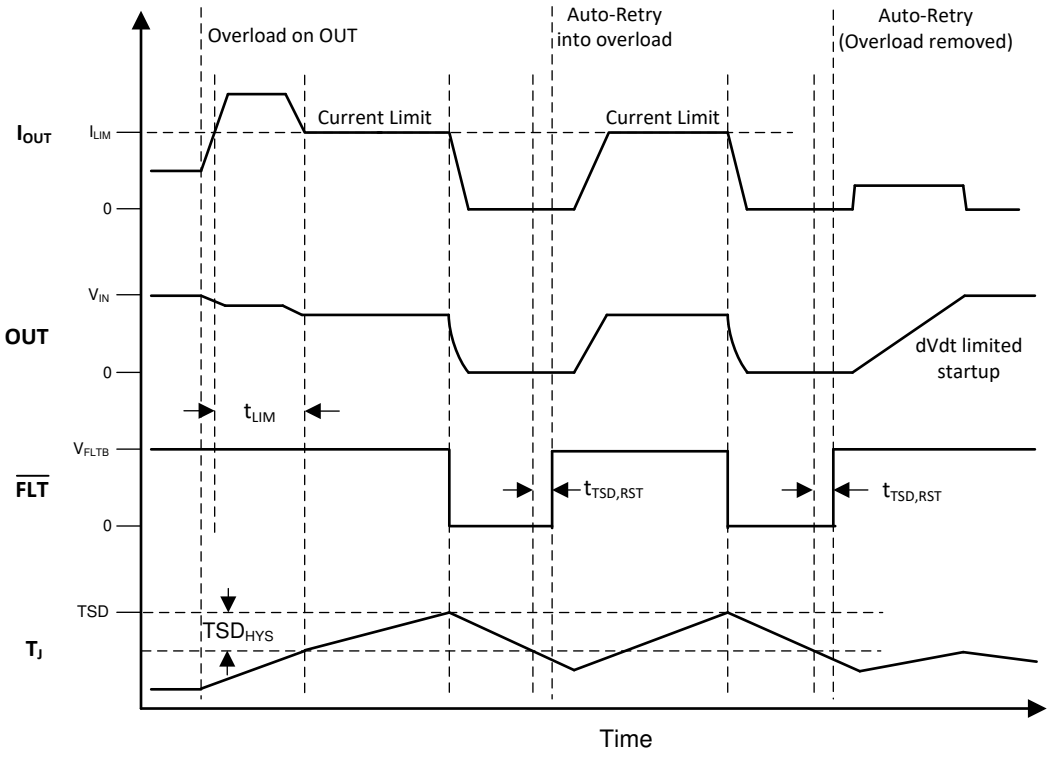


図 24. TPS2596x1 Overcurrent Response (Auto-retry)

ADVANCE INFORMATION

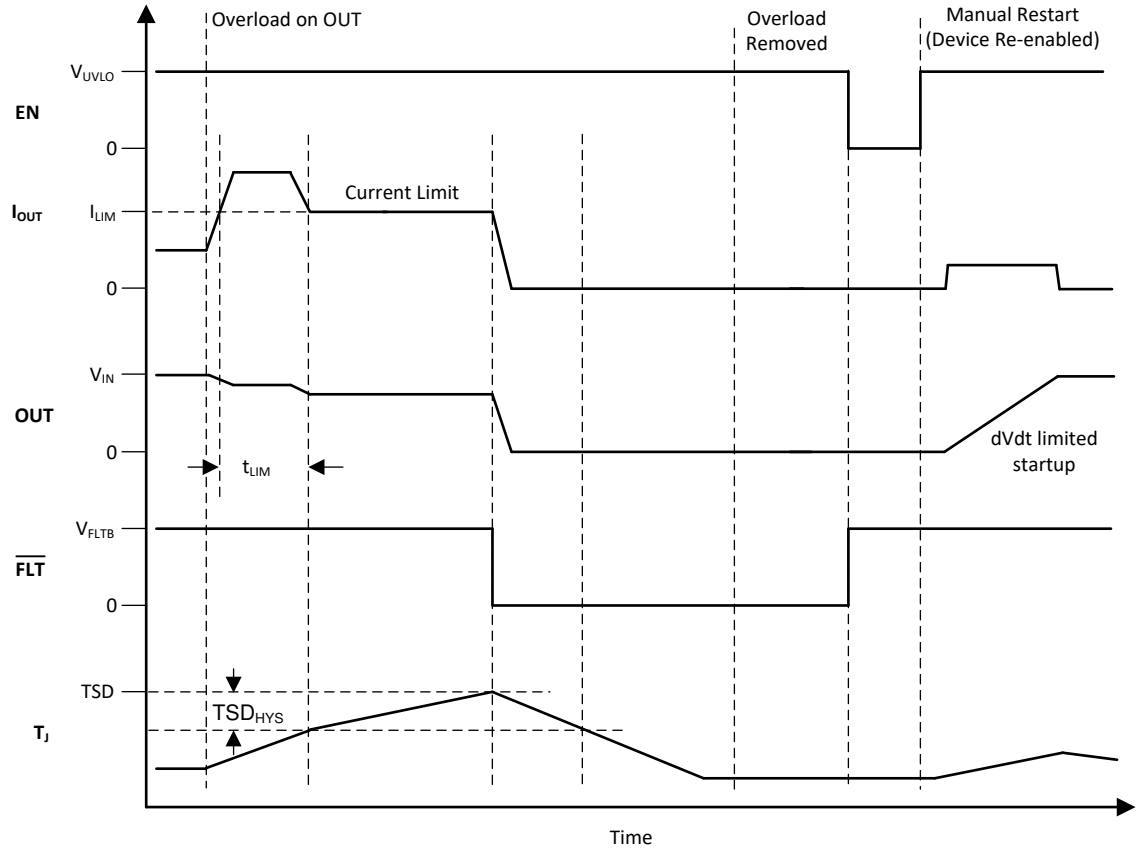


図 25. TPS2596x0 Overcurrent Response (Latch-off)

8.4.3.3 Short Circuit Protection

The current through the device increases very rapidly during a transient short circuit event. If the current exceeds 1.5 x I_{LIM}, the device engages a fast current clamping circuit to regulate down the current faster than the nominal overcurrent response time (t_{LIM}). The device does not completely turn off the power FET to ensure uninterrupted power in the event of transient overcurrents or supply transients. The device stops limiting the current once the load current falls below the programmed I_{LIM} threshold.

The output voltage drops in the current limiting state, resulting in increased power dissipation in the internal FET and might lead to thermal shutdown if the condition persists for an extended period of time. In this case, the device either stays latched-off or starts an auto retry cycle as explained in the Overtemperature Protection (OTP) section.

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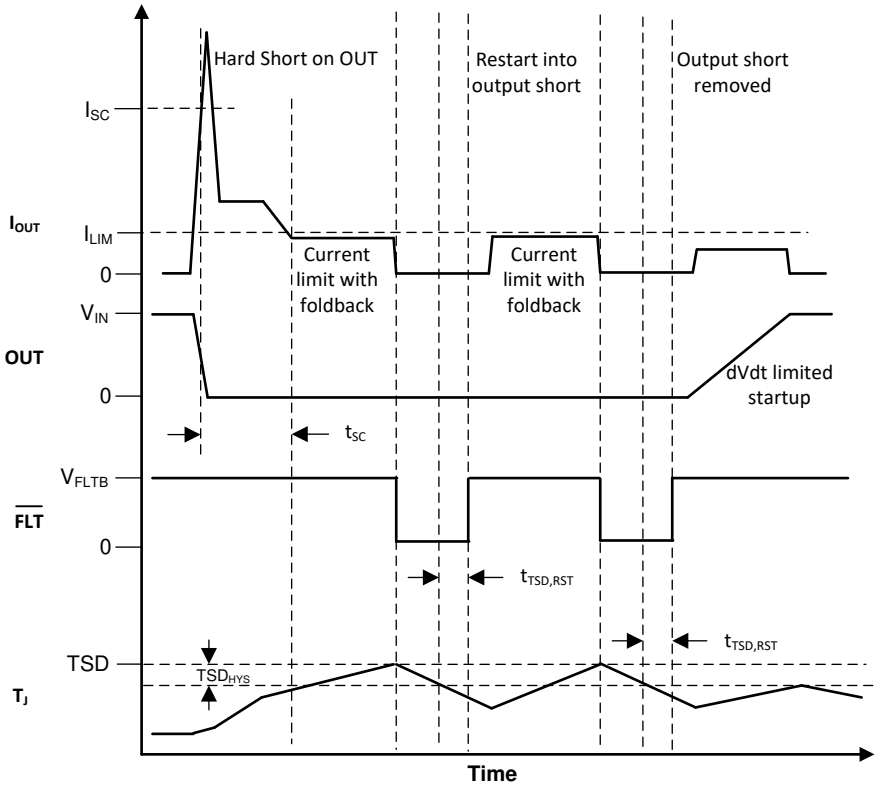

図 26. TPS2596xx Short Circuit Response

8.4.4 Analog Load Current Monitor (IMON)

The device allows the system to monitor the output load current accurately by providing an analog current on the ILM pin which is proportional to the current through the FET. The user can sense the voltage (V_{ILM}) across the R_{ILM} to get a measure of the output load current.

$$I_{OUT}(A) = \frac{V_{ILM}(V)}{G_{IMON}(\mu A / A) \times R_{ILM}(\Omega)} \quad (6)$$

8.4.5 Overtemperature Protection (OTP)

Thermal Shutdown will occur when the junction temperature (T_J) exceeds the thermal shutdown threshold (TSD). When the TPS2596x0 variant detects thermal overload, it will be shut down and remain latched off until the device is power cycled or re-enabled by toggling the EN/UVLO pin. When the TPS2596x1 variant detects thermal overload, it will remain off until it has cooled down sufficiently. Once the TPS2596x1 junction has cooled down below TSD - TSD_{HYS}, it will remain off for an additional delay of $t_{TSD,RST}$ after which it will automatically retry to turn on if it is still enabled.

表 3. TPS2596x Thermal Shutdown

Device	Enter TSD	Exit TSD
TPS2596x0 (Latch-Off)	$T_J \geq$ TSD	$T_J <$ TSD - TSD_{HYS} and Power Cycle ($V_{IN} < V_{UVP(F)}$) / Enable Cycle ($V_{EN} < V_{SD}$)
TPS2596x1 (Auto-Retry)	$T_J \geq$ TSD	$T_J <$ TSD - TSD_{HYS} and $t_{TSD-RST}$ timer expired

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8.4.6 Fault Indication

表 4 summarizes the protection response to various fault conditions.

表 4. Fault Response

Event / Fault	Protection Response	$\overline{FLT}$ Asserted	$\overline{FLT}$ Delay
Overtemperature	Shutdown	Yes	
Undervoltage	Cut-off	No	
Overvoltage	Clamp (OVC - TPS25962x only)	No	
	Cut-off (OVLO - TPS25963x only)	Yes	t_{OVLO}
Overcurrent	Current Limit	No	
Short-Circuit	Current Limit	No	
ILM Pin Short to GND	Shut down	Yes	
ILM Pin Open	Shut down	No	

When the device turns off due to one of these fault conditions, the $\overline{FLT}$ pin is pulled low.

Power cycling the part or pulling the EN/UVLO pin voltage below V_{SD} clears the fault and the $\overline{FLT}$ pin is de-asserted. It also clears the $t_{TSD,RST}$ timer (Auto-retry variants only). Pulling the EN/UVLO just below the UVLO threshold ($V_{UVLO(F)}$) has no impact on the device in this condition. This is true for both Latch-off (TPS2596x0) and Auto-retry (TPS2596x1) variants.

For Auto-retry (TPS2596x1) variants, on the end of the $t_{TSD,RST}$ timer after a fault, the device restarts automatically and the $\overline{FLT}$ pin is de-asserted.

8.5 Device Functional Modes

The features of the device depend on the operating mode.

8.5.1 Enable and Fault Pin Functional Mode 1: Single Device, Self-Controlled

In this mode of operation, the device is enabled by the VIN voltage without the need of an external processor to drive the ENABLE pin. The $\overline{FLT}$ pin is optionally monitored by an external host. See 図 27.

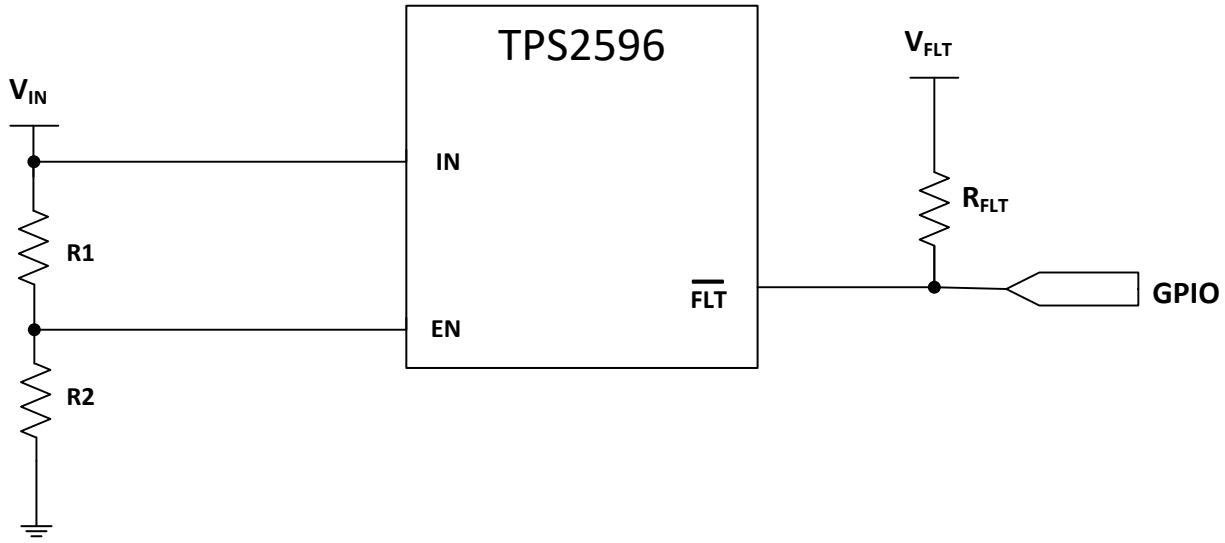

図 27. Single Device, Self-Controlled

8.5.2 Enable and Fault Pin Functional Mode 2: Single Device, Host-Controlled

In this mode of operation, the device is enabled by the VIN voltage without the need of an external processor to drive the ENABLE pin. The $\overline{FLT}$ pin is optionally monitored by an external host. See Figure 53.

Device Functional Modes (continued)

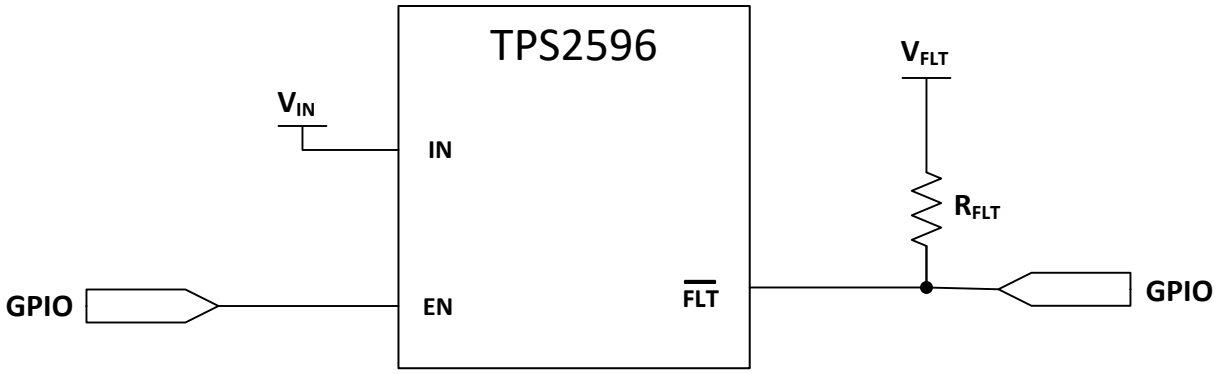

図 28. Single Device, Self-Controlled

8.5.3 Enable and Fault Pin Functional Mode 3: Multiple Devices, Self-Controlled

In this mode of operation, the devices are self-controlled (no host present). The EN and $\overline{FLT}$ pins of multiple devices are shorted together as shown in 図 28. In this configuration, when any one of the TPS2596xx devices detects a fault, it automatically disables the other TPS2596xx devices in the system.

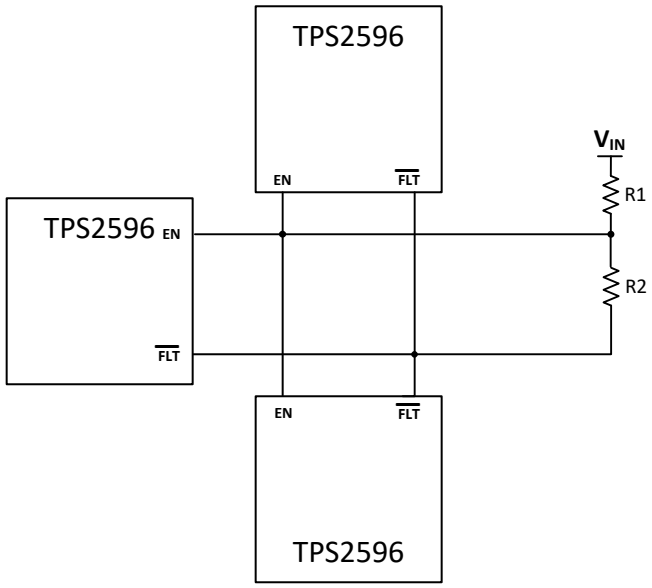

図 29. Multiple Devices, Self-Controlled

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

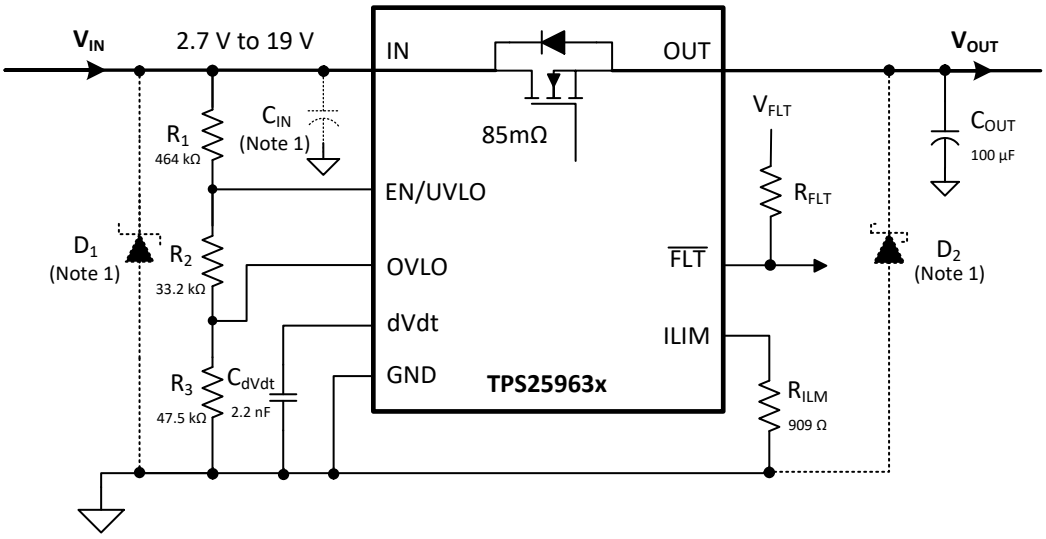
9.1 Application Information

The TPS2596xx device is an integrated eFuse that is typically used for hot-swap and power rail protection applications. The device operates from 2.7 V to 19 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as energy meters, white goods, building automation and adapter input protection. The device also provides robust protection for multiple faults on the sub-system rail.

The following design procedure can be used to select the supporting component values based on the application requirement.

9.2 Typical Application

9.2.1 Precision Current Limiting and Protection for White Goods



(1) C_{IN} is optional and 0.1 µF is recommended to suppress transients due to the inductance of PCB routing or from input wiring. If system needs to pass IEC 61000-4-4 EFT test, minimum C_{IN} of 1 µF should be used to prevent eFuse from turning off during EFT bursts.

図 30. Typical Application Schematic: Simple eFuse for White Goods

9.2.2 Design Requirements

表 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage , V_{IN}	12 V
Undervoltage lockout set point, V_{UV}	8 V
Overvoltage protection set point , V_{OV}	13.7 V
Overvoltage protection type	Lock-out
Load at start-up, $R_{L(SU)}$	24 Ω

ADVANCE INFORMATION

Typical Application (continued)

表 5. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Current limit, I_{LIM}	1 A
Load capacitance, C_{OUT}	100 µF
Maximum ambient temperatures, T_A	85°C

9.2.3 Detailed Design Procedure

The designer must know the following:

- Normal input operation voltage
- Maximum output capacitance
- Maximum current limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

9.2.3.1 Programming the Current-Limit Threshold: R_{ILM} Selection

The R_{ILM} resistor at the ILM pin sets the over load current limit, this can be set using 式 7.

$$R_{ILM}(\Omega) = \frac{905}{I_{LIM}(A) - 0.015} = \frac{905}{1 - 0.015} = 918.7\ \Omega \tag{7}$$

Choose closest standard value resistor: 909 Ω with 1% tolerance.

9.2.3.2 Undervoltage and Overvoltage Lockout Set Point

The undervoltage lockout (UVLO) and overvoltage lockout (OVLO) trip point is adjusted using the external voltage divider network of R_1, R_2 and R_3as connected between IN, EN/UVLO, OVLO and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated solving 式 8 and 式 9.

$$V_{UVLO} = \frac{R_2 + R_3}{(R_1 + R_2 + R_3)} \times V_{IN(UV)} \tag{8}$$

$$V_{OVLO} = \frac{R_3}{(R_1 + R_2 + R_3)} \times V_{IN(OV)} \tag{9}$$

Where $V_{UVLO(R)}$ is UVLO rising threshold (1.2 V). Because R_1, R_2 and R_3 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}.

The current drawn by R_1, R_2 and R_3 from the power supply is $I_{R123} = V_{IN} / (R_1 + R_2 + R_3)$.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{R123} must be chosen to be 20 times greater than the leakage current expected.

From the device electrical specifications, V_{OVLO} = 1.2 V and V_{UVLO} = 1.2 V. For design requirements, V_{OV} = 13.7 V and V_{UV} = 8 V. To solve the equation, first choose the value of R_3 = 47 kΩ and use 式 9 to solve for (R_1 + R_2) = 489.58 kΩ. Use Equation 8 and value of (R_1 + R_2) to solve for R_2 = 33.48 kΩ and finally R_1= 456.1 kΩ. Using the closest standard 1% resistor values gives R_1 = 464 kΩ, R_2 = 33.2 kΩ, and R_3 = 47.5 kΩ.

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9.2.3.3 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The required ramp-up capacitor C_{dVdT} is calculated considering the two possible cases (see Case 1: Start-Up Without Load. Only Output Capacitance C_{OUT} Draws Current and Case 2: Start-Up With Load. Output Capacitance C_{OUT} and Load Draw Current).

9.2.3.3.1 Case 1: Start-Up Without Load. Only Output Capacitance C_{OUT} Draws Current

During start-up, as the output capacitor charges, the voltage drop as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using 式 11.

For TPS2596xx device, the inrush current is determined as shown in 式 10.

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{T_{dVdT}} \tag{10}$$

Power dissipation during start-up is shown in 式 11.

$$P_{D(INRUSH)} = 0.5 \times V_{IN} \times I_{INRUSH} \tag{11}$$

式 11 assumes that load does not draw any current until the output voltage has reached its final value.

9.2.3.3.2 Case 2: Start-Up With Load. Output Capacitance C_{OUT} and Load Draw Current

When the load draws current during the turnon sequence, there is additional power dissipated. Considering a resistive load during start-up $R_{L(SU)}$, load current ramps up proportionally with increase in output voltage during T_{dVdT} time. Equations 12 to 15 show the average power dissipation in the internal FET during charging time due to resistive load.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V_{IN}^2}{R_{L(SU)}} \tag{12}$$

Total power dissipated in the device during start-up is 式 13.

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \tag{13}$$

Total current during start-up is given by 式 14.

$$I_{STARTUP} = I_{INRUSH} + I_L(t) \tag{14}$$

If $I_{STARTUP} > I_{LIMIT}$, the device limits the current to I_{LIMIT} and the current-limited charging time is determined by 式 15.

$$T_{dvdT(Current-Limited)} = C_{OUT} \times R_{L(SU)} \times \left[\frac{I_{LIMIT}}{I_{INRUSH}} - 1 + LN\left(\frac{I_{INRUSH}}{I_{LIMIT} - \frac{V_{IN}}{R_{L(SU)}}} \right) \right] \tag{15}$$

The power dissipation, with and without load, for selected start-up time must not exceed the shutdown limits as shown in 図 31.

ADVANCE INFORMATION

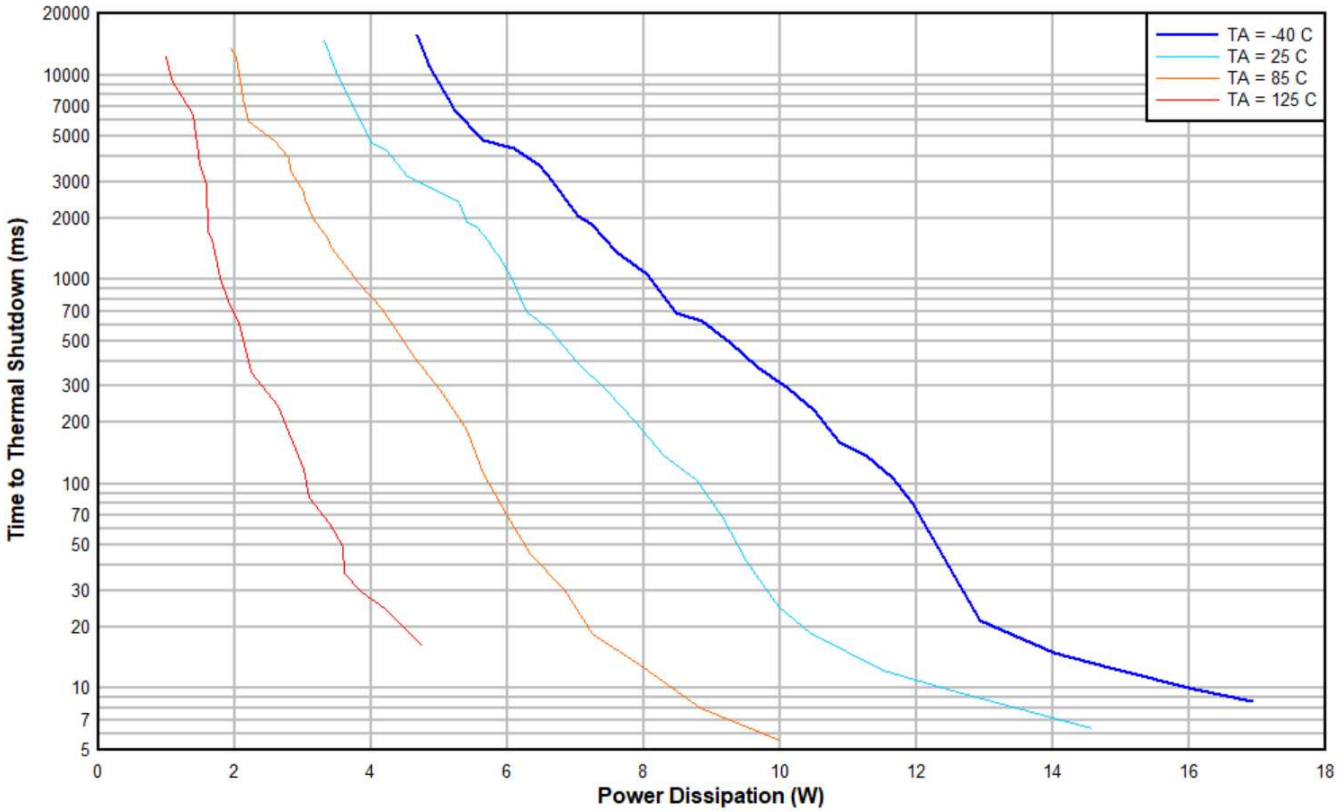


図 31. Thermal Shutdown Limit Plot

For the design example under discussion, select ramp-up capacitor C_{dVdt} = 22000 pF. The default slew rate for C_{dVdt} = 22000 pF is 1.9 mV/µs. With slew rate of 1.9 mV/µs, the ramp-up time T_{dVdt} for 12 V input is 6.3 ms.

The inrush current drawn by the load capacitance C_{OUT} during ramp-up using 式 16.

$$I_{INRUSH} = \frac{100\ \mu F \times 1.9\ mV}{\mu s} = 190\ mA \tag{16}$$

The inrush power dissipation is calculated using 式 17.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 190\ m = 1.14\ W \tag{17}$$

For 1.14 W of power loss, the thermal shutdown time of the device must not be less than the ramp-up time T_{dVdt} to avoid the false trip at the maximum operating temperature. 図 31 shows the thermal shutdown limit at T_A = 85 °C, for 1.14 W of power, the shutdown time is infinite. Therefore, it is safe to use 6.3 ms as the start-up time without any load on the output.

The additional power dissipation when a 10-Ω load is present during start-up is calculated using 式 18.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{12 \times 12}{24} = 1W \tag{18}$$

The total device power dissipation during start-up is given in 式 19.

$$P_{D(STARTUP)} = 1 + 1.14 = 2.24\ W \tag{19}$$

The 図 31 shows T_A = 85 °C and the thermal shutdown time for 2.24 W is approximately 2000 ms, which increases the margins further for shutdown time and ensures successful operation during start up and steady state conditions.

ADVANCE INFORMATION

When C_{OUT} is large, there is a need to decrease the power dissipation during start-up. This can be done by increasing the value of the C_{dVdt} capacitor.

9.2.4 Support Component Selection: R_{FLT} and C_{IN}

Reference to application schematics, R_{FLT} is required only if $\overline{FLT}$ is used; The resistor serves as pull-up for the open-drain output driver. The current sunk by this pin should not exceed 10 mA. C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range from 0.001 µF to 0.1 µF is recommended for C_{IN}.

9.2.5 Application Curves

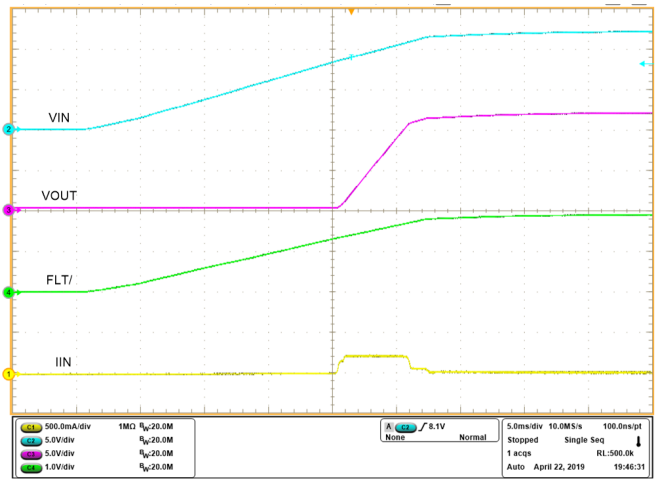


図 32. Output Ramp Without Any Load

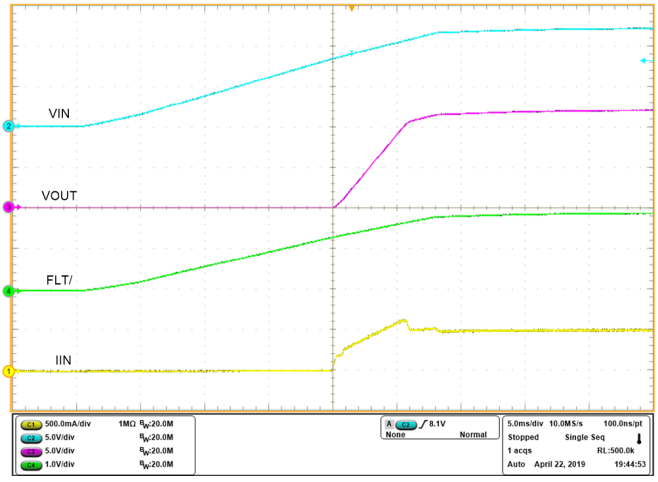


図 33. Output Ramp With 24-Ω Load at Start-up

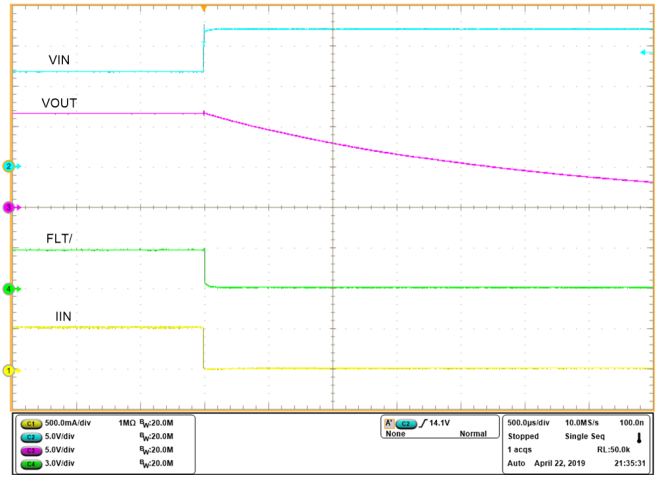


図 34. Overvoltage Protection (OVLO)

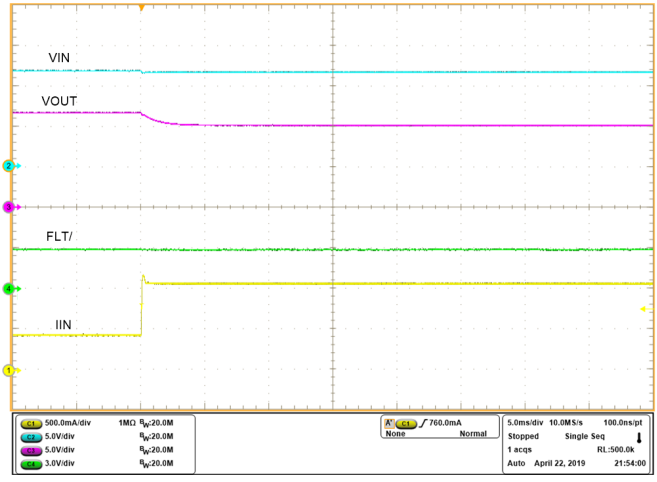


図 35. Overcurrent Protection

9.3 System Examples

The TPS2596xx provides a simple solution for current limiting, inrush current control and supervision of power rails for wide range of applications operating at 2.7 V to 19 V and delivering up to 2 A.

ADVANCE INFORMATION

System Examples (continued)

9.3.1 Current Limiting and Overvoltage Protection and for Energy Meter Power Rails

Energy meters generally use a single AC/DC power supply (for example: flyback converter) with multiple DC outputs for powering blocks like Metrology (analog front-end, microcontroller, memory), Real Time Clock (RTC), Relay (for remote load connect/disconnect) and Communications module. Metrology is the most critical sub-system and is required to operate uninterrupted under all conditions, even if a fault occurs in any of the supplementary blocks. One solution would be to oversize the power supply design so that it can handle the excess current demands during a fault condition, which increases the cost of the meter. A more elegant and cost-optimized solution would be to add an eFuse like TPS2596xx on the supplementary power rails, which provides accurate current limiting and fast short-circuit protection, thereby ensuring reliable operation of the metrology block without increasing the size or cost of the power supply. Apart from that, the TPS2596xx provides additional benefits such as:

- Overvoltage Protection (Lock-out and Clamp) to shield down-stream low voltage circuits from harmful overvoltages arising from poor cross-regulation between windings or AC input voltage surges.
- Disconnect supply to rarely used loads to minimize power consumption

図 36 shows a typical energy meter power supply implementation using TPS2596xx.

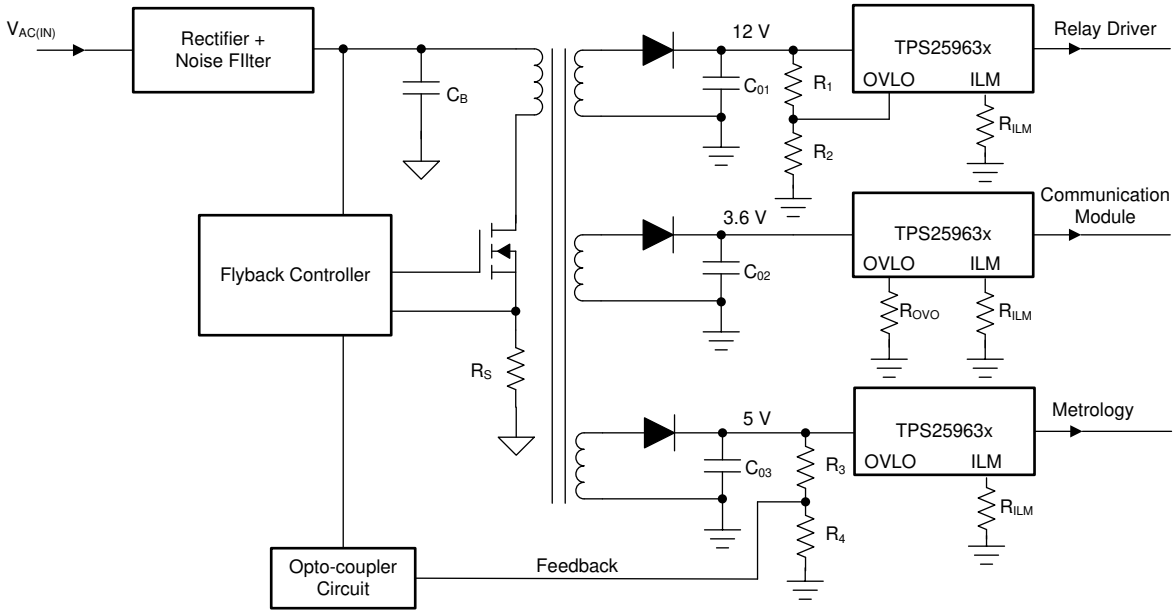


図 36. Energy Meter Power Rail Protection Example

The TIDA-010037 demonstrates energy meter design using eFuse for protecting auxiliary rails.

9.3.2 Precision Current Limiting and Protection in Appliances

Household and similar electrical appliances are subjected to various tests (for example: needle flame, glow wire) as part of the certification for electrical and fire safety compliance as per the regulations. Special precautions need to be taken in the design to pass these tests, which include the use of higher grade flame retardant plastic material for the housing enclosures. There are certain provisions in the standard which can be leveraged to make the certification easier, faster and also reduce the cost of plastic materials. For example, any node which has less than 15 W of power available to it is classified as a LPC (Low Power Circuit as per the definition in IEC 60335-1) and deemed to be safe. All circuits or sub-systems further downstream from a LPC node are exempt from the aforementioned tests.

ADVANCE INFORMATION

System Examples (continued)

eFuses like TPS2596xx are a simple and cost effective way to limit the power delivered to the downstream load. The key parameter to be considered is the current imit tolerance and accuracy, which determines how high one can set the nominal current limit without exceeding the 15 W power limit on the upper end. On the lower end, it determines the maximum power the load can draw in normal conditions without hitting the current limit. TPS2596xx provides a current limit accuracy of ±5 % (at room temperature), which allows the load to use nearly 90% out of the 15-W limit under normal operating conditions.

In contrast, an alternative current limiting solution with wider current limit tolerance, say ±25 % would leave only 50 % out of 15 W for the load circuit to operate under normal conditions. This places severe constraints on the load circuit design and/or capabilities.

図 37 shows a sub-system example of a refrigerator and freezer system where TPS2596xx is used for precision current limiting and protection of 15 W rails to ease the qualification as low-power circuit as per IEC 60335-1.

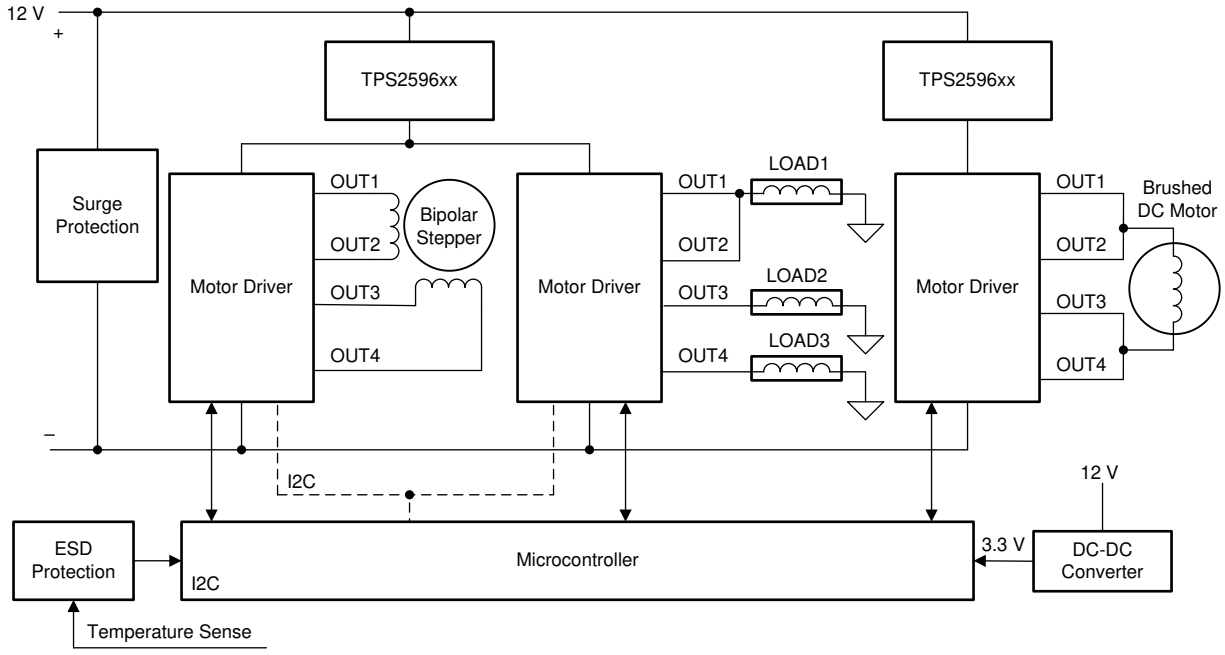


図 37. Appliances 15-W LPC Implementation Example

TIDA-010004 demonstrates a multi-load drive using single driver chip with eFuse for protection and 15-W LPC implementation.

10 Power Supply Recommendations

The TPS2596xx devices are designed for a supply voltage range of 2.7 V ≤ VIN ≤ 19 V. An input ceramic bypass capacitor higher than 0.1 µF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

10.1 Transient Protection

In the case of a short circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Use a Schottky diode across the output to absorb negative spikes.
- Use a low-value ceramic capacitor C_{IN} = 0.001 µF to 0.1 µF to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with this Equation:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}}$$

where

- V_{IN} is the nominal supply voltage
- I_{LOAD} is the load current
- L_{IN} equals the effective inductance seen looking into the source
- C_{IN} is the capacitance present at the input

NOTE: Systems which need to pass IEC 61000-4-4 tests for immunity to Electrical Fast Transients (EFT) should use a minimum C_{IN} of 1 µF to ensure the TPS2596xx doesn't turn OFF during the EFT burst.

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. The circuit implementation with optional protection components (a ceramic capacitor, TVS and Schottky diode) is shown in 図 38.

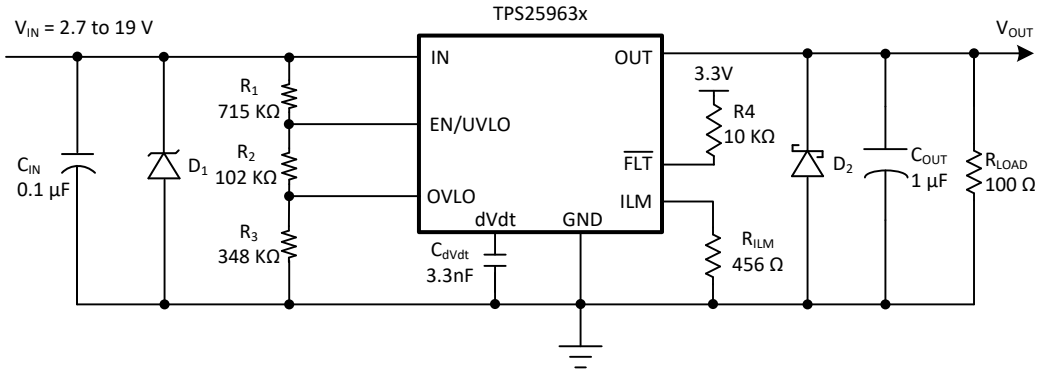


図 38. Circuit Implementation with Optional Protection Components

ADVANCE INFORMATION

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

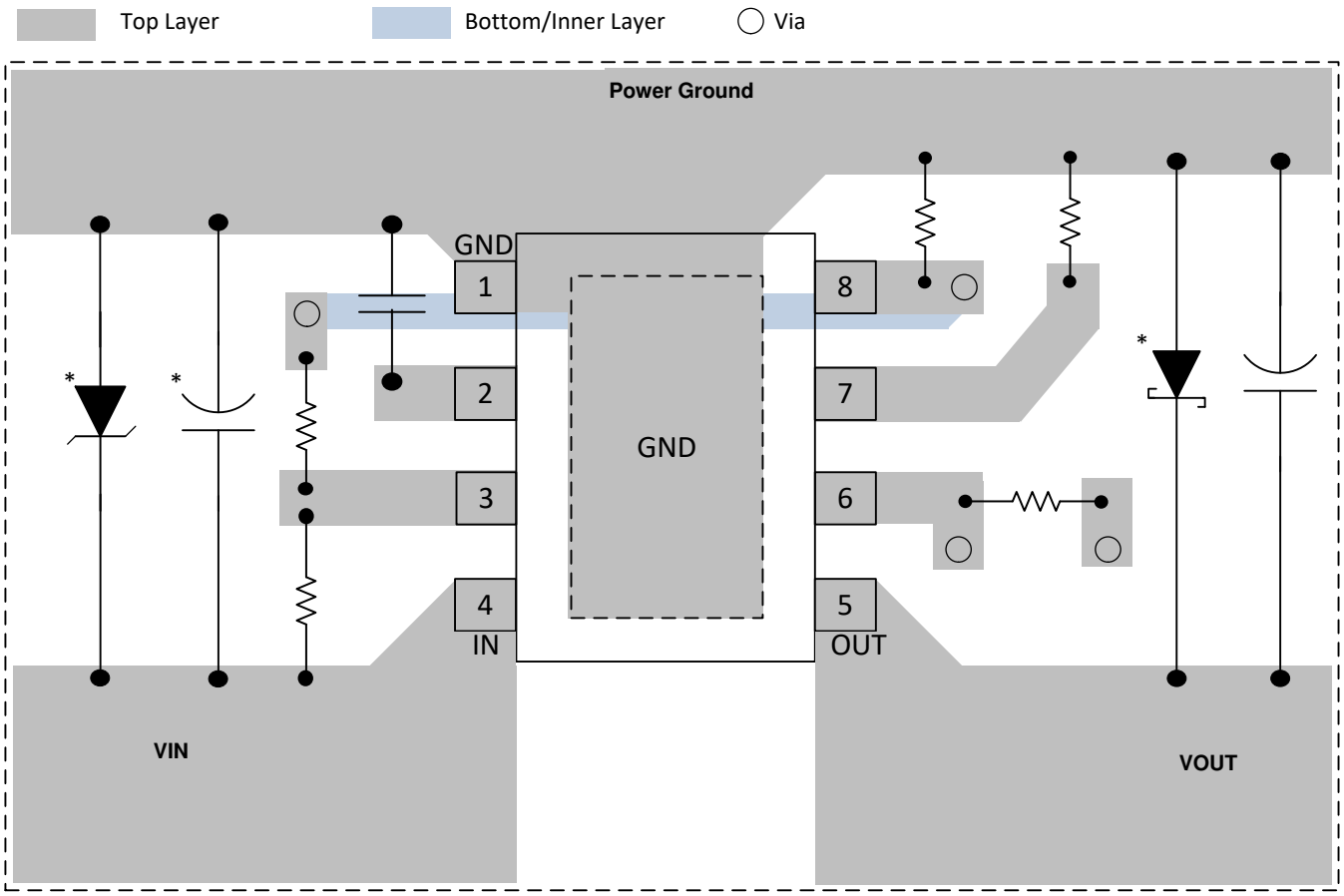
11 Layout

11.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.01 μF or greater is recommended between the IN terminal and GND terminal. For hot-plug applications, where input power-path inductance is negligible, this capacitor can be eliminated or minimized.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See 図 39 for a PCB layout example.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - Resistor network for the EN/UVLO pin
  - Resistor network for the OVLO pin for TPS25693x variants
  - Pull-down resistor on the OVCSEL pin for TPS25692x variants

  Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing from the R_{ILM}, C_{dVdT} and R_{OVCSEL} (for TPS25962x variants) components to the device pins must be as short as possible to reduce parasitic effects on the current limit, soft-start timing and overvoltage clamp response. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible; Layout Example has been shown to produce good results and is intended as a guideline.

11.2 Layout Example



* Optional: Needed only to suppress the transients caused by inductive load switching

図 39. TPS2596xx Layout Example

ADVANCE INFORMATION

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- *TPS2596EVM：評価基板、TPS2596xx 用*
- *TIDA-010037、スタンドアロン ADC を使用した高精度、相分割 CT (電流トランス) 電気メーターのリファレンス・デザイン*
- *TIDA-010004、12V、15W、電力制限、シングル・ドライバ・ベース・ステッパ、ブラシ付き DC、アクチュエータ向けドライブのリファレンス・デザイン*

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS259620DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259620
TPS259620DDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259620
TPS259620DDAT	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259620
TPS259620DDAT.A	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259620
TPS259621DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259621
TPS259621DDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259621
TPS259621DDAT	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259621
TPS259621DDAT.A	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259621
TPS259630DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259630
TPS259630DDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259630
TPS259630DDAT	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259630
TPS259630DDAT.A	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259630
TPS259631DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259631
TPS259631DDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259631
TPS259631DDAT	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259631
TPS259631DDAT.A	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	259631

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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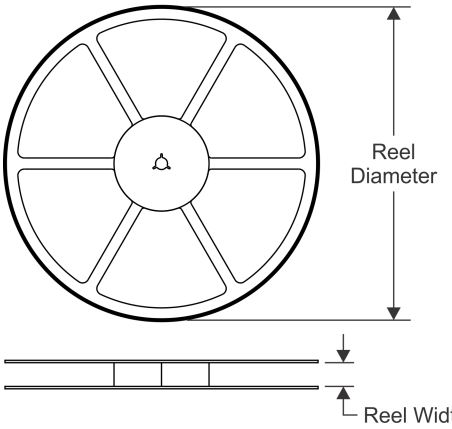
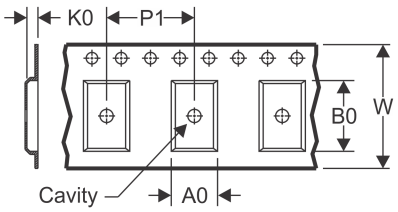
TAPE AND REEL INFORMATION

REEL DIMENSIONS

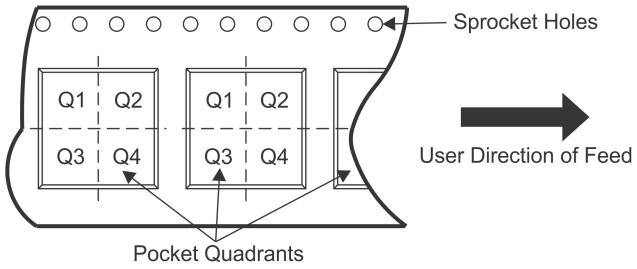


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

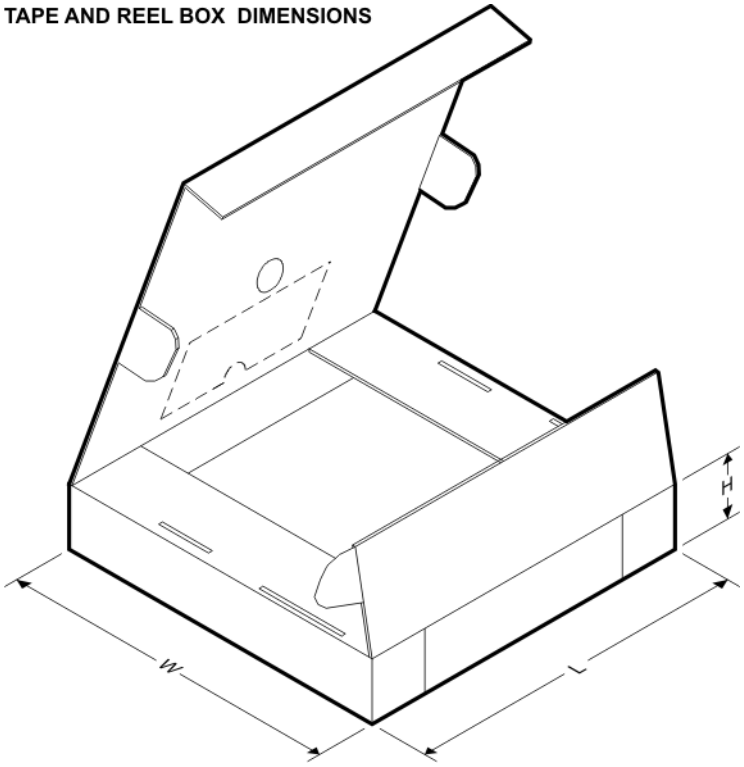


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259620DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS259620DDAT	SO Power PAD	DDA	8	250	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS259621DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS259621DDAT	SO Power PAD	DDA	8	250	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS259630DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS259630DDAT	SO Power PAD	DDA	8	250	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS259631DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS259631DDAT	SO	DDA	8	250	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	Power PAD											

TAPE AND REEL BOX DIMENSIONS

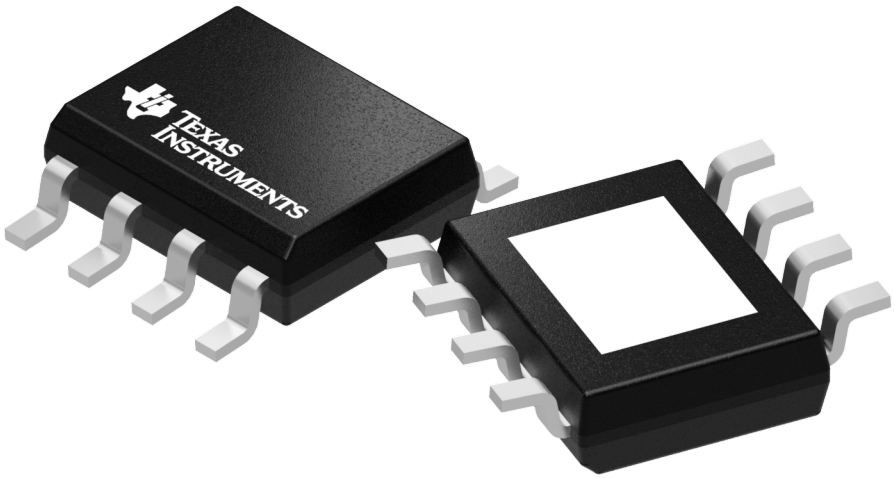


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259620DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS259620DDAT	SO PowerPAD	DDA	8	250	366.0	364.0	50.0
TPS259621DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS259621DDAT	SO PowerPAD	DDA	8	250	366.0	364.0	50.0
TPS259630DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS259630DDAT	SO PowerPAD	DDA	8	250	366.0	364.0	50.0
TPS259631DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS259631DDAT	SO PowerPAD	DDA	8	250	366.0	364.0	50.0

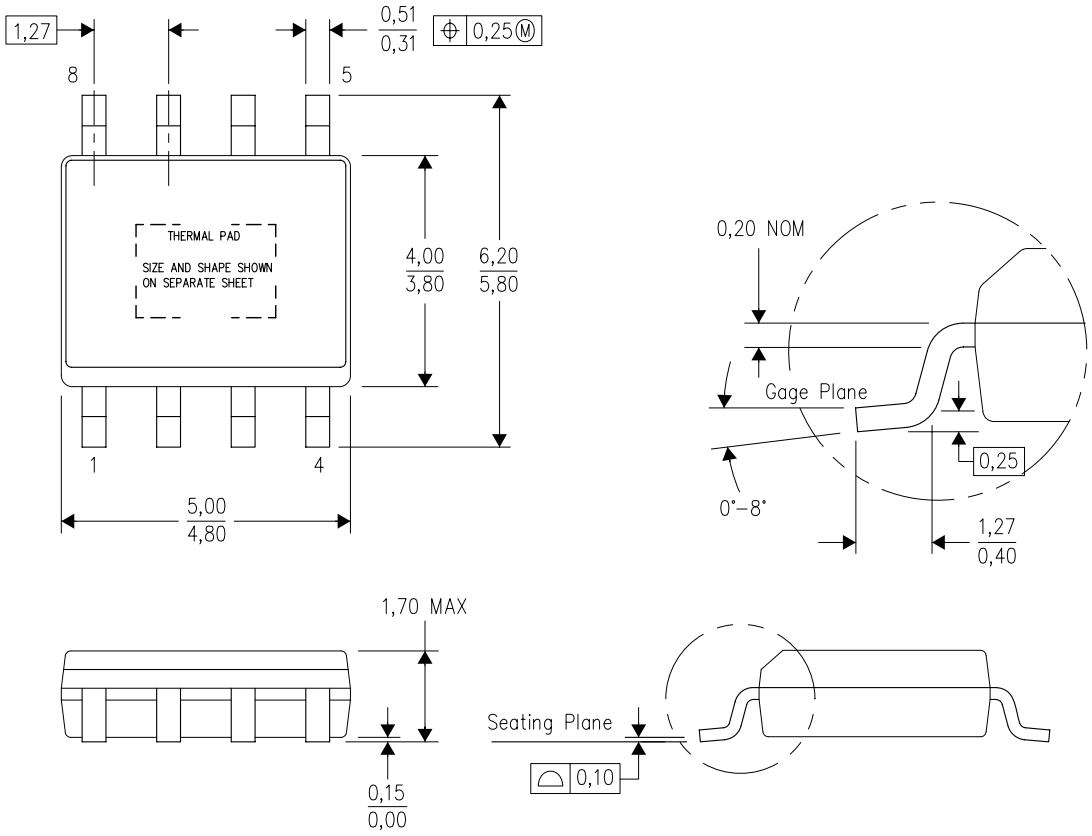
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

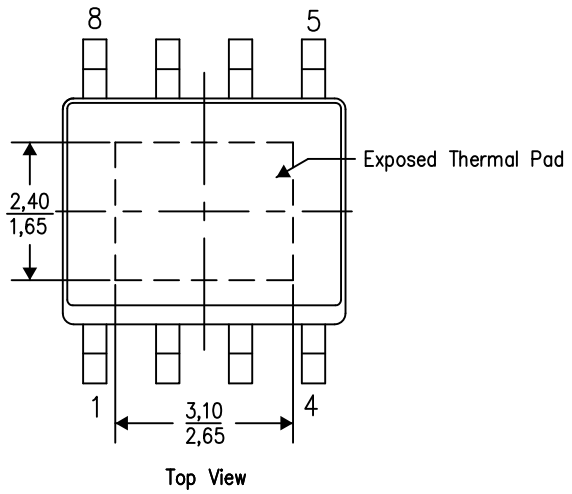
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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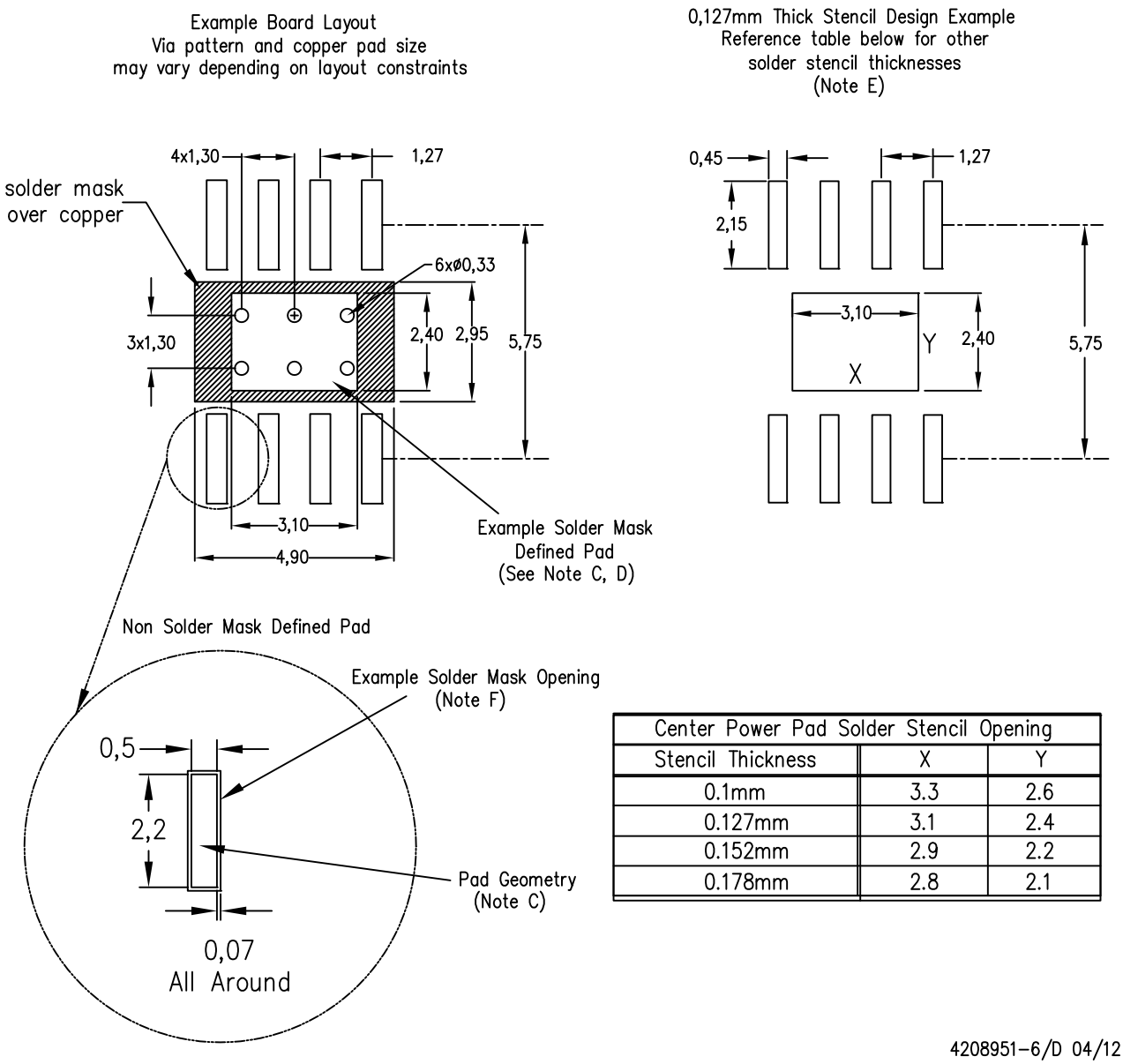
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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