TEXAS INSTRUMENTS
TPS25942A, TPS25942L, TPS25944A, TPS25944L
JAJSC23D – JUNE 2014 – REVISED OCTOBER 2017

TPS25942x/44x 2.7V～18V、5A eFuse Power MUX、複数の保護モード付き

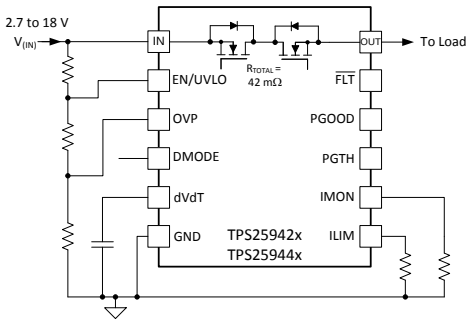
1 特長

- 動作電圧2.7V～18V、20V (最大値)
- 42mΩ R_{ON} (標準値)
- 電流制限を0.6A～5.3Aに調整可能(±8%)
- IMON電流インジケータ出力(±8%)
- 動作時I_Q: 200µA (標準値)
- ディセーブル時I_Q: 15µA (標準値)
- ±2%過電圧、低電圧スレッショルド
- 逆電流保護
- 1µsの逆電圧シャットオフ
- dV_o/dt制御をプログラム可能
- パワーグッドおよびフォルト出力
- 2つの過電流フォルト応答オプション
  - TPS25942: $I_{(LIMIT)}$とサーマル・シャットダウン
  - TPS25944: 4msのフォルト・タイマ後にシャットオフ
- 接合部温度範囲: –40℃～+125℃
- UL 2367認定済み
  - ファイル番号169910
  - R_{ILIM} ≥ 20kΩ (最大4.81A)
- UL60950 単一点障害時の安全性
  - オープン、短絡ILIMの検出

2 アプリケーション

- 電力パス管理
- 冗長化電源システム
- PCIeカード、NIC、RAIDシステム
- USBパワー・バンク、パワー・マルチプレクサ
- SSDおよびHDD
- タブレットおよびノートブックPC
- アダプタの電源デバイス
- PLC、SSリレー、ファン制御

概略回路図



3 概要

TPS25942、TPS25944 eFuse Power MUXは小型で豊富な機能を持つ電力管理デバイスで、完全な保護機能のセットが内蔵されています。動作電圧範囲が広いため、多くの一般的なDCバス電圧の制御が可能です。バック・ツー・バックFETが内蔵されており、双方向の電流制御を行うため、このデバイスは電力多重化や、複数の電源を持つシステムに適しています。

負荷、ソース、デバイス保護が組み込まれており、多くの機能をプログラム可能です。低電圧、過電圧、過電流、dV_o/dtランプ・レート、パワー・グッド、突入電流保護のスレッショルドはすべて、システム固有の要件に合わせてプログラム可能です。システム・ステータスの監視や下流負荷の制御のため、PGOOD、$\overline{FLT}$、および高精度の電流監視出力を備えています。

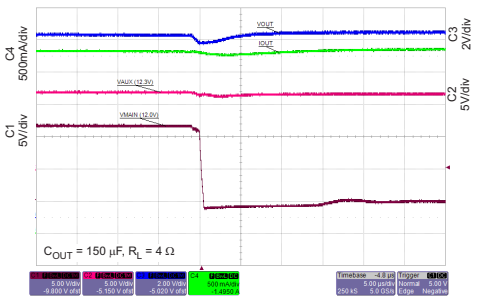
TPS25942、TPS25944デバイスは$V_{(IN)}$および$V_{(OUT)}$を監視し、$V_{(IN)} < (V_{(OUT)} – 10mV)$のときに真の逆電圧ブロックを行います。デバイスは、$\overline{FLT}$およびDMODEピンを使用して、メイン/補助電源の優先度を割り当てるように構成できます。

製品情報(1)

部品番号(2)	パッケージ	本体サイズ(公称)
TPS25942L	WQFN (20)	3.00mm×4.00mm
TPS25942A		
TPS25944L		
TPS25944A		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) TPS2594xL = ラッチ付き、TPS2594xA = 自動リトライ

$V_{(MAIN)}$ = 12Vから$V_{(AUX)}$ = 12.3Vへのフェイルオーバ ダイオード・モード制御を使用



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4 改訂履歴

Revision C (January 2017) から Revision D に変更 **Page**

- 「*Feature Description*」に、セクション9.3.5「逆電流保護」を 追加 ... 1

Revision B (October 2017) から Revision C に変更 **Page**

- Changed internal ramp rate of 12 V/ms for output to 30 V/ms in the *Hot Plug-In and In-Rush Current Control* section ... 23

Revision A (March 2015) から Revision B に変更 **Page**

- Changed Figure 49: Added Logic Inversion ... 21

2014年6月発行のものから更新 **Page**

- *特長*「UL 2367認定待ち」から「UL 2367認定済み、R_{ILIM} ≥ 20kΩ (最大4.81A)、ファイル番号169910」に変更 ... 1
- *概要*のテキストを「FLTおよびENBLKピン」から、「FLTおよびDMODEピン」に変更 ... 1
- 「*製品情報*」表から「製品プレビュー」の注記を削除 ... 1
- Changed Pin 1 From ENBLK To: DMODE throughout the data sheet ... 4
- Changed ENBLK To: DMODE in the *Pin Functions* table and updated the DESCRIPTION ... 4
- Moved the Storage Temperature From the *Handling Ratings* table To *Absolute Maximum Ratings* table ... 6
- Changed the *Handling Ratings* table To: *ESD Ratings* table ... 6
- Changed DIODE MODE INPUT (ENBLK): ACTIVE LOW To: DIODE MODE INPUT (DMODE): ACTIVE HIGH in the *Electrical Characteristics* ... 7
- Added Test Condition to $I_{(LIM)}$: "$R_{(ILIM)}$ = 20 kΩ" in the *Electrical Characteristics* ... 8
- Changed Test Condition in $I_{(LIM)}$ From: "ENBLK = High; Diode Mode" To: "DMODE = High; Non-ideal Diode Mode" in the *Electrical Characteristics* ... 8

- Changed "DIODE MODE INPUT: ACTIVE LOW ($\overline{\text{ENBLK}}$)" To: DIODE MODE INPUT: ACTIVE HIGH (DMODE)" in the *Timing Requirements* 9
- Changed Figure 22. 12
- Added condition $R_{(ILIM)}$ = 17.8 KΩ to Figure 39 and Figure 40 15
- Changed Figure 43. Added Figure 44, Figure 45, and Figure 46 16
- Changed Figure 48: $\overline{\text{ENBLK}}$ To: DMODE and Diode Mode To: Non-Ideal Diode Mode 20
- Changed Figure 49: $\overline{\text{ENBLK}}$ To: DMODE and Diode Mode To Non-Ideal Diode Mode 21
- Changed Equation 6 to include $I_{(IMON\_OS)}$ 25
- Change text in *Diode Mode* From:" $\overline{\text{ENBLK}}$...active low terminal" To: "DMODE ...active high terminal" 26
- Changed text in the last sentence of *Diode Mode* From: "In this mode, the overload current..." To:"In this mode, the circuit breaker functionality.." 26
- Added the NOTE to *Application and Implementation* 29
- Added Note A to Figure 60 33
- Changed Equation 37 From: $V_{(IN)}$ x $I_{(LOAD)}$ To: $V_{(IN)}$ + $I_{(LOAD)}$ 44

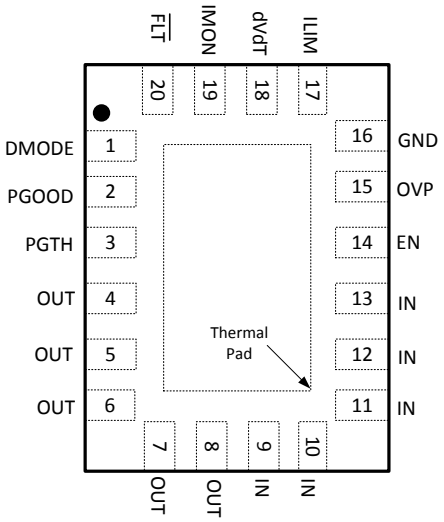
5 Device Comparison Table

DEVICE	T_J	OPERATION(1)	TYPE
TPS25942A	–40°C to +125°C	Current limiter	Auto retry
TPS25942L		Current limiter	Latched
TPS25944A		Circuit breaker	Auto retry
TPS25944L		Circuit breaker	Latched

(1) See the *Operational Differences Between the TPS25942 and TPS25944* section for detailed information.

6 Pin Configuration and Functions

RVC Package
20-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DMODE	I	Diode Mode control pin. A high at this pin activates the non-ideal diode mode
2	PGOOD	O	Active High. A high indicates PGTH has crossed the threshold value. It is an open drain output
3	PGTH	I	Positive input of PGOOD comparator
4	OUT	O	Power output of the device
5			
6			
7			
8			
9	IN	I	Power input and supply voltage
10			
11			
12			
13			
14	EN/UVLO	I	Input for setting programmable undervoltage lockout threshold. An undervoltage event opens internal FET and assert $\overline{FLT}$ to indicate power-failure. When pulled to GND, resets the fault latch in TPS25942L, TPS25944L
15	OVP	I	Input for setting programmable overvoltage protection threshold. An overvoltage event opens the internal FET and assert $\overline{FLT}$ to indicate overvoltage
16	GND	—	Ground

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
17	ILIM	I/O	A resistor from this pin to GND sets the overload and short-circuit current limit
18	dVdT	I/O	A capacitor from this pin to GND sets the ramp rate of output voltage
19	IMON	O	This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage, used as analog current monitor
20	$\overline{\text{FLT}}$	O	Fault event indicator, goes low to indicate fault condition due to undervoltage, pvervoltage, reverse voltage, circuit breaker timeout (TPS25944 only) and thermal shutdown events. It is an open drain output
—	PowerPAD™	—	The GND terminal must be connected to the exposed PowerPAD. This PowerPAD must be connected to a PCB ground plane using multiple vias for good thermal performance

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Input voltage	IN, OUT, PGTH, PGOOD, EN, OVP, DMODE, $\overline{FLT}$	–0.3	20	V
		IN (10-ms transient)		22	
		dVdT, ILIM	–0.3	3.6	
		IMON	–0.3	7	
	Sink current	PGOOD, $\overline{FLT}$, dVdT		10	mA
	Source current	dVdT, ILIM, IMON	Internally Limited		
	Continuous power dissipation		See the *Thermal Information*		
T_J	Maximum junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001s (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Input voltage	IN	2.7		18	V
		EN, OVP, DMODE, OUT, PGTH, PGOOD, $\overline{FLT}$	0		18	
		dVdT, ILIM	0		3	
		IMON	0		6	
	Resistance	ILIM	16.9		150	kΩ
		IMON	1			
	External capacitance	OUT	0.1			µF
		dVdT			470	nF
T_J	Operating junction temperature		–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS25942 TPS25944 RVC (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	40.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC[1]		TPS25942 TPS25944 RVC (WQFN) 20 PINS	UNIT
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

7.5 Electrical Characteristics

Conditions are –40°C ≤ T_J = T_A ≤ +125°C, 2.7 V ≤ $V_{(IN)}$ ≤ 18 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DMODE)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND INTERNAL UNDERVOLTAGE LOCKOUT						
$V_{(IN)}$	Operating input voltage		2.7		18	V
$V_{(UVR)}$	Internal UVLO threshold, rising		2.2	2.3	2.4	V
$V_{(UVRhys)}$	Internal UVLO hysteresis		105	116	125	mV
$I_{Q(ON)}$	Supply current, enabled	$V_{(EN/UVLO)}$ = 2 V, $V_{(IN)}$ = 3 V	140	210	300	µA
		$V_{(EN/UVLO)}$ = 2 V, $V_{(IN)}$ = 12 V	140	199	260	
		$V_{(EN/UVLO)}$ = 2 V, $V_{(IN)}$ = 18 V	140	202	270	
$I_{Q(OFF)}$	Supply current, disabled	$V_{(EN/UVLO)}$ = 0 V, $V_{(IN)}$ = 3 V	4	8.6	15	µA
		$V_{(EN/UVLO)}$ = 0 V, $V_{(IN)}$ = 12 V	6	15	20	
		$V_{(EN/UVLO)}$ = 0 V, $V_{(IN)}$ = 18 V	8	18.5	25	
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT						
$V_{(ENR)}$	EN/UVLO threshold voltage, rising		0.97	0.99	1.01	V
$V_{(ENF)}$	EN/UVLO threshold voltage, falling		0.9	0.92	0.94	V
$V_{(SHUTF)}$	EN threshold voltage for Low I_Q shutdown, falling		0.3	0.47	0.63	V
$V_{(SHUTFhys)}$	EN hysteresis for low I_Q shutdown, hysteresis[1]			66		mV
I_{EN}	EN input leakage current	0 V ≤ $V_{(EN/UVLO)}$ ≤ 18 V	–100	0	100	nA
OVER VOLTAGE PROTECTION (OVP) INPUT						
$V_{(OVPR)}$	Overvoltage threshold voltage, rising		0.97	0.99	1.01	V
$V_{(OVPF)}$	Overvoltage threshold voltage, falling		0.9	0.92	0.94	V
$I_{(OVP)}$	OVP input leakage current	0 V ≤ $V_{(OVP)}$ ≤ 5 V	–100	0	100	nA
DIODE MODE INPUT (DMODE)—ACTIVE HIGH						
$V_{(DMODE)}$	DMODE threshold voltage, rising		1.6	1.85	2	V
	DMODE threshold voltage, falling		0.8	0.96	1.1	V
$I_{(DMODE)}$	DMODE input leakage current	0.2 V ≤ $V_{(DMODE)}$ ≤ 18 V	0.6	1	1.25	µA
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT charging current	$V_{(dVdT)}$ = 0 V	0.85	1	1.15	µA
$R_{(dVdT)}$	dVdT discharging resistance	EN/UVLO = 0 V, $I_{(dVdT)}$ = 10 mA sinking		16	24	Ω
$V_{(dVdTmax)}$	dVdT maximum capacitor voltage		2.6	2.88	3.1	V
$GAIN_{(dVdT)}$	dVdT to OUT gain	$\Delta V_{(OUT)}/\Delta V_{(dVdT)}$	11.65	11.9	12.05	V/V
CURRENT LIMIT PROGRAMMING (I_{LIM})						
$V_{(ILIM)}$	ILIM bias voltage			0.87		V

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

Electrical Characteristics (continued)

Conditions are –40°C ≤ T_J = T_A ≤ +125°C, 2.7 V ≤ $V_{(IN)}$ ≤ 18 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DMODE)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(LIM)}$	Current limit $I_{(LIM)}$ for TPS25942 (2) $I_{(FAULT)}$ forTPS25944 (2)(3)	$R_{(ILIM)}$ = 150 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V	0.53	0.58	0.63	A
		$R_{(ILIM)}$ = 88.7 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V	0.9	0.99	1.07	
		$R_{(ILIM)}$ = 42.2 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V	1.92	2.08	2.25	
		$R_{(ILIM)}$ = 24.9 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V	3.25	3.53	3.81	
		$R_{(ILIM)}$ = 20 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V	4.09	4.45	4.81	
		$R_{(ILIM)}$ = 16.9 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V	4.78	5.2	5.62	
		$R_{(ILIM)}$ = OPEN, open resistor current limit (single point failure test: UL60950)	0.35	0.45	0.55	
		$R_{(ILIM)}$ = SHORT, shorted resistor current limit (single point failure test: UL60950)	0.55	0.67	0.8	
		DMODE = High; Non-ideal diode mode (1)		0.5 × $I_{(LIM)}$		
$I_{(OS)}$	Short-circuit current limit	$R_{(ILIM)}$ = 42.2 kΩ, $V_{(VIN)}$ = 12 V, ($V_{(IN)}$ – $V_{(OUT)}$) = 5 V	1.91	2.07	2.24	A
		$R_{(ILIM)}$ = 24.9 kΩ, $V_{(VIN)}$ = 12 V, ($V_{(IN)}$ – $V_{(OUT)}$) = 5 V	3.21	3.49	3.77	
		$R_{(ILIM)}$ = 16.9 kΩ, $V_{(VIN)}$ = 12 V, ($V_{(IN)}$ – $V_{(OUT)}$) = 5 V, –40°C ≤ T_J ≤ +85°C	4.7	5.11	5.52	
$I_{(FASTRIP)}$	Fast-trip comparator threshold (1)(2)			1.5 × $I_{(LIM)}$ + 0.375		A
CURRENT MONITOR OUTPUT (IMON)						
$GAIN_{(IMON)}$	Gain factor $I_{(IMON)}$:$I_{(OUT)}$	1 A ≤ $I_{(OUT)}$ ≤ 5 A	47.78	52.3	57.23	µA/A
MOSFET—POWER SWITCH						
R_{ON}	IN to OUT - ON resistance	1 A ≤ $I_{(OUT)}$ ≤ 5 A, T_J = 25°C	34	42	49	mΩ
		1 A ≤ $I_{(OUT)}$ ≤ 5 A, –40°C ≤ T_J ≤ +85°C	26	42	58	
		1 A ≤ $I_{(OUT)}$ ≤ 5 A, –40°C ≤ T_J ≤ +125°C	26	42	64	
PASS FET OUTPUT (OUT)						
$I_{lkg(OUT)}$	OUT leakage current in off state	$V_{(IN)}$ = 18 V, $V_{(EN/UVLO)}$ = 0 V, $V_{(OUT)}$ = 0 V (sourcing)	–2	0	2	µA
		$V_{(IN)}$ = 2.7 V, $V_{(EN/UVLO)}$ = 0 V, $V_{(OUT)}$ = 18 V (sinking)	6	13	20	
$V_{(REVTH)}$	$V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, falling		–15	–9.3	–3	mV
$V_{(FWDTH)}$	$V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, rising		86	100	114	mV
FAULT FLAG ($\overline{FLT}$)—ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ internal pull-down resistance	$V_{(OVP)}$ = 2 V, $I_{(\overline{FLT})}$ = 5 mA sinking	10	18	30	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 18 V	–1	0	1	µA
POSITIVE INPUT for POWER-GOOD COMPARATOR (PGTH)						
$V_{(PGTHR)}$	PGTH threshold voltage, rising		0.97	0.99	1.01	V
$V_{(PGTHF)}$	PGTH threshold voltage, falling		0.9	0.92	0.94	V
$I_{(PGTH)}$	PGTH input leakage current	0 V ≤ $V_{(PGTH)}$ ≤ 18 V	–100	0	100	nA
POWER-GOOD COMPARATOR OUTPUT (PGOOD): ACTIVE HIGH						
$R_{(PGOOD)}$	PGOOD internal pull-down resistance	$V_{(PGTH)}$ = 0V, $I_{(PGOOD)}$ = 5 mA sinking	10	20	35	Ω
$I_{(PGOOD)}$	PGOOD input leakage current	0 V ≤ $V_{(PGOOD)}$ ≤ 18 V	–1	0	1	µA
THERMAL SHUT DOWN (TSD)						
$T_{(TSD)}$	TSD threshold (1)			160		°C
$T_{(TSDhys)}$	TSD hysteresis (1)			12		°C
	Thermal fault: (latched or auto-retry)	TPS25942L, TPS25944L		Latched		
		TPS25942A, TPS25944A		Auto-retry		

(2) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(3) The TPS25942 limits current to the programmed $I_{(LIM)}$ level. TPS25944 does not limit current but runs the fault timer when $I_{(LOAD)}$ > $I_{(LIM)}$.

7.6 Timing Requirements

Conditions are –40°C ≤ T_J = T_A ≤ +125°C, 2.7 V ≤ $V_{(IN)}$ ≤ 18 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DMODE)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted). See Figure 47 for timing diagrams.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE AND UVLO INPUT						
$t_{ON(dly)}$	EN turnon delay	EN/UVLO ↑ (100 mV above $V_{(ENR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ < 0.8 nF		220		µs
		EN/UVLO ↑ (100 mV above $V_{(ENR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ ≥ 0.8 nF, see , [$C_{(dVdT)}$ in nF]		100 + 150 × $C_{(dVdT)}$		µs
$t_{OFF(dly)}$	EN turnoff delay	EN/UVLO ↓ (100 mV below $V_{(ENF)}$) to $\overline{FLT}$↓		2		µs
OVERVOLTAGE PROTECTION INPUT (OVP)						
$t_{OVP(dly)}$	OVP disable delay	OVP↑ (100 mV above $V_{(OVPR)}$) to $\overline{FLT}$↓		2		µs
DIODE MODE INPUT: ACTIVE HIGH (DMODE)						
t_{DMODE}	DMODE turnon delay	DMODE↓ to ($V_{(IN)}$ – $V_{(OUT)}$) ≤ 200 mV, with 1 A resistive load at OUT		2		µs
	DMODE turnoff delay	DMODE↑ to ($V_{(IN)}$ – $V_{(OUT)}$) > 200 mV, 1 A resistive load at OUT		220		ns
OUTPUT RAMP CONTROL (dVdT)						
t_{dVdT}	Output ramp time	EN/UVLO ↑ to $V_{(OUT)}$ = 4.5 V, with $C_{(dVdT)}$ = open		0.12		ms
		EN/UVLO ↑ to $V_{(OUT)}$ = 11 V, with $C_{(dVdT)}$ = open	0.25	0.37	0.5	ms
		EN/UVLO↑ to $V_{(OUT)}$ = 11 V, with $C_{(dVdT)}$ = 1 nF		0.97		ms
CURRENT LIMIT						
$t_{FASTRIP(dly)}$	Fast-trip comparator delay	$I_{(OUT)}$ > $I_{(FASTRIP)}$		200		ns
REVERSE PROTECTION COMPARATOR						
$t_{REV(dly)}$	Reverse protection comparator delay	($V_{(IN)}$ – $V_{(OUT)}$)↓ (1 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$↓		10		µs
		($V_{(IN)}$ – $V_{(OUT)}$)↓ (10 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$↓		1		µs
$t_{FWD(dly)}$		($V_{(IN)}$ – $V_{(OUT)}$)↑ (10 mV overdrive above $V_{(FWDTH)}$) to $\overline{FLT}$↑		3.1		µs
POWER-GOOD COMPARATOR OUTPUT (PGOOD): ACTIVE HIGH						
t_{PGOODR}	PGOOD delay (de-glitch) time	TPS25942: rising edge	0.42	0.54	0.66	ms
		TPS25944: rising edge		4		ms
t_{PGOODF}		TPS25942 and TPS25944: falling edge		10		µs
FAULT FLAG ($\overline{FLT}$)						
$t_{CB(dly)}$	$\overline{FLT}$ assertion delay in circuit breaker mode	TPS25944 only; delay from $I_{(OUT)}$ > $I_{(LIM)}$ to $\overline{FLT}$↓ (and internal FET turned off)		4		ms
$t_{CB(Retrydly)}$	Retry delay in circuit breaker mode	TPS25944A only; circuit breaker fault asserted, delay from to $\overline{FLT}$↓ to $\overline{FLT}$↑ edge		128		ms
THERMAL SHUT DOWN (TSD)						
	Retry delay in TSD	TPS25942A and TPS25944A only		128		ms

7.7 Typical Characteristics

Conditions are –40°C ≤ T_J = T_A ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DMODE)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

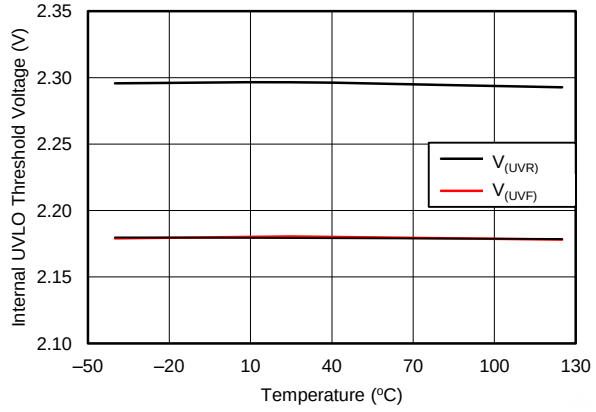


Figure 1. Internal UVLO Threshold Voltage vs Temperature

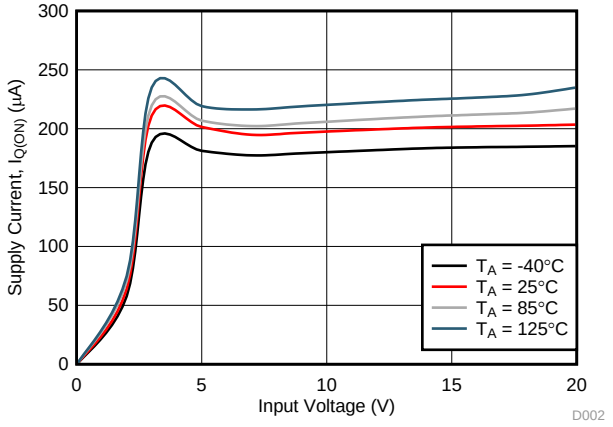


Figure 2. Input Supply Current vs Supply Voltage During Normal Operation

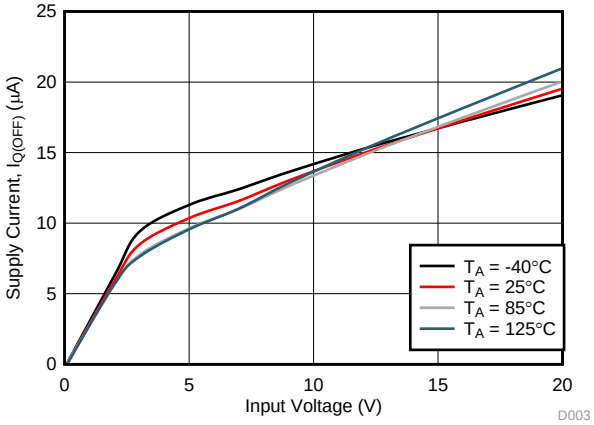


Figure 3. Input Supply Current vs Supply Voltage at Shutdown

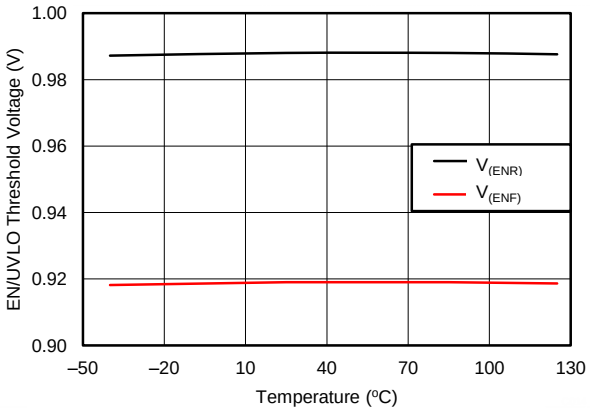


Figure 4. EN Threshold Voltage vs Temperature

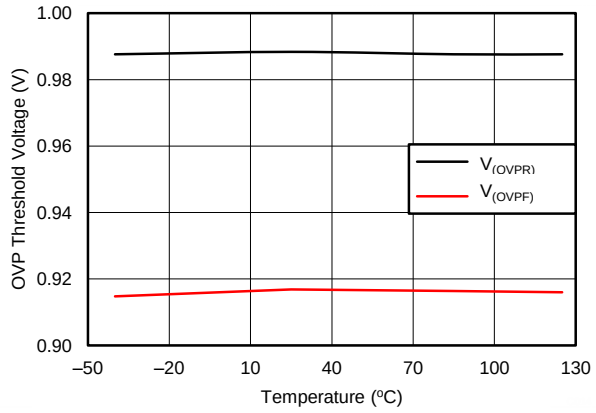


Figure 5. OVP Threshold Voltage vs Temperature

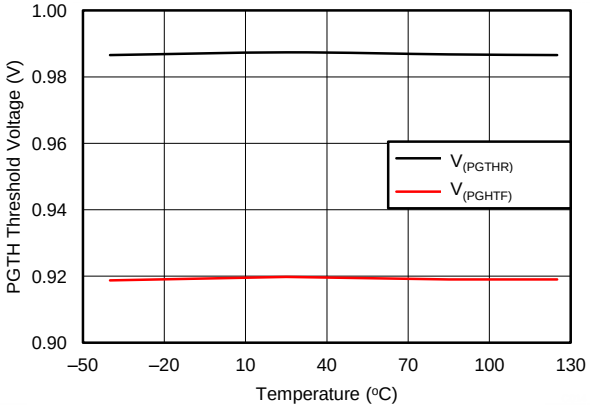


Figure 6. PGTH Threshold Voltage vs Temperature

Typical Characteristics (continued)

Conditions are –40°C ≤ T_J = T_A ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DMODE)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = FLT = IMON = OPEN. (unless stated otherwise)

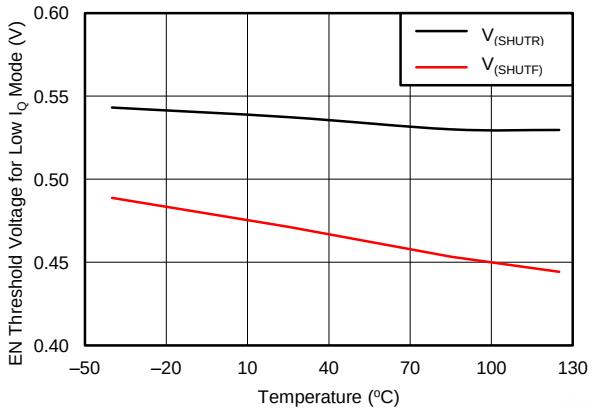


Figure 7. EN Threshold Voltage for Low IQ Mode vs Temperature

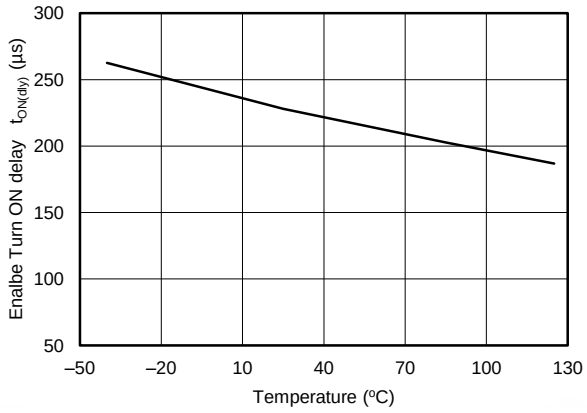


Figure 8. Enable Turnon Delay vs Temperature

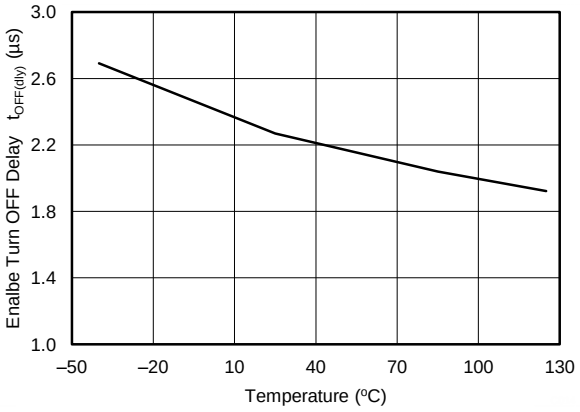


Figure 9. Enable Turnoff Delay vs Temperature

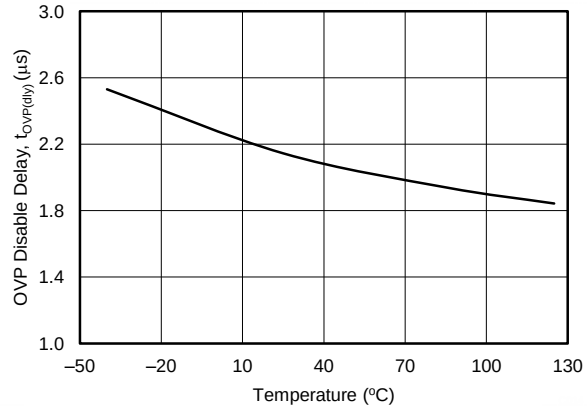


Figure 10. OVP Disable Delay vs Temperature

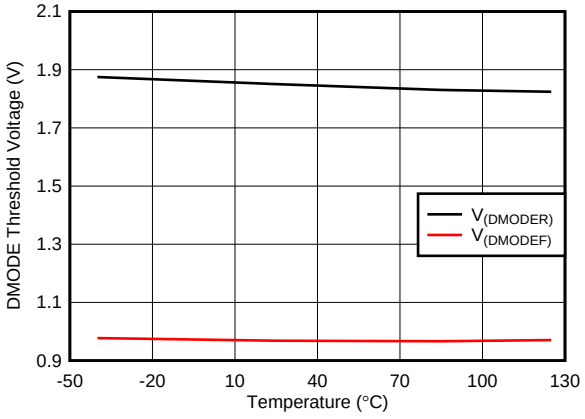


Figure 11. DMODE Threshold Voltage vs Temperature

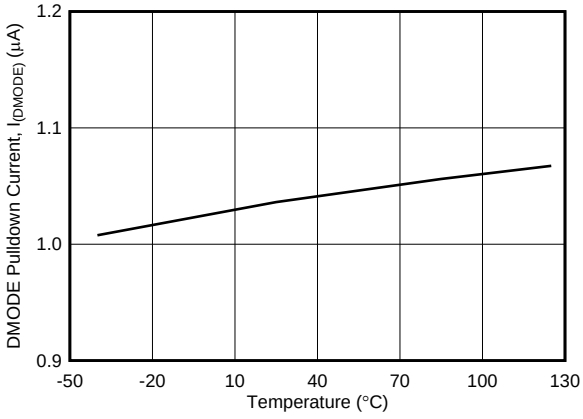


Figure 12. DMODE Pulldown Current vs Temperature

Typical Characteristics (continued)

Conditions are –40°C ≤ T_J = T_A ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DMODE)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

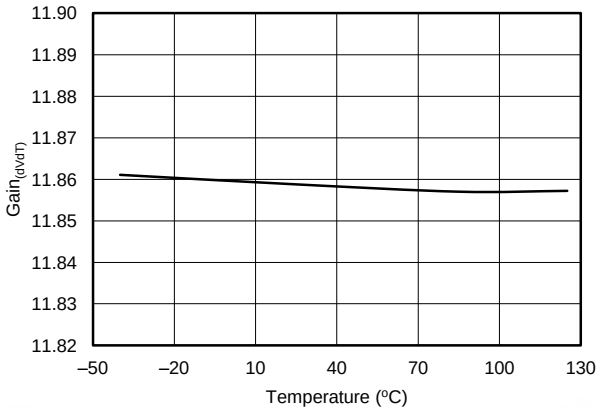


Figure 13. $GAIN_{(dVdT)}$ vs Temperature

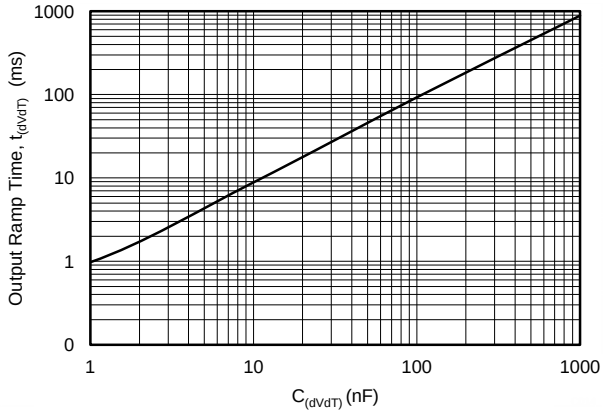


Figure 14. Output Ramp Time vs $C_{(dVdT)}$

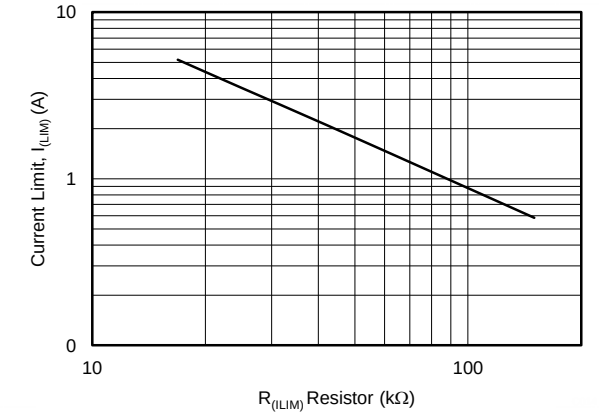


Figure 15. Current Limit vs Current Limit Resistor

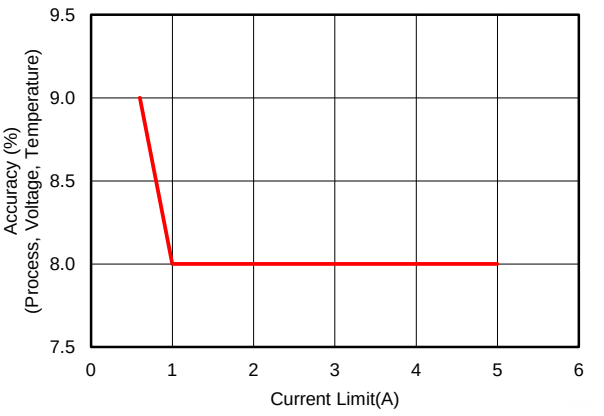


Figure 16. Current Limit Accuracy vs Current Limit

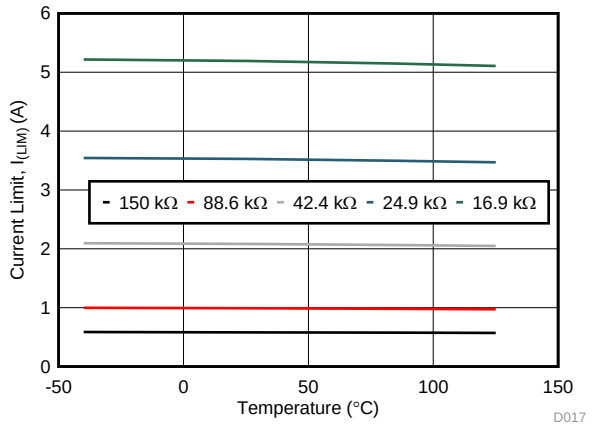


Figure 17. Current Limit vs Temperature Across $R_{(ILIM)}$

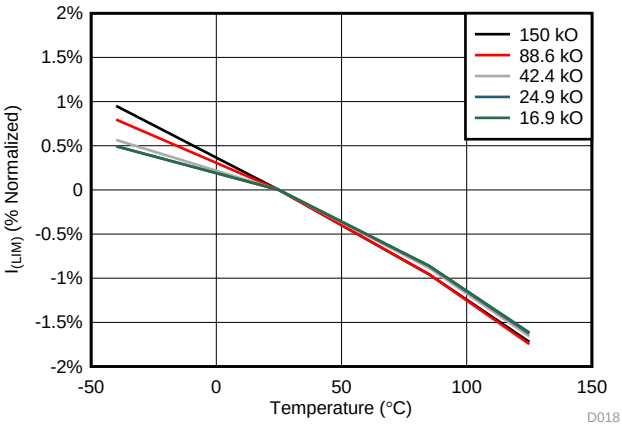
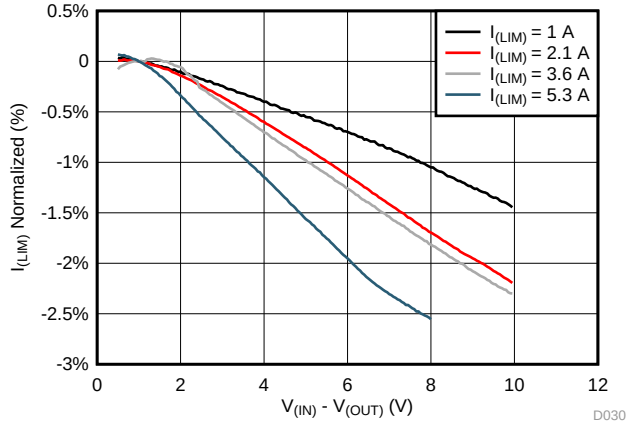


Figure 18. Current Limit (% Normalized) vs Temperature

Typical Characteristics (continued)

Conditions are –40°C ≤ T_J = T_A ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DMODE)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = FLT = IMON = OPEN. (unless stated otherwise)



For $I_{(LIM)}$ = 5.3 A, device goes into thermal shutdown for [$V_{(IN)}$ – $V_{(OUT)}$] > 8 V

Figure 19. Current Limit Normalized (%) vs $V_{(IN)}$ – $V_{(OUT)}$

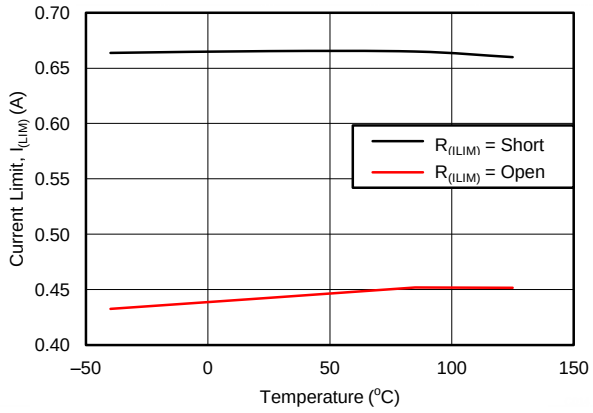


Figure 20. Current Limit for $R_{(ILIM)}$ = Open and Short vs Temperature

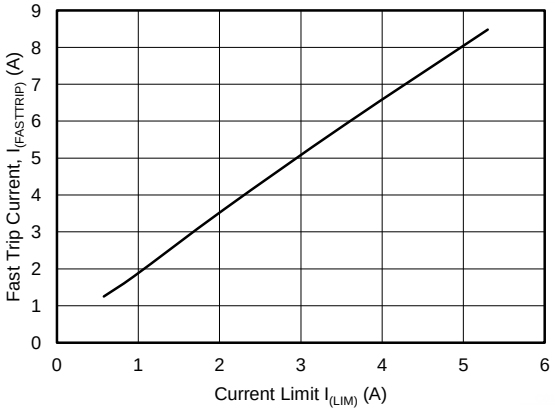


Figure 21. Fast Trip Threshold vs Current Limit

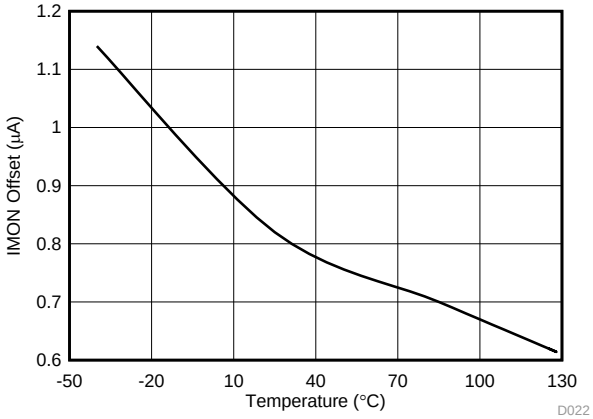


Figure 22. IMON Offset vs Temperature

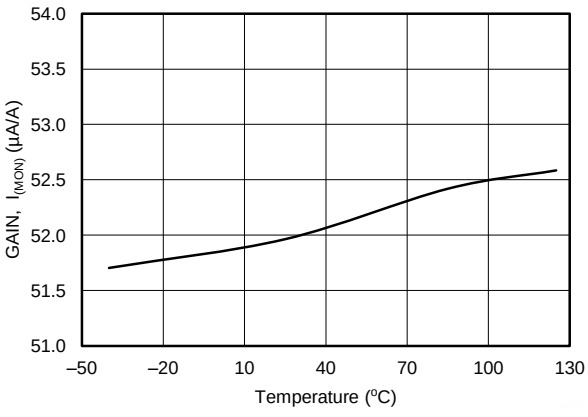


Figure 23. $GAIN_{(IMON)}$ vs Temperature

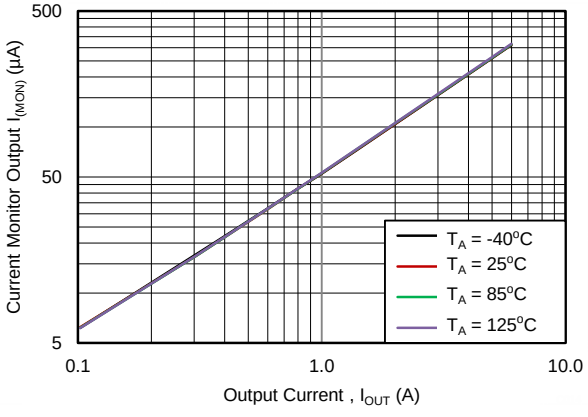


Figure 24. Current Monitor Output vs Output Current

Typical Characteristics (continued)

Conditions are –40°C ≤ T_J = T_A ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DMODE)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = FLT = IMON = OPEN. (unless stated otherwise)

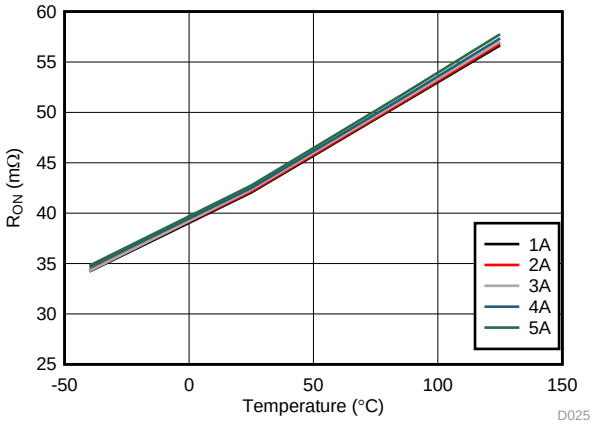


Figure 25. R_{ON} vs Temperature Across Load Current

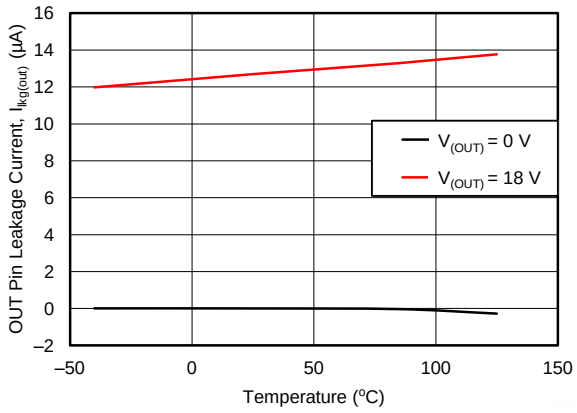


Figure 26. OUT Leakage Current in Off State vs Temperature

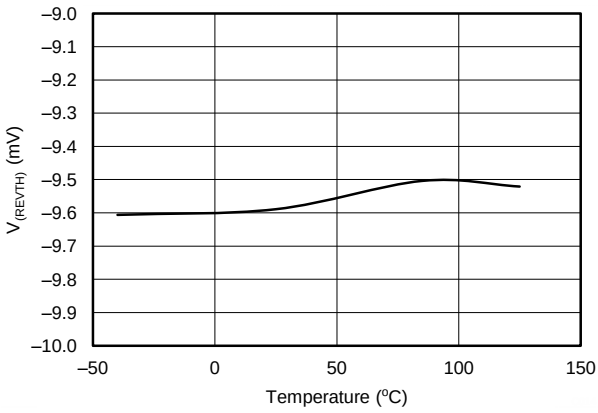


Figure 27. $V_{(REVTH)}$ vs Temperature

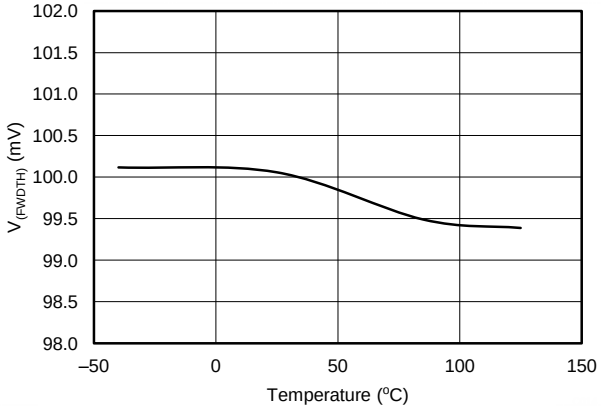


Figure 28. $V_{(FWDTH)}$ vs Temperature

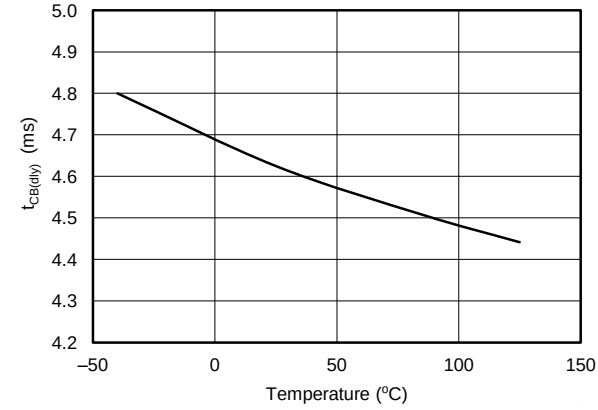
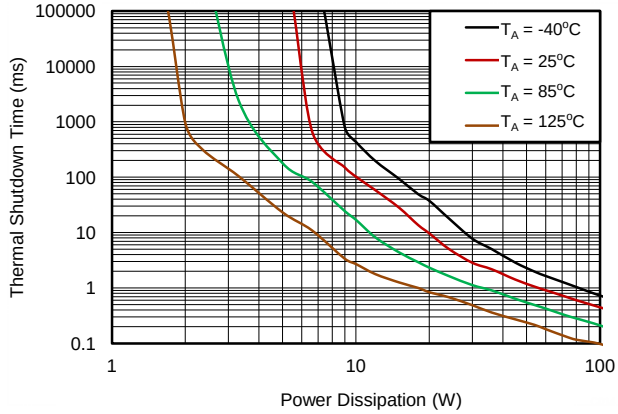


Figure 29. Circuit Breaker Timer Fault Assertion Delay vs Temperature

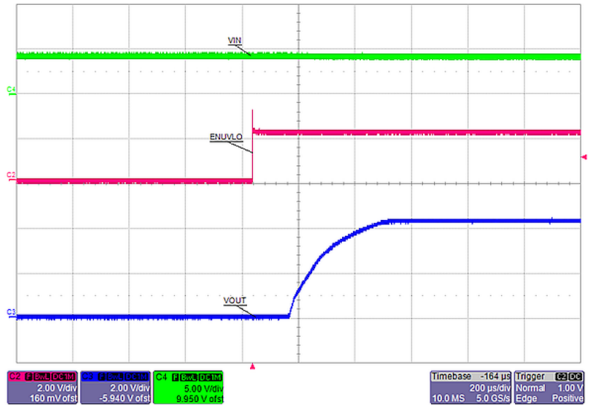


Taken on 2-Layer board, 2oz.(0.08-mm thick) with GND plane area: 14 cm^2 (Top) and 20 cm^2 (Bottom)

Figure 30. Thermal Shutdown Time vs Power Dissipation

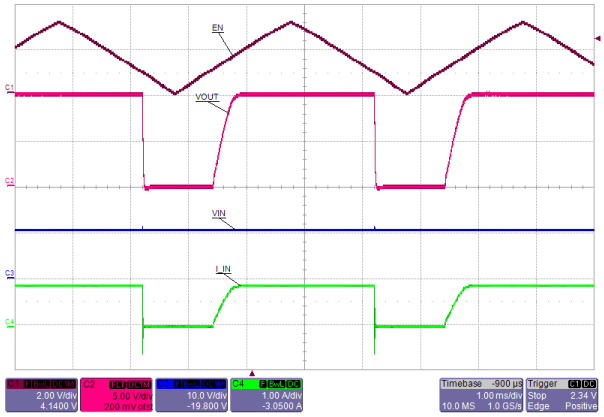
Typical Characteristics (continued)

Conditions are –40°C ≤ T_J = T_A ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DMODE)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)



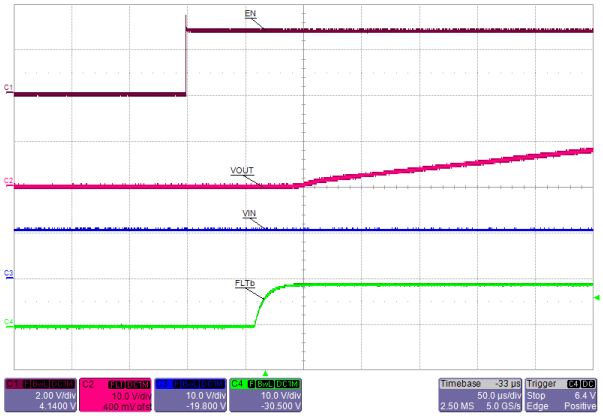
$V_{(IN)}$ = 4.5 V

Figure 31. Turnon With Enable



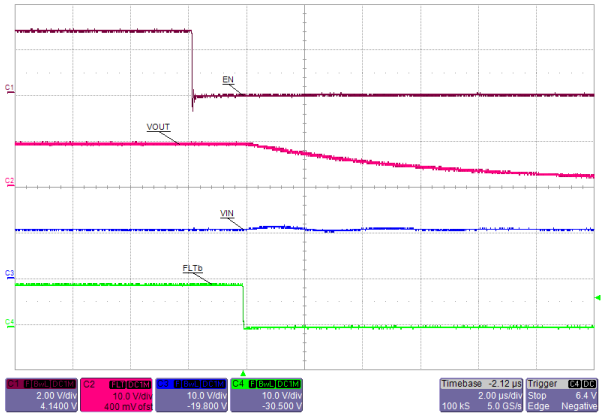
$V_{(IN)}$ = 11 V

Figure 32. Turnon and Turnoff With Enable



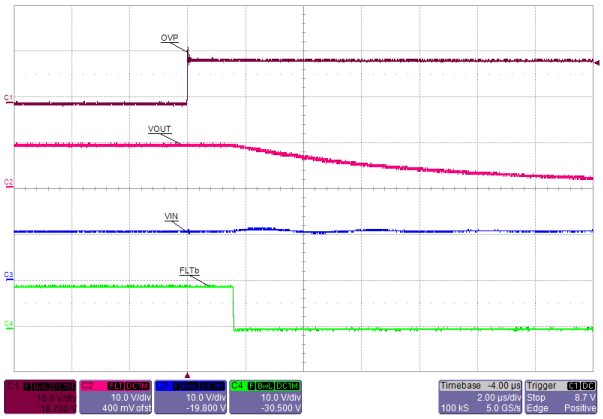
$R_{\overline{(FLT)}}$ = 100 kΩ

Figure 33. EN Turnon Delay : EN ↑ to Output Ramp ↑



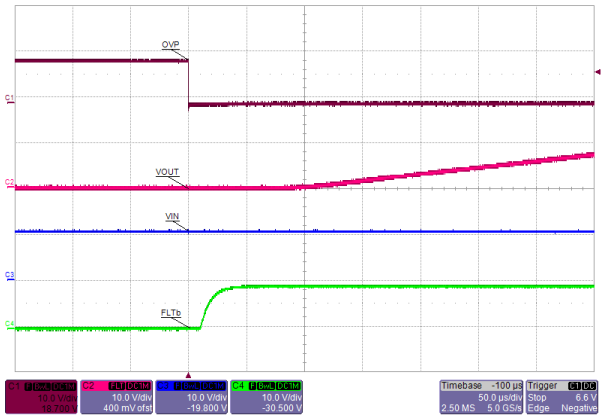
$R_{\overline{(FLT)}}$ = 100 kΩ

Figure 34. EN Turnoff Delay : EN ↓ to Fault ↓



$V_{(IN)}$ = 12 V R_L = 12 Ω $R_{\overline{(FLT)}}$ = 100 kΩ

Figure 35. OVP Turnoff Delay: OVP ↑ to Fault ↓

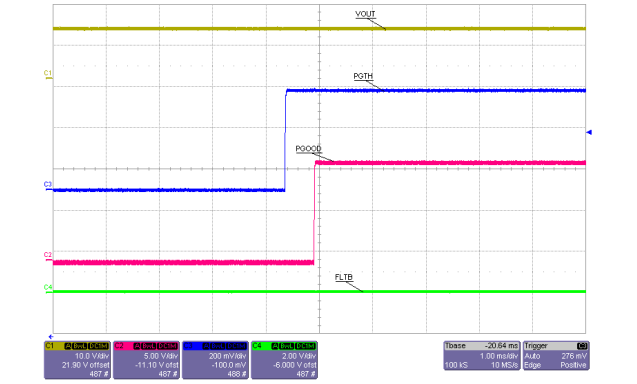


$V_{(IN)}$ = 12 V R_L = 12 Ω $R_{\overline{(FLT)}}$ = 100 kΩ

Figure 36. OVP Turnon Delay: OVP ↓ to Output Ramp ↑

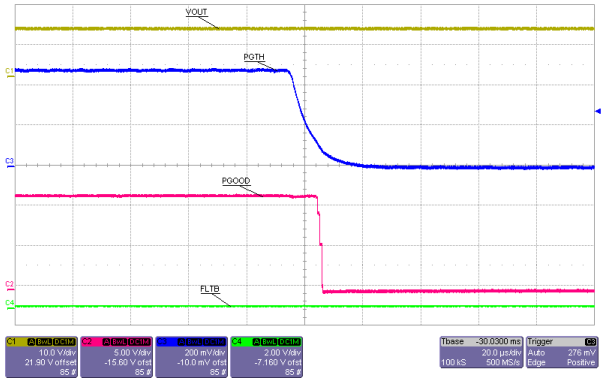
Typical Characteristics (continued)

Conditions are –40°C ≤ $T_J = T_A$ ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)} = V_{(DMODE)} = V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)



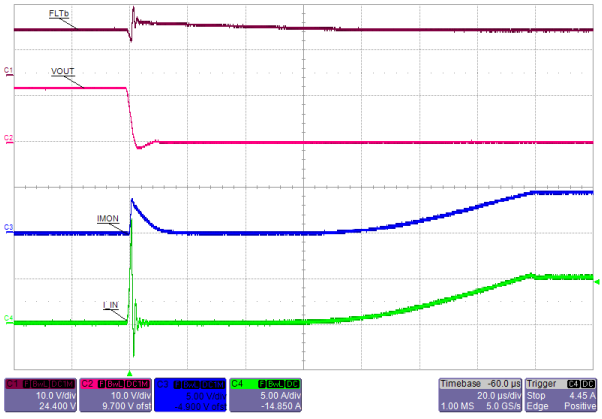
$V_{(IN)}$ = 12 V R_L = 12 Ω $R_{(\overline{FLT})}$ = 100 kΩ $R_{(PGOOD)}$ = 100 kΩ

Figure 37. Power Good Delay (Rising)



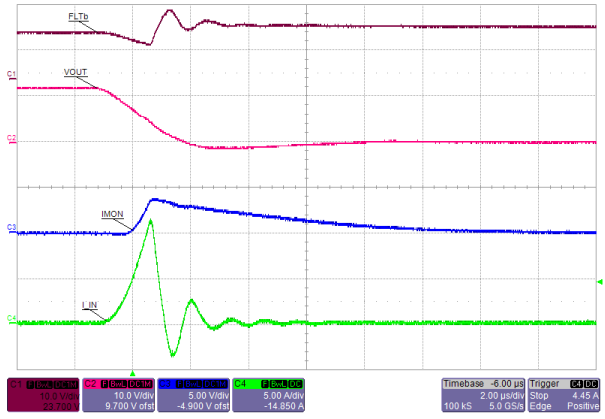
$V_{(IN)}$ = 12 V R_L = 12 Ω $R_{(\overline{FLT})}$ = 100 kΩ $R_{(PGOOD)}$ = 100 kΩ

Figure 38. Power Good Delay (Falling)



$V_{(IN)}$ = 12 V $R_{(IMON)}$ = 16.9 kΩ $R_{(\overline{FLT})}$ = 100 kΩ $R_{(ILIM)}$ = 17.8 KΩ

Figure 39. Hot-Short: Fast Trip Response and Current Regulation



$V_{(IN)}$ = 12 V $R_{(IMON)}$ = 16.9 kΩ $R_{(\overline{FLT})}$ = 100 kΩ $R_{(ILIM)}$ = 17.8 KΩ

Figure 40. Hot-Short: Fast Trip Response (Zoomed)

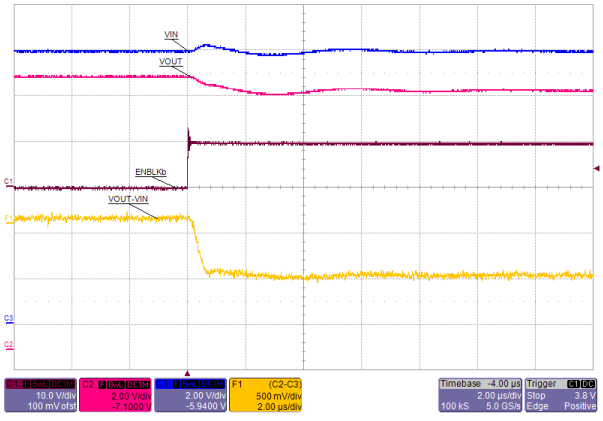


Figure 41. Transition from Normal Mode to Non-Ideal Diode Mode

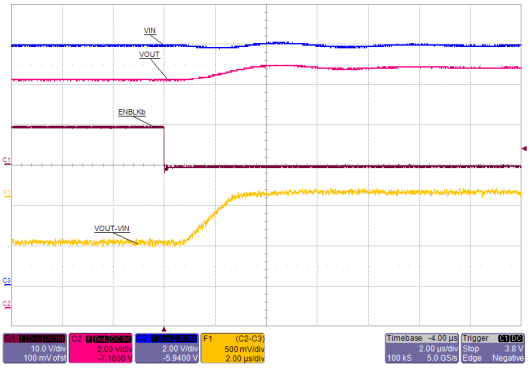
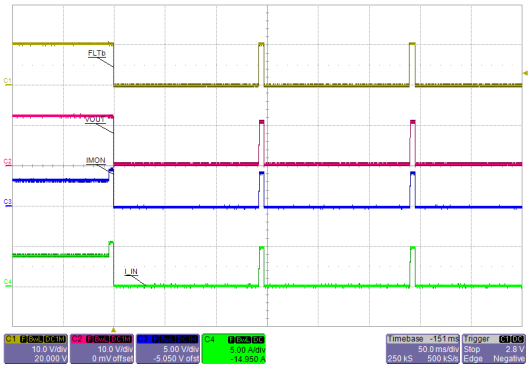


Figure 42. Transition from Non-Ideal Diode Mode to Normal Mode

Typical Characteristics (continued)

Conditions are –40°C ≤ $T_J = T_A$ ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)} = V_{(DMODE)} = V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)



$V_{(IN)}$ = 12 V R_L = 3 Ω to 2 Ω $R_{(IMON)}$ = 16.9 kΩ
$R_{(ILIM)}$ = 17.8 KΩ $R_{(\overline{FLT})}$ = 100 kΩ

Figure 43. Overload: TPS25944A Circuit Break Function

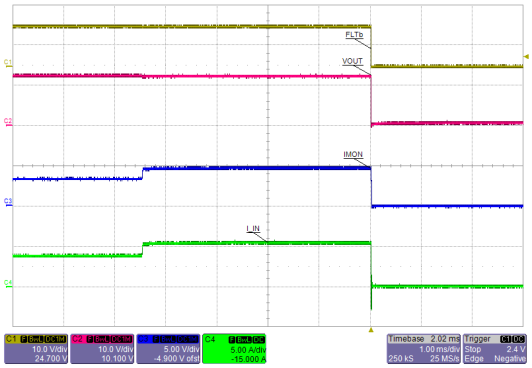
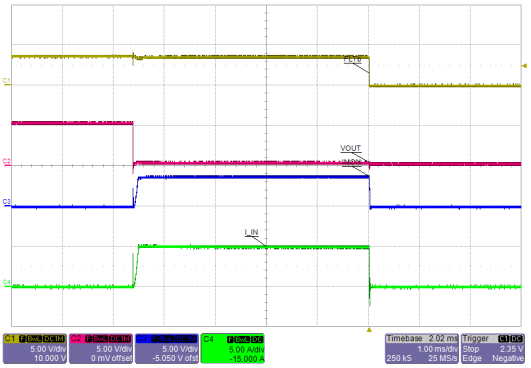
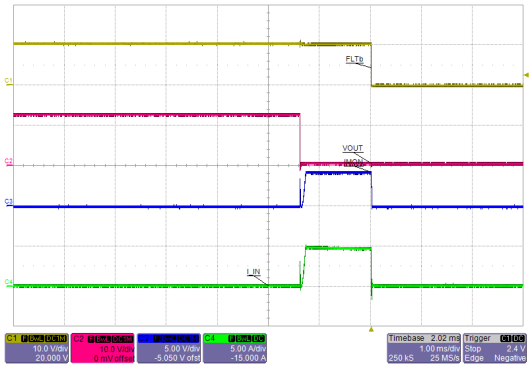


Figure 44. Overload: Zoomed In (First Cycle)



$V_{(IN)}$ = 5 V $R_{(IMON)}$ = 16.9 kΩ $R_{(\overline{FLT})}$ = 100 kΩ
$R_{(ILIM)}$ = 17.8 KΩ

Figure 45. Hot Short Response: TPS25944A Device Turns Off after the Fault Timer $t_{CB(dly)}$ (4 ms) Expires



$V_{(IN)}$ = 12 V $R_{(IMON)}$ = 16.9 kΩ $R_{(\overline{FLT})}$ = 100 kΩ
$R_{(ILIM)}$ = 17.8 KΩ

Figure 46. Hot Short Response: TPS25944A Device Turns Off When $T_J > T_{(TSD)}$ Before Timer Expires

8 Parameter Measurement Information

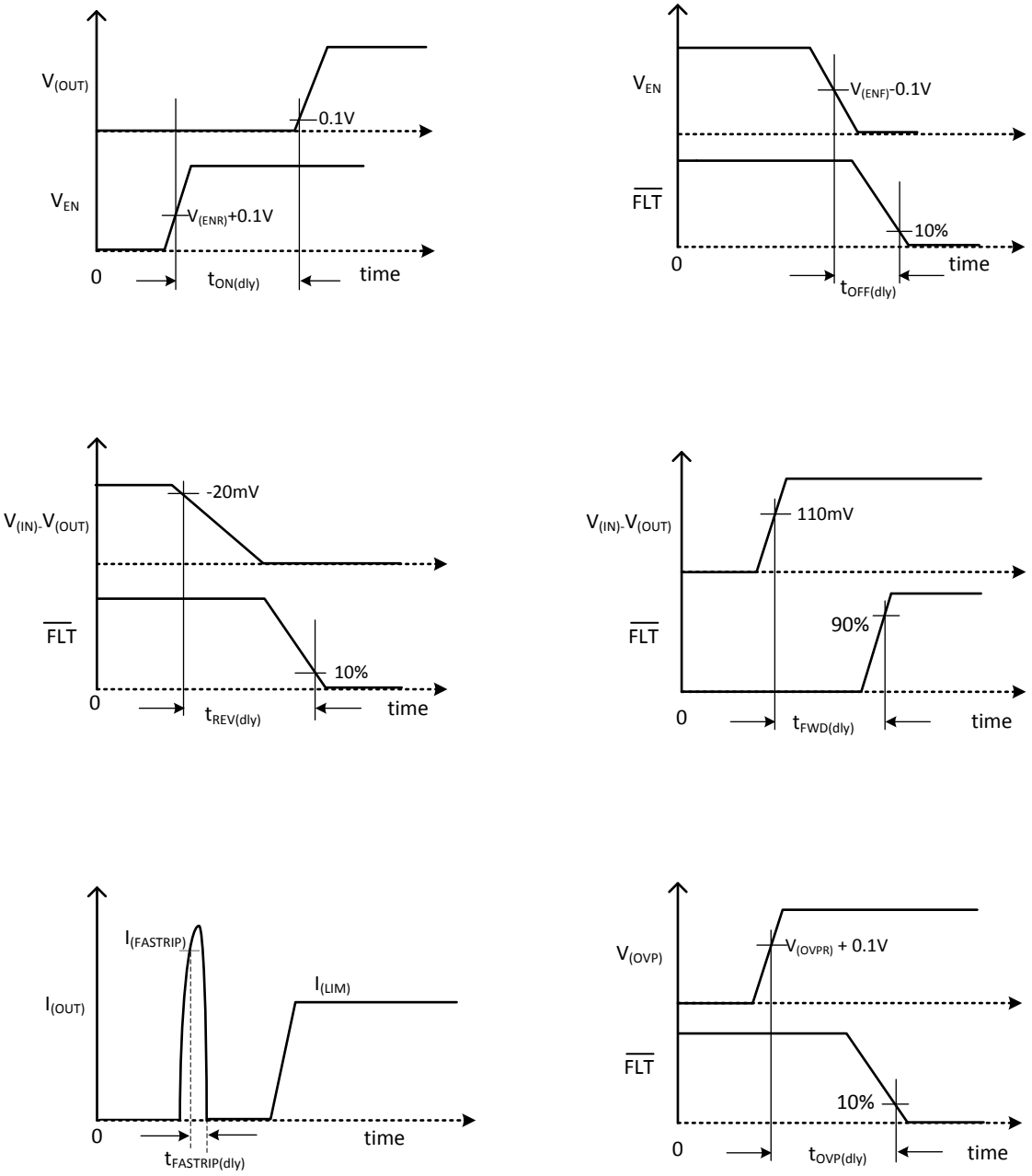


Figure 47. Timing Diagrams

9 Detailed Description

9.1 Overview

The TPS25942, TPS25944 is an eFuse Power Mux with integrated back-to-back FETs and enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 2.7 V to 18 V.

For hot-plug-in boards, the device provides hot-swap power management with in-rush current control and programmable output ramp-rate. The device integrates overcurrent and short circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply, while the fast response short circuit protection immediately isolates the load from input when a short circuit is detected. The device allows the user to program the overcurrent limit threshold between 0.6 A and 5.3 A via an external resistor.

The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault for downstream system. Its overall threshold accuracy of 2% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip. The TPS25942, TPS25944 is designed to control redundant power supply systems. The devices monitor $V_{(IN)}$ and $V_{(OUT)}$ to provide true reverse blocking from output when reverse condition or input power fail condition is detected. Also, a pair of the TPS25942 or TPS25944 devices can be configured to assign priority to the main power supply over the auxiliary power supply.

The additional features include:

- Precise current monitor output for health monitoring of the system
- Additional power good comparator with precision internal reference for output or any other rail voltage monitoring
- Electronic circuit breaker operation with overload timeout – TPS25944 only
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for brown-out and overvoltage faults
- A choice of latched or automatic restart mode

9.2 Functional Block Diagram

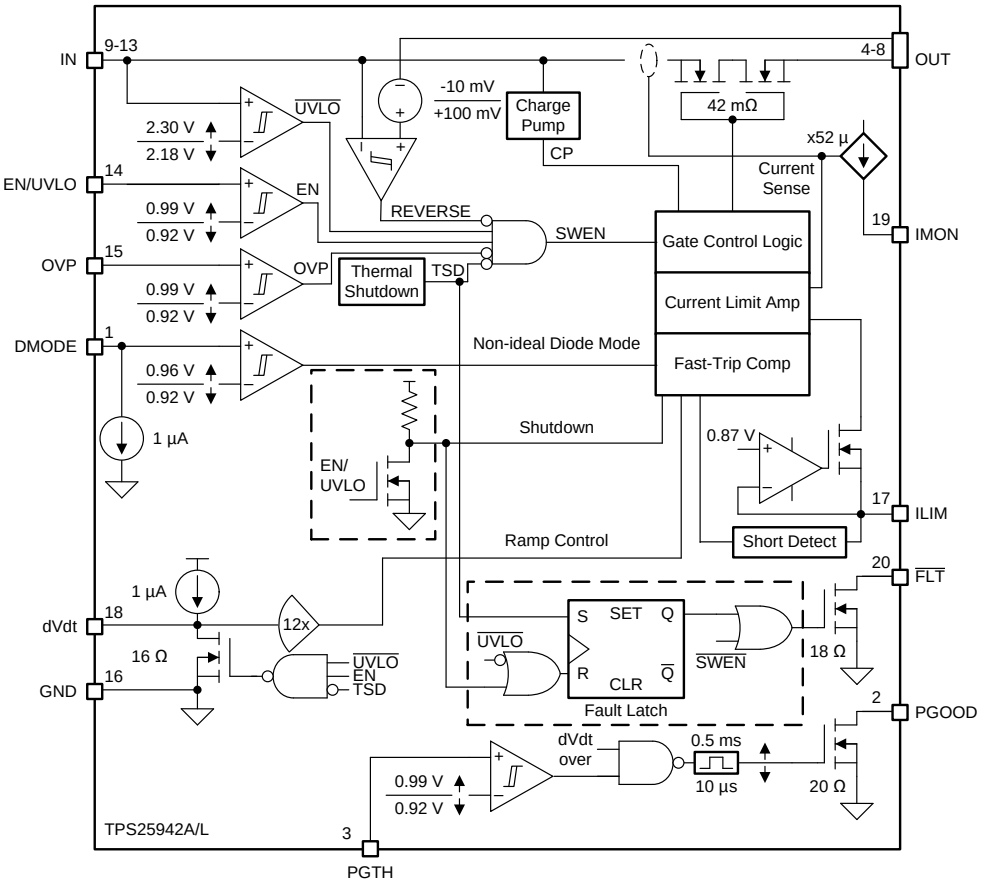


Figure 48. TPS25942A/L Block Diagram

Functional Block Diagram (continued)

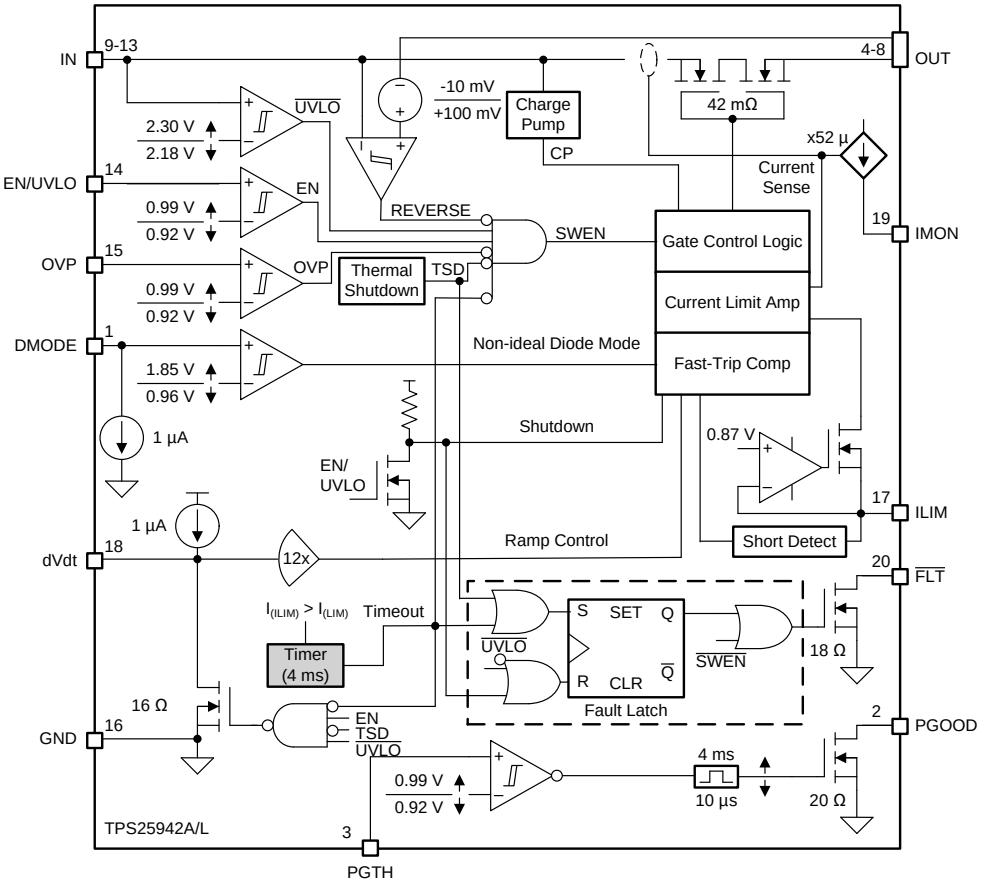


Figure 49. TPS25944A/L Block Diagram

9.3 Feature Description

9.3.1 Enable and Adjusting Undervoltage Lockout

The EN/UVLO pin controls the ON and OFF state of the internal FET. A voltage $V_{(EN/UVLO)} < V_{(ENF)}$ on this pin turns off the internal FET, thus disconnecting IN from OUT, while voltage below 0.6 V takes the device into shutdown mode, with I_Q less than 20 µA to ensure minimal power loss. Cycling EN/UVLO low and then back high resets the TPS2594xL that has latched off due to a fault condition.

The internal de-glitch delay on EN/UVLO falling edge is kept low for quick detection of power failure. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO terminal to GND.

The undervoltage lock out can be programmed by using an external resistor divider from supply IN terminal to EN/UVLO terminal to GND as shown in Figure 50. When an undervoltage or input power fail event is detected, the internal FET is quickly turned off, and $\overline{FLT}$ is asserted. If the Under-Voltage Lock-Out function is not needed, the EN/UVLO terminal must be connected to the IN terminal. EN/UVLO terminal must not be left floating.

The device also implements internal undervoltage-lockout (UVLO) circuitry on the IN terminal. The device disables when the IN terminal voltage falls below internal UVLO Threshold $V_{(UVF)}$. The internal UVLO threshold has a hysteresis of 115 mV.

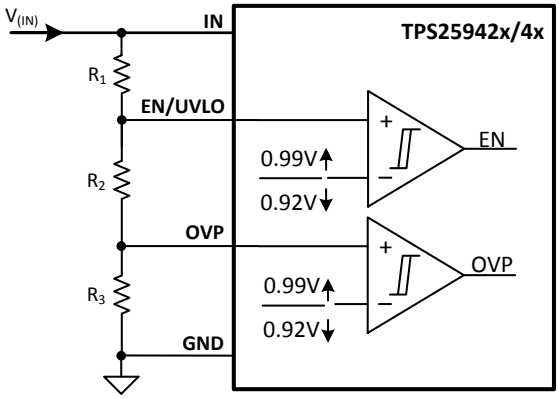


Figure 50. UVLO and OVP Thresholds Set By R_1, R_2 and R_3

9.3.2 Overvoltage Protection (OVP)

The device incorporates circuit to protect system during overvoltage conditions. A resistor divider connected from the supply to OVP terminal to GND (as shown in Figure 50) programs the overvoltage threshold. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. This pin must be tied to GND when not used.

9.3.3 Hot Plug-In and In-Rush Current Control

The device is designed to control the in-rush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. A slew rate controlled start-up (dVdT) also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on (as shown in Figure 51). Equation governing slew rate at start-up is shown in Equation 1.

Feature Description (continued)

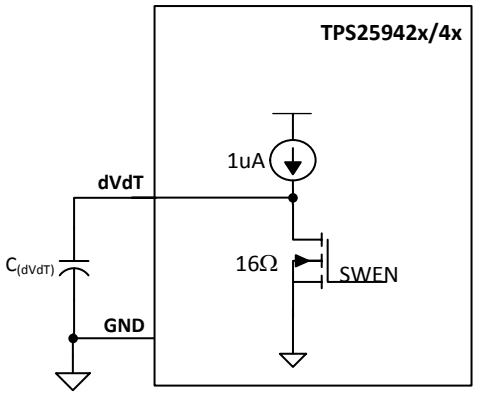


Figure 51. Output Ramp Up Time t_{dVdT} is Set by $C_{(dVdT)}$

$$I_{(dVdT)} = \left(\frac{C_{(dVdT)}}{GAIN_{(dVdT)}} \right) \times \left(\frac{dV_{(OUT)}}{dt} \right)$$

where

- $I_{(dVdT)}$ = 1 µA (typical)
- $\frac{dV_{(OUT)}}{dt}$ = Desired output slew rate
- $GAIN_{(dVdT)}$ = dVdT to OUT gain = 12 (1)

The total ramp time (t_{dVdT}) of $V_{(OUT)}$ for 0 to $V_{(IN)}$ can be calculated using Equation 2.

$$t_{dVdT} = 8.3 \times 10^4 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

The inrush current, $I_{(INRUSH)}$ can be calculated as shown in Equation 3.

$$I_{(INRUSH)} = C_{(OUT)} \times V_{(IN)} / t_{dVdT}. \quad (3)$$

The dVdT pin can be left floating to obtain a predetermined slew rate (t_{dVdT}) on the output. When terminal is left floating, the device sets an internal ramp rate of 30 V/ms for output ($V_{(OUT)}$) ramp.

Figure 61 and Figure 62 illustrate the inrush current control behavior of the TPS25942, TPS25944. For systems where load is present during start-up, the current never exceeds the overcurrent limit set by $R_{(ILIM)}$ resistor for the application. For defining appropriate charging time/rate under different load conditions, see the *Setting Output Voltage Ramp Time (t_{dVdT})* section.

9.3.4 Overload and Short Circuit Protection

The device monitors load current by sensing the voltage across the internal sense resistor. The FET current is monitored at both the start-up and during normal operation. During overload events, the device keeps the over current limited to the overcurrent limit ($I_{(LIM)}$) programmed by $R_{(ILIM)}$ resistor as shown in Equation 4.

$$I_{(LIM)} = \frac{89}{R_{(ILIM)}}$$

where

- $I_{(LIM)}$ is overload current limit in Ampere.
- $R_{(ILIM)}$ is the current limit resistor in kΩ (4)

The device incorporates two distinct levels: an overcurrent-limit ($I_{(LIM)}$) and a fast-trip threshold ($I_{(FASTRIP)}$). The illustration of fast trip and current limit operation is shown in Figure 52.

Since the bias current on ILIM pin directly controls the current-limiting behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.

Feature Description (continued)

9.3.4.1 Overload Protection

During overload conditions, the internal current-limit amplifier in the TPS25942 regulates the output current to $I_{(LIM)}$. The output voltage droops during current regulation, resulting in increased device power dissipation. If the device junction temperature reaches the thermal shutdown threshold ($T_{(TSD)}$), the internal FET is turned off. Once in thermal shutdown, The TPS25942L and 44L version stays latched off, whereas the TPS25942A and 44A commences an auto-retry cycle 128 ms after $T_J < [T_{(TSD)} – 12°C]$. During thermal shutdown, the fault pin $\overline{FLT}$ pulls low to signal a fault condition. Figure 65 and Figure 66 illustrate the behavior of the system for overload conditions in the TPS25942.

The TPS25944 allows the overload current to flow through the device until $I_{(LOAD)} < I_{(FASTRIP)}$. It starts the timer when $I_{(LIM)} < I_{(LOAD)} < I_{(FASTRIP)}$, and once the timer exceeds $t_{CB(dly)}$, the internal FET is turned off and $\overline{FLT}$ is asserted.

9.3.4.2 Short Circuit Protection

During a transient short circuit event, the current through the device increases very rapidly. As current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator, with a threshold $I_{(FASTRIP)}$. This comparator shuts down the pass device within 1 µs, when the current through internal FET exceeds $I_{(FASTRIP)}$ ($I_{(OUT)} > I_{(FASTRIP)}$), and terminates the rapid short-circuit peak current. The trip threshold is set to more than 50% of the programmed overload current limit ($I_{(FASTRIP)} = 1.5 \times I_{(LIM)} + 0.375$). The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(LIM)}$. Then, device behaves similar to overload condition. Figure 67 through Figure 69 illustrate the behavior of the system when the current exceeds the fast-trip threshold.

9.3.4.3 Start-Up With Short on Output

During start-up with short, the device limits the current to $I_{(LIM)}$ and behaves similar to the overload condition afterwards. Figure 70 and Figure 71 illustrate the behavior of the device for start-up with short on the output. This feature helps in quick isolation of the fault and hence ensures stability of the DC bus.

9.3.4.4 Constant Current Limit Behavior During Overcurrent Faults

If during current limit, power dissipation of the internal FET $P_D = [(V_{(IN)} – V_{(OUT)}) \times I_{(OUT)}]$ exceeds 10 W, there is an approximately 0% to 5% thermal fold back in the current limit value so that $I_{(LIM)}$ drops to I_{OS}. Eventually, the device shuts down due to over temperature.

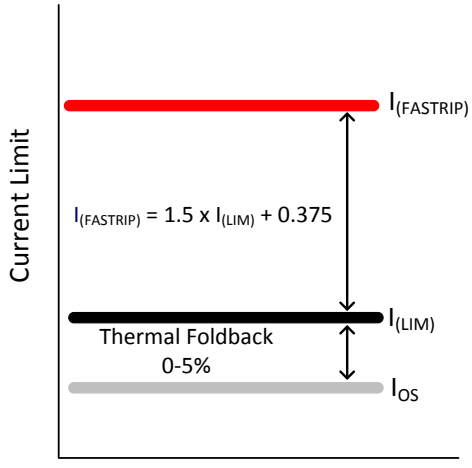


Figure 52. Fast-Trip Current

Feature Description (continued)

9.3.5 Reverse Current Protection

A fast reverse comparator controls the internal FET and turns off the FET whenever the output voltage $V_{(OUT)}$ exceeds the input voltage $V_{(IN)}$ by 10 mV (typical) for 1 µs (typical). This prevents damage to the devices on the input side of the TPS2594xx by preventing significant current from sinking into the input side. However, a reverse current of ($V_{(OUT)}$ - $V_{(IN)}$)/ R_{ON}) should flow from the output to the input to establish reverse voltage $V_{(REVTH)}$ of –10 mV across the device. The typical value of reverse current, needed for reverse voltage detection is –10 mV/ 42 mΩ = –238 mA

In power muxing applications, the reverse current magnitude $I_{(REV)}$ depends on the slew-rate of the output voltage $V_{(OUT)}$ and the system input capacitance C_{IN} as shown in Equation 5.

$$I_{(REV)} = C_{IN} \times \left(\frac{dV_{(OUT)}}{dt} \right) \quad (5)$$

For example, if the ramp rate of the output voltage is set at 10 mV/ µs then the required input capacitance C_{IN} to achieve reverse current greater than 238 mA is 23.8 µF. Considering tolerance of ±10% in capacitance and a standard value, capacitor of 33 µF should be used as C_{IN} in this case.

9.3.6 FAULT Response

The $\overline{FLT}$ open-drain output is asserted (active low) during undervoltage, overvoltage, reverse voltage-current and thermal shutdown conditions. Additionally, in the TPS25944, the $\overline{FLT}$ is asserted when overload condition exists for more than the fault time period ($t_{CB(dly)}$). The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. The device is designed to eliminate false fault reporting by using an internal "de-glitch" circuit for undervoltage and overvoltage (2.2-µs typical) conditions without the need for external circuitry. This ensures that fault is not accidentally asserted during transients on input bus.

Connect $\overline{FLT}$ with a pull up resistor to Input or Output voltage rail. $\overline{FLT}$ may be left open or tied to ground when not used. $V_{(IN)}$ falling below $V_{(UVF)}$ = 2.1 V resets $\overline{FLT}$.

9.3.7 Current Monitoring

The current source at IMON terminal is configured to be proportional to the current flowing from IN to OUT. This current can be converted to a voltage using a resistor $R_{(IMON)}$ from IMON terminal to GND terminal. This voltage, computed using Equation 7, can be used as a means of monitoring current flow through the system.

The maximum voltage range for monitoring the current ($V_{(IMONmax)}$) is limited to minimum([$V_{(IN)}$ – 2.2 V], 6 V) to ensure linear output. This puts limitation on maximum value of $R_{(IMON)}$ resistor and is determined by Equation 6.

$$R_{(IMONmax)} = \frac{\text{minimum } (V_{(IN)} - 2.2,\ 6)}{1.6 \times I_{(LIM)} \times GAIN_{(IMON)}} \quad (6)$$

The output voltage at IMON terminal is calculated from Equation 7.

$$V_{(IMON)} = \left[I_{(OUT)} \times GAIN_{(IMON)} + I_{(IMON\_OS)} \right] \times R_{(IMON)}$$

where

- $GAIN_{(IMON)}$ = Gain factor $I_{(IMON)}$:$I_{(OUT)}$ = 52 µA/A
- $I_{(OUT)}$ = Load current
- $I_{(IMON\_OS)}$ = 0.8 µA (typical) (7)

This pin must not have a bypass capacitor to avoid delay in the current monitoring information.

The voltage at IMON pin can be digitized using an ADC (such as ADS1100, SBAS239) to read the current monitor information over an I2C bus.

Feature Description (continued)

9.3.8 Power Good Comparator

The devices incorporate a Power Good comparator for co-ordination of status to downstream DC-DC converters or system monitoring circuits. The comparator has an internal reference of $V_{(PGTHR)}$ = 0.99 V at negative terminal and positive terminal PGTH can be utilized for monitoring of either input or output of the device. The comparator output PGOOD is an open-drain active high signal, which can be used to indicate the status to downstream units. PGOOD is asserted high when internal FET is fully enhanced and PGTH pin voltage is higher than internal reference $V_{(PGTHR)}$.

The PGOOD signal has deglitch time incorporated to ensure that internal FET is fully enhanced before heavy load is applied by downstream converters. Rising deglitch delay is determined by Equation 8.

$$t_{PGOOD(degl)} = \text{Maximum } \{(3.5 \times 10^6 \times C_{(dVdT)}), t_{PGOODR}\} \quad (8)$$

Connect the PGOOD pin with a pull up resistor to Input or Output voltage rail. PGOOD may be left open or tied to ground when not used.

9.3.9 IN, OUT and GND Pins

The device has multiple pins for input (IN) and output (OUT).

All IN pins must be connected together and to the power source. A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 2.7 V-18 V.

Similarly all OUT pins must be connected together and to the load. $V_{(OUT)}$ in the ON condition, is calculated using Equation 9.

$$V_{(OUT)} = V_{(IN)} - (R_{ON} \times I_{(OUT)}) \quad (9)$$

where, R_{ON} is the total ON resistance of the internal FET.

GND terminal is the most negative voltage in the circuit and is used as a reference for all voltage reference unless otherwise specified.

9.3.10 Thermal Shutdown

The device has built-in over temperature shutdown circuitry designed to disable the internal FET, if the junction temperature exceeds 160°C (typical). The TPS25942L, 44L version latches off the internal FET, whereas the TPS25942A, 44A commences an auto-retry cycle 128 ms after $T_J < [T_{(TSD)} – 12°C]$. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to signal a fault condition.

9.4 Device Functional Modes

9.4.1 Diode Mode

The device provides a Diode Mode, where the power path from IN to OUT acts as a non-ideal diode rather than a FET, as shown in Figure 53. This mode is activated through DMODE terminal. This is an active high terminal with internal pull-down. The terminal is useful in Power-Mux applications to switch over from master to slave supplies and vice-versa smoothly, when two supplies are within a diode drop of each other. A high at this terminal activates the non-ideal diode mode. In this mode, the circuit breaker functionality (TPS25944x) is disabled and the overload current limit is set to 50 % of current limit determined by $R_{(ILIM)}$ resistor.

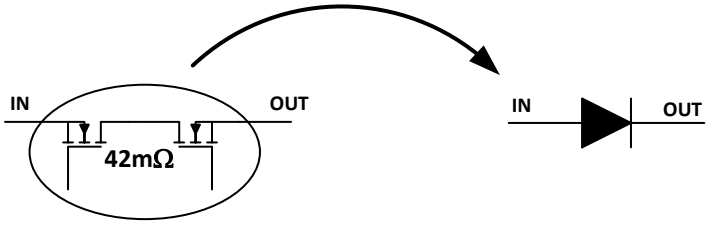


Figure 53. Diode Mode: IN to OUT Power Path

Device Functional Modes (continued)

9.4.2 Shutdown Control

The internal FET and hence the load current can be remotely switched off by taking the UVLO pin below its 0.6 V threshold with an open collector or open drain device as shown in Figure 54. The device quiescent current is reduced to less than 20 µA in this state. Upon releasing the UVLO pin the device turns on with soft-start cycle.

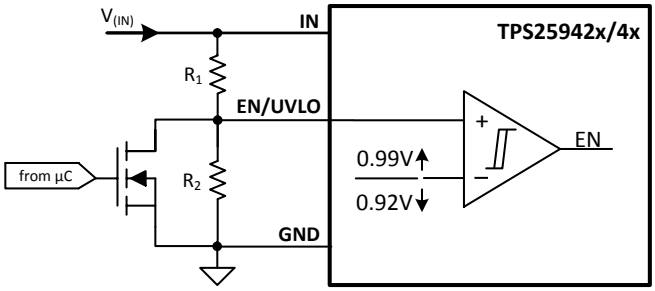


Figure 54. Shutdown Control

Device Functional Modes (continued)

9.4.3 Operational Differences Between the TPS25942 and TPS25944

The TPS25942 and TPS25944 respond differently to overload and short circuit conditions. The operational differences are explained in Table 1.

Table 1. Device Operational Differences

Device	TPS25942 (Current Limiter)	TPS25944 (Circuit Breaker)
Start-up	Inrush ramp controlled by dVdT	Inrush ramp controlled by dVdT
	Inrush limited to $I_{(LIM)}$ level as set by $R_{(ILIM)}$	Inrush limited to $I_{(LIM)}$ level as set by $R_{(ILIM)}$
		Fault Timer runs when current is limited to $I_{(LIM)}$
		Fault timer expires after $t_{CB(dly)}$ (4 ms) causing device shutoff
	If $T_J > T_{(TSD)}$ device shuts off	Device turns off if $T_J > T_{(TSD)}$ before timer expires
Over current response	Current is limited to $I_{(LIM)}$ level as set by $R_{(ILIM)}$	Current is allowed through the device if $I_{(LOAD)} < I_{(FASTRIP)}$
	Power dissipation increases as $V_{(IN)} – V_{(OUT)}$ grows	Fault Timer runs when current goes above $I_{(LIM)}$
		Fault timer expires after $t_{CB(dly)}$ (4 ms) causing device shutoff
	Device turns off when $T_J > T_{(TSD)}$	Device turns off if $T_J > T_{(TSD)}$ before timer expires
	‘L' Version remains off	‘L' Version remains off
	'A' Version attempts restart 128 ms after $T_J < [T_{(TSD)} –12°C]$	'A' Version attempts restart 128 ms after $T_J < [T_{(TSD)} – 12°C]$
Short-circuit response	Fast shut off when $I_{(LOAD)} > I_{(FASTRIP)}$	Fast shut off when $I_{(LOAD)} > I_{(FASTRIP)}$
	Quick restart and current limited to $I_{(LIM)}$, follows standard TPS25942 start-up	Quick restart and current limited to $I_{(LIM)}$, follows standard TPS25944 start-up

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

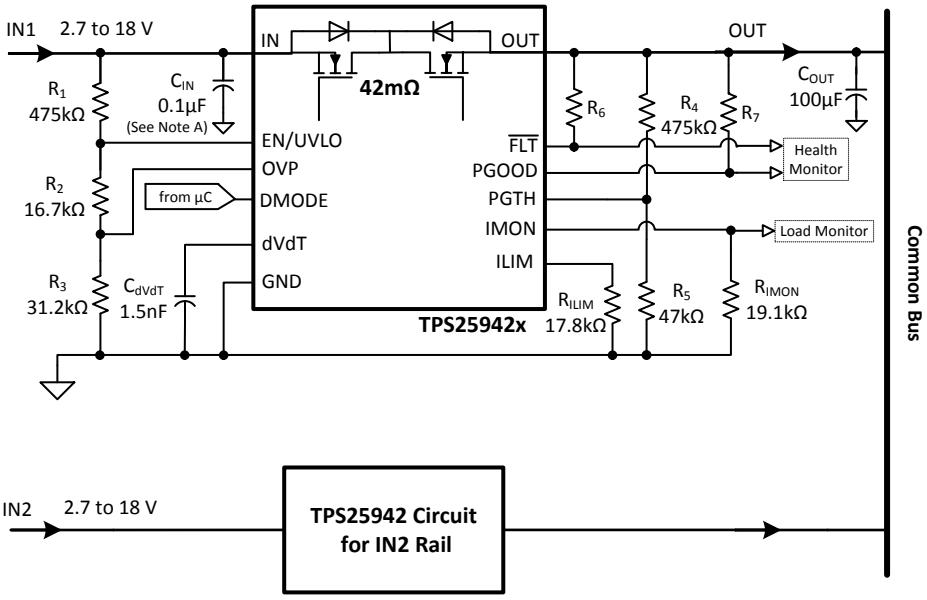
The device is a smart eFuse. It is typically used for Active ORing and Power Multiplexing applications. It operates from 2.7 V to 18 V with programmable current limit, overvoltage and undervoltage protection. The device aids in controlling the in-rush current and in seamless power path management of multiple voltage rails for systems such as PCIe cards, Network and Graphic Cards and SSDs. The device also provides robust protection for multiple faults on the sub-system rail.

The following design procedure can be used to select component values for the TPS25942, TPS25944.

Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS25942_44 Design Calculator* is available on web folder.

This section presents a simplified discussion of the design process.

10.2 Typical Application



A. C_{IN}: Optional and only for noise suppression.

Figure 55. Typical Application Schematics: Active ORing Configuration

Typical Application (continued)

10.2.1 Design Requirements

Table 2 lists the TPS25942, TPS25944 design parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, $V_{(IN)}$	12 V
Undervoltage lockout set point, $V_{(UV)}$	10.8 V
Overvoltage protection set point , $V_{(OV)}$	16.5 V
Load at start-up , $R_{L(SU)}$	4.8 Ω
Current limit, $I_{(LIM)}$	5 A
Load capacitance , $C_{(OUT)}$	100 µF
Maximum ambient temperatures , T_A	85°C

10.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS25942, TPS25944.

10.2.2.1 Step by Step Design Procedure

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal input operation voltage
- Maximum output capacitance
- Maximum current Limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

10.2.2.2 Programming the Current-Limit Threshold: $R_{(ILIM)}$ Selection

$R_{(ILIM)}$ sets the current limit. Using Equation 4.

$$R_{(ILIM)} = \frac{89}{5} = 17.8k\Omega \quad (10)$$

Choose the closest standard value: 17.8k, 1% standard value resistor.

10.2.2.3 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using the external voltage divider network of R_1, R_2 and R_3 as connected between IN, EN, OVP and GND pins of the TPS25942, TPS25944 devices. The values required for setting the undervoltage and overvoltage are calculated solving Equation 11 and Equation 12.

$$V_{(OVPR)} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{(OV)}$$

where

- $V_{(OVPR)}$ = OVP Threshold for rising voltage

(11)

$$V_{(ENR)} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{(UV)}$$

where

- $V_{(ENR)}$ = Enable threshold for rising voltage

(12)

For minimizing the input current drawn from the power supply {$I_{(R123)} = V_{(IN)}/(R_1 + R_2 + R_3)$}, it is recommended to use higher values of resistance for R_1, R_2 and R_3.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I_{(R123)}$ must be chosen to be 20x greater than the leakage current expected.

From the device electrical specifications, $V_{(OVPR)}$ = 0.99 V and $V_{(ENR)}$ = 0.99 V. For design requirements, $V_{(OV)}$ is 16.5 V and $V_{(UV)}$ is 10.8 V. To solve the equation, first choose the value of R_3 = 31.2 kΩ and use Equation 11 to solve for (R_1 + R_2) = 488.8 kΩ. Use Equation 12 and value of (R_1 + R_2) to solve for R_2 = 16.47 kΩ and finally R_1= 472.33 kΩ.

Using the closest standard 1% resistor values gives R_1 = 475 kΩ, R_2 = 16.7 kΩ, and R_3 = 31.2 kΩ.

The power fail threshold $V_{(PFAIL)}$ is detected on the falling edge of the power supply. The falling voltage threshold is 7% lower than the rising voltage threshold, so for a set $V_{(UV)}$ the power fail voltage $V_{(PFAIL)}$ is given by Equation 13.

$$V_{(PFAIL)} = 0.93 \times V_{(UV)} \tag{13}$$

10.2.2.4 Programming Current Monitoring Resistor—R_{IMON}

Voltage at IMON pin $V_{(IMON)}$ represents the voltage proportional to load current. This can be connected to an ADC of the downstream system for health monitoring of the system. The $R_{(IMON)}$ need to be configured based on the maximum input voltage range of the ADC used. $R_{(IMON)}$ is set using Equation 14.

$$R_{(IMON)} = \frac{V_{(IMONmax)}}{I_{(LIM)} \times 52 \times 10^{-6}} \ k\Omega \tag{14}$$

For $I_{(LIM)}$ = 5 A, and considering the operating range of ADC from 0 V to 5 V, $V_{(IMONmax)}$ is 5 V and $R_{(IMON)}$ is determined by Equation 15:

$$R_{(IMON)} = \frac{5}{5 \times 52 \times 10^{-6}} = 19.23 \ k\Omega \tag{15}$$

Selecting $R_{(IMON)}$ value less than determined by Equation 15 ensures that ADC limits are not exceeded for maximum value of load current.

If the IMON pin voltage is not being digitized with an ADC, $R_{(IMON)}$ can be selected to produce a 1V/1A voltage at the IMON pin, using Equation 14.

Choose closest 1 % standard value: 19.1 kΩ.

If current monitoring up to $I_{(FASTRIP)}$ is desired, $R_{(IMON)}$ can be reduced by a factor of 1.6, as in Equation 6.

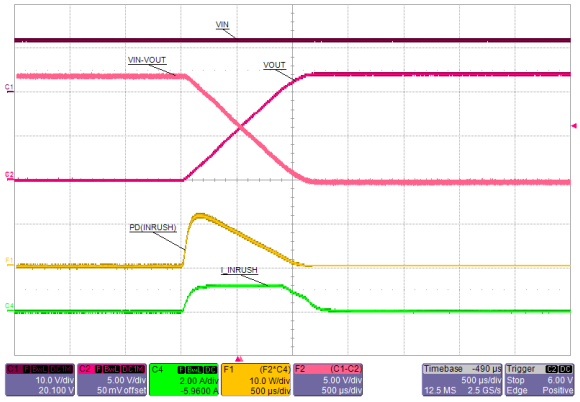
10.2.2.5 Setting Output Voltage Ramp Time (t_{dVdT})

For a successful design, the junction temperature of device must be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor $C_{(dVdT)}$ needed is calculated considering the two possible cases:

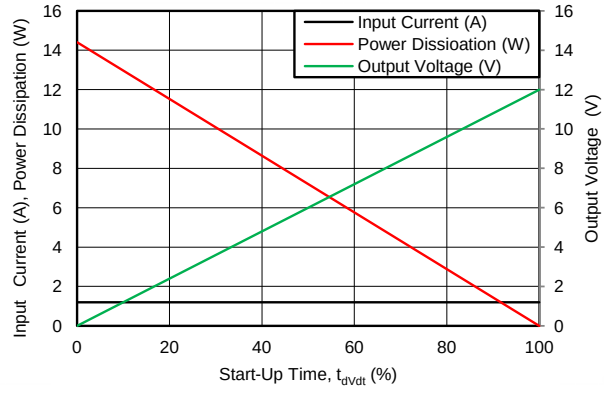
10.2.2.5.1 Case1: Start-Up Without Load: Only Output Capacitance $C_{(OUT)}$ Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference across the internal FET decreases, and the power dissipated decreases as well. Typical ramp-up of output voltage $V_{(OUT)}$ with inrush current limit of 1.2 A and power dissipated in the device during start-up is shown in Figure 56. The average power dissipated in the device during start-up is equal to area of triangular plot (red curve in Figure 57) averaged over t_{dVdT}.



$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $C_{(OUT)}$ = 100 µF

Figure 56. Typical Start-Up Without Load



$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $C_{(OUT)}$ = 100 µF

Figure 57. $P_{D(INRUSH)}$ Due to Inrush Current

For the TPS25944, TPS25944 device, the inrush current is determined as shown in Equation 16.

$$I = C \times \frac{dV}{dT} \Rightarrow I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \quad (16)$$

Power dissipation during start-up is given by Equation 17.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (17)$$

Equation 17 assumes that load does not draw any current until the output voltage has reached its final value.

10.2.2.5.2 Case 2: Start-Up With Load: Output Capacitance $C_{(OUT)}$ and Load Draws Current During Start-Up

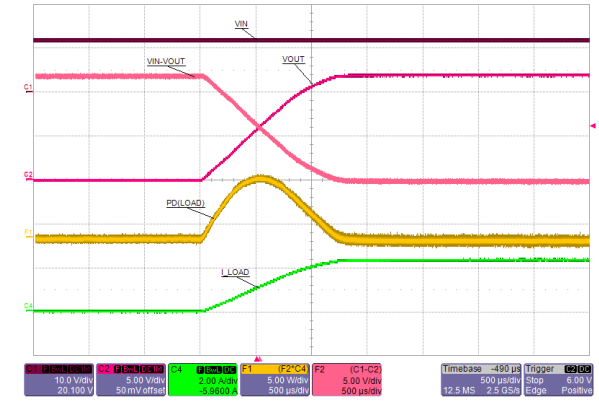
When load draws current during the turn-on sequence, there is additional power dissipated. Considering a resistive load $R_{L(SU)}$ during start-up, load current ramps up proportionally with increase in output voltage during t_{dVdT} time. Typical ramp-up of output voltage, load current and power dissipated in the device is shown in Figure 58 and power dissipation with respect to time is plotted in Figure 59. The additional power dissipation during start-up phase is calculated as follows shown in Equation 18 and Equation 19.

$$(V_I - V_O)(t) = V_{(IN)} \times \left(1 - \frac{t}{t_{dVdT}}\right) \quad (18)$$

$$I_L(t) = \left(\frac{V_{(IN)}}{R_{L(SU)}}\right) \times \frac{t}{t_{dVdT}} \quad (19)$$

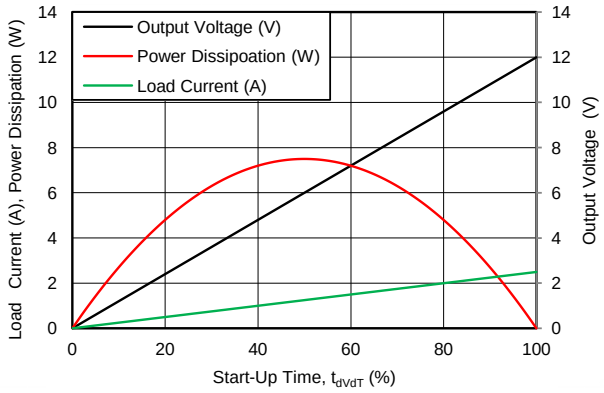
Where $R_{L(SU)}$ is the load resistance present during start-up. Average energy loss in internal FET during charging time due to resistive load is given by Equation 20.

$$W_t = \int_0^{tdVdT} V_{(IN)} \times \left(1 - \frac{t}{t_{dVdT}}\right) \times \left(\frac{V_{(IN)}}{R_{L(SU)}} \times \frac{t}{t_{dVdT}}\right) dt \quad (20)$$



$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF, $C_{(OUT)}$ = 100 µF $R_{L(SU)}$ = 4.8 Ω

Figure 58. Typical Start-Up With Load



$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF, $C_{(OUT)}$ = 100 µF $R_{L(SU)}$ = 4.8 Ω

Figure 59. $P_{D(LOAD)}$ in Load During Start-Up

Solving Equation 20 the average power loss in the device due to load is given by Equation 21.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V^2_{(IN)}}{R_{L(SU)}} \quad (21)$$

Total power dissipated in the device during start-up is given by Equation 22.

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (22)$$

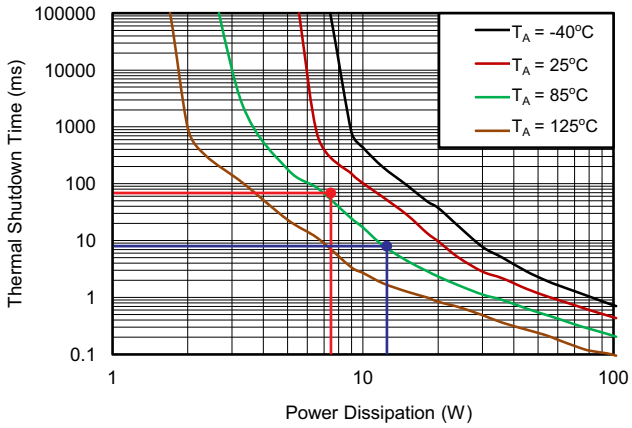
Total current during start-up is given by Equation 23.

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (23)$$

If $I_{(STARTUP)} > I_{(LIM)}$, the device limits the current to $I_{(LIM)}$ and the current limited charging time is determined by Equation 24.

$$t_{dVdT(current\ limited)} = C_{(OUT)} \times \frac{V_{(IN)}}{I_{(LIM)}} \quad (24)$$

The power dissipation, with and without load, for selected start-up time must not exceed the shutdown limits as shown in Figure 60.



Taken on 2-Layer board, 2oz.(0.08-mm thick) with GND plane area: 14 cm^2 (Top) and 20 cm^2 (Bottom)

Figure 60. Thermal Shutdown Limit Plot

For the design example under discussion,

Select ramp-up capacitor $C_{(dVdT)}$ = 1nF, using Equation 2, we get Equation 25.

$$t_{dvdt} = 8.3 \times 10^4 \times 12 \times 1 \times 10^{-9} = 0.996ms = \sim 1ms \quad (25)$$

The inrush current drawn by the load capacitance ($C_{(OUT)}$) during ramp-up is calculated using Equation 3 and Equation 26.

$$I_{(INRUSH)} = \left(100 \times 10^{-6}\right) \times \left(\frac{12}{1 \times 10^{-3}}\right) = 1.2\ A \quad (26)$$

The inrush Power dissipation is calculated, using Equation 17 and Equation 27.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 1.2 = 7.2\ W \quad (27)$$

For 7.2 W of power loss, the thermal shut down time of the device must not be less than the ramp-up time t_{dVdT} to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph Figure 60 at T_A = 85°C, for 7.2 W of power the shutdown time is approximately 60 ms. So it is safe to use 1 ms as start-up time without any load on output.

Considering the start-up with load 4.8 Ω, the additional power dissipation, when load is present during start-up is calculated, using Equation 21 and Equation 28.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{12 \times 12}{4.8} = 5\ W \quad (28)$$

The total device power dissipation during start up is given by Equation 29.

$$P_{D(STARTUP)} = (7.2 + 5) = 12.2\ W \quad (29)$$

From thermal shutdown limit graph at T_A = 85°C, the thermal shutdown time for 12.2 W is close to 7.5 ms. It is safe to have 30% margin to allow for variation of system parameters such as load, component tolerance, and input voltage. So it is well within acceptable limits to use the 1 nF capacitor with start-up load of 4.8 Ω.

If there is a need to decrease the power loss during start-up, it can be done with increase of $C_{(dVdT)}$ capacitor.

To illustrate, choose $C_{(dVdT)}$ = 1.5 nF as an option and recalculate as shown in Equation 30 to Equation 34.

$$t_{dvdt} = 1.5ms \quad (30)$$

$$I_{(INRUSH)} = \left(100 \times 10^{-6}\right) \times \left(\frac{12}{1.5 \times 10^{-3}}\right) = 0.8\ A \quad (31)$$

$$P_{D(INRUSH)} = 0.5 \times 12 \times 0.8 = 4.8\ W \quad (32)$$

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \left(\frac{12 \times 12}{4.8}\right) = 5\ W \quad (33)$$

$$P_{D(STARTUP)} = 4.8 + 5 = 9.8\ W \quad (34)$$

From thermal shutdown limit graph at T_A = 85°C, the shutdown time for 10 W power dissipation is approximately 17 ms, which increases the margins further for shutdown time and ensures successful operation during start-up and steady state conditions.

The spreadsheet tool available on the web can be used for iterative calculations.

10.2.2.6 Programing the Power Good Set Point

As shown in Figure 55, R_4 and R_5 sets the required limit for PGOOD signal as needed for the downstream converters. Considering a power good threshold of 11 V for this design, the values of R_4 and R_5 are calculated using Equation 35.

$$V_{(PGTH)} = 0.99 \times \left(1 + \frac{R_4}{R_5}\right) \quad (35)$$

It is recommended to have high values for these resistors to limit the current drawn from the output node. Choosing a value of R_4 = 475 kΩ, R_5 = 47 kΩ provides $V_{(PGTH)}$ = 11 V.

10.2.2.7 Support Component Selections—R_6, R_7 and C_{IN}

Reference to application schematics, R_6 and R_7 are required only if PGOOD and $\overline{FLT}$ are used; these resistors serve as pull-ups for the open-drain output drivers. The current sunk by each of these pins must not exceed 10 mA (see the *Absolute Maximum Ratings* table). C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended for C_{IN}.

10.2.3 Application Curves

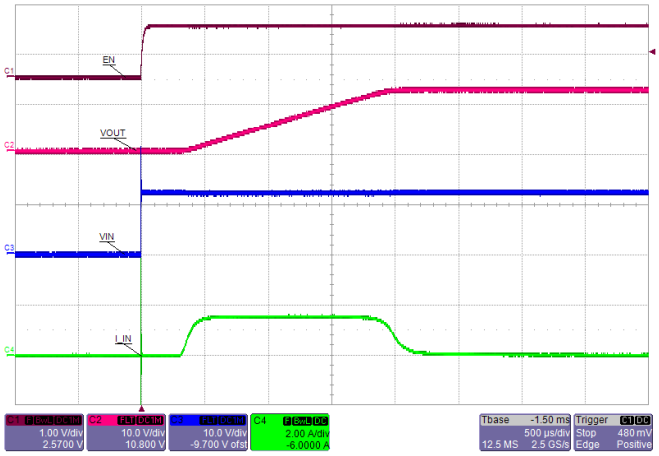


Figure 61. Hot-Plug Start-Up: Output Ramp Without Load on Output

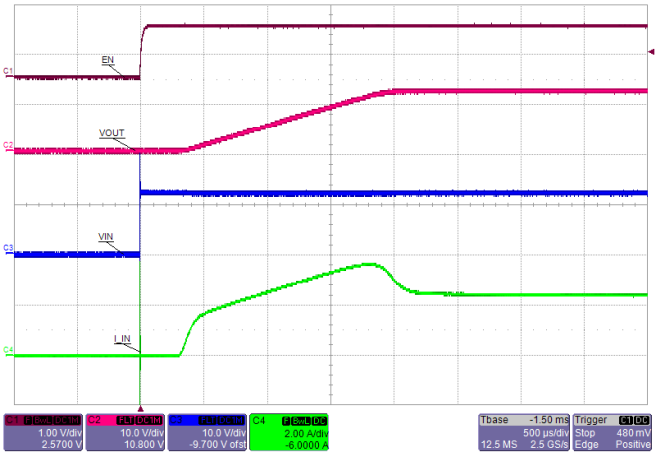


Figure 62. Hot-Plug Start-Up: Output Ramp With Start-Up load of 4.8 Ω

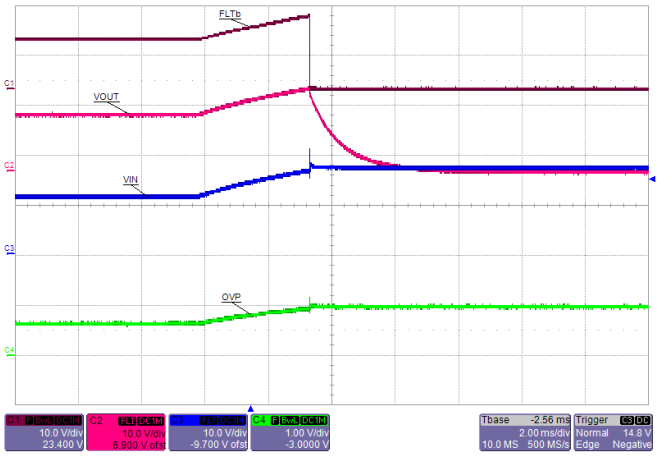


Figure 63. Overvoltage Shutdown

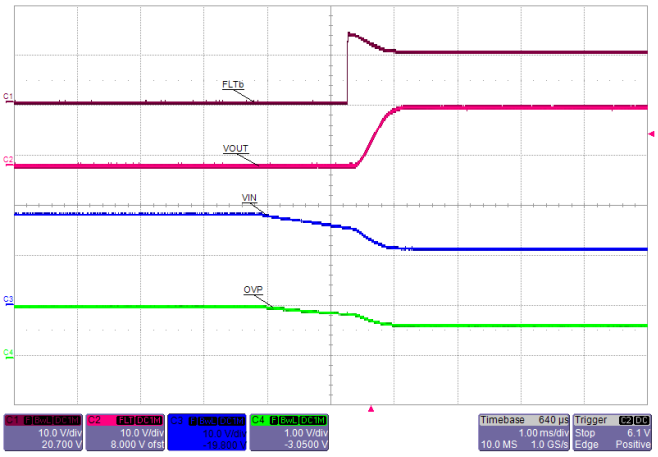


Figure 64. Overvoltage Recovery

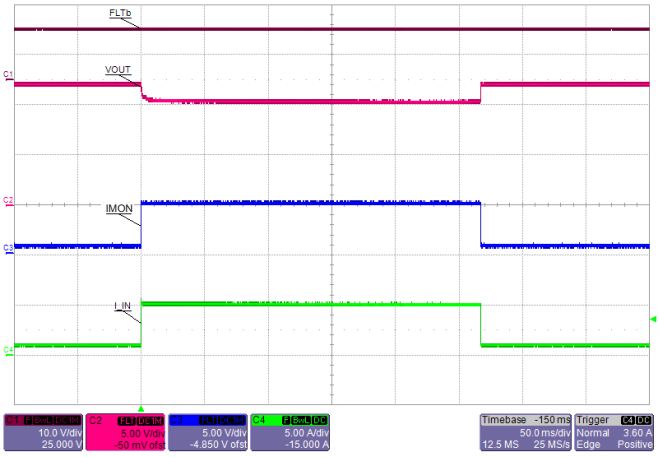


Figure 65. Over Load: Step Change in Load From 12 Ω to 2 Ω and Back

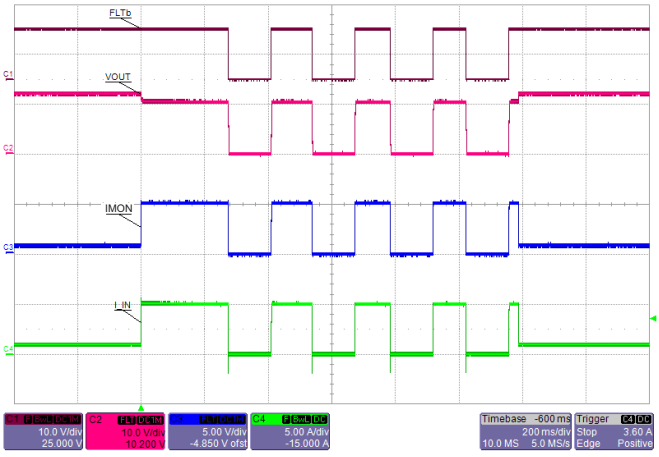


Figure 66. Overload Condition: Auto Retry and Recovery—TPS25942A

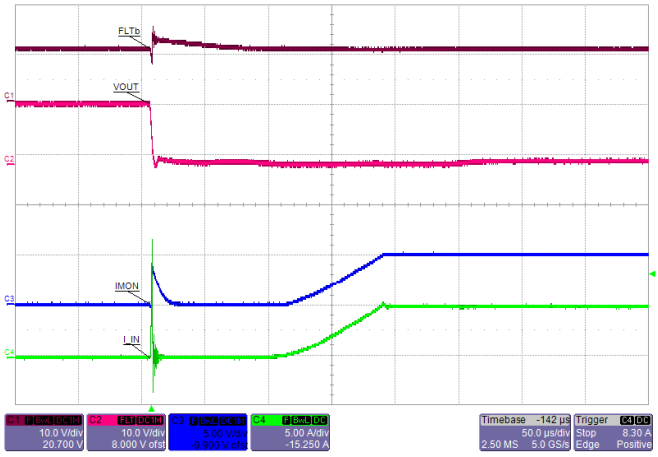


Figure 67. Hot Short: Fast Trip and Current Regulation

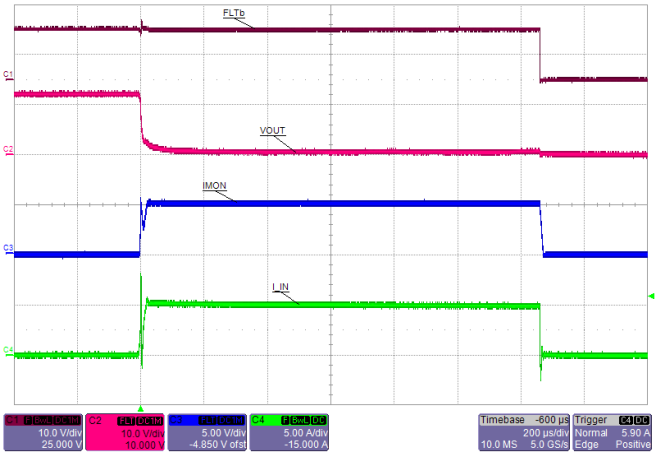


Figure 68. Hot Short: Latched—TPS25942L

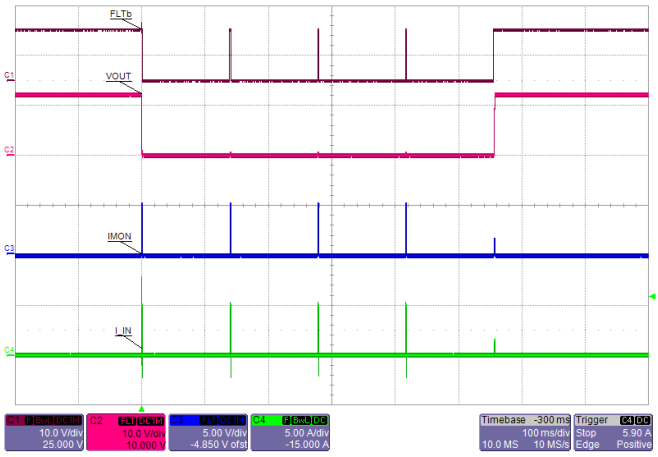


Figure 69. Hot Short: Auto-Retry and Recovery from Short Circuit—TPS25942A

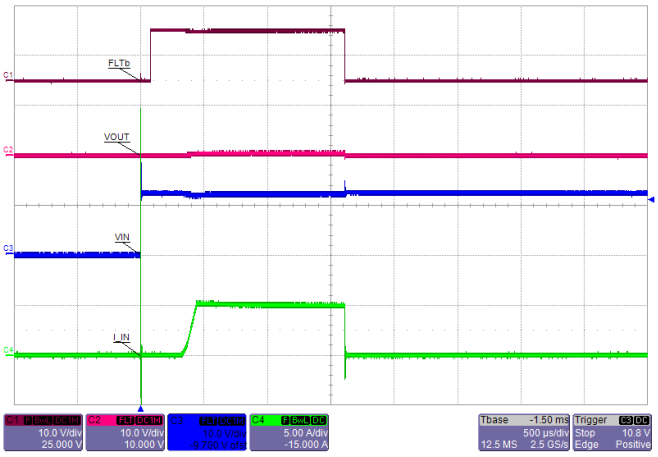


Figure 70. Hot Plug-In with Short on Output: Latched—TPS25942L

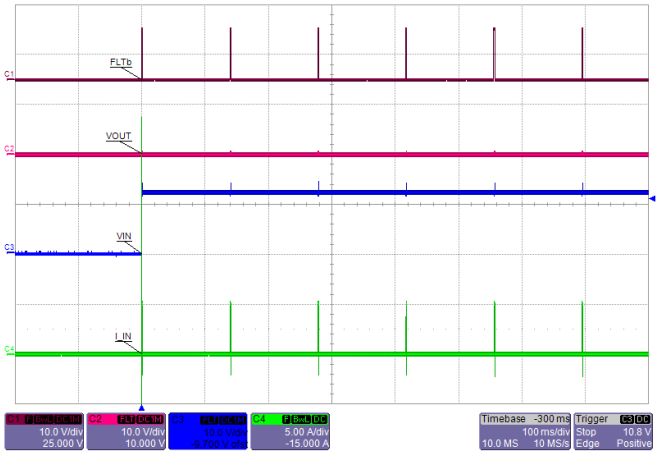


Figure 71. Hot Plug-In With Short on Output: Auto-Retry—TPS25942A

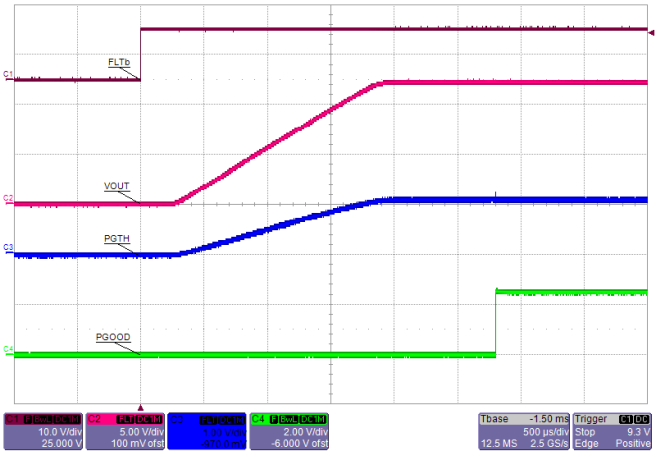


Figure 72. Power Good Response During Turnon

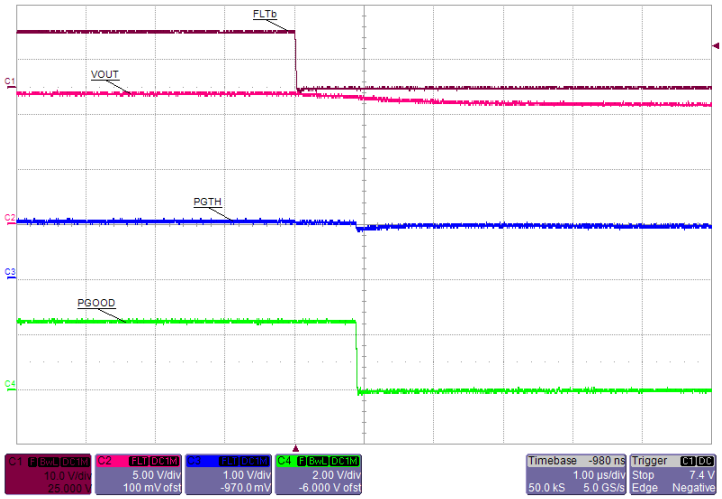


Figure 73. Power Good Response During Turnoff

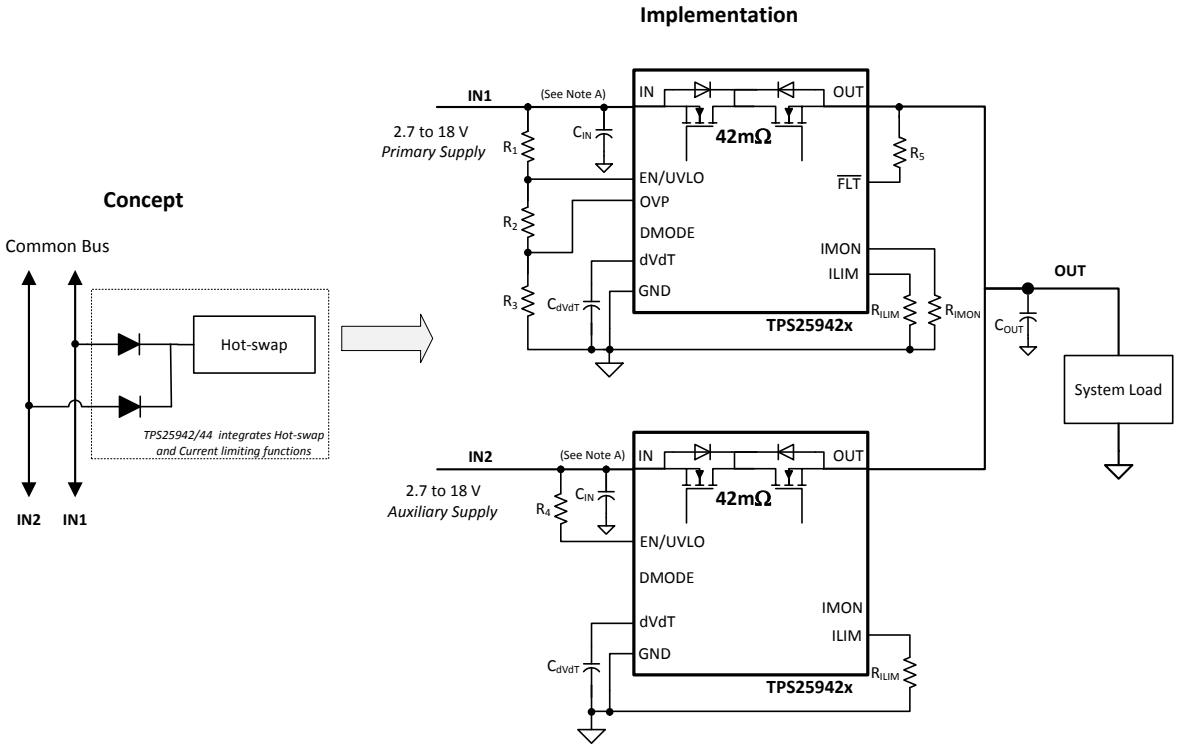
10.3 System Examples

The TPS25942 and TPS25944 provide a simple solution for power multiplexing applications through seamless transition between two power supplies, each operating at 2.7 V to 18 V and delivering up to 5 A. The devices with a distinctive feature set of true-reverse blocking, auto-forward conduction and fast switch over, support applications for both Active ORing and Priority power multiplexing.

10.3.1 Active ORing (Auto-Power Multiplexer) Operation

A typical redundant power supply configuration of the system is shown in Figure 74. Schottky ORing diodes have been popular for connecting parallel power supplies, such as parallel operation of wall adapter with a battery or a hold-up storage capacitor. The disadvantage of using ORing diodes is high voltage drop and associated power loss. The TPS25942 and TPS25944 with an integrated, low-ohmic N-channel FET provide a simple and efficient solution. Figure 74 shows the Active ORing implementation using the devices.

System Examples (continued)



A. C_{IN}: Optional and only for noise suppression.

Figure 74. Active ORing Implementation

A fast reverse comparator controls the internal FET and it is turned ON or OFF with hysteresis as shown in Figure 75. The internal FET is turned ON in less than 4 us (typical) when the forward voltage drop $V_{(IN)} – V_{(OUT)}$ exceeds 100 mV and is turned off in 1 µs (typical) as soon as $V_{(IN)} – V_{(OUT)}$ falls below –10 mV. When internal FET is turned ON, the ORed input supply experiences momentary in-rush current drawn as the FET turns on charging the bus capacitance. In addition, device can be operated in *Diode Mode* by independently controlling DMODE pin.

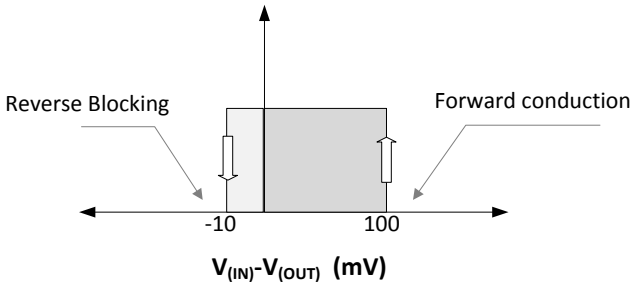
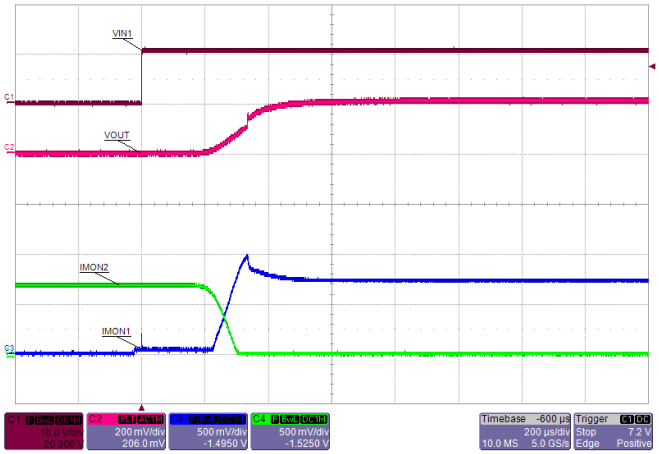


Figure 75. Active ORing Thresholds

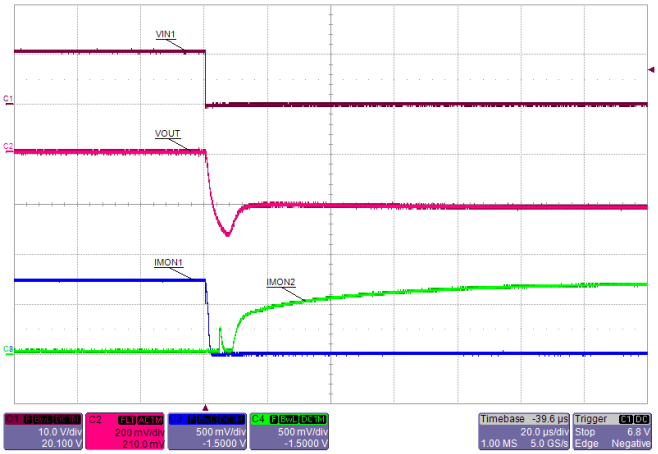
Figure 75 shows typical switch-over waveforms of Active ORing implementation using the TPS25942 or TPS25944.

System Examples (continued)



$V_{(IN1)}$ = 12.2 V
R_L = 14 Ω
$V_{(IN2)}$ = 12 V
$C_{(dVdT)}$ = 1.5 nF
$C_{(OUT)}$ = 100 µF

Figure 76. IN1 Power Recovery: Change Over from IN2 to IN1 ($V_{(OUT)}$ is AC Coupled)



$V_{(IN1)}$ = 12.2 V
R_L = 14 Ω
$V_{(IN2)}$ = 12 V
$C_{(dVdT)}$ = 1.5 nF
$C_{(OUT)}$ = 100 µF

Figure 77. IN1 Brownout Condition: Change Over from IN2 to IN1 ($V_{(OUT)}$ is AC Coupled)

When bus voltages (IN1 and IN2) are matched, device in each rail sees a forward voltage drop and is ON delivering the load current. During this period, current is shared between the rails in the ratio of differential voltage drop across each device.

In addition to above, the devices provide inrush current limit and protects each rail from potential overload and short circuit faults.

10.3.1.1 N+1 Power Supply Operation

The devices can be used to combine multiple power supplies to a common bus in an N+1 configuration. The N+1 power supply configuration as shown in Figure 78, is used where multiple power supplies are paralleled for either higher capacity, redundancy or both. If it takes N supplies to power the load, adding an extra identical unit in parallel permits the load to continue operation in the event that any one of the N supplies fails. The devices emulate the function of the ORing diode and provides with all protections as needed to isolate the rail during hot-plug, overvoltage, undervoltage, overcurrent and short-circuit conditions.

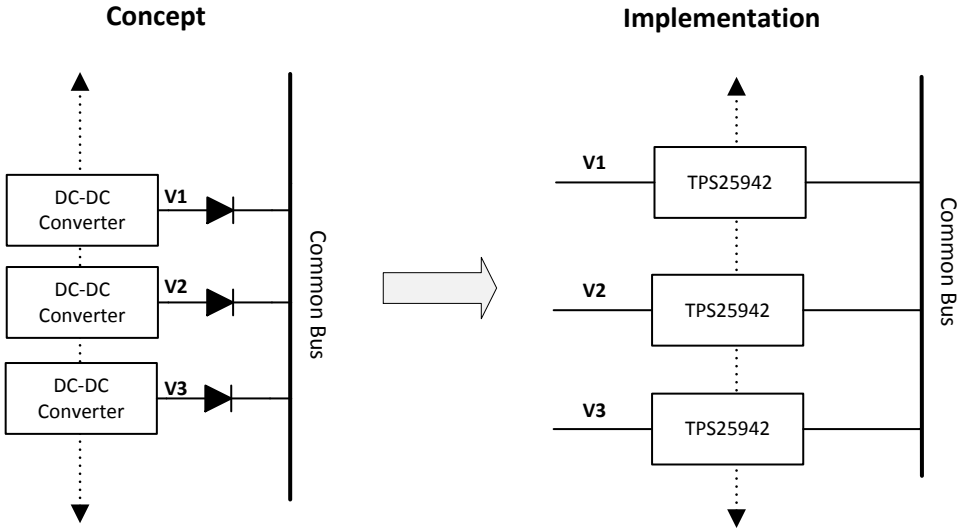


Figure 78. N+1 Configuration Implementation

System Examples (continued)

10.3.1.2 Priority Power MUX Operation

Applications having two energy sources such as PCIe cards, Tablets and Portable battery powered equipment require preference of one source to another. For example, mains power (wall-adapter) has the priority over the internal back-up power or auxiliary power. These applications demand for switch over from mains power to back-up power only when main input voltage falls below a user defined threshold. The devices provide a simple solution for priority power multiplexing needs.

Figure 79 shows a typical priority power multiplexing implementation using devices. When primary power IN1 is present, the device in IN1 path powers the OUT bus irrespective of whether auxiliary power IN2 is greater than or less than IN1. Once the voltage on the IN1 rail falls below the user-defined threshold, the device IN1 issues a signal to switch over to auxiliary power IN2. The transition happens seamlessly in less than 125 µs, with minimal voltage droop on the bus. The voltage droop during transition is a function of load current and bus capacitance (see Equation 36).

$$V_{(droop)} = \frac{I_{(Load)} \times 125\ \mu s}{C_{(BUS)}} \quad (36)$$

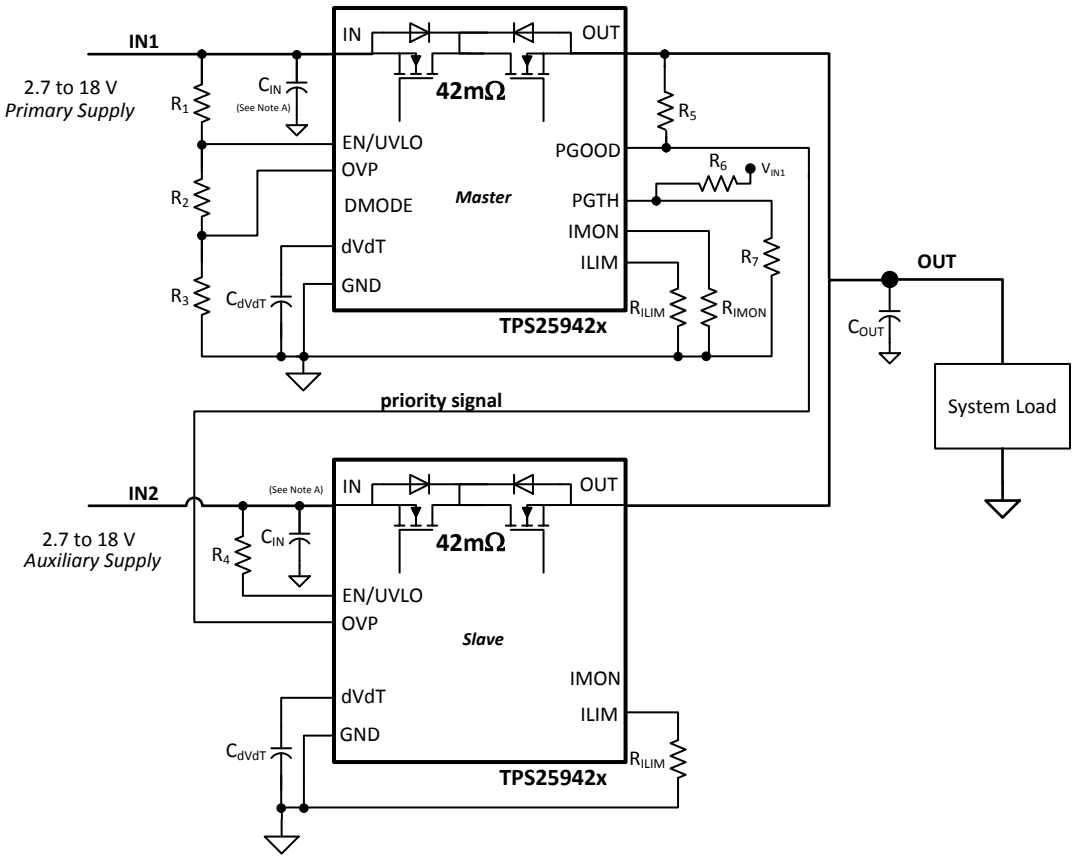
where

- $V_{(droop)}$ in Volts, $I_{(Load)}$ is load current in Ampere, $C_{(BUS)}$ is bus capacitance in µF

When the main voltage supply (IN1) is not present or during brown-out conditions, the device in auxiliary supply rail (IN2) provides power to the output. When IN1 recovers, the device connected to IN1 is turned on at defined slew rate and the device in IN2 path is turned off, allowing a seamless transition from auxiliary to the main voltage supply with minimal droop and with no shoot-through current.

Priority power multiplexing can be done either between two similar rails (such as 12 V Primary to 12 V Aux, 3.3 V Primary to 3.3 V Aux) or between dissimilar rails (such as 12 V Primary to 5 V Aux or 3.3 V Aux; or vice versa).

System Examples (continued)



A. C_{IN}: Optional and only for noise suppression.

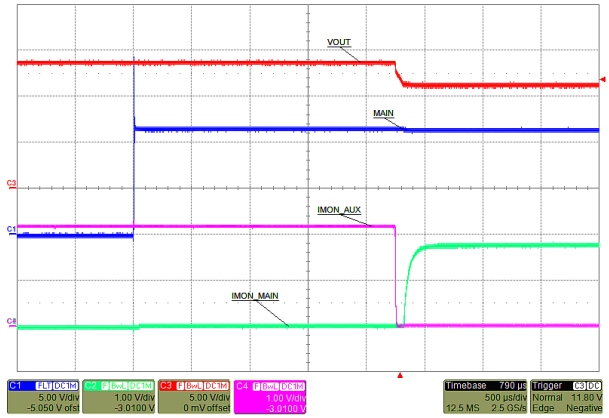
B. Master controls the slave using priority signal for switch over to Auxiliary power.

Figure 79. Priority Power Multiplexing Implementation

Figure 80 and Figure 81 show typical switch-over waveforms of Priority Muxing implementation using the TPS25942 or TPS25944 for 11.5 V Primary and 14.5 V Auxiliary Bus.

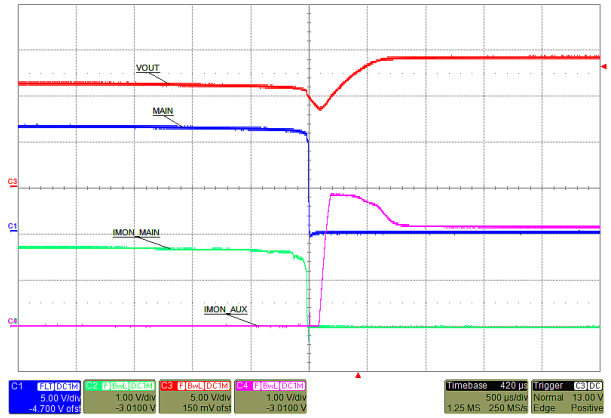
Figure 82 and Figure 83 show typical switch-over waveforms of Priority Muxing implementation using the TPS25942 or TPS25944 for 12 V Primary and 3.3 V Auxiliary Bus.

System Examples (continued)



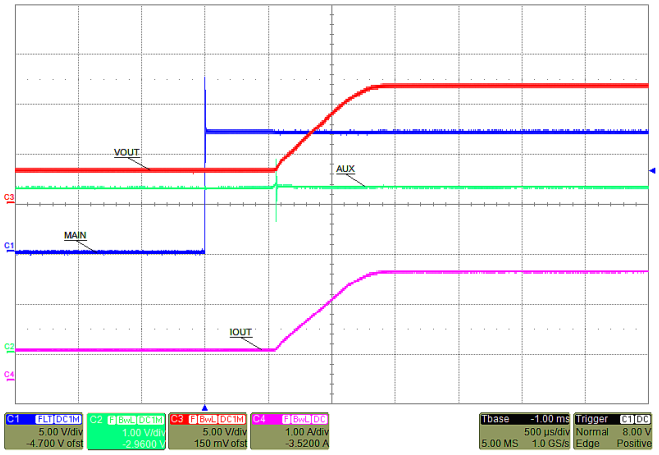
$V_{(IN1)}$ = 11.5 V
$V_{(IN2)}$ = 14.5 V
R_L = 5.6 Ω
$R_{(ILIM1)}$ = 24.6 kΩ,
$R_{(ILIM2)}$ = 33.2 kΩ
$R_{(IMON)}$ = 16.2 kΩ
$C_{(OUT)}$ = 150 µF
$C_{(dVdT)}$ = 1.2 nF
$V_{(UVLO-High)}$ = 10.8 V

Figure 80. IN1 Power Recovery: Change Over from Auxiliary IN2 to Primary Power IN1



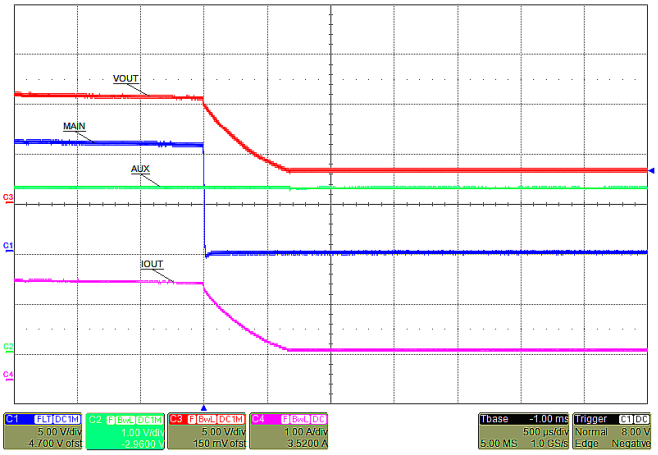
$V_{(IN1)}$ = 11.5 V
$V_{(IN2)}$ = 14.5 V
R_L = 5.6 Ω
$R_{(ILIM1)}$ = 24.6 kΩ
$R_{(ILIM2)}$ = 33.2 kΩ
$R_{(IMON)}$ = 16.2 kΩ
$C_{(OUT)}$ = 150 µF
$C_{(dVdT)}$ = 1.2 nF
$V_{(UVLO-Low)}$ = 10.2 V

Figure 81. IN1 Brownout Condition: Change Over from Main IN1 to Auxiliary Power IN2



$V_{(IN1)}$ = 12 V
$V_{(IN2)}$ = 3.3 V
R_{Load} = 5.6 Ω
$R_{(ILIM1)}$ = 24.6 kΩ
$R_{(ILIM2)}$ = 33.2 kΩ
$R_{(IMON)}$ = 16.2 kΩ
$C_{(OUT)}$ = 150 µF
$C_{(dVdT)}$ = 1.2 nF
$V_{(UVLO-High)}$ = 10.8 V

Figure 82. IN1 Power Recovery: Change Over from Auxiliary IN2 to Main Power IN1



$V_{(IN1)}$ = 12 V
$V_{(IN2)}$ = 3.3 V
R_L = 5.6 Ω
$R_{(ILIM1)}$ = 24.6 kΩ
$R_{(ILIM2)}$ = 33.2 kΩ
$R_{(IMON)}$ = 16.2 kΩ
$C_{(OUT)}$ = 150 µF
$C_{(dVdT)}$ = 1.2 nF
$V_{(UVLO-Low)}$ = 10.2 V

Figure 83. IN1 Brownout Condition: Change Over from Main IN1 to Auxiliary Power IN2

10.3.1.3 Priority MUXing With Almost Equal Rails (V_{IN1} ~ V_{IN2})

Most of the redundant power supply systems used in servers, storage and telecom, multiplex tightly regulated power rails to provide uninterrupted power to the load. In these systems, the primary and auxiliary rails are close to each other, typically within one diode drop when both rails are active.

For priority multiplexing in these systems, the TPS25942 or TPS25944 device in auxiliary rail path can be operated in *Diode Mode* for a fast switch-over (1 µs typical). The fast switch-over reduces the required hold-up capacitor on the output rail for a given droop specification.

The circuit implementation of this configuration is shown in Figure 84. During power-fail (brown-out) conditions of primary rail IN1, it changes IN2 from 'Diode-Mode' to normal operation using PGOOD. Similarly during power recovery of primary rail IN1, the auxiliary rail IN2 is driven into 'Diode-Mode'.

System Examples (continued)

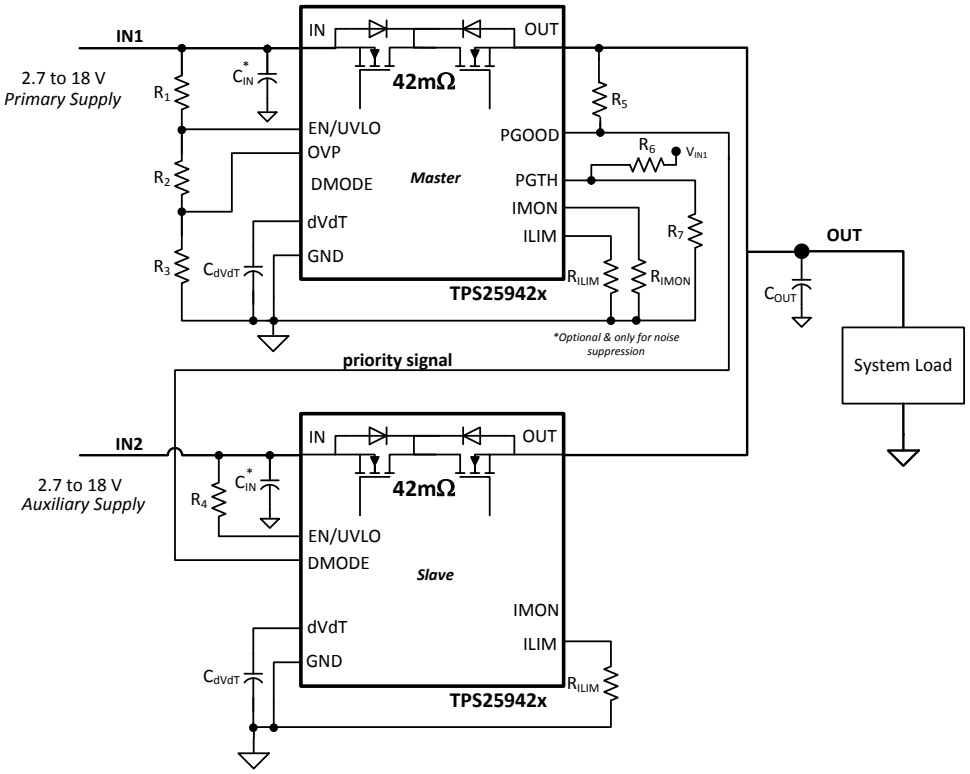
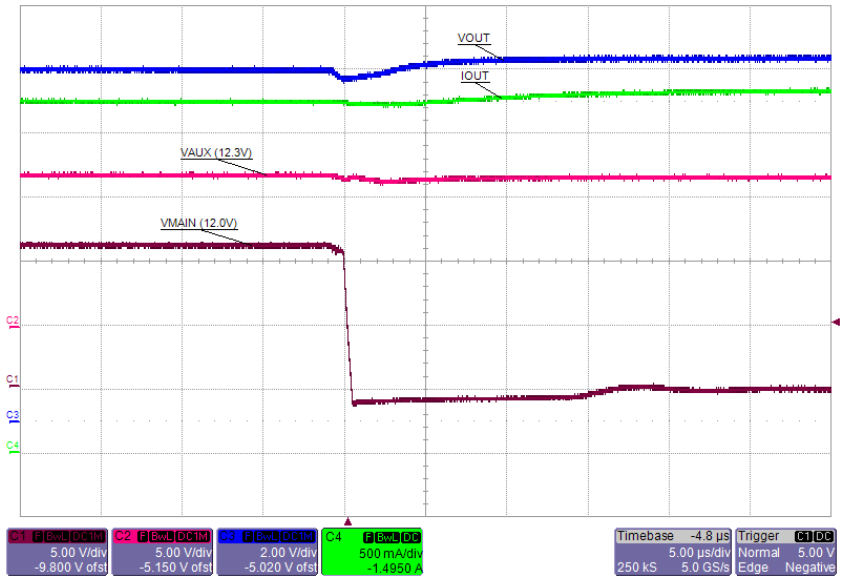


Figure 84. Priority Power Multiplexing Configuration for Almost Equal Rails

The fast switch-over performance is shown in Figure 85.



$C_{(OUT)}$ = 150 µF R_L = 4 Ω

Figure 85. Brownout Condition: Diode Mode for Multiplexing

System Examples (continued)

10.3.1.4 Reverse Polarity Protection

In applications demanding reverse polarity or reverse battery protection, the TPS25942 and TPS25944 can be used as an eFuse or ideal diode. A typical reverse polarity protection circuitry is shown in Figure 86. The signal diode in the GND terminal path ensures that device is not functional during reverse polarity conditions and internal FET blocks the reverse path.

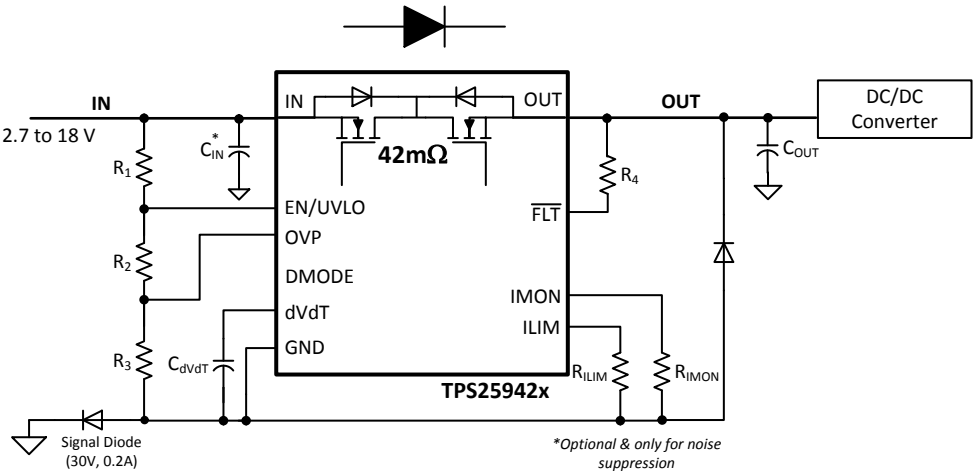


Figure 86. Reverse Polarity Protection Implementation

11 Power Supply Recommendations

The devices are designed for supply voltage range of 2.7 V ≤ V_{IN} ≤ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

11.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ = 0.001 µF to 0.1 µF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with Equation 37.

$$V_{SPIKE(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (37)$$

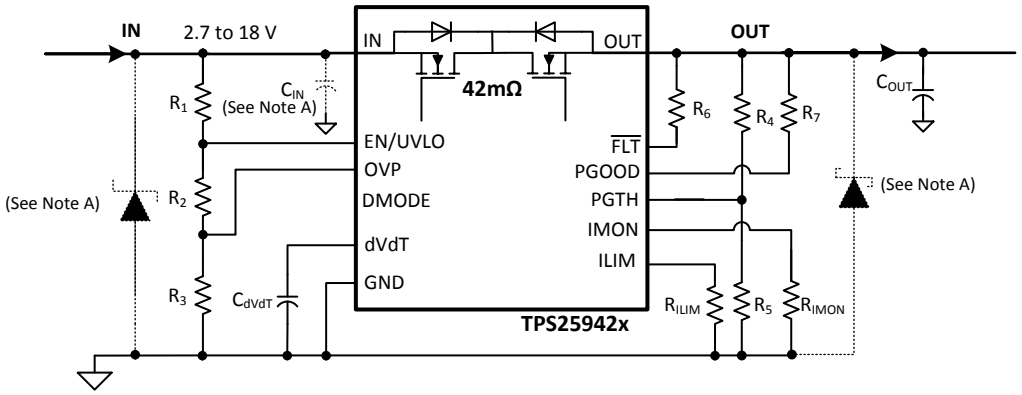
where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current,
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Transient Protection (continued)

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 87.



A. Optional components needed for suppression of transients

Figure 87. Circuit Implementation With Optional Protection Components

11.2 Output Short-Circuit Measurements

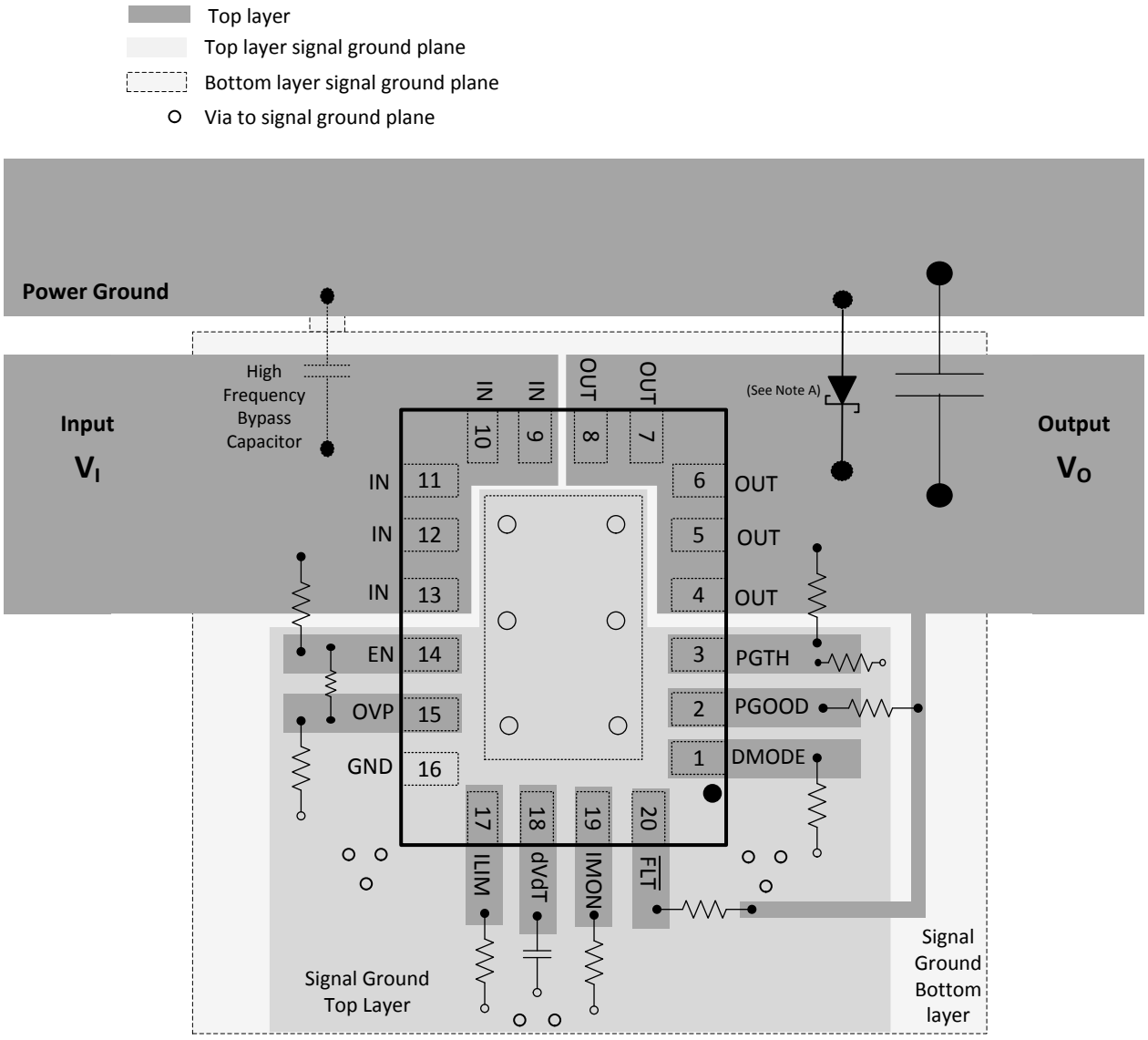
It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

12 Layout

12.1 Layout Guidelines

- For all applications, a 0.1-uF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated or minimized.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 88 for a PCB layout example.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- Low current signal ground (SGND), which is the reference ground for the device must be a copper plane or island.
- Locate all the TPS25942, TPS25944 support components: $R_{(ILIM)}$, C_{dVdT}, $R_{(IMON)}$, and resistors for UVLO and OVP, close to their connection pin. Connect the other end of the component to the SGND with shortest trace length.
- The trace routing for the R_{ILIM} and $R_{(IMON)}$ components to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- The SGND plane must be connected to high current ground (main power ground) at a single point, that is at the negative terminal of input capacitor.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Thermal Considerations: When properly mounted the PowerPAD™ package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the PowerPAD must be soldered directly to the board GND plane directly under the device. The PowerPAD is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. See the Technical Briefs: PowerPad™ Thermally Enhanced Package (SLMA002) and PowerPAD™ Made Easy (SLMA004) for more information on using this PowerPAD™ package.
- The thermal via land pattern specific to the TPS25942, TPS25944 can be downloaded from device webpage.
- Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

12.2 Layout Example



A. Optional: Needed only to suppress the transients caused by inductive load switching.

Figure 88. Board Layout

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

TPS25942AのPSpiceトランジェント・モデルについては、SLVMAA3Bを参照してください。

TPS25942LのPSpiceトランジェント・モデルについては、SLVMAA4Aを参照してください。

13.2 ドキュメントのサポート

13.2.1 関連資料

関連資料については、以下を参照してください。

- 『Power MUX内蔵の冗長化システムにおけるダイオード損失の低減』
- 『TPS25942x635EVM: TPS25942x用評価モジュール ユーザー・ガイド』
- 『TPS25944X635EVM: TPS25944X用評価モジュール』
- *『負荷スイッチとeFuseによる電源多重化』*

13.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS25942A	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS25942L	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS25944A	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS25944L	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

13.6 商標

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13.7 静電気放電に関する注意事項

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13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25942ARVCR	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25942A
TPS25942ARVCR.A	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25942A
TPS25942ARVCRG4	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25942A
TPS25942ARVCRG4.A	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25942A
TPS25942ARVCT	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25942A
TPS25942ARVCT.A	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25942A
TPS25942LRVCR	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25942L
TPS25942LRVCR.A	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25942L
TPS25942LRVCT	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25942L
TPS25942LRVCT.A	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25942L
TPS25942LRVCTG4	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25942L
TPS25942LRVCTG4.A	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25942L
TPS25944ARVCR	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25944A
TPS25944ARVCR.A	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25944A
TPS25944ARVCR.B	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25944A
TPS25944ARVCRG4	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25944A
TPS25944ARVCRG4.A	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25944A
TPS25944ARVCT	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25944A
TPS25944ARVCT.A	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25944A
TPS25944LRVCR	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25944L
TPS25944LRVCR.A	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25944L
TPS25944LRVCRG4	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25944L
TPS25944LRVCRG4.A	Active	Production	WQFN (RVC) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25944L
TPS25944LRVCT	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25944L
TPS25944LRVCT.A	Active	Production	WQFN (RVC) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25944L

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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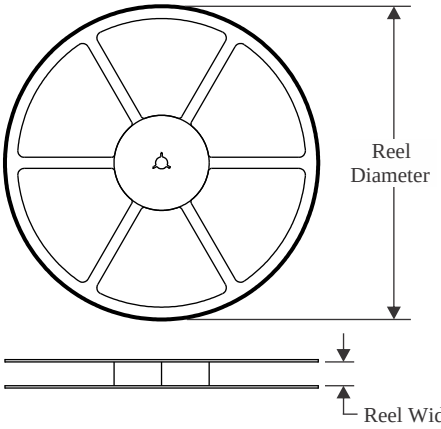
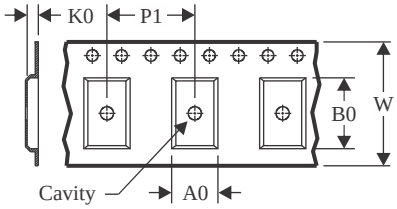
TAPE AND REEL INFORMATION

REEL DIMENSIONS

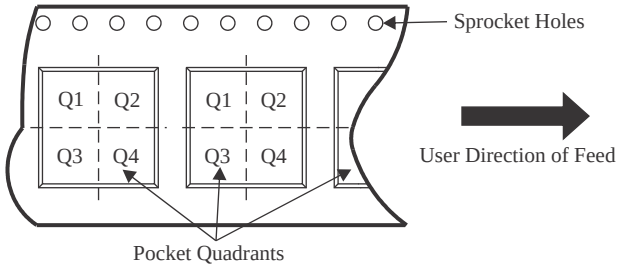


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

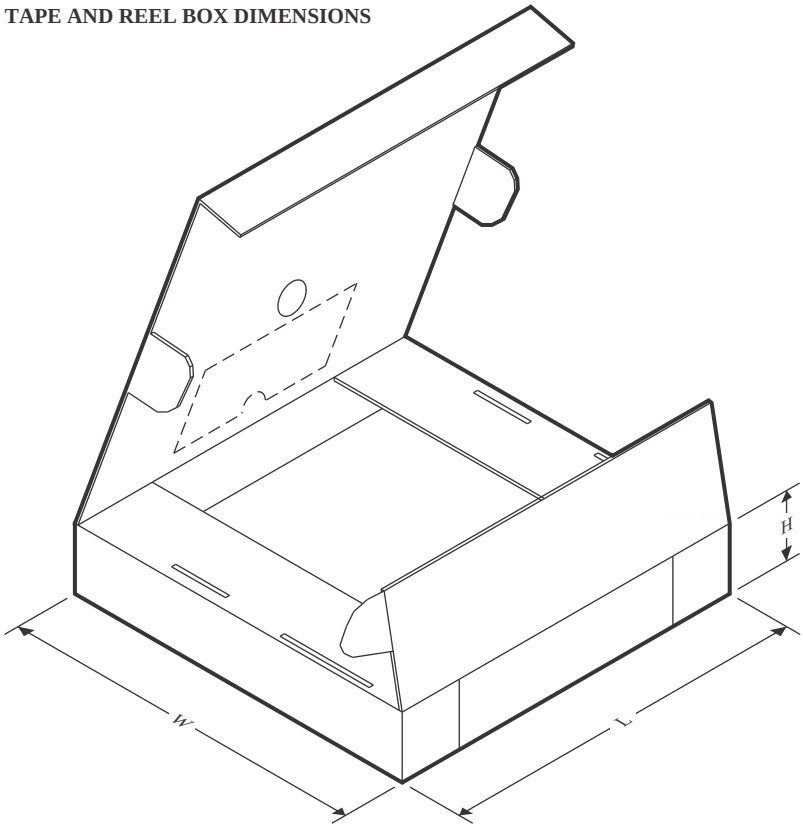
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25942ARVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25942ARVCRG4	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25942ARVCT	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25942LRVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25942LRVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25942LRVCT	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25942LRVCTG4	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25944ARVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25944ARVCRG4	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25944ARVCT	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25944LRVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25944LRVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25944LRVCRG4	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25944LRVCT	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



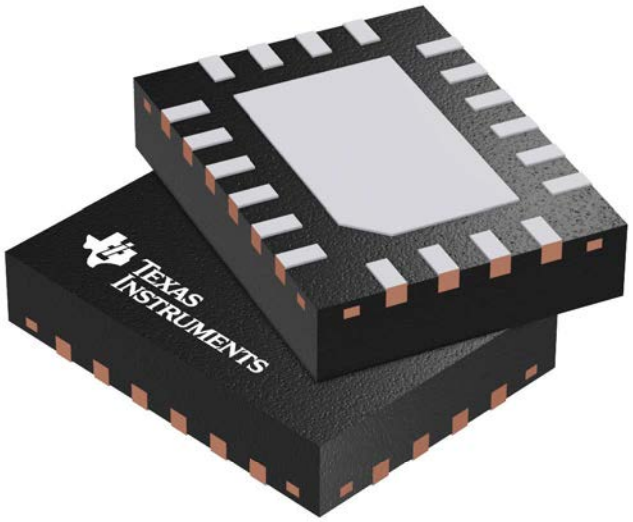
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25942ARVCR	WQFN	RVC	20	3000	346.0	346.0	33.0
TPS25942ARVCRG4	WQFN	RVC	20	3000	346.0	346.0	33.0
TPS25942ARVCT	WQFN	RVC	20	250	210.0	185.0	35.0
TPS25942LRVCR	WQFN	RVC	20	3000	346.0	346.0	33.0
TPS25942LRVCR	WQFN	RVC	20	3000	367.0	367.0	35.0
TPS25942LRVCT	WQFN	RVC	20	250	210.0	185.0	35.0
TPS25942LRVCTG4	WQFN	RVC	20	250	210.0	185.0	35.0
TPS25944ARVCR	WQFN	RVC	20	3000	346.0	346.0	33.0
TPS25944ARVCRG4	WQFN	RVC	20	3000	346.0	346.0	33.0
TPS25944ARVCT	WQFN	RVC	20	250	210.0	185.0	35.0
TPS25944LRVCR	WQFN	RVC	20	3000	367.0	367.0	35.0
TPS25944LRVCR	WQFN	RVC	20	3000	346.0	346.0	33.0
TPS25944LRVCRG4	WQFN	RVC	20	3000	346.0	346.0	33.0
TPS25944LRVCT	WQFN	RVC	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RVC 20 WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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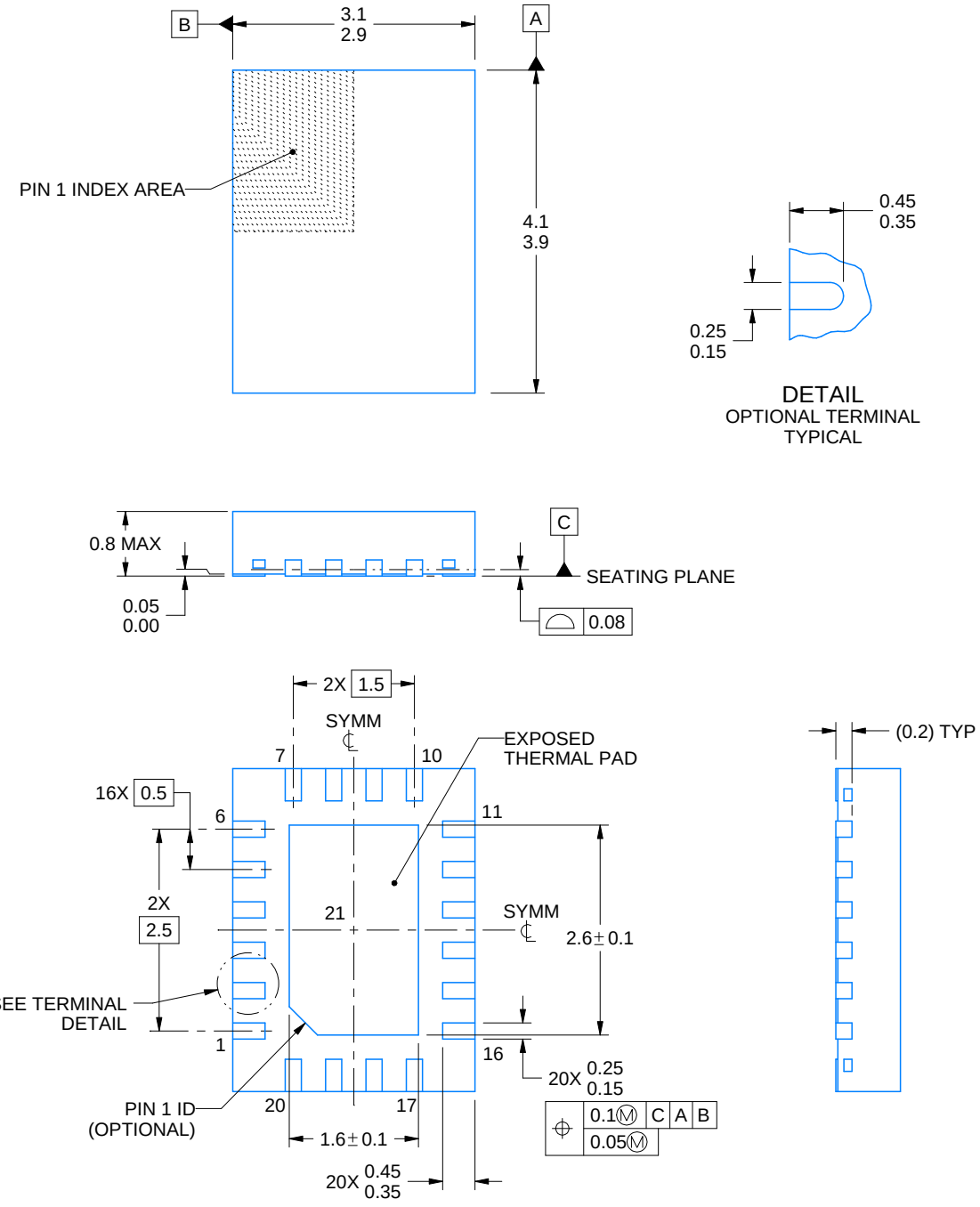
PACKAGE OUTLINE

RVC0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

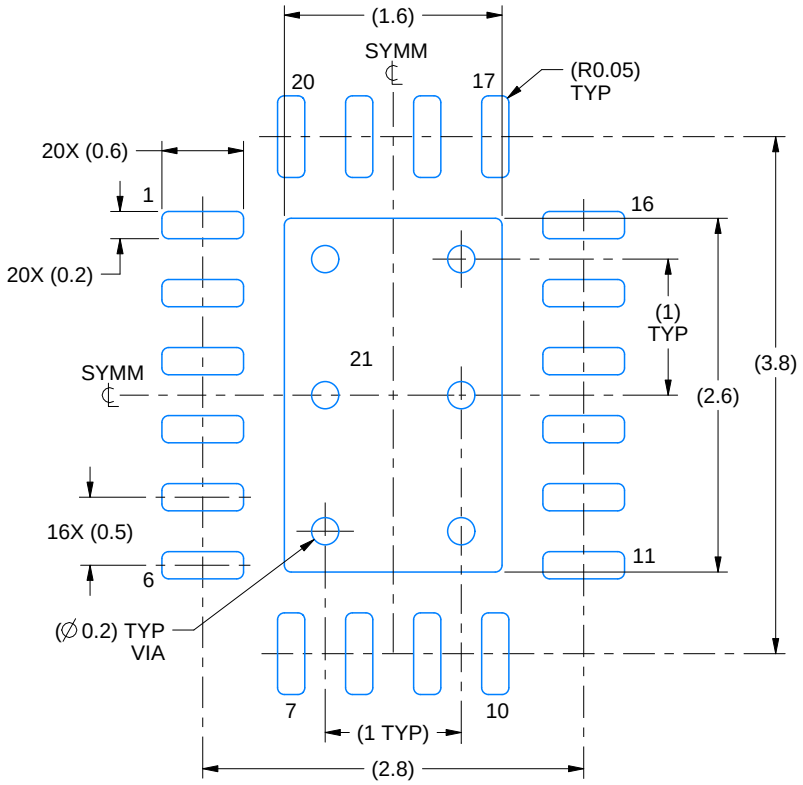
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

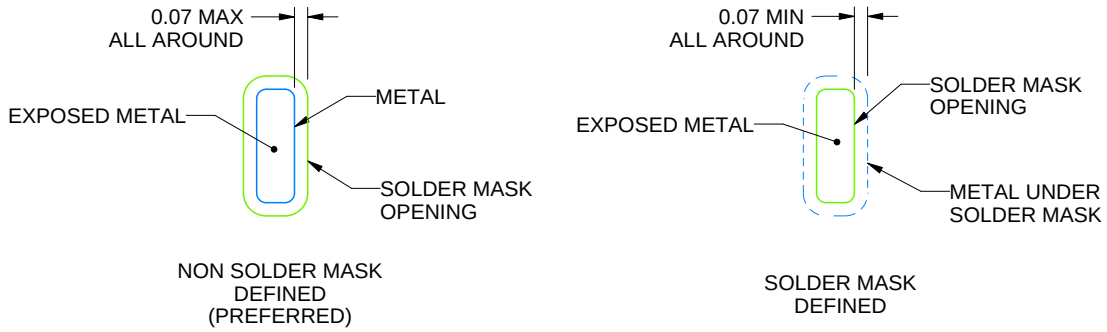
RVC0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

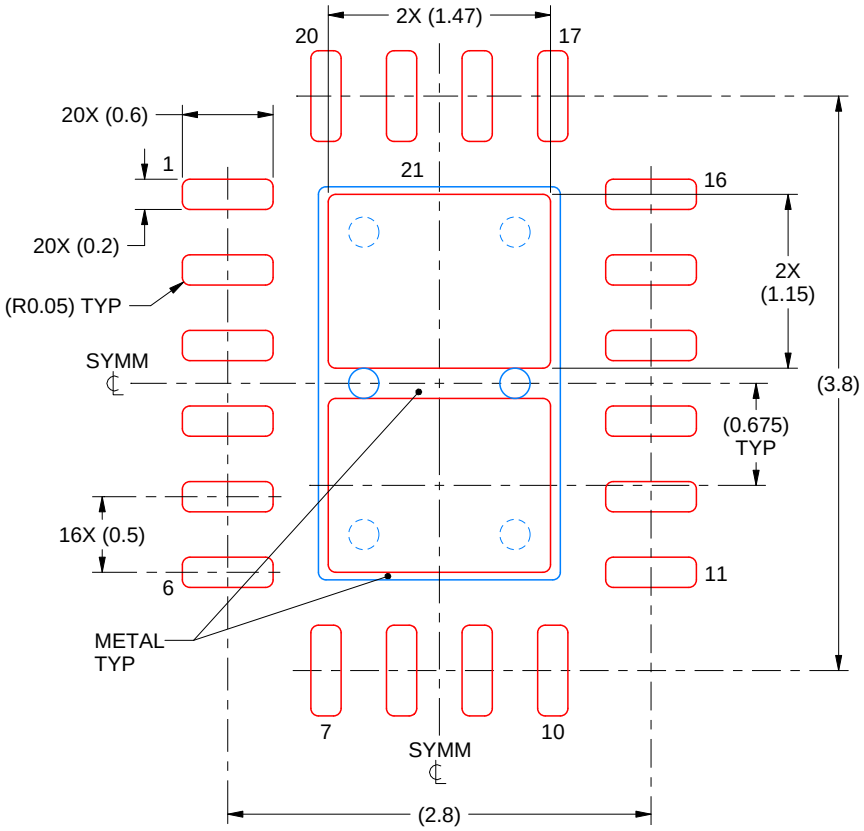
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RVC0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD X
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265