TPS25200-Q1 5-V eFuse With Precision Adjustable Current Limit and Overvoltage Clamp

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device HBM Classification Level 2
  - Device CDM Classification Level C5
- 2.5-V to 6.5-V Operation
- 20-V Continuous V_{IN} (Absolute Maximum)
- 7.6-V Input Overvoltage Shutoff
- 5.25-V to 5.55-V Fixed Overvoltge Clamp
- 0.6-µs Overvoltage Lockout Response
- 3.5-µs Short-Circuit Response
- 67-mΩ High-Side MOSFET
- Accurate 2.5-A Minimum, 2.9-A Maximum and 2.1-A Minimum, 2.5-A Maximum Setting (Including Resistor)
- ±6.3% Current-Limit Accuracy at 2.7 A
- Reverse Current Blocking While Disabled
- Built-in Soft Start
- Pin-to-Pin Compatible with TPS2553

2 Applications

- Automotive USB Port Protection
- USB Power Switch .
- USB Slave Devices

3 Description

The TPS25200-Q1 device is a 5-V eFuse with a precision current-limit and overvoltage clamp. The device provides robust protection for load and source during overvoltage and overcurrent events.

The TPS25200-Q1 device is an intelligent protected load-switch with a V_{IN} value tolerant to 20 V. In the event that an incorrect voltage is applied at the IN pin, the output clamps to 5.4 V to protect the load. If the voltage at the IN pin exceeds 7.6 V, the device disconnects the load to prevent damage to the device, load, or both.

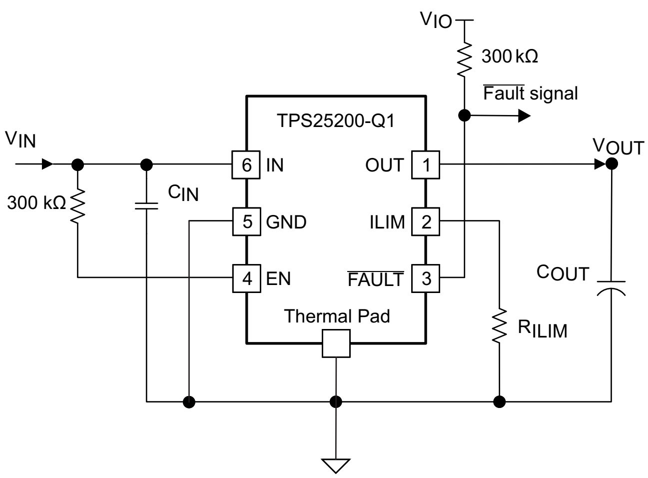
The TPS25200-Q1 device has an internal 67-mΩ power switch and is intended for protecting the source, device, and load under a variety of abnormal conditions. The device provides up to 2.4 A of continuous load current. The current-limit is programmable from 85 mA to 2.7 A with a single resistor to ground. During overload events, the output current is limited to the level set by the R_{ILIM} resistor. If a persistent overload occurs, the device eventually enters thermal shutoff to prevent damage to the TPS25200-Q1 device.

Device Information(1)

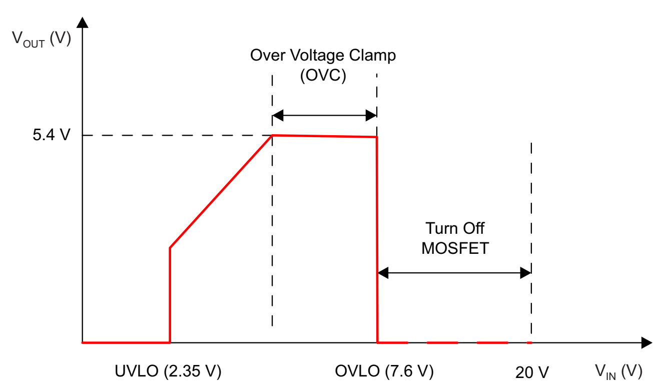
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25200-Q1	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



V_{OUT} vs V_{IN}



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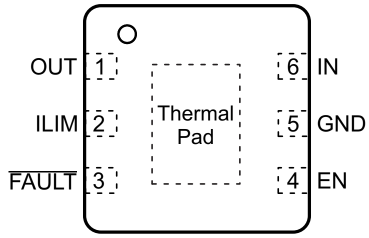
5 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

6 Pin Configuration and Functions

DRV Package
6-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	4	I	Logic-level control input. When this pin is driven high, the power switch is enabled. When this pin is driven low, the power switch turns off. This pin cannot be left floating and it must be limited below the absolute maximum rating if tied to the IN pin.
$\overline{FAULT}$	3	O	Active-low open-drain output. This pin is asserted during an overcurrent, overvoltage, or overtemperature event. Connect a pullup resistor to the logic I/O voltage.
GND	5	—	Ground connection. Connect this pin externally to the exposed thermal pad.
ILIM	2	O	External resistor. The ILIM pin is used to set the current-limit threshold. The recommended value for this pin is: 36 kΩ ≤ R_{ILIM} ≤ 1100 kΩ.
IN	6	I	Input voltage. Connect a ceramic capacitor with a value of 0.1 µF or greater from the IN pin to the GND pin as close to the IC as possible.
OUT	1	O	Protected power switch, V_{OUT}.
Thermal pad		—	The exposed thermal pad is internally connected to the GND pin. Use the thermal pad to heat-sink the device to the circuit board traces. Connect the thermal pad to the GND pin externally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	20	V
	OUT, EN, ILIM, $\overline{FAULT}$	–0.3	7	V
	From IN to OUT	–7	20	V
Continuous output current, I_O		Thermally Limited		
Continuous $\overline{FAULT}$ output sink current			25	mA
Continuous ILIM output source current			150	µA
Operating junction temperature, T_J		Internally limited		
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage of IN	2.5	6.5	V
V_{EN}	Enable pin voltage	0	6.5	V
$I_{\overline{FAULT}}$	Continuous $\overline{\text{FAULT}}$ sink current	0	10	mA
I_{OUT}	Continuous output current of OUT		2.4	A
R_{ILIM}	Current-limit set resistors	36	1100	kΩ
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC (1)		DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	
ψ_{JT}	Junction-to-top characterization parameter	1.6	
ψ_{JB}	Junction-to-board characterization parameter	36.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Conditions are –40°C ≤ T_J ≤ 125°C and 2.5 V ≤ V_{IN} ≤ 6.5 V. V_{EN} = V_{IN}, R_{ILIM} = 36 kΩ. Positive current into pins. Typical value is at 25°C. All voltages are with respect to ground (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	IN–OUT resistance(1)	2.5 V ≤ V_{IN} ≤ 5 V, I_{OUT} = 2.4 A	T_J = 25°C		67	75	mΩ
			–40°C ≤ T_J ≤ 85°C		67	95	
			–40°C ≤ T_J ≤ 125°C		67	105	
ENABLE INPUT EN							
	EN pin turn on threshold	Input rising				1.9	V
	EN pin turn off threshold	Input falling		0.6			V
	Hysteresis				330(2)		mV
I_{EN}	Leakage current	V_{EN} = 0 V or 5.5 V		–2		2	µA
DISCHARGE							
R_{DCHG}	OUT Discharge Resistance	V_{OUT} = 5 V, V_{EN} = 0 V			500	625	Ω
CURRENT LIMIT							
I_{OS}	Current-limit, see Figure 12	R_{ILIM} = 36 kΩ		2530	2700	2870	mA
		R_{ILIM} = 42.2 kΩ		2140	2300	2460	
		R_{ILIM} = 56 kΩ		1620	1740	1860	
		R_{ILIM} = 80.6 kΩ		1110	1206	1300	
		R_{ILIM} = 150 kΩ		590	647	710	
		R_{ILIM} = 1100 kΩ		40	83	130	
OVERVOLTAGE LOCKOUT, IN							
$V_{(OVLO)}$	IN rising OVLO threshold voltage	IN rising		6.8	7.6	8.45	V
	Hysteresis				70(2)		mV
VOLTAGE CLAMP, OUT							
$V_{(OVC)}$	OUT clamp voltage threshold	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 6.5 V		5.25	5.4	5.55	V
SUPPLY CURRENT							
$I_{IN(off)}$	Supply current, low-level output	V_{EN} = 0 V, V_{IN} = 5 V			1	5	µA
		V_{EN} = 0 or 5 V, V_{IN} = 20 V			1040	1700	
$I_{IN(on)}$	Supply current, high-level output	V_{IN} = 5 V, No load on OUT	R_{ILIM} = 36 kΩ		147	200	µA
			R_{ILIM} = 150 kΩ		120	190	
I_{REV}	Reverse leakage current	V_{OUT} = 6.5V, V_{IN} = V_{EN} = 0 V, T_J = 25°C, Measure I_{OUT}			3.2	5	µA
UNDERVOLTAGE LOCKOUT, IN							
V_{UVLO}	IN rising UVLO threshold voltage	IN rising			2.35	2.45	V
	Hysteresis				30(2)		mV
$\overline{\text{FAULT}}$ FLAG							
V_{OL}	Output low voltage, $\overline{\text{FAULT}}$	$I_{\overline{FAULT}}$ = 1 mA			50	180	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 6.5 V				1	µA
THERMAL SHUTDOWN							
	Thermal shutdown threshold, OTSD2(3)			155			°C
	Thermal shutdown threshold only in current-limit, OTSD1(3)			135			
	Hysteresis				20(2)		

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) These parameters are provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) For more information on the thermal sensors, OTSD1 and OTSD2, see the *Thermal Sense* section.

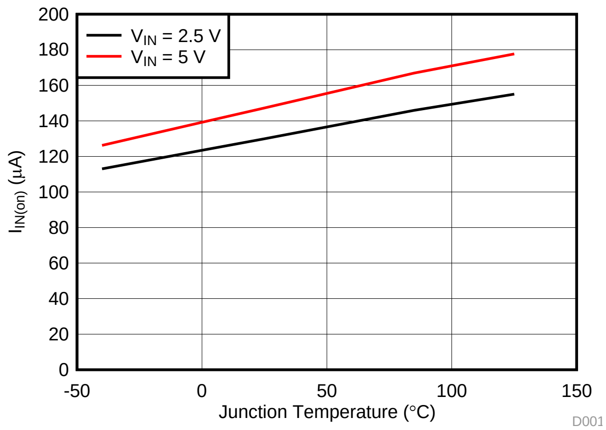
7.6 Switching Characteristics

Conditions are –40°C ≤ T_J ≤ 125°C and 2.5 V ≤ V_{IN} ≤ 6.5 V. V_{EN} = V_{IN}, R_{ILIM} = 36 kΩ. Positive current are into pins. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
t_r	OUT voltage rise time	C_L = 1 µF, R_L = 100 Ω, (see Figure 10)		2.05	3.2	ms
t_f	OUT voltage fall time	C_L = 1 µF, R_L = 100 Ω, (see Figure 10)		0.18	0.2	ms
ENABLE INPUT EN						
t_{on}	Turn-on time	2.5 V ≤ V_{IN} ≤ 5 V, C_L = 1 µF, R_L = 100 Ω, (see Figure 10)		5.12	7.3	ms
t_{off}	Turn-off time	2.5 V ≤ V_{IN} ≤ 5 V, C_L = 1 µF, R_L = 100 Ω, (see Figure 10)		0.22	0.3	ms
CURRENT LIMIT						
$t_{(IOS)}$	Short-circuit response time	V_{IN} = 5 V (see Figure 12)		3.5[(1)]		µs
OVERVOLTAGE LOCKOUT, IN						
$t_{(OVLO\_off\_delay)}$	Turn-off Delay for OVLO	V_{IN} = 5 V to 10 V with 1 V/µs ramp-up rate, V_{OUT} with 100-Ω load		0.6[(1)]		µs
$\overline{\text{FAULT}}$ FLAG						
	$\overline{\text{FAULT}}$ deglitch	$\overline{\text{FAULT}}$ assertion or deassertion because of overcurrent condition	5	8	12	ms

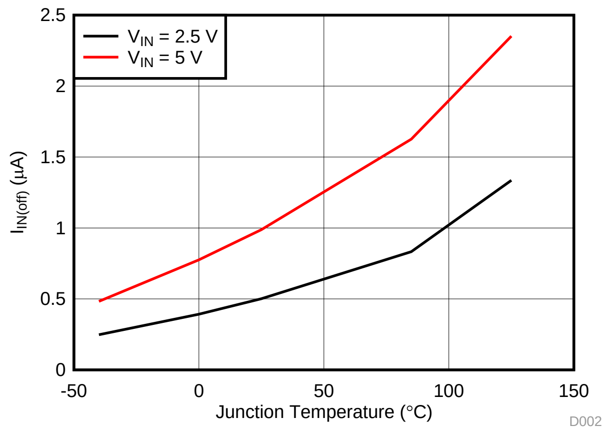
(1) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.7 Typical Characteristics



R_{ILIM} = 36 KΩ

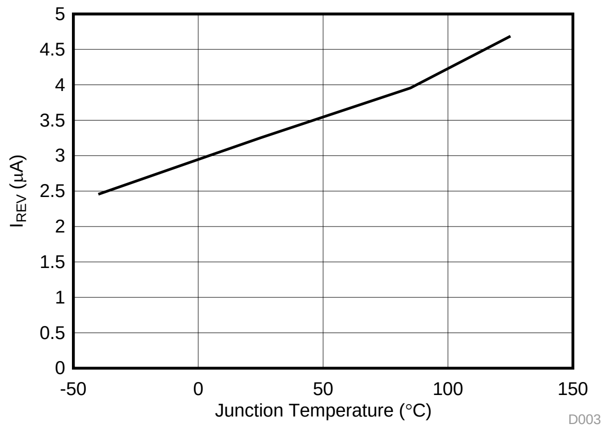
Figure 1. $I_{IN(on)}$ vs Junction Temperature



R_{ILIM} = 36 KΩ

Figure 2. $I_{IN(off)}$ vs Junction Temperature

Typical Characteristics (continued)



$V_{EN} = V_{IN} = 0$ V $V_{OUT} = 6.5$ V

Figure 3. I_{REV} vs Junction Temperature

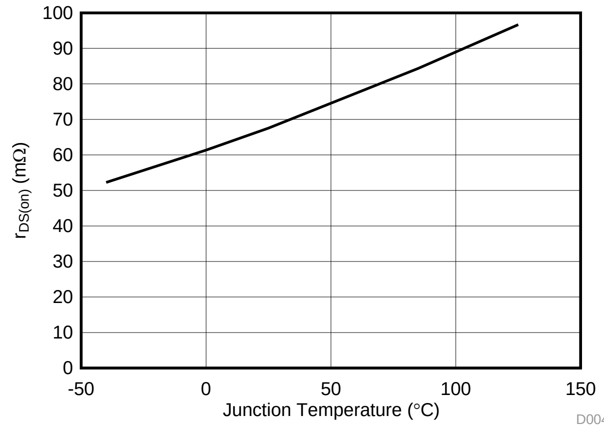


Figure 4. $r_{DS(ON)}$ vs Junction Temperature

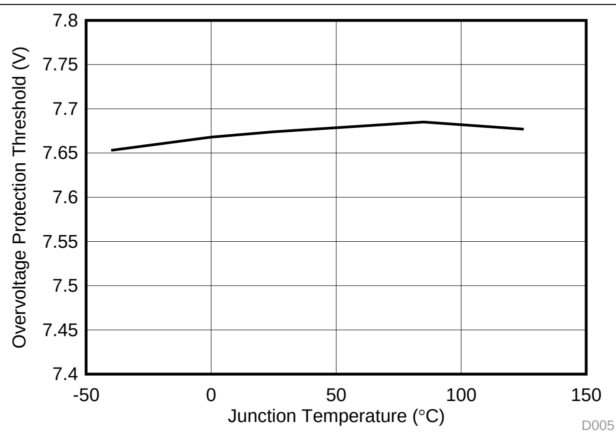
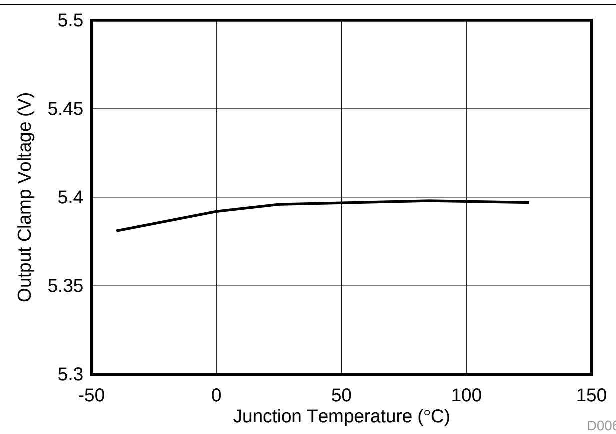


Figure 5. $V_{(OVLO)}$ vs Junction Temperature



$C_L = 1$ µF $R_L = 100$ Ω $V_{IN} = 6.5$ V

Figure 6. $V_{O(VC)}$ vs Junction Temperature

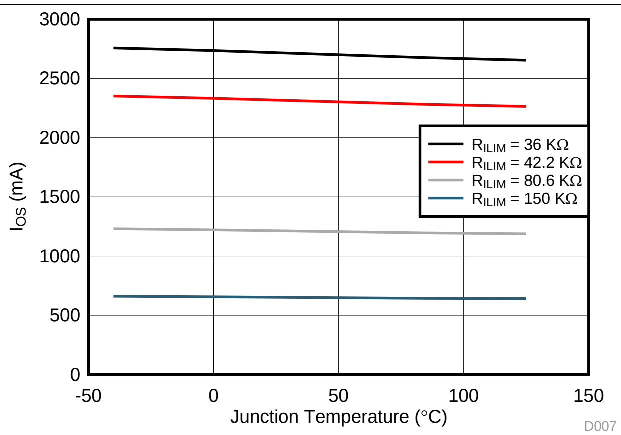


Figure 7. I_{OS} vs Junction Temperature

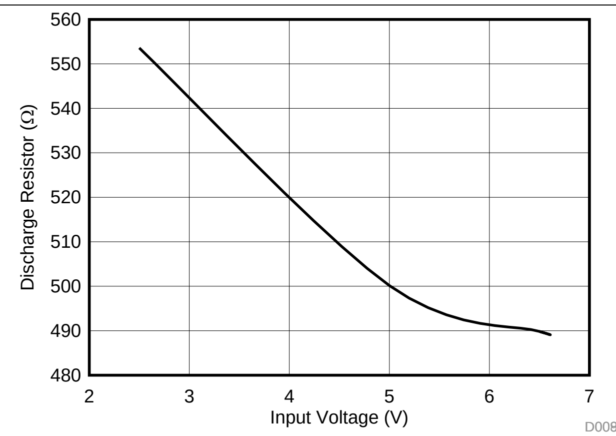


Figure 8. Discharge Resistance vs V_{IN}

8 Parameter Measurement Information

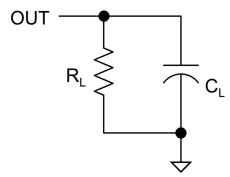


Figure 9. Output Rise and Fall Test Load

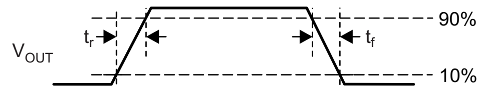


Figure 10. Power-On and Off Timing

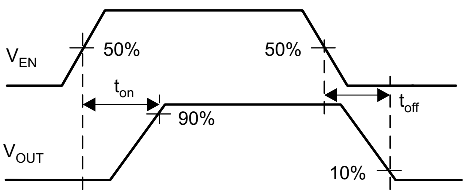


Figure 11. Enable Timing, Active High Enable

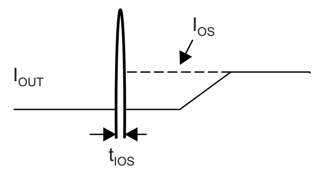


Figure 12. Output Short Circuit Parameters

9 Detailed Description

9.1 Overview

The TPS25200-Q1 device is an intelligent low-voltage switch or e-Fuse with robust overcurrent and overvoltage protection which are suitable for a variety of applications.

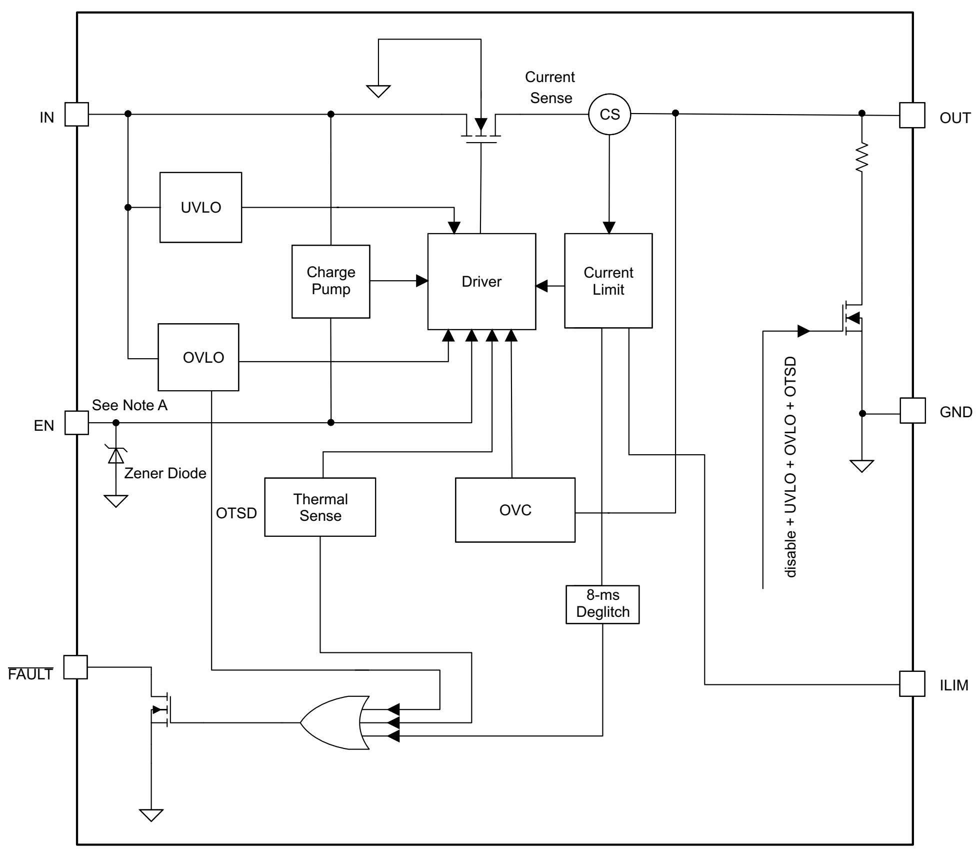
The TPS25200-Q1 current-limited power switch uses N-channel MOSFETs in applications requiring up to 2.4 A of continuous load current. The device allows the user to program the current-limit threshold between 85 mA and 2.7 A (typical) through an external resistor. The device enters constant-current mode when the load exceeds the current-limit threshold.

The TPS25200-Q1 input can withstand 20-V DC voltage, but clamps V_{OUT} to a precision regulated 5.4 V and shuts down in the event that the V_{IN} value exceeds 7.6 V. The device also integrates overcurrent and short-circuit protection. The precision overcurrent limit helps minimize over designing of the input power supply while the fast response short-circuit protection isolates the load when a short circuit is detected.

The additional features of the device include the following:

- Overtemperature protection to safely shutdown in the event of an overcurrent event or a slight overvoltage event where the V_{OUT} clamp is engaged over an extended period of time.
- Deglitched fault reporting to filter the $\overline{\text{FAULT}}$ signal to ensure that the TPS25200-Q1 device does not provide false-fault alerts.
- Output discharge pulldown to ensue a load is off and not in an undefined operational state.
- Reverse blocking when disabled to prevent back-drive from an active load which inadvertently causes undetermined behavior in the application.

9.2 Functional Block Diagram



A. 6.4-V typical clamp voltage

9.3 Feature Description

9.3.1 Enable

This logic enable input controls the power switch and device supply current. A logic-high input on the EN pin enables the driver, control circuits, and powers the switch. The enable input is compatible with both TTL and CMOS logic levels.

The EN pin can be tied to V_{IN} with a pullup resistor, and is protected with an integrated Zener diode. Use a sufficiently large (300 kΩ) pullup resistor to ensure that $V_{(EN)}$ is limited below the absolute maximum rating.

9.3.2 Thermal Sense

The TPS25200-Q1 device uses two independent thermal sensing circuits for self protection that monitor the operating temperature of the power switch and disable operation if the temperature exceeds the values listed in the *Recommended Operating Conditions* table. The TPS25200-Q1 device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across the power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD1) turns off the power switch when the die temperature exceeds 135°C (minimum) and the device is in current-limit protection. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled by approximately 20°C.

The TPS25200-Q1 device also has a second ambient thermal sensor (OTSD2). The thermal sensor turns off the power switch when the die temperature exceeds 155°C (minimum) regardless of whether the power switch is in current-limit protection and turns on the power switch after the device has cooled by approximately 20°C. The TPS25200-Q1 device continues to cycle off and on until the fault is removed.

9.3.3 Overcurrent Protection

The TPS25200-Q1 device initiates thermal protection by thermal cycling during an extended overcurrent condition. The device turns off when the junction temperature exceeds 135°C (typical) while in current limit. The device remains off until the junction temperature cools by 20°C (typical) and then restarts. The TPS25200-Q1 device cycles on and off until the overload is removed (see Figure 26 and Figure 29).

The TPS25200-Q1 device responds to an overcurrent condition by limiting the output current to the I_{OS} levels shown in Figure 12. When an overcurrent condition is detected, the device maintains a constant output current and the output voltage is reduced accordingly. During an overcurrent event, two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered up or enabled. The output voltage is held near zero potential with respect to ground and the TPS25200-Q1 device ramps the output current to the I_{OS} level. The TPS25200-Q1 device limits the current to the I_{OS} level until the overload condition is removed or the device begins a thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within the time, t_{IOS} (see Figure 12). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to the I_{OS} level. Similar to the previous case, the TPS25200-Q1 device limits the current to the I_{OS} level until the overload condition is removed or the device begins a thermal cycle.

9.3.4 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent, overtemperature, or overvoltage condition. The TPS25200-Q1 device asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS25200-Q1 device is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay *deglitch* circuit for overcurrent (8-ms typical) conditions without the requirement for external circuitry. This design ensures that the $\overline{\text{FAULT}}$ signal is not accidentally asserted because of normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions.

Feature Description (continued)

The FAULT signal is not deglitched when the MOSFET is disabled because of an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents FAULT oscillation during an overtemperature event.

The FAULT signal is not deglitched when the MOSFET is disabled into overvoltage-lockout (OVLO) or out of OVLO. The TPS25200-Q1 device does not assert the FAULT during output-voltage clamp mode.

Connect the FAULT pin with a pullup resistor to a low-voltage I/O rail.

9.3.5 Output Discharge

A 480-Ω (typical) output discharge dissipates the stored charge and leakage current on the OUT pin when the TPS25200-Q1 device is in undervoltage-lockout (UVLO) or OVLO or is disabled. The pulldown capability decreases as V_{IN} decreases (see Figure 8).

9.4 Device Functional Modes

The input voltage of the TPS25200-Q1 device can withstand up to 20 V. The input voltage, within a range of 0 V to 20 V, can be divided to four modes which are described in the following sections.

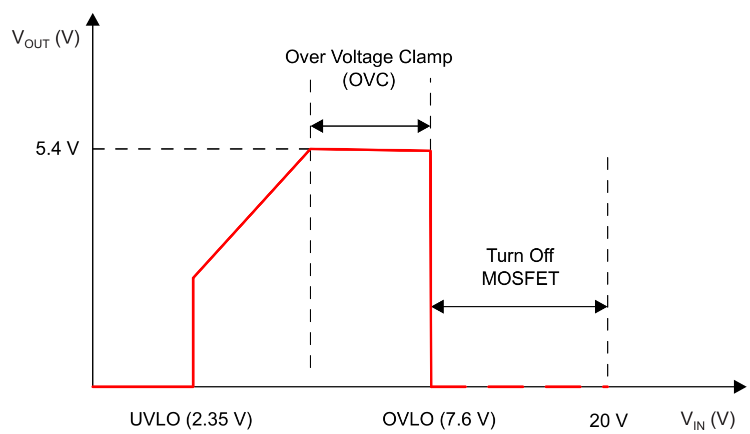


Figure 13. Output vs Input Voltage

9.4.1 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on and off cycling because of input voltage droop during turn on.

9.4.2 Overcurrent Protection (OCP)

When 2.35 V < V_{IN} < 5.4 V, the TPS25200-Q1 device is a traditional power switch that provides overcurrent protection.

9.4.3 Overvoltage Clamp (OVC)

When 5.4 V < V_{IN} < 7.6 V, the overvoltage-clamp (OVC) circuit clamps the output voltage to 5.4 V. Within this V_{IN} range, the overcurrent protection remains active. Fast transients can exceed the bandwidth of the internal gate-control amplifier but such events will not risk damage to the load. In the unlikely event that a transient is fast enough to exceed the amplifier bandwidth but not severe enough to exceed 7.6 V, it may cause momentary droops in V_{OUT} while the amplifier catches up and settles on V_{OUT} = 5.4 V. For example, a 5-V to 7-V transient with 0.5-V/ms slew rate and with 2 × 47 µF // 100-Ω load, some drooping occurs at V_{OUT}.

9.4.4 Overvoltage Lockout (OVLO)

When V_{IN} exceeds 7.6 V, the overvoltage lockout (OVLO) circuit turns off the protected power switch.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS25200-Q1 device is a 5-V eFuse with precision current-limit and overvoltage clamp. When a slave device such as a mobile data-card device is hot plugged into a USB port as shown in Figure 14, an input transient voltage could damage the slave device because of the cable inductance. Placing the TPS25200-Q1 device at the input of a mobile device as an overvoltage and overcurrent protector can help safeguard the slave device. Input transients also occur when the current through the cable parasitic inductance changes abruptly which can occur when the TPS25200-Q1 device turns off the internal MOSFET in response to an overvoltage or overcurrent event. The TPS25200-Q1 device can withstand the transient without a bypass bulk capacitor, or other external overvoltage protection components at the input side. The TPS25200-Q1 device also can be used at the host side as a traditional power switch that is pin-to-pin compatible with the TPS2553 device.

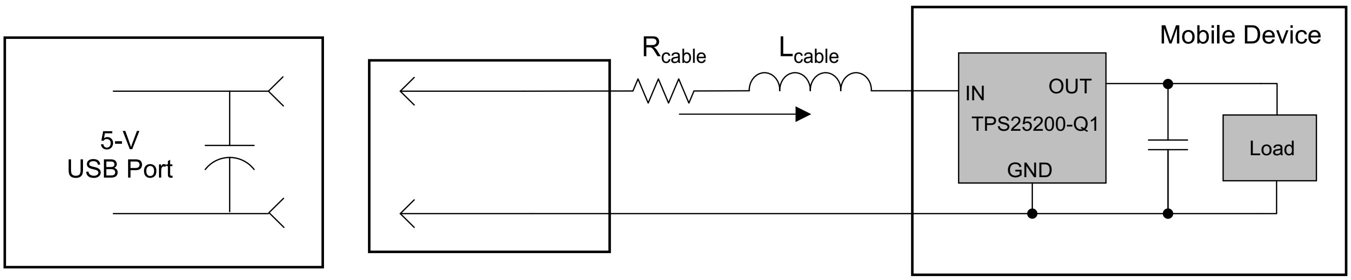


Figure 14. Hot Plug into 5-V USB Port With Parasitic Cable Resistance and Inductance

10.2 Typical Application

10.2.1 Overvoltage and Overcurrent Protector

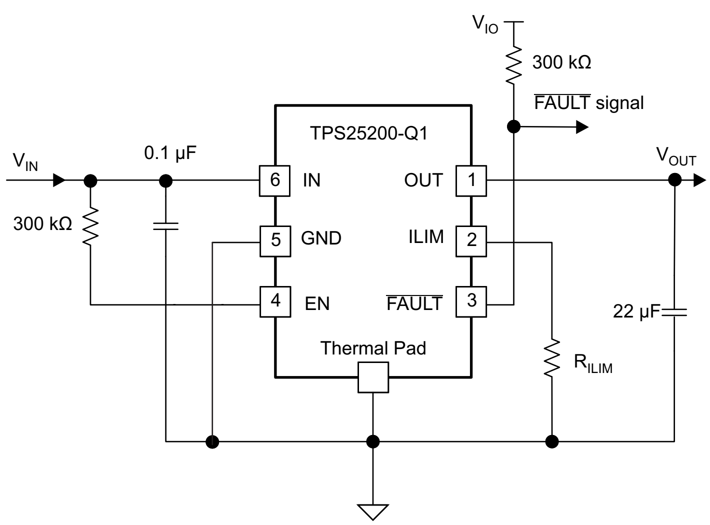


Figure 15. Typical Application Schematic

Use the I_{OS} level listed in the *Electrical Characteristics* table or the I_{OS} value in the Equation 1 to select the value of R_{ILIM}.

Typical Application (continued)

10.2.1.1 Design Requirements

For this design example, use the values listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Normal input operation voltage	5 V
Output transient voltage	6.5 V
Minimum current limit	2.1 A
Maximum current limit	2.9 A

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Step by Step Design Produce

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal Input Operation Voltage
- Output transient voltage
- Minimum Current Limit
- Maximum Current Limit

10.2.1.2.2 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a ceramic bypass capacitor with a value of 0.1 µF or greater is recommended between the IN and GND pins. This capacitor should be placed as close to the device as possible for local noise decoupling.

When V_{IN} ramp up exceeds 7.6 V, V_{OUT} follows V_{IN} until the TPS25200-Q1 device turns off the internal MOSFET after $t_{(OVLO\_off\_delay)}$. Because $t_{(OVLO\_off\_delay)}$ largely depends on the V_{IN} ramp rate, V_{OUT} receives some peak voltage. Increasing the output capacitance can lower the output peak voltage as shown in Figure 16.

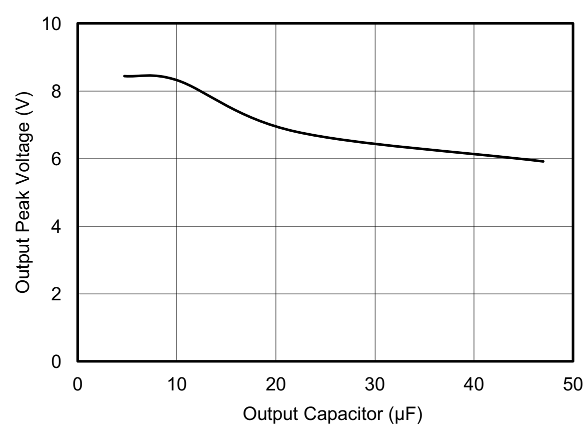


Figure 16. V_{OUT} Peak Voltage vs C_{OUT}
(V_{IN} Step From 5 V to 15 V With 1-V/us Ramp-Up Rate)

10.2.1.2.3 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable through an external resistor. The TPS25200-Q1 device uses an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of the ILIM pin. The recommended 1% resistor range for R_{ILIM} is 36 kΩ ≤ R_{ILIM} ≤ 1100 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level. Therefore, considering the tolerance of the overcurrent threshold is important when selecting a value for R_{ILIM}. The following equations approximate the resulting overcurrent threshold for a given external resistor value, R_{ILIM}. See the *Electrical Characteristics* table for specific current-limit settings. The traces routing the R_{ILIM} resistor to the TPS25200-Q1 device should be as short as possible to reduce parasitic effects on the current-limit accuracy.

R_{ILIM} can be selected to provide a current-limit threshold that occurs either above a minimum load current or below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the minimum desired load current on the $I_{OS(min)}$ curve. Select a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads.

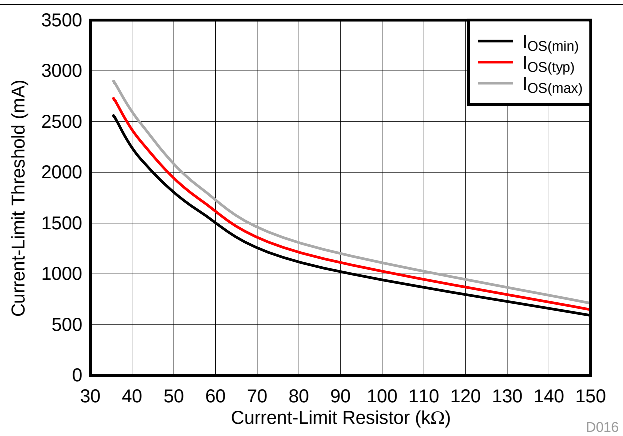
To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve. Select a value of R_{ILIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting the upstream power supplies which causes the input voltage bus to droop.

Use Equation 1, Equation 2, and Equation 3, to calculate the minimum, nominal, and maximum current-limit thresholds for I_{OS} (respectively). For each equation, 36 kΩ ≤ R_{ILIM} ≤ 1100 kΩ.

$$I_{OSmin}\,(mA) = \frac{97399\,(V)}{R_{ILIM}^{\;1.015}\,(k\Omega)} - 30 \quad (1)$$

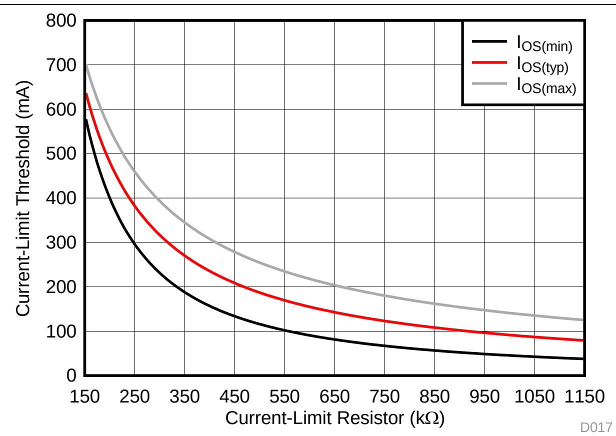
$$I_{OSnom}\,(mA) = \frac{98322\,(V)}{R_{ILIM}^{\;1.003}\,(k\Omega)} \quad (2)$$

$$I_{OSmax}\,(mA) = \frac{96754\,(V)}{R_{ILIM}^{\;0.985}\,(k\Omega)} + 30 \quad (3)$$



36 kΩ ≤ R_{ILIM} ≤ 150 KΩ

Figure 17. Current-Limit Threshold vs R_{ILIM} I



150 kΩ ≤ R_{ILIM} ≤ 1100 KΩ

Figure 18. Current-Limit Threshold vs R_{ILIM} II

10.2.1.2.4 Design Above a Minimum Current Limit

Some applications require that current limiting does not occur below a certain threshold. For this example, assume that 2.1 A must be delivered to the load so that the minimum desired current-limit threshold is 2100 mA. Use Equation 1 and Figure 17 to select a value for R_{ILIM}, with I_{OSmin} = 2100 mA, as shown in Equation 4.

$$R_{ILIM}\ (k\Omega) = \left(\frac{97399}{I_{OS(min)} + 30}\right)^{\frac{1}{1.015}} = \left(\frac{97399}{2100 + 30}\right)^{\frac{1}{1.015}} = 43.22\ k\Omega \tag{4}$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 42.2 kΩ. This value sets the minimum current-limit threshold at 2130 mA as shown in Equation 5.

$$I_{OSmin}\ (mA) = \frac{97399\ (V)}{R_{ILIM}^{1.015}\ (k\Omega)} - 30 = \frac{97399}{(42.2 \times 1.01)^{1.015}} - 30 = 2130\ mA \tag{5}$$

Use Equation 3, Figure 17, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold as shown in Equation 6.

$$I_{OSmax}\ (mA) = \frac{96754}{(42.2 \times 0.99)^{0.985}} + 30 = 2479\ mA \tag{6}$$

The resulting current-limit threshold minimum is 2130 mA and maximum is 2479 mA with R_{ILIM} = 42.2kΩ ± 1%.

10.2.1.2.5 Design Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that 2.9 A must be delivered to the load so that the minimum desired current-limit threshold is 2900 mA. Use Equation 3 and Figure 18 to select R_{ILIM}.

$$IR_{ILIM}\ (k\Omega) = \left(\frac{96754}{I_{OS(max)} - 30}\right)^{\frac{1}{0.985}} = \left(\frac{96754}{2900 - 30}\right)^{\frac{1}{0.985}} = 35.57\ k\Omega \tag{7}$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 36 kΩ. This value sets the maximum current-limit threshold at 2894 mA as shown in Equation 8.

$$I_{OSmax}\ (mA) = \frac{96754\ (V)}{R_{ILIM}^{0.985}\ (k\Omega)} + 30 = \frac{96754}{(36 \times 0.99)^{0.985}} + 30 = 2894\ mA \tag{8}$$

Use Equation 1, Figure 18, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold as shown in Equation 9.

$$I_{OSmin}\ (mA) = \frac{97399}{(36 \times 1.01)^{1.015}} - 30 = 2508\ mA \tag{9}$$

The resulting minimum current-limit threshold minimum is 2592 mA and maximum is 2894 mA with R_{ILIM} = 36 kΩ ± 1%.

10.2.1.2.6 Power Dissipation and Junction Temperature

The low on-resistance of the internal N-channel MOSFET allows small surface-mount packages to pass large currents. Estimating the power dissipation and junction temperature is good design practice. The following analysis provides an approximation for calculating the junction temperature based on the power dissipation of the package.

NOTE

Thermal analysis is strongly dependent on additional system-level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system-level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ value of the N-channel MOSFET relative to the input voltage (V_{IN}) and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 4 in the *Typical Characteristics* section. When V_{IN} is lower than $V_{(OVC)}$, the TPS25200-Q1 device is an traditional power switch. Using this value, calculate the power dissipation with Equation 10.

$$P_D = r_{DS(on)} \times I_{OUT}^2$$

where

- P_D = Total power dissipation (W)
- $r_{DS(on)}$ = Power switch on-resistance (Ω)
- I_{OUT} = Maximum current-limit threshold (A) (10)

When V_{IN} exceeds $V_{(OVC)}$, but is lower than $V_{(OVLO)}$, the TPS25200-Q1 clamp output is fixed to $V_{(OVC)}$. Use Equation 11 to calculate the power dissipation.

$$P_D = (V_{IN} - V_{(OVC)}) \times I_{OUT}$$

where

- $V_{(OVC)}$ = Overvoltage clamp voltage (V) (11)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature using Equation 12.

$$T_J = P_D \times R_{\theta JA} + T_A$$

where

- $R_{\theta JA}$ = Thermal resistance (°C/W)
- T_A = Ambient temperature (°C) (12)

Compare the calculated junction temperature with the initial estimate. If these two values are not within a few degrees, repeat the calculation using the *refined* $r_{DS(on)}$ value from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance $R_{\theta JA}$, and the thermal resistance is highly dependent on the individual package and board layout.

10.2.1.3 Application Curves

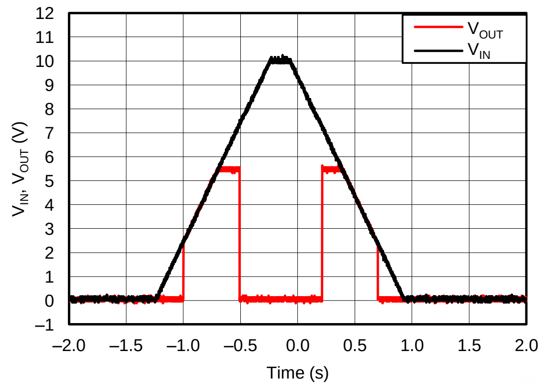


Figure 19. V_{OUT} vs V_{IN} (0 V to 10 V)

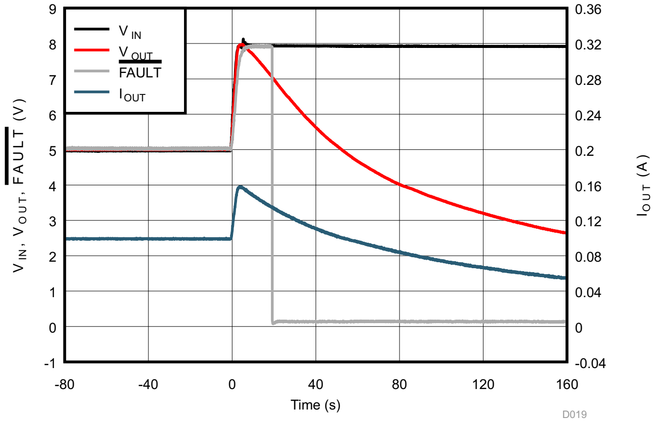


Figure 20. V_{IN} Step, 5 V to 8 V With 4.7 µF || 100 Ω

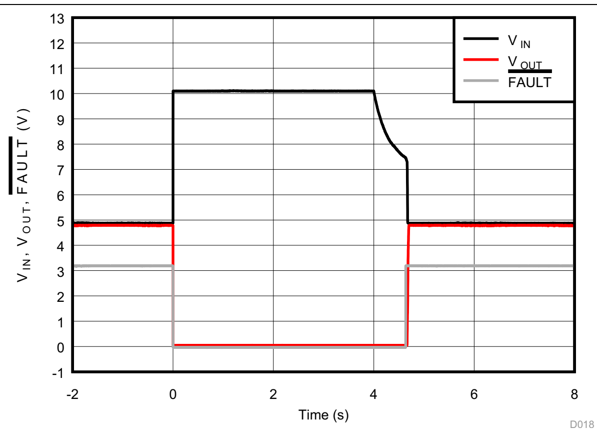


Figure 21. Pulse Overvoltage With 100 Ω

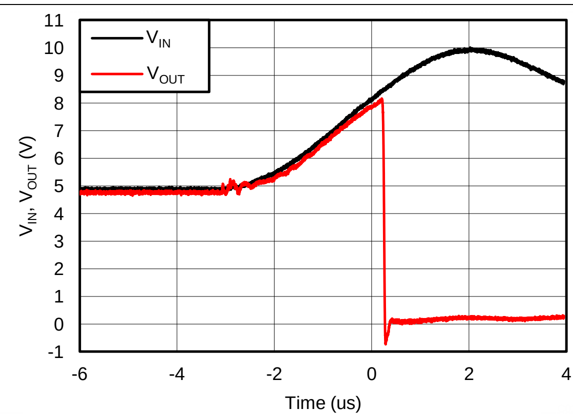


Figure 22. 5-V to 10-V OVLO Response Time

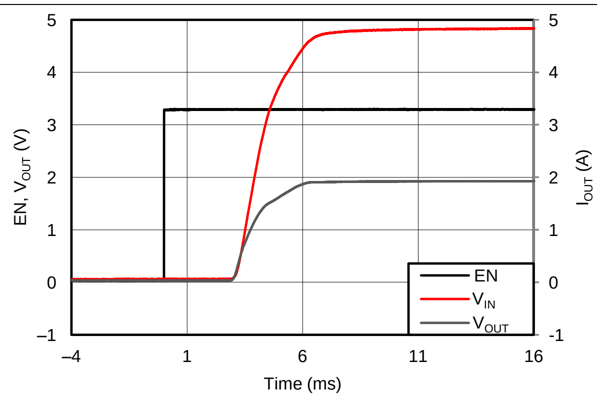


Figure 23. Turn On Delay and Rise Time, 150 µF || 2.5 Ω

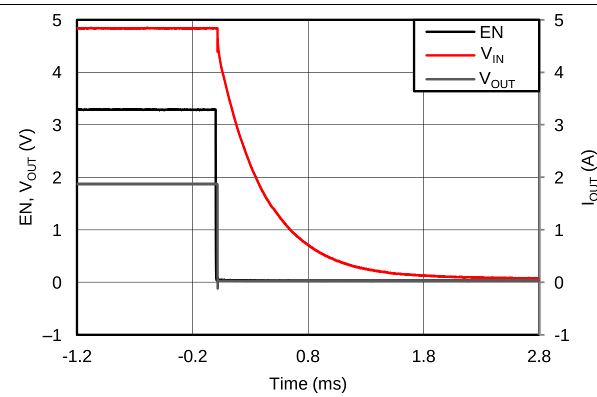


Figure 24. Turn Off Delay and Fall Time, 150 µF || 2.5 Ω

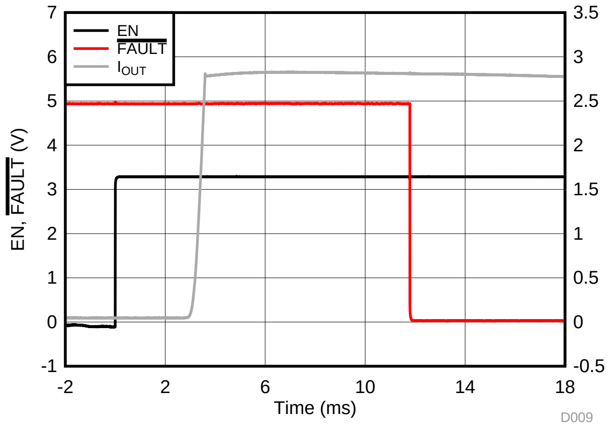


Figure 25. Enable into Output Short

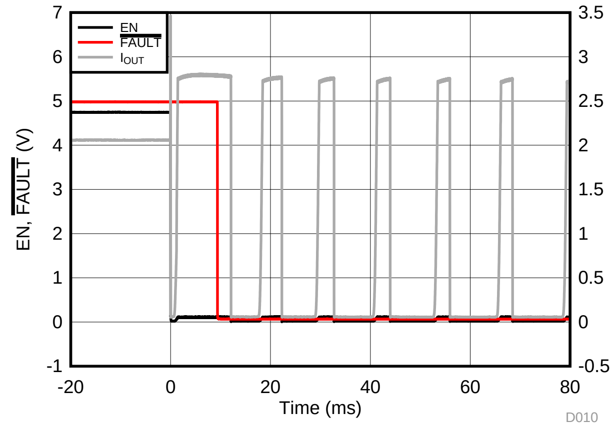


Figure 26. 2.5-Ω to Output Short Transient Response

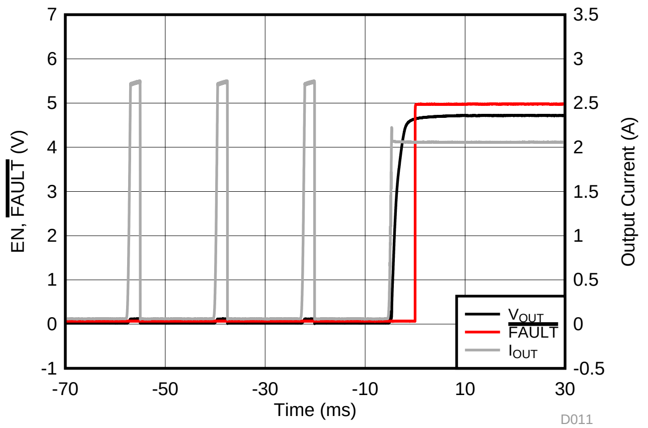


Figure 27. Output Short to 2.5-Ω Load Recovery Response

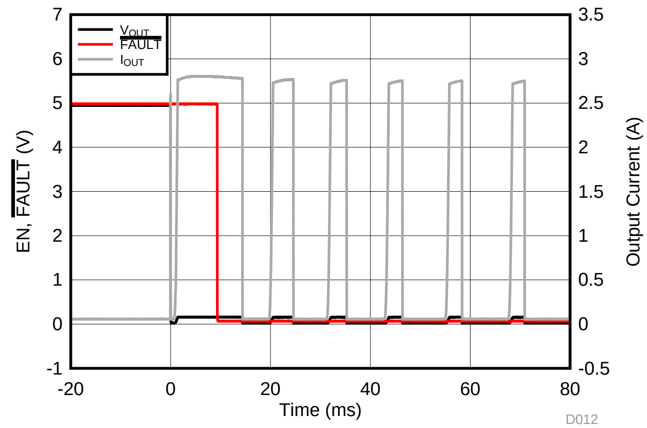


Figure 28. No Load to Output Short-Transient Response

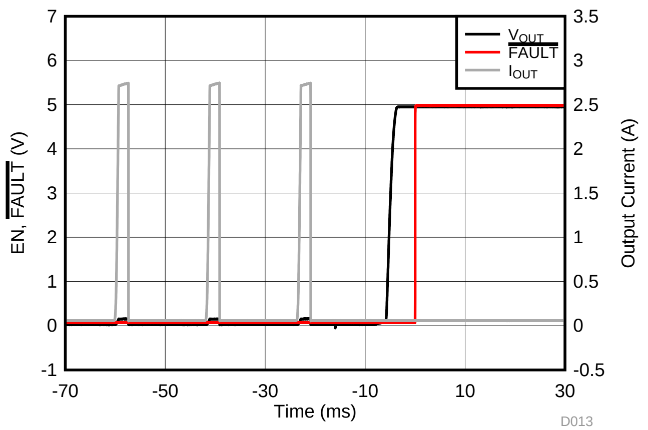


Figure 29. Output Short to No-Load Recovery Response

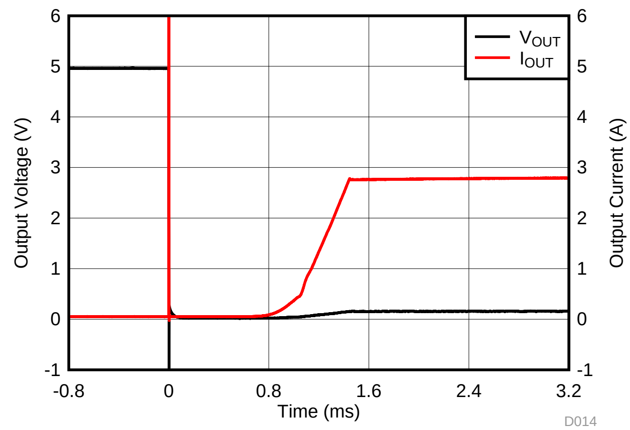


Figure 30. Hot-Short With 50 mΩ

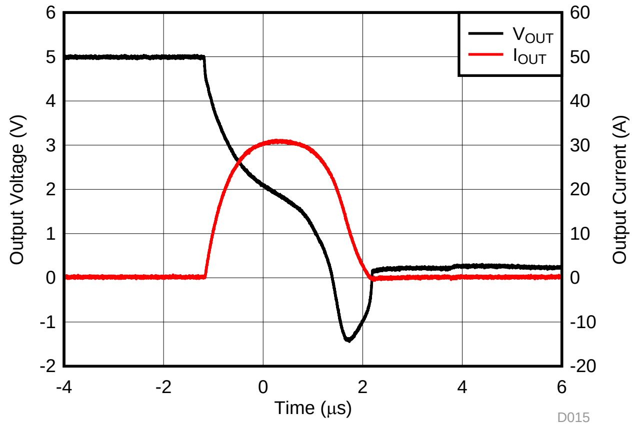


Figure 31. 50-mΩ Hot-Short Response Time

11 Power Supply Recommendations

The TPS25200-Q1 device is designed for 2.7 V < V_{IN} < 5 V (typical) voltage rails. Although a V_{OUT} clamp is provided, it is not intended to regulate V_{OUT} at approximately 5.4 V with 6 V < V_{IN} < 7 V. This clamp is a protection feature only.

12 Layout

12.1 Layout Guidelines

- For all applications, a 0.1-µF or greater ceramic bypass capacitor between the IN and GND pins is recommended as close to the device as possible for local noise decoupling.
- For output capacitance, see Figure 16. A low-ESR ceramic capacitor is recommended.
- The traces routing the R_{ILIM} resistor to the device should be as short as possible to reduce parasitic effects on the current-limit accuracy.
- The thermal pad should be directly connected to PCB ground plane using wide and short copper trace.

12.2 Layout Example

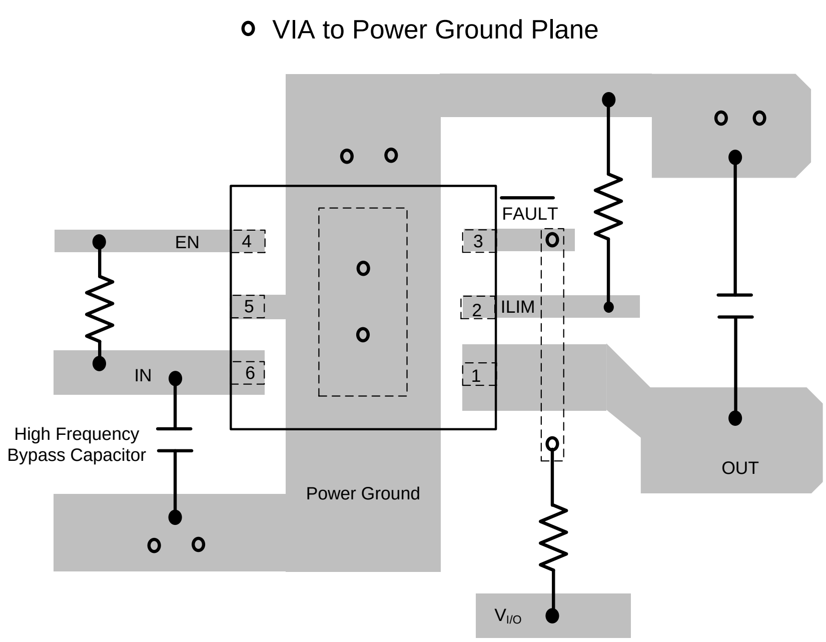


Figure 32. TPS25200-Q1 Board Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

TPS2553, *PRECISION ADJUSTABLE CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES*, SLVS841

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25200QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIL
TPS25200QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIL
TPS25200QDRVTQ1	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIL
TPS25200QDRVTQ1.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS25200-Q1 :

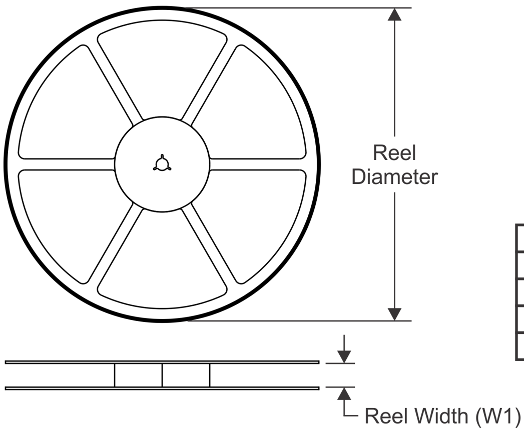
- Catalog : TPS25200

NOTE: Qualified Version Definitions:

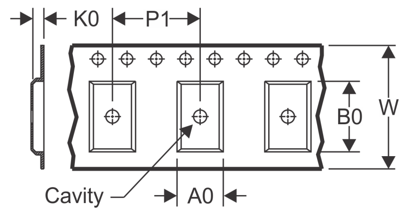
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

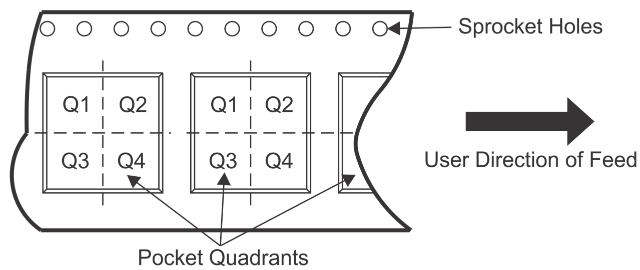


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

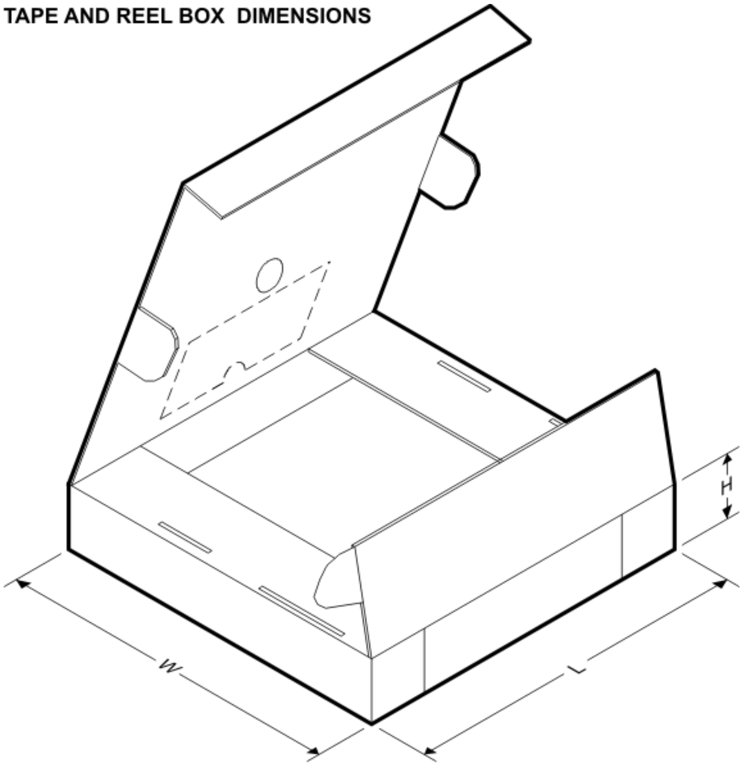
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25200QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25200QDRVTQ1	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

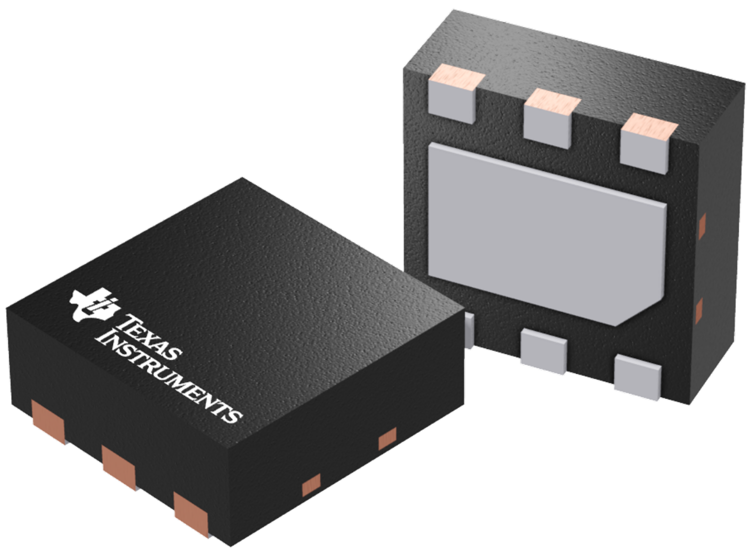


*All dimensions are nominal

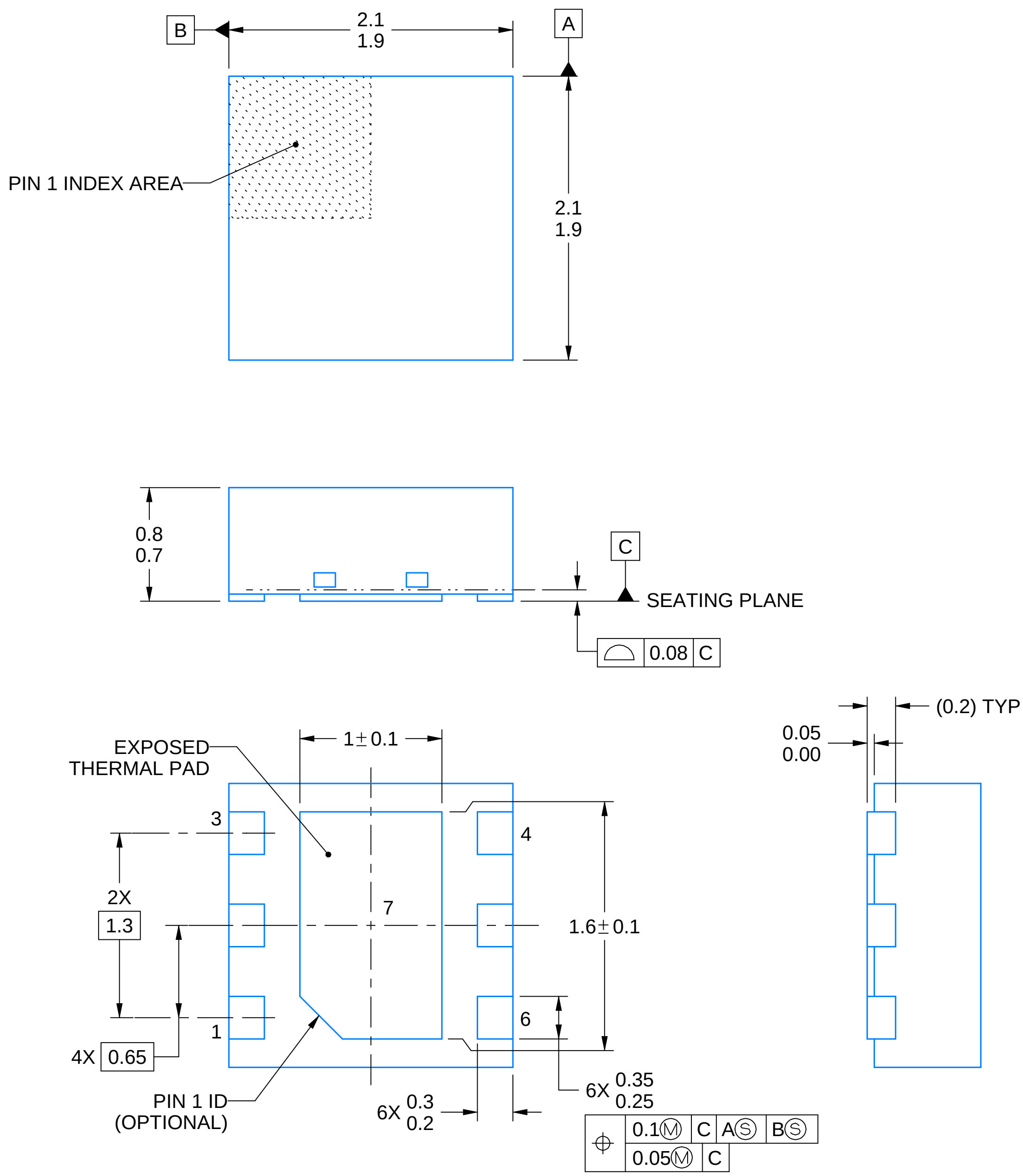
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25200QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS25200QDRVTQ1	WSON	DRV	6	250	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



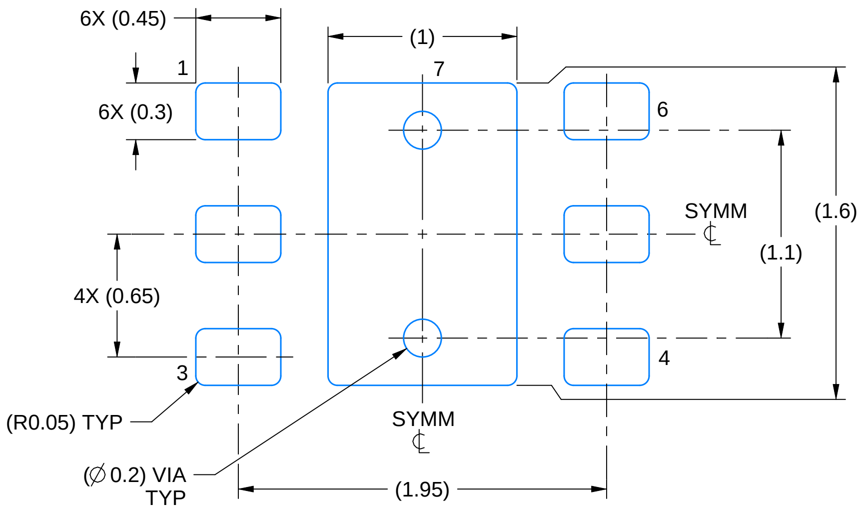
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



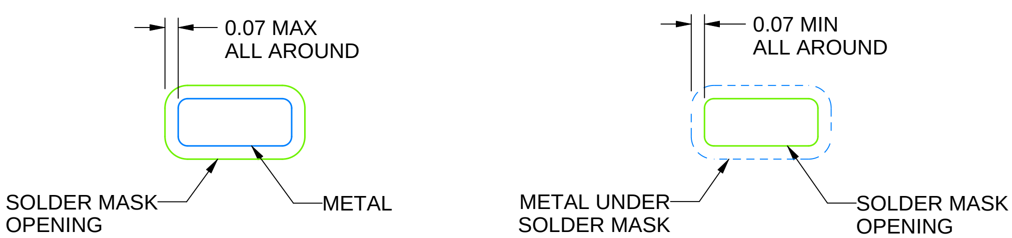
4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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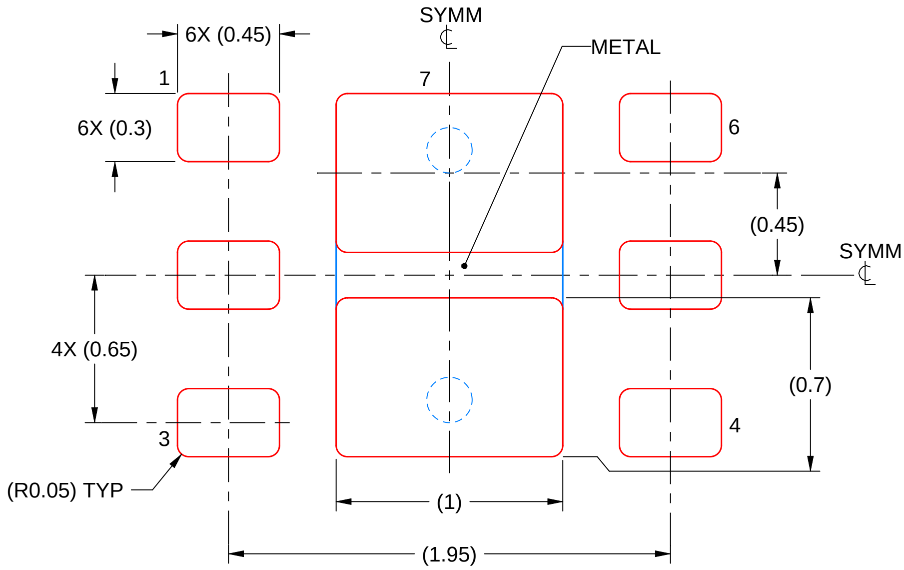
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.